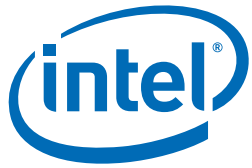

Consolidating Communications and Networking Workloads onto one Architecture

White Paper

Intel® Xeon® Processor

Equipment Platform Architecture

Communications Industry

An effective approach for reducing CapEx and OpEx

The explosion of global network traffic driven by consumer demand for mobile rich content anytime, anywhere, and the need to rapidly introduce new revenue generating services is driving service providers to carefully scrutinize future network capital expenditures (CapEx). At the same time, network infrastructure energy costs are spiraling higher and driving up operational expenditures (OpEx). Faced with increasing CapEx and OpEx, service providers are looking for telecom and networking solutions delivering both optimized cost/performance and energy efficiency.

How can telecom equipment manufacturers reduce their customers' CapEx and OpEx? Now, there's a compelling architecture that offers scalable platform choices for consolidating workloads on a single architecture that dramatically reduces development effort, power consumption and time to market. Traditionally, network elements run different workloads on different hardware architectures, like packet processing on network processors and control and application processing on general purpose processors. Today, all of these workloads can be consolidated onto a single architecture, thanks to the extraordinary performance gains from Intel® multi-core technology. Application, control plane and packet processing are already running on Intel® Architecture Processors. In addition, Intel is adding new instructions and optimized software libraries to further enhance signal processing performance and is on a path to deliver workload consolidation for application, control plane, packet and signal processing.

Workload consolidation lowers development costs by creating more software reuse opportunities and simplifying the tool chain, which boosts efficiency, reduces training time, decreases license fees and enables programmers to work on any system function. Moreover, moving to a single architecture eliminates many integration and validation issues, saving time and effort. If equipment manufacturers want to avoid hardware development altogether, they can use commercial, off-the-shelf (COTS) boards available from Intel's broad and experienced ecosystem.

Service providers will also benefit from lower OpEx, because Intel® processors optimize power consumption and lower the maintenance costs associated with managing complex multi-architecture systems. This white paper describes the high performance, low power consumption, development flexibility and time to market advantages equipment manufacturers can achieve by consolidating layers 1-7 onto Intel® architecture.

Data Plane Performance Highlights

The need for good data plane performance cuts across many communications and networking equipment types, including wireless base stations (BTS), radio network controllers (RNC), routers and switches, security appliances and streaming appliances. Table 1 lists the performance numbers, measured and projected, for different solutions. Today, systems based on Intel® Xeon® processor C5500 series (Jasper Forest) can achieve around 20 million packets per second (Mpps), and the next generation processor is expected to support around 50 Mpps. The details around these performance milestones are provided in the following sections and sidebars.

Timeframe	Function	Solution	Million packets per second (Mpps)	Gigabits per second (Gbps)
Today	Packet forwarding	Vyatta*	20	3
	Packet processing	Wind River*	21	12.2Δ
	Packet processing	6WIND*	24.6	16.5Δ
Future	Packet processing	Projections based on the next generation Intel® Xeon® processor	50*	33Δ

Table 1. Data Plane Performance Measurements (Δ is projected)

The Need for More Bandwidth

It's hard to overestimate future mobile data demand after seeing forecasts for mobile traffic. This is especially true for mobile video, the fastest growing segment, which is expected to make up 66 percent of the overall traffic in 2014[1] . Globally, mobile data traffic is forecasted to double every year through 2014, increasing 39 times between 2009 and 2014, as shown in Figure 1. To satisfy this growing appetite for data, service providers are relying on equipment manufacturers to find innovative and cost-effective ways to increase capacity, which often leads to re-architecting network elements to lower CapEx and OpEx.

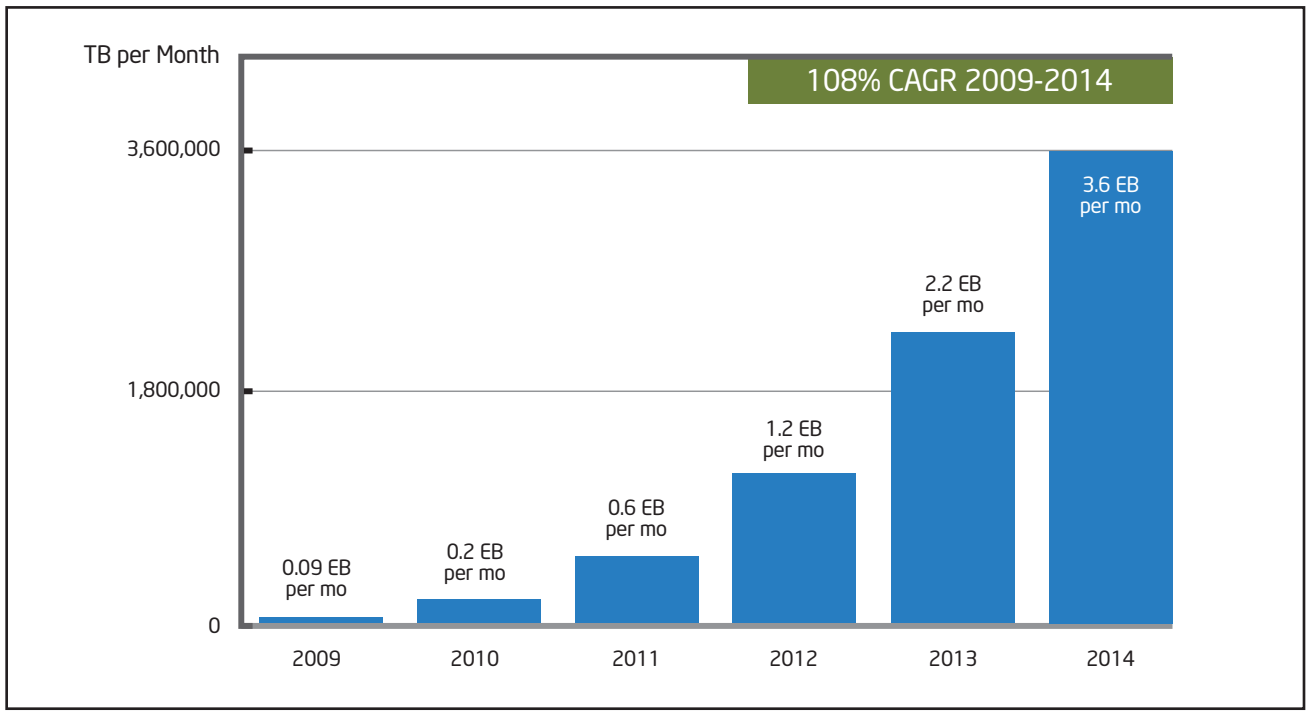

Figure 1 . Cisco* Forecast of Mobile Data Traffic (Source: Cisco, 2010[1])

[1] Source: Cisco* Visual Networking Index: Forecast and Methodology, 2009-2014 from February 9, 2010 found at http://www.cisco.com/en/US/solutions/collateral/ns341/ns525/ns537/ns705/ns827/white_paper_c11-520862.html.

Consolidating Diverse Workloads

Equipment development managers carefully review system partitioning options in order to select the software components and hardware architectures that best meet system requirements. When running diverse workloads on a network element (e.g., radio network controller (RNC)), there's a natural tendency to follow traditional methods and design in multiple hardware architectures. As a result, there can be as many as ten different hardware architectures running in a network, and this diversity complicates hardware and software design.

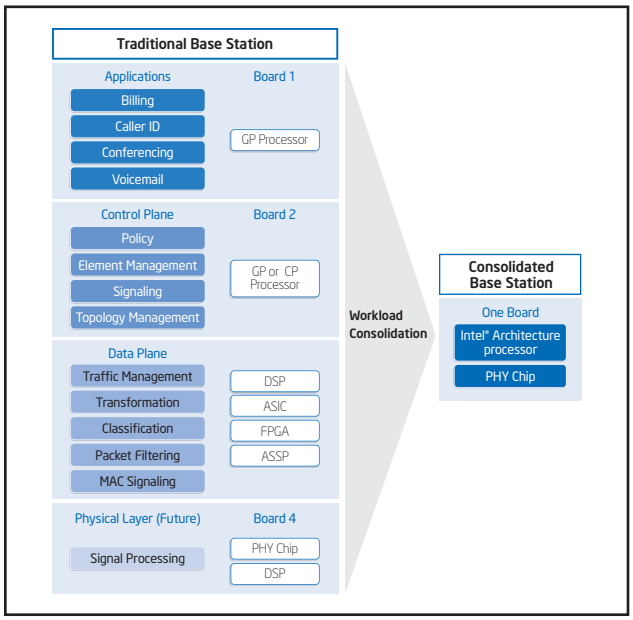

Figure 2. Base Station Functions Consolidated on an Intel® Processor

Within a base station alone, there are often various boards using a range of processing silicon, such as CPUs, NPUs, DSPs, FGPAs, ASICs and ASSPs, each requiring dedicated firmware and software. This system architecture invites inefficiencies with respect to component reuse, integration, inventory and ongoing compatibility, just to name a few areas. The alternative is using a single computing architecture for consolidating application, control plane and data plane workloads – all running on an Intel® multi-core processor-based platform (see Wind River* sidebar). This approach promotes the reuse of hardware and software components because it's relatively easy to apply them to new network elements or different Intel processors. Reuse can dramatically reduce development cost and improve time to market for equipment manufacturers, while simplifying the network architecture, which lowers maintenance cost for service providers.

Consolidation is now a practical option because the exceptional performance gains from multi-core processors are being applied to data plane workloads and producing impressive results. These are the same Intel processors that are routinely used for application and control plane processing, with the computing power needed to run large compute and data-intensive programs. For example, it's possible to run all three workloads on a single Intel multi-core processor, as illustrated in Figure 2, and satisfy WiMAX and eNodeB LTE base station throughput requirements. Taking integration one step further, Intel is adding capabilities to consolidate a fourth workload, Layer 1 signal processing, and efforts are underway to optimize its performance.

Wind River* Accelerates Packet Processing

Achieving a remarkable 21 million packets per second throughput (64 byte packets), Wind River* offers a Layer 2-7 solution running on an Intel® Xeon® Processor E5540 series using two of its four cores. As illustrated in Figure 3, the solution uses one or more processor cores to run control and applic ation level software using either Wind River Linux* or VxWorks*, while the other processor cores run a scaled-down real-time execution environment (Wind River Exec), which increases packet processing performance as much as six times over a full-featured operating system.

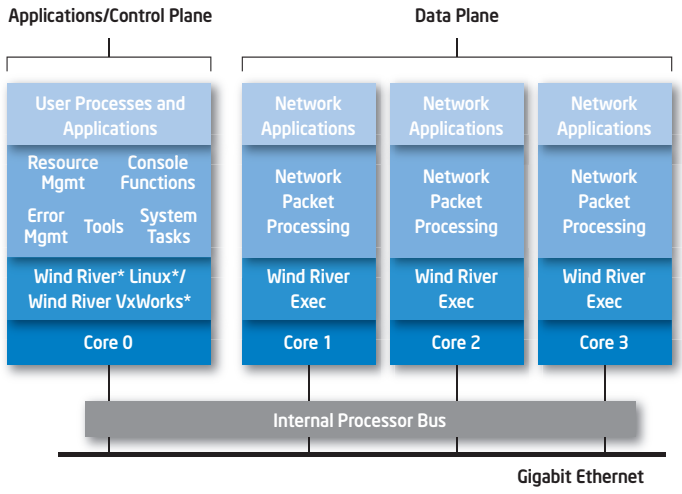

Figure 3. Wind River* Network Acceleration Platform

Advantages of Consolidating on Intel® Architecture

Intel® architecture offers a scalable family of code-compatible processors that cover top-to-bottom performance requirements, so manufacturers can create a range of products – even enter new markets – while leveraging software reuse. Manufacturers also benefit from a large ecosystem, supplying COTS boards, software components and industry-leading development tools, which reduces design effort and allows engineering resources to focus on value-added activities. In addition to these benefits, the following describes how consolidating workloads on Intel architecture can reduce software and hardware development costs and facilitate systems and operations optimization.

Reduce Software Development Cost

- **Work with one tool chain,** which makes it easier to observe workload interactions and identify bottlenecks
- **Assign programmers to any system function,** thereby increasing project management flexibility since there are no architectural barriers
- **Leverage a large software community** for open source code, BSPs and drivers, reducing the amount of code that needs to be written (see Vyatta* sidebar)
- **Protect software investments** by using Intel architecture processors that are truly software backwards compatible

Vyatta* Offers Open Networking Software

Delivering 20 gigabit-per-second (Gbps) bidirectional performance and over 3 million packets per second forwarding performance (Figure 4), Vyatta* software provides routing, firewall and VPN functionality suitable for large datacenters and service provider borders. Vyatta open networking software, combined with the Intel® Xeon® processor 5500 series, delivers networking capability at one-twentieth the price of proprietary alternatives. Furthermore, solutions can scale by just adding processor cores and network adapters. This router solution enables faster time-to-market, a scalable product family, and lower engineering and product costs.

In another study, Intel used a second open software product to demonstrate the ability to distribute routing workloads across multiple servers, yielding performance that scales linearly with the number of servers. This capability, called distributed soft routing, combined with Layers 4-7 services, like video processing, caching, policy serving and application acceleration, enables router manufacturers to expand functionality and increase the value of their solution.

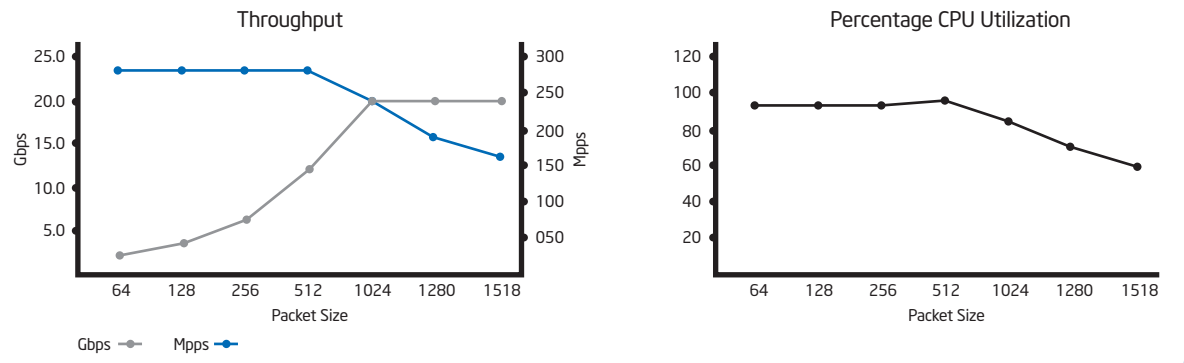

Figure 4. Vyatta* Bi-directional Packet-Forwarding Results

Reduce Hardware Development Costs

- **Design fewer boards** by adopting COTS solutions, thus minimizing design effort while using the latest processor technologies
- **Avoid integration and validation issues** created from melding together multiple hardware architectures, thus saving time
- **Design one platform for multiple applications** because it can run a variety of application software

Optimize Systems and Operations

- **Easily optimize systems** by repartitioning processor cores in software and putting computing power where it's needed (see 6WIND* sidebar)
- **Simply scale system performance** by adding processor cores to achieve different cost performance targets without impacting the code base
- **Increase system functionality** by consolidating multiple applications on a single piece of equipment (e.g., multiple radio standards – LTE, WiMAX), thus increasing the value of the solution
- **Reduce operations costs** because there are fewer boards to build, inventory, maintain and support

6WIND* Simplifies System Optimization

Achieving a performance of 24.6 Mpps with the EDS profile, 6WINDGate* is one of the fastest and most complete Layer 2 through Layer 7 software packet processing solution for Intel® Xeon® processors. It is specifically designed to simplify software development and minimize system design time using a Linux*-based control plane. The 6WINDGate enhanced development suite (EDS) profile addresses the full spectrum of multi-core design requirements, from one to any number of cores on one or multiple processors. In order to share CPUs, the fast path is implemented as a Linux kernel module between the Linux networking stack and the interface drivers, thus throughput is greatly increased because the Fast Path code scales from core to core and bypasses most of the overhead of the Linux kernel stack.

The 6WINDGate "SDS" profile will provide maximum packet processing performance. In multicore platforms configured with the SDS profile, the Fast Path runs under the Intel Data Plane Development Kit on multiple cores, maximizing the system's packet processing performance since most packets are processed within the fast path rather than being passed to the Linux stack. The Linux stack itself is configured to run on only as many cores as required (typically one), allowing all the remaining cores to be allocated to the fast path.

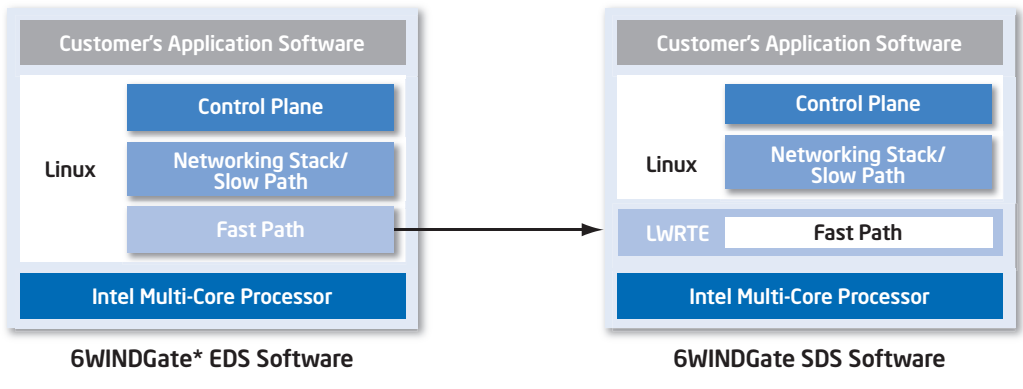

Figure 5. 6WINDGate* EDS and SDS Architectures

Path to Faster Packet Processing

Creating an environment where a general purpose multi-core processor is capable of reaching NPU-like packet processing throughput is no small feat. Intel has been developing this capability over several years and is committed to deliver faster packet processing with new product releases. The evolution towards faster data plane performance, with throughput projected to exceed 50 million packets per second (Mpps) for the next generation of processors, is illustrated in Figure 4. The following lists the enhancements made along the way.

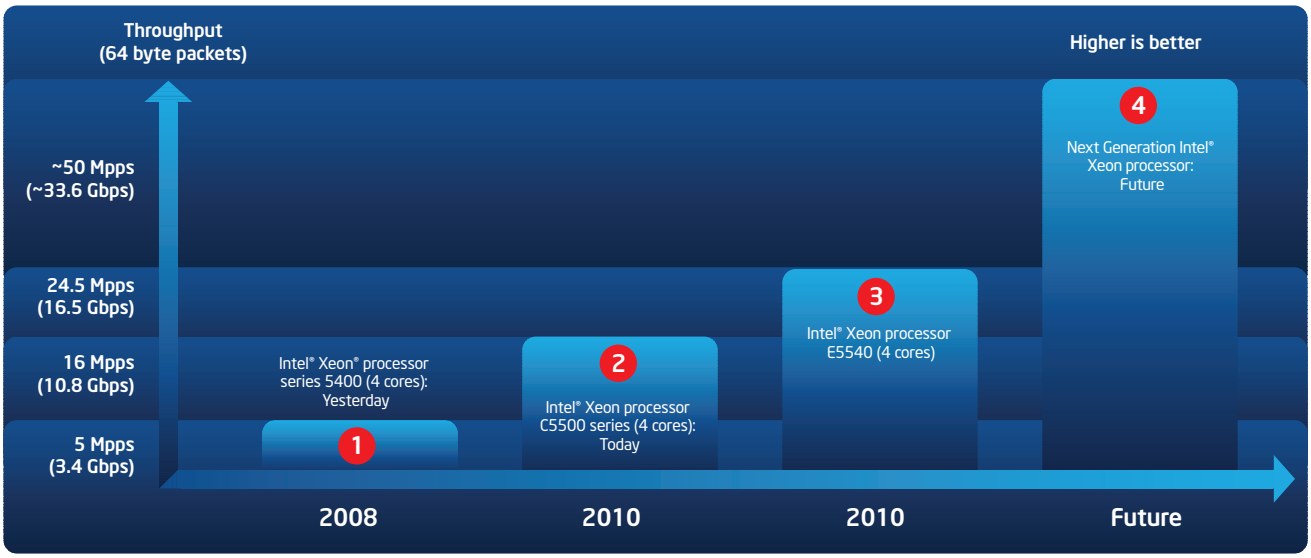

Figure 4. Packet Performance on an Intel® Processor

1 5 Mpps (3.4 Gbps) – Intel® Xeon® processor series 5400 (4 cores): Yesterday

Results are based on a standard Linux* network stack with a few optimizations:

- Enabled MSI interrupt mode
- Disabled processor hardware memory prefetchers
- Integrated the Intel® PRO/1000 GT Quad Port Server Adapter (i.e., NIC) with a NAPI-enabled driver

2 16 Mpps (10.8 Gbps) – Intel® Xeon processor C5500 series (4 cores): Today

Results are based on enhanced L3 forwarding software with the following modifications:

- Replaced sections of the Linux IP and forwarding stack with custom packet handling software
- Eliminated several Linux IP stack bottlenecks caused by spinlocks and the lack of multi-queue support
- Bypassed the Linux Kernel for packet processing (e.g., flow lookup and processing, descriptor bunching)
- Implemented new API (NAPI) mode soft interrupt mode that uses polling, a substitute for hard interrupts

3 35.7 Mpps (24 Gbps) – Intel® Xeon processor E5540 (4 cores)

Results are based on Intel Data Plane Development Kit prototype with the following features:

- A lightweight run-time environment, offering a low-overhead, run-to-completion model with high performance data plane packet processing
- Libraries for memory, queue and buffer management, providing fast, efficient and highly-optimized software functions to obtain outstanding performance
- Poll mode drivers, performing efficient packet operations with 1 and 10 gigabit Ethernet (GbE) NICs
- An environmental abstraction layer, handling hardware resource allocation requirements, which may differ between different deployment models (e.g., bare metal and Linux user space)

4 Greater than 50 Mpps – Next Generation Intel® Xeon processor: Future

Projected results are based on a new microarchitecture (see "Tick-Tock" in the next section) and the integration of Intel Data Plane Development Kit into commercial network stacks from 6Wind* and Wind River*.

The Intel Data Plane Development Kit, illustrated in Figure 5, is a BSD license software package, that will be available in the second half of 2010. The development kit does not include the software modules shown in the upper half of the figure (security, routing and wireless); however, they can be obtained from software vendors. The data plane development kit provides a good starting point for system developers at OEMs, ISV and EBMs; and fully featured, commercial solutions are expected shortly for solution providers.

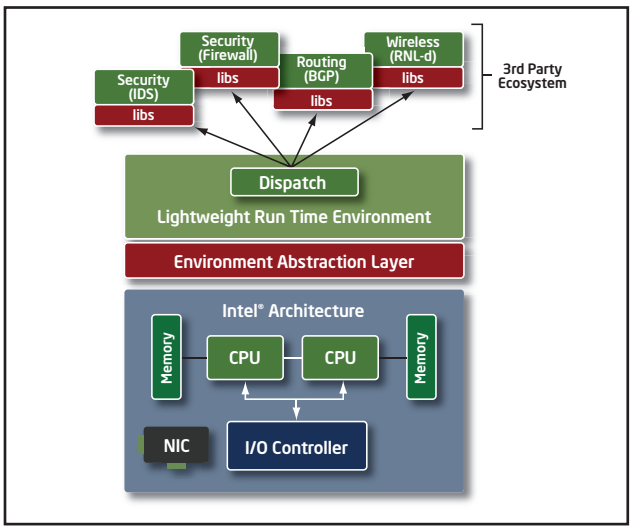

Figure 5. Intel Data Plane Development Kit

Lowering OpEx with Power-Efficient Intel® Processors

Developers who use Intel can count on getting the most advanced technology for future products on a reliable and predictable timeline. The timeline follows Intel's "Tick-Tock" model for ongoing innovation based on delivering new silicon process technology (Tick) one year, and an entirely new processor microarchitecture (Tock) the next year.

The results can be seen in the regular product launches by RadiSys*, a leading provider of application-ready software and hardware platforms for use in the communications industry. Figure 6 shows the increasing integer and floating point performance of four generations of single board computers. Most notable is the RadiSys Promentum* ATCA-4500, equipped with a single Intel® Xeon® processor L5518 (4 cores with Intel® Hyper-Threading Technology), that outperforms its predecessor, the RadiSys RMS420-5000XSL server with dual Intel® Xeon® processor L5408 (8 cores total). Based on this data, the Intel Xeon processor L5518 has 1.8 times better integer performance-per-watt, chip-for-chip, than the Intel Xeon processor 5408 (2.0 times better floating point)i. In addition, the Intel Xeon processor L5518 integrates the memory controller to further decrease board power consumption.

The Intel Xeon processor L5518 also offers automated energy efficiency enhancements, providing users with greater control of their energy consumption. This includes a processor idle power level of only 10 watts, enabling a 50 percent reduction[i,1] in system idle power compared to the previous generation. New integrated power gates, based on Intel's unique high-k metal gate technology, allow idle cores to power down independently.

The processor supports up to 15 automated operating states that take intelligent power to a new level. The states significantly increase power management flexibility by adjusting system power consumption based on real-time throughput and without sacrificing performance. With service providers focusing on utility costs, Intel's Tick-Tock model will continue to address the need for greater energy efficiency.

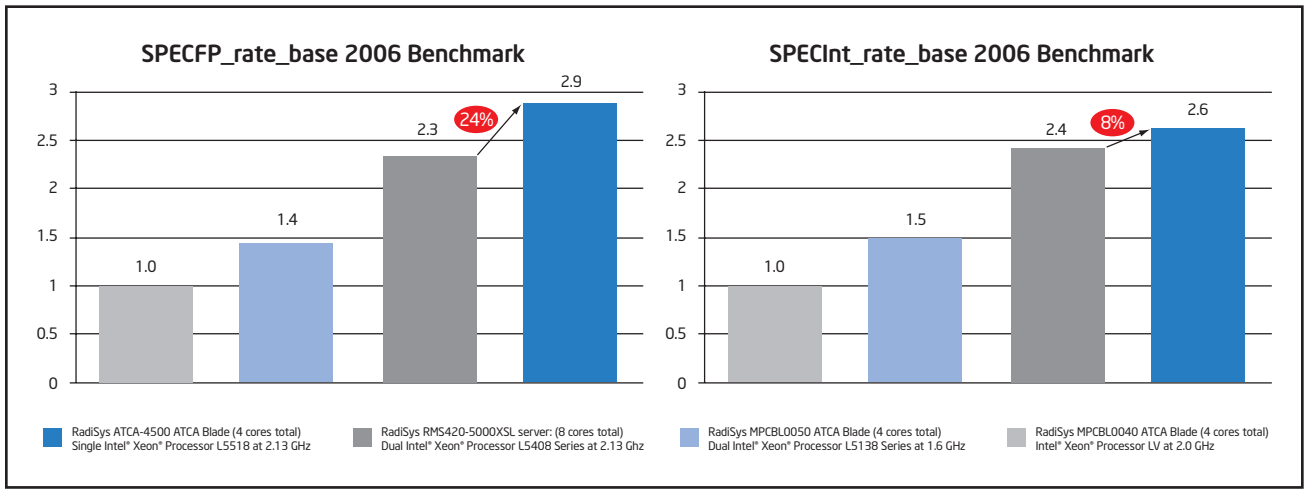

Figure 6. SPEC Performance Benchmark Results[i]

Integrating PCI Express* on the Processor

When saving board space and lowering power consumption are important, the Intel® Xeon® processor C5500/C3500 series, based on the Intel® microarchitecture codenamed Nehalem, delivers both. PCI Express* lanes, typically found in the I/O hub, are integrated into the processors, eliminating the need for a separate I/O hub chip. This decreases the total chip count by one and saves on overall system power, making it an ideal platform for thermally and space-constrained applications.

This new series offers unprecedented scalability, with single-core to quad-core options ranging from 23W to 85W thermal design power (TDP[2]). They are available in both uni-processor (Figure 7) and dual-processor configurations, via an Intel® QuickPath Interconnect, which provides even more design flexibility. Table 1 lists some of the telecom-oriented features supported by the Intel Xeon processor C5500/C3500 series, which vary by processor option.

"Intel's new generation of multicore CPU, the Intel® Xeon® processor C5500 series (Jasper Forest), with its excellent performance, has been chosen as the main processor for ZTE's next generation wireless equipment. Use of it will enable ZTE wireless systems to become more flexible and simpler with this consolidated architecture. It also achieves our goal of one common board for all Control, Data, Media and Applications, so that the ZTE next generation wireless equipment will have more flexible configuration, better performance and be more competitive in the market."

Xie DaXiong, Corporate Executive Vice President, Chief Technology Officer, ZTE Corporation

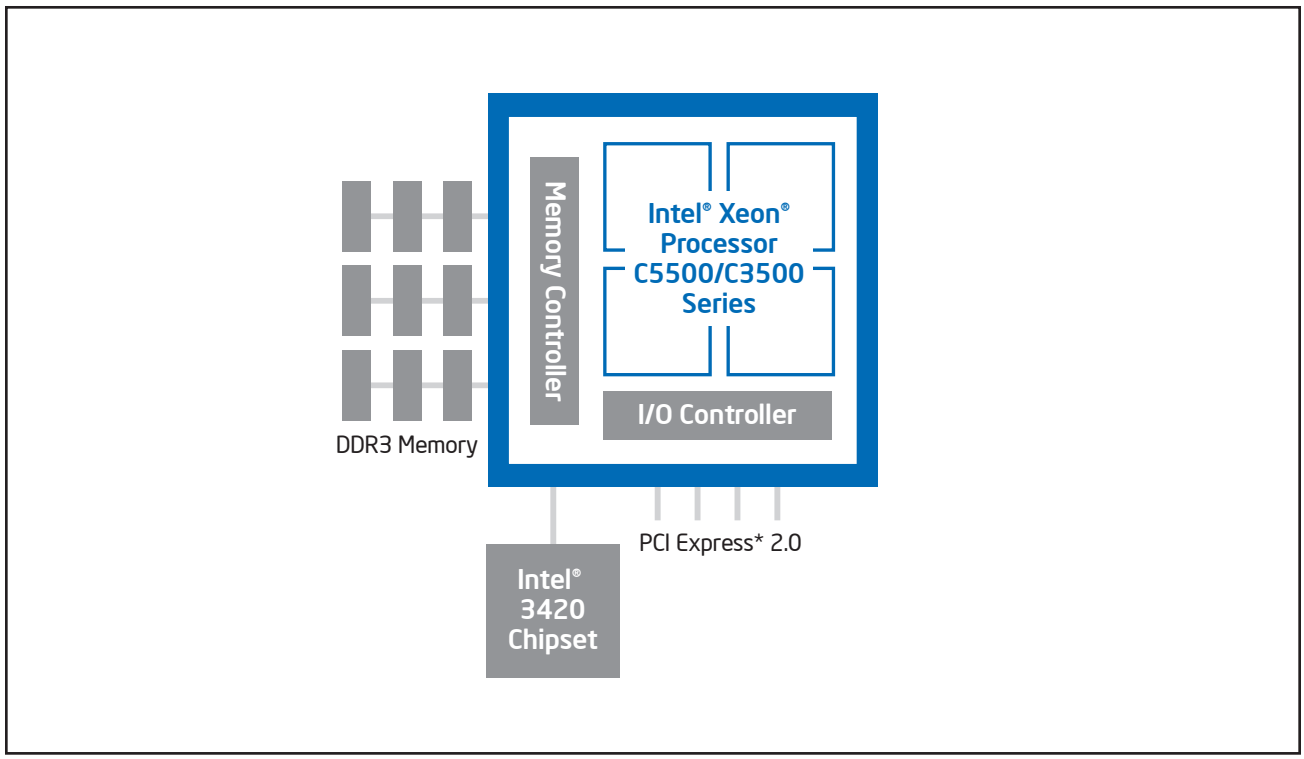

Figure 7. Single-socket configuration of Intel® Xeon® processor C5500/C3500 series-based platform

[2] TDP is the maximum amount of power the cooling system is required to dissipate.

Features of the Intel® Xeon® Processor C5500/C3500 Series	Benefits for Telecom Applications
Integrated PCI Express*	Lowers total system thermal design power and frees up board real estate.
Lowest power Intel® Xeon® processors (i.e., single-core Intel® Xeon® processor LC3518 at 23W; dual-core Intel® Xeon® processor LC3528 at 35W)	Meets requirements for NEBS Level 3 ambient operating temperature specifications (thermal profile).
Intel® Turbo Boost Technology[2]	Boosts performance for specific workloads by increasing processor frequency, thermal conditions permitting.
Intel® QuickPath Technology	Provides high-speed connections (up to 5.86 GT/s) between Intel processors when data is shared among processor cores.
Intel® Hyper-Threading Technology[3]	Delivers two processing threads per physical core for a total of eight threads, which dramatically speeds up decomposable applications, like packet processing.
Intel® Virtualization Technology[4]	Reduces virtualization overhead with hardware assist, thereby increasing the performance of telecom equipment running multiple operating systems.
Multi-level cache, including the addition of L3 (last-level) cache	Allows pipelined software (e.g., security processing) to efficiently share images between cores. Cache is dynamically allocated to the processing cores, in accordance to their workload.
Integrated Memory Controller	Offers memory performance up to 25.6 gigabytes per second for memory-hungry communications protocol encoding.

Table 1. Mapping Processor Features to Communications and Networking Applications

Reduce Complexity and Lower Design Cost

As service providers add network capacity to satisfy explosive demand in the near future, they will have a laser focus on CapEx and OpEx. In response, equipment manufacturers that lower their development costs can pass on some of the savings in order to create a competitive advantage in the market. Today, the extraordinary performance of multi-core Intel processors is creating a new opportunity: consolidating multiple networking workloads onto a single architecture. This architectural approach reduces hardware and software engineering effort, while benefiting from the ever-increasing performance-per-watt of Intel processor-based platforms. For designs using an assortment of NPUs, DSPs, FPGAs and ASICs, it may be time for a new approach that improves time to market and reduces complexity without sacrificing performance.

For more information

For more information on embedded Intel® processors, please visit
http://www.intel.com/embedded

[i] Performance tests and ratings are measured using specific computer systems and/or components and reflect the approximate performance of Intel® products as measured by those tests. Any difference in system hardware or software design or configuration may affect actual performance. Buyers should consult other sources of information to evaluate the performance of systems or components they are considering purchasing. For more information on performance tests and on the performance of Intel products, visit Intel Performance Benchmark Limitations: www.intel.com/performance/resources/benchmark_limitations.htm

[1] Configuration details for 50 percent lower idle power: Intel internal measurements of 221W at idle with Supermicro 2xE5450 (3.0GHz 80W) processors, 8x2GB 667MHz FBDIMMs, 1x700W PSU, 1x320GB SATA hard drive vs. 111W at idle with Supermicro software development platform with 2xE5540 (2.53GHz Nehalem 80W) processors, 6x2GB DDR3-1066 RDIMMs, 1x800W PSU, 1x150GB 10k SATA hard drive. Both systems were running Windows* 2008 with USB suspend select enabled and maximum power savings mode for PCIe* link state power management. Measurements as of February 2009.

[2] Intel® Turbo Boost Technology requires a PC with a processor with Intel Turbo Boost Technology capability. Intel Turbo Boost Technology performance varies depending on hardware, software and overall system configuration. For more information, see http://www.intel.com/technology/turboboost.

[3] Intel® Hyper-Threading Technology (Intel® HT Technology) requires a computer system with an Intel® processor supporting Intel HT Technology and an Intel HT Technology enabled chipset, BIOS, and operating system. Performance will vary depending on the specific hardware and software you use. See www.intel.com/products/ht/hyperthreaing_more.htm for more information including details on which processors support Intel HT Technology.

[4] Intel® Virtualization Technology (Intel® VT) requires a computer system with an enabled Intel® processor, BIOS, virtual machine monitor (VMM) and, for some uses, certain computer system software enabled for it. Functionality, performance or other benefits will vary depending on hardware and software configurations and may require a BIOS update. Software applications may not be compatible with all operating systems. Please check with your application vendor.

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