Logic Performance Evaluation and Transport Physics of Schottky-Gate III-V Compound Semiconductor Quantum Well Field Effect Transistors for Power Supply Voltages (V_{CC}) Ranging from 0.5V to 1.0V

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Abstract

In this paper for the first time, the logic performance of Schottky-gate $In_{0.7}Ga_{0.3}As$ QWFETs is measured and evaluated against that of advanced Strained Si MOSFETs from Vcc = 0.5 to 1.0V. The QWFET is shown to have measured drive current gain over the Si MOSFET for the entire Vcc range. Effective velocity (V_{eff}) of the QWFET exhibits 4.6X-3.3X gain over the Si MOSFET. The high V_{eff} enables 65% intrinsic drive current gain at V_{CC} = 0.5V and 20% gain at V_{CC} = 1.0V for the $In_{0.7}Ga_{0.3}As$ QWFET over that of Strained Si, despite 2.5x lower charge density.

Introduction

III-V compound semiconductor based quantum well field effect transistor (QWFET) has been proposed as a promising device candidate for future high speed and low power logic applications due to its high electron mobility [1-2]. At low operating voltage (Vcc) of 0.5V, the Schottky-gate $In_{0.7}Ga_{0.3}As$ QWFET has shown significant performance gain over strained silicon MOSFET [1-3]. There are at least two reasons why these devices should be evaluated at higher Vcc: (i) possible application to earlier logic technology nodes which use Vcc > 0.5V and (ii) flexibility for circuit applications that require multiple Vcc's at a given technology node. For the first time, the logic performance of Schottky-gate $In_{0.7}Ga_{0.3}As$ QWFETs is measured on the same test bench and evaluated against that of advanced Strained Si MOSFETs [4-5] over a wide range of Vcc from 0.5-1.0V. For logic applications it is essential to compare the performance of these devices at the same transistor off-state leakage (I_{off}). At constant I_{off}, it is shown that the $In_{0.7}Ga_{0.3}As$ QWFET has significant drive current gain over strained Si for the entire Vcc range. Also, effective carrier velocity (V_{eff}) measurements and temperature dependent studies are used to understand the device performance for Vcc from 0.5-1.0V.

Device Characterization and Benchmarking Metrics

The Schottky-gate $In_{0.7}Ga_{0.3}As$ QWFETs were grown and processed as described in [1] with remote delta doping (Si doping ~ 8e12/cm^2) and Pt gate electrode (Fig. 1). The TEMs in Figs. 2-3 show that the gate-to-QW channel separation is 5nm of $In_{0.52}Al_{0.48}As$ and that the physical gate length (L_G) of the $In_{0.7}Ga_{0.3}As$ QWFET is 80nm, respectively.

For rigorous logic performance comparison of the current $In_{0.7}Ga_{0.3}As$ QWFET and the Strained Si MOSFET (L_G=40nm) at different operating voltages (V_{CC}=V_{GS}=V_{DS}), correct benchmarking metrics must be used. To compensate for ~300mV difference in the threshold voltage (V_T) of the two systems, they are compared at equivalent gate overdrive (V_{GS}-V_T). In addition, the two devices have the same measured sub-threshold slope (SS) and drain induced barrier lowering (DIBL) at every drain bias (V_{DS}) used for all comparisons in this work. Fig. 4 depicts the drive current versus V_{GS}-V_T comparing the $In_{0.7}Ga_{0.3}As$ QWFET and the L_G=40nm Strained Si MOSFET at matched DIBL, SS, and I_{off} for V_{DS} of 0.05V, 0.5V, and 1.0V. Drive current is measured at the source side due to high gate-to-drain leakage in the Schottky-gate device. The $In_{0.7}Ga_{0.3}As$ QWFET exhibits 20-30% drive current gain over the Strained Si MOSFET for a wide range of V_{GS}-V_T in Fig. 5, despite higher external resistance (R_{EXT}) and the 2.5X lower intrinsic gate capacitance (C_{GI}) depicted in Fig. 6. The capacitance of the Si MOSFET is measured at 1 MHz on a long L_G device. Due to high gate leakage in the Schottky-gate QWFET, its intrinsic gate capacitance is extracted at RF with V_{DS} = 0.05V.

Measured (G_m) and intrinsic trans-conductance (G_{mi}) versus V_{GS}-V_T at V_{DS} = 0.5V for both devices are shown in Fig. 7. G_{mi} is extracted using [6]:

$$G_{m(i)} = \frac{G_m}{1 - G_m R_S - G_{DS}(R_S + R_D)}$$

where G_{DS} is the output conductance and $R_S + R_D$ are source and drain resistances. Peak G_{mi} for the $In_{0.7}Ga_{0.3}As$ QWFET exhibits significant gain compared to the Strained Si MOSFET. The table in Fig. 8 summarizes the key measured parameters at V_{CC} = 0.5V and 1.0V for both devices in this work.

Fig. 9 compares drive current for the QWFET and Si MOSFET with a constant V_T=0.2V. The secondary axis depicts the increasing I_{off} with increasing V_{DS} for both systems due to increasing DIBL effect. However, for logic applications, constant I_{off} is essential. Fig. 10 depicts measured drive current versus V_{CC} comparing $In_{0.7}Ga_{0.3}As$ QWFET and Strained Si MOSFET for constant I_{off} = 100 nA/μm. $In_{0.7}Ga_{0.3}As$ QWFET exhibits drive current gain over strained Si MOSFET for all V_{CC}, with greater gains (35%) at lower Vcc.

Intrinsic Device Performance and Transport

The V_{eff} of both devices is extracted using [7]:

$$v_{eff(i)} = \frac{I_{dsat(i)}}{\int_{V_T}^{V_{GS}} C_{GI}\, dVg} = \frac{\int_{V_{Tsat}}^{V_{GS}} G_{mi}\, dVg}{\int_{V_T}^{V_{GS}} C_{GI}\, dVg}$$

where $Id_{sat(i)}$ is the intrinsic drive current per unit width and V_{Tsat} is $V_T + \Delta V_T$ due to DIBL effect at high V_{DS}. The comparison of V_{eff} in Fig. 11 shows that the $In_{0.7}Ga_{0.3}As$ QWFET has 4.6X to 3.3X gain over Strained Si from V_{CC}= 0.5V to 1.0V. The V_{eff} gain in the QWFET more than overcomes the 2.5X lower gate charge (n_s) shown in Fig. 12. The lower n_s in the QWFET is due to a combination of lower effective mass and thicker gate insulator. Fig. 13 shows that V_{eff} lowering at high Vcc (Fig. 11) is not due to the increasing V_{DS}. Figs 14-15 show temperature dependence of G_m of the QWFET from -50C to 200C at V_{DS}=0.05V and at V_{DS}=0.5V, respectively. Both phonon and surface roughness scattering are evident and indicate that the current $In_{0.7}Ga_{0.3}As$ QWFET does not operate in the ballistic regime. Fig 15 suggests that the lower V_{eff} and G_m roll-off at high V_{CC} are due in part to these scattering mechanisms.

Intrinsic drive current ($q*n_s*V_{eff}$) of the $In_{0.7}Ga_{0.3}As$ QWFET is shown to have 65% performance gain at Vcc = 0.5V and 20% gain at V_{CC} = 1.0V over that of Strained Si (Fig. 16). As a result of higher drive current achieved at a lower n_s, Fig. 17 shows that the QWFET achieves 1.5-2X improvement in intrinsic gate delay over the Strained Si MOSFET despite having a longer L_G. Fig. 18 shows drive current versus Vcc for (i) Strained Si as measured, (ii) $In_{0.7}Ga_{0.3}As$ QWFET as measured, and (iii) $In_{0.7}Ga_{0.3}As$ QWFET with matched R_{EXT} to Strained Si and 50% reduction upper InAlAs barrier thickness as simulated, which requires the insertion of high K gate dielectric. The simulation predicts 45% and 85% drive gain over the Strained Si MOSFET for V_{CC} = 1.0V and 0.5V respectively.

Conclusions

For the first time the logic performance of Schottky-gate $In_{0.7}Ga_{0.3}As$ QWFETs is measured and evaluated against that of advanced Strained Si MOSFETs from Vcc = 0.5 to 1.0V at constant I_{off}. It is shown that the L_G=80nm III-V QWFET has measured drive current gain over L_G=40nm Strained Si for the entire Vcc range despite higher R_{EXT} and lower n_s, with more significant gain at lower Vcc (35% gain at 0.5V). The gain is due to the >3X higher V_{eff} of the current III-V QWFET over Strained Si, despite the presence of phonon and surface roughness scattering as indicated by temperature dependence studies. The $In_{0.7}Ga_{0.3}As$ QWFET shows significantly improved gate delay over the Strained Si MOSFET for all V_{CC} despite 2X longer L_G. At constant I_{off}, III-V QWFET shows intrinsic drive current ($q*n_s*V_{eff}$) gain from 20% (Vcc=1V) to 65% (Vcc =0.5V) over Strained Si, making it a high-performance logic device over the entire Vcc range of interest for logic applications.

References

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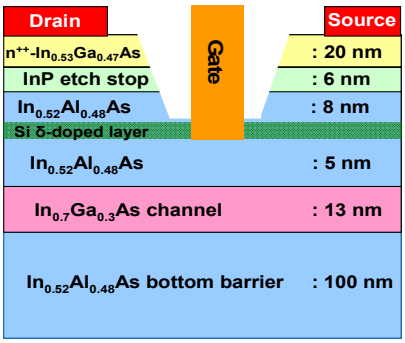

Fig 1: Schottky-gate $In_{0.7}Ga_{0.3}As$ QWFET with remote delta doping (Si doping ~ 8e12/cm^2) and Pt gate electrode. This entire structure was integrated onto Si substrate as described in ref. [1].

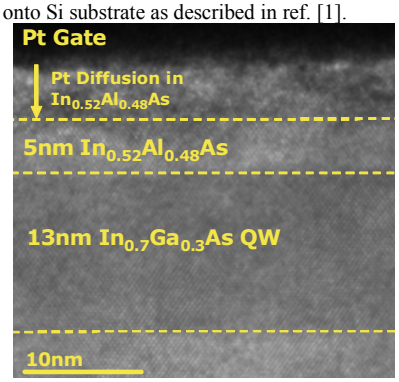

Fig 2: TEM micrograph of $In_{0.7}Ga_{0.3}As$ QWFET stack showing the Pt gate and Pt diffusion into $In_{0.52}Al_{0.48}As$ upper barrier using thermal anneal. The final Pt gate electrode is 5nm above the $In_{0.7}Ga_{0.3}As$ QW channel.

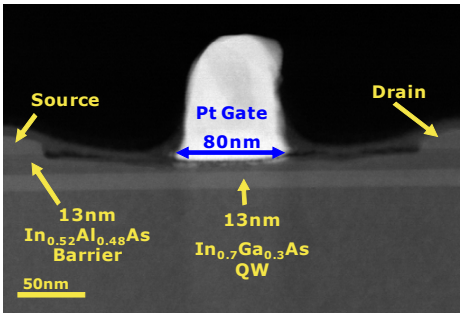

Fig 3: TEM micrograph of $In_{0.7}Ga_{0.3}As$ QWFET showing transistor physical gate length (L_G) = 80nm.

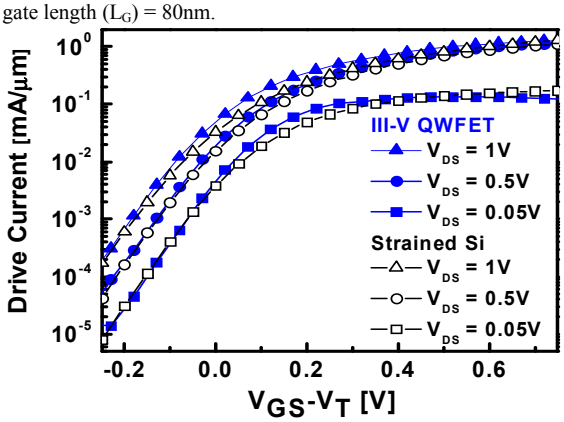

Fig. 4: Drive current (measured at source end) versus gate overdrive (V_{GS}-V_T) comparing the $In_{0.7}Ga_{0.3}As$ QWFET (L_G=80nm) and Strained Si MOSFET (L_G=40nm) at matched DIBL, SS, and I_{off} for V_{DS} of 0.05V, 0.5V, and 1.0V.

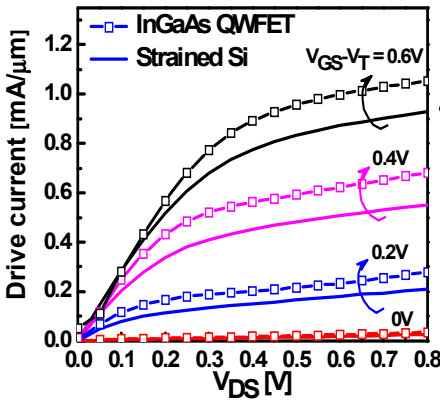

Fig 5: Measured drive current versus drain voltage (V_{DS}) comparing the 80nm $In_{0.7}Ga_{0.3}As$ QWFET and 40nm Strained Si MOSFET at matched DIBL, SS and I_{off}. $In_{0.7}Ga_{0.3}As$ QWFET exhibits 20-30% drive current gain over Strained Si MOSFET for a wide range of V_{GS}-V_T.

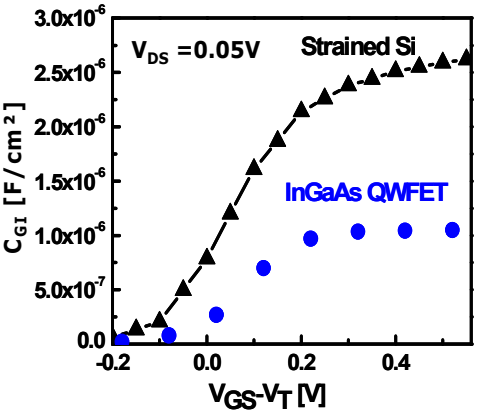

Fig 6: Intrinsic gate capacitance (C_{GI}) versus (V_{GS}-V_T) comparing the $In_{0.7}Ga_{0.3}As$ QWFET and the Strained Si MOSFET. The capacitance for the III-V QWFET is extracted from RF measurements instead of standard 1MHz measurement due to high gate leakage.

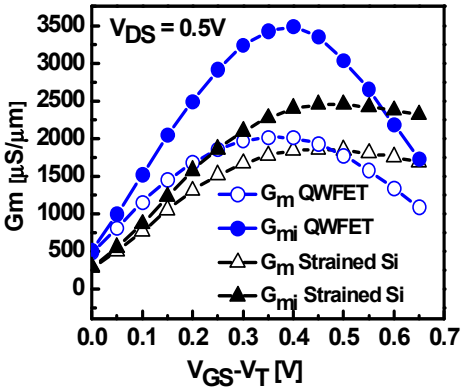

Fig 7: Measured G_m and intrinsic G_{mi} versus V_{GS}-V_T at V_{DS} = 0.5V for 80nm $In_{0.7}Ga_{0.3}As$ QWFET and 40nm Strained Si MOSFET. Excluding external resistance, peak G_{mi} of the $In_{0.7}Ga_{0.3}As$ QWFET exhibits significant gain compared to the strained Si MOSFET. The G_{mi} roll-off at high V_{GS}-V_T for $In_{0.7}Ga_{0.3}As$ QWFET will be discussed (Figs. 13-15).

	V_{DS}	V_{GS}-V_T	L_G	R_S+R_D	DIBL	SS	C_{GI} @ V_{DS} = 0.05V	Peak G_m	Peak G_{mi}
	[V]	[V]	[nm]	[Ω-μm]	[mV/V]	[mV/dec]	[μF/cm²]	[μS/μm]	[μS/μm]
InGaAs QWFET	0.5	0.3	80	320	135	95	1.02	2013	3488
Strained Si	0.5	0.3	40	195	135	95	2.45	1859	2451
InGaAs QWFET	1	0.8	80	320	130	102	1.04	2082	3560
Strained Si	1	0.8	40	195	128	101	2.57	2007	2615

Fig 8: Table of key measured parameters comparing L_G = 80nm $In_{0.7}Ga_{0.3}As$ QWFET and L_G = 40nm Strained Si MOSFET for both V_{DS}= 0.5V and 1.0V.

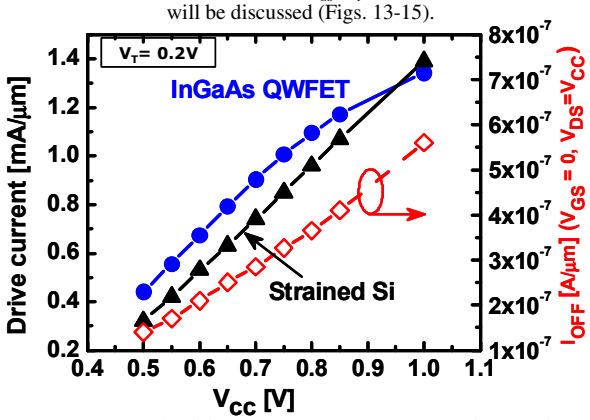

Fig 9: Measured drive current versus operating voltage (V_{CC}=V_{GS}=V_{DS}) comparing 80nm $In_{0.7}Ga_{0.3}As$ QWFET and 40nm Strained Si MOSFET for constant V_T of 0.2V. Secondary axis shows increasing transistor off state leakage as a function of V_{CC} for both the QWFET and the MOSFET due to DIBL effect as V_{DS} increases.

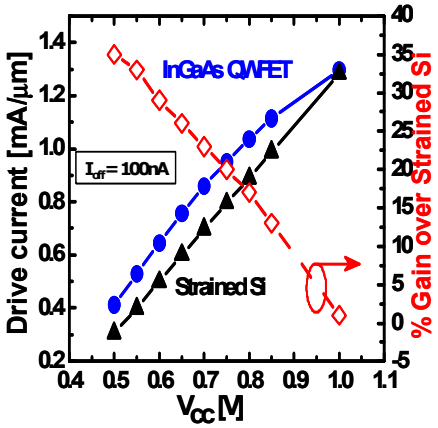

Fig 10: Measured drive current versus operating voltage (V_{CC}) comparing 80nm $In_{0.7}Ga_{0.3}As$ QWFET and 40nm Strained Si MOSFET for constant I_{off} = 100 nA/μm. Despite 2.5X lower capacitance and 60% higher R_S+R_D, $In_{0.7}Ga_{0.3}As$ QWFET exhibits drive current gain over strained Si MOSFET for all V_{CC}, with greater gains at lower Vcc.

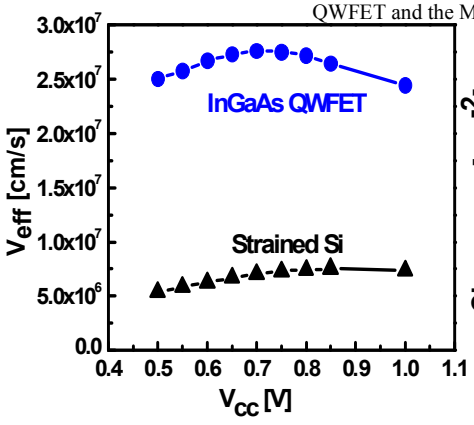

Fig 11: Extracted effective carrier velocity (V_{eff}) versus operating voltage (V_{CC}) comparing 80nm $In_{0.7}Ga_{0.3}As$ QWFET and 40nm Strained Si MOSFET at constant I_{off} = 100 nA/μm. $In_{0.7}Ga_{0.3}As$ QWFET exhibits 3.3X-4.6X gain in V_{eff} over Strained Si MOSFET for the V_{CC} range of interest for logic applications.

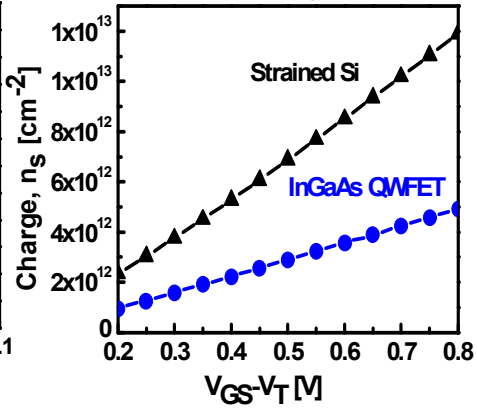

Fig 12: Gate charge (n_s) determined from C_{GI} versus gate overdrive (V_{GS}-V_T) comparing $In_{0.7}Ga_{0.3}As$ QWFET and Strained Si MOSFET.

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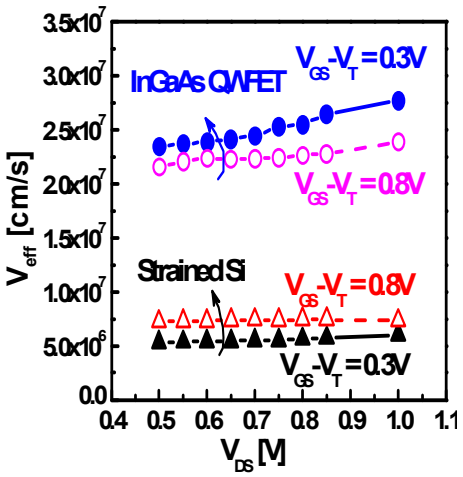

Fig. 13: Effective carrier velocity (V_{eff}) as a function of V_{DS} for $In_{0.7}Ga_{0.3}As$ QWFET. The data shows that V_{eff} does not degrade with increasing lateral field (i.e.V_{DS}) for both high and low vertical field (i.e.V_{GS}-V_T).

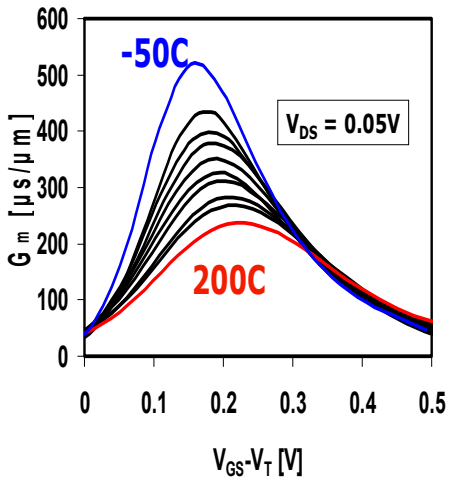

Fig. 14: Temperature dependence of transconductance of the 80nm $In_{0.7}Ga_{0.3}As$ QWFET at V_{DS}=0.05V from -50C to 200C for V_{GS}-V_T = 0 to 0.5V. The data indicates that $In_{0.7}Ga_{0.3}As$ QWFET is not operating in the ballistic regime because G_m degrades with increasing temperature at low vertical field. The data also indicates that both phonon and surface roughness scattering are important.

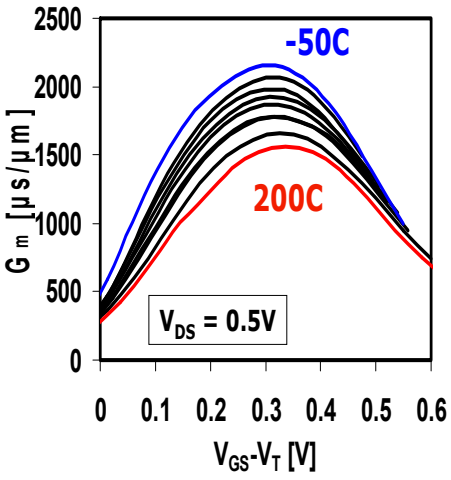

Fig. 15: Temperature dependence of transconductance of the 80nm $In_{0.7}Ga_{0.3}As$ QWFET at V_{DS}=0.5V from -50C to 200C for V_{GS}-V_T ranging from 0 to 0.5V. At high V_{DS} both phonon and surface roughness scattering are important, with the former being dominant.

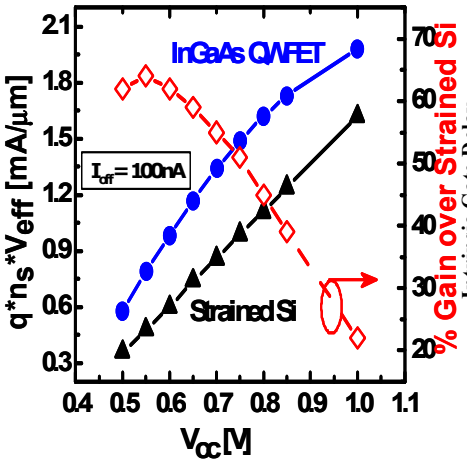

Fig. 16: Intrinsic drive current $I_{dsat\ (i)}$=q*n_s*V_{eff} versus Vcc comparing 80nm $In_{0.7}Ga_{0.3}As$ QWFET and 40nm Strained Si MOSFET at constant I_{off} = 100nA/μm. The data shows significant performance gain for the $In_{0.7}Ga_{0.3}As$ QWFET over Strained Si MOSFET for Vcc ranging from 0.5V(65% gain) to 1.0V(20% gain).

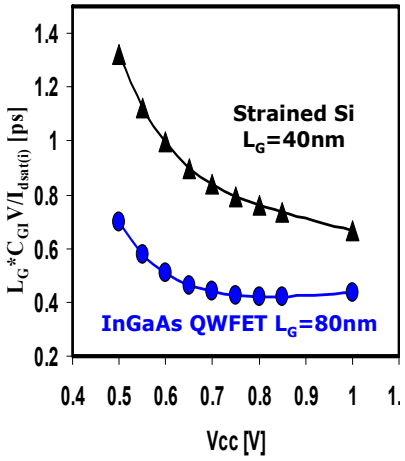

Fig 17: Intrinsic Gate Delay ($C_{GI}V/I_{dsat(i)}$) versus operating voltage comparing $In_{0.7}Ga_{0.3}As$ QWFET and Strained Si MOSFET for constant I_{off}=100 nA/μm. The $In_{0.7}Ga_{0.3}As$ QWFET shows significantly improved gate delay over the Strained Si MOSFET for all V_{CC} despite 2X longer L_G.

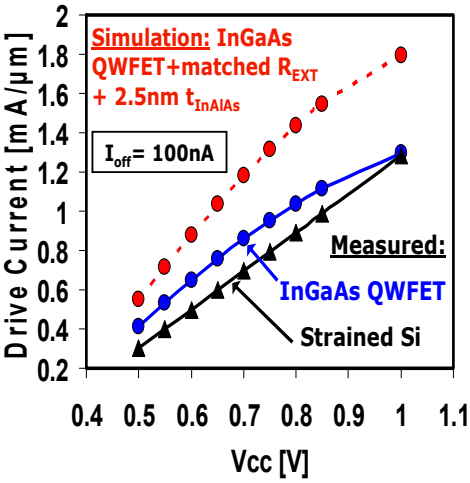

Fig 18: Drive current versus Vcc for (i) Strained Si as measured, (ii) InGaAs QWFET as measured, and (iii) InGaAs QWFET with matched R_{EXT} to Strained Si and 50% reduction in upper InAlAs thickness as simulated. The ultra thin upper InAlAs barrier in (iii) will result in excessive gate leakage current which requires the insertion of high K gate dielectric.