RF CMOS Technology Scaling in High-k/Metal Gate Era for RF SoC (System-on-Chip) Applications

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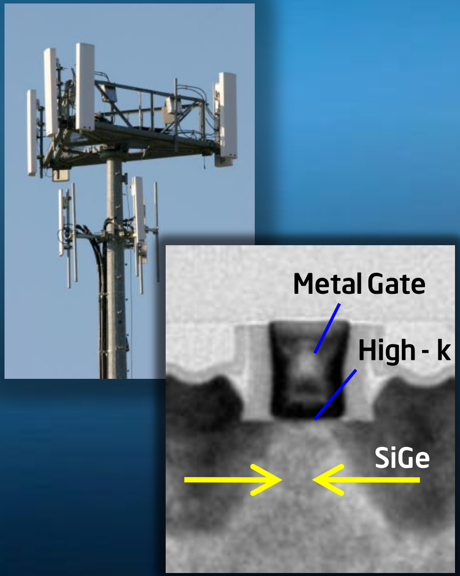


Outline

- Introduction - RF SoC and RF CMOS
- CMOS Scaling Trend
- RF CMOS Scaling
- RF CMOS Designs – PA, LNA, Wireless Transceivers
- Conclusions

SoC and RF SoC (Radio Frequency System-on-Chip)

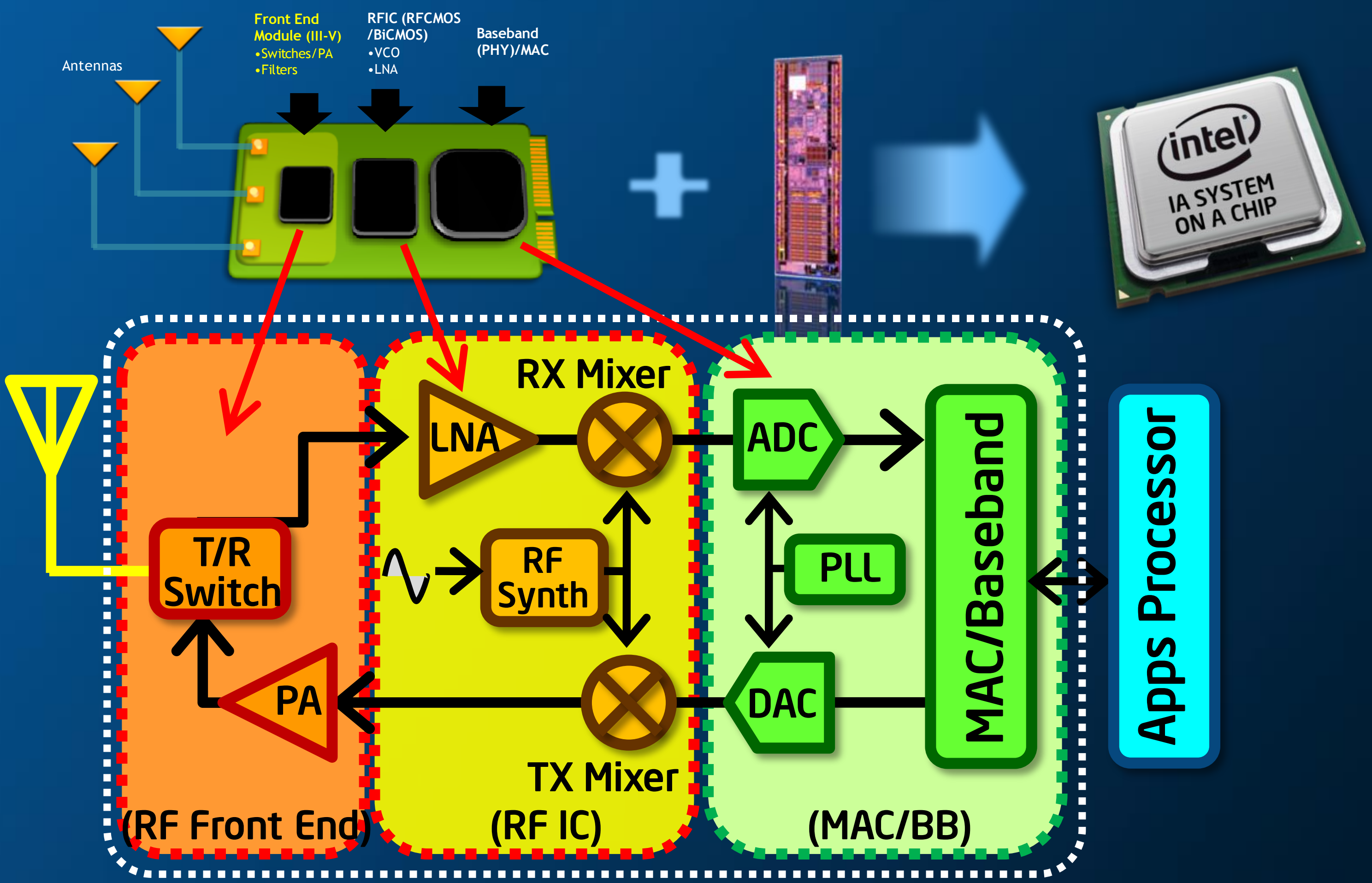
Server
Desktop
Laptop
CPU

Nettop/Netbook
MID
DTV
Embedded
Pocket Device
SoC

60 GHz
Satellite
Terrestial Broadcast
Blue Tooth
RF SoC

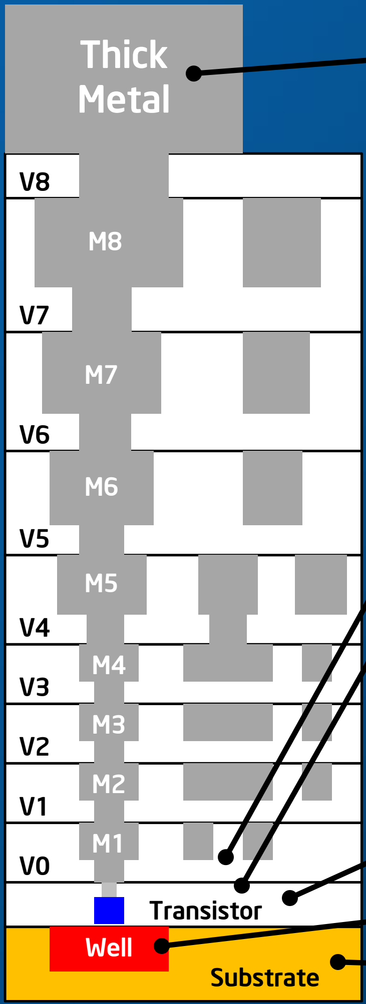
RF SoC → SoC derivatives with integrated RF and communication IPs

RF SoC - RF Systems Integration



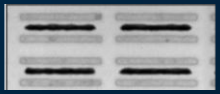
- Integration of RF subsystem into an advanced CMOS platform
- Is CMOS scaling capable of meeting RF system requirements ?

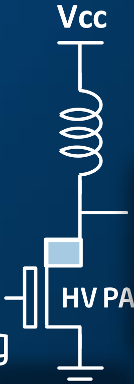
32 nm RF CMOS Technology

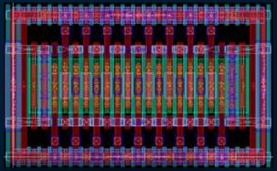


- TM1 Inductor: high Q and density

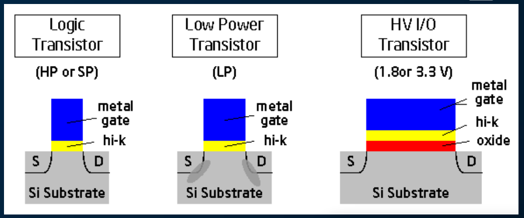
- Passives:
  - Precision Resistor
  - High Q Inductor
  - High Density Decap

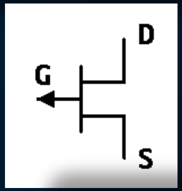


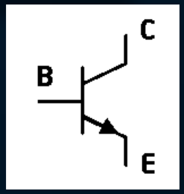




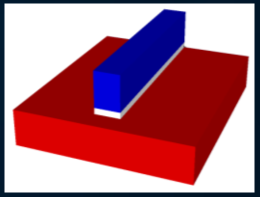
- HV PA Transistor
- RF Transistor: Templates/Modeling





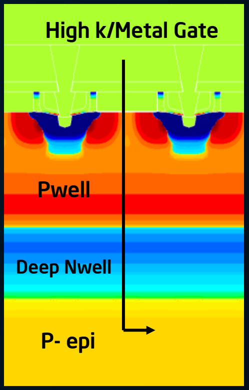


- Transistor:
  - Logic, low power, I/O
  - JFET, BJT



- Well: Triple Well/Deep Nwell
- Substrate: High Resistivity

RF Models



Basic 32 nm CMOS technology is expanded with many more mixed signals/RF features to meet RF SoC requirements

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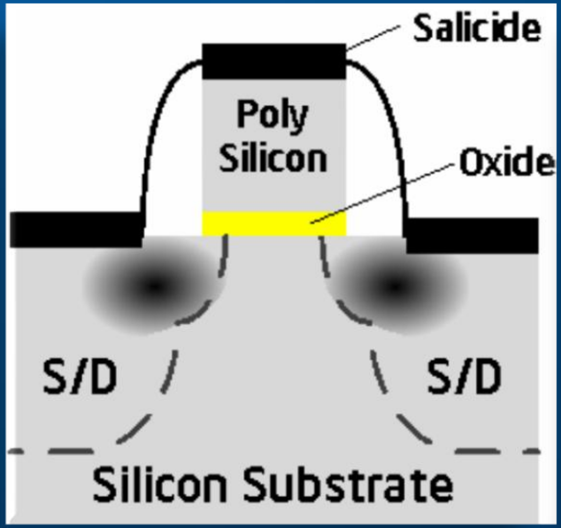
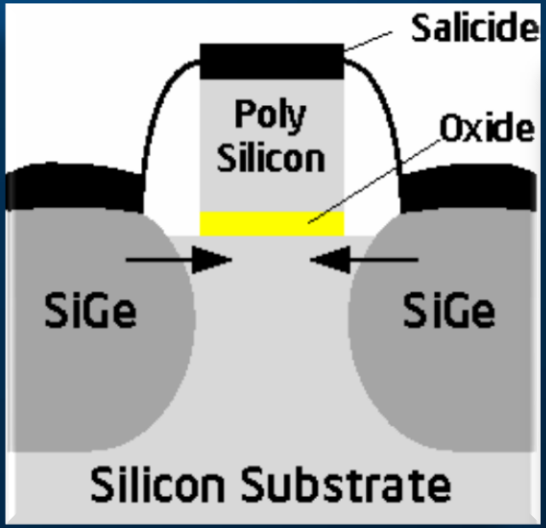
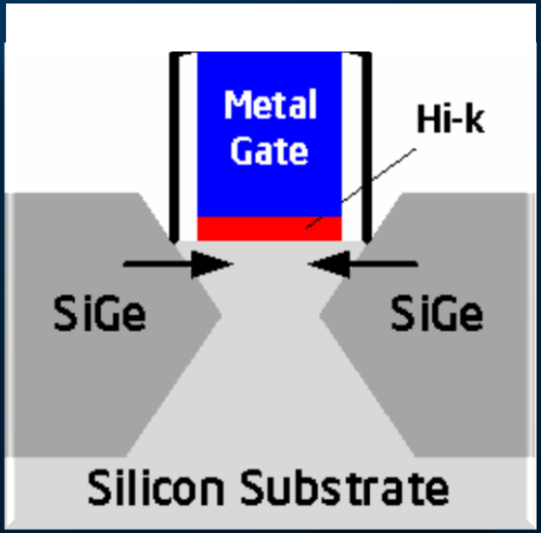
Intel CMOS Transistor Architecture Evolution in the Last Decade

.13 um and before	90nm/65 nm	45 nm/32 nm
Traditional	Strained Silicon	High k/Metal Gate + Strained Silicon

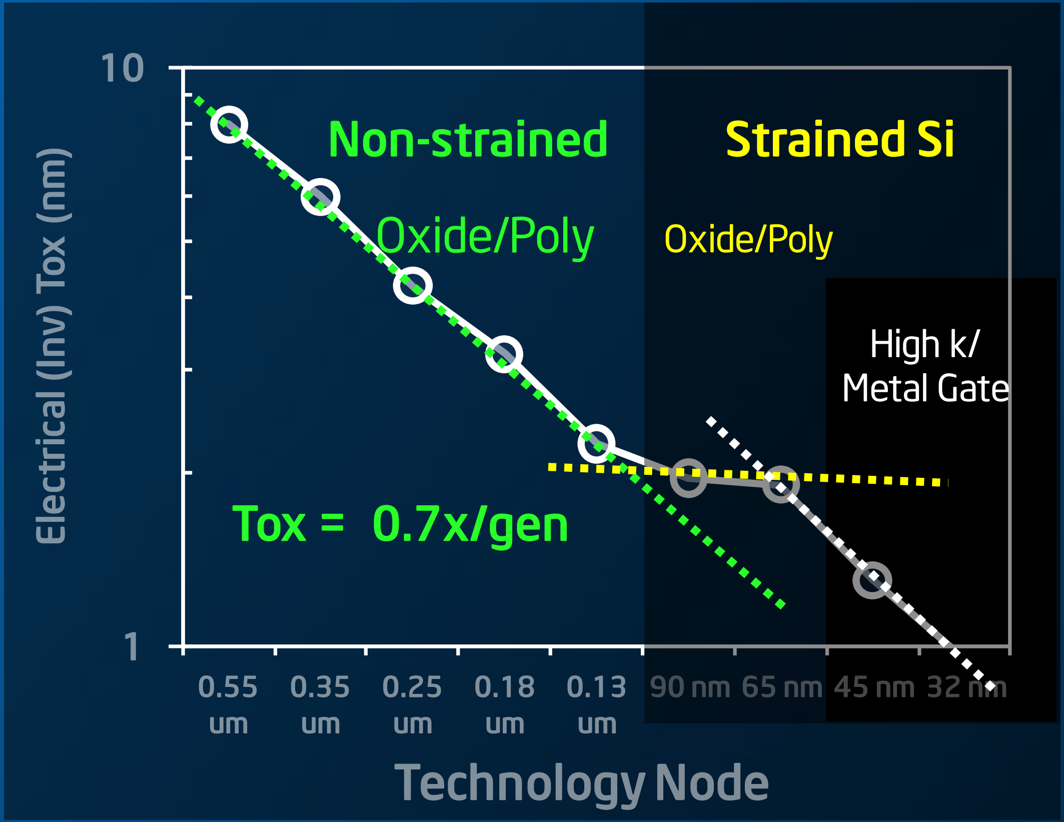


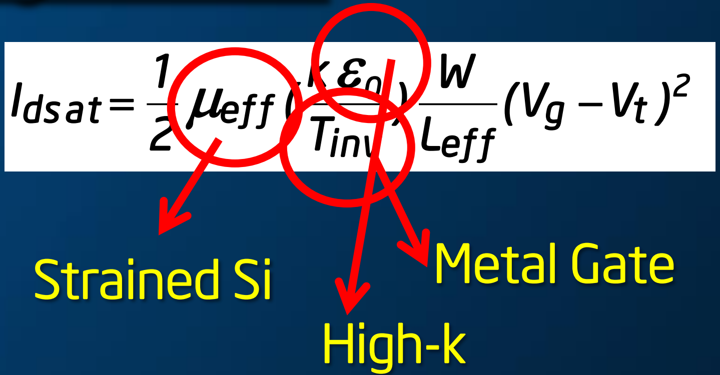




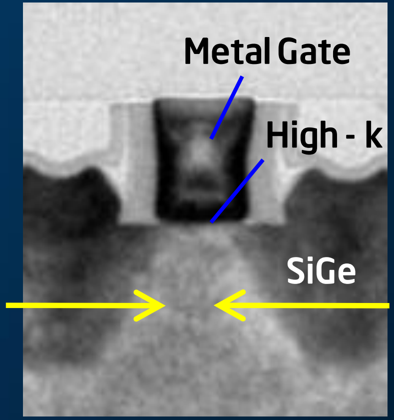
CMOS scaling has evolved from classical dimensional scaling to modern scaling with innovations in structures and materials

CMOS Scaling Challenges - Cox



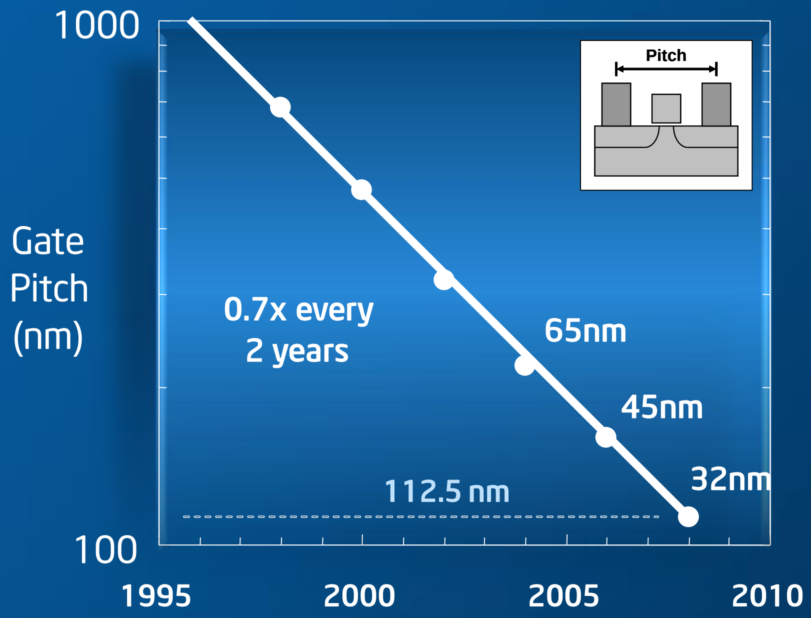


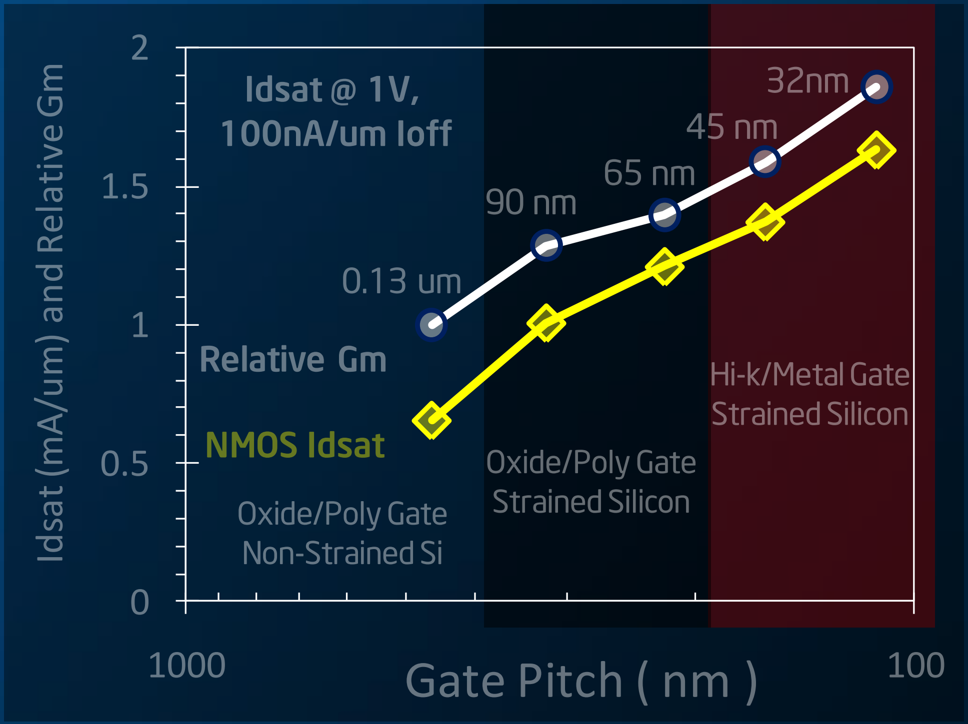
$$I_{dsat} = \frac{1}{2}\mu_{eff}\left(\frac{\kappa\varepsilon_0}{T_{inv}}\right)\frac{W}{L_{eff}}(V_g - V_t)^2$$



- Constant field oxide scaling not sustainable beyond .13 um (high gate leakage)
- Strained silicon implementation at 90 nm compensated the lack of Tox scaling
- Hi-k/metal gate implementation at 45 nm recovered Tox scaling

Moore's Law Continues on CMOS ……





Innovations of strained silicon and high k/metal gates enabled Moore's law scaling with continuous ~ 30% /gen. performance/gm enhancement

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RF CMOS Technology Performance Metrics

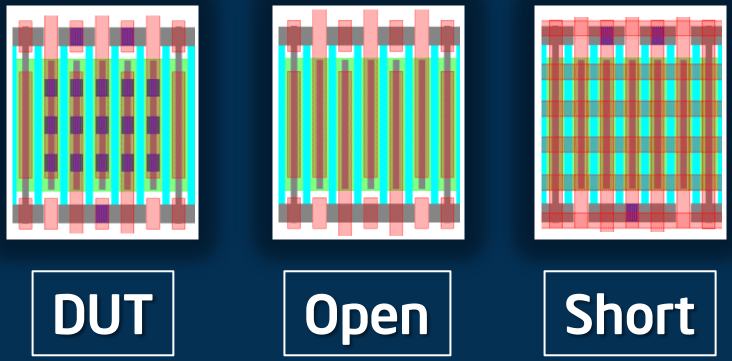
- RF CMOS scaling focuses on a different set of performance metrics (f_T, noise, Q factor and so on) from basic CMOS technology

RF Devices	RF Circuits	Key Device Characteristics
Logic Transistor	MAC/BB, ADC, DAC	I_{dsat}, I_{dlin}, V_t, I_{off}
Analog Transistor	ADC, DAC, MAC/BB	Gm, Rout, Matching, Linearity, Noise, NF_{min}
RF Transistor	PA, Mixer, T/R Switch	f_T, f_{max}, 1/f Noise, NF_{min}
PA Transistors	PA	Ron, Linearity, f_T, f_{MAX}, Efficiency, Breakdwn V,
Precision Resistors	ADC, DAC, BB Filter, others	R, σR/R, Matching
Linear Capacitors	PLL, VCO	C, Q, Matching
Varactors	PLL, VCO	Tuning Ratio, Q, Kv_{CO},
Inductor/ Transformer/Balun	PA, LNA, Mixer	L, Q

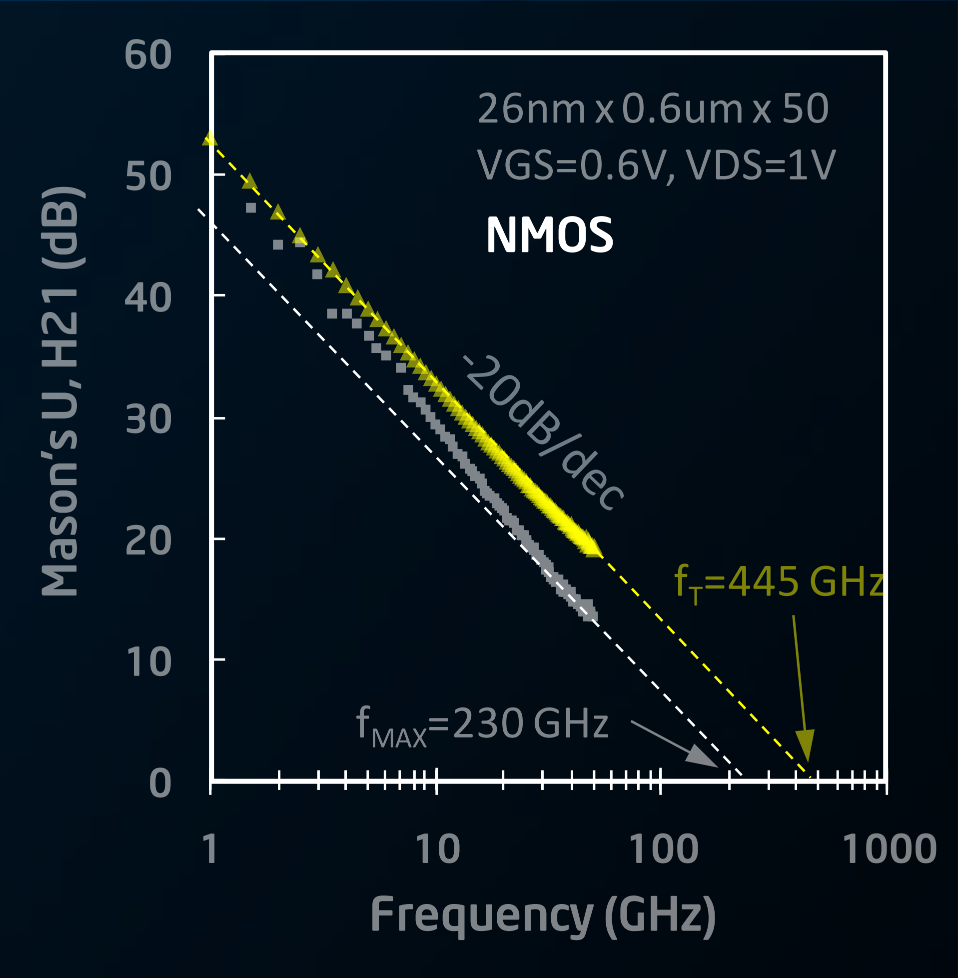
What are the impacts of CMOS scaling on these metrics ?

32 nm RF CMOS Cut-off Frequency f_T – 445 GHz !

De-embeding Structures

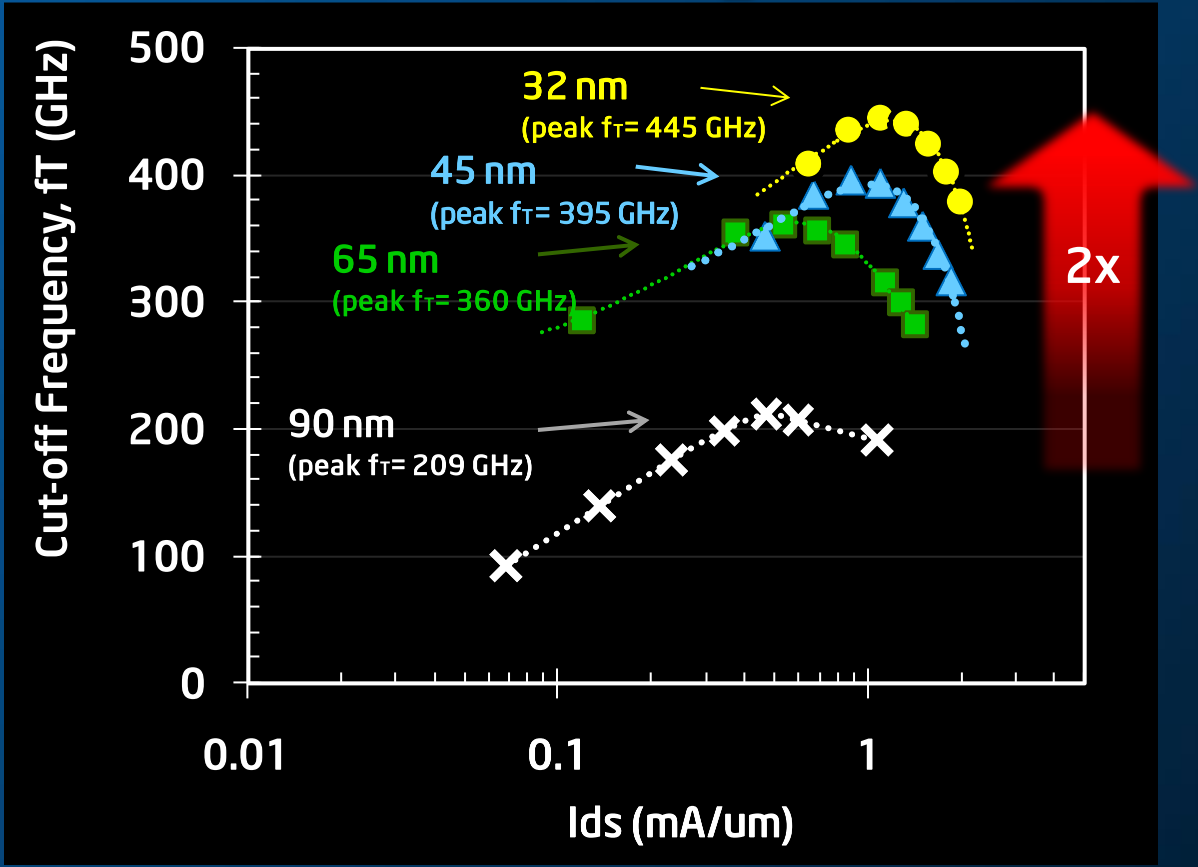


- De-embedded to M1 (inlcuded)
- 7% faster than previous result from g_m improvement



A new 32 nm NMOS RF CMOS record 445 GHz f_T achieved

RF Cut-off Frequency f_T Scaling Trend

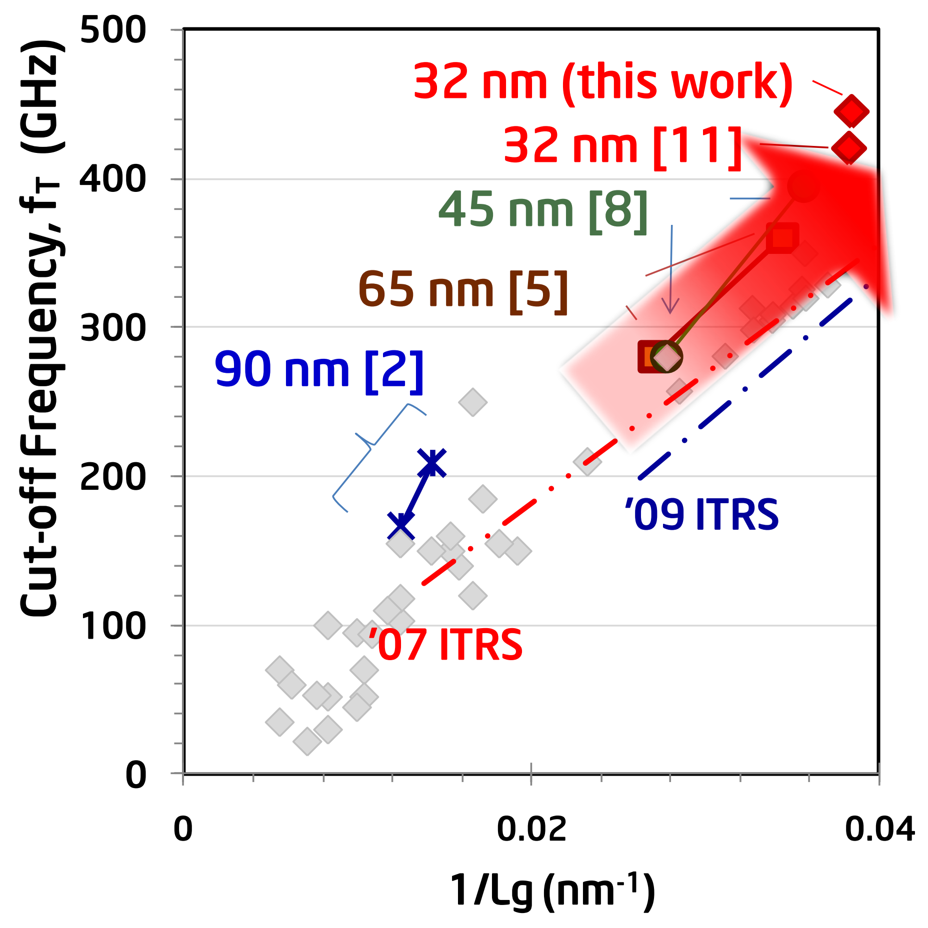


Cut-off frequency f_T started from 200 GHz at 90 nm, to 360 GHz at 65 nm, to 395 GHz at 45 nm (HK/MG), to the new record of 445 GHz at 32 nm HK/MG

CMOS Scaling on RF - Cut-off Frequency f_T

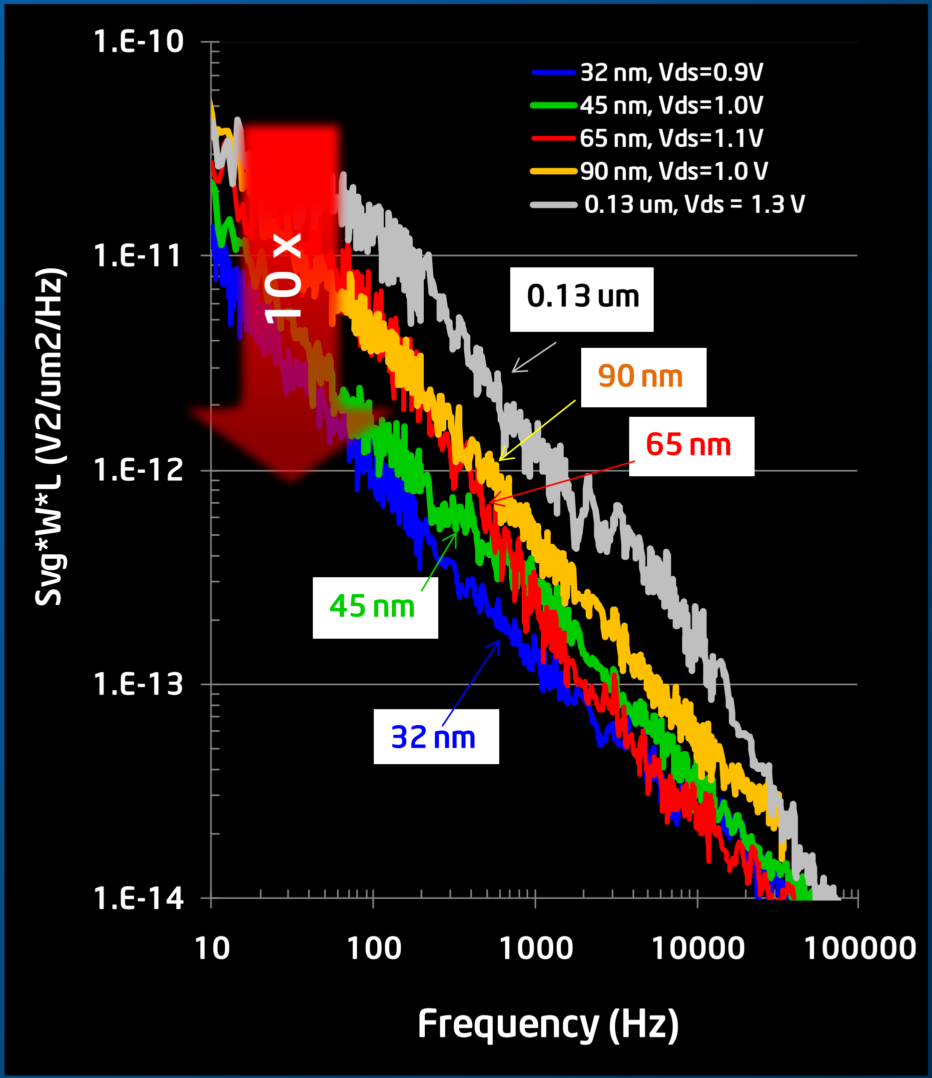
$$f_T = \frac{g_m}{2\pi C_{gg}}$$

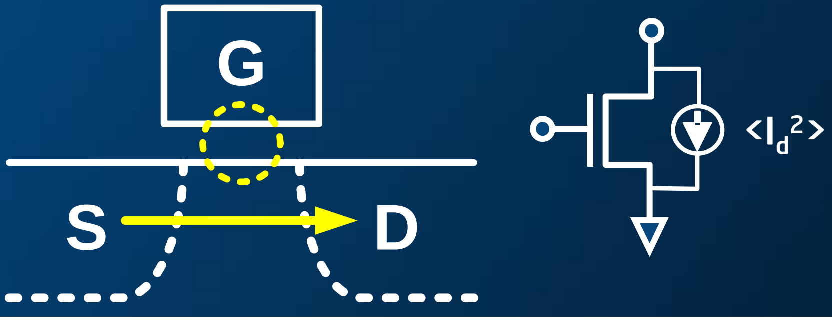
- Record f_T 445 GHz, closing gaps to SiGe HBT and III-V devices
- f_T improvement ~ 20-30% per gen
- g_m improvement dominating (thanks to CMOS technology scaling !)
- Cgg effects somewhat mixed
- Parasitics and layout optimization critical for future scaling



[2] K. Kuhn et al., VLSI Technology Symp., p. 224 (2004)
[5] I. Post et al, IEDM Tech Dig., pp. 1-3 (2006)
[8] C.-H. Jan et al, IEDM Tech. Dig., pp. 637-640 (2008)
[11] P. VanDerVoorn et al, VLSI Tech. Symp., p. 137 (2010)

CMOS Scaling on RF - 1/f Flicker Noise



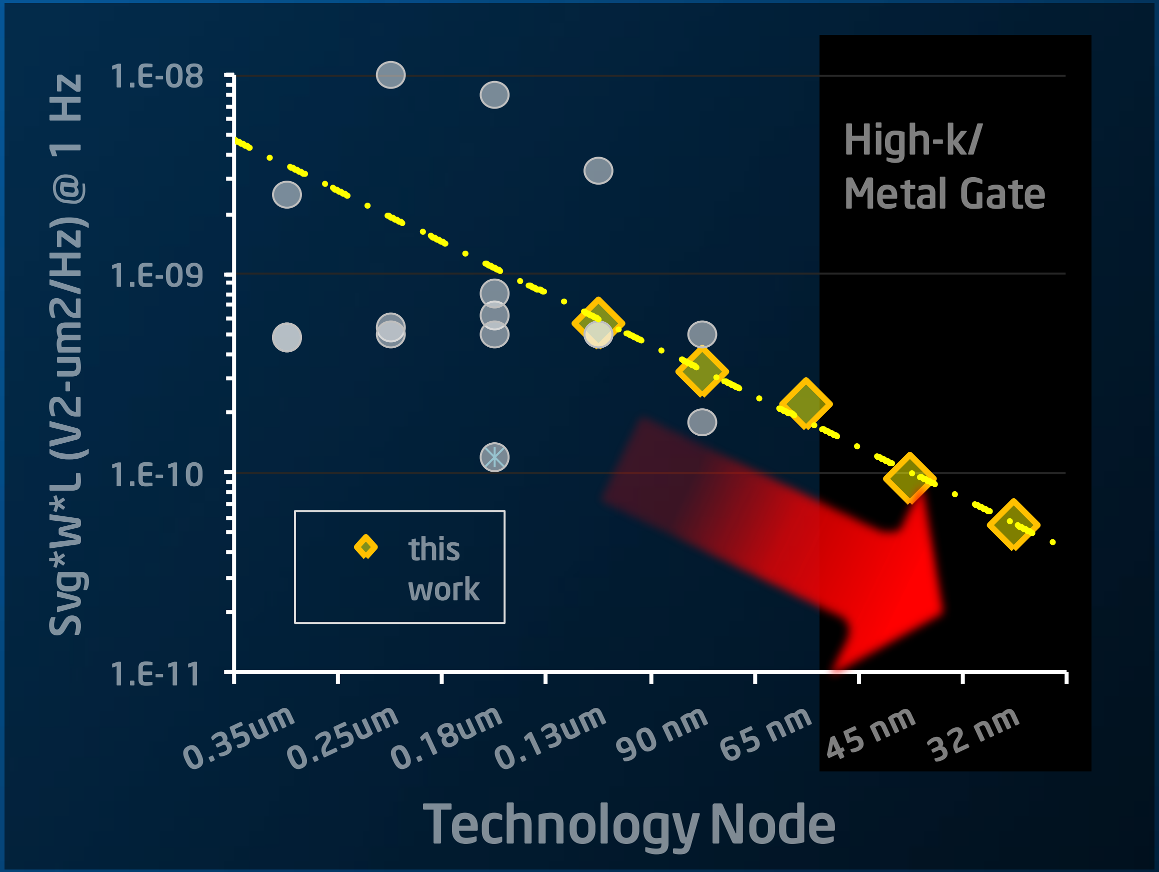


$$S_{Id} = \frac{k\cdot T\cdot I_d^2}{\gamma\cdot f\cdot W\cdot L}\left(\frac{1}{N}+\alpha\mu\right)^2 N_t(E_{fn}) = \frac{K}{f}\frac{g_m^2}{W\cdot L\cdot C_{ox}^2}$$

$$Svg\cdot W\cdot L = \frac{Sid}{g_m^2}\cdot W\cdot L = \frac{K}{f}\frac{1}{C_{ox}^2}$$

- 10x 1/f flicker noise improvement over five nodes
- Enabled by Cox scaling from high-k
- Interface engineering to stabilize process factor K

RF 1/f Flicker Noise Scaling Trend

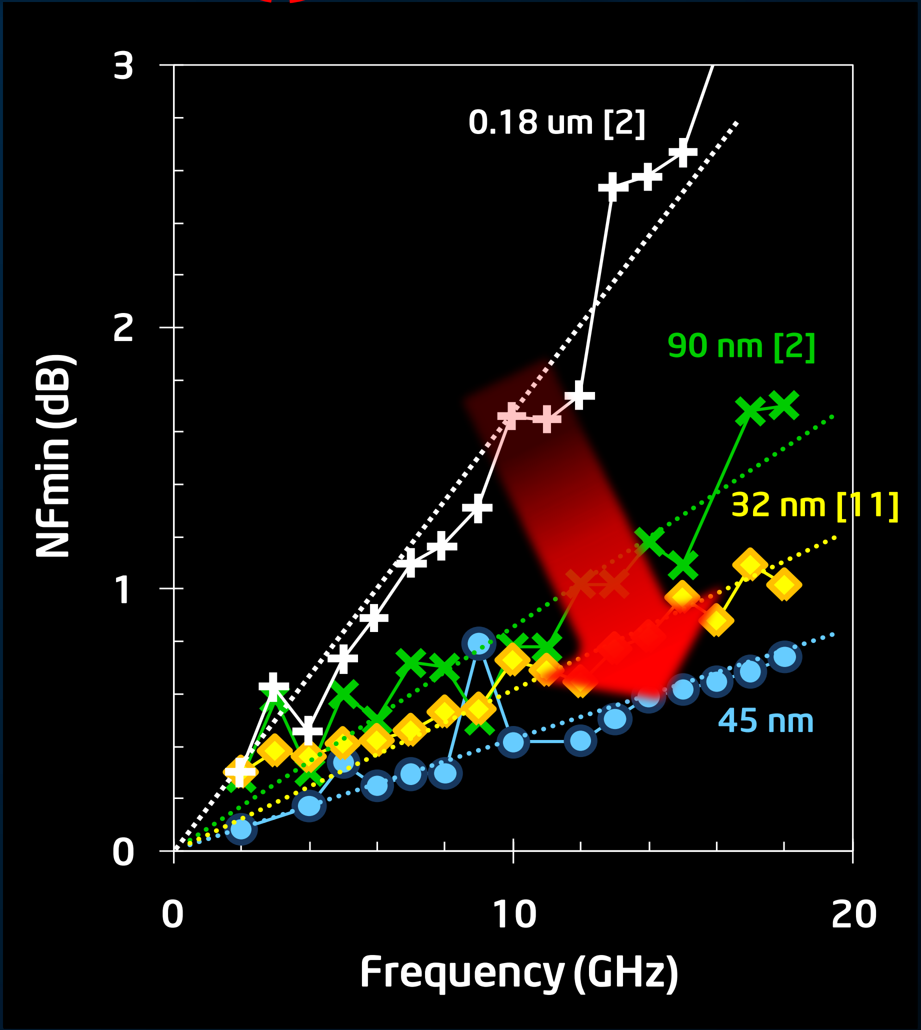


1/f flicker noise scaling, 10x reduction from 0.13 um to 32 nm, enabled by HK/MG Tox scaling and interface engineering

CMOS Scaling on RF - Noise Figures

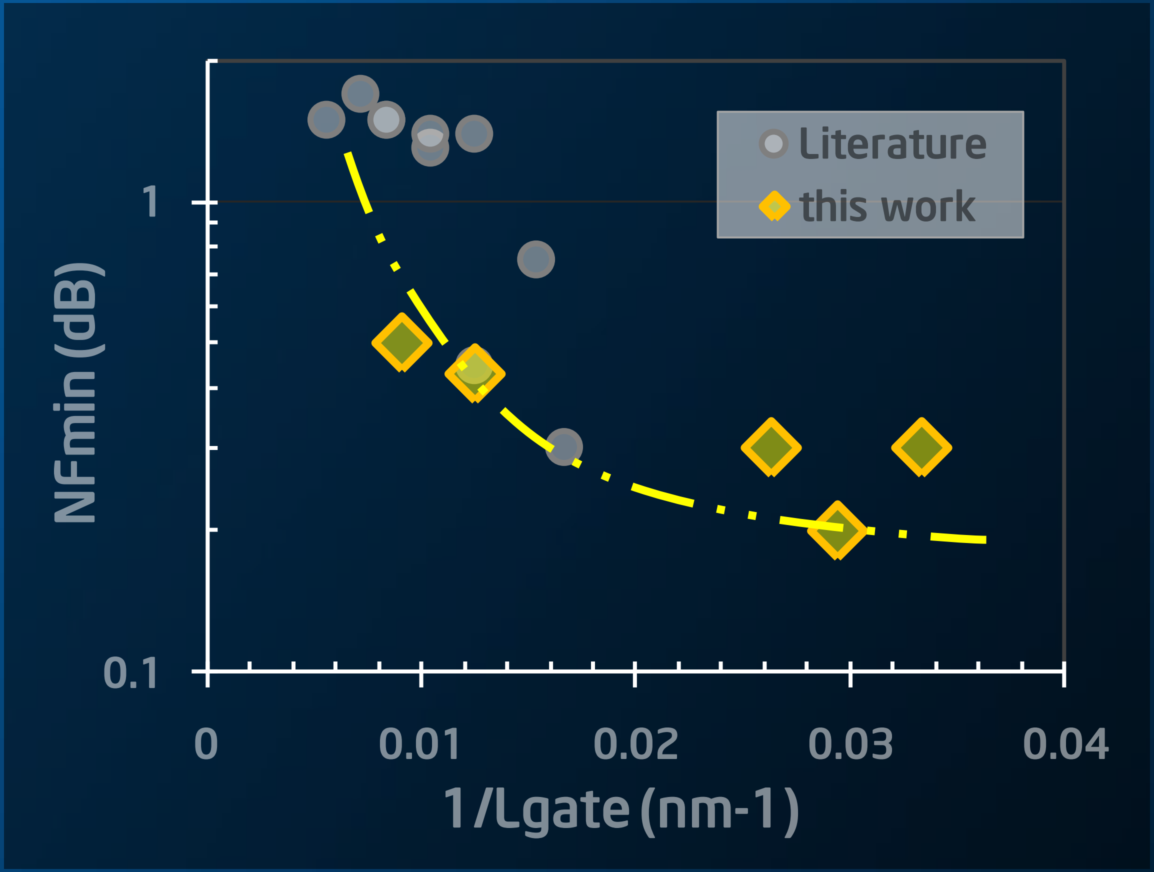
$$NF_{min} = 1 + K\frac{f}{f_T}\sqrt{g_m \cdot (R_g + R_s)} = 1 + K\frac{2\pi f \cdot C_{gg}}{\sqrt{g_m}}\sqrt{(R_g + R_s)}$$

- NFmin improved to < 1 dB level after 45 nm node
- g_m improvement needs to balance gate cap and gate resistance increase
- Layout optimization becomes critical for future scaling



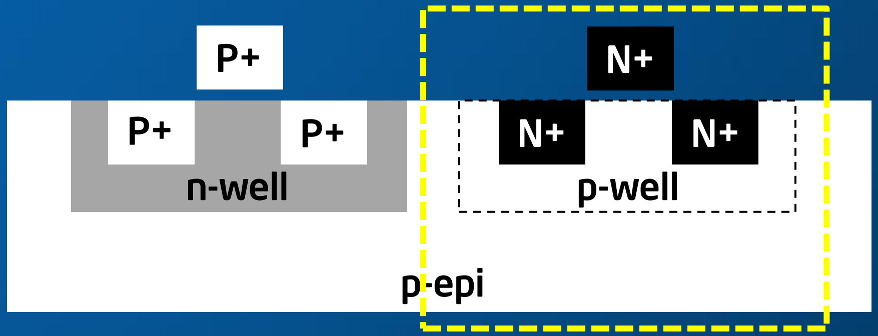
[2] K. Kuhn et al., VLSI Technology Symp., p. 224 (2004)
[5] I. Post et al, IEDM Tech Dig., pp. 1-3 (2006)
[8] C.-H. Jan et al, IEDM Tech. Dig., pp. 637-640 (2008)
[11] P. VanDerVoorn et al, VLSI Tech. Symp., p. 137 (2010)
[12] C.-H. Jan et al, IEDM Tech Dig., (2010)

RF Noise Figure Scaling Trend

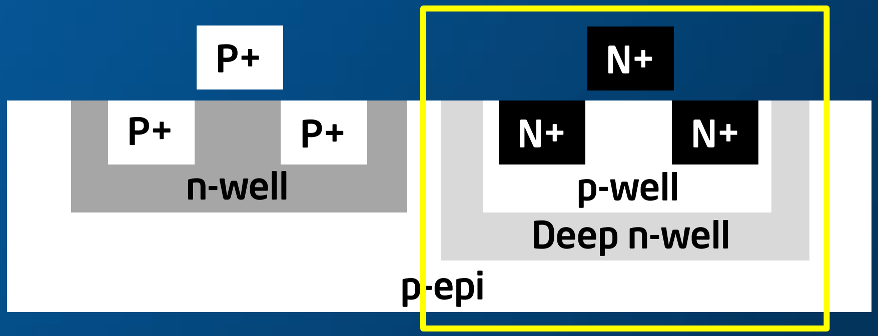


Noise figure NFmin scaling to a low level after 45 nm node

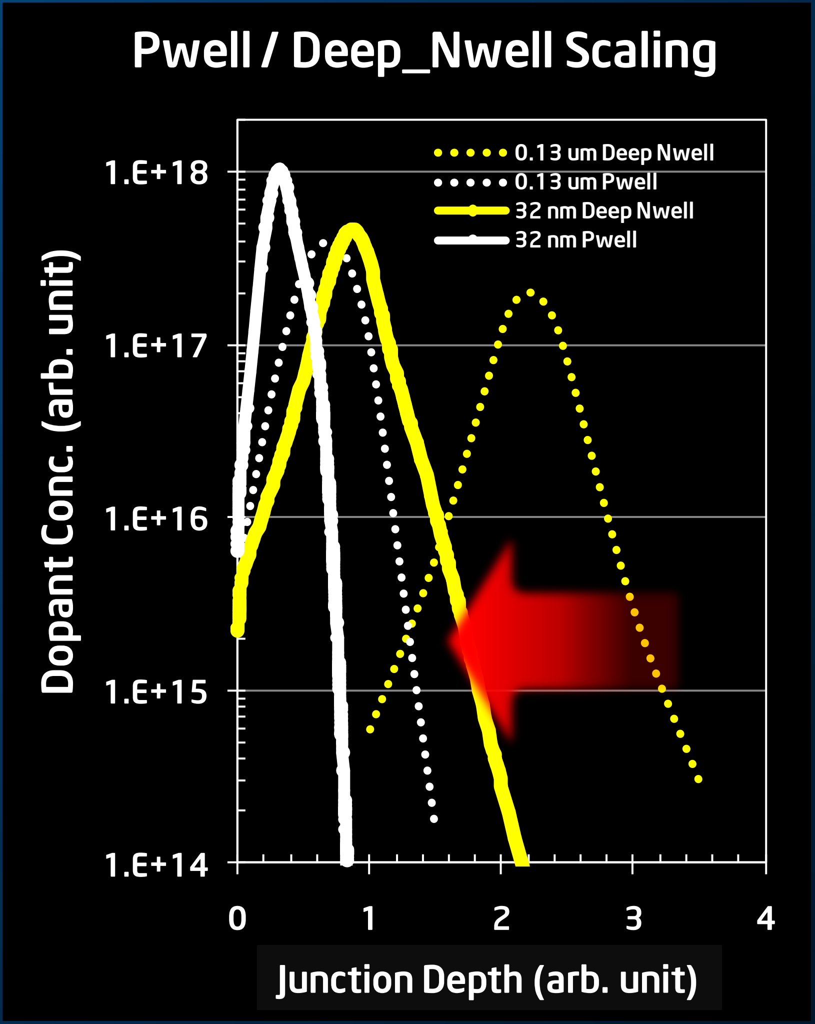
CMOS Scaling on RF – Deep Nwell



P-well in CMOS twin-well architecture

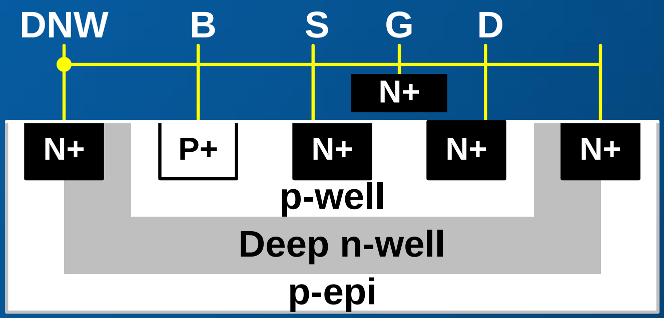


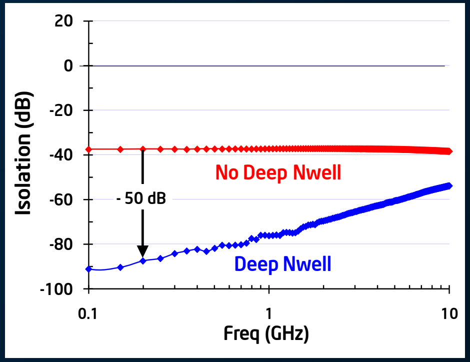
Deep n-well in triple-well architecture with MeV implants at older technology



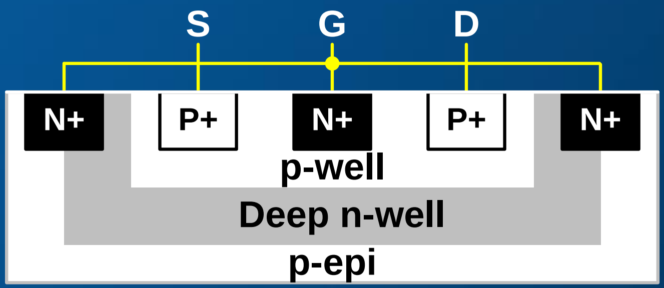
Deep n-well depth scaled by 2.5x from 0.13 um to 32 nm. Deep n-well integration is now more manufaturable with sub-MeV implants

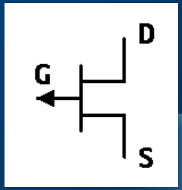
Deep Nwell Applications for M/S RF

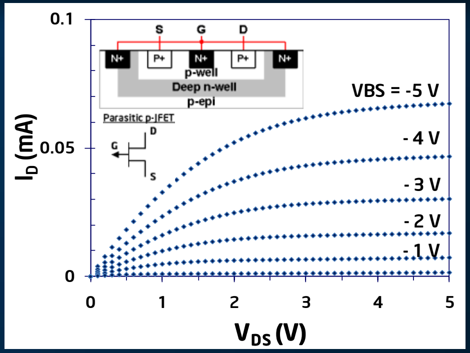




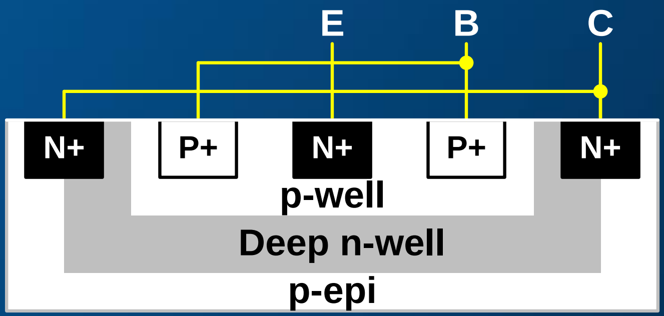
Substrate noise isolation (~ 50dB)

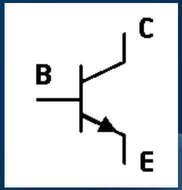


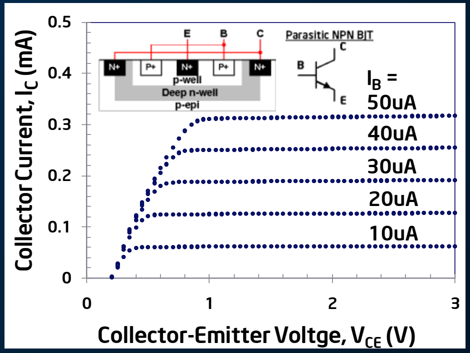




CMOS p-JFET

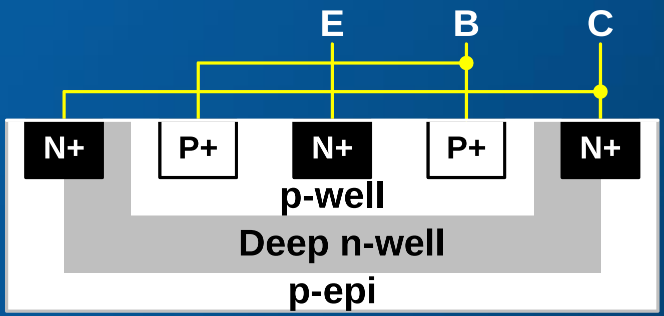




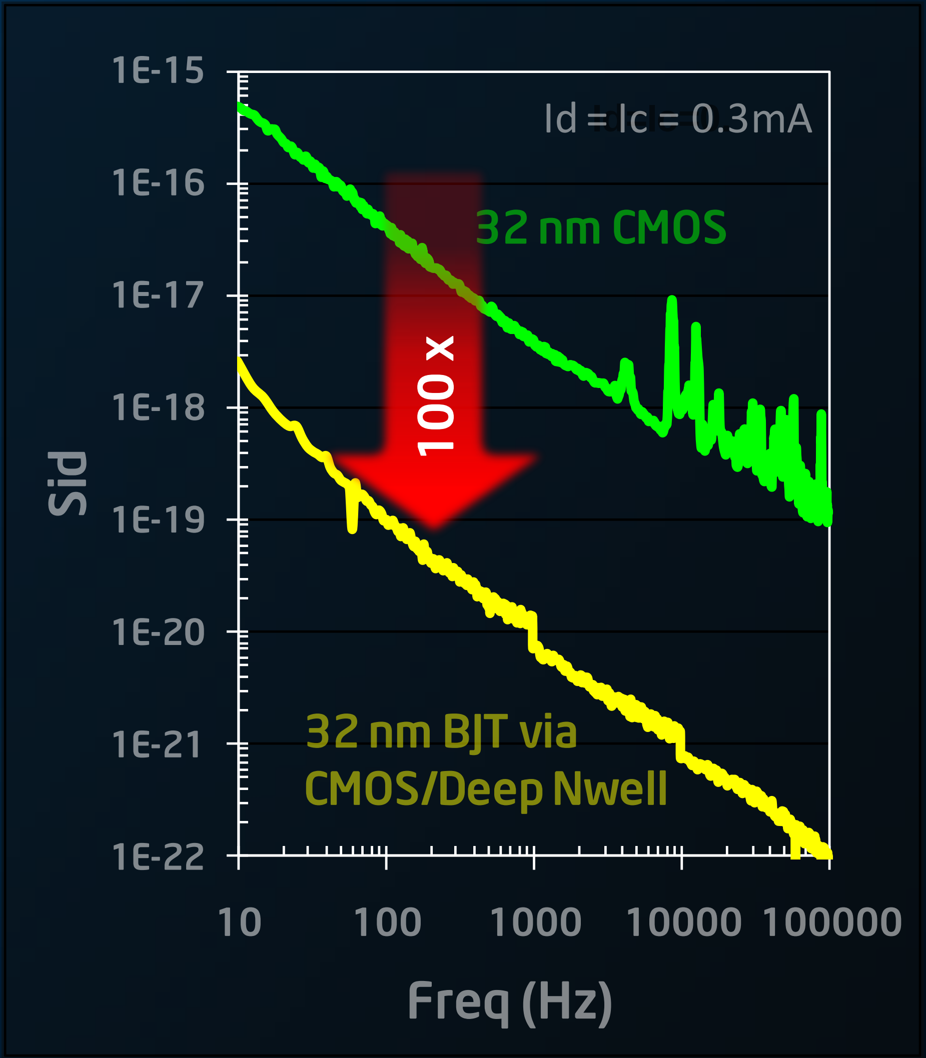


CMOS Parasitic NPN BJT

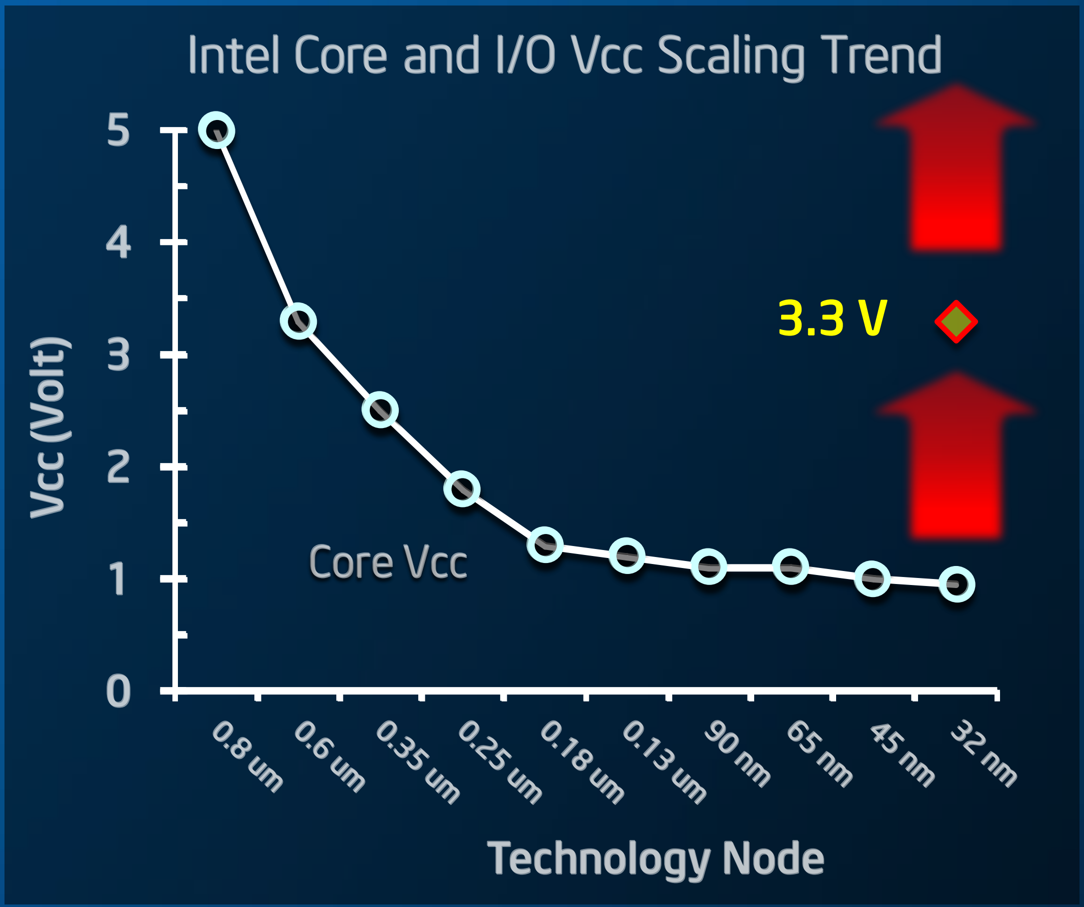
1/f Flicker Noise Reduction by BJT (via Deep Nwell)

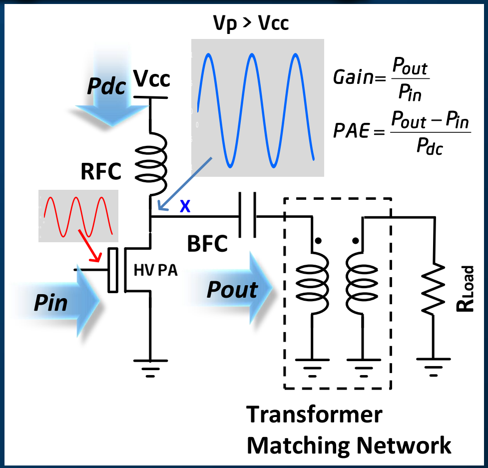


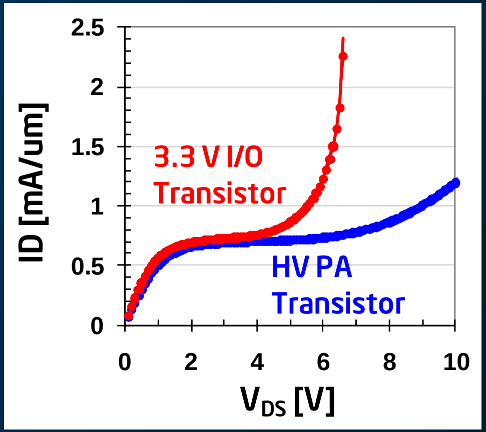
- BJT immune to oxide interface charge trapping/de-trapping (source of 1/f flicker noise)
- 100x flicker noise reduction measured on BJT (via CMOS/Deep Nwell)
- Applications in RF mixer circuits requiring very low flicker noise

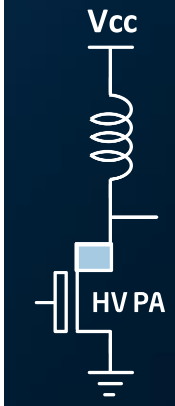


CMOS Scaling on RF – Voltage Scaling









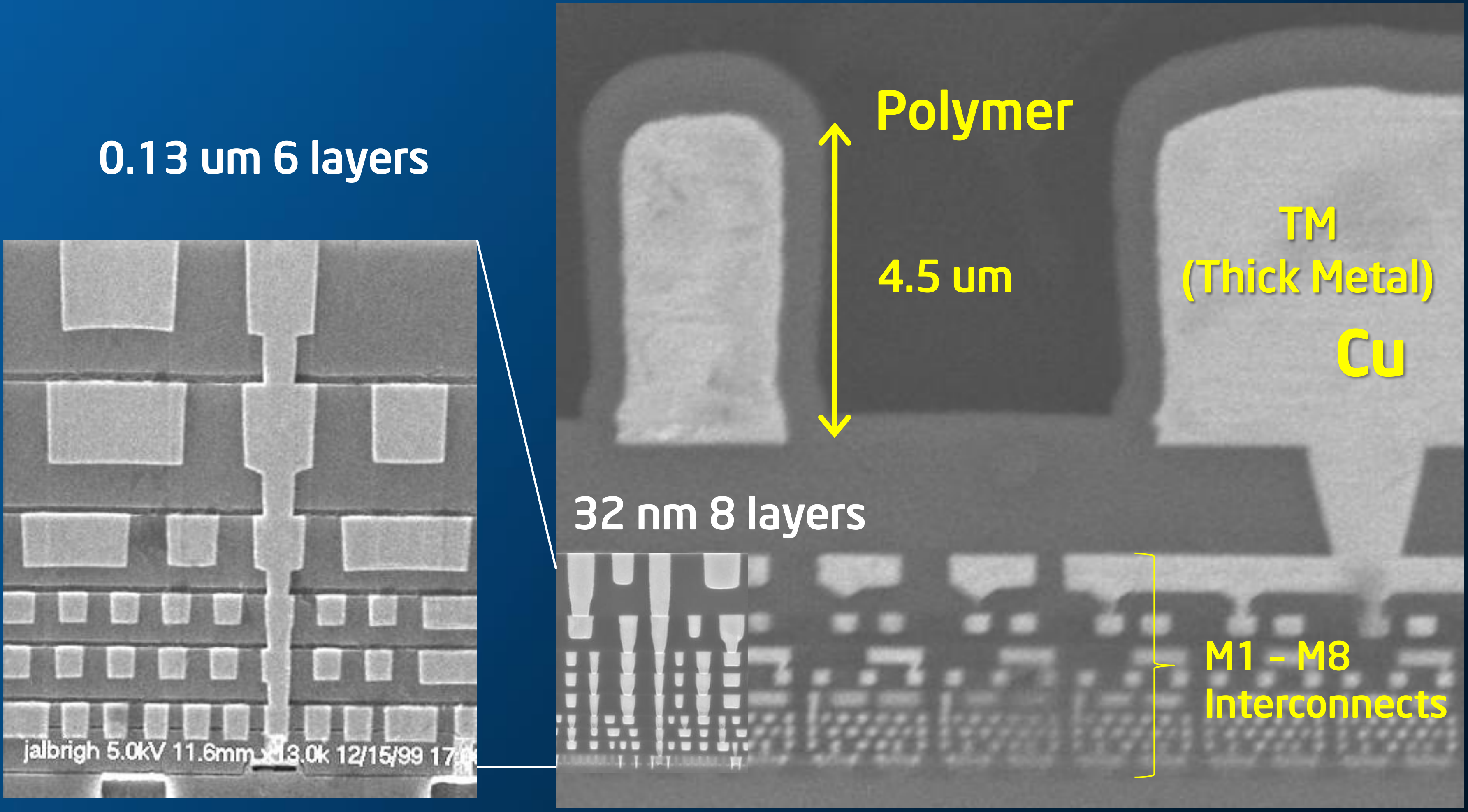
[11] P. VanDerVoorn et al, VLSI Tech. Symp., p. 137 (2010)

CMOS voltage scaling not favored for high voltage needs of RF (PA)

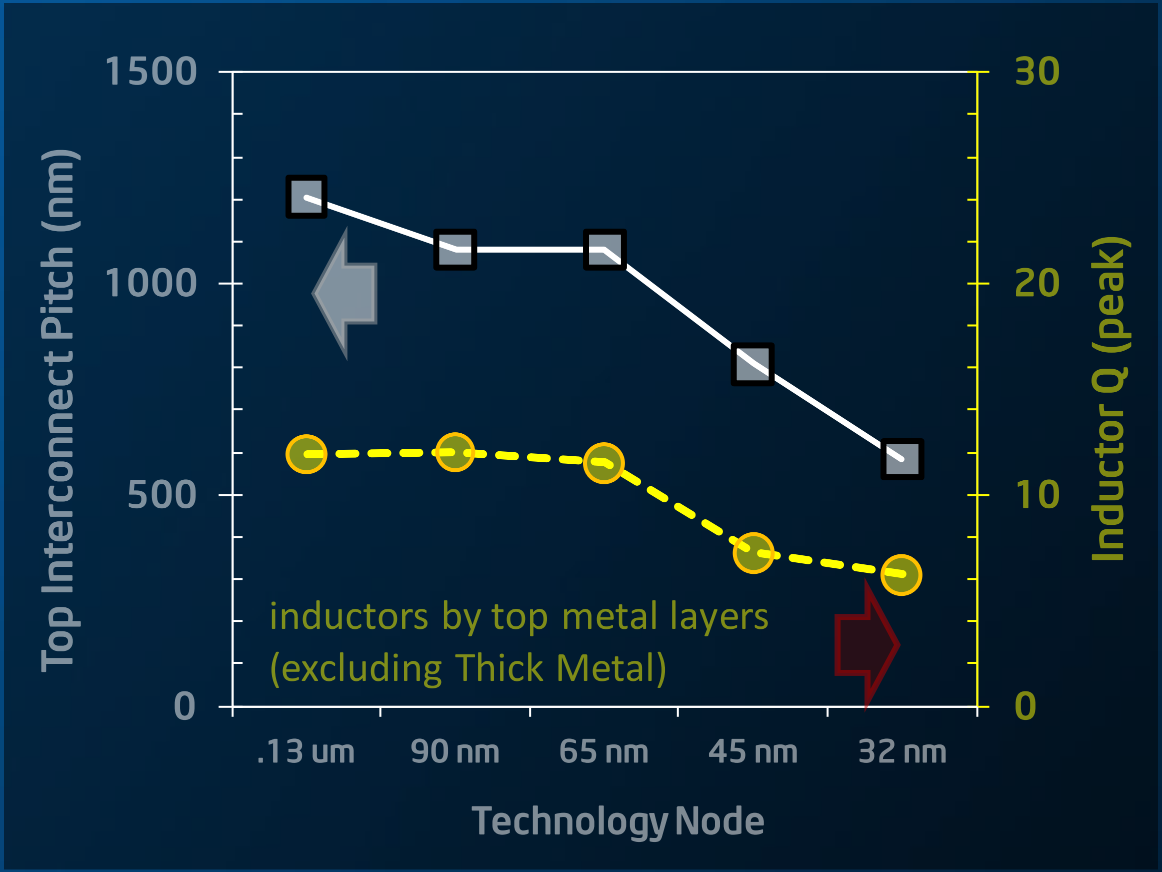
New high voltage PA transistors are developed to support HV needs

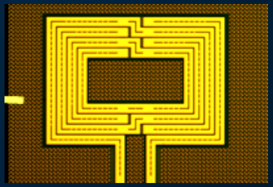
CMOS Interconnect Scaling

Interconnect scaling adversely impacts quality factor of RF Passives.
Thick metal (TM) solves the dilemma. Inductor Q of 25 achieved



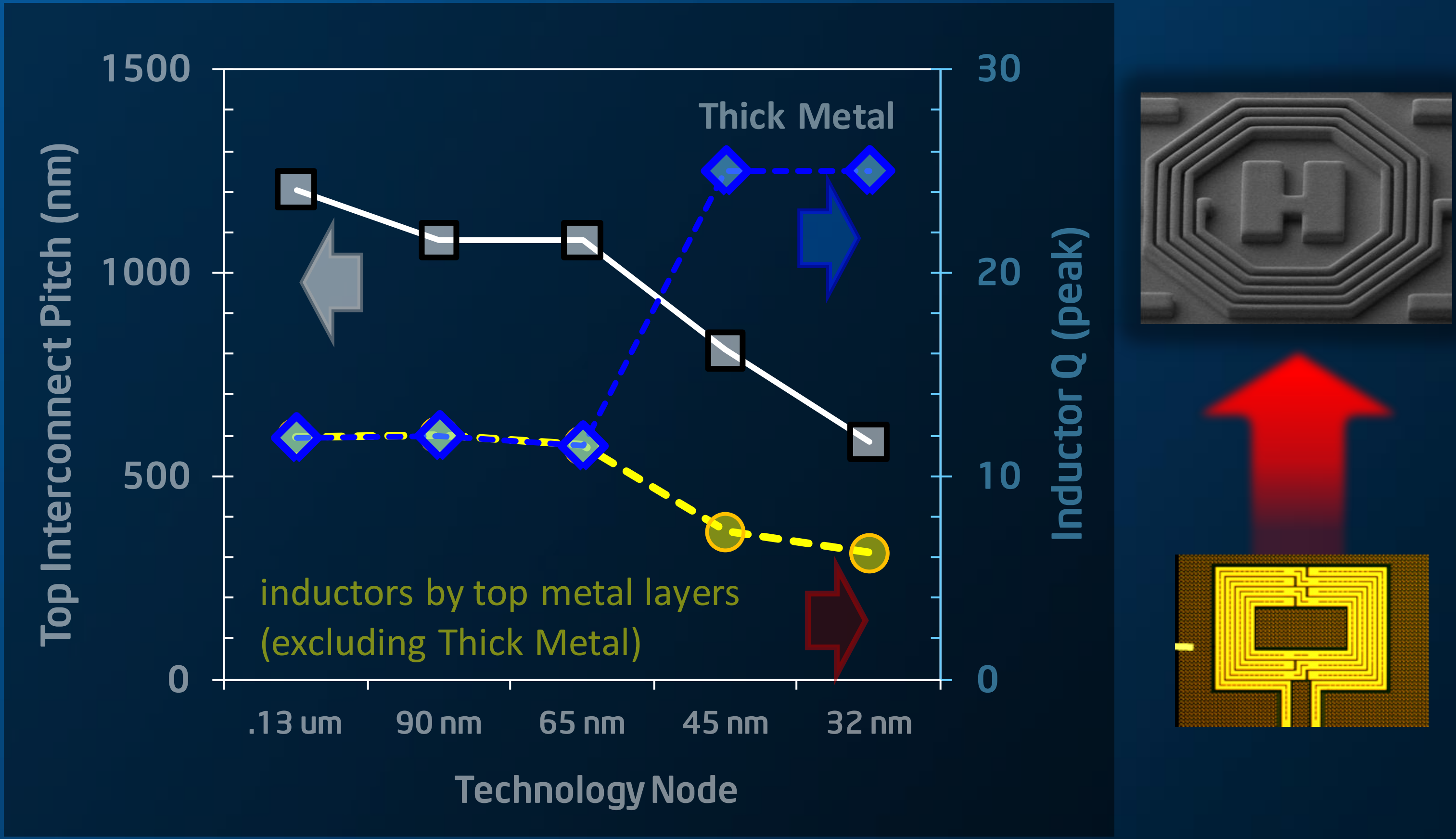
CMOS Interconnect Scaling on RF





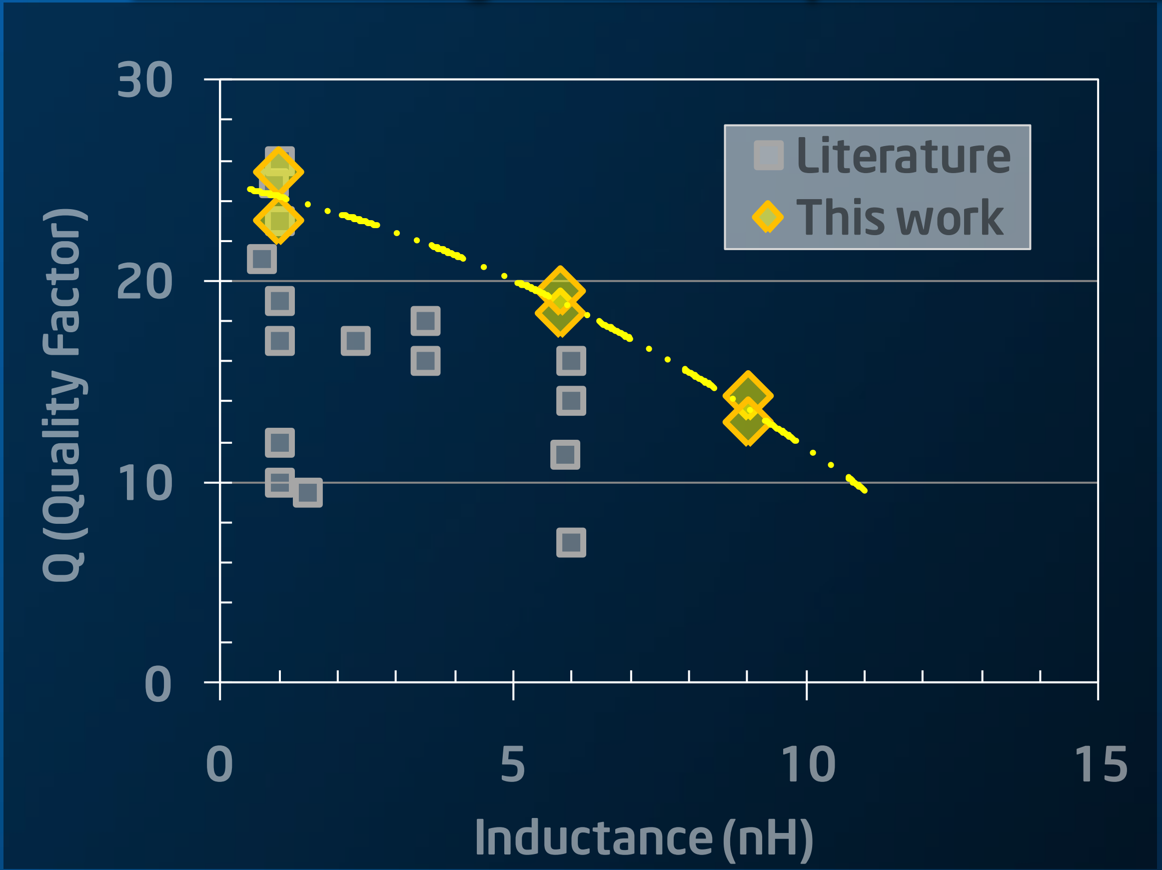
Metal spiral Inductor Q progressively degraded with the scaling of interconnect pitch and metal thickness ($Q = \omega L/R$)

CMOS Interconnect Scaling on RF with TM

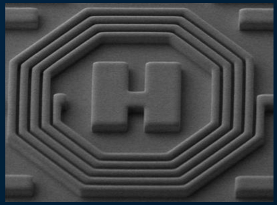


Spiral Inductors by TM recover and improve the quality factor to achieve Q~25

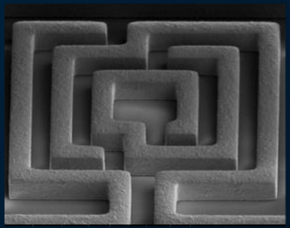
32 nm High Q RF Spiral Inductor Family



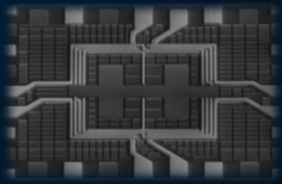
Complex high Q monolithic silicon spiral inductors were developed using TM for 32 nm RF designs, including PA, LNA, and VCO



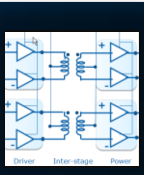
Single End Inductor



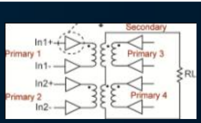
Differential Inductor



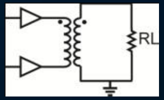
Transformer/ Spliter



Power Combiner



Balun



Conclusions

- ☐ Moore's Law alive and well for RF CMOS, enabled by the innovations in transistors architectures and interconnects
- ☐ Continuous improvement in CMOS g_m and Cox keys to the RF CMOS cut-off frequency and noise performance scaling
- ☐ RF passives scaling needs creative solutions in interconnect architectures scaling
- ☐ 32 nm wireless transceiver demonstrated with state of the art 32 nm RF CMOS technology

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