A 32nm SoC Platform Technology with 2nd Generation High-k/Metal Gate Transistors Optimized for Ultra Low Power

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Logic Technology Development
Technology Manufacturing Group

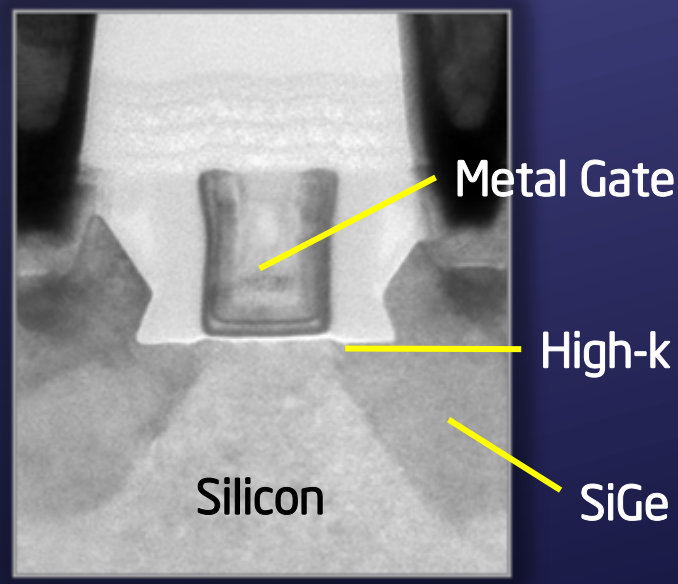
Intel Corporation

Outline

- 32 nm High-k/Metal Gate SoC Technology
- 32 nm SoC Transistor Architecture
- 32 nm SoC Interconnects and Passives
- 32 nm SoC Embedded Memory
- Summary

32 nm High-k/Metal Gate Transistor

- 2nd gen high-k/metal gate
- Replacement Metal Gate (RMG) Flow
- 4th gen strained silicon
- 20% performance improvement over 45 nm high-k/metal gate
- In high volume manufacturing production of multi-core CPU products in multiple fabs



Replacement Metal Gate (RMG) SOC Flow

CPU Flow

- Isolation (wells, Vt)
- Dielectric growth
- Poly-Si dep
- Poly-Si patterning
- Logic S/D extension- HP/LP
- Spacer dep/patterning
- S/D formation
- Poly-Si Gate Removal
- Metal Gate Replacement
- Contact Formation

SOC Flow

- Isolation (wells, Vt)
- ***Oxide I/O gate growth***
- ***Oxide I/O gate patterning***
- Dielectric growth
- Poly-Si dep
- Poly-Si patterning
- Logic S/D extension- HP/SP
- ***LP S/D extension***
- ***I/O S/D extension***
- Spacer dep/patterning
- S/D formation
- Poly-Si Gate Removal
- Metal Gate Replacement
- Contact Formation

SoC process flow is derived from the 2nd generation CPU RMG (Replacement Metal Gate) flow

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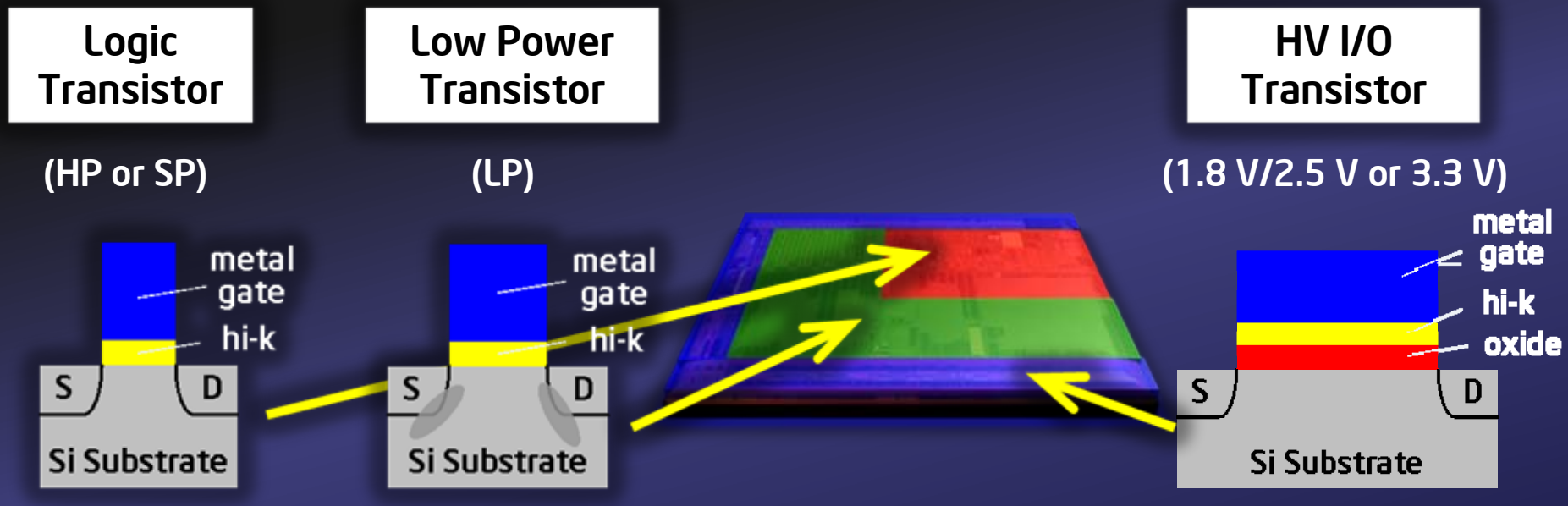
Triple Transistor Architecture



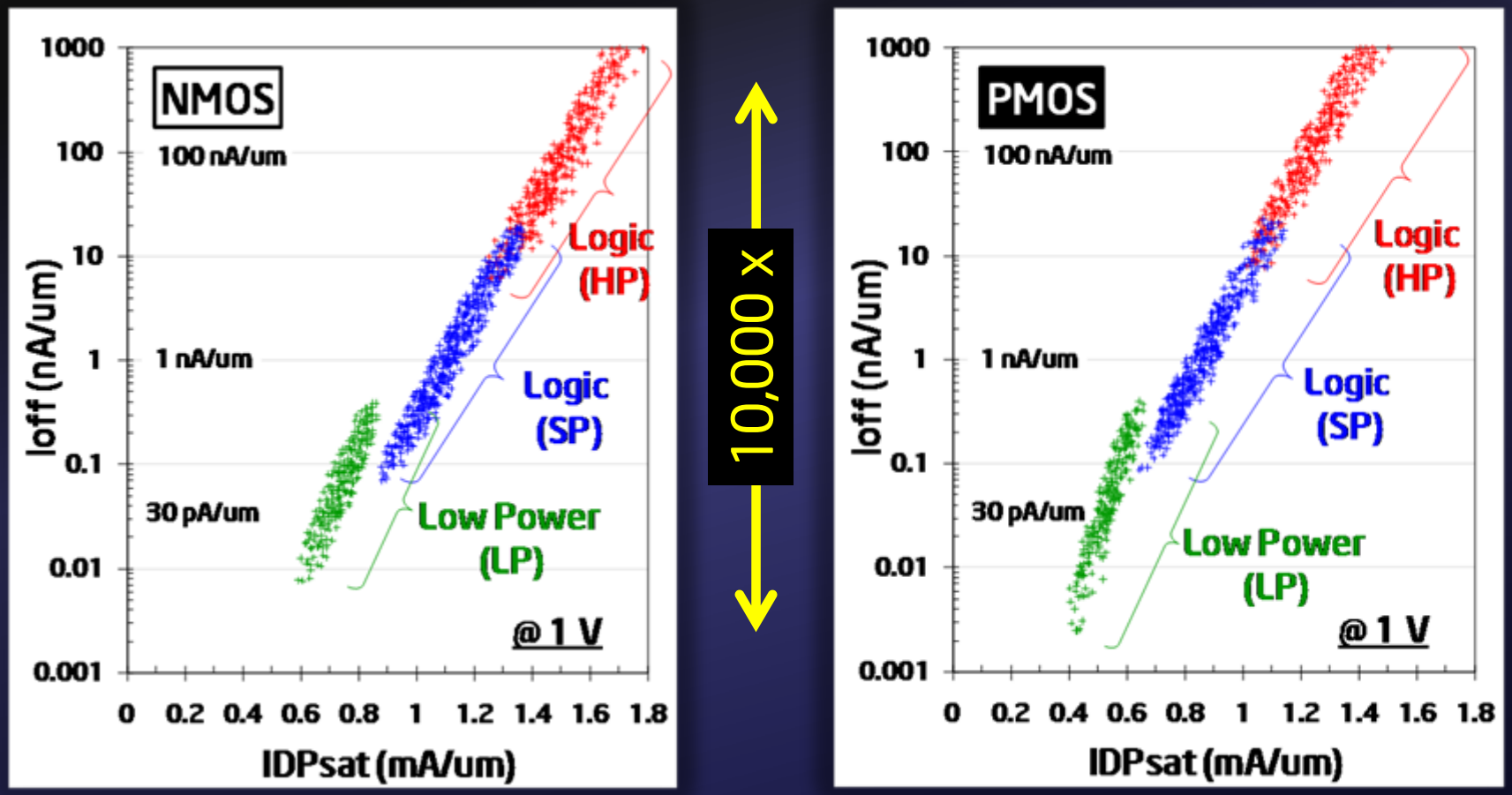
- A low cost implementation with three types of transistors "co-exist" on the same die:
  - ✓ Logic (HP or SP) : for burst CPU performance
  - ✓ Low Power (LP) : for always-on-always-connected application and long battery life
  - ✓ HV I/O: for high voltage I/O
- Take advantage of the low gate leakage of high-k/metal gate to avoid the traditional expensive "triple gate" approach

Transistors Summary

Transistor Type	Logic (option for HP or SP)		Low Power	HV I/O (option for 1.8 or 3.3 V)	
	HP	SP	LP	1.8/2.5 V	3.3V
EOT (nm)	0.95	0.95	0.95	~ 4	~ 7
Vdd (V)	.75/ 1	.75/ 1	0.75/1.2	1.5 /1.8	1.5 /3.3
Pitch (nm)	112.5	112.5	126	min. 338	min. 450
Lgate (nm)	30	34	46	>140	>300
NMOS Idsat (mA/um)	1.53 @ 1 V	1.12 @ 1 V	0.71 @ 1 V	0.68 @1.8 V	0.7 @3.3 V
PMOS Idsat (mA/um)	1.23 @ 1V	0.87 @ 1 V	0.55 @ 1 V	0.59 @1.8 V	.6 @3.3 V
Ioff (nA/um)	100	1	0.03	0.1	<0.01

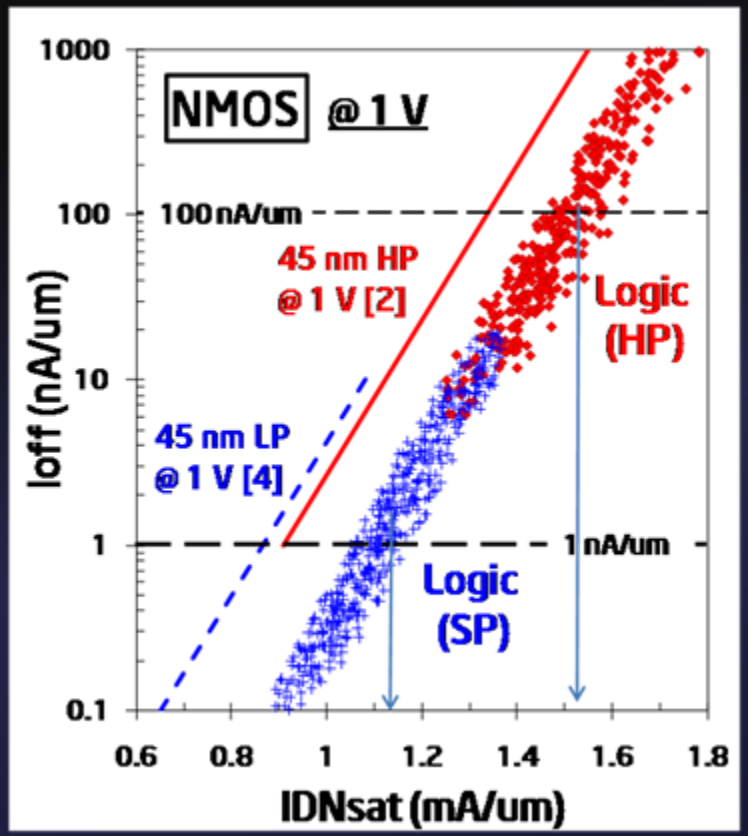
Tightest minimum gate pitch for 32/28 nm processes

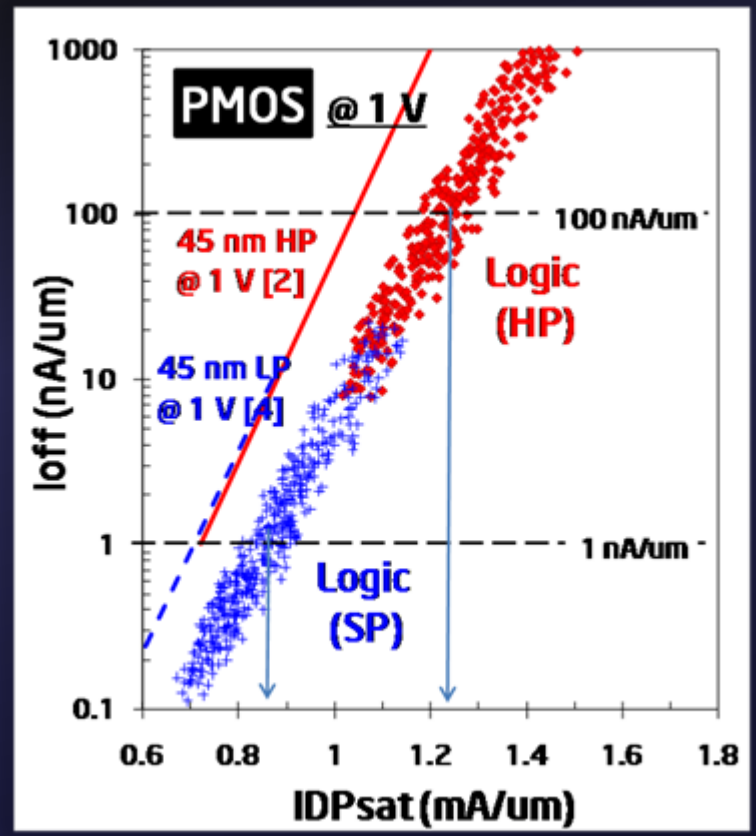
Logic and LP Transistors Dynamic Range



Logic and LP transistors cover 4 orders of magnitude (10,000 x) of leakage power to support a wide dynamic range SoC applications

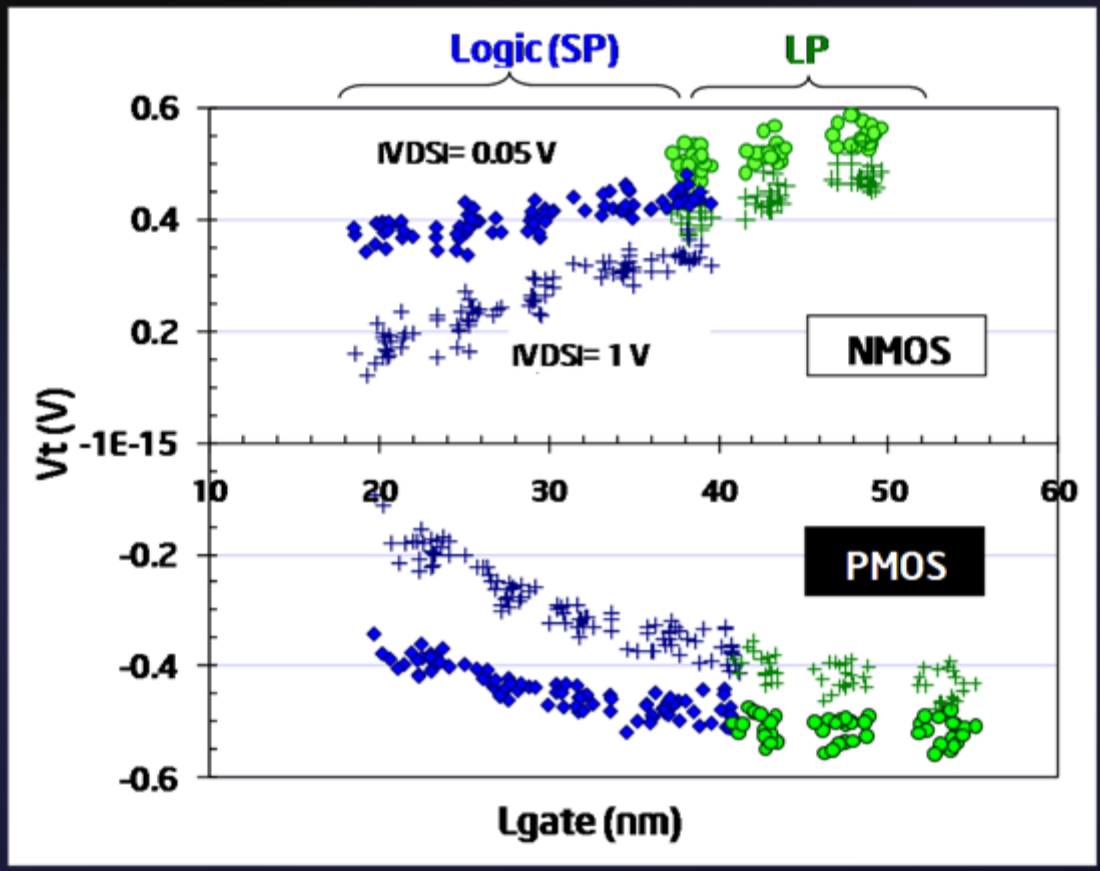
Logic Transistors Ion-Ioff (HP/SP)





- Highest reported drives for 32/28 nm SoC process at tightest gate pitch (112 nm) -1.53 mA/um (N) / 1.12 mA/um (P) at 100nA/um
- 20-35% improvement over 45 nm high-k/MG logic transistors

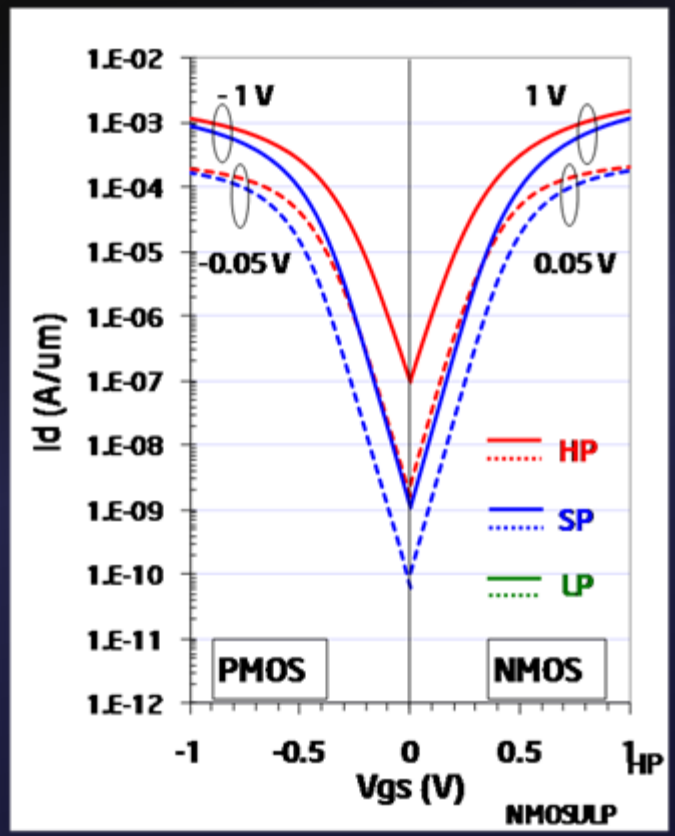
Logic/LP Transistors Vt vs. L



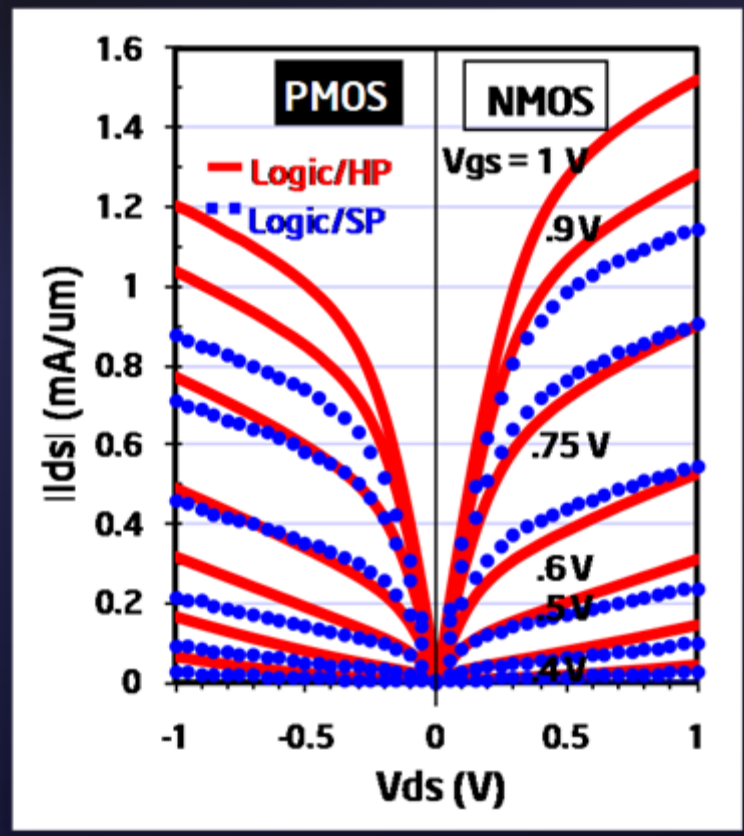
- Short channel effect, DIBL, Vt roll-off are well controlled
- SP Vt < 400 mV, LP Vt ~ 500 mV

Logic Transistor I-V Characteristics

Sub-threshold

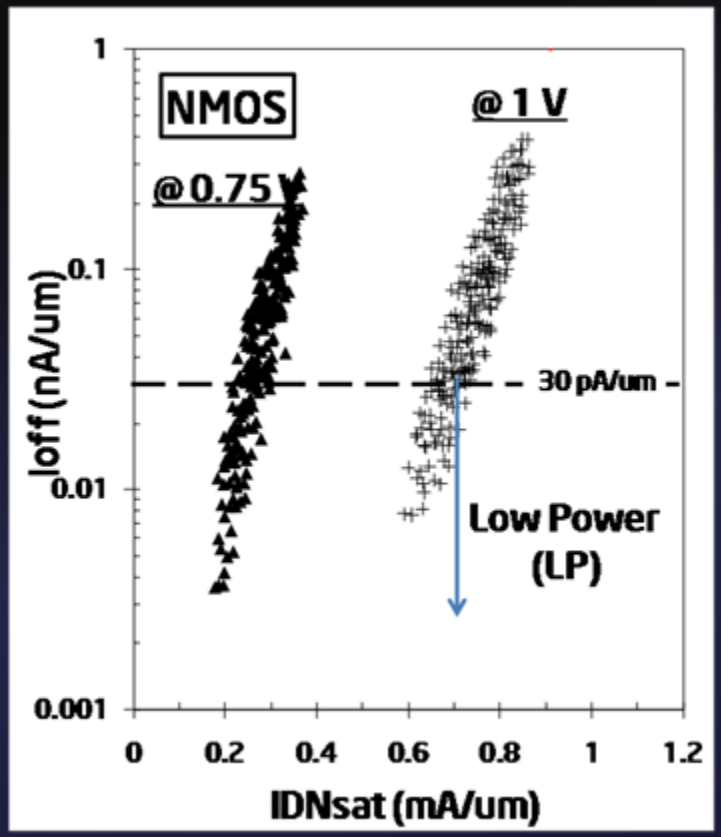


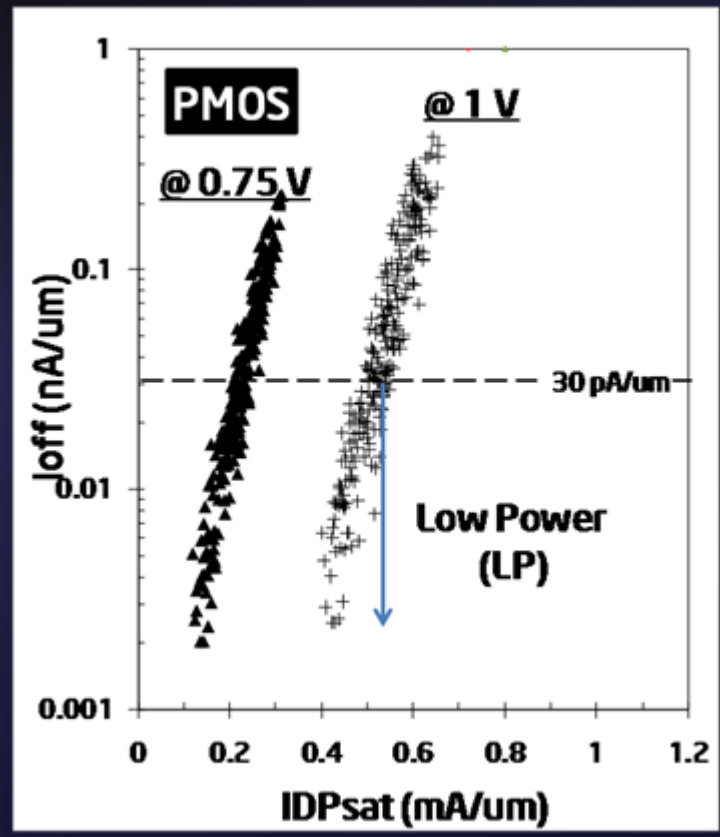
Id-Vd Characteristics



- Well controlled transistor I-V characteristics – HP and SP
- Sub-threshold slope ~ 100mV/decade (HP), < 90 mV/decade (SP)
- DIBL – SP: 90 mV (N)/100 mV (P); HP: 130 mV (N)/140 mV (P)

Low Power Transistors Ion-Ioff (LP)

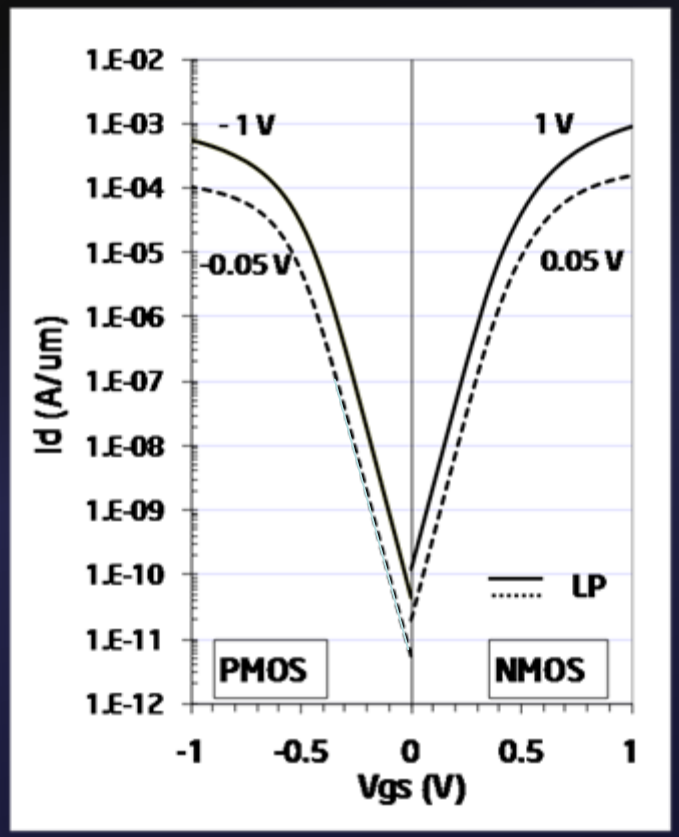




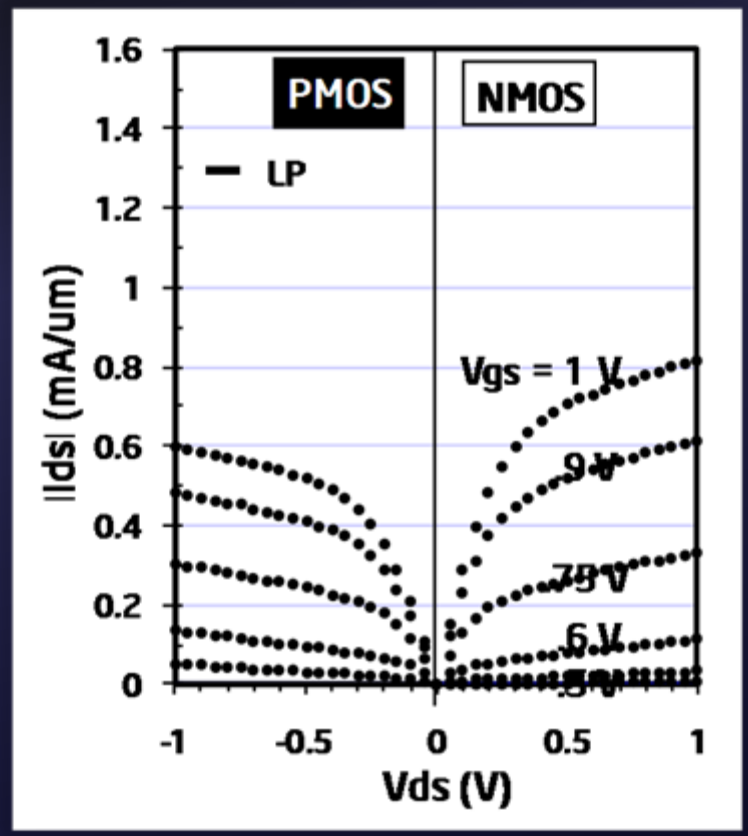
- Highest reported drive currents at lowest standby leakage (30pA/um, 1000x lower than HP) AND
- Low active power (0.75 V) with good performance

Low Power Transistor I-V Characteristics

Sub-threshold

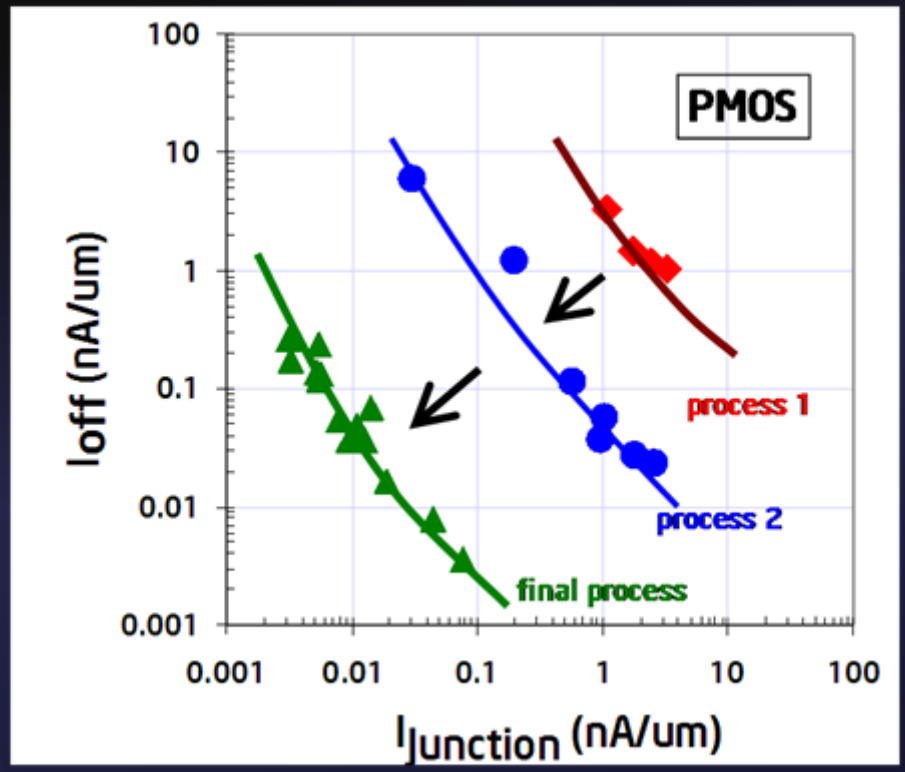


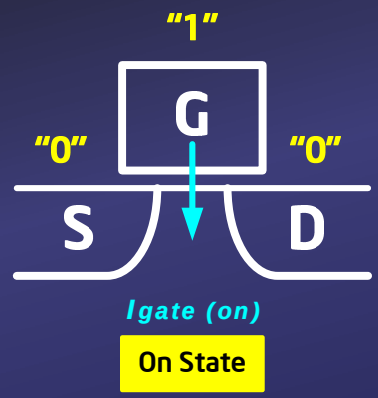
Id-Vd Characteristics

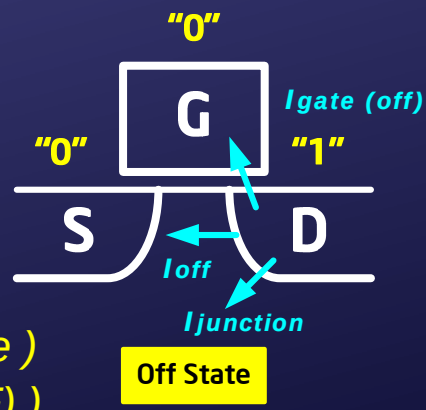


- Well controlled transistor I-V characteristics - LP
- Sub-threshold slope ~ < 85 mV/decade
- DIBL - 70 mV (N)/100 mV (P)

Low Power Transistors Total Leakage







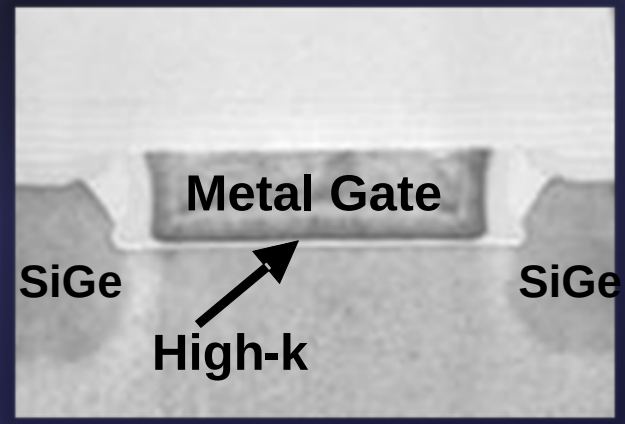
I_{LKG} = ½ ("ON" State Leakage) + ½ ("OFF" State Leakage)

= ½ (I_{gate} (ON)) + ½ (SF x I_{off} + I_{junc} + I_{gate} (OFF))

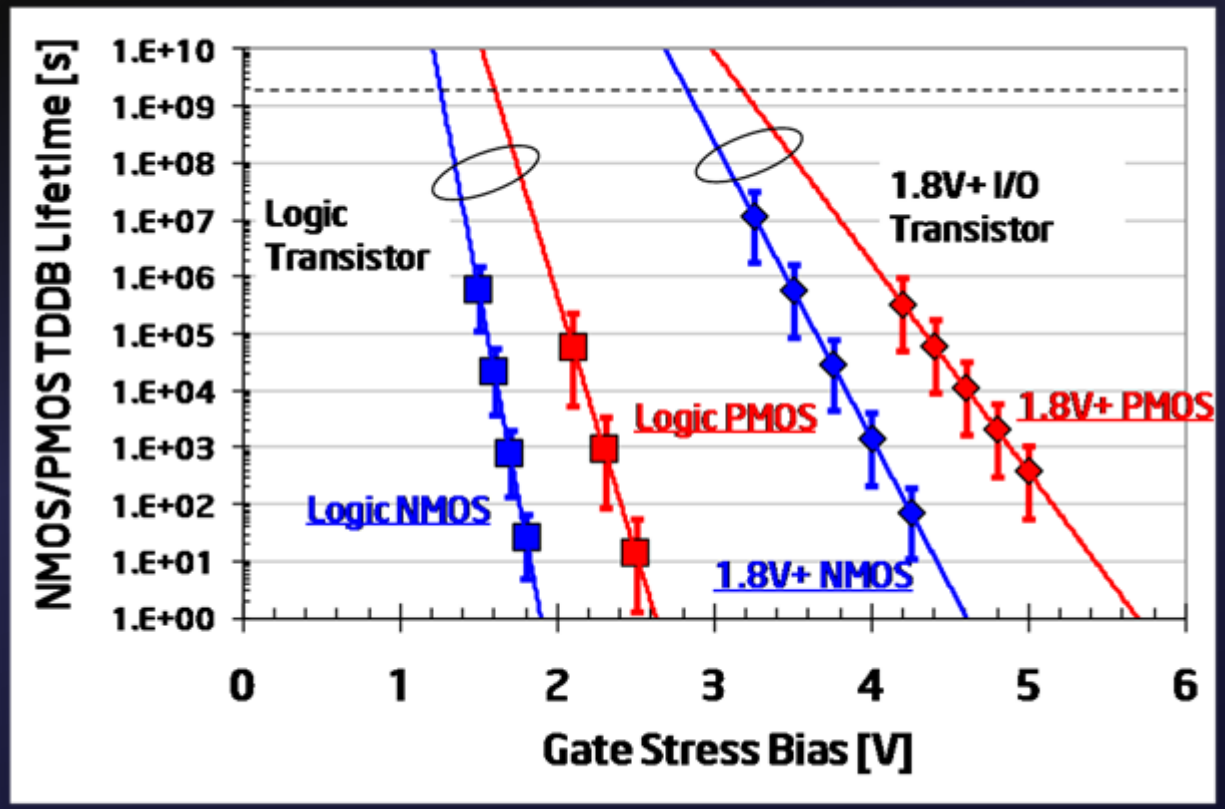
All leakage components – Ioff, Igate(on), Igate(off) and Ijunction need to be mitigated for low power transistor

High Voltage Transistors (1.8/2.5 V or 3.3 V)

- 2nd gen high-k/metal gate I/O Transistors
- 1.8/2.5 V or 3.3 V options
- High-k/Oxide composite gate stack
- Min gate length = 140 nm (1.8 V)
  Min gate length = 300 nm (3.3 V)



Reliability – Logic and High Voltage



Robust NMOS and PMOS high k + metal gate logic and I/O transistors TDDB

Outline

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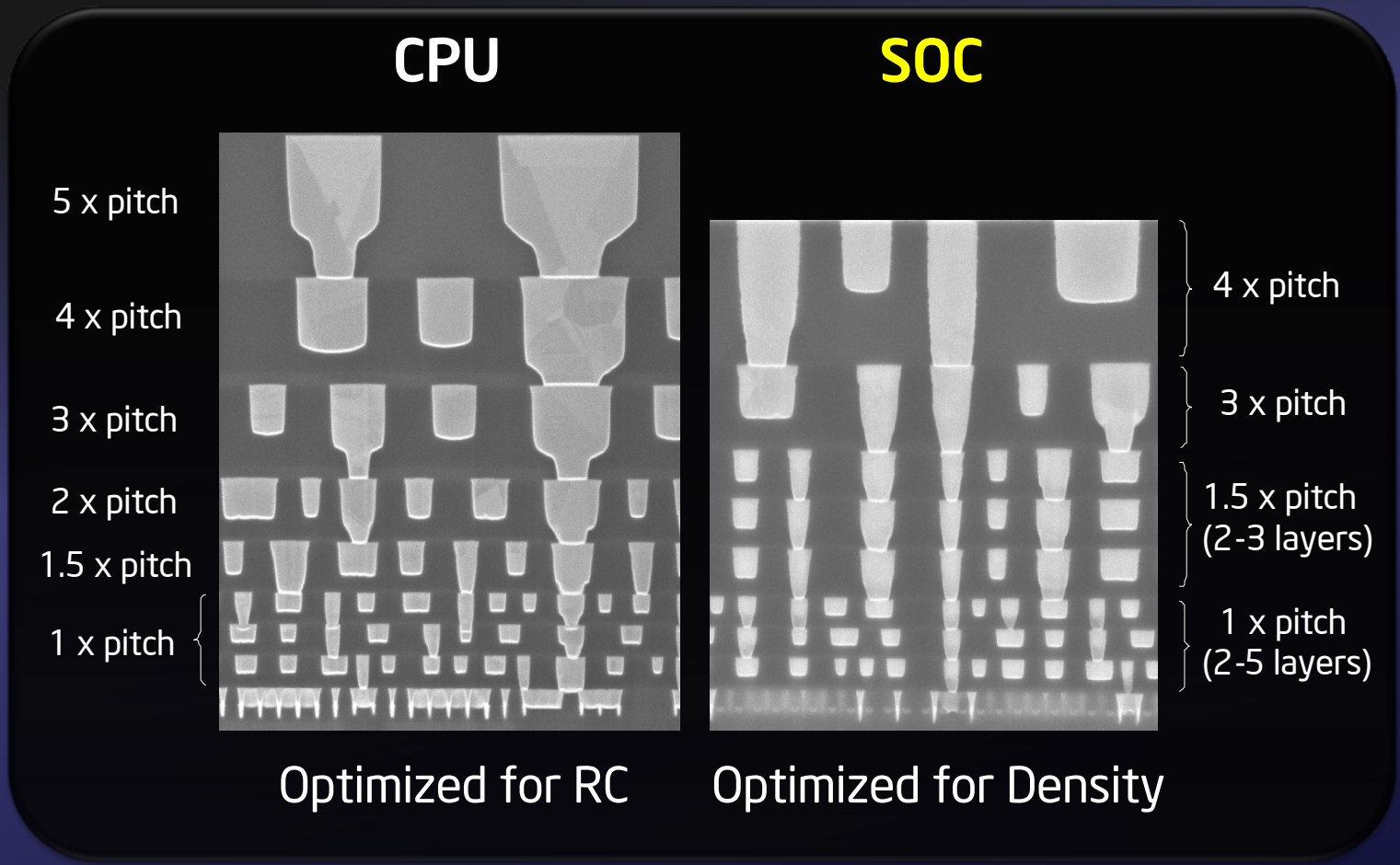
32 nm SoC Interconnects



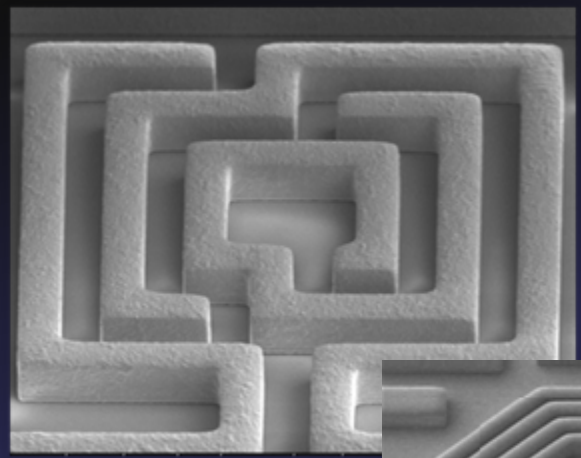
SOC interconnect system optimized for density and flexibility

32 nm SoC Interconnects – Thick Top Metal

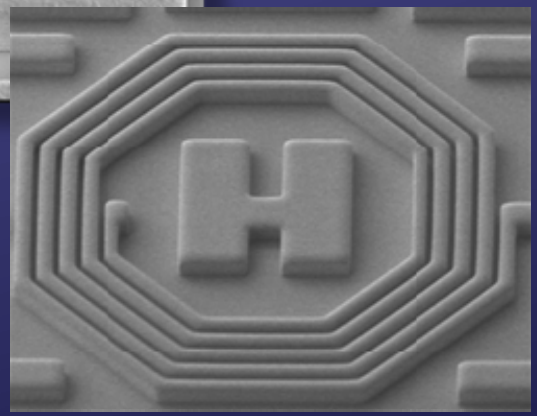
Thick top metal for power delivery and I/O routing

32 nm SoC High Q Inductors

Inductors

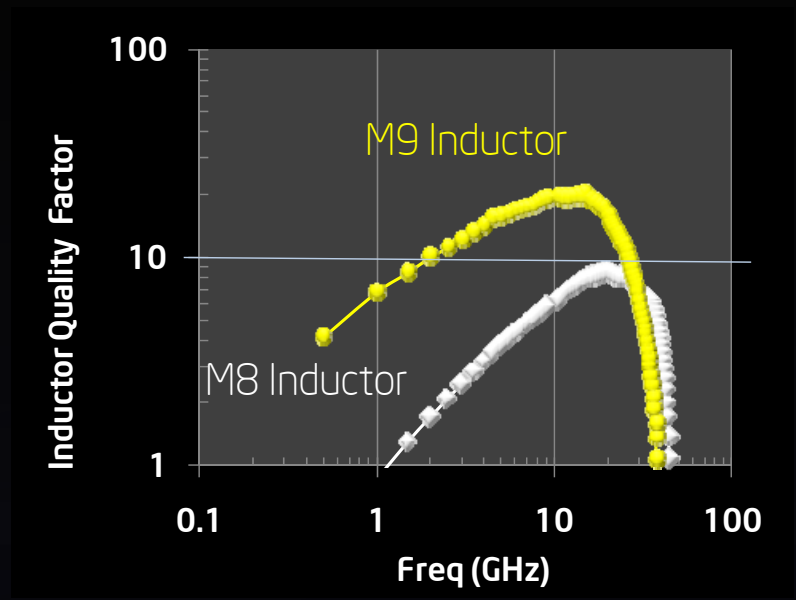


1 nH Inductor for VCO



6 nH inductor for 2.4 GHz Wi-Fi LNA

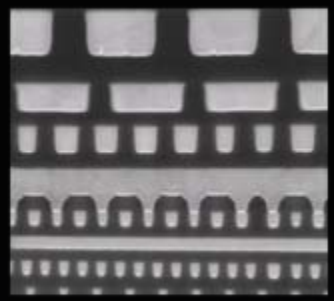
Quality Factor Comparison of M9 and M8 Inductors



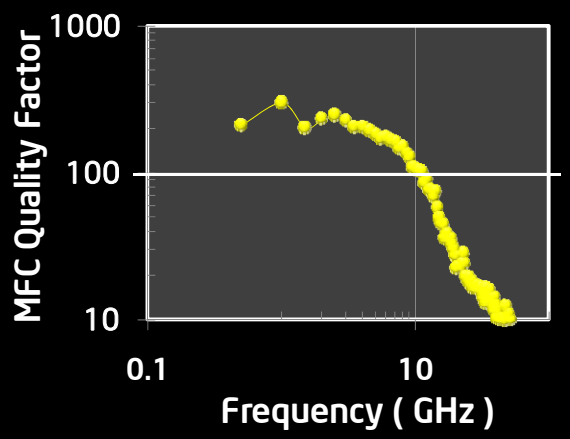
Thick top metal ideal for high Q inductors (Q > 20)

32 nm SoC Capacitors and Resistors

Capacitors

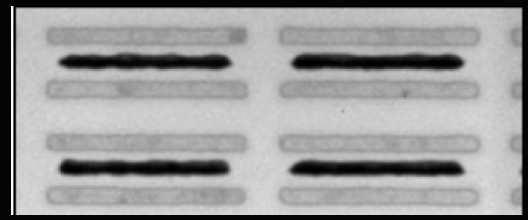


Metal Finger Capacitor

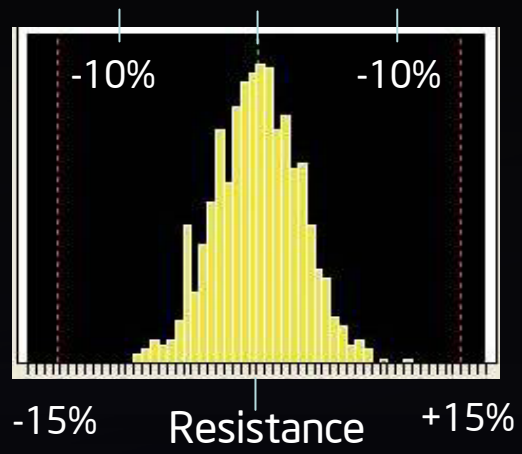


Q of Metal Finger Capacitor

Resistors



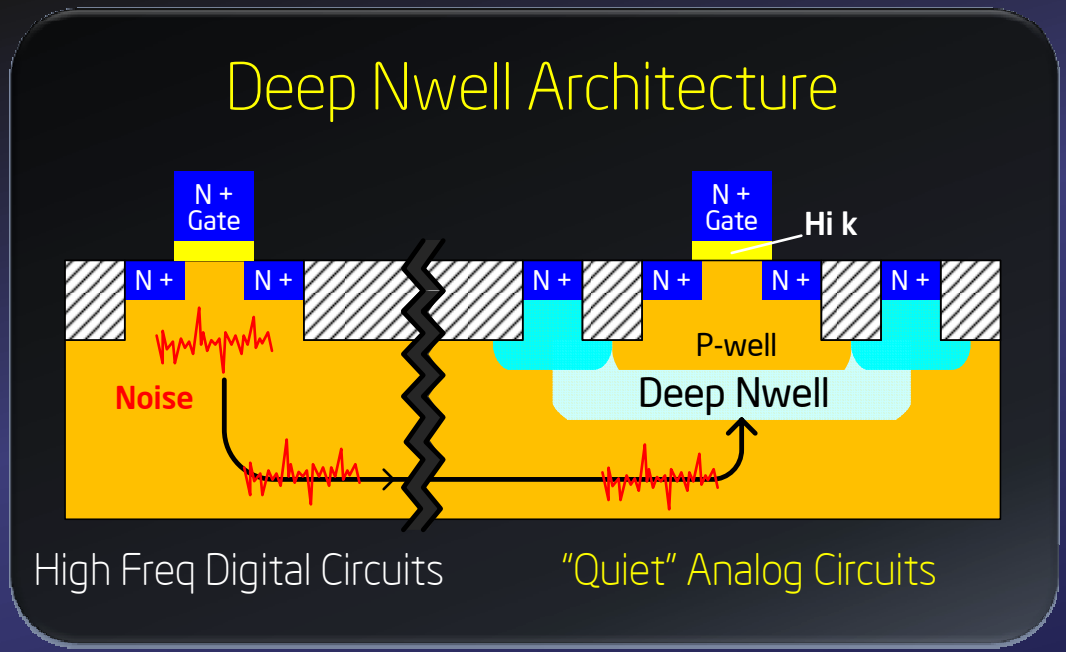
Linear Resistor



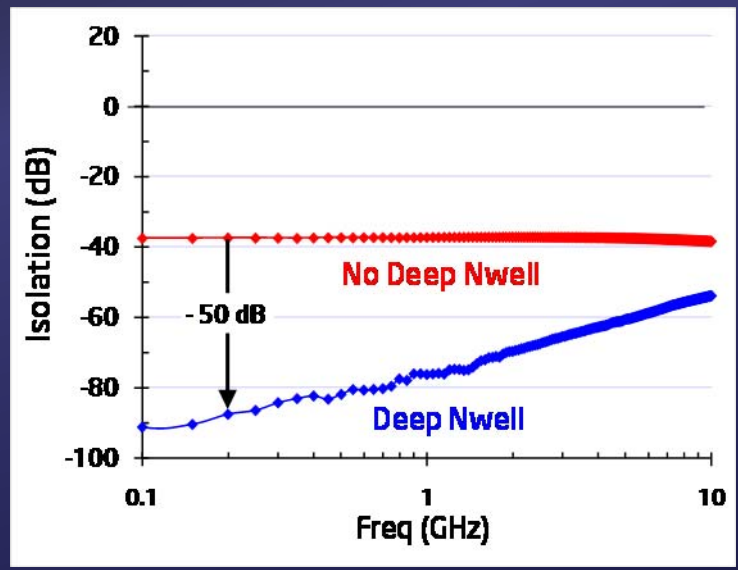
Precision Resistor

Rich high quality factor and high precision passives

Deep Nwell for Substrate Noise Isolation



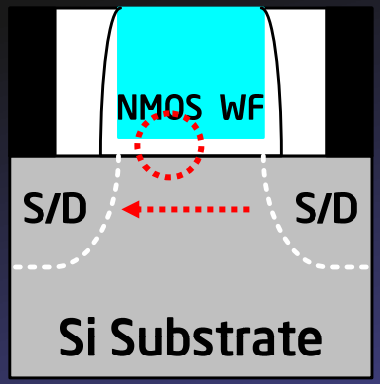
Substrate Noise Measurement

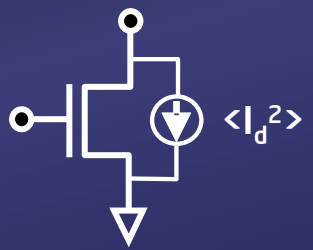


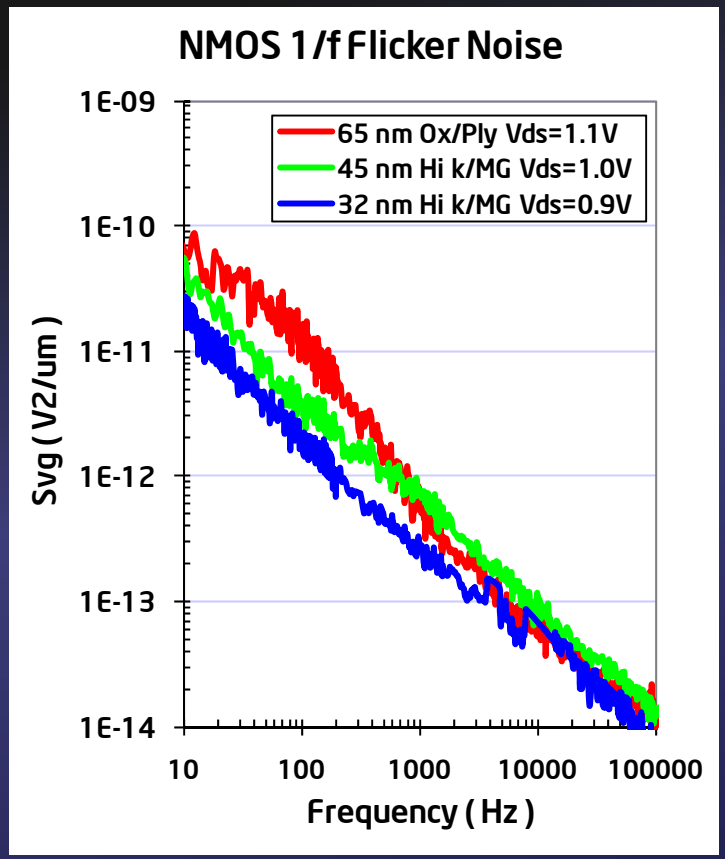
50 dB substrate noise reduction measured on deep Nwell for noise sensitive analog circuits – ADC (Analog-Digital Converter), DAC (Digital-Analog Converter), PA (Power Amplifier) and VCO

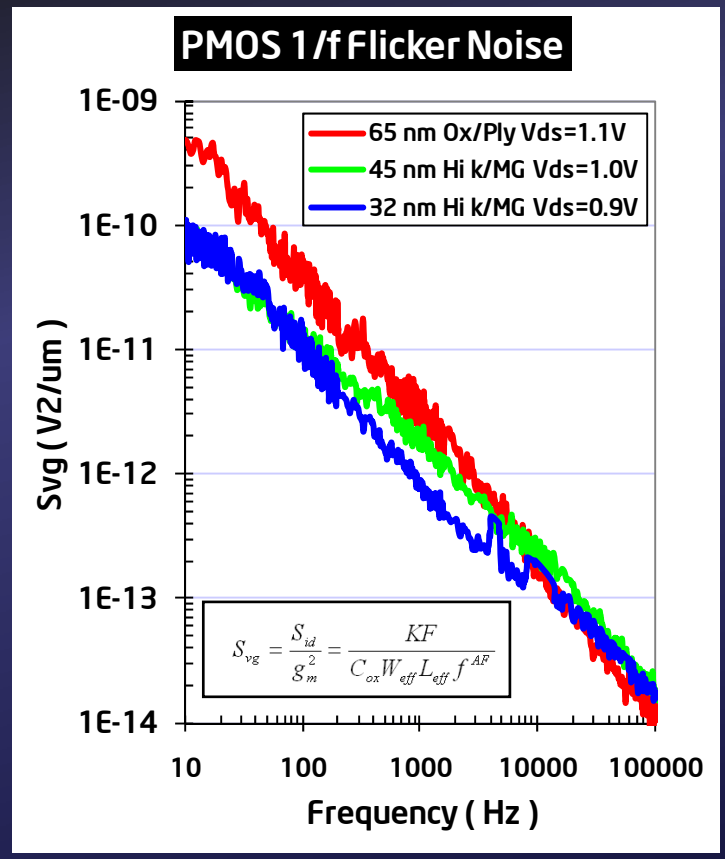
1/f Flicker Noise

Hi k/Metal Gt.









65 (poly/ox) /45/32 nm (high k/metal gate) 1/f flicker noise trend shows healthy Si/dielectric interfaces and no degradation from high-k/metal gate processing, critical for analog circuits

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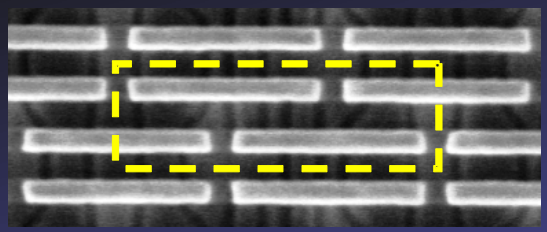
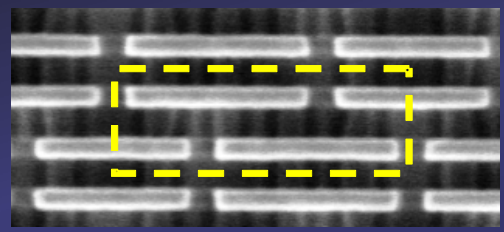
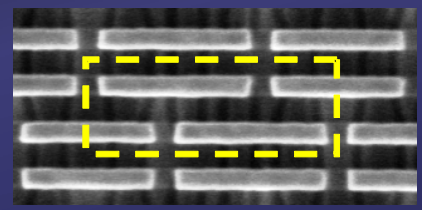
6T SRAM Bit Cells



High Speed
0.199 um^2
3.66 Mb/mm2



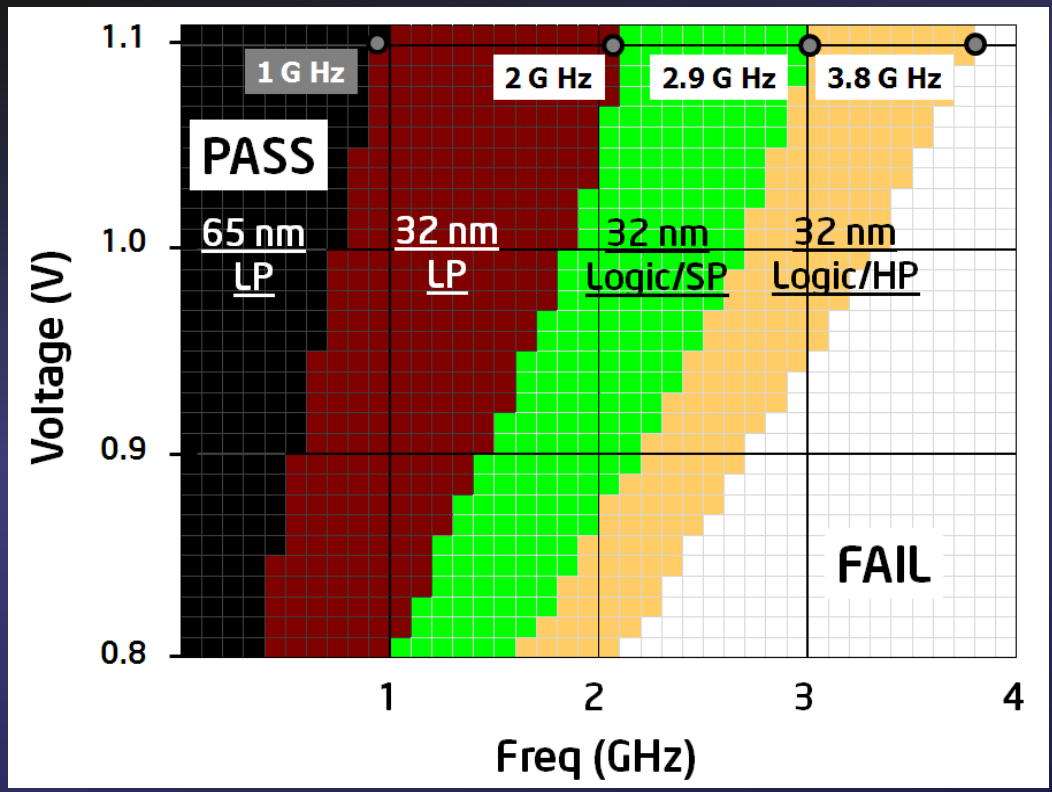
Low Voltage
0.171 um^2
4.10 Mb/mm2



High Density
0.148 um^2
4.62 Mb/mm2

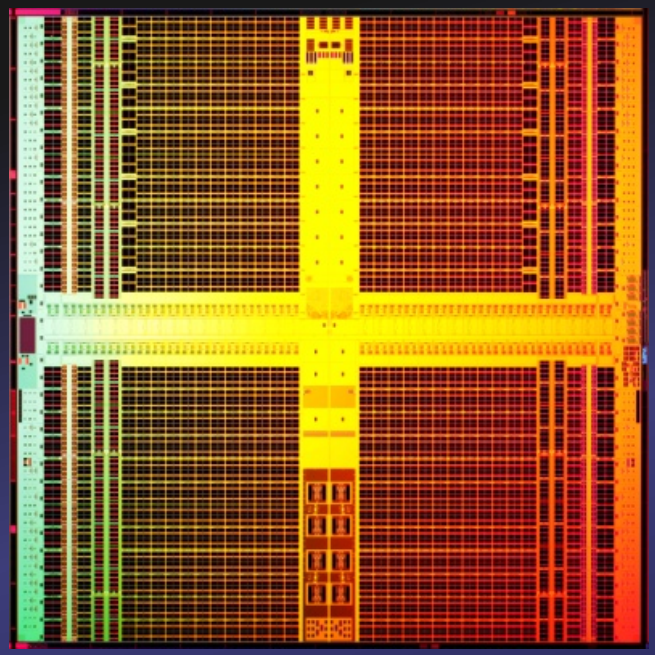
Multiple SRAM bit cells offered for high speed, low voltage and high density SoC applications. Highest reported array density

6T SRAM Performance – Shmoo Plot

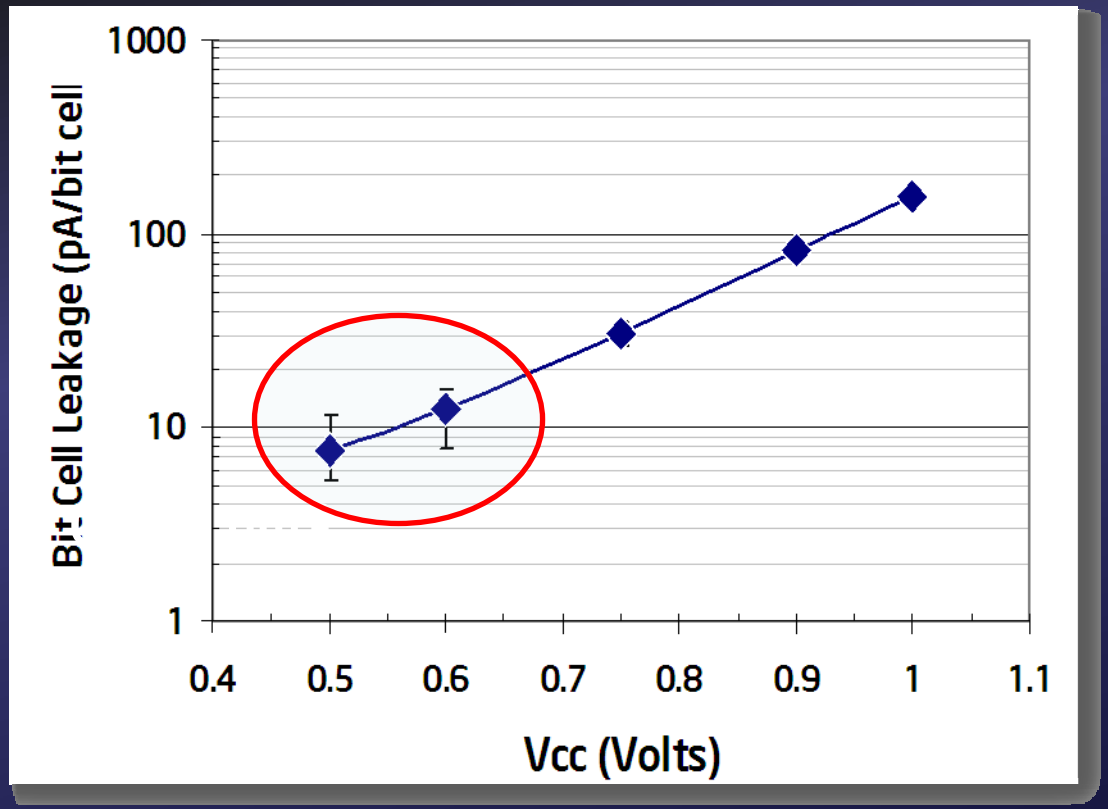


All bit cells are capable of supporting high performance needs.
32 nm LP can operate up to 2 GHz, 2x faster than 65 nm LP

6T SRAM Vccmin and Leakages

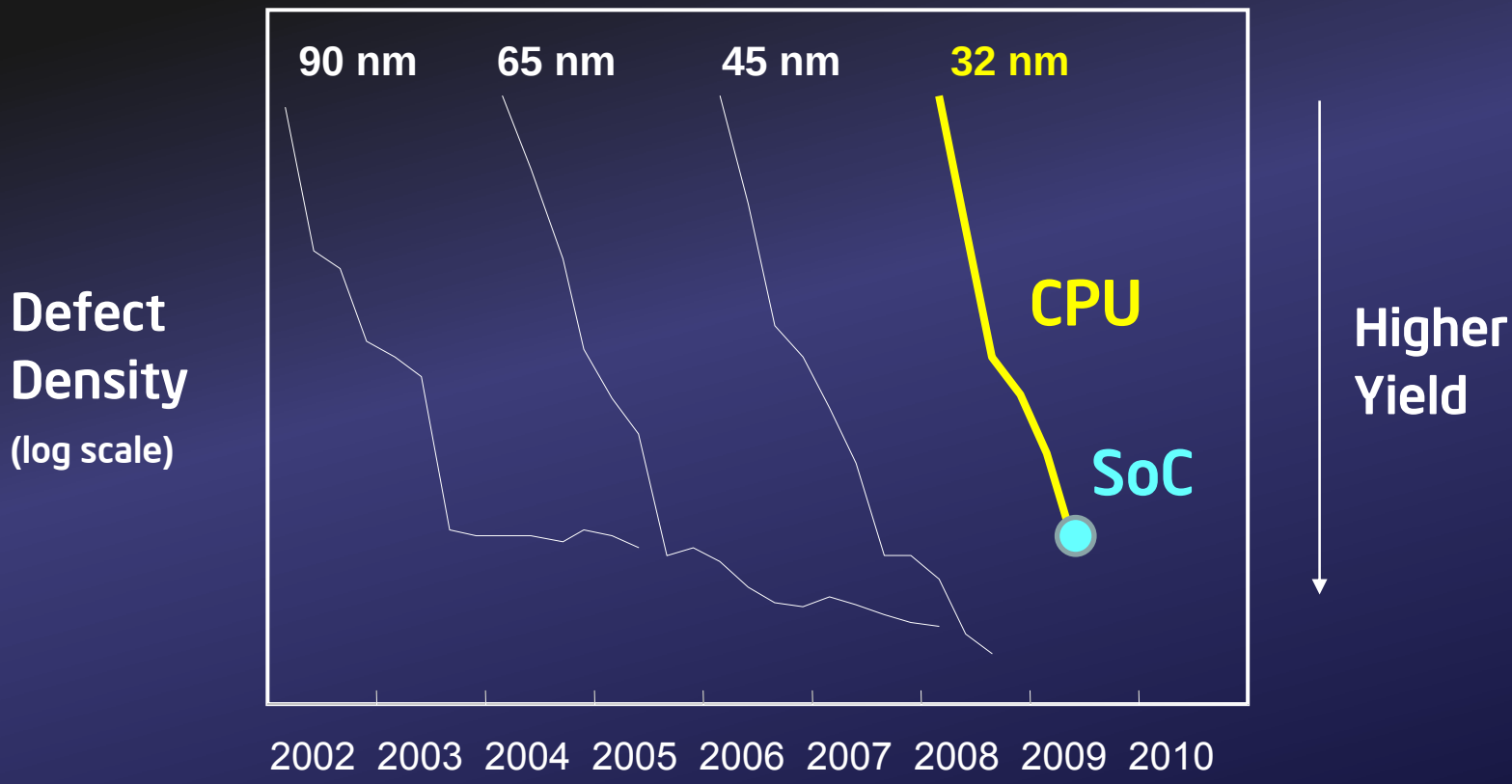


Die photo of 6T SRAM test chip with 291 Mbits



Low bit cell leakages (< 20 pA/cells) at low retention Vccmin

32 nm Yield Trend – CPU and SoC



SoC process has the same low defect density as CPU process

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Summary

- 32 nm high-k/metal gate technology has been optimized for high performance/low power System-On-Chip (SOC) platform
- A new triple transistor architecture provides record drive currents and low leakages spanning 4 orders of magnitude of leakage
- Tightest reported gate pitch and highest reported SRAM array density of any 32nm or 28nm technology
- Other SOC device elements (resistors, inductors, capacitors, diodes, and varactors) all exhibit well controlled performance and reliability

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- Technology CAD
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- Assembly & Test Technology Development
- Intel Labs/RIR

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