

```
-- Boundary-Scan Description Language (BSDL) file
-- Manufacturer: Intel Corporation
-- Component : Millbrook-1 Memory Buffer
-- Package(s) : BGA (Ball Grid Array)
-- Version : For MB1 C0-Step (Rev0.3)
-- Date : 06/18/2009
-- Entity name : mb1_top (Based on top level verilog module)
```

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```
-- This BSDL file has been syntax checked against the Scan Port Driver Tool
-- from Agilent("Revision 3070 07.00p").
```

Revision History

NOTES:

```
-- There is a sequencing requirement for VCCPWRGOOD and VDDPWRGOOD signals.
-- It needs to follow the timing diagram titled "Cold Power Up Reset"
-- in Chapter titled "Resets" of the Millbrook-1 EDS.
```

```
entity mb1_top is
```

```
generic(PHYSICAL_PIN_MAP : string := "bga");
```

```
port(
```

```
-- INPUT DECLARATIONS
```

```
CLK133N      : linkage bit;
CLK133P      : linkage bit;
FBDSBI_CLKN  : in      bit;
FBDSBI_CLKP  : in      bit;
FBDSBIN      : in      bit_vector (10 downto 0);
FBDSBIP      : in      bit_vector (10 downto 0);
```

```
-- OUTPUT DECLARATIONS
```

```
FBDCCMP      : linkage bit;
FBDNBOCLKN   : buffer  bit;
FBDNBOCLKP   : buffer  bit;
FBDNBON      : buffer  bit_vector ( 13 downto 0);
FBDNBOP      : buffer  bit_vector ( 13 downto 0);
```

```
-- INOUT DECLARATIONS
```

```
DDROA        : buffer  bit_vector ( 15 downto 0);
DDROBA       : buffer  bit_vector (  2 downto 0);
DDROCAS_N    : buffer  bit;
DDROCB       : buffer  bit_vector (  7 downto 0);
DDROCKE      : buffer  bit_vector (  3 downto 0);
DDROCLKN     : buffer  bit_vector (  1 downto 0);
DDROCLKP     : buffer  bit_vector (  1 downto 0);
DDROCS_N     : buffer  bit_vector (  7 downto 0);
DDRODQ       : buffer  bit_vector ( 63 downto 0);
DDRODQSN     : buffer  bit_vector ( 17 downto 0);
DDRODQSP     : buffer  bit_vector ( 17 downto 0);
DDROERR_N    : in      bit_vector (  1 downto 0);
DDROEVENT_N  : inout   bit;
DDROODT      : buffer  bit_vector (  3 downto 0);
DDROPAR      : buffer  bit;
DDRORAS_N    : buffer  bit;
DDRORASET_N  : buffer  bit;
DDR0WE_N     : buffer  bit;
DDR1A        : buffer  bit_vector ( 15 downto 0);
DDR1BA       : buffer  bit_vector (  2 downto 0);
DDR1CAS_N    : buffer  bit;
DDR1CB       : buffer  bit_vector (  7 downto 0);
DDR1CKE      : buffer  bit_vector (  3 downto 0);
DDR1CLKN     : buffer  bit_vector (  1 downto 0);
DDR1CLKP     : buffer  bit_vector (  1 downto 0);
DDR1CS_N     : buffer  bit_vector (  7 downto 0);
DDR1DQ       : buffer  bit_vector ( 63 downto 0);
DDR1DQSN     : buffer  bit_vector ( 17 downto 0);
DDR1DQSP     : buffer  bit_vector ( 17 downto 0);
DDR1ERR_N    : in      bit_vector (  1 downto 0);
DDR1EVENT_N  : inout   bit;
DDR10DT      : buffer  bit_vector (  3 downto 0);
DDR1PAR      : buffer  bit;
```

```

MB1_BGA_BSDL[1].uni x. r03. txt
DDR1RAS_N      : buffer bit;
DDR1RESET_N    : buffer bit;
DDR1WE_N       : buffer bit;
DDRCOMP        : linkage bit_vector ( 2 downto 0);
LAI EV         : inout bit_vector ( 3 downto 0);
LAI MODE_N     : inout bit;
LAI SCL        : inout bit;
LAI SDA        : inout bit;
RST_N          : in bit; -- Compliance Pin
SAO            : inout bit;
SCL            : inout bit;
SDA            : inout bit;
TCK            : in bit;
TDI            : in bit;
TDO            : out bit;
TMS            : in bit;
TRST_N         : in bit;
VCC1P1         : linkage bit_vector ( 28 downto 0);
VCCFBD1P1      : linkage bit_vector ( 4 downto 0);
VCCPWRG00D     : in bit; -- Compliance Pin
VDD1P5         : linkage bit_vector ( 41 downto 0);
VDDPWRG00D     : in bit; -- Compliance Pin
VREG1P8        : linkage bit;
VSS            : linkage bit_vector (151 downto 0);
RSVD           : linkage bit_vector ( 37 downto 0)

```

```
);
```

```
use STD_1149_1_2001.all;
```

```
attribute COMPONENT_CONFORMANCE of mb1_top : entity is "STD_1149_1_1993";
```

```
attribute PIN_MAP of mb1_top : entity is PHYSICAL_PIN_MAP;
```

```
constant bga : PIN_MAP_STRING :=
```

```

" VSS      : (Y9,      " &
"          Y5,        " &
"          Y26,       " &
"          Y21,       " &
"          Y2,        " &
"          Y19,       " &
"          Y17,       " &
"          Y15,       " &
"          Y13,       " &
"          Y11,       " &
"          W7,        " &
"          W3,        " &
"          W27,       " &
"          W22,       " &
"          V28,       " &
"          V25,       " &
"          V22,       " &
"          V20,       " &
"          V1,        " &
"          U8,        " &
"          U5,        " &
"          U21,       " &
"          U2,        " &
"          U18,       " &
"          U16,       " &
"          U14,       " &
"          U12,       " &

```

"	T6,	"	&
"	T27,	"	&
"	T24,	"	&
"	T17,	"	&
"	T15,	"	&
"	T13,	"	&
"	R4,	"	&
"	R28,	"	&
"	R18,	"	&
"	R16,	"	&
"	R14,	"	&
"	R12,	"	&
"	R10,	"	&
"	R1,	"	&
"	P8,	"	&
"	P5,	"	&
"	P29,	"	&
"	P26,	"	&
"	P23,	"	&
"	P20,	"	&
"	P2,	"	&
"	P17,	"	&
"	P15,	"	&
"	P13,	"	&
"	N9,	"	&
"	N27,	"	&
"	N24,	"	&
"	N21,	"	&
"	N18,	"	&
"	N16,	"	&
"	N14,	"	&
"	N12,	"	&
"	M7,	"	&
"	M4,	"	&
"	M28,	"	&
"	M25,	"	&
"	M17,	"	&
"	M15,	"	&
"	M13,	"	&
"	M10,	"	&
"	L8,	"	&
"	L5,	"	&
"	L29,	"	&
"	L23,	"	&
"	L20,	"	&
"	L2,	"	&
"	L18,	"	&
"	L16,	"	&
"	L14,	"	&
"	L12,	"	&
"	K6,	"	&
"	K3,	"	&
"	K27,	"	&
"	K24,	"	&
"	K21,	"	&
"	K17,	"	&
"	K15,	"	&
"	K13,	"	&
"	J28,	"	&
"	J18,	"	&
"	J16,	"	&
"	J14,	"	&
"	J12,	"	&

```

" J10, " &
" J1, " &
" H8, " &
" H5, " &
" H26, " &
" H23, " &
" H2, " &
" G3, " &
" G27, " &
" G24, " &
" G20, " &
" F7, " &
" F4, " &
" F28, " &
" F17, " &
" F1, " &
" E9, " &
" E29, " &
" E26, " &
" E2, " &
" E19, " &
" D3, " &
" D27, " &
" D21, " &
" D11, " &
" C29, " &
" C23, " &
" C13, " &
" B5, " &
" B25, " &
" B2, " &
" B15, " &
" AC9, " &
" AC7, " &
" AC6, " &
" AC27, " &
" AC21, " &
" AC19, " &
" AC17, " &
" AC15, " &
" AC13, " &
" AC11, " &
" AB23, " &
" AB2, " &
" AA8, " &
" AA6, " &
" AA4, " &
" AA29, " &
" AA25, " &
" AA22, " &
" AA20, " &
" AA18, " &
" AA16, " &
" AA14, " &
" AA12, " &
" AA10, " &
" A7, " &
" A27, " &
" A17, " &
" J9, " &
" H19, " &
" G12), " &
" VREG1P8 : AC23, " &

```

```

" VDDPWRGOOD      : K10,
" VDD1P5           : (Y7,
"                  W24,
"                  V4,
"                  U29,
"                  U26,
"                  T9,
"                  T3,
"                  R7,
"                  R25,
"                  R22,
"                  N6,
"                  N3,
"                  M22,
"                  M1,
"                  L26,
"                  K9,
"                  J7,
"                  J4,
"                  J25,
"                  J22,
"                  H29,
"                  G21,
"                  G10,
"                  F25,
"                  F12,
"                  E23,
"                  E14,
"                  D6,
"                  D16,
"                  C8,
"                  C26,
"                  C19,
"                  C1,
"                  B28,
"                  B20,
"                  B10,
"                  AC3,
"                  AB28,
"                  AA1,
"                  A3,
"                  A22,
"                  A12),
" VCCPWRGOOD       : L10,
" VCCFBD1P1        : (V18,
"                  V16,
"                  V14,
"                  V12,
"                  V10),
" VCC1P1           : (U17,
"                  U15,
"                  U13,
"                  T18,
"                  T16,
"                  T14,
"                  T12,
"                  R17,
"                  R15,
"                  R13,
"                  P18,
"                  P16,
"                  P14,
"                  P12,

```

```

" N17, " &
" N15, " &
" N13, " &
" M18, " &
" M16, " &
" M14, " &
" M12, " &
" L17, " &
" L15, " &
" L13, " &
" K18, " &
" K16, " &
" K14, " &
" K12, " &
" J17), " &
" TRST_N : H12, " &
" TMS : K11, " &
" TDO : H11, " &
" TDI : L11, " &
" TCK : M11, " &
" SDA : K19, " &
" SCL : L19, " &
" SA0 : H18, " &
" RST_N : J19, " &
" RSVD : (V8, " &
" U9, " &
" U20, " &
" U19, " &
" J15, " &
" J13, " &
" AB6, " &
" V11, " &
" AB21, " &
" W19, " &
" W11, " &
" AA21, " &
" V19, " &
" U10, " &
" U11, " &
" T10, " &
" T11, " &
" G15, " &
" G16, " &
" F20, " &
" D20, " &
" B14, " &
" C15, " &
" A14, " &
" C16, " &
" C17, " &
" E15, " &
" C18, " &
" D15, " &
" H13, " &
" H14, " &
" G13, " &
" G14, " &
" N10, " &
" N11, " &
" J11, " &
" H10, " &
" T19), " &
" LAI SDA : H16, " &

```

```

" LAI SCL          : H17,
" LAI MODE_N       : H15,
" LAI EV           : (R19,
"                  M19,
"                  N19,
"                  P19),
" FBDSBI P         : (W21,
"                  V15,
"                  W20,
"                  Y18,
"                  W17,
"                  W16,
"                  V13,
"                  Y12,
"                  Y10,
"                  V9,
"                  W8),
" FBDSBI N         : (V21,
"                  W15,
"                  Y20,
"                  W18,
"                  V17,
"                  Y16,
"                  W13,
"                  W12,
"                  W10,
"                  W9,
"                  Y8),
" FBDSBI CLKP      : Y14,
" FBDSBI CLKN      : W14,
" FBDNBOP          : (AA13,
"                  AB15,
"                  AC22,
"                  AC20,
"                  AB19,
"                  AC18,
"                  AB17,
"                  AC16,
"                  AB12,
"                  AA11,
"                  AB10,
"                  AA9,
"                  AB8,
"                  AA7),
" FBDNBON          : (AB13,
"                  AA15,
"                  AB22,
"                  AB20,
"                  AA19,
"                  AB18,
"                  AA17,
"                  AB16,
"                  AC12,
"                  AB11,
"                  AC10,
"                  AB9,
"                  AC8,
"                  AB7),
" FBDNBCLKP        : AB14,
" FBDNBCLKN        : AC14,
" FBDCDCMP         : R11,
" DDRCOMP          : (G11,
"                  H9,

```



```

"      G9),
" DDR1WE_N      : D10,
" DDR1RESET_N   : D24,
" DDR1RAS_N     : C10,
" DDR1PAR       : E12,
" DDR1ODT       : (E7,
"               D8,
"               G7,
"               F9),
" DDR1EVENT_N   : F11,
" DDR1ERR_N     : (G18,
"               G17),
" DDR1DQ        : (V7,
"               Y4,
"               T7,
"               T8,
"               W6,
"               Y6,
"               U6,
"               U7,
"               P9,
"               P7,
"               N5,
"               N7,
"               R9,
"               R8,
"               P4,
"               N4,
"               M5,
"               M6,
"               M9,
"               L9,
"               N8,
"               M3,
"               M8,
"               K7,
"               K5,
"               J6,
"               F5,
"               H7,
"               K8,
"               J8,
"               G4,
"               G5,
"               H21,
"               H22,
"               K23,
"               K22,
"               H20,
"               J20,
"               K25,
"               L25,
"               N25,
"               N26,
"               M20,
"               N20,
"               L24,
"               M24,
"               L21,
"               M21,
"               R27,
"               R26,
"               T20,

```

```

"      R20,      " &
"      P24,      " &
"      P25,      " &
"      R21,      " &
"      P21,      " &
"      U22,      " &
"      U24,      " &
"      Y22,      " &
"      AA23,     " &
"      T21,      " &
"      T23,      " &
"      Y24,      " &
"      Y23),     " &
" DDR1DQSP      : (F24,      " &
"      V5,       " &
"      P6,       " &
"      L7,       " &
"      H6,       " &
"      J23,      " &
"      N22,      " &
"      T22,      " &
"      W23,      " &
"      E24,      " &
"      W5,       " &
"      T5,       " &
"      L4,       " &
"      J3,       " &
"      J21,      " &
"      L22,      " &
"      R24,      " &
"      U23),     " &
" DDR1DQSN      : (F26,      " &
"      V6,       " &
"      R6,       " &
"      L6,       " &
"      H4,       " &
"      J24,      " &
"      N23,      " &
"      P22,      " &
"      V23,      " &
"      E25,      " &
"      W4,       " &
"      R5,       " &
"      K4,       " &
"      J5,       " &
"      K20,      " &
"      M23,      " &
"      R23,      " &
"      V24),     " &
" DDR1CS_N      : (F6,       " &
"      G6,       " &
"      E8,       " &
"      D9,       " &
"      E6,       " &
"      E5,       " &
"      F8,       " &
"      G8),      " &
" DDR1CLKP      : (D17,      " &
"      F14),     " &
" DDR1CLKN      : (D18,      " &
"      F13),     " &
" DDR1CKE       : (F22,      " &
"      F23,      " &

```

```

"      G22,
"      G19),
" DDR1CB      : (C27,
"              D26,
"              H25,
"              H24,
"              C25,
"              D25,
"              G25,
"              G23),
" DDR1CAS_N   : E10,
" DDR1BA      : (D23,
"              C11,
"              E11),
" DDR1A       : (F21,
"              E22,
"              F10,
"              D22,
"              E20,
"              C12,
"              E21,
"              D19,
"              F19,
"              F18,
"              E18,
"              E17,
"              E16,
"              F15,
"              F16,
"              D12),
" DDROWE_N    : B9,
" DDRORESET_N : A25,
" DDRORAS_N   : A9,
" DDROPAR     : B13,
" DDROODT     : (A5,
"              A6,
"              B6,
"              D7),
" DDROEVENT_N : A13,
" DDROERR_N   : (C21,
"              C20),
" DDRODQ      : (AC4,
"              AA5,
"              W2,
"              W1,
"              AC5,
"              AB5,
"              Y3,
"              Y1,
"              V2,
"              U3,
"              P3,
"              T4,
"              U4,
"              V3,
"              R3,
"              P1,
"              M2,
"              L3,
"              G1,
"              G2,
"              N2,
"              N1,

```

"	H1,	"	&
"	H3,	"	&
"	F2,	"	&
"	E3,	"	&
"	B3,	"	&
"	B4,	"	&
"	E4,	"	&
"	F3,	"	&
"	C3,	"	&
"	D4,	"	&
"	J26,	"	&
"	H27,	"	&
"	L27,	"	&
"	M26,	"	&
"	F27,	"	&
"	G26,	"	&
"	K26,	"	&
"	L28,	"	&
"	N28,	"	&
"	N29,	"	&
"	U28,	"	&
"	V29,	"	&
"	M27,	"	&
"	M29,	"	&
"	T29,	"	&
"	U27,	"	&
"	U25,	"	&
"	V26,	"	&
"	W25,	"	&
"	Y25,	"	&
"	T25,	"	&
"	T26,	"	&
"	Y29,	"	&
"	W26,	"	&
"	AA27,	"	&
"	AB27,	"	&
"	AC24,	"	&
"	AB24,	"	&
"	Y27,	"	&
"	AA28,	"	&
"	AC25,	"	&
"	AA24),	"	&
" DDR0DQSP	: (E28,	"	&
"	AA2,	"	&
"	R2,	"	&
"	J2,	"	&
"	C2,	"	&
"	K29,	"	&
"	T28,	"	&
"	Y28,	"	&
"	AB25,	"	&
"	D28,	"	&
"	AB4,	"	&
"	U1,	"	&
"	L1,	"	&
"	E1,	"	&
"	J27,	"	&
"	P27,	"	&
"	V27,	"	&
"	AA26),	"	&
" DDR0DQSN	: (E27,	"	&
"	AA3,	"	&
"	T1,	"	&

```

"      K1,      " &
"      D1,      " &
"      K28,     " &
"      R29,     " &
"      W29,     " &
"      AC26,    " &
"      D29,     " &
"      AB3,     " &
"      T2,      " &
"      K2,      " &
"      D2,      " &
"      J29,     " &
"      P28,     " &
"      W28,     " &
"      AB26),   " &
" DDROCS_N      : (A4,      " &
"                D5,      " &
"                C6,      " &
"                B7,      " &
"                C5,      " &
"                C4,      " &
"                C7,      " &
"                C9),     " &
" DDROCLKP      : (C14,    " &
"                D13),    " &
" DDROCLKN      : (D14,    " &
"                E13),    " &
" DDROCKE       : (A24,    " &
"                C24,     " &
"                B24,     " &
"                C22),    " &
" DDROCB        : (B27,    " &
"                C28,     " &
"                G29,     " &
"                H28,     " &
"                A26,     " &
"                B26,     " &
"                F29,     " &
"                G28),    " &
" DDROCAS_N     : A8,      " &
" DDROBA        : (B22,    " &
"                B11,     " &
"                A10),    " &
" DDROA         : (B23,    " &
"                A23,     " &
"                B8,      " &
"                B21,     " &
"                A20,     " &
"                A11,     " &
"                A21,     " &
"                A19,     " &
"                B19,     " &
"                B18,     " &
"                A18,     " &
"                B17,     " &
"                B16,     " &
"                A15,     " &
"                A16,     " &
"                B12),    " &
" CLK133P       : P10,     " &
" CLK133N       : P11 ";

```

attribute PORT_GROUPING of mb1_top : entity is

```

MB1_BGA_BSDL[1].uni x. r03. txt
"Di fferenti al _Vol tage ((FBDNBOP(0), FBDNBON(0)) , "&
" (FBDNBOP(1), FBDNBON(1)) , "&
" (FBDNBOP(2), FBDNBON(2)) , "&
" (FBDNBOP(3), FBDNBON(3)) , "&
" (FBDNBOP(4), FBDNBON(4)) , "&
" (FBDNBOP(5), FBDNBON(5)) , "&
" (FBDNBOP(6), FBDNBON(6)) , "&
" (FBDNBOP(7), FBDNBON(7)) , "&
" (FBDNBOP(8), FBDNBON(8)) , "&
" (FBDNBOP(9), FBDNBON(9)) , "&
" (FBDNBOP(10), FBDNBON(10)) , "&
" (FBDNBOP(11), FBDNBON(11)) , "&
" (FBDNBOP(12), FBDNBON(12)) , "&
" (FBDNBOP(13), FBDNBON(13)) , "&
" (FBDNBOPCLKP, FBDNBOPCLKN )) , "&

attribute TAP_SCAN_IN of TDI : signal is true;
attribute TAP_SCAN_MODE of TMS : signal is true;
attribute TAP_SCAN_OUT of TDO : signal is true;
attribute TAP_SCAN_CLOCK of TCK : signal is (40.0e6, BOTH);
attribute TAP_SCAN_RESET of TRST_N : signal is true;

-- This section specifies compliance enable description (Section 4.8)
attribute COMPLIANCE_PATTERNS of mb1_top : entity is
"(VCCPWGOOD, VDDPWGOOD, RST_N) (110)";

attribute INSTRUCTION_LENGTH of mb1_top : entity is 7;
attribute INSTRUCTION_OPCODE of mb1_top : entity is
"extest (0000000), " &
"sample (0000001), " &
"idcode (0000010), " &
"clamp (0000100), " &
"hi ghz (0001000), " &
"bypass (1111111), " &
"reserved (0110100, 0110101, 1000011, 1000110, 1000111, " &
" 1001000, 1001001, 1001101, 1001110, 1001111, " &
" 1010000, 1010001, 1010010, 1010011, 1010101, " &
" 1010110, 1010111, 1100000, 1100001, 1100010, " &
" 1100011, 1110000)";

attribute INSTRUCTION_CAPTURE of mb1_top : entity is "0000001";
attribute INSTRUCTION_PRIVATE of mb1_top : entity is "reserved";

attribute IDCODE_REGISTER of mb1_top : entity is
"1000" & -- Version Number (C0-Step)
"111110" & -- Product Segment
"000000" & -- Product Type
"000010" & -- Component Number
"000001001" & -- Manufacturer ID
"1"; -- Required by IEEE Std. to be 1

attribute REGISTER_ACCESS of mb1_top : entity is
"BOUNDARY (extest, sample), " &
"DEVICE_ID (idcode), " &
"BYPASS (bypass, hi ghz)";

attribute BOUNDARY_LENGTH of mb1_top : entity is 439;
attribute BOUNDARY_REGISTER of mb1_top : entity is
-- GC=1/0, RX is input; GC=0, RX is output GC has to be 0 for RX to be output, for
input we do not care.
-- num cell port function safe
[ccell disval rslt]

```

```

-
" 438( bc_1, *, control ,
0), " &
" 437( bc_7, SCL, bi di r, X,
438, 0, WEAK1), " &
" 436( bc_1, *, control ,
0), " &
" 435( bc_7, LAI EV(0), bi di r, X,
436, 0, WEAK1), " &
" 434( bc_1, *, control ,
0), " &
" 433( bc_7, LAI EV(1), bi di r, X,
434, 0, WEAK1), " &
" 432( bc_1, *, control ,
0), " &
" 431( bc_7, LAI EV(2), bi di r, X,
432, 0, WEAK1), " &
" 430( bc_1, *, i n t e r n a l ,
0), " &
" 429( bc_1, *, i n t e r n a l ,
X), " &
" 428( bc_1, *, control ,
0), " &
" 427( bc_7, SDA, bi di r, X,
428, 0, WEAK1), " &
" 426( bc_1, *, i n t e r n a l ,
0), " &
" 425( bc_1, *, i n t e r n a l ,
X), " &
" 424( bc_1, *, control ,
0), " &
" 423( bc_7, SA0, bi di r, X,
424, 0, Z), " &
" 422( bc_1, *, control ,
0), " &
" 421( bc_7, LAI MODE_N, bi di r, X,
422, 0, Z), " &
" 420( bc_1, *, control ,
0), " &
" 419( bc_7, LAI EV(3), bi di r, X,
420, 0, WEAK1), " &
" 418( bc_1, *, control ,
0), " &
" 417( bc_7, LAI SCL, bi di r, X,
418, 0, WEAK1), " &
" 416( bc_1, *, i n t e r n a l ,
0), " &
" 415( bc_1, *, i n t e r n a l ,
X), " &
" 414( bc_1, *, i n t e r n a l ,
0), " &
" 413( bc_1, *, i n t e r n a l ,
X), " &
" 412( bc_1, *, control ,
0), " &
" 411( bc_7, DDROEVENT_N, bi di r, X, 412,
0, Z), " &
" 410( bc_1, *, control ,
0), " &
" 409( bc_7, LAI SDA, bi di r, X,
410, 0, WEAK1), " &
" 408( bc_1, *, control ,
0), " &

```

```

" 407( bc_7, DDR1EVENT_N, bi di r, X, 408,
0, Z), " &
" 406( bc_1, *, i n t e r n a l ,
0), " &
" 405( bc_1, *, i n t e r n a l ,
X), " &
" 404( bc_1, *, i n t e r n a l ,
X), " &
" 403( bc_1, *, i n t e r n a l ,
X), " &
" 402( bc_10, DDR0DQ(57), output2, X), "
&
" 401( bc_10, DDR0DQ(56), output2, X), "
&
" 400( bc_10, DDR0DQ(59), output2, X), "
&
" 399( bc_10, DDR0DQ(58), output2, X), "
&
" 398( bc_0, DDR0DQSN(7), output2, X), " &
" 397( bc_0, DDR0DQSP(7), output2, X), " &
" 396( bc_0, DDR0DQSN(16), output2, X), " &
" 395( bc_0, DDR0DQSP(16), output2, X), " &
" 394( bc_10, DDR0DQ(61), output2, X), "
&
" 393( bc_10, DDR0DQ(60), output2, X), "
&
" 392( bc_10, DDR0DQ(63), output2, X), "
&
" 391( bc_10, DDR0DQ(62), output2, X), "
&
" 390( bc_1, *, i n t e r n a l ,
X), " &
" 389( bc_10, DDR1DQ(57), output2, X), "
&
" 388( bc_10, DDR1DQ(56), output2, X), "
&
" 387( bc_10, DDR1DQ(59), output2, X), "
&
" 386( bc_10, DDR1DQ(58), output2, X), "
&
" 385( bc_0, DDR1DQSN(7), output2, X), " &
" 384( bc_0, DDR1DQSP(7), output2, X), " &
" 383( bc_0, DDR1DQSN(16), output2, X), " &
" 382( bc_0, DDR1DQSP(16), output2, X), " &
" 381( bc_10, DDR1DQ(60), output2, X), "
&
" 380( bc_10, DDR1DQ(61), output2, X), "
&
" 379( bc_10, DDR1DQ(63), output2, X), "
&
" 378( bc_10, DDR1DQ(62), output2, X), "
&
" 377( bc_1, *, i n t e r n a l ,
X), " &
" 376( bc_10, DDR0DQ(49), output2, X), "
&
" 375( bc_10, DDR0DQ(48), output2, X), "
&
" 374( bc_10, DDR0DQ(50), output2, X), "
&
" 373( bc_10, DDR0DQ(51), output2, X), "
&
" 372( bc_0, DDR0DQSN(6), output2, X), " &

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MB1_BGA_BSDL[1].uni x. r03. txt
" 371( bc_0, DDR0DQSP(6), output2, X), " &
" 370( bc_0, DDR0DQSN(15), output2, X), " &
" 369( bc_0, DDR0DQSP(15), output2, X), " &
" 368( bc_10, DDR0DQ(53), output2, X), "
&
" 367( bc_10, DDR0DQ(55), output2, X), "
&
" 366( bc_10, DDR0DQ(54), output2, X), "
&
" 365( bc_10, DDR0DQ(52), output2, X), "
&
" 364( bc_1, *, i n t e r n a l ,
X), " &
" 363( bc_10, DDR1DQ(50), output2, X), "
&
" 362( bc_10, DDR1DQ(48), output2, X), "
&
" 361( bc_10, DDR1DQ(49), output2, X), "
&
" 360( bc_10, DDR1DQ(51), output2, X), "
&
" 359( bc_0, DDR1DQSN(6), output2, X), " &
" 358( bc_0, DDR1DQSP(6), output2, X), " &
" 357( bc_0, DDR1DQSN(15), output2, X), " &
" 356( bc_0, DDR1DQSP(15), output2, X), " &
" 355( bc_10, DDR1DQ(55), output2, X), "
&
" 354( bc_10, DDR1DQ(54), output2, X), "
&
" 353( bc_10, DDR1DQ(52), output2, X), "
&
" 352( bc_10, DDR1DQ(53), output2, X), "
&
" 351( bc_1, *, i n t e r n a l ,
X), " &
" 350( bc_10, DDR0DQ(40), output2, X), "
&
" 349( bc_10, DDR0DQ(41), output2, X), "
&
" 348( bc_10, DDR0DQ(42), output2, X), "
&
" 347( bc_10, DDR0DQ(43), output2, X), "
&
" 346( bc_0, DDR0DQSN(5), output2, X), " &
" 345( bc_0, DDR0DQSP(5), output2, X), " &
" 344( bc_0, DDR0DQSN(14), output2, X), " &
" 343( bc_0, DDR0DQSP(14), output2, X), " &
" 342( bc_10, DDR0DQ(44), output2, X), "
&
" 341( bc_10, DDR0DQ(45), output2, X), "
&
" 340( bc_10, DDR0DQ(46), output2, X), "
&
" 339( bc_10, DDR0DQ(47), output2, X), "
&
" 338( bc_1, *, i n t e r n a l ,
X), " &
" 337( bc_10, DDR1DQ(41), output2, X), "
&
" 336( bc_10, DDR1DQ(40), output2, X), "
&
" 335( bc_10, DDR1DQ(43), output2, X), "
&

```

```

" 334( bc_10, DDR1DQ(42), output2, X), "
&
" 333( bc_0, DDR1DQSN(5), output2, X), " &
" 332( bc_0, DDR1DQSP(5), output2, X), " &
" 331( bc_0, DDR1DQSN(14), output2, X), " &
" 330( bc_0, DDR1DQSP(14), output2, X), " &
" 329( bc_10, DDR1DQ(44), output2, X), "
&
" 328( bc_10, DDR1DQ(45), output2, X), "
&
" 327( bc_10, DDR1DQ(46), output2, X), "
&
" 326( bc_10, DDR1DQ(47), output2, X), "
&
" 325( bc_1, *, i n t e r n a l ,
X), " &
" 324( bc_10, DDR0DQ(33), output2, X), "
&
" 323( bc_10, DDR0DQ(32), output2, X), "
&
" 322( bc_10, DDR0DQ(35), output2, X), "
&
" 321( bc_10, DDR0DQ(34), output2, X), "
&
" 320( bc_0, DDR0DQSN(4), output2, X), " &
" 319( bc_0, DDR0DQSP(4), output2, X), " &
" 318( bc_0, DDR0DQSN(13), output2, X), " &
" 317( bc_0, DDR0DQSP(13), output2, X), " &
" 316( bc_10, DDR0DQ(36), output2, X), "
&
" 315( bc_10, DDR0DQ(37), output2, X), "
&
" 314( bc_10, DDR0DQ(39), output2, X), "
&
" 313( bc_10, DDR0DQ(38), output2, X), "
&
" 312( bc_1, *, i n t e r n a l , X), "
&
" 311( bc_10, DDR1DQ(35), output2, X), "
&
" 310( bc_10, DDR1DQ(34), output2, X), "
&
" 309( bc_10, DDR1DQ(33), output2, X), "
&
" 308( bc_10, DDR1DQ(32), output2, X), "
&
" 307( bc_0, DDR1DQSN(4), output2, X), " &
" 306( bc_0, DDR1DQSP(4), output2, X), " &
" 305( bc_0, DDR1DQSN(13), output2, X), " &
" 304( bc_0, DDR1DQSP(13), output2, X), " &
" 303( bc_10, DDR1DQ(36), output2, X), "
&
" 302( bc_10, DDR1DQ(38), output2, X), "
&
" 301( bc_10, DDR1DQ(37), output2, X), "
&
" 300( bc_10, DDR1DQ(39), output2, X), "
&
" 299( bc_1, *, i n t e r n a l ,
X), " &
" 298( bc_10, DDR0ODT(0), output2, X), "
&
" 297( bc_10, DDR0CS_N(1), output2, X), " &

```

```

MB1_BGA_BSDL[1]. uni x. r03. txt
" 296( bc_10, DDROCS_N(0), output2, X), " &
" 295( bc_10, DDROCS_N(4), output2, X), " &
" 294( bc_10, DDROODT(2), output2, X), "
&
" 293( bc_10, DDROCS_N(7), output2, X), " &
" 292( bc_10, DDROODT(1), output2, X), "
&
" 291( bc_10, DDROCS_N(3), output2, X), " &
" 290( bc_10, DDROODT(3), output2, X), "
&
" 289( bc_10, DDROCS_N(6), output2, X), " &
" 288( bc_10, DDROCS_N(5), output2, X), " &
" 287( bc_10, DDROCS_N(2), output2, X), " &
" 286( bc_1, *, i n t e r n a l ,
X), " &
" 285( bc_10, DDR1CS_N(1), output2, X), " &
" 284( bc_10, DDR1CS_N(4), output2, X), " &
" 283( bc_10, DDR1CS_N(5), output2, X), " &
" 282( bc_10, DDR1ODT(0), output2, X), "
&
" 281( bc_10, DDR1CS_N(0), output2, X), " &
" 280( bc_10, DDR1CS_N(6), output2, X), " &
" 279( bc_10, DDR1ODT(1), output2, X), "
&
" 278( bc_10, DDR1CS_N(2), output2, X), " &
" 277( bc_10, DDR1ODT(3), output2, X), "
&
" 276( bc_10, DDR1CS_N(3), output2, X), " &
" 275( bc_10, DDR1ODT(2), output2, X), "
&
" 274( bc_10, DDR1CS_N(7), output2, X), " &
" 273( bc_1, *, i n t e r n a l ,
X), " &
" 272( bc_1, *, i n t e r n a l ,
X), " &
" 271( bc_1, *, i n t e r n a l ,
X), " &
" 270( bc_1, *, i n t e r n a l ,
X), " &
" 269( bc_1, *, i n t e r n a l ,
X), " &
" 268( bc_10, DDR1CLKP(1), output2, X), " &
" 267( bc_10, DDR1CLKN(1), output2, X), " &
" 266( bc_1, *, i n t e r n a l ,
X), " &
" 265( bc_1, *, i n t e r n a l ,
X), " &
" 264( bc_1, *, i n t e r n a l ,
X), " &
" 263( bc_1, *, i n t e r n a l ,
X), " &
" 262( bc_10, DDR1CLKP(0), output2, X), " &
" 261( bc_10, DDR1CLKN(0), output2, X), " &
" 260( bc_1, *, i n t e r n a l ,
X), " &
" 259( bc_1, *, i n t e r n a l ,
X), " &
" 258( bc_1, *, i n t e r n a l ,
X), " &
" 257( bc_10, DDROCLKP(0), output2, X), " &
" 256( bc_10, DDROCLKN(0), output2, X), " &
" 255( bc_1, *, i n t e r n a l ,
X), " &

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" 254( bc_1, *, i n t e r n a l ,
X), " &
" 253( bc_1, *, i n t e r n a l ,
X), " &
" 252( bc_1, *, i n t e r n a l ,
X), " &
" 251( bc_10, DDROCLKP(1), output2, X), " &
" 250( bc_10, DDROCLKN(1), output2, X), " &
" 249( bc_1, *, i n t e r n a l ,
X), " &
" 248( bc_1, *, i n t e r n a l ,
X), " &
" 247( bc_1, *, i n t e r n a l ,
X), " &
" 246( bc_10, DDROA(13), output2, X), "
&
" 245( bc_10, DDROBA(1), output2, X), "
&
" 244( bc_10, DDROBA(0), output2, X), "
&
" 243( bc_10, DDROA(0), output2, X), "
&
" 242( bc_10, DDROPAR, output2, X), "
&
" 241( bc_10, DDROA(10), output2, X), "
&
" 240( bc_10, DDROA(1), output2, X), "
&
" 239( bc_10, DDROA(4), output2, X), "
&
" 238( bc_10, DDROA(2), output2, X), "
&
" 237( bc_10, DDROA(3), output2, X), "
&
" 236( bc_1, *, i n t e r n a l ,
X), " &
" 235( bc_10, DDR1A(10), output2, X), "
&
" 234( bc_10, DDR1A(0), output2, X), "
&
" 233( bc_10, DDR1BA(1), output2, X), "
&
" 232( bc_10, DDR1A(13), output2, X), "
&
" 231( bc_10, DDR1A(4), output2, X), "
&
" 230( bc_10, DDR1A(3), output2, X), "
&
" 229( bc_10, DDR1A(2), output2, X), "
&
" 228( bc_10, DDR1A(1), output2, X), "
&
" 227( bc_10, DDR1BA(0), output2, X), "
&
" 226( bc_10, DDR1PAR, output2, X), "
&
" 225( bc_1, *, i n t e r n a l ,
X), " &
" 224( bc_10, DDR0DQ(0), output2, X), "
&
" 223( bc_10, DDR0DQ(1), output2, X), "
&
" 222( bc_10, DDR0DQ(2), output2, X), "

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```

&
" 221( bc_10,          DDR0DQ(3),          output2,          X), "
&
" 220( bc_0,          DDR0DQSN(0),          output2,          X), " &
" 219( bc_0,          DDR0DQSP(0),          output2,          X), " &
" 218( bc_0,          DDR0DQSN(9),          output2,          X), " &
" 217( bc_0,          DDR0DQSP(9),          output2,          X), " &
" 216( bc_10,          DDR0DQ(5),          output2,          X), "
&
" 215( bc_10,          DDR0DQ(4),          output2,          X), "
&
" 214( bc_10,          DDR0DQ(6),          output2,          X), "
&
" 213( bc_10,          DDR0DQ(7),          output2,          X), "
&
" 212( bc_1,          *,          i n t e r n a l ,
X), " &
" 211( bc_10,          DDR1DQ(0),          output2,          X), "
&
" 210( bc_10,          DDR1DQ(1),          output2,          X), "
&
" 209( bc_10,          DDR1DQ(3),          output2,          X), "
&
" 208( bc_10,          DDR1DQ(2),          output2,          X), "
&
" 207( bc_0,          DDR1DQSN(0),          output2,          X), " &
" 206( bc_0,          DDR1DQSP(0),          output2,          X), " &
" 205( bc_0,          DDR1DQSN(9),          output2,          X), " &
" 204( bc_0,          DDR1DQSP(9),          output2,          X), " &
" 203( bc_10,          DDR1DQ(5),          output2,          X), "
&
" 202( bc_10,          DDR1DQ(4),          output2,          X), "
&
" 201( bc_10,          DDR1DQ(6),          output2,          X), "
&
" 200( bc_10,          DDR1DQ(7),          output2,          X), "
&
" 199( bc_1,          *,          i n t e r n a l ,
X), " &
" 198( bc_10,          DDR0DQ(8),          output2,          X), "
&
" 197( bc_10,          DDR0DQ(9),          output2,          X), "
&
" 196( bc_10,          DDR0DQ(11),          output2,          X), "
&
" 195( bc_10,          DDR0DQ(10),          output2,          X), "
&
" 194( bc_0,          DDR0DQSN(1),          output2,          X), " &
" 193( bc_0,          DDR0DQSP(1),          output2,          X), " &
" 192( bc_0,          DDR0DQSN(10),          output2,          X), " &
" 191( bc_0,          DDR0DQSP(10),          output2,          X), " &
" 190( bc_10,          DDR0DQ(13),          output2,          X), "
&
" 189( bc_10,          DDR0DQ(12),          output2,          X), "
&
" 188( bc_10,          DDR0DQ(14),          output2,          X), "
&
" 187( bc_10,          DDR0DQ(15),          output2,          X), "
&
" 186( bc_1,          *,          i n t e r n a l ,
X), " &
" 185( bc_10,          DDR1DQ(8),          output2,          X), "
&

```

```

" 184( bc_10,      DDR1DQ(9),      output2,      X), "
&
" 183( bc_10,      DDR1DQ(10),     output2,      X), "
&
" 182( bc_10,      DDR1DQ(11),     output2,      X), "
&
" 181( bc_0,      DDR1DQSN(1),     output2,      X), " &
" 180( bc_0,      DDR1DQSP(1),     output2,      X), " &
" 179( bc_0,      DDR1DQSN(10),    output2,      X), " &
" 178( bc_0,      DDR1DQSP(10),    output2,      X), " &
" 177( bc_10,     DDR1DQ(13),     output2,      X), "
&
" 176( bc_10,     DDR1DQ(12),     output2,      X), "
&
" 175( bc_10,     DDR1DQ(15),     output2,      X), "
&
" 174( bc_10,     DDR1DQ(14),     output2,      X), "
&
" 173( bc_1,      *,              i n t e r n a l ,
X), " &
" 172( bc_10,     DDR0DQ(17),     output2,      X), "
&
" 171( bc_10,     DDR0DQ(16),     output2,      X), "
&
" 170( bc_10,     DDR0DQ(18),     output2,      X), "
&
" 169( bc_10,     DDR0DQ(19),     output2,      X), "
&
" 168( bc_0,      DDR0DQSN(2),     output2,      X), " &
" 167( bc_0,      DDR0DQSP(2),     output2,      X), " &
" 166( bc_0,      DDR0DQSN(11),    output2,      X), " &
" 165( bc_0,      DDR0DQSP(11),    output2,      X), " &
" 164( bc_10,     DDR0DQ(21),     output2,      X), "
&
" 163( bc_10,     DDR0DQ(20),     output2,      X), "
&
" 162( bc_10,     DDR0DQ(22),     output2,      X), "
&
" 161( bc_10,     DDR0DQ(23),     output2,      X), "
&
" 160( bc_1,      *,              i n t e r n a l ,
X), " &
" 159( bc_10,     DDR1DQ(17),     output2,      X), "
&
" 158( bc_10,     DDR1DQ(16),     output2,      X), "
&
" 157( bc_10,     DDR1DQ(18),     output2,      X), "
&
" 156( bc_10,     DDR1DQ(19),     output2,      X), "
&
" 155( bc_0,      DDR1DQSN(2),     output2,      X), " &
" 154( bc_0,      DDR1DQSP(2),     output2,      X), " &
" 153( bc_0,      DDR1DQSN(11),    output2,      X), " &
" 152( bc_0,      DDR1DQSP(11),    output2,      X), " &
" 151( bc_10,     DDR1DQ(23),     output2,      X), "
&
" 150( bc_10,     DDR1DQ(20),     output2,      X), "
&
" 149( bc_10,     DDR1DQ(22),     output2,      X), "
&
" 148( bc_10,     DDR1DQ(21),     output2,      X), "
&
" 147( bc_1,      *,              i n t e r n a l ,

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X), " &
" 146( bc_10,          DDR0DQ(25),          output2,          X), "
&
" 145( bc_10,          DDR0DQ(24),          output2,          X), "
&
" 144( bc_10,          DDR0DQ(27),          output2,          X), "
&
" 143( bc_10,          DDR0DQ(26),          output2,          X), "
&
" 142( bc_0,           DDR0DQSN(3),          output2,          X), " &
" 141( bc_0,           DDR0DQSP(3),          output2,          X), " &
" 140( bc_0,           DDR0DQSN(12),         output2,          X), " &
" 139( bc_0,           DDR0DQSP(12),         output2,          X), " &
" 138( bc_10,          DDR0DQ(29),          output2,          X), "
&
" 137( bc_10,          DDR0DQ(28),          output2,          X), "
&
" 136( bc_10,          DDR0DQ(30),          output2,          X), "
&
" 135( bc_10,          DDR0DQ(31),          output2,          X), "
&
" 134( bc_1,           *,                      i n t e r n a l ,
X), " &
" 133( bc_10,          DDR1DQ(24),          output2,          X), "
&
" 132( bc_10,          DDR1DQ(26),          output2,          X), "
&
" 131( bc_10,          DDR1DQ(27),          output2,          X), "
&
" 130( bc_10,          DDR1DQ(25),          output2,          X), "
&
" 129( bc_0,           DDR1DQSN(3),          output2,          X), " &
" 128( bc_0,           DDR1DQSP(3),          output2,          X), " &
" 127( bc_0,           DDR1DQSN(12),         output2,          X), " &
" 126( bc_0,           DDR1DQSP(12),         output2,          X), " &
" 125( bc_10,          DDR1DQ(28),          output2,          X), "
&
" 124( bc_10,          DDR1DQ(29),          output2,          X), "
&
" 123( bc_10,          DDR1DQ(30),          output2,          X), "
&
" 122( bc_10,          DDR1DQ(31),          output2,          X), "
&
" 121( bc_1,           *,                      i n t e r n a l ,
X), " &
" 120( bc_10,          DDROCB(1),          output2,          X), "
&
" 119( bc_10,          DDROCB(0),          output2,          X), "
&
" 118( bc_10,          DDROCB(2),          output2,          X), "
&
" 117( bc_10,          DDROCB(3),          output2,          X), "
&
" 116( bc_0,           DDRODQSN(8),          output2,          X), " &
" 115( bc_0,           DDRODQSP(8),          output2,          X), " &
" 114( bc_0,           DDRODQSN(17),         output2,          X), " &
" 113( bc_0,           DDRODQSP(17),         output2,          X), " &
" 112( bc_10,          DDROCB(5),          output2,          X), "
&
" 111( bc_10,          DDROCB(4),          output2,          X), "
&
" 110( bc_10,          DDROCB(6),          output2,          X), "
&

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" 109( bc_10, DDR0CB(7), output2, X), "
&
" 108( bc_1, *, internal ,
X), " &
" 107( bc_10, DDR1CB(0), output2, X), "
&
" 106( bc_10, DDR1CB(1), output2, X), "
&
" 105( bc_10, DDR1CB(3), output2, X), "
&
" 104( bc_10, DDR1CB(2), output2, X), "
&
" 103( bc_0, DDR1DQSN(8), output2, X), " &
" 102( bc_0, DDR1DQSP(8), output2, X), " &
" 101( bc_0, DDR1DQSN(17), output2, X), " &
" 100( bc_0, DDR1DQSP(17), output2, X), " &
" 99( bc_10, DDR1CB(4), output2, X), "
&
" 98( bc_10, DDR1CB(5), output2, X), "
&
" 97( bc_10, DDR1CB(6), output2, X), "
&
" 96( bc_10, DDR1CB(7), output2, X), "
&
" 95( bc_1, *, internal ,
X), " &
" 94( bc_10, DDROA(12), output2, X), "
&
" 93( bc_10, DDROA(14), output2, X), "
&
" 92( bc_10, DDROA(15), output2, X), "
&
" 91( bc_10, DDROBA(2), output2, X), "
&
" 90( bc_10, DDROCKE(2), output2, X), "
&
" 89( bc_10, DDROCKE(1), output2, X), "
&
" 88( bc_10, DDROCKE(3), output2, X), "
&
" 87( bc_10, DDROCKE(0), output2, X), "
&
" 86( bc_1, *, internal ,
X), " &
" 85( bc_4, DDROERR_N(1), observe_onl y, X), " &
" 84( bc_4, DDROERR_N(0), observe_onl y, X), " &
" 83( bc_4, *, internal ,
X), " &
" 82( bc_10, DDRORESET_N, output2, X), " &
" 81( bc_10, DDR1A(12), output2, X), "
&
" 80( bc_10, DDR1BA(2), output2, X), "
&
" 79( bc_10, DDR1A(14), output2, X), "
&
" 78( bc_10, DDR1A(15), output2, X), "
&
" 77( bc_10, DDR1CKE(0), output2, X), "
&
" 76( bc_10, DDR1CKE(1), output2, X), "
&
" 75( bc_10, DDR1CKE(2), output2, X), "
&

```



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" 74( bc_10, DDR1CKE(3), output2, X), "
&
" 73( bc_1, *, internal ,
X), " &
" 72( bc_4, DDR1ERR_N(0), observe_onl y, X), " &
" 71( bc_4, DDR1ERR_N(1), observe_onl y, X), " &
" 70( bc_4, *, internal ,
X), " &
" 69( bc_10, DDR1RESET_N, output2, X), " &
" 68( bc_1, *, internal ,
X), " &
" 67( bc_10, DDROA(6), output2, X), "
&
" 66( bc_10, DDROA(11), output2, X), "
&
" 65( bc_10, DDROA(8), output2, X), "
&
" 64( bc_10, DDROA(7), output2, X), "
&
" 63( bc_10, DDROA(5), output2, X), "
&
" 62( bc_10, DDROWE_N, output2, X), "
&
" 61( bc_10, DDROA(9), output2, X), "
&
" 60( bc_10, DDROCAS_N, output2, X), "
&
" 59( bc_10, DDRORAS_N, output2, X), "
&
" 58( bc_1, *, internal ,
X), " &
" 57( bc_10, DDR1A(6), output2, X), "
&
" 56( bc_10, DDR1A(11), output2, X), "
&
" 55( bc_10, DDR1A(5), output2, X), "
&
" 54( bc_10, DDR1A(8), output2, X), "
&
" 53( bc_10, DDR1A(9), output2, X), "
&
" 52( bc_10, DDR1WE_N, output2, X), "
&
" 51( bc_10, DDR1CAS_N, output2, X), "
&
" 50( bc_10, DDR1A(7), output2, X), "
&
" 49( bc_10, DDR1RAS_N, output2, X), "
&
" 48( bc_1, *, internal ,
X), " &
" 47( bc_1, *, internal ,
X), " &
" 46( bc_4, *, internal ,
X), " &
" 45( bc_4, *, internal ,
X), " &
" 44( bc_1, FBDSBI P(0), i nput, X), "
&
" 43( bc_1, FBDSBI N(0), i nput, X), "
&
" 42( bc_1, FBDSBI P(1), i nput, X), "
&

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```

" 41( bc_1, FBDSBI N(1), i nput, X), "
&
" 40( bc_1, FBDSBI P(2), i nput, X), "
&
" 39( bc_1, FBDSBI N(2), i nput, X), "
&
" 38( bc_1, *, i nternal ,
X), " &
" 37( bc_1, *, i nternal ,
X), " &
" 36( bc_1, FBDSBI P(3), i nput, X), "
&
" 35( bc_1, FBDSBI N(3), i nput, X), "
&
" 34( bc_1, *, i nternal ,
X), " &
" 33( bc_1, *, i nternal ,
X), " &
" 32( bc_1, FBDSBI P(8), i nput, X), "
&
" 31( bc_1, FBDSBI N(8), i nput, X), "
&
" 30( bc_1, FBDSBI P(7), i nput, X), "
&
" 29( bc_1, FBDSBI N(7), i nput, X), "
&
" 28( bc_1, FBDSBI CLKP, i nput, X), "
&
" 27( bc_1, FBDSBI CLKN, i nput, X), "
&
" 26( bc_1, FBDSBI P(9), i nput, X), "
&
" 25( bc_1, FBDSBI N(9), i nput, X), "
&
" 24( bc_1, FBDSBI P(4), i nput, X), "
&
" 23( bc_1, FBDSBI N(4), i nput, X), "
&
" 22( bc_1, FBDSBI P(6), i nput, X), "
&
" 21( bc_1, FBDSBI N(6), i nput, X), "
&
" 20( bc_1, FBDSBI P(5), i nput, X), "
&
" 19( bc_1, FBDSBI N(5), i nput, X), "
&
" 18( bc_1, FBDSBI P(10), i nput, X), " &
" 17( bc_1, FBDSBI N(10), i nput, X), " &
" 16( bc_1, *, i nternal ,
X), " &
" 15( bc_1, *, i nternal ,
X), " &
" 14( bc_1, FBDNBOP(1), output2, X), "
&
" 13( bc_1, FBDNBOP(0), output2, X), "
&
" 12( bc_1, FBDNBOP(3), output2, X), "
&
" 11( bc_1, FBDNBOP(2), output2, X), "
&
" 10( bc_1, FBDNBOP(13), output2, X), " &
" 9( bc_1, FBDNBOP(12), output2, X), " &
" 8( bc_1, FBDNBOPCLKP, output2, X), "

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&
" 7( bc_1, FBDNBOP(7), output2, X), "
&
" 6( bc_1, FBDNBOP(6), output2, X), "
&
" 5( bc_1, FBDNBOP(8), output2, X), "
&
" 4( bc_1, FBDNBOP(4), output2, X), "
&
" 3( bc_1, FBDNBOP(10), output2, X), " &
" 2( bc_1, FBDNBOP(5), output2, X), "
&
" 1( bc_1, FBDNBOP(11), output2, X), " &
" 0( bc_1, FBDNBOP(9), output2, X)
",
end mb1_top;

```