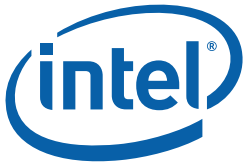


Mobile Intel® 915GM/PM/GME/GMS and 910GML/GMLE Express Chipset

Specification Update

April 2007

Document Number: 307167-012

NFORMATION IN THIS DOCUMENT IS PROVIDED IN CONNECTION WITH INTEL® PRODUCTS. NO LICENSE, EXPRESS OR IMPLIED, BY ESTOPPEL OR OTHERWISE, TO ANY INTELLECTUAL PROPERTY RIGHTS IS GRANTED BY THIS DOCUMENT. EXCEPT AS PROVIDED IN INTEL'S TERMS AND CONDITIONS OF SALE FOR SUCH PRODUCTS, INTEL ASSUMES NO LIABILITY WHATSOEVER, AND INTEL DISCLAIMS ANY EXPRESS OR IMPLIED WARRANTY, RELATING TO SALE AND/OR USE OF INTEL PRODUCTS INCLUDING LIABILITY OR WARRANTIES RELATING TO FITNESS FOR A PARTICULAR PURPOSE, MERCHANTABILITY, OR INFRINGEMENT OF ANY PATENT, COPYRIGHT OR OTHER INTELLECTUAL PROPERTY RIGHT. Intel products are not intended for use in medical, life saving, life sustaining, critical control or safety systems, or in nuclear facility applications.

Intel may make changes to specifications and product descriptions at any time, without notice. Designers must not rely on the absence or characteristics of any features or instructions marked "reserved" or "undefined." Intel reserves these for future definition and shall have no responsibility whatsoever for conflicts or incompatibilities arising from future changes to them. The information here is subject to change without notice. Do not finalize a design with this information.

The products described in this document may contain design defects or errors known as errata which may cause the product to deviate from published specifications. Current characterized errata are available on request.

Contact your local Intel sales office or your distributor to obtain the latest specifications and before placing your product order.

Copies of documents which have an order number and are referenced in this document, or other Intel literature, may be obtained by calling 1-800-548-4725, or by visiting Intel's Web Site.

This document contains information on products in the design phase of development.

Intel processor numbers are not a measure of performance. Processor numbers differentiate features within each processor family, not across different processor families. See http://www.intel.com/products/processor_number for details.

Code Names are only for use by Intel to identify products, platforms, programs, services, etc. ("products") in development by Intel that have not been made commercially available to the public, i.e., announced, launched or shipped. They are never to be used as "commercial" names for products. Also, they are not intended to function as trademarks.

BunnyPeople, Celeron, Celeron Inside, Centrino, Centrino logo, Core Inside, FlashFile, i960, InstantIP, Intel, Intel logo, Intel386, Intel486, Intel740, IntelDX2, IntelDX4, IntelSX2, Intel Core, Intel Inside, Intel Inside logo, Intel. Leap ahead., Intel. Leap ahead. logo, Intel NetBurst, Intel NetMerge, Intel NetStructure, Intel SingleDriver, Intel SpeedStep, Intel StrataFlash, Intel Viiv, Intel vPro, Intel XScale, Itanium, Itanium Inside, MCS, MMX, Oplus, OverDrive, PDCharm, Pentium, Pentium Inside, skoool, Sound Mark, The Journey Inside, VTune, Xeon, and Xeon Inside are trademarks of Intel Corporation in the U.S. and other countries.

*Other names and brands may be claimed as the property of others.

This device is protected by U.S. patent numbers 5,315,448 and 6,516,132, and other intellectual property rights. The use of Macrovision's copy protection technology in the device must be authorized by Macrovision and is intended for home and other limited pay-per-view uses only, unless otherwise authorized in writing by Macrovision. Devices incorporating Macrovision's copy protection technology can only be sold or distributed to companies appearing on Macrovision's list of "Authorized Buyers" at: www.macrovision.com. Reverse engineering or disassembly is prohibited.

Contents

Revision History

Revision	Description	Date
-001	Initial public release	March 2005
-002	• Added Errata 25 – 27 • Added Specification Changes 2 – 5 • Added Specification Clarification 1 • Added Documentation Change 5	May 2005
-003	• Added Erratum 28 • Added Erratum and Component Marking Information for C1 Stepping	June 2005
-004	• Added Erratum 29	July 2005
-005	• Added Erratum 30 • Updated Erratum 7 & 25 • Updated Specification Clarification 1	August 2005
-006	• Spec Clarification: DVMT 3.0 support configurations • Doc Change : LBKLT_CRTL signal description update	September 2005
-007	• Corrected S-Spec numbers for 915GMS & 910GML PB-free parts (S-Spec numbers were swapped)	September 2005
-008	• Added Erratum 31	October 2005
-009	• Updated Erratum 29 status • Added C-2 stepping information	November 2005
-010	• Added Erratum 32 • Doc Change : register bit definition changed for C0DRC0 • Doc Change : register bit definition changed for C0DRC1	January 2006
-011	• Added Erratum 33	October 2006
-012	• Added 915GME SKU to most references of 915GM • Added 910GMLE SKU to most references of 910GML	April 2007

§

Preface

This document is an update to the specifications contained in the documents listed in the following Affected Documents table. It is a compilation of device and document errata and specification clarifications and changes, and is intended for hardware system manufacturers and for software developers of applications, operating system, and tools.

Information types defined in the Nomenclature section of this document are consolidated into this update document and are no longer published in other documents. This document may also contain information that has not been previously published.

Affected Documents

Document Title	Document Location / Number
Mobile Intel® 915 and 910 Express Chipset Family of Products Datasheet	305264

Nomenclature

Errata are design defects or errors. Errata may cause the behavior of the Intel® 915GM/PM/GMS/GME and 910GML/GMLE Express Chipset GMCH to deviate from published specifications. Hardware and software designed to be used with any given stepping must assume that all errata documented for that stepping are present on all devices.

Specification Changes are modifications to the current published specifications. These changes will be incorporated in the next release of the specifications.

Specification Clarifications describe a specification in greater detail or further highlight a specification's impact to a complex design situation. These clarifications will be incorporated in the next release of the specifications.

Documentation Changes include typos, errors, or omissions from the current published specifications. These changes will be incorporated in the next release of the specifications.

Note: Errata remain in the specification update throughout the product's lifecycle, or until a particular stepping is no longer commercially available. Under these circumstances, errata removed from the specification update are archived and available upon request. Specification changes, specification clarifications and documentation changes are removed from the specification update when the appropriate changes are made to the appropriate product specification or user documentation (datasheets, manuals, etc.).

§

Summary Tables of Changes

The following table indicates the Errata, Specification Changes, Specification Clarifications or Documentation Changes which apply to the listed Intel 915GM/PM/GMS/GME and 910GML/GMLE Express Chipset GMCH steppings. Intel intends to fix some of the errata in a future stepping of the component and to account for the other outstanding issues through documentation or Specification Changes as noted.

Note: B1 and C1 stepping parts will not be produced for the 915GME and the 910GMLE products.

This table uses the following notations:

Codes Used in Summary Table

Stepping

X:	Erratum, Specification Change or Clarification that applies to this stepping.
(No mark) or (Blank Box):	This erratum is fixed in listed stepping or specification change does not apply to listed stepping.

Status

Doc:	Document change or update that will be implemented.
Plan Fix:	This erratum may be fixed in a future stepping of the product.
Fixed:	This erratum has been previously fixed.
No Fix:	There are no plans to fix this erratum.

Row

Shaded:	This item is either new or modified from the previous version of the document.

No	Steppings												Plans	ERRATA
	915PM			915GM/GME			915GMS			910GML/GMLE				
	C0	C1	C2	B1	C1	C2	C0	C1	C2	B1	C1	C2		
1	X	X	X	X	X	X							No Fix	Reported L0s Exit Latency Is Not Updated When PCI Express* Is Not Operating in Common Clock Mode
2	X	X	X	X	X	X							No Fix	GMCH Will Not Identify Back to Back Malformed Packets
3	X	X	X	X	X	X							No Fix	The GMCH Is Limited to Reporting Poisoned TLPs through Standard PCI Error Status Reporting Structures
4	X	X	X	X	X	X							No Fix	Incorrect PCI Express Lane Transition after Receiving Several TS1 Packets
5	X	X	X	X	X	X	X	X	X	X	X		No Fix	DMI Link Egress Port Address Is Not Programmable
6	X	X	X	X	X	X	X	X	X	X	X		No Fix	DDR2 OCD Nonfunctional
7	X	X	X	X	X	X							No Fix	PCI Express Graphics Initiated Snooped Reads to Memory That Are Fast Dispatched Could Result in Incorrect Data Being Returned
8	X	X	X	X	X	X							No Fix	PCI Express Common Mode Voltage Noise Immediately Following Receiver Detect sequence
9	X	X	X	X	X	X							No Fix	GMCH Does Not Ignore a PCI Express Null Packet

No	Steppings												Plans	ERRATA
	915PM			915GM/GME			915GMS			910GML/GMLE				
	C0	C1	C2	B1	C1	C2	C0	C1	C2	B1	C1	C2		
10	X	X	X	X	X	X							No Fix	Data Payload Byte Count Supplied during an unsupported Upstream Configuration Read Is Not 4 Bytes
11	X	X	X	X	X	X							No Fix	PCI Express Replay Timer Register Default Setting Is Incorrect
12	X	X	X	X	X	X	X	X	X	X	X	X	No Fix	E_SMERR Bit Set Incorrectly
13				X									Fixed	PCI Express Lane 3 Bit Errors Occur on a Small Percentage of GMCH B-1 Units on certain Boards. PCI Express x16 Interface Only Supported on C0 or Later Stepping
14				X	X	X	X	X	X	X	X	X	No Fix	Pixel Discoloration Seen When Intel® Dual Frequency Graphics Technology (Intel® DFGT) Is Enabled
15	X			X			X			X			Fixed	System Hang with DDR-333 Memory When Intel® Rapid Memory Power Management Is Enabled during C2/C3/C4
16				X			X						Fixed	Display becomes a solid Color with Intel® S2DDT Enabled (Only supported on 915GM, 915GMS & 915GME)
17	X	X	X	X	X	X							No Fix	PCI Express Scrambling

No	Steppings												Plans	ERRATA
	915PM			915GM/GME			915GMS			910GML/GMLE				
	C0	C1	C2	B1	C1	C2	C0	C1	C2	B1	C1	C2		
18				X			X			X			Fixed	Macrovision Failure for 480p / 576p Modes
19	X	X	X	X	X	X	X	X	X	X	X	X	No Fix	Thermometer Read Register is Non-Functional with Negative Calibration Offset
20	X	X	X	X	X	X	X	X	X	X	X	X	No Fix	Potential Electrical Spec Violation If a SO-DIMM Is Only Populated in Channel B
21				X	X	X	X	X	X	X	X	X	No Fix	LVDS Panel Power Down Timing Violation during System Reset
22	X	X	X	X	X	X							No Fix	PCI Express SKP/InitFCx Contention
23	X			X			X			X			Fixed	SMVREF High Current Draw
24				X	X	X	X	X	X	X	X	X	No Fix	Mobile Intel 915GM/GMS/GME and 910GML/GMLE Express Chipset Graphics Clock Crossing Issue
25	X	X	X	X	X	X	X	X	X	X	X	X	NoFix	Mobile Intel 915GM/PM/GMS/GME and 910GML/GMLE Express Chipset Memory Refresh Queue
26	X	X	X	X	X	X							NoFix	Packet Dropped When Replay Timer Expires and Replay Is in Progress
27	X	X	X	X	X	X	X	X	X	X	X	X	NoFix	LOCK to non-DRAM Memory Flag (Register Dev 0, Fun 0, Offset C8, Bit 9) Is Getting Asserted

No	Steppings												Plans	ERRATA
	915PM			915GM/GME			915GMS			910GML/GMLE				
	C0	C1	C2	B1	C1	C2	C0	C1	C2	B1	C1	C2		
28				X	X	X	X	X	X	X	X	X	NoFix	Mobile Intel 915GM/GMS/GME and 910GML/GMLE Express Chipset LVDS — CRT Switching
29				X	X*		X	X*		X	X*		Fixed	Mobile Intel 915GM/GMS/GME and 910GML/GMLE Express Chipset LVDS Vos *C1 units with FPO date code of WW49 or later are not affected by the erratum.
30	X	X	X	X	X	X							NoFix	Mobile Intel 915PM/GM/GME Express Chipset x1 False Detect
31	X	X	X	X	X	X							NoFix	Mobile Intel 915PM/GM/GME Express Chipset PCI Express Ztx_diff_dc Impedance Violation
32	X	X	X	X	X	X	X	X	X	X	X	X	No Fix	Mobile Intel 915PM/GM/GMS/GME and 910GML/GMLE Express Chipset DRAM Clock to CKE Power-up Timing
33	X	X	X	X	X	X	X	X	X	X	X	X	No Fix	Mobile Intel 915PM/GM/GMS/GME and 910GML/GMLE Express Chipset SMRAM D_CLS Bit

NOTE: B1 and C1 stepping parts will not be produced for the 915GME and the 910GMLE products.

Number	SPECIFICATION CHANGES
1	Graphics Render and Display Clock Frequency Combination Support
2	Intel 915GM Express Chipset Host/Memory/Graphics Clock Support Update
3	Intel 915GM Express Chipset Host/Memory/Graphics Clock Support Table 11-1 Update

Number	SPECIFICATION CHANGES
4	Mobile Intel 915GM/GMS/GME and 910GML/GMLE Express Chipset Display and Render Clock Support Updates
5	Mobile Intel 910GML/GMLE Express Chipset Memory Channel Organization Support Update

Number	SPECIFICATION CLARIFICATIONS
1	Slow Transfers for LPC Devices
2	DVMT 3.0 Support Configurations

Number	DOCUMENTATION CHANGES
1	DRAM Enhanced Addressing Update
2	Section 5.2.15 C0DRC1 – Channel 0 DRAM Controller Mode 1
3	Section 5.2.31 DCC – DRAM Channel Control
4	Section 2.2.33 GCFGC – Graphics Clock Frequency and Gating Control
5	Section 5.2.12 C0DRT1 – Channel 0 DRAM Timing Register 1
6	Section 2.5.3 – LBKLT_CRTL Signal Description Update
7	Section 17.2.14 C0DRC0 – Channel 0 DRAM Controller Mode 0
8	Section 17.2.15 C0DRC1 – Channel 0 DRAM Controller Mode 1

§

Identification Information

Component Identification via Programming Interface

The Intel 915PM/GM/GMS/GME and 910GML/GMLE Express Chipset family may be identified by the following register contents:

Stepping	Vendor ID[1]	Device ID[2]	Revision Number[3]
B1	8086h	2590h	03
C0	8086h	2590h	03
C1 and C2	8086h	2590h	04

NOTES:

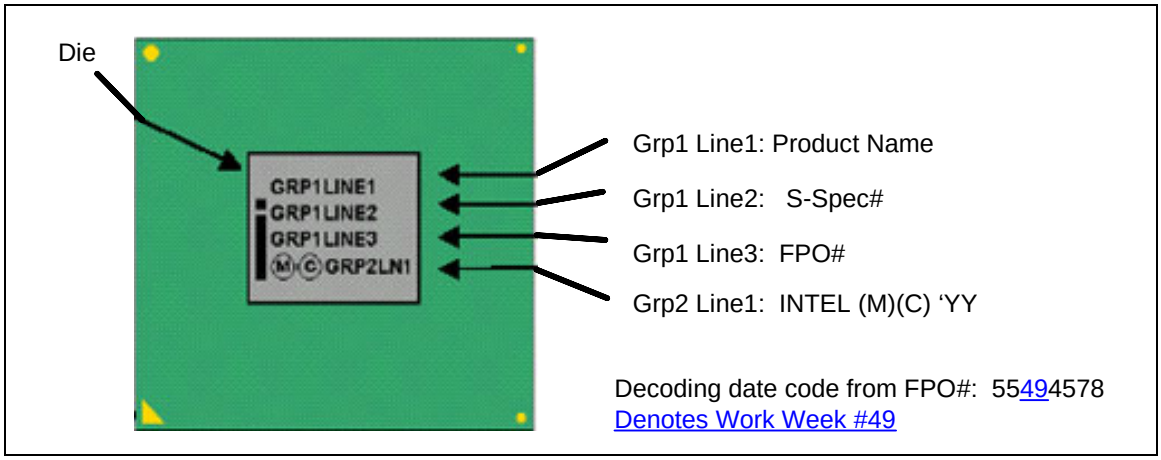
1. The Vendor ID corresponds to bits 15:0 of the Vendor ID Register located at offset 00–01h in the PCI function 0 configuration spaces.
2. The Device ID corresponds to bits 15:0 of the Device ID Register located at offset 02–03h in the PCI function 0 configuration spaces.
3. The Revision Number corresponds to bits 7:0 of the Revision ID Register located at offset 08h in the PCI function 0 configuration spaces.

Component Marking Information

The Intel 915PM/GM/GMS/GME and 910GML/GMLE Express Chipset family may be identified by the following component markings:

Product	MM# or S-Spec#	Stepping	Notes
Mobile Intel 915GM Express Chipset	865926	B1	
Mobile Intel 915GM Express Chipset	865971	B1	Pb-free
Mobile Intel 910GML Express Chipset	865930	B1	
Mobile Intel 910GML Express Chipset	865923	B1	Pb-free
Mobile Intel 915PM Express Chipset	867706	C0	
Mobile Intel 915PM Express Chipset	867713	C0	Pb-free
Mobile Intel 915GMS Express Chipset	867708	C0	
Mobile Intel 915GMS Express Chipset	867712	C0	Pb-free
Mobile Intel 915GM Express Chipset	SL8G2	C1 and C2	
Mobile Intel 915GM Express Chipset	SL8G6	C1 and C2	Pb-free
Mobile Intel 915GME Express Chipset	SLA9K	C1 and C2	Pb-free
Mobile Intel 915PM Express Chipset	SL8G3	C1 and C2	
Mobile Intel 915PM Express Chipset	SL8G7	C1 and C2	Pb-free
Mobile Intel 915GMS Express Chipset	SL8G4	C1 and C2	
Mobile Intel 915GMS Express Chipset	SL8G9	C1 and C2	Pb-free
Mobile Intel 910GML Express Chipset	SL8G5	C1 and C2	
Mobile Intel 910GML Express Chipset	SL8G8	C1 and C2	Pb-free
Mobile Intel 910GMLE Express Chipset	SLA9L	C1 and C2	Pb-free

Figure 1. Mobile 915PM/GM/GMS/GME & 910GML/GMLE Express Chipset Package Markings



§

Errata

1. Reported L0s Exit Latency Is Not Updated When PCI Express* Is Not Operating in Common Clock Mode

Problem: When PCI Express is operating with separate reference clocks, L0s exit latency may be greater than the setting in the L0s Exit Latency register.

Implication: If the PCI Express link is operating in non-common clock mode, the actual L0s exit latency may be longer than advertised. In this situation the link will likely enter the Recovery state before transitioning into the normal L0 state.

Workaround: System BIOS can program the appropriate Exit Latency and advertised N_FTS value if it detects that the downstream device is not using the common reference clock (indicated in the Slot Clock Configuration bit 12 of the device's Link Status register).

Status: For the steppings affected, see the *Summary Tables of Changes*.

2. GMCH Will Not Identify Back-to-Back Malformed Packets

Problem: If the GMCH receives two back-to-back malformed packets, the second malformed packet is not trapped or logged.

Implication: The GMCH will not log or identify the second malformed packet. However, the 1st malformed TLP is logged, and is considered a Fatal Error. Link behavior is not guaranteed at that point whether a 2nd malformed TLP is detected or not.

Workaround: None

Status: For the steppings affected, see the *Summary Tables of Changes*.

3. The GMCH Is Limited to Reporting Poisoned TLPs through Standard PCI Error Status Reporting Structures

Problem: The GMCH does not set the Non-Fatal Error Detected status bit, in the PCI Express Device Status register when a poisoned TLP is received.

Implication: Future OS's (that comprehend PCI Express error reporting) will not be notified via standard PCI Express mechanisms when a poisoned TLP is received.

Workaround: Standard PCI error status reporting must be used for Poisoned TLP reporting. The reception of Poisoned TLP is reported by hardware setting the Detected Parity Error bit in Device 1, secondary status register, and if so enabled by additionally setting the Master Data Parity Error bit in the same register.

Status: For the steppings affected, see the *Summary Tables of Changes*.

4. Incorrect PCI Express Lane Transition after Receiving Several TS1 Packets

Problem: If the GMCH receives several TS1 packets with Link and Lane numbers set to PAD, after 4 µs it will time out and transition into configuration state instead of going directly to the Detect state as it should. However, the link will still transition to the Detect state after timing out of Configuration.

Implication: The GMCH will experience longer latency when transitioning to Detect state.

Workaround: None

Status: For the steppings affected, see the *Summary Tables of Changes*.

5. DMI Link Egress Port Address Is Not Programmable

Problem: The PCI SIG approved ECR 04 to allow future system software (e.g., operating system) to discover the link structure of the Root Complex. One of the registers in the GMCH that “points” from the DMI port to the ICH cannot be programmed correctly.

Implication: There is no impact on platform functionality. ECR’s do not retroactively apply to the current *PCI Express* 1.0a Specification* and no existing software understands the Root Topology discovery structures. These structures are implemented in the GMCH only to aid future software development. Such software will need to comprehend the incorrect pointer

Workaround: None

Status: For the steppings affected, see the *Summary Tables of Changes*.

6. DDR2 OCD Nonfunctional

Problem: During BIOS initialization the GMCH will not be able to adjust and set the DDR2-DRAM Device DQ/DQS/DQS# buffer impedance.

Implication: Adjustable DQ/DQS/DQS# buffer impedance settings will not be programmed into the DDR2-DRAM Devices, and the DRAM device OCD default output characteristics will be used instead.

Workaround: None

Status: For the steppings affected, see the *Summary Tables of Changes.*

7. PCI Express* Graphics Initiated Snooped Reads to Memory That Are Fast Dispatched Could Result in Incorrect Data Being Returned

Problem: This has only occurred at 1.05-V Core and 533-MHz FSB. GMCH could provide incorrect data for a PCI Express Graphics initiated memory read.

Implication: Could cause a data miscompare or system hang.

Workaround: It is possible for system BIOS to contain a workaround. Contact your Intel field representative for more details.

Status: For the steppings affected, see the *Summary Tables of Changes.*

8. PCI Express Common Mode Voltage Noise Immediately following Receiver Detect Sequence

Problem: The PCI Express Common Mode Voltage is not stable immediately after Receiver Detect Sequence when entering Polling.Active from Detect.Active states.

Implication: Common Mode Voltage noise may result in bit errors early in Polling.Active state. May result in additional training time before transitioning on to Polling.Configuration. Performance impact expected to be minimal.

Workaround: None

Status: For the steppings affected, see the *Summary Tables of Changes.*

9. GMCH Does Not Ignore a PCI Express Null Packet

Problem: If the GMCH receives a PCI Express Null packet, it should drop the packet and not perform sequence number checking or respond with any Ack or Nak DLLP. The issue is that the GMCH still performs sequence number checks for Null packets and may respond with an ACK or NAK depending on the result of the check.

Implication: GMCH may send ACK or NAK DLLPs in response to a Null packet if the sequence number is not as expected. This may cause unnecessary retries, but Null packets are expected to be rare on the link.

Workaround: None

Status: For the steppings affected, see the *Summary Tables of Changes.*

10. Data Payload Byte Count Supplied during an Unsupported Upstream Configuration Read Is Not 4 Bytes

Problem: During configuration reads to unsupported PCI Express configuration space, the byte count for data payload is not 4.

Implication: Data payload byte count is 5 and not the expected 4.

Workaround: Do not perform unsupported upstream PCI Express configuration cycles.

Status: For the steppings affected, see the *Summary Tables of Changes.*

11. PCI Express Replay Timer Register Default Setting Is Incorrect

Problem: The default Replay timer value is too aggressive and does not properly account for L0s exit latency or internal pipeline delays. As a result the GMCH may initiate a replay sooner than expected.

Implication: The GMCH may initiate a replay sooner than expected. This should not happen as long as the downstream device complies with the PCI Express Ack Latency requirement.

Workaround: It is possible for BIOS to contain a workaround. Contact your Intel Field Representative for more details.

Status: For the steppings affected, see the *Summary Tables of Changes.*

12. E_SMERR Bit Set Incorrectly

Problem: The E_SMERR bit may be incorrectly set when performing valid accesses to SMM space.

Implication: If this bit is used by the SMI handler to determine cache line flushes, unnecessary cache line flushes may occur when in SMM mode**.** A slight performance impact to the SMI handler may result from unnecessary cache line flushes.

Workaround: None

Status: For the steppings affected, see the *Summary Tables of Changes.*

13. PCI Express* Lane 3 Bit Errors Occur on a Small Percentage of GMCH B-1 Units on Certain Boards

Problem: On systems with External Graphics, a small percentage of GMCH B-1 units may experience bit-errors on PCI Express lane 3 on certain boards. To date, we have only seen these bit errors on internal test (SV) boards at nominal core voltage (1.05 V).

Implication: A significant level of bit errors could lead to link retraining, link down, or hang conditions. Intel is currently trying to understand the variables that affect the bit error rate. All samples shipped outside of Intel have been screened for this issue and Intel has not seen any system hangs with screened parts. *PCI Express x16 Graphics not supported on Mobile Intel 915GM/GME B1 stepping.*

Workaround: None

Status: For the steppings affected, see the *Summary Tables of Changes*.

14. Pixel Discoloration Seen When Intel® Dual Frequency Graphics Technology (DFGT) Is Enabled

Problem: Pixel discoloration seen when Intel Dual Frequency Graphics Technology (Intel DFGT) is enabled. Root caused to the internal render clocks getting misaligned during the frequency switching.

Implication: Pixel discoloration seen on display.

Workaround: Disable the DFGT feature through VBT.

Status: For the steppings affected, see the *Summary Tables of Changes*.

15. System Hang with DDR-333 Memory When Intel® Rapid Memory Power Management Is Enabled during C2/C3/C4

Problem: DDR333 systems may not exit self refresh state when memory self refresh is enabled during C2/C3/C4.

Implication: System may hang.

Workaround: None.

Status: For the steppings affected, see the *Summary Tables of Changes.*

16. Display becomes a Solid Color with Intel® Smart 2D Display Technology (Intel® S2DDT) Enabled

Problem: If Memory Self-Refresh during C3 (C3SR) occurs when the Intel Smart 2D Display Technology (Intel S2DDT) recompresses at the start of a frame, the graphics engine may use the uncompressed frame instead of the recompressed frame. The issue may occurs if the system is left idle (>20 minutes) with Intel S2DDT.

Implication: Display becomes a solid color or may cause a system hang.

Workaround: None

Status: For the steppings affected, see the *Summary Tables of Changes.*

17. PCI Express Scrambling

Problem: While entering the Recovery state, 915PM/GM/GME PCI Express discrete graphics port stops scrambling two symbols before the first TS (training sequence).

Implication: When these non-scrambled symbols are received by the endpoint, the de-scrambler of the endpoint will observe two symbols of random data. The first symbol of TS1 will reset the endpoint's de-scrambler so that the endpoint should recognize the TS1 and TS2 ordered-sets being transmitted and move into the Recovery state as planned. There is no system level impact if the endpoint is PCI Express Specification 1.0a compliant in ignoring the random data.

Workaround: None

Problem: For the steppings affected, see the *Summary Tables of Changes.*

18. Macrovision Failure for 480p / 576p Modes

Problem: GMCH does not encode Macrovision (content protection) properly for 480p and 578p progressive modes and does not meet the Macrovision specification for these modes. 480p and 576p progressive modes will not pass MacroVision certification.

Implication: No DVD playback supported/available for these modes, other progressive scan modes are not affected.

Workaround: None

Status: For the steppings affected, see the *Summary Tables of Changes.*

19. Thermometer Read Register is Non-Functional with Negative Calibration Offset

Problem: When initializing the Thermometer counter, a negative offset will cause an overflow condition, causing the counter to stop. The GMCH will not update the Thermometer Read Register (TRR) register with the correct temperature trending values and the TRR will display “FF”. All other thermal sensor features will still work (throttling, trip points and interrupts) since these do not use the thermometer mode.

Implication: Thermometer Read Register (TRR) is not functional with negative Thermal Calibration Offset value (TCO).

Workaround: Please contact your Intel representative for the latest information.

Status: For the steppings affected, see the *Summary Tables of Changes.*

20. Potential Electrical Spec Violation if an SO-DIMM Is Only Populated in Channel B

Problem: When DDR or DDR2 memory devices are present on channel B, but not channel A, memory control logic only looks at channel A and incorrectly performs Rcomp value update. This could cause an electrical spec violation internal to the chip.

Implication: System with 915PM/GM/GME, or 910GML/GMLE may hang or experience other anomalous system behavior. No impact on system with 915GMS.

Workaround: It is possible for BIOS to contain a workaround. Contact your Intel Field Representative for more details.

Status: For the steppings affected, see the *Summary Tables of Changes.*

21. LVDS Panel Power Down Timing Violation during System Reset

Problem: During system reset, there is insufficient time for handshake between ICH and GMCH LVDS logic. As a result, timing from panel backlight enable going low to LVDS data going low (TX) and timing from LVDS data going low to panel VCC enable going low (T3) do not match the programmed values. Panel backlight enable (LBKLT_EN), panel Vcc enable (LVDD_EN) and LVDS data lines go low at the same time.

Implication: No system level issues have been observed.

Workaround: None

Status: For the steppings affected, see the *Summary Tables of Changes*.

22. PCI Express SKP / InitFCx Contention

Problem: During GMCH PCI Express initialization, if a SKP is being transmitted immediately before an InitFCx DLLP, then a partial InitFCx may be transmitted.

Implication: A slight delay (less than 100 ns) may occur during link initialization. Device may report correctable error. InitFCx will automatically be repeated.

Workaround: None

Status: For the steppings affected, see the *Summary Tables of Changes*

23. SMVREF High Current Draw

Problem: When SMOCDCOMP[1:0] are connected to ground (either directly or through a pull-down resistor), SMVREF[1:0] may draw significantly more current than specified. If the corresponding voltage supply is not capable of handling the resulting current, the SMVREF[1:0] voltage will droop below specification.

Implication: If SMVREF[1:0] droops below specification, the system may hang. Failure observed during S3 only.

Workaround: Leave SMOCDCOMP[1:0] as NC (No Connect) for both DDR and DDR2 designs. This limits the maximum current draw on SMVREF[1:0] to 200 µA (i.e. 100uA/pin). In addition, use a voltage supply that can supply at least 200 µA (total) for SMVREF[1:0].

Status: For the steppings affected, see the *Summary Tables of Changes.*

24. Mobile Intel 915GM / GMS / GME and 910GML / GMLE Express Chipset Graphics Clock Crossing Issue

Problem: While attempting to launch or exit an application that uses the overlay engine (e.g. media playback software running a video clip), the system may hang (blue screen) or screen resolution may change to VGA mode. This event may occur when a signal pulse is missed inside the chip due to synchronization of the graphics render and display clocks while graphics overlay mode is being turned off.

Implication: Failure is difficult to reproduce because this event only occurs under a very rare but valid timing condition where graphics render and display clocks are aligned while the graphics overlay is being turned off. System will hang or screen resolution may change to VGA mode when launching or exiting an application that uses the overlay engine. Mobile Intel 915GM/GMS/GME and 910GML/GMLE platforms that use render clock at 166 MHz are not affected by this sighting.

Workaround: It is possible for BIOS to contain a workaround. Contact your Intel Field Representative for more details.

Status: For the steppings affected, see the *Summary Tables of Changes.*

25. Mobile Intel 915PM/GM/GMS/GME and 910GML/GMLE Express Chipset Memory Refresh Queue

Problem: When thermal based throttling is enabled, memory refresh commands get queued up inside MCH/GMCH. As a result, MCH/GMCH may not perform memory refresh commands at a frequency needed by memory devices. Thermal based throttling happens only when either using the on-die memory thermal sensors or the external thermal sensor.

Implication: When not enough refresh commands are issued to system memory to retain memory content, data loss may occur. System is more susceptible to this issue when memory devices approach temperature limit.

Workaround: It is possible for system BIOS to contain a workaround. Contact your Intel field representative for more details.

Status: For affected steppings, see the *Summary Tables of Changes*.

26. Packet Dropped When Replay Timer Expires and Replay Is in Progress

Problem: When a packet replay is in progress on the PCI Express Port, and if some but not all of the packets to be replayed are acknowledged and the replay timer expires on the same clock cycle as the replay start of the first unacknowledged packet, the next packet in the replay buffer may be sent with an old sequence number. That packet is seen by receiver side as a duplicate and subsequently dropped.

Note: This has only been reproduced in a synthetic test environment.

Implication: Anomalous behavior may result if all of the above conditions are met.

Workaround: None

Status: For the steppings affected, see the *Summary Tables of Changes*.

27. LOCK to non-DRAM Memory Flag (Register Dev 0, Fun 0, Offset C8, Bit 9) Is Getting Asserted

Problem: A CPU lock cycle request is unintentionally being recognized as request to a non-system memory destination.

Implication: The GMCH may incorrectly flag an error for a valid lock cycle that targets DRAM. A System Error (SERR) may be generated if enabled by System BIOS.

Note: The default setting for ERRCMD[9] Bus 0 Device 0 Offset CAh is to disable this reporting.

Workaround: Do not enable or change default setting of ERRCMD[9] Bus 0 Device 0 Offset CAh (SERR reporting for Lock cycles to non-DRAM Memory)

Status: For the steppings affected, see the *Summary Tables of Changes*.

28. Mobile Intel 915GM/GMS/GME and 910GML/GMLE Express Chipset LVDS – CRT Switching

Problem: 915GM/GMS/GME and 910GML/GMLE LVDS interface may hang while switching between LVDS and CRT outputs.

Implication: Once LVDS interface hangs a system reset is required.

Workaround: Fixed in VBIOS, Please refer to release notes for VBIOS version 1220 or Newer.

Status: For the steppings affected, see the *Summary Tables of Changes*.

29. Mobile Intel 915GM/GMS/GME and 910GML/GMLE Express Chipset LVDS Vos

Problem: On some Mobile Intel 915GM/GMS/GME and 910GML/GMLE Express devices, one or more LVDS lanes may exceed Intel's Vos specification limits.

LVDS Interface: Functional Operating Range (VCC= 2.5V ±5%)

Symbol	Parameter	Min	Nom	Max	Unit
$V_{OS(Tested)}$	Offset Voltage	0.700	1.25	1.600	V
$V_{OS\ (Spec)}$	Offset Voltage	1.125	1.25	1.375	V

NOTES: Table reflects Intel tested Vos specification limits and the Mobile Intel 915GM/GMS/GME & 910GML/GMLE specification for Vos values. Intel may make changes to specifications, release dates and product descriptions from time to time.

Implication: LVDS Panels sensitive to Vos range may not detect transmitted LVDS data. Potential visual anomalies on LVDS display panels may occur, although no visual anomalies have been reported due to Vos levels in the above tested range.

Workaround: None

Status: For the steppings affected, see the *Summary Tables of Changes*.

30. Mobile Intel 915PM/GM/GME Express Chipset x1 False Detect

Problem: 915PM/GM/GME may falsely detect the presence of a PCIe endpoint while operating in PCIe Low Power Mode.

- False detect may occur for 915PM/GM/GME systems supporting x1 only endpoints.
- False detect may occur on PCIe* lanes 1 through 15 for a graphics endpoint when switching from x16 to x1.

Implication: Systems may become inoperable when an endpoint is operating in x1 mode.

- The scenario occurs because false detection of a PCIe endpoint occurs on one or more lanes resulting in the GMCH's PCIe interface erroneously entering and looping continuously in Polling.Compliance.
- When an endpoint is operating in x1 mode, the scenario may occur at boot or during any subsequent attempt to retrain the link.

Workaround: For systems requiring x1 PCIe link operation:

- Systems operating in x1 mode only: It is possible for system BIOS to contain a workaround. Contact your Intel field representative for more details.
- Systems requiring run-time switching between x16 and x1 operation: A graphics driver workaround has been defined. Please contact your graphic's controller vendor for driver status.
- Use the erratum title when contacting graphic's controller vendor for driver status.
- For questions pertaining to the erratum or workaround please contact your Intel representative.

Status: For the steppings affected, see the *Summary Tables of Changes*.

31. Mobile Intel 915PM/GM/GME Express Chipset PCI Express Ztx_diff_dc Impedance Violation

Problem: 915PM/GM violates the PCI Express Ztx_diff_dc max impedance specification.

Implication: None

- No failures have been observed due to the violation of the PCI Express Ztx_diff_dc impedance specification.
- PCI Express Tx_eye signal integrity specifications are still met.

Workaround: None

Status: For affected steppings, see the *Summary Tables of Changes*.

32. Mobile Intel 915PM/GM/GMS/GME and 910GML/GMLE Express Chipset DRAM Clock to CKE Power-up Timing

Problem: During memory power-up and initialization, the timing between DRAM clock stabilization to CKE going high is observed to be minimum of 35 ns against the JEDEC spec of 200 µs.

Implication: None. No functional failures have been observed.

- Intel has characterized the timing and shared the data with major DRAM suppliers. Intel has determined and major DRAM suppliers agree that DRAM devices need < 35 ns. This erratum should not cause memory-clock functionality or timing related issues. Please refer to latest Intel DRAM spec Addendum for power-up and initialization timing requirements available at http://developer.intel.com/technology/memory/#Specs

Workaround: None.

Status: For affected steppings, see the *Summary Tables of Changes*.

33. Mobile Intel 915PM/GM/GMS/GME and 910GML/GMLE Express Chipset SMRAM D_CLS Bit

Problem: Data and stack which residing in Extended SMRAM (TSEG/HSEG) is inaccessible if D_CLS bit (Bus 0, Device 0, Function 0, Register 9Dh, Bit 5) is set.

Implication: May result in system hang.

Workaround: It is possible for system BIOS to contain a workaround. Contact your Intel field representative for more details.

Status: No Fix. For steppings affected, see the *Summary Tables of Changes.*

§

Specification Changes

1. Graphics Core Clock Frequency Update

The following section replaces the *Mobile Intel® 915 and 910 Express Chipset Family of Products Datasheet*, Section 10.14.3.

10.14.3.1 Intel 915GM/GME Express Chipset Host/Memory/Graphics Clock Support

Table 10-16a. Intel 915GM/GME Express Chipset Graphics Clock Frequency Support at 1.05 V

Host	Memory	2D Display clock	3D Render Clock
400 MHz	DDR 333	200	166
400 MHz	DDR 333	213	200
533 MHz	DDR 333	190	166
533 MHz	DDR 333	213	190
400 MHz / 533 MHz	DDR2 400 / DDR2 533	200	160
400 MHz / 533 MHz	DDR2 400 / DDR2 533	213	200

NOTE: Mobile Intel 915GM/ 915GME / 910GML / 910GMLE Express Chipset will remove support for 133 MHz for both graphics render and display clock due to graphics clock crossing issue (Errata #24).

Table 10-16b. Intel 915GM/GME Express Chipset Graphics Clock Frequency Support at 1.5 V

Host	Memory	2D Display clock	3D Render Clock
400 MHz / 533 MHz	DDR2 400 / DDR2 533	200	160
400 MHz / 533 MHz	DDR2 400 / DDR2 533	213	200
400 MHz / 533 MHz	DDR2 400 / DDR2 533	333	333

NOTE: Mobile Intel 915GM/GME/ 910GML/GMLE does not support DDR333 if chipset core voltage is designed for 1.5 V.

10.14.3.2 Intel 915GMS Express Chipset Host/Memory/Graphics Clock Support

Table 10-17. Intel 915GMS Express Chipset Graphics Clock Frequency Support at 1.05 V

Host	Memory	2D Display Clock	3D Render Clock
400 MHz	DDR2 400	152	133
400 MHz	DDR2 400	200	160

10.14.3.3 Intel 910GML/GMLE Express Chipset Host/Memory/Graphics Clock Support

Table 10-18. Intel 910GML/GMLE Express Chipset Graphics Clock Frequency Support at 1.05 V

Host	Memory	2D Display Clock	3D Render Clock
400 MHz	DDR 333	200	166
400 MHz	DDR2 400	200	160

2. Intel 915GM/GME Express Chipset Host/Memory/Graphics Clock Support Update

Table 10-16 and Table 10-7 incorrectly state support for Display clocks for 400 MHz / DDR333 and 533 MHz/DDR333 frequency combinations. These combinations will result with a Display clock of 222 MHz. See Specification Change Item #1 above and Documentation Change #4 for updated information in grey shaded text.

3. Mobile Intel 915GM/GMS/GME and 910GML/GMLE Express Chipset Display and Render Clock Support Update

The following section replaces the *Mobile Intel® 915 and 910 Express Chipset Family of Products Datasheet*, *Graphics Clock Frequency Feature* section, on page 22.

— 2D Display core frequency at 190/200 or 213/222 MHz @ Vcc=1.05 V depending on the host/memory configurations
— 3D Render core frequency at 160/166 or 190/200 MHz @ Vcc=1.05 V depending on the host/memory configurations
— 2D Display core frequency at 200, 213 or 333 MHz @ Vcc=1.5 V depending on the host/memory configurations
— 3D Render core frequency at 166, 200 or 333 MHz @ Vcc=1.5 V depending on the host/memory configurations

The following section replaces the *Mobile Intel® 915 and 910 Express Chipset Family of Products Datasheet*, *Graphics Clock Frequency Feature* section, on page 25.

— 2D Display core frequency at 152 or 200 MHz @ Vcc=1.05 V depending on the host/memory configurations
— 3D Render core frequency at 133 or 160 MHz @ Vcc=1.05 V depending on the host/memory configurations

The following section replaces the *Mobile Intel® 915 and 910 Express Chipset Family of Products Datasheet*, *Graphics Clock Frequency Feature* section, on page 26.

— 2D Display core frequency at 200 MHz @ Vcc=1.05 V depending on the host/memory configurations
— 3D Render core frequency at 160/166 MHz @ Vcc=1.05 V depending on the host/memory configurations

4. Mobile Intel 910GML/GMLE Express Chipset Memory Channel Organization Support Update

The following section replaces the *Mobile Intel® 915 and 910 Express Chipset Family of Products Datasheet* in the *Mobile Intel 910GML Express Chipset Feature* section, on page 26 and in Section 10.2.

— Memory channel organization support for DDR is:
  — Single Channel Mode
— Memory channel organization support for DDR2 is:
  — Dual Channel Asymmetric Mode only

Note: Dual Channel Symmetric (Interleave) Mode not supported on Mobile Intel 910GML/GMLE Express Chipset

The following bullet replaces the *Mobile Intel® 915 and 910 Express Chipset Family of Products Datasheet,* Section 10.2, *System Memory Controller*.

— Dual Channel Symmetric (Interleave) Mode not supported for Mobile Intel 910GML/GMLE Express Chipset.

§

Specification Clarifications

1. Slow DMA Transfers for LPC Devices

8-bit DMA transfers to some LPC devices, may incur latencies, that result in a slowed down transfer rate. Longer latencies may occur when the platform becomes idle and the GMCH dynamically asserts HCPUSLP# for Processor C2 states.

For example, a 4-Mbps FIR device may transmit faster than the resulting 8-bit DMA transfer rate resulting in data retransmission and lower FIR throughput.

So as not to impede the transfer rate of certain LPC Devices, the dynamic assertion of HCPUSLP# by GMCH during Processor C2 states can be disabled. Contact your Intel field representative for more details on how to disable HCPUSLP# assertion during C2 states.

2. Dynamic Video Memory Technology (DVMT) 3.0 Support Configurations

The following note should be added to Section 1.1 of the *Mobile Intel® 915 and 910 Express Chipset Family of Products Datasheet:*

Please contact your local Intel field representative for additional information regarding DVMT 3.0 support configurations.

§

Documentation Changes

1. DRAM Enhanced Addressing Update

The following section is inserted into the *Mobile Intel® 915 and 910 Express Chipset Family of Products Datasheet* Chapter 10, Section 10.2.1.3

10.2.1.3 DRAM Address Mapping

Enhanced Addressing swaps the most significant bit controlling one of the Sx_BS lines with bit 18 (which normally controls row address bit 2). Without Enhanced Addressing, rank bits are the most significant two bits of the address. With Enhanced Addressing, the rank bits are always bits 19 and 20.

Table 10-8 DRAM Device Configurations – Dual Channel Asymmetric Mode w/Enh. Addr. Swap (0)

Technology (Mb)	256	256	512	512	512	512	1024	1024	1024	1024
Row bits	13	13	13	13	13	14	14	14	13	14
Column bits	9	10	10	11	10	10	10	11	10	10
Bank bits	2	2	2	2	2	2	2	2	3	3
Width (b)	16	8	16	8	16	8	16	8	16	8
Rows	8192	8192	8192	8192	8192	16384	16384	16384	8192	16384
Columns	512	1024	1024	2048	1024	1024	1024	2048	1024	1024
Banks	4	4	4	4	4	4	4	4	8	8
Page Size (KB)	4	8	8	16	8	8	8	16	8	8
Devices per rank	4	8	4	8	4	8	4	8	4	8
Rank Size (MB)	128	256	256	512	256	512	512	1024	512	1024
Depth (M)	16	32	32	64	32	64	64	128	64	128
Addr bits [n:0]	26	27	27	28	27	28	28	29	28	29
Available in DDR	yes	yes	yes	yes	no	no	yes	yes	no	no
Available in DDRII	yes	yes	no	no	yes	yes	no	No	yes	yes
Host Address bit	Mem Addr-bit									
31	-	-	-	-	-	-	-	-	-	-
30	-	-	-	-	-	-	-	r 3	-	r 3
29	-	-	-	r 3	-	r 3	r 3	r 13	r 3	r 13

28	-	r 3	r 3	r 11	r 3	r 13	r 13	r 11	r 11	r 11
27	r 3	r 12	r 12	r 12	r 12	r 12	r 12	r 12	r 12	r 12
26	r 10	r 10	r 10	r 10	r 10	r 10	r 10	r 10	r 10	r 10
25	r 9	r 9	r 9	r 9	r 9	r 9	r 9	r 9	r 9	r 9
24	r 8	r 8	r 8	r 8	r 8	r 8	r 8	r 8	r 8	r 8
23	r 7	r 7	r 7	r 7	r 7	r 7	r 7	r 7	r 7	r 7
22	r 6	r 6	r 6	r 6	r 6	r 6	r 6	r 6	r 6	r 6
21	r 5	r 5	r 5	r 5	r 5	r 5	r 5	r 5	b 2	b 2
20	r 4	r 4	r 4	r 4	r 4	r 4	r 4	r 4	r 4	r 4
19	s 0	s 0	s 0	s 0	s 0	s 0	s 0	s 0	s 0	s 0
18	b 1	b 1	b 1	b 1	b 1	b 1	b 1	b 1	b 1	b 1
17	r 1	r 1	r 1	r 1	r 1	r 1	r 1	r 1	r 1	r 1
16	r 0	r 0	r 0	r 0	r 0	r 0	r 0	r 0	r 0	r 0
15	r 11	r 11	r 11	r 2	r 11	r 11	r 11	r 2	r 5	r 5
14	r 12	r 2	r 2	b 0	r 2	r 2	r 2	b 0	r 2	r 2
13	r 2	b 0	b 0	c 11	b 0	b 0	b 0	c 11	b 0	b 0
12	b 0	c 9	c 9	c 9	c 9	c 9	c 9	c 9	c 9	c 9
11	c 8	c 8	c 8	c 8	c 8	c 8	c 8	c 8	c 8	c 8
10	c 7	c 7	c 7	c 7	c 7	c 7	c 7	c 7	c 7	c 7
9	c 6	c 6	c 6	c 6	c 6	c 6	c 6	c 6	c 6	c 6
8	c 5	c 5	c 5	c 5	c 5	c 5	c 5	c 5	c 5	c 5
7	c 4	c 4	c 4	c 4	c 4	c 4	c 4	c 4	c 4	c 4
6	c 3	c 3	c 3	c 3	c 3	c 3	c 3	c 3	c 3	c 3
5	c 2	c 2	c 2	c 2	c 2	c 2	c 2	c 2	c 2	c 2
4	c 1	c 1	c 1	c 1	c 1	c 1	c 1	c 1	c 1	c 1
3	c 0	c 0	c 0	c 0	c 0	c 0	c 0	c 0	c 0	c 0

Table 10-9 DRAM Device Configurations –Dual Channel Interleaved Mode w/ Enh. Addr. Swap (0)

Technology (Mb)	256	256	512	512	512	512	1024	1024	1024	1024
Row bits	13	13	13	13	13	14	14	14	13	14
Column bits	9	10	10	11	10	10	10	11	10	10
Bank bits	2	2	2	2	2	2	2	2	3	3
Width (b)	16	8	16	8	16	8	16	8	16	8
Rows	8192	8192	8192	8192	8192	16384	16384	16384	8192	16384
Columns	512	1024	1024	2048	1024	1024	1024	2048	1024	1024
Banks	4	4	4	4	4	4	4	4	8	8
Page Size (KB)	4	8	8	16	8	8	8	16	8	8
Devices per rank	4	8	4	8	4	8	4	8	4	8
Rank Size (MB)	128	256	256	512	256	512	512	1024	512	1024
Depth (M)	16	32	32	64	32	64	64	128	64	128
Addr bits [n:0]	26	27	27	28	27	28	28	29	28	29
Available in DDR	yes	yes	yes	yes	no	no	yes	Yes	no	no
Available in DDRII	yes	yes	no	no	yes	yes	no	No	yes	yes
Host Address bit	Mem Addr-bit									
31	-	-	-	-	-	-	-	r 3	-	r 3
30	-	-	-	r 3	-	r 3	r 3	r 13	r 3	r 13
29	-	r 3	r 3	r 11	r 3	r 13	r 13	r 11	r 11	r 11
28	r 3	r 12	r 12	r 12	r 12	r 12	r 12	r 12	r 12	r 12
27	r 10	r 10	r 10	r 10	r 10	r 10	r 10	r 10	r 10	r 10
26	r 9	r 9	r 9	r 9	r 9	r 9	r 9	r 9	r 9	r 9
25	r 8	r 8	r 8	r 8	r 8	r 8	r 8	r 8	r 8	r 8
24	r 7	r 7	r 7	r 7	r 7	r 7	r 7	r 7	r 7	r 7
23	r 6	r 6	r 6	r 6	r 6	r 6	r 6	r 6	r 6	r 6
22	r 5	r 5	r 5	r 5	r 5	r 5	r 5	r 5	b 2	b 2
21	r 4	r 4	r 4	r 4	r 4	r 4	r 4	r 4	r 4	r 4
20	s 0	s 0	s 0	s 0	s 0	s 0	s 0	s 0	s 0	s 0
19	b 1	b 1	b 1	b 1	b 1	b 1	b 1	b 1	b 1	b 1
18	r 1	r 1	r 1	r 1	r 1	r 1	r 1	r 1	r 1	r 1
17	r 0	r 0	r 0	r 0	r 0	r 0	r 0	r 0	r 0	r 0
16	r 11	r 11	r 11	r 2	r 11	r 11	r 11	r 2	r 5	r 5
15	r 12	r 2	r 2	b 0	r 2	r 2	r 2	b 0	r 2	r 2

14	r 2	b 0	b 0	c 11	b 0	b 0	b 0	c 11	b 0	b 0
13	b 0	c 9	c 9	c 9	c 9	c 9	c 9	c 9	c 9	c 9
12	c 8	c 8	c 8	c 8	c 8	c 8	c 8	c 8	c 8	c 8
11	c 7	c 7	c 7	c 7	c 7	c 7	c 7	c 7	c 7	c 7
10	c 6	c 6	c 6	c 6	c 6	c 6	c 6	c 6	c 6	c 6
9	c 5	c 5	c 5	c 5	c 5	c 5	c 5	c 5	c 5	c 5
8	c 4	c 4	c 4	c 4	c 4	c 4	c 4	c 4	c 4	c 4
7	c 3	c 3	c 3	c 3	c 3	c 3	c 3	c 3	c 3	c 3
6	h	h	H	h	h	h	h	H	h	h
5	c 2	c 2	c 2	c 2	c 2	c 2	c 2	c 2	c 2	c 2
4	c 1	c 1	c 1	c 1	c 1	c 1	c 1	c 1	c 1	c 1
3	c 0	c 0	c 0	c 0	c 0	c 0	c 0	c 0	c 0	c 0

2. Section 5.2.15 C0DRC1 – Channel 0 DRAM Controller Mode 1

The following register bits definition replaces the *Mobile Intel® 915 and 910 Express Chipset Family of Products Datasheet,* Section 5.2.15

5.2.15 C0DRC1––Channel 0 DRAM Controller Mode 1

PCI Device: MCHBAR
Address Offset: 124h
Default Value: 00000000h
Access: RO, R/W
Size: 32 bits

Bit	Access and Default	Description
31	R/W 0 b	**Swap Mode Enable:** 0 = Swap mode disabled. Dram Address Map Follows the standard address map described in the EDS. 1 = Swap mode enabled. This bit can be enabled if all dimm are either single sided or symmetrically populated.
30	R/W 0 b	**Reserved**
29	R/W 00 b	**Address Swap Mode:** 0 = Swap Enabled for Bank Selects and Rank Selects. 1 = Swap Enabled for Bank Selects only.

<table>
<tr><th>Bit</th><th>Access and Default</th><th>Description</th></tr>
<tr><td>28:27</td><td>RO
0 b</td><td>Reserved</td></tr>
<tr><td>26:24</td><td>R/W
000 b</td><td>Swap Address Selection:
Single Channel and Asymm-Stacked Dual Channel:
<table>
<tr><th>Mode</th><th>Rank Select</th><th>Bank Select 0</th><th>Bank Select 1</th><th>Bank Select 2</th><th>Dimm Select</th></tr>
<tr><td>000</td><td>A19</td><td>std</td><td>A18</td><td>A21</td><td>A20</td></tr>
<tr><td>001</td><td>A20</td><td>std</td><td>A19</td><td>A22</td><td>A21</td></tr>
<tr><td>010</td><td>A18</td><td>std</td><td>A17</td><td>A20</td><td>A19</td></tr>
<tr><td>011</td><td>A17</td><td>Std</td><td>A16</td><td>A19</td><td>A18</td></tr>
<tr><td>Others</td><td>Rsvd.</td><td>Rsvd.</td><td>Rsvd.</td><td>Rsvd.</td><td></td></tr>
</table>
Recommended Priority: 0, 1, 2
Dual Channel Interleaved
<table>
<tr><th>Mode</th><th>Rank Select</th><th>Bank Select 0</th><th>Bank Select 1</th><th>Bank Select 2</th><th>Dimm Select</th></tr>
<tr><td>000</td><td>A20</td><td>std</td><td>A19</td><td>A22</td><td>A21</td></tr>
<tr><td>001</td><td>A21</td><td>Std</td><td>A20</td><td>A23</td><td>A22</td></tr>
<tr><td>010</td><td>A19</td><td>std</td><td>A18</td><td>A21</td><td>A20</td></tr>
<tr><td>011</td><td>A18</td><td>std</td><td>A17</td><td>A20</td><td>A19</td></tr>
<tr><td>Others</td><td>Rsvd.</td><td>Rsvd.</td><td>Rsvd.</td><td>Rsvd.</td><td></td></tr>
</table>
Recommended Priority: 2, 3, 0</td></tr>
</table>

3. Section 5.2.31 DCC – DRAM Channel Control

The following register bits definition replaces the *Mobile Intel® 915 and 910 Express Chipset Family of Products Datasheet;* Section 5.2.31

Section 5.2.31 DCC—DRAM Channel Control

MMIO Range: MCHBAR
Address Offset: 200h
Default Value: 00000000h
Access: RO, R/W
Size: 32 bits

This register controls how the DRAM channels work together. It affects how the CxDRB registers are interpreted and allows them to steer transactions to the correct channel.

Bit	Access and Default	Description
10	R/W 0 b	**Channel XOR Randomization Disable (CXRDIS):** When enabled, the DRAM Controller will try to spread page accesses evenly among the channels by including more address bits in the choice for which channel holds the requested address. 0: Channel XOR Randomization is enabled. CXRSEL's bit will be XORed with CHSEL's bit to pick the channel for a given address. 1: Channel XOR Randomization is disabled
9	R/W 0 b	**Channel XOR Randomization Control Bit (CXRSEL):** When Channel XOR Randomization is in use (see CXRDIS), the channel select will be randomized by XORing it with either host address bit 11 or 17. 0: Bit 11 will be XORed with the Channel Select bit 1: Bit 17 will be XORed with the Channel Select bit

4. Section 7.2.33 GCFGC – Graphics Clock Frequency and Gating Control

The following register bits definition replaces the *Mobile Intel® 915 and 910 Express Chipset Family of Products Datasheet;* Section 7.2.33

Section 7.2.33 GCFGC—Graphics Clock Frequency and Gating Control

PCI Device	2
Function:	0
Address Offset	F0h
Default Value	0000h
Access:	RO, R/W
Size:	16 bits

Bit	Access and Default	Description
15	R/W 0 b	**Graphics Display Clock Low Frequency Override (for 915GMS only):** 0 = Do not use Graphics cdclk low frequency override 1 = Use Graphics cdclk = 152 MHz low frequency **NOTE:** This bit is **reserved** for 915GM, 910GML and 910GMLE
14	R/W 0 b	**Reserved**
13	R/W 0 b	**GFX GVL Low Frequency Enable:** 0 = Do not Use GFX GVL low frequency target for Render Clock. 1 = Use GFX GVL low frequency target for Render Clock.
12	R/W 0 b	**GFX GVL Low Frequency Target:** 0 = 133 MHz (Default Value) 1 = Reserved
11	R/W 0 b	**Gate Core Render Clock (GCRC):** 0: Core render clock (crclk) is running 1: Core render clock (crclk) is gated
10	R/W 0 b	**Asynchronously Change Core Render Clock (ACCRC):** A 0 to 1 transition on this bit will immediately load new pre- and post-divider values for the crclk and crx2clk. Writing 1 to 1, 1 to 0, and 0 to 0 have no effect.

Bit	Access and Default	Description
9	R/W 0 b	**Gate Core Display Clock (GCRC):** 0: Core display clock (cdclk) is running 1: Core display clock (cdclk) is gated
8	R/W 0 b	**Asynchronously Change Core Display Clock (ACCDC):** A 0 to 1 transition on this bit will immediately load new pre- and post-divider values for the cdclk. Writing 1 to 1, 1 to 0, and 0 to 0 have no effect.
7	R/W 0 b	**Core Display Low Frequency Enable:** 0 = Do not Use low frequency target for Display Clock. 1 = Use low frequency target (152 MHz) for Display Clock. (For 915GMS only) **NOTE:** This bit is **reserved** for 915GM / 915GME and 910GM / 910GMLE.
6:4	R/W 000 b	**Graphics Core Display Clock Select:** 000 = 190/200 MHz (Intel 915GM / 915GMS / 915GME and Intel 910GML / 910GMLE) 001 = 213/222 MHz (Intel 915GM / 915GME) 010 = Reserved 011 = Reserved 100 = 333 MHz (Intel 915GM/GME @ 1.5 V only) 101 = Reserved 110 = Reserved 111 = Reserved
3	RO 0 b	**Reserved**
2:0	R/W 000 b	**Graphics Core Render Clock Select:** 000 = 160/166 MHz (Intel 915GM / 915GMS / 915GME and Intel 910GML / 910GMLE) 001 = 190/200 MHz (Intel 915GM / 915GME) 010 = Reserved 011 = Reserved 100 = 333 MHz (Intel 915GM/GME @ 1.5 V only) 101 = Reserved Others = Reserved

5. Section 5.2.12 C0DRT1 – Channel 0 DRAM Timing Register 1

The following register bits definition replaces the *Mobile Intel® 915 and 910 Express Chipset Family of Products Datasheet;* Section 5.2.12

Section 5.2.12 C0DRT1—Channel 0 DRAM Timing Register 1

PCI Device: MCHBAR
Address Offset: 114h
Default Value: 00006111h
Access: RO, R/W
Size: 32 bits

Bit	Access and Default	Description
31:30	RO 00 b	**Reserved**
29:28	R/W 00 b	**Read to Pre-charge (tRTPC):** These bits control the number of clocks that are inserted between a read command to a row pre-charge command to the same rank. **Encoding** **tRP** 00: BL/2 01: Reserved 10: **Reserved** 11: **Reserved**
27:24	R/W 0 h	**Reserved**

Bit	Access and Default	Description
23:20	R/W 6 h	**Activate to Precharge Delay (tRAS):** This bit controls the number of DRAM clocks for tRAS. Minimum recommendations are beside their corresponding encodings. 0000: Reserved 0001: Reserved 0010: Reserved 0011: Reserved 0100: 4 clocks 0101: 5 clocks 0110: 6 clocks 0111: 7 clocks (DDR333) 1000: 8 clocks 1001: 9 clocks (DDR 2 400) 1010: 10 clocks 1011: 11 clocks 1100: 12 clocks (DDR 2 533) 1101: 13 clocks 1110: 14 clocks 1111: 15 clocks **Recommended values:** 7h DDR 333 9h DDR 2 400 Ch DDR 2 533
19	RO 0 b	**Reserved**
18	R/W 0 b	**Reserved**
17	R/W 0 b	**Activate to Activate Delay:** Control Act to Act delay between the different banks of the same rank. Trr is specified in “ns”. 10 ns for 2-KB page size and 7.5 ns for 1-KB page 0 = 2 Clock 1 = 3 Clock

<table>
<tr><th>Bit</th><th>Access and Default</th><th>Description</th></tr>
<tr><td>16</td><td>R/W
0 b</td><td>Pre-All to Activate Delay (tRPALL).
This is applicable only to 8 bank architectures.
Must be set to 1 if any Rank is populated with 8 bank device technology.
0: tRPALL = tRP
1: tRPALL = tRP + 1</td></tr>
<tr><td>15:11</td><td>R/W
01100 b</td><td>Refresh Cycle Time (tRFC).
Refresh cycle time is measured from a Refresh command (REF) until the first Activate command (ACT) to the same rank, required to perform a read or write.
DDR 2 tRFC spec
<table>
<tr><th>tRFC</th><th>256 Mb</th><th>512 Mb</th><th>1 Gb</th></tr>
<tr><td>DDR2 400 (5 ns)</td><td>75 ns = 15 clks</td><td>105 ns = 21 clks</td><td>127.5 ns = 26 clks</td></tr>
<tr><td>DDR2 533 (3.75 ns)</td><td>75 ns = 20 clks</td><td>105 ns = 28 clks</td><td>127.5 ns = 34clks</td></tr>
</table>
DDR 1 tRFC spec
<table>
<tr><th>tRFC</th><th>64 Mb -512 Mb</th><th>1 Gb</th></tr>
<tr><td>DDR 333 (6 ns)</td><td>75 ns = 13 clks</td><td>120 ns = 20 clks</td></tr>
</table>
00000b – 11111b Zero Clocks to Thirty-one Clocks respectively
Actual clocks period depends on DDR clock frequency.
BIOS should round up. If the required clock count exceeds as allowed by this register, the bios should set this register to the max value and set corresponding bits in SDBUP.</td></tr>
<tr><td>10</td><td>RO</td><td>Reserved</td></tr>
<tr><td>9:8</td><td>R/W
01 b</td><td>CASB Latency (tCL):
This value is programmable on DDR 2 SO-DIMM’s. The value programmed here must match the CAS Latency of every DDR 2 SO-DIMM in the system.
Encoding DDR CL DDR2 CL
00: 3 5
01: 2.5 4 (DDR2 533)
10: Reserved 3 (DDR2 400)
11: Reserved Reserved
NOTE: Only the above recommended DDR2 timing values have been validated.</td></tr>
<tr><td>7</td><td>RO</td><td>Reserved</td></tr>
</table>

Bit	Access and Default	Description
6:4	R/W 001 b	**DRAM RASB to CASB Delay (tRCD):** This bit controls the number of clocks inserted between a row activate command and a read or write command to that row. Encoding DDR tRCD DDR2 tRCD 000: 2 2 clocks 001: 3 3 clocks (DDR2 400) 010: 4 4 clocks (DDR2 533) 011: 5 5 clocks 100 - 111: Reserved Reserved **NOTE:** Only the above recommended DDR2 timing values have been validated.
3	RO	**Reserved**
2:0	R/W 001 b	**DRAM RASB Precharge (tRP):** This bit controls the number of clocks that are inserted between a row precharge command and an activate command to the same rank. Encoding DDR tRP DDR2 tRP 000: 2 2 Clocks 001: 3 3 Clocks (DDR2 400) 010: 4 4 Clocks (DDR2 533) 011: 5 5 Clocks 100 - 111: Reserved **NOTE:** Only the above recommended DDR2 timing values have been validated.

6. LBKLT_CRTL Signal Description Update

The LBKLT_CRTL signal description in Section 2.5.3 should be replaced with the following:

LBKLT_CRTL	O HVCMOS	**Panel Backlight Brightness Control:** Panel brightness control. This signal is also called VARY_BL in the CPIS specification and is used as the PWM Clock input signal. The accuracy of the PWM duty cycle of LBKLT_CRTL signal for any given value will be within ±20 ns.

7. Section 17.2.14 C0DRC0 – Channel 0 DRAM Controller Mode 0

The following register bit definition replaces the *Mobile Intel® 915PM/GM/GME/GMS and 910GML/GMLE Express Chipset EDS* Volume 2.0 (Doc #17139); Section 17.2.14.

Section 17.2.14 C0DRC0—Channel 0 DRAM Controller Mode 0

PCI Device: MCHBAR
Address Offset: 120h
Default Value: 40002801h
Access: RO, R/W
Size: 32 bits

Bit	Access & Default	Description
31:30	RO 01 b	**Reserved**
29	R/W 0 b	**Initialization Complete (IC):** This bit is used for communication of software state between the memory controller and the BIOS. BIOS sets this bit to 1 after initialization of the DRAM memory array is complete.
28	R/W 0 b	**Reserved**
27:24	R/W 0 h	**Active SDRAM Ranks:** Implementations may use this field to limit the maximum number of SDRAM ranks that may be active at once. 0000: All ranks allowed to be in the active state 0001: One Rank 0010: Two Ranks 0011: Three Ranks Others: Reserved. If this field is set to a non-zero value, then bits CXDRT2(4:0) should be set to the minimum value as described by the formula, else the system hangs.
23:22	R/W 00 b	**Reserved**
21:20	R/W 00 b	**Reserved**

Bit	Access & Default	Description
19:18	RO 00 b	**Reserved**
17	R/W 0 b	**Reserved**
16	R/W 0 b	**Reserved**
15	R/W 0 b	**CMD Copy Enable:** In a single channel mode, the CMD pins (MA, BS, RAS, CAS, WE) on both channels are driven and are physical copies of each other. Setting this bit disables the CMD pins on channel B. Having the additional copy of CMD pins helps reduce loading on these pins, since in a two SO-DIMM system, each copy can be routed up to separate SO-DIMM. In a single DIMM system, the second copy can be disabled to eliminate unnecessary toggling of these pins. If this bit needs to be set, BIOS should do that before memory init sequence. This bit should not be set in a dual channel system
14	RO 0 b	**Reserved**
13:12	R/W 10 b	**Reserved**
11	RO 1 b	**Reserved**
10:8	R/W 000 b	**Refresh Mode Select (RMS):** This field determines whether refresh is enabled and, if so, at what rate refreshes will be executed. 000: Refresh disabled 001: Refresh enabled. Refresh interval 15.6 µs 010: Refresh enabled. Refresh interval 7.8 µs Other: Reserved
7	RO 0 b	**Reserved**

Bit	Access & Default	Description
6:4	R/W 000 b	**Mode Select (SMS):** These bits select the special operational mode of the DRAM interface. The special modes are intended for initialization at power up. **000**: Post Reset state – When the GMCH exits reset (power-up or otherwise), the mode select field is cleared to 000. During any reset sequence, while power is applied and reset is active, the GMCH deasserts all DRAM CLK and CKE signals. After internal reset is deasserted, DRAM CLK and CKE signals remain deasserted until this field is written to a value different than "000". On this event, DRAM CLKs are enabled and CKE signals remain deasserted for a minumum of 35 ns before CKE signals are asserted. During suspend, GMCH internal signal triggers DRAM controller to flush pending commands and enter all ranks into Self-Refresh mode. As part of resume sequence, GMCH will be reset – which will clear this bit field to "000" and maintain all DRAM CLK and CKE signals deasserted. After internal reset is deasserted, DRAM CLK and CKE signals remain deasserted until this field is written to a value different than "000". On this event, DRAM CLKs are enabled and CKE signals remain deasserted for a minumum of 35 ns before CKE signals are asserted. During entry to other low power states (C3, S1), GMCH internal signal triggers DRAM controller to flush pending commands and enter all ranks into Self-Refresh mode. During exit to normal mode, GMCH signal triggers DRAM controller to exit Self-Refresh and resume normal operation without S/W involvement. **001:** NOP Command Enable – All CPU cycles to DRAM result in a NOP command on the DRAM interface. **010:** All Banks Pre-charge Enable – All CPU cycles to DRAM result in an "all banks precharge" command on the DRAM interface. **011:** Mode Register Set Enable – All CPU cycles to DRAM result in a "mode register" set command on the DRAM interface. Host address lines are mapped to DRAM address lines in order to specify the command sent. Host address lines [12:3] are mapped to MA[9:0], and HA[13] is mapped to MA[11]. **101**: Reserved **110: CBR Refresh Enable** – In this mode all CPU cycles to DRAM result in a CBR cycle on the DRAM interface **111:** Normal operation
3	R/W 0 b	**Reserved**

Bit	Access & Default	Description
2	R/W 0 b	**Burst Length (BL):** The burst length is the number of QWORDS returned by a SO-DIMM per read command, when not interrupted. This bit is used to select the DRAM controller's Burst Length operation mode. It must be set to match to the behavior of the SO-DIMM. 0: Burst Length of 4 1: Burst Length of 8
1:0	RO 01 b	**DRAM Type (DT):** Used to select between supported SDRAM types. 00: Reserved 01: Dual Data Rate (DDR) SDRAM 10: Dual Data Rate 2 (DDR 2) SDRAM 11: Reserved

8. Section 17.2.15 C0DRC1 – Channel 0 DRAM Controller Mode 1

The following register bit definition replaces the *Mobile Intel® 915PM/GM/GME/GMS and 910GML/GMLE Express Chipset EDS* Volume 2.0 (Doc #17139); Section 17.2.15.

PCI Device: MCHBAR
Address Offset: 124h
Default Value: 00000000h
Access: RO, R/W
Size: 32 bits

Bit	Access & Default	Description
31	R/W 0 b	**Reserved**
30	R/W 0 b	**Reserved**
29:28	R/W 00 b	**Reserved**
27	RO 0 b	**Reserved**

Bit	Access & Default	Description
26:24	R/W 000 b	**Reserved**
23:20	RO 00 h	**Reserved**
19:16	R/W 0 h	**CKE Tri-state Enable Per Rank:** Bit 16 corresponds to rank 0 Bit 17 corresponds to rank 1 Bit 18 corresponds to rank 2 Bit 19 corresponds to rank3 0 = CKE is not tri-stated. 1 = CKE is tri-stated. This is set only if the Rank is physically not populated.
15:13	RO 000 b	**Reserved**
12	R/W 0 b	**CS# Tri-state Enable (CSBTRIEN):** When set to a 1, the DRAM controller will tri-state CS# when the corresponding CKE is deasserted. 0: Address Tri-state Disabled 1: Address Tri-state Enabled
11	R/W 0 b	**Address Tri-state Enable (ADRTRIEN):** When set to a 1, the DRAM controller will tri-state the MA, CMD, and CSB (CSB if lines only when all CKEs are deasserted. CKEs deassert based on Idle timer or max rank count control. 0: Address Tri-state Disabled 1: Address Tri-state Enabled
10	R/W 0 b	**Reserved**
9	RO 0 b	**Reserved**

Bit	Access & Default	Description
8	R/W 0 b	**DRAM Channel IO-Buffers Activate:** This bit is cleared to 0 during reset and remains inactive until it is set to 1 by BIOS. In addition, this bit can be cleared and set during debug procedures. **While 0**, the DRAM controller core logic forces the state of the IO-buffers in this channel to “reset” or “preset”, depending on the specific buffer type. The buffers’ state flops (counters, pointers, etc) are forced into their initial state. The core logic receive FIFO read pointer is forced into its initial state. Output signal groups are driven to their initial state (tri-stated). Refer to the following tables for the specific state. **While 1**, the DRAM controller core logic enables the DRAM IO-buffers in this channel to operate normally.
7	R/W 0 b	**Reserved**
6	R/W 0 b	**Reserved**
5	RO 0 b	**Reserved**
4	R/W	**Reserved**
3:2	RO 00 b	**Reserved**
1	R/W 0 b	**Reserved**
0	R/W 0 b	**Reserved**

§