Intel® 855GM/855GME Chipset Graphics and Memory Controller Hub (GMCH)

Specification Update

November 2007

Notice: The Intel® 855GM/855GME chipset may contain design defects or errors known as errata, which may cause the product to deviate from published specifications. Current characterized errata are documented in this Specification Update.

Document Number: 253572-007

Contents

Revision History

Revision	Description	Date
-001	Initial Release	July 2003
-002	Added the Intel 855GME chipset	October 2003
-003	Document Change #1 added	September 2004
-004	Document Changes #2 & #3 added	October 2004
-005	Errata Change #5 added Specification Change #1 added Document Change #4 added	November 2004
-006	Errata Change #6 and #7 added Specification Change #2 added Document Change #5 added	March 2005
-007	Errata Change #8 added Errata Change #4 Updated	November 2007

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Preface

This document is an update to the specifications contained in the documents listed in the following Affected Documents/Related Documents table. It is a compilation of device and document errata and specification clarifications and changes, and is intended for hardware system manufacturers and for software developers of applications, operating system, and tools.

Information types defined in the Nomenclature section of this document are consolidated into this update document and are no longer published in other documents. This document may also contain information that has not been previously published.

Affected Documents

Document Titel	Document Number/Locataion
Intel® 855GM/855GME Chipset GMCH Datasheet	252615-004

Nomenclature

Specification Changes are modifications to the current published specifications. These changes will be incorporated in the next release of the specifications.

Errata are design defects or errors. Errata may cause the Intel 855GM/855GME Chipset GMCH behavior to deviate from published specifications. Hardware and software designed to be used with any given stepping must assume that all errata documented for that stepping are present on all devices.

Specification Clarifications describe a specification in greater detail or further highlight a specification's impact to a complex design situation. These clarifications will be incorporated in the next release of the specifications.

Documentation Changes include typos, errors, or omissions from the current published specifications. These changes will be incorporated in the next release of the specifications.

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Summary Table of Changes

The following table indicates the Specification Changes, Errata, Specification Clarifications or Documentation Changes that apply to the listed Intel 855GM/855GME chipset GMCH steppings. Intel intends to fix some of the errata in a future stepping of the component and to account for the other outstanding issues through documentation or Specification Changes as noted. This table uses the following notations:

Codes Used in Summary Table

X:	Erratum, Specification Change or Clarification that applies to this stepping.
Doc:	Document change or update that will be implemented.
Fix:	This erratum is intended to be fixed in a future stepping of the component.
Fixed:	This erratum has been previously fixed.
NoFix	There are no plans to fix this erratum.
(No mark) or (Blank Box):	This erratum is fixed in listed stepping or specification change does not apply to listed stepping.
Shaded:	This item is either new or modified from the previous version of the document.

Errata

NO.	Stepping		PLANS	ERRATA
	A2			
	855GM	855GME		
1	X	X	No Fix	VGA Panning Test Issue
2	X	X	No Fix	VGA Timing issue
3	X	X	No Fix	Intermittent System hangs during power cycle test.
4	X	X	No Fix	Display may flicker when integrated graphics and ECC support are enabled UPDATED
5		X	No Fix	Anomalous System Behavior May Occur When AGP GART Size is 64 MB and APBASE bit 27 is Set
6		X	No Fix	AGP PCI Write to system memory may be corrupted.
7		X	No Fix	AGP write failure when ECC memory is enabled.
8	X	X	No Fix	855GM/855GME Express Chipset SMRAM D_CLS Bit Erratum

Specification Changes

NO.	SPECIFICATION CHANGES
1	24 Bit LVDS Interface Will Not Be Supported on 855GM/GME Platforms
2	ECC is not a validated or supported feature on 855GM/GME Mobile Platforms.

Specification Clarifications

NO.	Stepping	PLANS	SPECIFICATION CLARIFICATIONS
	A2		
1	X	No Fix	Graphics Limitations Using ECC DIMM Memory

Documentation Changes

NO.	Stepping		DOCUMENTATION CHANGES
	A2		
	855GM	855GME	
1	X	X	Ball definition for RSTIN# incorrectly shown in table 44
2	X	X	DVODETECT internal resistor incorrectly defined in Section 3.6.3
3		X	Section 8.4 and Section 10 incorrectly shows some signal pins as reserved
4	X	X	LVDS Panel Clock Frequency Range Is Incorrect
5	X	X	Electrical Characteristics Chapter added to the Public Datasheets.

Identification Information

Component Identification via Programming Interface

The Intel 855GM/855GME chipset GMCH may be identified by the following register contents.

Component	Stepping	Vendor ID[1]	Device ID[2]	Revision Number[3]
855GM	A2	8086h	3580h (Device #0)	02h
855GME	A2	8086h	3580h (Device #0)	02h

NOTES:

1. The Vendor ID corresponds to bits 15-0 of the Vendor ID Register located at offset 00-01h in the PCI function 0 configuration space.
2. The Device ID corresponds to bits 15-0 of the Device ID Register located at offset 02-03h in the PCI function 0 configuration space.
3. The Revision Number corresponds to bits 7-0 of the Revision ID Register located at offset 08h in the PCI function 0 configuration space.

Component Marking Information

The Intel 855GM chipset GMCH may be identified by the following component markings.

Component	Stepping	S-Spec	Top Marking	Notes
855GM	A2	SL6WW	RG82855GM	Production 82855GM GMCH
855GME	A2	SL72L	RG82855GME	Production 82855GME GMCH

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Errata

1. VGA Panning

Problem: VGA text mode diagnostic and stress test applications that use pixel panning can experience temporary visual anomalies under certain memory configurations. This issue was seen in two test configurations.

1. Test applications using a single VGA font table with a 32-kB font buffer range could fail. The failure can occur using 64-MB technology products that use 2-kB and 4-kB page sizes. This failure was seen in a diagnostic utility.
2. Test applications using multiple VGA font tables could fail if the first two fonts are from different tables. This failing condition can occur in any memory configuration. This failure was seen in a stress test utility.

Implication: Entire scan lines will appear to flicker in some VGA diagnostic and stress test applications. However, there are no known customer sightings of this erratum. No known end user applications fail for this erratum.

Workaround: No workaround exists.

Status: There are no plans to fix this erratum in silicon. For steppings affected, see the *Summary Tables of Changes.*

2. VGA Timings

Problem: Some VGA applications, running in 40-column modes that use a non-black border color may experience color/visual issues on systems configured with certain monitors.

Implication: 40-column VGA modes may experience visual color anomalies on some CRT monitors. This was observed using VGA focused Intel test software. With certain monitors, colors in active areas may change as the border color changes. As observed while using the test software, visual color anomalies can range from a slight color change difference to a blank screen. Based on the lack of customer or end user reported issues related to this erratum, the number of VGA applications that run in 40-column modes and also use non-black border colors is low. Based on Intel's validation and compatibility testing, the number of CRT monitors that exhibit this color anomaly is also low.

Workaround: No workaround exists.

Status: There are no plans to fix this erratum in silicon. For steppings affected, see the *Summary Tables of Changes.*

3. Intermittent System Hangs during BIOS Memory Testing When Power Cycle Testing

Problem: Systems may intermittently hang during BIOS memory testing as a result of the internal RCOMP state machine colliding with BIOS induced RCOMP cycle.

Implication: System hang may occur during boot-up or resume from S3. No other failures have been identified or reported. Issues are resolved with a BIOS workaround.

Workaround: Please refer to Intel 855GM Memory BIOS Specification and BIOS Spec Update for details.

Status: There are no plans to fix this erratum in silicon. For steppings affected, see the *Summary Tables of Changes.*

4. Display May Flicker When Integrated Graphics and ECC Support Are Enabled

Problem: Display flicker and flashing may occur when integrated graphics and ECC support are enabled under certain graphics resolution modes.

Implication: A potentially undesirable amount of display flicker may occur.

Workaround: No workaround available.

Status: There are no plans to fix this erratum in silicon. For steppings affected, see the *Summary Tables of Changes.*

5. Anomalous System Behavior May Occur When AGP GART Size Is 64 MB and APBASE Bit 27 Is Set

Problem: Incorrect address decoded when AGP aperture size is set to 64 MB and the aperture base has bit 27 set (e.g. APBASE=0xD8000000 causes failures, but 0xD0000000 is fine).

Implication: Problem may result in anomalous system behavior which can cause a system hang.

Workaround: Use an aperture base size of 128 MB or 256 MB. If using a 64-MB aperture size, set APBASE such that bit 27 is cleared (e.g. use 0xD0000000 instead of 0xD8000000).

Status: There are no plans to fix this erratum in silicon. For steppings affected, see the *Summary Tables of Changes.*

6. AGP Write Failure When ECC Memory is Enabled.

Problem: Memory corruption or system hang may result if an AGP semantic write cycle targets a cache line in the AGP aperture window at the same time a PCI semantic write cycle from another PCI device is targeting the same cache line if ECC memory is enabled.

Implication: If ECC memory is enabled, data corruption or system hang may result.

Workaround: No workaround available. ECC memory will not be supported when using an AGP graphics device.

Status: There are no plans to fix this erratum in silicon. For steppings affected, see the *Summary Tables of Changes.*

7. A4, B4 – AGP PCI Write to System Memory May Be Corrupted

Problem: Display corruption or a system hang may result if an upstream AGP FRAME#-based PCI write crosses a 32-byte aligned boundary. Note that upstream AGP FRAME#-based PCI writes which cross a 32-byte aligned boundary are expected to be rare.

Implication: The issue may cause display corruption or a system hang. With the workaround implemented, Intel has done extensive validation and expects less than 3% impact on system performance.

Workaround: A BIOS workaround is available which disconnects upstream AGP FRAME#-based PCI writes to system memory at 32-byte aligned boundaries. Please refer to your Intel representative for BIOS workaround details.

Status: There are no plans to fix this erratum in silicon. For steppings affected, see the *Summary Tables o Changes.*

8. Mobile Intel® 855GM/855GME Express Chipset SMRAM D_CLS Bit Erratum

Problem: Data and Stack which resides in Extended SMRAM (TSEG/HSEG) is inaccessible if D_CLS bit (Bus 0, Device 0, Function 0, Register 60h, bit 5) is set.

Implication: May result in a system hang..

Workaround: See *Intel® 852GM/855GM/855GME/852GME/852PM/852GMV BIOS Spec Update* Rev 2.1 or later.

Status: No Fix. For steppings affected, see the *Summary Table of Changes.*

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Specification Changes

1. 24-Bit LVDS Will Not Be Supported on 855GM/855GME Platforms

24-bit LVDS support has been dropped from 855GM/855GME platforms. This change affects Section 6.5.2.1 paragraph 4. Text stating 24-bit LVDS should be ignored.

2. ECC Is Not a Validated or Supported Feature on 855GM/GME Mobile Platforms

ECC is not a validated or supported feature on 855GM/GME mobile platforms. All text stating support for ECC is not applicable for mobile platforms.

For ECC usage in embedded applications please refer to the *Intel® 855GME Embedded Chipset Graphics and Memory Controller Hub (GMCH) Specification Update Addendum.*

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Specification Clarifications

1. Graphics Limitations Using ECC DIMM Memory

Memory with ECC enabled requires more system memory resources. This will cause the Integrated graphics engine to have less memory bandwidth for accesses to the graphics frame buffer. A system BIOS workaround is required to allow integrated graphics more access time to memory. (contact your BIOS vendor for latest updates).

SO-DIMM memory with ECC enabled is **not** supported.

DIMM memory with ECC enabled will be supported under the following display configurations for non- mobile configurations. Please see the following tables below for supported display configurations**.**

Supported internal graphics display configuration with ECC enabled:

Graphics Core (Minimum Frequency)	200MHz
Memory (Minimum Frequency)	266MHZ
FSB (Minimum Frequency)	400 MHz
Display Usage	Dual Independent Display
Dual Pipe Independent (Maximum Display Resolution)	Please contact your local Field Represenative for supported Dual Independent Display configurations
Single Pipe Independent (Maximum Display Resolution)	1600x1200, 2 BPP, 85 Hz (DCLK=56.25MHz) on CRT/DVO 1600x1200, 4 BPP, 85 Hz (DCLK=56.25MHz) on CRT/DVO 1600x1200, 4 BPP, 60 Hz (DCLK=65MHz) on LVDS
LVDS Support	Yes
ADD card Support	Yes
Display Concurrency	1 Plane Per Pipe + Cursor + Overlay
SSC Support	No

NOTE: Bytes per pixel (BPP)

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Documentation Changes

1. Ball Definition for RSTIN# Incorrectly shown in Table 51

Table 51, “XOR Chain Exclusion List of Pins” incorrectly shows the ball definition for RSTIN# to be D28. Actual ball definition is AD28. D28 is a VSS ball. This is the only reference where RSTIN# is incorrectly defined. Ballout diagram in Section 11 is correct.

2. DVODETECT Internal Resistor Is Improperly Defined in Section 3.6.3

The text in Section 3.6.3 Intel 855GME GMCH DVO/I2C to AGP Pin Mapping states:

“The GMCH has an internal 8.2-k, pull-up on this signal that will naturally pull it high. If an AGP graphics device is present, the signal will be pulled low at the AGP graphics device and the AGP/DVO mux select bit in the SHIC register will be set to AGP mode.”

Text should now read:

“The GMCH has an internal 8.2-k, pull-down on this signal that will naturally pull it low. If an AGP graphics device is present, the signal will be pulled high at the AGP graphics device and the AGP/DVO mux select bit in the SHIC register will be set to AGP mode.”

3. Section 9.4 and Section 11 Incorrectly Show Some Signal Pins As Reserved

Section 9.4 Table 51 , Section 11 Figure 9, and Section 11 Table 58 show balls D2, D3, B3, F2, F3, L4 , and B2 as reserved. Balls should be defined as follows for the 855GME.

Ball	Signal Name
D2	GWBF#
D3	GRBF#
B3	GREQ#
F2	GSBSTB
F3	GSBSTB#
L4	GCBE2#
B2	GGNT#

4. LVDS Panel Clock Range Is Incorrect

LVDS Flat Panel Clock Speed is shown as a range of 35 MHz – 112 MHz throughout the document. The lower end should be changed to 25 MHz. The correct range is from 25 MHz – 112 MHz. This correction will apply to Table 2 Intel 855GM/855GME GMCH Interface Clocks, Section 6.5.2.1 paragraph 1, and Section 6.5.2.2 paragraph 2.

5. Electrical Characteristics Chapter Added to the Public Datasheets

Electrical Characteristics Chapter 8 was added to the Intel 855GM/855GME Chipset Graphics and Memory Controller Hub (GMCH) Public Datasheets. Information added include the following information:

Electrical Characteristics

- Absolute Maximum Ratings
- Thermal Characteristics
- Power Characteristics
- Signal Groups
- DC Characteristics
  - General
  - DAC DC Characteristics
  - DAC Reference and Output Specifications

Note: There are chapter re-assignments as a result of adding the Electrical Characteristics chapter to the Public Datasheets. Testability is now Chapter 9, Intel 855GM/GME GMCH Strap Pins is now Chapter 10, and Ballout and Package Information is now Chapter 11.

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