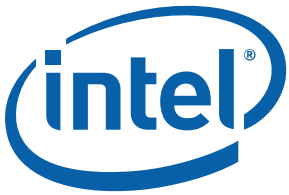


Intel® 7300 Chipset Memory Controller Hub (MCH)

Specification Update

October 2009

Notice: The Intel® 7300 Chipset Memory Controller Hub (MCH) may contain design defects or errors known as errata which may cause the product to deviate from published specifications. Current characterized errata are available on request.

Document Number: 318083-004

Contents

Revision History

Date	Revision	Description
September 2007	-001	Initial Relase
March 2008	-002	Added Erratum #53
April 2008	-003	Added Erratum #54
October 2009	-004	Added Erratum #55 and #56

Preface

This document is an update to the specifications contained in the Affected Documents table below. This document is a compilation of device and documentation errata, specification clarifications and changes. It is intended for hardware system manufacturers and software developers of applications, operating systems, or tools.

Information types defined in Nomenclature are consolidated into the specification update and are no longer published in other documents.

This document is intended to errata for the Intel® 7300 Chipset Memory Controller Hub (MCH). Customers can use this data to know and understand the Intel® 7300 Chipset Memory Controller Hub (MCH) issues that Intel has identified.

Affected Documents

Document Title	Document Number / Location
Intel® 7300 Chipset Memory Controller Hub (MCH) Datasheet	318082-001

Related Documents

Document Title	Document Number / Location
None	

Nomenclature

Errata are design defects or errors. These may cause the Intel® 7300 Chipset Memory Controller Hub (MCH) behavior to deviate from published specifications. Hardware and software designed to be used with any given stepping must assume that all errata documented for that stepping are present on all devices.

S-Spec Number is a five-digit code used to identify products. Products are differentiated by their unique characteristics,e.g., core speed, L2 cache size, package type, etc. as described in the processor identification information table. Read all notes associated with each S-Spec number.

Specification Changes are modifications to the current published specifications. These changes will be incorporated in any new release of the specification.

Specification Clarifications describe a specification in greater detail or further highlight a specification's impact to a complex design situation. These clarifications will be incorporated in any new release of the specification.

Documentation Changes include typos, errors, or omissions from the current published specifications. These will be incorporated in any new release of the specification.

Note: Errata remain in the Specification Update throughout the product's lifecycle, or until a particular stepping is no longer commercially available. Under these circumstances, errata removed from the Specification Update are archived and available upon request. Specification changes, specification clarifications and documentation changes are

removed from the Specification Update when the appropriate changes are made to the appropriate product specification or user documentation (datasheets, manuals, etc.).

Summary Tables of Changes

The following tables indicate the errata, specification changes, specification clarifications, or documentation changes which apply to the Intel® 7300 Chipset Memory Controller Hub (MCH). Intel may fix some of the errata in a future stepping of the component, and account for the other outstanding issues through documentation or specification changes as noted. These tables uses the following notations:

Codes Used in Summary Tables

Stepping

X:	Erratum exists in the stepping indicated. Specification Change or Clarification that applies to this stepping.
(No mark) or (Blank box):	This erratum is fixed in listed stepping or specification change does not apply to listed stepping.

Status

Doc:	Document change or update will be implemented.
Plan Fix:	This erratum may be fixed in a future stepping of the product.
Fixed:	This erratum has been previously fixed.
No Fix:	There are no plans to fix this erratum.

Row

Change bar to left of table row indicates this erratum is either new or modified from the previous version of the document.

Errata (Sheet 1 of 3)

Number	Stepping	Status	Erratum
	A1		
1	X	No Fix	PCI Express* Intel® Interconnect BIST (Intel® IBIST) on x8 Port Will Not Stop Testing of Entire Port if an Error is Detected on Any Lane Other Than Lowest 4 Lanes of the Port
2	X	No Fix	Leakage from 1.5V VCC to 1.2V VTT
3	X	No Fix	Processor Reset Bit in System Reset Register Fails to Clear
4	X	No Fix	ESI Reset Timeout Error Incorrectly Logged in PEX Error Register
5	X	No Fix	The NRECADDRH[3:0] Will Log Incorrect Information for Certain FSB Errors
6	X	No Fix	Packet May be Dropped When Entering PCI Express* Recovery Mode Resulting in Spurious Correctable Error being Logged
7	X	No Fix	Simultaneous Memory Errors May Result in Incorrect Data being Logged in Error Reporting Registers
8	X	No Fix	Coalesce Mode Cannot be Used with Max Payload Size of 256B
9			Erratum Removed
10			Erratum Removed

Errata (Sheet 2 of 3)

Number	Stepping	Status	Erratum
	A1		
11	X	No Fix	Incorrect Default Settings for Intel® 7300 Chipset Memory Controller Hub (MCH) Queuing Structure
12	X	No Fix	Accesses to IOxAPIC Address Space of Disabled PCI Express* Ports Will Cause System Hang
13			Erratum Removed
14			Erratum Removed
15			Erratum Removed
16	X	No Fix	Hard Reset to the Intel® 7300 Chipset Memory Controller Hub (MCH) Via Intel® 631xESB/632xESB I/O Controller Hub Could Result in False Correctable Receiver Errors Being Logged
17	X	No Fix	MCH B1Err Errors Logged Incorrectly
18			Erratum Removed
19			Erratum Removed
20	X	No Fix	Spurious B3 Errors (Coherency Violation Error for Explicit Writebacks) May be Logged
21			Erratum Removed
22			Erratum Removed
23			Erratum Removed
24	X	No Fix	FB-DIMM I/O Compensation Logic for the Intel® 7300 Chipset Memory Controller Hub (MCH) Does Not Allow for Individual Branch Initialization
25			Erratum Removed
26	X	No Fix	The Intel® QuickData Technology Integrated DMA Engine May Log Both FERR and NERR for Single Error
27	X	No Fix	Thermal Throttling Update Values Should be Disabled Prior to Link Initialization
28	X	No Fix	Memory Error Incorrectly Logged in Mirrored Mode
29	X	No Fix	Coherency Engine Errors Logged in NERR not Signaled
30	X	No Fix	Incorrect Error Reporting for PCI Express* Non-Fatal and Fatal Errors
31	X	No Fix	Incorrect Intel® 7300 Chipset Memory Controller Hub (MCH) Default Settings
32	X	No Fix	Memory Controller Branch Incorrectly Degrades on Replay Transaction
33	X	No Fix	PCI Express* DMA Transactions May Not be Tracked Correctly in the Intel® 7300 Chipset Memory Controller Hub (MCH)
34	X	No Fix	Spurious Errors Logged in Reserved Error Log Register Field
35	X	No Fix	Inbound Flow Control Logic for PCI Express* not Configured Correctly
36	X	No Fix	Memory Queue Depth Incorrectly Sized
37			Erratum Removed
38	X	No Fix	Northbound Lane May Lose Bitlock During TS1 Loopback
39	X	No Fix	S4 or S5 Hang Due to PCI Express* Bus Master Traffic
40	X	No Fix	Incorrect Source ID May Be Logged in the RPERRSID for Root Port Detected Errors
41			Erratum Removed
42			Erratum Removed
43			Erratum Removed
44	X	No Fix	Incorrect Default Configuration Values for the Data Manager and Coherency Engine Threshold Limits

Errata (Sheet 3 of 3)

Number	Stepping	Status	Erratum
	A1		
45	X	No Fix	The Intel® 7300 Chipset Memory Controller Hub (MCH) Does Not Log Select PEX_NF_FERR/NERR Registers When Severity is Set to Non-Fatal
46	X	No Fix	Insufficient PCI Express* Inbound Flow Control Credits
47	X	No Fix	Header Logs have Incorrect Data when Logging UR for an Outbound Completion with UR
48	X	No Fix	Partial Write Combining may cause Logic in the Intel® 7300 Chipset Memory Controller Hub (MCH) to Hang
49	X	No Fix	M13Err, M14Err or M15Err may be Incorrectly Set in NERR_NF_FBD
50	X	No Fix	PCI Express* Global Control Register (PEXGCTRL) Access
51			Erratum Removed
52	X	No Fix	Simultaneous AMB Config Accesses Through Multiple Separate Mechanisms may Interfere with Each Other and With Memory Traffic
53	X	No Fix	CRC errors may be logged by the AMB when the MCH is placed in Electrical Idle
54	X	No Fix	Read Transactions may be delayed
55	X	No Fix	PCI express TLP packets not flagged “Malformed” under certain conditions.
56	X	No Fix	Error Source Identification (ID) is not properly reporting the Requestor ID when the uncorrectable (Non-fatal/fatal) error is detected in the PCI express Root Port

Specification Changes

Number	SPECIFICATION CHANGES

Specification Clarifications

Number	SPECIFICATION CLARIFICATIONS
1	Specification Clarification Removed (Included in the referenced documentation)
2	Intel® 7300 Chipset EDS, Intel® 7300 Chipset Memory Controller Hub (MCH) BIOS Setting for the REDIRCTL Register

Documentation Changes

Number	DOCUMENTATION CHANGES

Identification Information

Component Identification via Programming Interface

The Intel® 7300 Chipset Memory Controller Hub (MCH) stepping can be identified by the following register contents:

Stepping	Vendor ID[1]	Device ID[2]	Revision Number[3]
A-1	8086h	3600h	01h

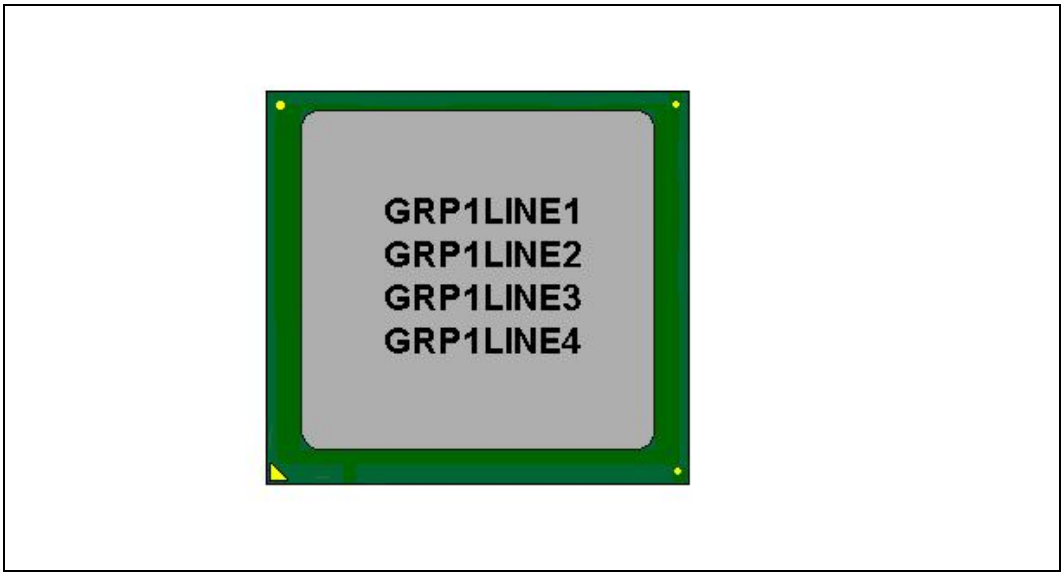
Notes:
1. The Vendor ID corresponds to bits 15:0 of the Vendor ID Register located at offset 00 - 01h in the PCI* function 0 configuration space.
2. The Device ID corresponds to bits 15:0 of the Device ID Register located at offset 02 - 03h in the PCI function 0 configuration space.
3. The Revision Number corresponds to bits 7:0 of the Revision ID Register located at offset 08h in the PCI function 0 configuration space.

Component Marking Information

The Intel® 7300 Chipset Memory Controller Hub (MCH) stepping can be identified by the following component markings:

Stepping	QDF-Spec	Top Marking	Notes
A-1	SLAGJ	QG7300	Production

Figure 1. Top-Side Marking Example



Errata

1. PCI Express* Intel® Interconnect BIST (Intel® IBIST) on x8 Port Will Not Stop Testing of Entire Port if an Error is Detected on Any Lane Other Than Lowest 4 Lanes of the Port

Problem: During PCI Express Intel IBIST “stop on error” testing, if an error is detected on a x4 port then the test will stop for the entire port and the error is logged. Likewise, if an error is detected on the lower 4 lanes of a x8 port, the test will stop for the entire port and the error is logged. If an error is detected on the upper 4 lanes of a x8 port, the error is logged, the test stops running on the upper 4 lanes, but the test will continue on the lower 4 lanes of the port.

Implication: Intel IBIST test will continue running in spite of errors if errors occur anywhere other than lowest 4 lanes of a x8 port.

Workaround: If “stop on error” functionality is desired, changes will have to be made to the Intel IBIST scripts to enable this functionality by polling the global status registers. If an error occurred in only the upper lanes, halt Intel IBIST (if in loop continuous mode) as the Intel IBIST engine for that set of 4 lanes has stopped (if stop on error is enabled). If an error occurred in the lowest 4 lanes, all of the Intel IBIST engines will be forced to stop (exit from Loopback). Check the loop count error status register to determine what set of 4 lanes failed first. One thing to note is that the upper lanes will likely record an error in all lanes whereas the lower 4 may or may not depending on the nature of the real error. Whether the ports are in x4 or x8 mode, the DIO0IBSTAT and DIO0IBERR registers need to be checked to determine which set of 4 lanes had an error and which set of 4 lanes did not.

Status: For the steppings affected, see the *Summary Tables of Changes*.

2. Leakage from 1.5V VCC to 1.2V VTT

Problem: The MCH 1.5V VCC power rail must ramp ahead of the MCH 1.2V VTT power rail. During this power-up sequence, a leakage path exists within the MCH from the 1.5V VCC pins to the 1.2V VTT pins. This leakage path only exists while the MCH is powering up.

Implication: Higher than expected current seen on MCH 1.2V VTT power rail while the 1.5V VCC power rail is ramping. This leakage path does not impact the reliability or functionality of the MCH.

Workaround: Use the power good output of the 1.5V Vreg to enable/start the VTT Vreg. Having the VTT rail ramp up immediately after the 1.5V VCC rail is in regulation will eliminate the potential for leakage.

Status: For the steppings affected, see the *Summary Tables of Changes*.

3. Processor Reset Bit in System Reset Register Fails to Clear

Problem: Processor Reset bit 14 in the System Reset register (D16:F0:Reg 40h), SYRE.CPURST, is not being cleared by the MCH after being set, as expected. Subsequent reads to this register will incorrectly return a 1b. Writing a 1b to this register bit will assert processor reset as intended even in the presence of this errata.

Implication: Data returned from this register will not return intended result. Using data from this register without accommodating this issue may cause unexpected behavior. For instance, if data from this register is used in a read-modify-write to this register, a 1b will be read from this bit and a writeback to that register will cause an unintended CPU reset.

Workaround: BIOS may write 0 to SYRE.CPURST to clear the bit after the CPU comes out of reset.

Status: For the steppings affected, see the *Summary Tables of Changes*.

4. ESI Reset Timeout Error Incorrectly Logged in PEX Error Register

Problem: MCH incorrectly sends a CPU_RESET_DONE message on a processor only reset to Intel® 631xESB/632xESB I/O Controller Hub and waits for a responding CPU_RESET_DONE_ACK message. This transaction is never generated from the Intel® 631xESB/632xESB I/O Controller Hub. ESI Reset Timeout errors are logged in the PCI Express error register.

Implication: An incorrect error will be logged in the MCH error-reporting registers. Software that monitors these error registers may take inappropriate action based on assertion of this error.

Workaround: Prior to issuing a processor only reset, BIOS must mask the ESI Reset Timeout Error by writing a 1b to bit[21] of the Uncorrectable Error Mask Register (UNCERRMSK[0].IO18MSK), (D0:F0:Reg 108h).

Status: For the steppings affected, see the *Summary Tables of Changes*.

5. The NRECADDRH[3:0] Will Log Incorrect Information for Certain FSB Errors

Problem: For FSB error F1 (Request/Address Parity Error) and FSB error F9 (FSB protocol error) the address field in NRECADDRH will contain incorrect information. For the F1 error, this field should contain the requestor address. For the F9 error, this field should contain the response address. The data in these fields is inaccurate.

Implication: For these FSB error classes the data logged in these registers should be ignored.

Workaround: None

Status: For the steppings affected, see the *Summary Tables of Changes*.

6. Packet May be Dropped When Entering PCI Express* Recovery Mode Resulting in Spurious Correctable Error being Logged

Problem: When the Intel® 7300 Chipset Memory Controller Hub (MCH) enters PCI Express Recovery mode, some packets may get dropped because the upstream agent has not yet entered Recovery. This will result in a correctable error being logged.

Implication: A correctable error will be logged. The dropped packet will not affect system operation.

Workaround: None

Status: For the steppings affected, see the *Summary Tables of Changes*.

7. Simultaneous Memory Errors May Result in Incorrect Data being Logged in Error Reporting Registers

Problem: If simultaneous errors occur on two branches and the higher priority error is masked, then the data for the lower priority error log will be inaccurate. Some of the fields from the higher priority error registers will get logged in the error reporting registers, instead of the lower priority error information (FERR and RECMEMx).

Implication: Incorrect error information logged in FERR and RECMEMx registers.

Workaround: None

Status: For the steppings affected, see the *Summary Tables of Changes*.

8. Coalesce Mode Cannot be Used with Max Payload Size of 256B

Problem: When Max Payload Size is set to 256B (PEXDEVCTRL[7:0] registers, Devices 7-0, Function 0, Register 74h, bits 7:5 set to 001), and read completion coalescing is enabled (PEXCTRL[7:0] registers, Devices 7-0, Function 0, Offset 48h, bit 10 set to 1), the system may hang. If MPS of 256B is used, coalescing must be disabled. If coalescing is desired, MPS must be set to 128B.

Implication: A system hang may occur.

Workaround: Set Max Payload Size to 256B (PEXDEVCTRL[7:0] registers, Devices 7-0, Function 0, Offset 74h, bits 7:5 set to 001). Disable coalescing (PEXCTRL[7:0] registers, Devices 7-0, Function 0, Offset 48h, bit 10 set to 0).

If coalescing is desired, use the following settings:

Enable coalescing (PEXCTRL[7:0] registers, Devices 7-0, Function 0, Offset 48h, bit 10 set to 1). Set Max Payload Size to 128B (PEXDEVCTRL[7:0] registers, Devices 7-0, Function 0, Offset 74h, bits 7:5 set to 000).

In all cases, the following coalesce settings should be used:

Set COALESCE_MODE to 00 (PEXCTRL[7:0] registers, Devices 7-0, Function 0, Offset 48h, bits 25:24). Use Max_rdcmp_lmt_EN default setting of 0 (PEXCTRL[7:0] registers, Devices 7-0, Function 0, Offset 48h, bit 12). Use COALESCE_FORCE default setting of 0 (PEXCTRL[7:0] registers, Devices 7-0, Function 0, Offset 48h, bit 11).

Status: For the steppings affected, see the *Summary Tables of Changes*.

9. Erratum Removed

10. Erratum Removed

11. Incorrect Default Settings for Intel® 7300 Chipset Memory Controller Hub (MCH) Queuing Structure

Problem: The default configuration values for the Memory Controller (MC) queuing structure contains incorrect settings. BIOS is required to overwrite the default value to ensure correct operation.

Implication: System may hang and IERR# may be asserted. Intel has seen this issue occur while running IO stress tests.

Workaround: Write 10b to bits[23:22] of the register located at D16:F1:Reg 1F4h.

Status: For the steppings affected, see the *Summary Tables of Changes*.

12. Accesses to IOxAPIC Address Space of Disabled PCI Express* Ports Will Cause System Hang

Problem: The expected behavior of accessing a IOxAPIC address space (FECx_xxxx) for a disabled PCI Express port will result in a Master Abort (MA) transaction. Because of this errata, accesses to IOxAPICs for these address regions may instead result in system hang. This includes the upper x4 port of a x8 PCI Express port. For example, if port 2 and port 3 are being combined for x8 operation, accesses to the IOxAPIC address space of port 3 may experience this errata.

Implication: System will hang for IOxAPIC accesses to disabled ports.

Workaround: BIOS should check whether a port is x4 or x8 using the PXPLWTCTRL (dev0, func0, offset 0xe0). If a port is x8 (ports 2, 4, and 6) then BIOS should avoid accesses to the IOxAPIC ranges to the slave port (ports 3, 5, and 7). BIOS should also check that PXPLWTCTRL.ILNKTRN0 and/or PXPLWTCTRL.ILNKTRN1 are set appropriately.

Status: For the steppings affected, see the *Summary Tables of Changes*.

13. Erratum Removed

14. Erratum Removed

15. Erratum Removed

16. Hard Reset to the Intel® 7300 Chipset Memory Controller Hub (MCH) Via Intel® 631xESB/632xESB I/O Controller Hub Could Result in False Correctable Receiver Errors Being Logged

Problem: A hard reset via writing 0x06 to port 0xCF9 will cause the ESI link on the Intel® 631xESB/632xESB I/O Controller Hub to reset prior to the Intel® 7300 Chipset Memory Controller Hub (MCH) reset. This will result in a false IO12 receiver error to be logged.

Implication: False IO12 receiver errors may be logged. Any software monitoring these correctable errors may be alerted to this error. It is recommended that BIOS clear this error bit when system is reset in this manner.

Workaround: None

Status: For the steppings affected, see the *Summary Tables of Changes*.

17. MCH B1Err Errors Logged Incorrectly

Problem: B1Err logging does not operate correctly. In the event that an internal data manager parity error occurs B1Err may not be logged. In addition, B1Err may get logged if poisoned data is passed to the internal data manager from the FSB and PCI Express* interfaces.

Implication: B1Err error reporting is unreliable.

Workaround: B1Err error logging should be disabled (EMASK_INT D16:F2:Reg CCh[0] = 1). The lack of B1Err error logging does not cause internal data manager errors to go undetected. An internal data manager parity error will be flagged at the destination interface.

Any parity error in the data manager will cause one of the following:

- A data parity error on the FSB if the destination is FSB
- A poisoned data pattern will be written to memory if the destination is system memory
- EP bit will be set on outbound PCI Express* packets if the destination is one of the PCI Express ports

Status: For the steppings affected, see the *Summary Tables of Changes*.

18. Erratum Removed

19. Erratum Removed

20. Spurious B3 Errors (Coherency Violation Error for Explicit Writebacks) May be Logged

Problem: Under normal operation, B3 Errors (Coherency Violation Error for Explicit Writebacks) may be incorrectly logged in FERR_FAT_INT (D16:F2:Reg C0h, Bit [2]) and NERR_FAT_INT (D16:F2:Reg C2h, Bit[2]) registers. No actual error has occurred and the system will continue to operate normally.

Implication: Spurious B3 Errors will be logged.

Workaround: Mask out B3Err by writing 1b to bit [2] (B3MSK bit) of the Internal Error mask register (EMASK_INT), D16:F2:Reg CCh) Note: Masking this bit will prevent real B3 Errors from being logged as well.

Status: For the steppings affected, see the *Summary Tables of Changes*.

21. Erratum Removed

22. Erratum Removed

23. Erratum Removed

24. FB-DIMM I/O Compensation Logic for the Intel® 7300 Chipset Memory Controller Hub (MCH) Does Not Allow for Individual Branch Initialization

Problem: Due to reset logic limitations in both FB-DIMM branches compensation logic, a specific initialization programming order must be followed.

Implication: FB-DIMM compensation may not be configured correctly which may result in functional problems with the FB-DIMM channel.

Workaround: Details of the workaround are outlined below.

If only Branch 0 is populated:

Branch1, FBDRST[1] stays at 0

Dev 21, FBDRST[0]

1. Write 0x0
2. Write 0x5. Wait for minimum of 21 ns
3. Write 0x4. Wait for a minimum of 2 µs
4. Write 0x7

To bring up branch 1, write 0x3 to Dev 22 FBDRST register.

If only Branch 1 is populated:

Write 0x4 to branch 0 FBDRST register

Dev 22, FBDRST

1. Write 0x4
2. Write 0x5. Wait for 21 ns
3. Write 0x4. Wait for 2 µs
4. Write 0x7

To bring up Branch 0 after this, write 0x7 to Dev 22 FBDRST register.

If both branches are populated simultaneously:

1. Write 0x0 to both FBDRST
2. Write 0x5 to Dev 21, FBDRST. Wait for 21 ns
3. Write 0x4 to Dev 21 FBDRST. Wait for 2 µs
4. Write 0x7 to Dev21, FBDRST
5. Write 0x3 to Dev22, FBDRST

Status: No Fix

25. Erratum Removed

26. The Intel® QuickData Technology Integrated DMA Engine May Log Both FERR and NERR for Single Error

Problem: Invalid Intel® QuickData Technology DMA transactions may cause a single error to incorrectly assert both FERR_CHANERR (device 8, function 0, offset 80h) and NERR_CHANERR (device 8, function 0, offset BCh).

Implication: Incorrect error handling of NERR_CHANERR may occur. NERR_CHANERR may be logged in the case of a single error.

Workaround: No workaround. Software that monitors these error registers need to be aware of this limitation and ignore the NERR_CHANERR bit when FERR_CHANERR is logged.

Status: For the steppings affected, see the *Summary Tables of Changes*.

27. Thermal Throttling Update Values Should be Disabled Prior to Link Initialization

Problem: The Intel® 7300 Chipset Memory Controller Hub (MCH) incorrectly allows FBD thermal update activities on an uninitialized link in its default configuration.

Implication: Thermal updates on an uninitialized link can cause Transaction ID (TID) synchronization problems.

Workaround: Write a 1b to bit 3 of the register located at D16:F1:Reg 19Ch, prior to FBD link initialization.

Status: For the steppings affected, see the *Summary Tables of Changes*.

28. Memory Error Incorrectly Logged in Mirrored Mode

Problem: Error logging mechanism for M23 in mirrored mode is not reliable and can cause spurious errors.

Implication: Fatal error can get logged due to fast reset fail on already degraded mirrored branch.

Workaround: (Option 1) Do not signal M23 as an MCERR while in mirroring mode, but through an ERR[2:0] pin. Error handler would then check if we are in degraded mode, and that M23 was in fact caused by the already degraded channel. (Option 2) Mask out M23 while in mirroring mode by writing a 1b to the ERR[2-0]_FBD.M23Err fields (Dev 16, Fcn 1, Off ACh & B0h & B4h). Don't route M23 to the error pins, ERR[2:0].

Status: For the steppings affected, see the *Summary Tables of Changes*.

29. Coherency Engine Errors Logged in NERR not Signaled

Problem: Coherency Engine (CE) interrupt errors logged in NERR are not signaled.

Implication: Some Coherency Engine errors may not signal an MCERR.

Workaround: If one error within a particular FERR group requires MCERR, all other errors in the same group must be promoted to MCERR or masked off. Errors may be configured as follows to allow for proper error signaling:

CE Fatal Errors - Promote to MCERR or mask

- B1 - CNB - Parity error from DM (does not include poisoned data) - promote to MCERR
- B2 - SF illegal state - promote to MCERR
- B3 - Coherency violation-EWB error - promote to MCERR
- B4 - VPP Interface ERROR - Either promote to MCERR or mask this error. If this error is masked, can still poll PEX_UNIT_FERR/NERR to determine whether there was a VPP interface.
- B7 - Multiple bit ECC error on snoop filter lookup - promote to MCERR

CE Non Fatal Errors - no MCERR required

- B5 - CNB Address map error - software programming error, no signal is required, but may use ERR[2:0] depending on platform strategy
- B6 - Single bit ECC error - corrected in hardware, no signal is required, but may use ERR[2:0] depending on platform strategy
- B8 - Coherency Violation BIL error - should be masked for Tigerton and Dunnington processors as they can generate this case legitimately

Status: For the steppings affected, see the *Summary Tables of Changes*.

30. Incorrect Error Reporting for PCI Express* Non-Fatal and Fatal Errors

Problem: PEXCMD.SERRE prevents PEXRTCTRL from masking out assertion of the ERR or MCERR signals.

Implication: If PEXCMD.SERRE is enabled, the Intel® 7300 Chipset Memory Controller Hub (MCH) will always assert the ERR or MCERR signal even if it is turned off in the PCI Express Root Control register, PEXRTCTRL (D [7-0]:F0:Reg 88h).

Workaround: Use PEXRTCTRL register to report and enable system errors.

Status: For the steppings affected, see the *Summary Tables of Changes*.

31. Incorrect Intel® 7300 Chipset Memory Controller Hub (MCH) Default Settings

Problem: The memory controller default configuration value contains incorrect settings.

Implication: Data transactions through the memory controller may be corrupted. The default value for this register must be overwritten to ensure correct operation.

Workaround: BIOS needs to write a 0b to bit 30 of the register located at D16:F1:Reg 1FCh, prior to FBD link initialization.

Status: For the steppings affected, see the *Summary Tables of Changes*.

32. Memory Controller Branch Incorrectly Degrades on Replay Transaction

Problem: Memory controller branch erroneously degrades on initial replay transaction.

Implication: Branch degrades unnecessarily. This may result in degraded RAS capability.

Workaround: BIOS needs to write a 002h to bits[25:16] of the register located at D16:F1: Reg 18Ch. This workaround alleviates this issue.

Status: For the steppings affected, see the *Summary Tables of Changes*.

33. PCI Express* DMA Transactions May Not be Tracked Correctly in the Intel® 7300 Chipset Memory Controller Hub (MCH)

Problem: The Intel® 7300 Chipset Memory Controller Hub (MCH) fails to generate the correct tracking mechanism for a PCI Express DMA transaction.

Implication: PCI Express transactions may be incorrectly tracked and may lead to unpredictable behavior.

Workaround: BIOS needs to write a 1b to bit[28] of the Coherency Control register, COHC, located at D16:F0:Reg F4h.

Status: For the steppings affected, see the *Summary Tables of Changes*.

34. Spurious Errors Logged in Reserved Error Log Register Field

Problem: Spurious errors may be incorrectly logged in a reserved error log register bit.

Implication: Unexpected errors logged in this error logging register bit must be masked off.

Workaround: BIOS needs to write a 1b to bit[23] of the FBD Error Mask registers EMASK_FBD and ERR[2:0]_FBD, located at D16:F1:Reg [A8h, ACh, B0h, B4h].

Status: For the steppings affected, see the *Summary Tables of Changes*.

35. Inbound Flow Control Logic for PCI Express* not Configured Correctly

Problem: The Intel® 7300 Chipset Memory Controller Hub (MCH) default configuration may lead to improper throttling of inbound PCI Express requests.

Implication: Potential overflow condition may occur on inbound PCI Express buffers.

Workaround: BIOS needs to write a 1b to bit[30] of the Coherency Control 2 register, COHC2, located at D16:F0:Reg Off F8h.

Status: For the steppings affected, see the *Summary Tables of Changes*.

36. Memory Queue Depth Incorrectly Sized

Problem: The Intel® 7300 Chipset Memory Controller Hub (MCH) default configuration for the memory queue is set to an incorrect value. BIOS is required to overwrite the default value to ensure correct operation.

Implication: Memory queue overflow condition may occur resulting in error condition.

Workaround: BIOS needs to write 31h to bits[27:22] of the Memory Control Settings A register field, MCA.RQHTH (D16:F1:Reg 58h).

Status: For the steppings affected, see the *Summary Tables of Changes*.

37. Erratum Removed

38. Northbound Lane May Lose Bitlock During TS1 Loopback

Problem: During TS1 loopback, receivers on the FBD northbound lane may lose bitlock.

Implication: The FBD link may go down.

Workaround: Prior to updating the FBD Branch State Control field to an active state by writing 30h to the FBD State Control registers, FBDHPC[1:0], (D[22-21]:F0:Reg 4Fh), the FBD IBIST TX and RX Pattern Generator register values need to be updated. BIOS needs to write 10002420h to FBD[3:0]IBTXPGTL (D[22-21]:F0:Reg [284h, 184h]) and FBD[3:0] IBRXPGTL (Dev [22-21]:F0:Reg [2A0h, 1A0h].

Status: For the steppings affected, see the *Summary Tables of Changes*.

39. S4 or S5 Hang Due to PCI Express* Bus Master Traffic

Problem: Certain devices do not shut down bus master traffic when trying to enter S4 or S5. This steady stream of traffic will prevent the system from transitioning into S4 or S5.

Implication: System will hang.

Workaround: BIOS must intercept S4 or S5 requests, and turn off bus master requests in all root port functions. This workaround needs to be implemented in the SMI handler. (1) Clear BME bit in configuration space of every Intel® 7300 Chipset Memory Controller Hub (MCH) PCI Express port including ESI. (2) Clear BME bit in all Intel® 7300 Chipset Memory Controller Hub (MCH) integrated endpoint functions that support bus mastering (i.e. DMA engines).

Status: For the steppings affected, see the *Summary Tables of Changes*.

40. Incorrect Source ID May Be Logged in the RPERRSID for Root Port Detected Errors

Problem: The ERR_CORR_SID of the RPERRSID register (B0:D[0-7]:F0:Reg 134h, bits [15:0]) typically contains the source ID of the most recently received correctable error for a given port. Due to this errata, however, if the root port is the entity that detects a correctable error, the value logged in ERR_CORR_SID will be incorrect. Specifically, for

ports 0 through 3, a value of 0x0000 will always be logged for root port detected errors, and for ports 4 through 7, a value of 0x0020 will always be logged. This errata only affects root port detected errors. Incoming error messages will have their source ID correctly logged in this register.

Implication: The data logged in the ERR_CORR_SID of the RPERRSID register may not be correct. Software which monitors and decodes error information should not use the data contained in this register.

Workaround: Software should poll each PCI Express* device to determine the source of a reported error.

Status: For the steppings affected, see the *Summary Tables of Changes*.

41. Erratum Removed

42. Erratum Removed

43. Erratum Removed

44. Incorrect Default Configuration Values for the Data Manager and Coherency Engine Threshold Limits

Problem: Default values for select Intel® 7300 Chipset Memory Controller Hub (MCH) Data Manager and Coherency Engine threshold settings are incorrect. This may lead to buffer allocation overflow conditions in the Data Manager and Coherency Engines.

Implication: System may hang with an IERR# assertion. This condition will typically manifest itself during extensive coherency stress tests, including FSB and PCI Express* stress traffic.

Workaround: Change the threshold values to the correct limits for the Intel® 7300 Chipset Memory Controller Hub (MCH) design by updating the following registers:

- Write 1010010b to COHC2 (B0:D16:F0:Reg 0F8h) Bits[8:2]
- Write 00617964h to register at B0:D17:F0:Reg 1e8h Bits[31:0]
- Write 00617964h to register at B0:D17:F3:Reg 1e8h Bits[31:0]

Status: For the steppings affected, see the *Summary Tables of Changes*.

45. The Intel® 7300 Chipset Memory Controller Hub (MCH) Does Not Log Select PEX_NF_FERR/NERR Registers When Severity is Set to Non-Fatal

Problem: The Intel® 7300 Chipset Memory Controller Hub (MCH) will not log Advisory Errors: IO2 (Unsupported Request Error), IO4 (Poison TLP Error), IO7 (Completer Abort), and IO8 (Unexpected Completion Error) in PEX_NF_CORR_FERR[7:1] (D[1-7]:F0:Reg 158h) and PEX_NF_CORR_NERR[7:1] (D[1-7]:F0:Reg 160h).

Implication: Select Advisory errors may not be logged in the chipset.

Workaround: The same errors will still be logged in the PCI*/PCI Express* architected registers: UNCERRSTS[7:1] (D[1-7]:F0:Reg 104h) and SECSTS[7:1] (D[1-7]:F0:Reg 1eh) as expected. These errors can be signaled on ERR#[2:0] pins or MCERR# on FSB based on PEX_ERR_DOCMD[7:1] (D[1-7]:F0:Reg 144h) register setting. BIOS needs to read these standard PCI/PCI Express registers to workaround this issue.

Advisory errors are logged in UNCERRSTS and CORERRSTS (only one bit indicating that advisory error happened) if and only if:

- CORERRMSK[7:1] bit 13 is set to 0, and,
- EMASK_UNCOR_PEX[7:1] is set to 0

Status: For the steppings affected, see the *Summary Tables of Changes*.

46. Insufficient PCI Express* Inbound Flow Control Credits

Problem: PCI Express inbound flow control credits is insufficient.

Implication: System may hang with an IERR and / or MCERR. The failing signature results during heavy address conflict stress testing.

Workaround: For x4 width, set device number [0, 2, 4, 6], function 0, offset 22Ch, bits [19:14] to 2

For x8 width, set device number [0, 2, 4, 6], function 0, offset 22Ch, bits [19:14] to 1

Status: For the steppings affected, see the *Summary Tables of Changes*.

47. Header Logs have Incorrect Data when Logging UR for an Outbound Completion with UR

Problem: The Intel® 7300 Chipset Memory Controller Hub (MCH) sends out the completion for a Peer-to-Peer request in which the Peer-to-Peer device returned an unsupported request (UR). This is logged by the Intel® 7300 Chipset Memory Controller Hub (MCH) as an unsupported request error. However, the header from the original request is long gone at this point and the header logged in the header log is whatever transaction is currently coming into the port at this point.

Implication: An incorrect header data is logged.

Workaround: None

Status: For the steppings affected, see the *Summary Tables of Changes*.

48. Partial Write Combining may cause Logic in the Intel® 7300 Chipset Memory Controller Hub (MCH) to Hang

Problem: Partial write combining may cause logic in the Intel® 7300 Chipset Memory Controller Hub (MCH) to hang.

Implication: System may hang.

Workaround: Set D16:F0:Reg f4h bit 13 to a 1.

Status: For the steppings affected, see the *Summary Tables of Changes*.

49. M13Err, M14Err or M15Err may be Incorrectly Set in NERR_NF_FBD

Problem: The first FBD error is logged in the FERR_NF_FBD (Bus: 0, Device: 16, Function: 1, Offset: A0h) , and all subsequent and lower-priority non-fatal errors are logged in NERR_NF_FBD (Bus: 0, Device: 16, Function: 1, Offset: A4h) . There are cases, however, where a valid first error is logged in the FERR_NF_FBD and a spurious error is logged in the NERR_NF_FBD. The potential spurious NERR_NF_FBD errors vary with the error logged in FBD_NF_FERR.

Error Logged in FERR_NF_FBD	Potential Spurrious Error Logged in NERR_NF_FBD
M13err	M15err
M14err	M15err
M15err	M15err
M15err	M13err, M14err, M15err

Implication: NERR_NF_FBD may have invalid M13Err, M14Err or M15Err errors logged.

Workaround: None

Status: For the steppings affected, see the *Summary Tables of Changes*.

50. PCI Express* Global Control Register (PEXGCTRL) Access

Problem: The PCI Express Global Control Register (D19:F0:Reg 17Ch) can only be accessed via FSB Configuration commands.

Implication: The PCI Express Global Control Register can not be accessed via SMBus or JTAG.

Workaround: None

Status: For the steppings affected, see the *Summary Tables of Changes*.

51. Erratum Removed

52. Simultaneous AMB Config Accesses Through Multiple Separate Mechanisms may Interfere with Each Other and With Memory Traffic

Problem: Buffer management problem inside the Intel® 7300 Chipset Memory Controller Hub (MCH). When CPU initiated AMB config accesses (delivered via FSB) and System SMBus initiated AMB config accesses (delivered via CFGSMB{CLK/DATA}) happen concurrently, and both of these are converted into FBD inband transactions by the Intel® 7300 Chipset Memory Controller Hub (MCH), these may interfere with each other and with concurrent memory traffic.

Implication: The Intel® 7300 Chipset Memory Controller Hub (MCH) BIOS or SW implementation should not convert both of these mechanisms into FBD inband transactions:
a) CPU initiated AMB config access (via FSB)
AND
b) System SMBus initiated AMB config access (via CFGSMB{DATA/CLK}).

Workaround: If AMB config space needs to be accessed by both CPU AND System SMBus, one of these accesses will need to be re-routed to the SPD interface (using the Intel® 7300 Chipset Memory Controller Hub (MCH) as master and AMB as slave). Either the Intel® 7300 Chipset Memory Controller Hub (MCH) BIOS or CPU SW should
a) send all CPU initiated AMB config accesses to the AMB via the SPD interface
OR
b) send all System SMBus initiated AMB config accesses to the AMB via SPD interface.
Only one of these mechanisms can be converted into FBD inband transactions, the other has to be sent to the AMB via the SPD interface.

Status: For the steppings affected, see the *Summary Tables of Changes*.

53. CRC errors may be logged by the AMB when the MCH is placed in Electrical Idle

Problem: The Intel(r) 7300 Chipset MCH does not set IgnoreERR (Ignore command and CRC errors until after the next reset) in the SYNC packet sent to the AMB preceding Electrical Idle (EI) entry.

Implication: System BIOS implementations that optimize S1 power savings by transitioning the MCH FBD channel to Electrical Idle may encounter this issue, implementations that do not put the FBD channel in EI are not affected.

Workaround: BIOS should clear Bit [0] in the following AMB registers after exiting EI. (Function: 1, Offset: 90h and 94h)

Status: For the steppings affected, see the *Summary Tables of Changes*.

54. Read Transactions may be delayed

Problem: Under a certain sequence of read and write transactions issued from processors or bus mastering I/O devices, the read transaction may be delayed.

Implication: A read transaction may be delayed. Intel has not observed this behavior with any commercially available software.

Workaround: None

Status: For the steppings affected, see the *Summary Tables of Changes*.

55. PCI express TLP packets not flagged “Malformed” under certain conditions.

Problem: PCI express Transaction Layer Protocol (TLP) packets that are of exactly 256B in length will not be flagged with Malformed TLP when the Maximum Payload Size (MPS) is set to 128B in the PEXDEVCTRL register. All packet sizes greater than 128B except for exactly 256B are correctly reported as a Malformed TLP in the error reporting registers. This does not affect systems with the MPS set to 256B, in this case all packets greater than 256B are correctly reported as Malformed TLP in the error reporting registers.

Implication: When the MPS is set to 128B, if the PCI express end point incorrectly transmits a packet that is exactly 256B the Intel® 5100 MCH will process the packet and will not report a malformed TLP error. **Note**: There is an errata 8 on MPS setting to 256B, please refer to item 8 for details.

Workaround: None

Status: For the steppings affected, see the *Summary Tables of Changes*.

56. Error Source Identification (ID) is not properly reporting the Requestor ID when the uncorrectable (Non-fatal/fatal) error is detected in the PCI express Root Port

Problem: The event collector for uncorrectable error source ID in the Root Complex of the PCI express ports reported in RPERRSID[7:2,0] register under bits[31:16] ERR_FAT_NOFAT_SID field is not capturing the Requestor ID of the source when a Fatal or Non Fatal error is received by the Root Port.

Implication: The value reported in the RPERRSID[7:2,0][ERR_FAT_NOFAT_SID] does not represent the source of the uncorrectable (Non-fatal/fatal) error detected by the root port.

Workaround: Do not use RPERRSID[7:2,0][ERR_FAT_NOFAT_SID] information when a uncorrectable error is detected by the PCI express Root Port.

Status: For the steppings affected, see the *Summary Tables of Changes*.

Specification Changes

There are no Specification Changes for this revision.

The Specification Changes listed in this section apply to the following documents:

1. Intel® 7300 Chipset Memory Controller Hub (MCH) *Datasheet* (Document Number 318082-001)

All Specification Changes will be incorporated into a future version of the appropriate Intel® 7300 Chipset documentation.

Specification Clarifications

The Specification Clarifications listed in this section apply to the following documents:

1. Intel® 7300 Chipset Memory Controller Hub (MCH) *Datasheet* (Document Number 318082-001)

All Specification Clarifications will be incorporated into a future version of the appropriate Intel® 7300 Chipset documentation.

1. Specification Clarification Removed (Included in the referenced documentation)

2. Intel® 7300 Chipset EDS, Intel® 7300 Chipset Memory Controller Hub (MCH) BIOS Setting for the REDIRCTL Register

The REDIRCTL.CHECK_APICID bit (D16:F0:Reg 6E[15]) controls how the Intel® 7300 Chipset Memory Controller Hub (MCH) processses an xTPR_Update transactions on the processor bus. The default setting for CHECK_APICID is “0”. When CHECK_APIC is “1”, the Intel® 7300 Chipset Memory Controller Hub (MCH) checks the logical APICID (Aa[11:4]) and if the logical APICID field is all zeros it will not update the Cluster Mode bit, if the logical APICID is non-zero the Cluster Mode bit will be updated from an xTPR_Update transaction.

xTPR_Update transactions from disabled cores have an APICID of all zeros and with the default CHECK_APICID setting causes the Intel® 7300 Chipset Memory Controller Hub (MCH) to update the Cluster Mode bit, switching from flat to cluster mode or vice versa., resulting in missed interrupts. Intel’s recommendation for disabled cores is to have the xAPIC software disabled and to have the CHECK_APICID bit in the Intel® 7300 Chipset Memory Controller Hub (MCH) set to “1”.

Documentation Changes

There are no Documentation Changes for this revision.

The Documentation Changes listed in this section apply to the following documents:

1. Intel® 7300 Chipset Memory Controller Hub (MCH) *Datasheet* (Document Number 318082-001)