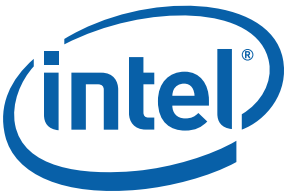

Intel® 3 Series Chipset Family

Specification Update

— For the Intel® 82Q35, 82Q33, 82G33 Graphics and Memory Controller Hub (GMCH) and 82P35 Express Chipset Memory Controller Hub (MCH)

October 2007

Notice: The Intel® 82Q35, 82Q33, 82G33, and 82P35 (G)MCH may contain design defects or errors known as errata which may cause the product to deviate from published specifications. Current characterized errata are available on request.

Order Number: 316967-003

Contents

Revision History

Revision	Description	Date
-001	• Initial Release	June 2007
-002	• Added specifications for the 82Q35 GMCH and 82Q33 GMCH	August 2007
-003	• Added Errata #2 and #3	October 2007

Preface

This document is an update to the specifications contained in the Affected Documents/ Related Documents table below. This document is a compilation of device and documentation errata, specification clarifications and changes. It is intended for hardware system manufacturers and software developers of applications, operating systems, or tools.

Information types defined in Nomenclature are consolidated into the specification update and are no longer published in other documents.

This document may also contain information that was not previously published.

Note: The term (G)MCH refers to the 82Q35 GMCH, 82Q33 GMCH, 82G33 GMCH and 82P35 MCH.

Affected Documents/Related Documents

Title	Number
Intel® 3 Series Chipset Family Datasheet	316966-002

Nomenclature

Errata are design defects or errors. These may cause the (G)MCH's behavior to deviate from published specifications. Hardware and software designed to be used with any given stepping must assume that all errata documented for that stepping are present on all devices.

Specification Changes are modifications to the current published specifications. These changes will be incorporated in any new release of the specification.

Specification Clarifications describe a specification in greater detail or further highlight a specification's impact to a complex design situation. These clarifications will be incorporated in any new release of the specification.

Documentation Changes include typos, errors, or omissions from the current published specifications. These will be incorporated in any new release of the specification.

Note: Errata remain in the specification update throughout the product's lifecycle or until a particular stepping is no longer commercially available. Under these circumstances, errata removed from the specification update are archived and available upon request. Specification changes, specification clarifications and documentation changes are removed from the specification update when the appropriate changes are made to the appropriate product specification or user documentation (datasheets, manuals, etc.).

Summary Tables of Changes

The following tables indicate the errata, specification changes, specification clarifications, or documentation changes which apply to the Product Name product. Intel may fix some of the errata in a future stepping of the component, and account for the other outstanding issues through documentation or specification changes as noted. These tables uses the following notations:

Codes Used in Summary Tables

Stepping

X:	Errata exists in the stepping indicated. Specification Change or Clarification that applies to this stepping.
(No mark) or (Blank box):	This erratum is fixed in listed stepping or specification change does not apply to listed stepping.

Page

(Page):	Page location of item in this document.

Status

Doc:	Document change or update will be implemented.
Plan Fix:	This erratum may be fixed in a future stepping of the product.
Fixed:	This erratum has been previously fixed.
No Fix:	There are no plans to fix this erratum.

Row

Change bar to left of table row indicates this erratum is either new or modified from the previous version of the document.

Errata

No.	Steppings	Status	Errata
	A2		
1	X	No Fix	Graphics Debug Reset
2	X	No Fix	When using Intel® Virtualization Technology for Directed I/O with integrated graphics, the DMA remapping engine caches invalid address translations
3	X	1	Visual Corruption with Integrated Graphics & Intel® Flex Memory Technology Enabled using Microsoft* Vista[1]

NOTES:
1. 82Q35 A2 stepping - No Fix, All other steppings - Fixed

Specification Changes

No.	Specification Changes
	There are no Specificaiton Changes in this revision of the specificaiton update.

Specification Clarifications

No.	Specification Clarifications
	There are no Specificaiton Clarifications in this revision of the specificaiton update.

Documentation Changes

No.	Documentation Changes
	There are no Documentation Changes in this revision of the specificaiton update.

Identification Information

Component Identification via Programming Interface

The Intel® 82Q35, 82Q33, 82G33 and 82P35 (G)MCHs may be identified by the following register contents:

Stepping	Vendor ID	Device ID	Revision ID	Notes
A2	8086h	29B0h	02h	Intel® 82Q35 GMCH
A2	8086h	29C0h	02h	Intel® 82G33, 82P35 (G)MCH
A2	8086h	29D0h	02h	Intel® 82Q33GMCH

Note:

1. Vendor ID corresponds to bits 15:0 of the Vendor ID register located at offset 00-01h in the PCI function 0 configuration space.
2. Device ID corresponds to bits 15:0 of the Device ID register located at offset 02-03h in the PCI function 0 configuration space.
3. Revision Number corresponds to bits 7:0 of the Revision ID register located at offset 08h in the PCI function 0 configuration space.

Component Marking Information

The Intel® 82Q35, 82Q33, 82G33 and 82P35 (G)MCHs may be identified by the following register content

Stepping	Product	S-Spec #	Top Marking	Notes
A2	82Q35 GMCH	SLAEX	LE82Q35	Intel Q35 Express Chipset – Production
A2	82Q33 GMCH	SLAEW	LE82Q33	Intel Q33 Express Chipset – Production
A2	82G33 GMCH	SLA9Q	LE82G33	Intel G33 Express Chipset – Production
A2	82P35 MCH	SLA9R	LE82P35	Intel P35 Express Chipset – Production

Errata

1. Graphics Debug Reset

Problem: If the Graphics Reset Enable (PCI Bus 0 Device 2 Function 0; offset C0h, bit 0) is set and there are new cursor, display, or overlay engine commands, the internal graphics may not be able to complete its reset.

Implication: Since the internal graphics may not be able to be reset, the system may hang or have video corruption.

Workaround: Disable the cursor, display, and overlay engines. Wait 1uS. Issue the graphics reset by setting this bit to 1. The Intel® Graphics Media Accelerator driver implements this workaround.

Status: No Fix

2. When using Intel® Virtualization Technology for Directed I/O with integrated graphics, the DMA remapping engine caches invalid address translations

Problem: When the Intel® Q35 Express Chipset GMCH uses Intel® Virtualization Technology for Directed I/O with integrated graphics and fault processing is disabled by software, the DMA remapping engine may cache invalid guest to host physical address translations for integrated graphics.

Implication: None known. This has only been seen in a synthetic test environment. In normal system operation, software drivers invalidate translation entries when initializing graphics devices.

Workaround: Software (such as a virtual memory manager or operating system) must not turn off fault processing in the integrated graphics DMA remapping engine.

Status: No Fix

3. Visual Corruption with Integrated Graphics and Intel® Flex Memory Technology Enabled using Microsoft* Vista

Problem: Visual corruption is observed with the Intel® 3 Series GMCHs using new Microsoft* Vista paging model when Intel® Flex Memory Technology is enabled in the Dual Channel Asymmetric Configuration.

Implication: When using Microsoft Vista operating system, there may be visual graphics corruption on the display when running 3D applications.

Workaround: Use the latest Intel® Graphics Media Accelerator driver (Revision 15.4.4 or newer).

For the 82Q35 GMCH, system BIOS must disable Intel® Flex Memory Technology in dual channel asymmetric memory configurations when Intel® Virtualization Technology for Directed I/O is enabled. See latest BIOS Specification Update for more details.

Status: No Fix

Specification Changes

There are no Specificaiton Changes in this revision of the specificaiton update.

Specification Clarifications

There are no Specificaiton Clarification in this revision of the specificaiton update.

Documentation Changes

There are no Documentaiton Changes in this revision of the specification update.