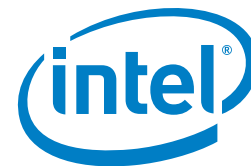


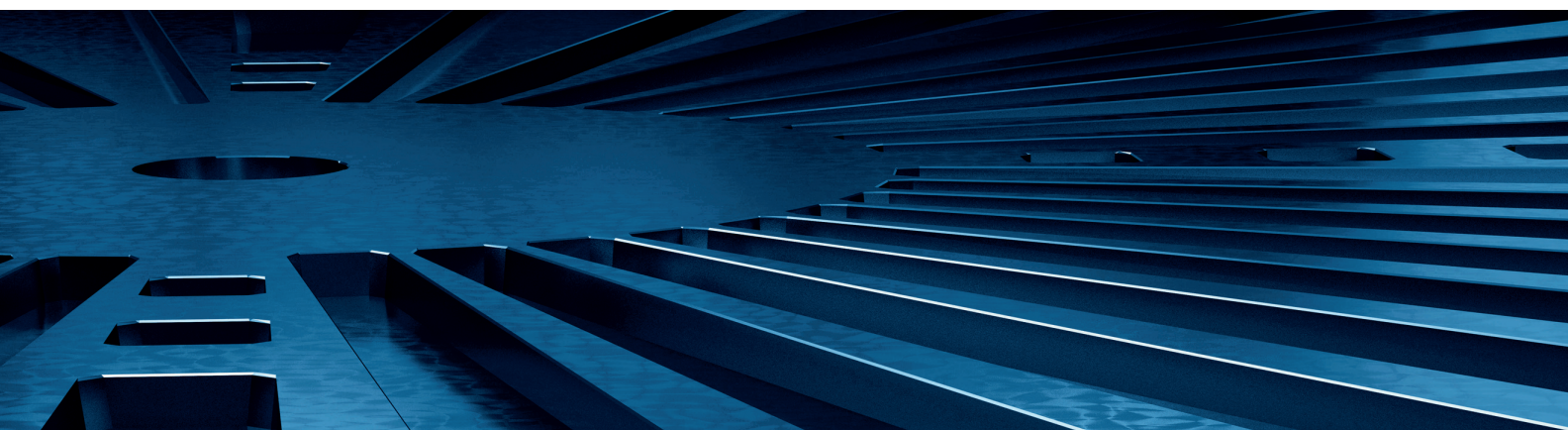
SOLUTION PROFILE

Intel® Xeon® Processor E7 Family
Allegro DVT



Scaling Up Performance for Broadcast-Quality Video

Allegro DVT reaches new heights of video quality, scalability, and power efficiency with encoding algorithms optimized for the Intel® Xeon® processor E7 family.



In the broadcasting business, providers constantly strive to increase the density of channels that can be transcoded on each piece of equipment. Allegro DVT addresses that requirement by constantly tuning its proprietary algorithms for scalability, efficiency, and performance. Allegro DVT's latest achievement is the live H.264/SVC broadcast encoder, AL8000, which is highly optimized for the Intel Xeon processor E7 family.

Solution provided by:



CHALLENGE:

Provide live video encoding software that delivers 1080p HD content and full-HD 3D while saving operators' network bandwidth by avoiding simulcasting of multiple H.264/AVC streams.

SOLUTION:

The Allegro DVT AL8000 live H.264/SVC broadcast encoder takes excellent advantage of the scalable performance and energy efficiency of four-processor servers based on the Intel Xeon processor E7 family. The solution is capable of live-encoding High-Definition (1080p) high-bandwidth 3G-SDI inputs to multiple video H.264/SVC layers.

CUSTOMER BENEFIT:

Using the Allegro DVT solution, broadcasters can encode live-to-live and live-to-file streams, which enables them to provide online and live news streams to public and private TV networks. AL8000 lets operators add the best available HD content (1080p60 and full-HD 3D), and saves operator's network bandwidth by avoiding simulcasting of multiple H.264/AVC streams.

Making a Great Thing Better: Optimization for the Intel® Xeon® Processor E7 Family

As satellite, cable, and telecommunications service providers explore their options for transcoding video streams, they place very high demands on potential solutions, in terms of both quality and cost effectiveness. Allegro DVT strives to exceed their expectations by delivering products that take full advantage of the latest Intel® platforms, including the Intel Xeon processor E7 family.

Because encoding performance is crucial to Allegro DVT's customers, it is also a primary competitive imperative for Allegro DVT. The Intel Xeon processor's innovative microarchitecture, as well as high core count, large cache, and expanded memory addressability help make the Allegro DVT AL8000 live H.264/SVC broadcast encoder a very effective customer solution.

Allegro DVT engineers pursue every advantage to constantly improve encoder performance on the latest hardware, including the Intel Xeon processor E7 family:

- **Four-way server platforms.** The capacity afforded by four-processor platforms is critical to Allegro. To enhance the solution's ability to take advantage of hardware resources, Allegro DVT prioritizes the performance of its multi-threading model, including the use of Intel® Parallel Studio, Intel® Thread Checker, and Intel® Thread Profiler.
- **Performance tools.** Allegro DVT engineers find that Intel® compilers help them generate fast code, the Intel® VTune™ Performance Analyzer is an efficient way to find performance bottlenecks, and Intel® Integrated Performance Primitives are a dependable, simple means of introducing high-performance parallel code.
- **Direct support from Intel.** Working closely with its contacts within Intel, Allegro DVT has found an effective means of staying up to date about upcoming hardware features in future Intel platforms. That early exposure lets it optimize its code to take advantage of new platforms in advance of their public availability.

Together, the ongoing efforts being made by Allegro DVT engineers to enable their encoder for the Intel Xeon processor E7 family are facilitating very high levels of video quality, scalability, and power efficiency. Moreover, the platform's reliability, availability, and serviceability are vital assets in a world where broadcasters must scrupulously avoid server outages.

Engines of Change: The Intel® Xeon® Processor E7 Family

The Intel Xeon processor E7 family extends the limits of scalable performance, reliability, security, and energy efficiency for enterprise servers:

- **Scalable Performance.** Up to 10 cores (20 threads), support for 32-GB DDR3 DIMMs (2 TB per four-socket system),¹ and 30 MB of last-level cache.
- **Reliability and Security.** Intel® Trusted Execution Technology, Double Device Data Correction (DDDC), and Partial Memory Mirroring.
- **Energy Efficiency.** More performance within the same power envelope as predecessors, Intel® Intelligent Power Technology,² and low-voltage DIMM support.³

Learn more about Allegro DVT: www.allegrodvt.com

Learn more about the Intel® Xeon® processor E7 family: www.intel.com/xeon

¹ Up to 64 slots per standard four-socket system x 32 GB/DIMM = 2 TB.

² Uses similar core and package C6 power states enabled on Intel® Xeon® processor 5500 and 5600 series. Requires OS support.

³ Savings dependent on workload and configuration. Example: At 100-percent SPECpower® load it can save ~0.8W for 4-GB DIMM DRx8 based on early Intel internal estimates.

Software and workloads used in performance tests may have been optimized for performance only on Intel microprocessors. Performance tests, such as SYSmark and MobileMark, are measured using specific computer systems, components, software, operations and functions. Any change to any of those factors may cause the results to vary. You should consult other information and performance tests to assist you in fully evaluating your contemplated purchases, including the performance of that product when combined with other products.

Intel® compilers, associated libraries, and associated development tools may include or utilize options that optimize for instruction sets that are available in both Intel® and non-Intel microprocessors (for example SIMD instruction sets) but do not optimize equally for non-Intel microprocessors. In addition, certain compiler options for Intel compilers, including some that are not specific to Intel® microarchitecture, are reserved for Intel microprocessors. For a detailed description of Intel compiler options, including the instruction sets and specific microprocessors they implicate, please refer to the "Intel® Compiler User and Reference Guides" under "Compiler Options." Many library routines that are part of Intel® compiler products are more highly optimized for Intel microprocessors than for other microprocessors. While the compilers and libraries in Intel compiler products offer optimizations for both Intel and Intel-compatible microprocessors, depending on the options you select, your code, and other factors, you likely will get extra performance on Intel microprocessors.

Intel compilers, associated libraries, and associated development tools may or may not optimize to the same degree for non-Intel microprocessors for optimizations that are not unique to Intel microprocessors. These optimizations include Intel® Streaming SIMD Extensions 2 (Intel® SSE2), Intel® Streaming SIMD Extensions 3 (Intel® SSE3), and Intel® Supplemental Streaming SIMD Extensions 3 (Intel® SSSE3) instruction sets and other optimizations. Intel does not guarantee the availability, functionality, or effectiveness of any optimization on microprocessors not manufactured by Intel. Microprocessor-dependent optimizations in this product are intended for use with Intel microprocessors.

While Intel believes our compilers and libraries are excellent choices to assist in obtaining the best performance on Intel and non-Intel microprocessors, Intel recommends that you evaluate other compilers and libraries to determine which best meet your requirements. We hope to win your business by striving to offer the best performance of any compiler or library; please let us know if you find we do not. Notice revision #20101101

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