82578 Layout Checklist (Version 2.2)

Project Name	
Fab Revision	
Date	
Designer	
Intel Contact	

SECTION	CHECK ITEMS	REMARKS	DONE	COMMENTS
	Completed by:	Design Engineer Name:		
General	Obtain the most recent documentation and specification updates.	Documents are subject to frequent change.		
	Route the transmit and receive differential traces before routing the digital traces.	Layout of differential traces is critical.		
	IMPORTANT: Recommend that all signals are routed in reference to a solid plane. If signals cross planes, stitching caps are required between the planes within 40 mils of the signal.			
	If the differential signals transition from a ground referenced layer to a power referenced layer, place a decoupling capacitor on the power and ground within 40 mils of the signal vias.			

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General	Obtain the most recent stack-up information from your Printed Circuit Board (PCB) vendor.			
	Refer to the *Intel® 5 Series Family PDGs* for detailed routing requirements.			
Placement of the 82578	Place the 82578 at least one inch from the edge of the board.	With closer spacing, fields can follow the surface of the magnetics module or wrap past edge of the board. As a result, EMI might increase.		
	Place the 82578 at least one inch from the magnetics module but less than four inches.	Keep trace length under four inches from the 82578 through the magnetics to the RJ-45 connector. Signal attenuation can cause problems for traces longer than four inches. However, due to near field EMI and common mode noise, the 82578 should be placed at least one inch away from the magnetics module.		
	Place the RBIAS compensation resistor less than one inch from the silicon.			
Clock Source (Crystal Option)	Place crystal within 0.75 inches of the 82578.	This reduces EMI.		
	Place the crystal load capacitors within 0.09 inches of the crystal.			

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Clock Source (Crystal Option)	Keep clock lines away from other digital traces (especially reset signals), I/O ports, board edge, transformers and differential pairs.	This helps reduce EMI. Do not route the crystal traces as differential pairs.		
Clock Source (Oscillator Option)	Make sure that the oscillator has it's own local power supply decoupling capacitors. Make sure the decoupling capacitors are within 0.25 inches of the oscillator.	Helps oscillator stability.		
	If the oscillator is shared or is more than two inches away from the 82578, a back-termination resistor should be placed near the oscillator. Note that it is better to not share this clock source. If it is shared keep the traces for the two clock lines matched in length.	This enables tuning to ensure that reflections do not distort the clock waveform. Matching shared clock lines keeps the reflections from one spur of the clock from affecting the other.		
	Keep clock lines at least five times the dielectric thickness away from other digital traces (especially reset signals), I/O ports, board edge, transformers and differential pairs.	Helps reduce EMI.		

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Clock Source (Oscillator Option)	Use a 50 Ω transmission line for the trace between the oscillator and the 82578.	This is a single-ended transmission line. Make sure the transmission line does not cross any plane cuts. Also use stitching capacitors as needed when transferring from one reference plane to another.		
	If the oscillator is powered through a ferrite bead, make sure that the local decoupling capacitor is connected close to oscillator package power input pin. Use a pore for the isolated power input.	A local power well provides a way to isolate system noise from the main time base of the Ethernet. This improves jitter and Bit Error Rate (BER) results.		
General Power Supply Guidance	Use planes to deliver 3.3 Vdc, 2.5 Vdc, and 1.2 Vdc.	Narrow finger-like planes and very wide traces are allowed. If traces are used, 100 mils is the minimum.		

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General Power Supply Guidance	Place decoupling and bulk capacitors close to 82578, with some along every side, using short, wide traces and large vias. Place these to minimize the inductance from each power pin to the nearest decoupling capacitor. The 3.3 Vdc, 1.2 Vdc, and 2.5 Vdc rails should have decoupler capacitors placed near the 82578. The 1.8 Vdc rail should have 1 µF of capacitance placed at the center tap of the transformer.	If power is distributed on traces, bulk capacitors should be used at both ends. If power is distributed on cards, bulk capacitors should be used at the connector.		
1.2 Vdc Power	When using the internal regulator control circuit of the 82578 with an external PNP transistor, keep the trace length from the CTRL1P2 output ball to the transistor very short (less one inch) and use 15 mil (minimum) wide trace.	A low inductive loop should be kept from the regulator control pin, through the PNP transistor, and back to the 82578 from the transistor's collector output. The power pins should connect to the collector of the transistor through a power plane to reduce the inductive path. This reduces oscillation and ripple in the power supply.		
	The 1.2 Vdc regulating circuit requires 1/2 inch x 1/2 inch thermal relief pads for each PNP.	The pads should be placed on the top layer, under the PNP. Refer to BCP69 vendor documentation for additional guidance.		

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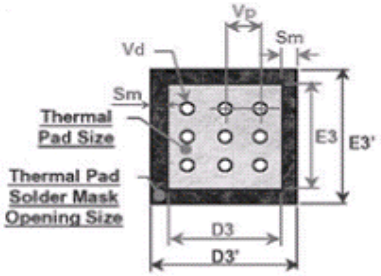
Epad	Use appropriate number of vias to connect Epad to ground.	Refer to the *Intel® 5 Series Family PDG* for additional details. Note that the Epad connection is the only source for ground and is used for both electrical and thermal.  Thermal pad size = D3 * E3 = D2 * E2. Solder mask opening size = D3' * E3' = (D3+2*Sm)*(E3+2*Sm) =(D2+0.1)*E2+0.1) where Sm = 0.05 mm (machine capability) D2.E2 are exposed die attach pad size Thermal via diameter Vd (circled hole) Vd = 0.3~0.33 mm (general drilling machine capability) where thermal via is a Plated Through Hole (PTH) and plugged in solder mask from top-side of PCB. The thermal via pitch Vp Vp = 1.0~1.25 mm		
PCIe-Based Interface	Place the AC coupling capacitors on the PCI-based Tx traces as close as possible to the 82578 but not further than 250 mils (PCIe 1.0 requirement).	Size 0402, X7R is recommended. The AC coupling capacitors should be placed near the transmitter for the PCIe-based interface.		

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PCIe-Based Interface	Make sure the trace impedance for the PCIe-based differential pairs is 85 Ω +/- 15%.	Simulation shows 85 Ω differential trace impedances meets Intel's PCIe-based minimum receive eye requirements when using the Customer Reference Board (CRB) design stack up. When using the CRB design stack up, Intel recommends that board designers use a 85 Ω differential trace impedance for PCIe-based I/O with the expectation that the center of the impedance is always targeted at 85 Ω. The ±15% tolerance is provided to allow for board manufacturing process variations and not lower target impedances.		
	Match trace lengths within each PCIe-based pair on a segment-by-segment basis. Match trace lengths within a pair to five mils.	A PCIe segment is defined as any trace within the same layer. For example, transitioning from one layer to another through a via is considered as two separate PCIe segments. The differential pairs within each segment needs to be matched to 5 mils. Refer to the Intel® 5 Series Family PDGs for additional placement and routing requirements.		

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PCIe-Based Interface	Use a minimum of 15 mil (0.381 mm) pair-to-pair spacing for board designs that use approximately 3 mil dielectric thickness in the design stack up.	Pair-to-pair spacing is five times the thickness of the material.		
	Make sure the PCIe clock differential pair is routed using 100 Ω characteristic impedance. Keep a spacing of three times the dielectric thickness between the PCIe clock and any other traces (digital, analog, and power).			
	If any of the PCIe signals cross a plane or transfers from one plane to another, add stitching capacitors to provide a return path for the common mode currents.	This reduces EMI.		
SMBus	Connect the SMBus using little or no stubs at the pull-up resistor.			
MDI Interface	Design traces for 100 Ω differential impedance (± 15%). Refer to the *Intel® 5 Series Family PDG* for spacing guidance between any signal and the MDI channels.	Primary requirement for 10/100/1000 Mb/s Ethernet. Paired 50 Ω traces do not make 100 Ω differential. An impedance calculator can be used to verify this.		

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MDI Interface	Design traces for 100 W differential impedance (± 15%). Refer to the Intelâ 5 Series Family PDG for spacing guidance between any signal and the MDI channels.	Please use the 82578 Trace Length Calculator available from Intel. Trace width and separation of the MDI pairs is determined by the board stack up in order to achieve the correct impedance. For applications that require a longer MDI trace lengths, Intel recommends that thicker dielectric or lower Er materials be used. This permits higher differential trace impedance and wider, lower loss traces.		
		Target differential impedance is 100 Ω +/- 15%. If a stack up does not allow for 100 Ω +/- 15% differential trace impedance, consider trying a stack up that allows 95 Ω +/- 10%.		
		Stripline is NOT recommended due to thinner more resistive signal layers.		
	Maximum MDI trace length is four inches.	For applications that require a longer MDI trace length of more than four inches, Intel recommends that thicker dielectric or lower Er materials be used. This permits higher differential trace impedance and wider, lower loss traces.		
	Place the MDI termination within 250 mils of the 82578. Keep the trace stub lengths to a minimum. Make sure that the matching or the pair lengths is maintained.			

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MDI Interface	Do not make 90° bends.	Bevel corners with turns based on 45° angles.		
	Minimize through holes (vias).	If using through holes (vias), the budget is two 10 mil finished hole size vias per trace.		
	Keep traces close together inside a differential pair.			
	Pair-to-pair trace length does not have to be matched as differences are not critical.	The difference between the length of longest pair and the length of the shortest pair should be kept below two inches.		
	Keep differential pairs more than seven times the dielectric thickness away from each other and other traces, including NVM traces and parallel digital traces.	This minimizes crosstalk and noise injection. Tighter spacing is allowed for the first 200 mils of trace near of the components.		
	Ensure that the MDI traces (including Bob Smith termination) between the magnetics and the RJ-45 connector are at least 80 mils from all other traces.	This is to ensure the system can survive a high voltage on the MDI cable. (Hi-POT) Refer to the *Intel® 5 Series Family PDGs* for routing and placement guidelines.		
	Keep traces at least 0.1 inches away from the board edge.	This reduces EMI.		
	Do not have stubs along the traces.	Stubs cause discontinuities.		

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MDI Interface	Route traces on appropriate layers.	Run pairs on outer layers to improve routing. Make sure the adjacent layer is a ground layer. There must be no splits in the GND planes under the MDI channel. When differential signals transition from one board layer to another, place ground vias within 40 mils of the signal vias. Avoid broadside coupling to traces on other layers. The broadside effect significantly increases the insertion loss and reduce signal quality. Make sure digital signals on adjacent layers cross at 90° angles. **Note:** Refer to the general section of the layout checklist for guidance on routing signals over reference planes.		
	Total trace resistance from the 82578 to the LAN magnetics should not exceed 10 Ω.	The trace resistance includes the series resistance of any components that might be present such as inductors or resistors.		

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Chassis Ground	Consider using a separate chassis ground for the LAN connector.	If using a discrete magnetics module, provide a separate chassis ground "island" to ground the shroud of the RJ-45 connector and to terminate the line side of the magnetics module. This design improves EMI behavior. Split in ground plane should be at least 50 mils wide. Split should run under center of magnetics module. Differential pairs never cross the split. If using an integrated magnetics module without USB, provide a separate chassis ground "island" to ground around the RJ-45 connector. Split in ground plane should be at least 50 mils wide. If using an integrated magnetics module with USB, do not use a separate chassis ground. Refer to the *Intel® 5 Series Family PDGs* for more details.		
Magnetics Module	Capacitors connected to center taps should be placed very close (less than 0.1 inch recommended) to the integrated magnetics module. Connect a 1 µF capacitor near the magnetics module (1/4 inch).	This improves BER. Note that the 0.1 µF capacitors are only needed for discrete magnetics that don't have them integrated internally.		

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Magnetics Module	The system side center tap on the transformer should be connected to the VCT power supply through a 100 mil trace or a power plane pore.	The center tap voltage is critical to performance of MDI interface. Any voltage drop can cause violations to the specification. Assure that adequate trace width is provided and that the feed is low inductance and low resistance. Refer to the VCT copper loss calculator to determine VCT trace geometry. Contact your Intel representative for access.		
	Place the magnetics module (closer to RJ-45) between the 82578 and the RJ-45.	Applies to designs using discrete magnetics modules only.		
LED Circuits	Keep LED traces away from sources of noise, for example, high speed digital traces running in parallel.	LED traces can carry noise into integrated magnetics modules, RJ-45 connectors, or out to the edge of the board, increasing EMI.		
	If using decoupling capacitors on LED lines, place them carefully.	Capacitors on LED lines should be placed near the LEDs (typically adjacent to integrated magnetics module).		

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82578 Schematic Checklist (Version 2.2)

Project Name	
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Reviewer	

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	Completed by:	Design Engineer Name:		
General	Obtain the most recent documentation and specification updates.	Documents are subject to frequent change.		
	Use this checklist in conjunction with the Customer Reference Board (CRB) reference schematics.			
	Observe instructions for special pins needing pull-up or pull-down resistors.			
	Refer to the *Intel® 5 Series Family Platform Design Guide (PDG)*, the *Intel® 5 Series Express Chipset EDS*, and the Specification Update for integrated GbE LAN (MAC) details.			
Support Pins	Connect TEST_EN (pin 30) through a 1 KΩ pull-down resistor.			

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Support Pins	Connect LAN_DISABLE_N (pin 3) to a 10 KΩ pull-up resistor to 3.3 Vdc and a 10 KΩ no-stuff pull-down resistor to ground. Connect to Intel® 5 Series Express Chipset LAN_PHY_PWR_CTRL (pin AU34) through a 0 Ω resistor.			
	Connect RBIAS (pin 12) to a 2.37 KΩ 1% pull-down resistor.			
	Connect RSVD_VCC3P3 (pin 1) and RSVD_VCC3P3 (pin 2) to a 2.37 KΩ 5% pull-up resistors to 3.3 Vdc.	A value of 3.01 KΩ is suggested. A range of 2.37 KΩ to 10 KΩ can also be used.		
	Connect the Epad (pin 49) to ground plane.	Refer to *Intel® 5 Series Family PDG* for more information.		
PCIe Interface	Connect PCIe interface pins to corresponding pins on the Intel® 5 Series Express Chipset.	Recommend that the default connection be lane six of the Intel® 5 Series Express Chipset. However, the PCIe interface pins can be connected to any available PCIe port.		
	Connect PETn (pin 39) and PETp (pin 38) to Intel® 5 Series Express Chipset PERn6 (pin D8) and PERp6 (pin C9), respectively.			
	Connect PERn (pin 42) and PERp (pin 41) to Intel® 5 Series Express Chipset PETn6 (pin G11) and PETp6 (pin H11), respectively.			

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PCIe Interface	Place AC coupling capacitors (0.1 µF) near the PCIe transmitter (PCIe 1.0 requirement).	Size 0402, X7R is recommended.		
	Connect PE_CLKn (pin 45) and PE_CLKp (pin 44) to Intel® 5 Series Express Chipset CLKOUT_PCIE5N (pin Y8) and CLKOUT_PCIE5P (pin Y9), respectively.	The PCIe clock buffer can be connected to any clock port. It does not have to be port 5. This connection should match the CLK_REQ_N port number.		
	Connect CLK_REQ_N (pin 48) through a 10 KΩ pull-up resistor to 3.3 Vdc and then through a series 0 Ω resistor to Intelâ 5 Series Express Chipset PCIECLKRQ5# (pin AW38).	CLK_REQ_N can be connected to one of the eight Intelâ 5 Series Express Chipset inputs (PCIECLKRQ[7:0]#). This connection should match the PCIe clock output port number. If connecting this PHY output to the PCIECLKRQ1# or PCIECLKRQ2# pins (powered by the core well), the pull-up resistor needs to be connected to the +V3.3S rail. If connecting to any of the other PCIECLKRQ# pins (powered by Sus well), the pull-up resistor needs to be connected to the +V3.3A rail.		

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PCIe Interface	Connect CLK_REQ_N (pin 48) through a 10 KΩ pull-up resistor to 3.3 Vdc and then through a series 0 Ω resistor to Intel® 5 Series Express Chipset PCIECLKRQ5# (pin AW38).	When the PHY is powered down, connecting to the +V3.3A rail results in a small amount of current leakage (~300 µA) through the PHY CLK_REQ_N buffer. This results in a small residual voltage (~0.6 Vdc) on the PHY +V3.3 power rail. The power impact is less than 1 mW and does not affect PHY functionality or reliability. Designers can avoid this leakage by connecting the PHY CLK_REQ_N output to the PCIECLKREQ#1 or PCIECLKREQ#2 pins or by adding a blocking FET. **Note:** Additional guidance is available in the *Intel® 5 Series Family PDGs*.		
	Connect PE_RST_N (pin 36) through a series 0 Ω resistor to Intel® 5 Series Express Chipset PLTRST# (pin AV34).			
SMBus	Connect pull-up resistors to SMB_CLK (pin 28) and SMB_DATA (pin 31).	Use 2.2 KΩ 5% pull-up resistors. Ensure pull-ups are connected to the power rail that is present while in Sx states and while transitioning from G3 to S5. Note that the PHY SMBus address is 0xC8 and default MAC SMBus address is 0xE0.		

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SMBus	Connect SMB_CLK (pin28) and SMB_DATA (pin31) to Intel® 5 Series Express Chipset SML0CLK (pin AW33) and SML0DATA (pin AT34), respectively.	The Intel® 5 Series Express Chipset has a dedicated SMBus for the PHY (SMBus channel 0). No other device (such as an external BMC) can be connected to SML0CLK or SML0DATA.		
Clock Source (Crystal Option)	Use a 25 MHz 30 ppm accuracy @ 25 °C crystal. Avoid components that introduce jitter.	Parallel resonant crystals are required. The calibration load should be 18 pF. Specify Equivalent Series Resistance (ESR) to be 50 Ω or less. Avoid PLL clock buffers.		
	Connect two load capacitors to the crystal; one on XTAL_OUT (pin 9) and one on XTAL_IN (pin 10). Use 27 pF capacitors as a starting point, but be prepared to change the value based on testing.	Capacitance affects accuracy of the frequency and must be matched to crystal specifications, including estimated trace capacitance in calculation. Use capacitors with low ESR (types C0G or NPO, for example). Refer to the Datasheet and the Intel Ethernet Controllers Timing Device Selection Guide for more information.		
	Connect XTAL_IN (pin 10) and XTAL_OUT (pin 9) to the appropriate crystal pins.			

SECTION	CHECK ITEMS	REMARKS	DONE	COMMENTS
Clock Source (Oscillator Option)	Connect the output of the clock oscillator to pin XTAL_IN (pin 10) through appropriate signal conditioning (capacitance-coupled voltage divider). Do not connect XTAL_OUT (pin 9).	Use a 25 MHz 50 ppm oscillator. The oscillator needs to maintain 50 ppm under all applicable temperature and voltage conditions. Avoid PLL clock buffers. Place voltage divider near the XTAL_IN of the PHY (less than 325 mils).		
	Use a local decoupling capacitor on the oscillator power supply. Include a bulk 1 µf capacitor as well as a high frequency 0.1 µf decoupling capacitor.	If isolated with a ferrite bead, include a bulk decoupling capacitor next to the oscillator. Refer to the *Intel® 5 Series Family PDG* for more details.		
	The signal from the oscillator must be AC coupled into the 82578.	The 82578 has internal circuitry to set the input common mode voltage.		
	The amplitude of the clock signal going into the 82578 should be within the maximum input clock amplitude specification for the 82578.	The clock oscillator has an internal voltage regulator to isolate it from the external noise of other circuits to minimize jitter. For example, if a 3.3 Vdc oscillator is used, it's output signal should be attenuated to a maximum value with a resistive divider circuit. Refer to the *Intel® 5 Series Family PDGs* for more details.		
	If the oscillator driver is further away than two inches then add a 33 Ω series resistor directly at the output.			

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3.3 and 1.2 Vdc Power	Provide a 3.3 Vdc supply. Use the power rail that is present while in Sx states and while transitioning from G3 to S5.	This is necessary to support wake up from power down states.		
	Connect a 4.99 KΩ resistor from CTRL1P2 (pin 7) to the LAN 3.3 Vdc supply and BCP69/SOT.	Place decoupling and bulk capacitors close to the 82578, using short, wide traces and large vias. If power is distributed on traces, bulk capacitors should be used at both ends. If power is distributed on cards, bulk capacitors should be used at the connector. Refer to the CRB reference schematics for quantity and placement.		
	Connect a 0 Ω 0805 resistor between the BCP69/SOT emitter and the 3.3 Vdc supply.			
	Place a 0 Ω resistor in series with the BCP69 collector and the V_1P2_LAN supply. The resistor is used to measure the power delivered to the V_1P2_LAN supply.			

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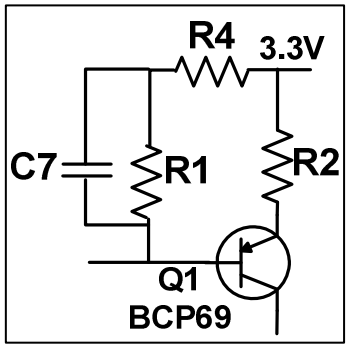
3.3 and 1.2 Vdc Power	Leave empty sites for R1 (4.99 KΩ), R4 (0 Ω), and C7 (0.01 µF), as shown. Refer to the CRB reference schematics for more BCP69 connection details. **Note:** Specific CRBs might have different designations for R1, R4, and C7. The designations shown are for reference only. Place decoupling and bulk capacitors close to the 82578, using short, wide traces and large vias. If power is distributed on traces, bulk capacitors should be used at both ends. If power is distributed on cards, bulk capacitors should be used at the connector.			
2.5 Vdc Power	This is an internal power rail and should not be connected any components except for a 1 µF decoupling capacitor.			
Magnetics	Qualify magnetic modules carefully for return loss, insertion loss, open circuit inductance, common mode rejection, and crosstalk isolation.	Magnetics module is critical to passing IEEE PHY conformance tests and EMI test. Refer to the 82578 Datasheet for magnetics requirements.		

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Magnetics	Supply VCT (Pin 6) to the transformer center taps and use 0.1 µF bypass capacitors. Connect to ground through a 1 µF bulk decoupling capacitor placed near the magnetics center tap input to the transformer.	Ceramic capacitors with low ESR should be used. **Note:** Some magjacks have local decoupling (0.1 µF) integrated into the part.		
	Bob Smith termination: If the RJ-45 connector does not have integrated Bob Smith termination, use 4 x 75 Ω resistors for cable-side center taps and unused pins. Use a high-voltage isolation capacitor attached to the termination plane. A suggested value is 1500 pF/3 KV.	Terminate pair-to-pair common mode impedance of the CAT5 cable. If the discrete magnetics already has Bob Smith termination, then there is no need to add. **Note:** Some magjacks have Bob Smith termination integrated into the part. Name the common connection between the 75 Ω resistors and high-voltage isolation capacitor so it can be used as a reference plane.		
VCT	Supply VCT (Pin 6) to the transformer center taps through a 0 Ω 0805 resistor.	Place the 0805 resistor as close as possible to the 82578.		
MDI Termination	External MDI termination BOM devices MUST be installed. Use 49.9 Ω, 1% resistors and 0.1 µF capacitors.	MDI channel connections cannot be swapped. Eight resistors and four capacitors are used for MDI termination.		

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Chassis Ground (10/100/1000Base-T interface)	If possible, provide a separate chassis ground to connect the shroud of the RJ-45 connector and to terminate the line side of the magnetic module.	This design improves EMI behavior. Also, if using integrated magnetics with USB, do not isolate ground for RJ45.		
	Place pads for approximately 4-6 "stitching" capacitors to bridge the gap from chassis ground to signal ground.	Typical values range from 0.1 µF to 4.7 µF. The correct value should be determined experimentally.		
Decoupling	Use decoupling capacitors generously. The minimum acceptable decoupling by the power supply is identified in the remarks field (not including decoupling at magnetic):	Place near 3.3 Vdc LAN pin: one 10 µF and one 0.1 µF capacitor.		
		Place near BCP69 emitter: two 4.7 µF capacitors.		
		Place near BCP69 collector: one 10 µF and one 0.1 µF capacitor.		
		Place near magnetics center tap input: one 1 µF capacitor. Leave an empty site for another 1 µF capacitor near the VCT pin 6.		
		Place near VDD2P5_OUT, AVDD2P5, and DVDD2P5 pins: one 1 µF capacitor.		

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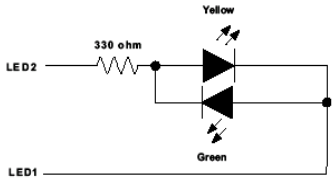
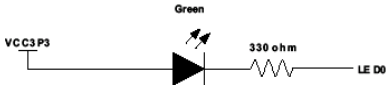
LED Circuits	Basic recommendation is a single green LED for Activity and a dual (bi-color) LED for Speed. Many other configurations are possible. LEDs are configurable through the NVM.	Two LED configuration is compatible with integrated magnetic modules. For the Link/Activity (green) LED, connect the cathode to the LED0 pin and the anode to VCC. For the bi-color speed LED pair, have the LED2 signal drive one end. The other end should be connected to LED1. When LED2 is low, the 100 Mb/s (green) LED is lit. When LED1 is low the 1000 Mb/s (yellow) LED is lit.  		
	Connect LEDs to 3.3 Vdc as indicated in reference schematics.	Use the power rail for designs supporting wake-up (present in Sx states and G3 to S5 transition). Consider adding one or two filtering capacitors per LED for extremely noisy situations. Suggested starting value is 470 pF.		

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LED Circuits	Add current limiting resistors to LED paths.	Typical current limiting resistors are 250 Ω to 330 Ω when using a 3.3 Vdc supply. Current limiting resistors are typically included with integrated magnetic modules.		
Miscellaneous	Intel® 5 Series Express Chipset output SLP_LAN# (pin BA35) can be used to gate power rails that do not need to be on when host WoL and manageability hardware are disabled.	Specific configurations that leave power on/off depending on WoL and manageability hardware settings are design dependent. Refer to the *Intel® 5 Series Express Chipset EDS* for more details. SLP_LAN# replaces the glue logic in previous designs that was an OR FUNCTION between WOL_EN and SLP_M#. For Intel® 5 Series Family, this glue logic is not required. Design a circuit in such a way that when SLP_LAN# is low, cut power to the PHY. When SLP_LAN# is high, PHY power is on.		
	Leave an empty site for a 10 KΩ pull-up resistor at the SLP_LAN# output of the Intel® 5 Series Express Chipset.	The empty pull-up resistor enables G3->S5 WoL to work if the SLP_LAN# signal was not driven by the Intel® 5 Series Express Chipset after a G3->S5 transition. (SLP_LAN# is expected to be driven by the Intel® 5 Series Express Chipset after a G3->S5 transition).		

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Miscellaneous	Place a TVS device between the RJ-45 and the magnetics assembly.	TVS diodes can be added to the MDI for additional ESD protection. If using an integrated magnetics and RJ45 connector, verify that it contains a TVS diode.		
	Intel® 5 Series Express Chipset LAN_RST# (pin AY31) timing requirement needs to be met.	Refer to the *Intel® 5 Series Express Chipset EDS* for more details on LAN_RST# timing requirements.		
Mfg Test	The 82578 allows a JTAG Test Access Port.	The 82578 does not support BSDL. The 82578 supports XOR for manufacturing line tests.		
	Add empty 10 KΩ pull-up resistors for JTAG_TCK (pin 35) and JTAG_TMS (pin 33).	The JTAG pins can be pulled up to 3.3 Vdc supply.		
	Route JTAG to test points.			

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