# MAC-PHY Interface Connector for the PCI Express™ Architecture

**Version 0.9**
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**PIPE Connector 0_9.doc**

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# 1 Preface

## *1.1 Scope of this Revision*

Version 0.9 of the PCI Express MAC-PHY Interface Connector Specification has connector, pin-out and placement definitions.

## *1.2 Revision History*

| Revision Number | Date | Description |
|---|---|---|
| 0.3 | 8/8/05 | Initial Draft |
| 0.5 | 8/12/05 | Added MAC and PHY connector placement graphics, added contributor names (partial list) |
| 0.7 | 8/18/05 | Updated mac and phy placement figures. Updated pin-out with 8_04_05 data. Added QSE footprint. |
| 0.71 | 8/19/05 | Added pin1 designations to mac and phy figures. Updated contributor list. Cleaned up formatting/spacing. Added comments on connector placement/positioning markings. Added notes to pin list. |
| 0.9 | 8/20/05 | Draft for Industry review |

 

# 2 Introduction

The **P**HY **I**nterface for the **P**CI **E**xpress Architecture (**PIPE)** has a strong need for compatibility testing. An important enabling element for compatibility testing is to define a standardized connector to use between **PIPE** MAC and PHY test boards. Along with the connector, a mechanical interface specification is required to allow interoperation.

The **P**HY **I**nterface for the **P**CI **E**xpress Architecture **C**onnector (**PIPE_C**) specification is intended to facilitate the development, integration and testing of functionally equivalent **PIPE** interfaces. The specification defines a connector, connector pin-out and form factor/layout that must be implemented to achieve a **PIPE_C** specification compliant MAC or PHY development/prototype board. This specification addresses implementations for X1 up to X4 widths.

The intent of the **PIPE_C** specification is to reduce development costs and time for **PIPE** MAC and PHY implementations by defining a standard connector interface for prototyping and interoperability testing. This document defines a PIPE connector interface to which MAC and PHY vendors can develop.

The authors of the specification do not make claims of suitability of this connector for production boards as it remains outside the scope of this effort. It will remain up to the individual companies of **PIPE** devices to determine the applicability of this specification for their specific product design.

Requirements:

1. Standardized connector
2. Standardized mechanical layout
3. Maximum speed of the interface is 1 GHz
4. Supports 16 bit PIPE interface
5. RefClock from system provided to both MAC and PHY
6. JTAG is required
7. Supports X1 with a single connector
8. Specify retention mechanism/mounting hole location(s)
9. Supplies extra bi-directional reset
10. Provides 2 extra reserve pins for 8b-10b bypass mode

Optional:

1. Supplies power to the PHY board
2. Supports SATA for alternate pin definitions
3. Supports X4 implementations with multiple connectors (3)
4. Support for differential signaling
5. Provides logic analyzer connector (strongly recommended for MAC board)

 

# 3 Connector

The specified connectors are the Samtec* socket connector (QSE-060-01-F-D-A) for the MAC board and the Samtec header connector (QTE-060-04-F-D-A) for the PHY board.

For X1 implementations only 1 connector is required and is designated as Connector 0.

For X4 implementations, 3 connectors are required with the additional connectors designated Connector 1 and Connector 2.

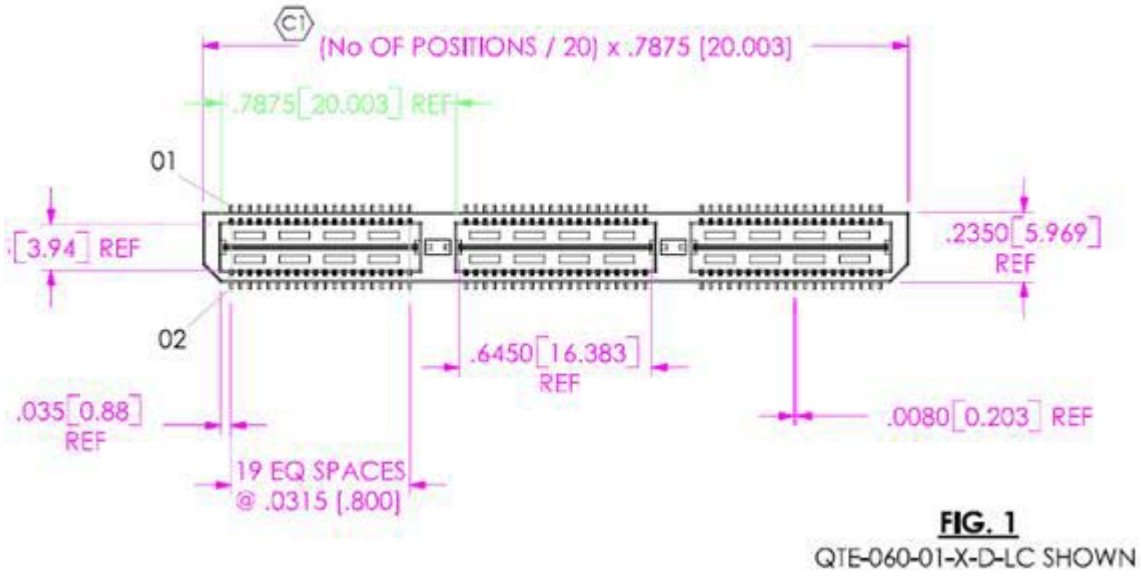


**Figure 1 PHY Connector (QTE-060-04-F-D-A)**

 

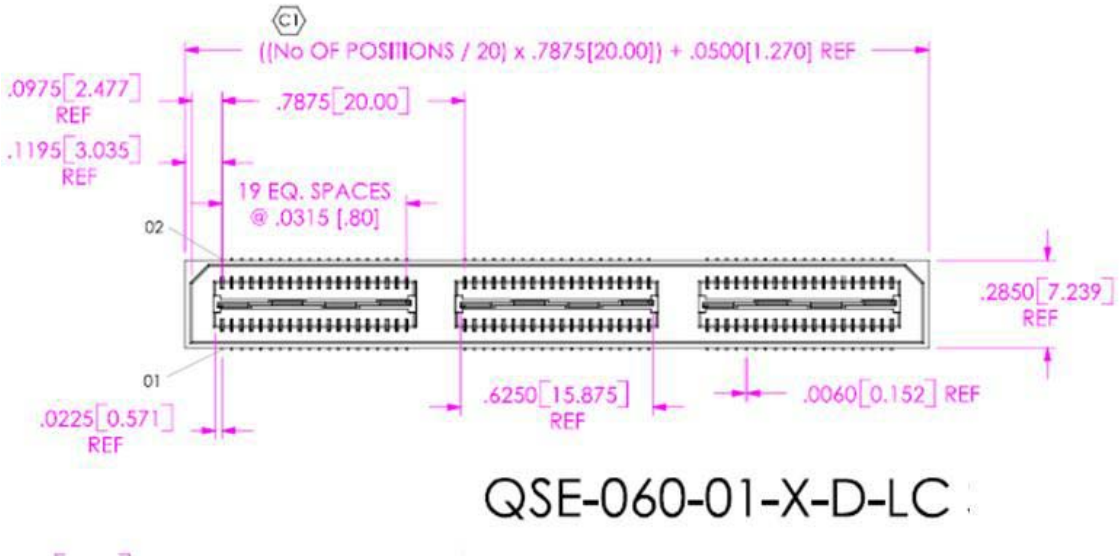


**Figure 2 MAC Connector (QSE-060-01-F-D-A)**

Note: The notches on the Samtec connectors shown here are located near pins 2 and 120. Pin 1 should be marked on the silkscreen with the pin 1 location for the connectors indicated above as a guide to proper placement for assembly.

# 4 Connector Placement and Layout

For mechanical dimensions and connector placement considerations the following conventions are used:

- Primary (component) side is the PCB side that faces away from the CPU when plugged into the PCI Express slot
- Secondary (solder) side is the PCB side that faces the CPU when plugged into the PCI Express connector.
- Bottom edge is the edge of the board closest to motherboard when plugged into the PCI Express slot
- Left edge is the side adjacent to the PCI Express I/O panel.

 

### *4.1 PHY Connector Placement*

The PHY Connector and mounting hole placement is shown in the figure below.

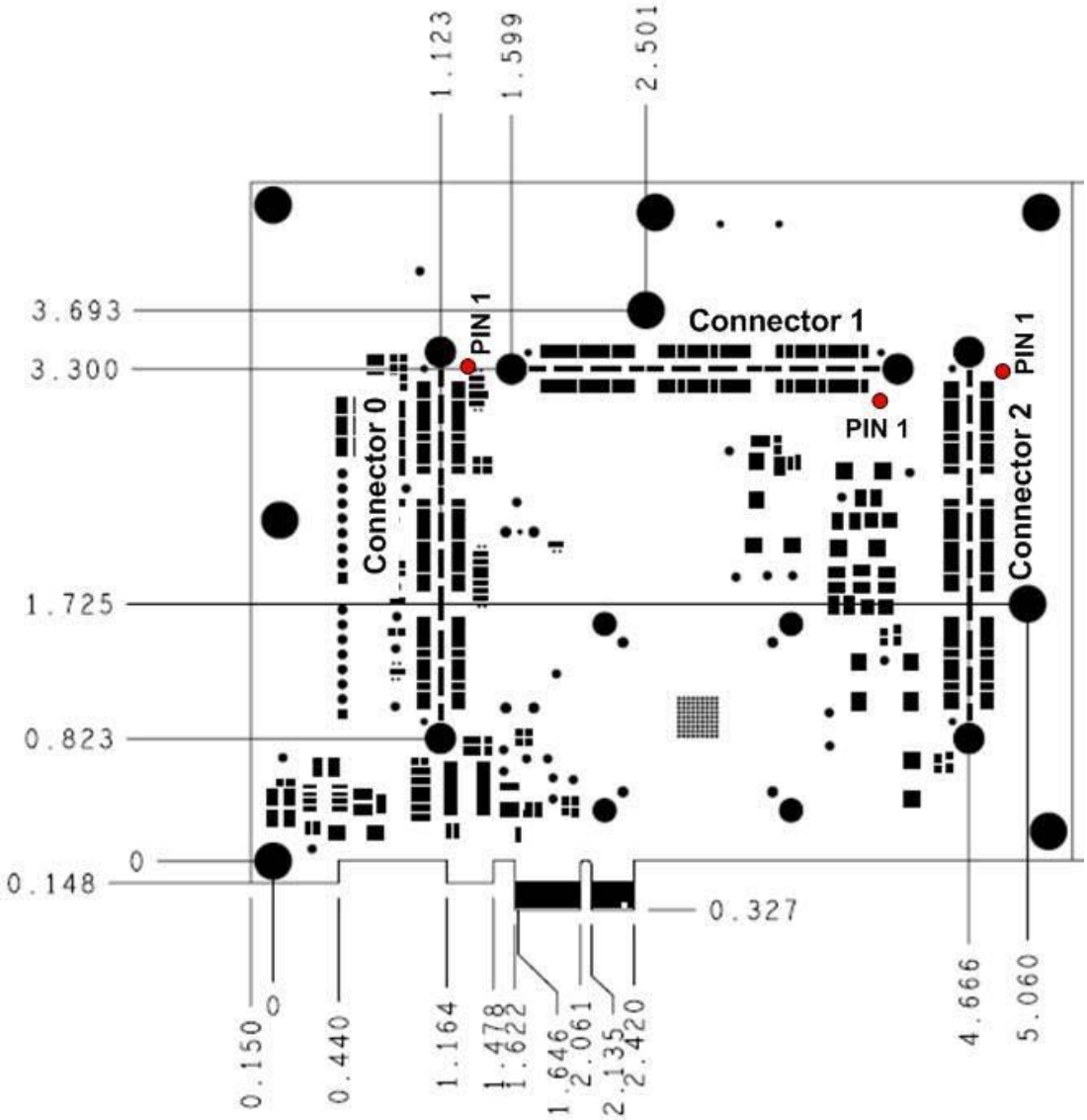


**Figure 3 PHY Connector Placement**

- All dimensions are relative to the lower left mounting bracket hole.
- The specified connectors shown in figure 3 are Samtec header connectors (QTE-060-04-F-D-A).
- Figure 3 illustrates a PHY that supports X4. For X1 implementations only Connector 0 would be used.

***Note: The PHY board connectors mount to the primary side of the board. Figure 3 is a view of the primary (component) side of the board.***

 

## 4.2 MAC Connector Placement

The MAC Connector placement is shown in the figure below.

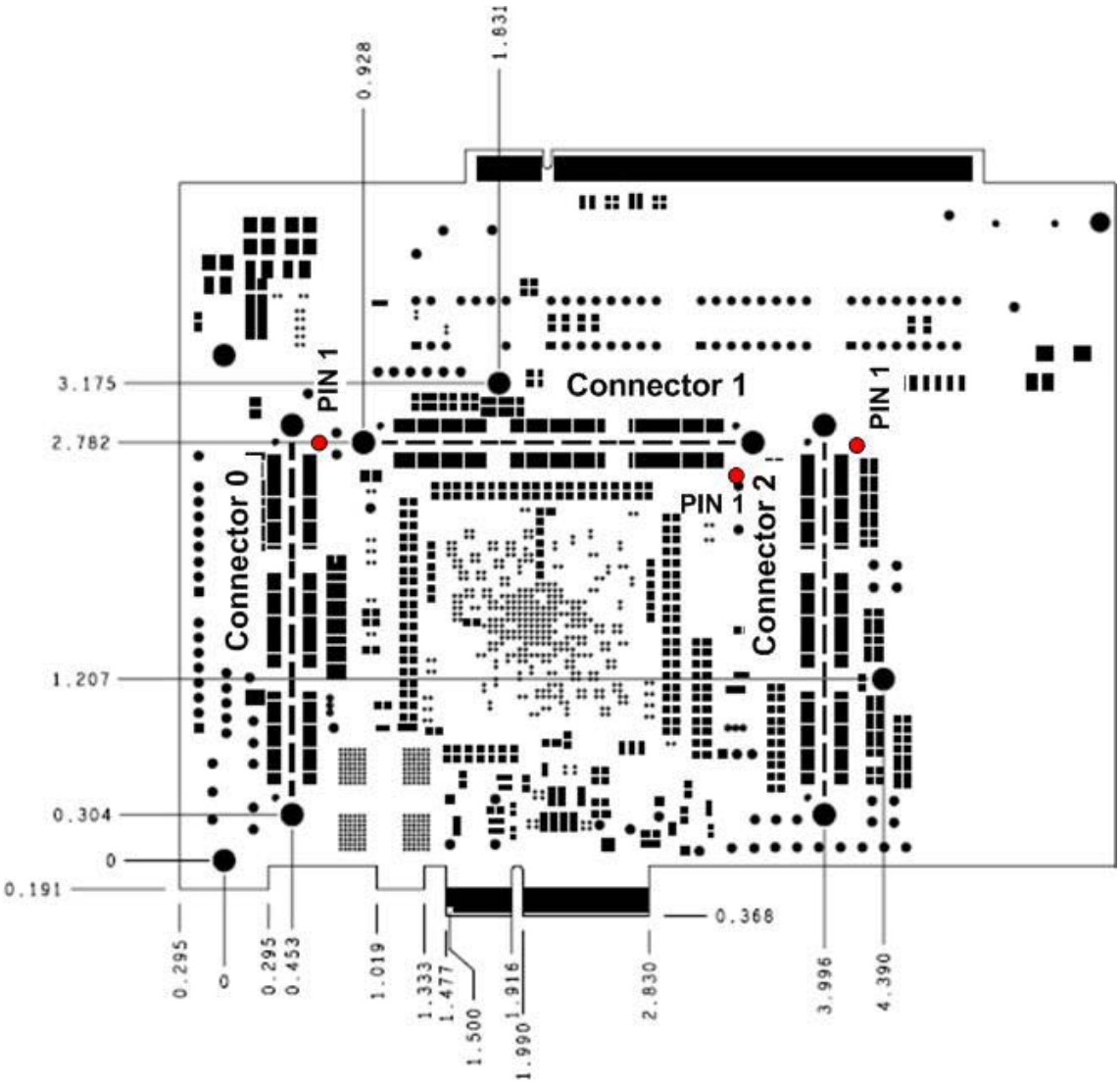


**Figure 4 MAC Connector Placement**

- All dimensions are relative to the lower left mounting bracket hole.
- For X1 MAC designs only Connector 0 is used.

***Note: The MAC board Samtec socket connectors shown above mount to the secondary side of the board. Figure 4 is a view of the primary (component) side of the board.***

 

# 5 Retention mechanism/mounting Holes

PCI I/O Bracket mounting holes are shown in Figure 3 and Figure 4. The placement is in accordance with the latest PCI specification at www.pcisig.com.

Two additional mounting holes are defined to provide a stronger mechanical connection between the MAC and PHY boards. They are located adjacent to Connector 1 and Connector 2 as shown in Figure 3 and Figure 4 above.

# 6 Power

Power is supplied to the PHY via the PCI Express connector with optional power available through the MAC board. The use of the optional Adaptable Power Supply (APS) signals is defined in the XENPAK spec at www.xenpak.org.

 

# 7 Connector Pin-out

**Table 1: Connector 0 pin-out**

| Connector 0 (Left) | | | | | |
|---|---|---|---|---|---|
| A | Note 2 | | | | Note 3 |
| RXDATA_P0[19] | + | 119 | 120 | + | RXDATAK_P0[1] |
| RXDATA_P0[18] | - | 117 | 118 | - | RXDATAK_P0[0] |
| RXDATA_P0[17] | + | 115 | 116 | + | RXELECIDLE_P0 |
| RXDATA_P0[16] | - | 113 | 114 | - | RXSTATUS_P0[2] |
| RXDATA_P0[15] | + | 111 | 112 | + | RXSTATUS_P0[1] |
| RXDATA_P0[14] | - | 109 | 110 | - | RXSTATUS_P0[0] |
| RXDATA_P0[13] | + | 107 | 108 | + | RXVALID_P0 |
| RXDATA_P0[12] | - | 105 | 106 | - | Unallocated fpga I/O |
| RXDATA_P0[11] | + | 103 | 104 | + | Unallocated fpga I/O |
| RXDATA_P0[19] | - | 101 | 102 | - | Unallocated fpga I/O |
| RXDATA_P0[9] | + | 99 | 100 | | APS1_SET[1] |
| RXDATA_P0[8] | - | 97 | 98 | | APS1_SENSE[1] |
| RXDATA_P0[7] | + | 95 | 96 | | APS1[1] |
| RXDATA_P0[6] | - | 93 | 94 | | APS1[1] |
| RXDATA_P0[5] | + | 91 | 92 | | APS2_SET[1] |
| RXDATA_P0[4] | - | 89 | 90 | | APS2_SENSE[1] |
| RXDATA_P0[3] | + | 87 | 88 | | APS2[1] |
| RXDATA_P0[2] | - | 85 | 86 | | APS2[1] |
| RXDATA_P0[1] | + | 83 | 84 | + | PCLK/RXCLK |
| RXDATA_P0[0] | - | 81 | 82 | - | optional PCLK/RXCLK- |
| B | | | | | |
| TXDATA_P0[0] | + | 79 | 80 | + | TXDATAK_P0[1] |
| TXDATA_P0[1] | - | 77 | 78 | - | TXDATAK_P0[0] |
| TXDATA_P0[2] | + | 75 | 76 | + | TXELECIDLE_P0 |
| TXDATA_P0[3] | - | 73 | 74 | - | TXCOMPLIANCE_P0 |
| TXDATA_P0[4] | + | 71 | 72 | + | RXPOLARITY_P0 |
| TXDATA_P0[5] | - | 69 | 70 | - | Unallocated fpga I/O |
| TXDATA_P0[6] | + | 67 | 68 | + | Unallocated fpga I/O |
| TXDATA_P0[7] | - | 65 | 66 | - | Unallocated fpga I/O |
| TXDATA_P0[8] | + | 63 | 64 | + | Unallocated fpga I/O |
| TXDATA_P0[9] | - | 61 | 62 | - | Unallocated fpga I/O |
| TXDATA_P0[10] | + | 59 | 60 | | APS3_SET[1] |
| TXDATA_P0[11] | - | 57 | 58 | | APS3_SENSE[1] |
| TXDATA_P0[12] | + | 55 | 56 | | APS3[1] |
| TXDATA_P0[13] | - | 53 | 54 | | APS3[1] |
| TXDATA_P0[14] | + | 51 | 52 | | APS4_SET[1] |
| TXDATA_P0[15] | - | 49 | 50 | | APS4_SENSE[1] |
| TXDATA_P0[16] | + | 47 | 48 | | APS4[1] |
| TXDATA_P0[17] | - | 45 | 46 | | APS4[1] |
| TXDATA_P0[18] | + | 43 | 44 | + | optional TXCLK |
| TXDATA_P0[19] | - | 41 | 42 | - | optional TXCLK- |

 

| Connector 0 (Left) – continued | | | | | |
|---|---|---|---|---|---|
| C | | | | | |
| GND | | 39 | 40 | | V12 from pcie connector |
| REFCK+ | | 37 | 38 | | V12 from pcie connector |
| REFCK- | | 35 | 36 | | V12 from pcie connector |
| GND | | 33 | 34 | | V12 from pcie connector |
| JTAG_TRST# | | 31 | 32 | | V12 from pcie connector |
| JTAG_TCK | | 29 | 30 | | V33 from pcie connector |
| JTAG_TMS | | 27 | 28 | | V33 from pcie connector |
| JTAG_TDI | | 25 | 26 | | V33 from pcie connector |
| JTAG_TDO | | 23 | 24 | | V33AUX from pcie connector |
| SMCLK | | 21 | 22 | | V12 from fpga board |
| SMDAT | | 19 | 20 | | V12 from fpga board |
| WAKE# | | 17 | 18 | | V33 from fpga board |
| PRSNT1 | | 15 | 16 | | V33 from fpga board |
| PRSNT2x1 | | 13 | 14 | | V33AUX from fpga board |
| PRSNT2x4 | | 11 | 12 | | GND |
| TXDETECTRX/LOOPBACK | | 9 | 10 | | DIFF_CK_1+ from fpga board |
| PHYSTATUS | | 7 | 8 | | DIFF_CK_1- from fpga board |
| POWERDOWN[0] | | 5 | 6 | | GND |
| POWERDOWN[1] | | 3 | 4 | | PRST# from edge connector |
| optional BUS_SELECT | | 1 | 2 | | RESET_RTN# from fpga board |

Note1: All APS may be disabled by the PRSNT1 line.
Note2: Signals designated with a +/- may optionally be routed as differential pairs
Note3: Shaded cells indicate optional/unassigned pins.

 

**Table 2: Connector 1 pin-out**

| Connector 1 (Middle) | | | | | |
|---|---|---|---|---|---|
| A | | | | | |
| RXDATA_P1[0] | + | 119 | 120 | + | RXDATAK_P1[1] |
| RXDATA_P1[1] | - | 117 | 118 | - | RXDATAK_P1[0] |
| RXDATA_P1[2] | + | 115 | 116 | + | RXELECIDLE_P1 |
| RXDATA_P1[3] | - | 113 | 114 | - | RXSTATUS_P1[2] |
| RXDATA_P1[4] | + | 111 | 112 | + | RXSTATUS_P1[1] |
| RXDATA_P1[5] | - | 109 | 110 | - | RXSTATUS_P1[0] |
| RXDATA_P1[6] | + | 107 | 108 | + | RXVALID_P1 |
| RXDATA_P1[7] | - | 105 | 106 | - | Unallocated fpga I/O |
| RXDATA_P1[8] | + | 103 | 104 | + | Unallocated fpga I/O |
| RXDATA_P1[9] | - | 101 | 102 | - | Unallocated fpga I/O |
| RXDATA_P1[10] | + | 99 | 100 | + | Unallocated fpga I/O |
| RXDATA_P1[11] | - | 97 | 98 | - | Unallocated fpga I/O |
| RXDATA_P1[12] | + | 95 | 96 | + | Unallocated fpga I/O |
| RXDATA_P1[13] | - | 93 | 94 | - | Unallocated fpga I/O |
| RXDATA_P1[14] | + | 91 | 92 | + | Unallocated fpga I/O |
| RXDATA_P1[15] | - | 89 | 90 | - | Unallocated fpga I/O |
| RXDATA_P1[16] | + | 87 | 88 | + | Unallocated fpga I/O |
| RXDATA_P1[17] | - | 85 | 86 | - | Unallocated fpga I/O |
| RXDATA_P1[18] | + | 83 | 84 | + | Unallocated fpga I/O |
| RXDATA_P1[19] | - | 81 | 82 | - | Unallocated fpga I/O |
| B | | | | | |
| TXDATA_P1[0] | + | 79 | 80 | + | TXDATAK_P1[1] |
| TXDATA_P1[1] | - | 77 | 78 | - | TXDATAK_P1[0] |
| TXDATA_P1[2] | + | 75 | 76 | + | TXELECIDLE_P1 |
| TXDATA_P1[3] | - | 73 | 74 | - | TXCOMPLIANCE_P1 |
| TXDATA_P1[4] | + | 71 | 72 | + | RXPOLARITY_P1 |
| TXDATA_P1[5] | - | 69 | 70 | - | Unallocated fpga I/O |
| TXDATA_P1[6] | + | 67 | 68 | + | Unallocated fpga I/O |
| TXDATA_P1[7] | - | 65 | 66 | - | Unallocated fpga I/O |
| TXDATA_P1[8] | + | 63 | 64 | + | Unallocated fpga I/O |
| TXDATA_P1[9] | - | 61 | 62 | - | Unallocated fpga I/O |
| TXDATA_P1[10] | + | 59 | 60 | + | Unallocated fpga I/O |
| TXDATA_P1[11] | - | 57 | 58 | - | Unallocated fpga I/O |
| TXDATA_P1[12] | + | 55 | 56 | + | Unallocated fpga I/O |
| TXDATA_P1[13] | - | 53 | 54 | - | Unallocated fpga I/O |
| TXDATA_P1[14] | + | 51 | 52 | + | Unallocated fpga I/O |
| TXDATA_P1[15] | - | 49 | 50 | - | Unallocated fpga I/O |
| TXDATA_P1[16] | + | 47 | 48 | + | Unallocated fpga I/O |
| TXDATA_P1[17] | - | 45 | 46 | - | Unallocated fpga I/O |
| TXDATA_P1[18] | + | 43 | 44 | + | Unallocated fpga I/O |
| TXDATA_P1[19] | - | 41 | 42 | - | Unallocated fpga I/O |

 

| Connector 1 (Middle) - continued | | | | | |
|---|---|---|---|---|---|
| C | | | | | |
| RXDATA_P2[0] | + | 39 | 40 | + | RXDATAK_P2[1] |
| RXDATA_P2[1] | - | 37 | 38 | - | RXDATAK_P2[0] |
| RXDATA_P2[2] | + | 35 | 36 | + | RXELECIDLE_P2 |
| RXDATA_P2[3] | - | 33 | 34 | - | RXSTATUS_P2[2] |
| RXDATA_P2[4] | + | 31 | 32 | + | RXSTATUS_P2[1] |
| RXDATA_P2[5] | - | 29 | 30 | - | RXSTATUS_P2[0] |
| RXDATA_P2[6] | + | 27 | 28 | + | RXVALID_P2 |
| RXDATA_P2[7] | - | 25 | 26 | - | Unallocated fpga I/O |
| RXDATA_P2[8] | + | 23 | 24 | + | Unallocated fpga I/O |
| RXDATA_P2[9] | - | 21 | 22 | - | Unallocated fpga I/O |
| RXDATA_P2[10] | + | 19 | 20 | + | Unallocated fpga I/O |
| RXDATA_P2[11] | - | 17 | 18 | - | Unallocated fpga I/O |
| RXDATA_P2[12] | + | 15 | 16 | + | Unallocated fpga I/O |
| RXDATA_P2[13] | - | 13 | 14 | - | Unallocated fpga I/O |
| RXDATA_P2[14] | + | 11 | 12 | + | Unallocated fpga I/O |
| RXDATA_P2[15] | - | 9 | 10 | - | Unallocated fpga I/O |
| RXDATA_P2[16] | + | 7 | 8 | + | Unallocated fpga I/O |
| RXDATA_P2[17] | - | 5 | 6 | - | Unallocated fpga I/O |
| RXDATA_P2[18] | + | 3 | 4 | + | Unallocated fpga I/O |
| RXDATA_P2[19] | - | 1 | 2 | - | Unallocated fpga I/O |

 

**Table 3: Connector 2 pin-out**

| Connector 2 (Right) | | | | | |
|---|---|---|---|---|---|
| A | | | | | |
| Unallocated fpga I/O | - | 119 | 120 | - | TXDATA_P3[19] |
| Unallocated fpga I/O | + | 117 | 118 | + | TXDATA_P3[18] |
| GND | | 115 | 116 | - | TXDATA_P3[17] |
| DIFF_CK_2+ from fpga board | | 113 | 114 | + | TXDATA_P3[16] |
| DIFF_CK_2- from fpga board | | 111 | 112 | - | TXDATA_P3[15] |
| GND | | 109 | 110 | + | TXDATA_P3[14] |
| Unallocated fpga I/O | - | 107 | 108 | - | TXDATA_P3[13] |
| Unallocated fpga I/O | + | 105 | 106 | + | TXDATA_P3[12] |
| Unallocated fpga I/O | - | 103 | 104 | - | TXDATA_P3[11] |
| Unallocated fpga I/O | + | 101 | 102 | + | TXDATA_P3[10] |
| Unallocated fpga I/O | - | 99 | 100 | - | TXDATA_P3[9] |
| Unallocated fpga I/O | + | 97 | 98 | + | TXDATA_P3[8] |
| Unallocated fpga I/O | - | 95 | 96 | - | TXDATA_P3[7] |
| Unallocated fpga I/O | + | 93 | 94 | + | TXDATA_P3[6] |
| Unallocated fpga I/O | - | 91 | 92 | - | TXDATA_P3[5] |
| RXPOLARITY_P3 | + | 89 | 90 | + | TXDATA_P3[4] |
| TXCOMPLIANCE_P3 | - | 87 | 88 | - | TXDATA_P3[3] |
| TXELECIDLE_P3 | + | 85 | 86 | + | TXDATA_P3[2] |
| TXDATAK_P3[0] | - | 83 | 84 | - | TXDATA_P3[1] |
| TXDATAK_P3[1] | + | 81 | 82 | + | TXDATA_P3[0] |
| B | | | | | |
| Unallocated fpga I/O | - | 79 | 80 | - | RXDATA_P3[19] |
| Unallocated fpga I/O | + | 77 | 78 | + | RXDATA_P3[18] |
| Unallocated fpga I/O | - | 75 | 76 | - | RXDATA_P3[17] |
| Unallocated fpga I/O | + | 73 | 74 | + | RXDATA_P3[16] |
| Unallocated fpga I/O | - | 71 | 72 | - | RXDATA_P3[15] |
| Unallocated fpga I/O | + | 69 | 70 | + | RXDATA_P3[14] |
| Unallocated fpga I/O | - | 67 | 68 | - | RXDATA_P3[13] |
| Unallocated fpga I/O | + | 65 | 66 | + | RXDATA_P3[12] |
| Unallocated fpga I/O | - | 63 | 64 | - | RXDATA_P3[11] |
| Unallocated fpga I/O | + | 61 | 62 | + | RXDATA_P3[10] |
| Unallocated fpga I/O | - | 59 | 60 | - | RXDATA_P3[9] |
| Unallocated fpga I/O | + | 57 | 58 | + | RXDATA_P3[8] |
| Unallocated fpga I/O | - | 55 | 56 | - | RXDATA_P3[7] |
| RXVALID_P3 | + | 53 | 54 | + | RXDATA_P3[6] |
| RXSTATUS_P3[0] | - | 51 | 52 | - | RXDATA_P3[5] |
| RXSTATUS_P3[1] | + | 49 | 50 | + | RXDATA_P3[4] |
| RXSTATUS_P3[2] | - | 47 | 48 | - | RXDATA_P3[3] |
| RXELECIDLE_P3 | + | 45 | 46 | + | RXDATA_P3[2] |
| RXDATAK_P3[0] | - | 43 | 44 | - | RXDATA_P3[1] |
| RXDATAK_P3[1] | + | 41 | 42 | + | RXDATA_P3[0] |

 

| Connector 2 (Right) - continued | | | | | |
|---|---|---|---|---|---|
| C | | | | | |
| Unallocated fpga I/O | - | 39 | 40 | - | TXDATA_P2[19] |
| Unallocated fpga I/O | + | 37 | 38 | + | TXDATA_P2[18] |
| Unallocated fpga I/O | - | 35 | 36 | - | TXDATA_P2[17] |
| Unallocated fpga I/O | + | 33 | 34 | + | TXDATA_P2[16] |
| Unallocated fpga I/O | - | 31 | 32 | - | TXDATA_P2[15] |
| Unallocated fpga I/O | + | 29 | 30 | + | TXDATA_P2[14] |
| Unallocated fpga I/O | - | 27 | 28 | - | TXDATA_P2[13] |
| Unallocated fpga I/O | + | 25 | 26 | + | TXDATA_P2[12] |
| Unallocated fpga I/O | - | 23 | 24 | - | TXDATA_P2[11] |
| Unallocated fpga I/O | + | 21 | 22 | + | TXDATA_P2[10] |
| Unallocated fpga I/O | - | 19 | 20 | - | TXDATA_P2[9] |
| Unallocated fpga I/O | + | 17 | 18 | + | TXDATA_P2[8] |
| Unallocated fpga I/O | - | 15 | 16 | - | TXDATA_P2[7] |
| Unallocated fpga I/O | + | 13 | 14 | + | TXDATA_P2[6] |
| Unallocated fpga I/O | - | 11 | 12 | - | TXDATA_P2[5] |
| RXPOLARITY_P2 | + | 9 | 10 | + | TXDATA_P2[4] |
| TXCOMPLIANCE_P2 | - | 7 | 8 | - | TXDATA_P2[3] |
| TXELECIDLE_P2 | + | 5 | 6 | + | TXDATA_P2[2] |
| TXDATAK_P2[0] | - | 3 | 4 | - | TXDATA_P2[1] |
| TXDATAK_P2[1] | + | 1 | 2 | + | TXDATA_P2[0] |

 