IT@Intel Brief

Intel Information Technology

Computer Manufacturing

64-Bit Computing

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Increasing Design Productivity with Digital Workbenches

In Intel IT tests simulating the daily workflow of a silicon design engineer, a digital workbench based on the Intel® Xeon® processor 5500 series completed multiple, concurrent electronic design automation (EDA) application workloads 2.9x faster than a workstation based on the Intel® Xeon® processor 5100 series, and 1.53x faster than a workstation based on Intel® Xeon® processor 5400 series. Performance comparisons are shown in Figure 1.

Profile: Intel® Xeon® Processor 5500 Series

- Up to 2.9x performance increase
- Enables increase in design engineer productivity
- Potential for faster time to market and quality improvements

Digital workbenches are high-performance dual-processor workstations, based on the Intel Xeon processor 5500 series, that let engineers create and test designs more quickly using multiple EDA applications concurrently. This allows faster design iterations with more-demanding design workloads, accelerating product time to market. It also allows for more validation cycles, enabling improvements in product quality.

In our tests, each system ran multiple front-end and back-end EDA applications operating on real Intel silicon design workloads. A dual-processor digital workbench based on Intel Xeon processor W5580 ran eight EDA applications concurrently—2x as many as a dual-processor workstation based on Intel Xeon processor 5160—and completed each workload faster than the other systems tested.

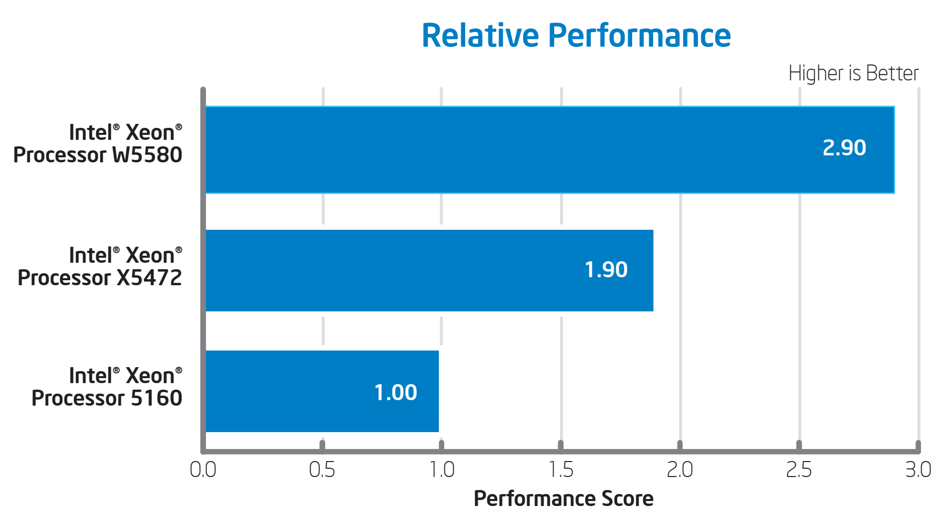

Figure 1. Relative performance of workstations running multiple front-end and back-end electronic design automation (EDA) applications. Based on Intel IT tests with up to eight concurrent EDA application processes operating on Intel silicon design workloads. Intel internal measurements, June 2009.

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Business Challenge

Design engineers at Intel face the challenges of integrating more features into ever-shrinking silicon chips, bringing products to market faster, and keeping engineering design and manufacturing costs low.

In a typical workday, each design engineer works simultaneously on several of the functional blocks of a silicon design. For each block, the engineer uses an iterative design method in which each front-end (logical) design stage is followed by a corresponding back-end (physical) design stage, as shown in Figure 2. Each of these design stages is supported by EDA applications that run on engineering workstations based on Intel® Xeon® processors. Each application workload is processor-intensive and can take from several minutes to hours to complete.

Digital Workbenches

In the past, design engineers staggered design tasks due to limitations in the number of processor cores and the processing power of each workstation.

However, as processor performance has increased, a new category of workstations has emerged: the digital workbench, based on the Intel Xeon processor 5500 series. Digital workbenches allow engineers to more quickly create and test design ideas by running suites of multiple front-end and back-end EDA applications concurrently.

The Intel Xeon processor 5500 series, based on Intel® microarchitecture formerly codenamed Nehalem, includes four cores per processor, with features to maximize performance such as Intel® Turbo Boost Technology, Intel® QuickPath Interconnect, and Intel® Hyper-Threading Technology.

Dual-processor digital workbenches based on the Intel Xeon processor 5500 series include up to 192 GB RAM capacity (with 16 GB DIMMS) to support more-demanding workloads. These systems enable engineers to simultaneously run more EDA applications, allocating one core per application process or thread to increase throughput.

To evaluate the impact on design engineers' productivity, we performed tests to compare a digital workbench based on Intel Xeon processor 5500 series with workstations based on previous processor generations.

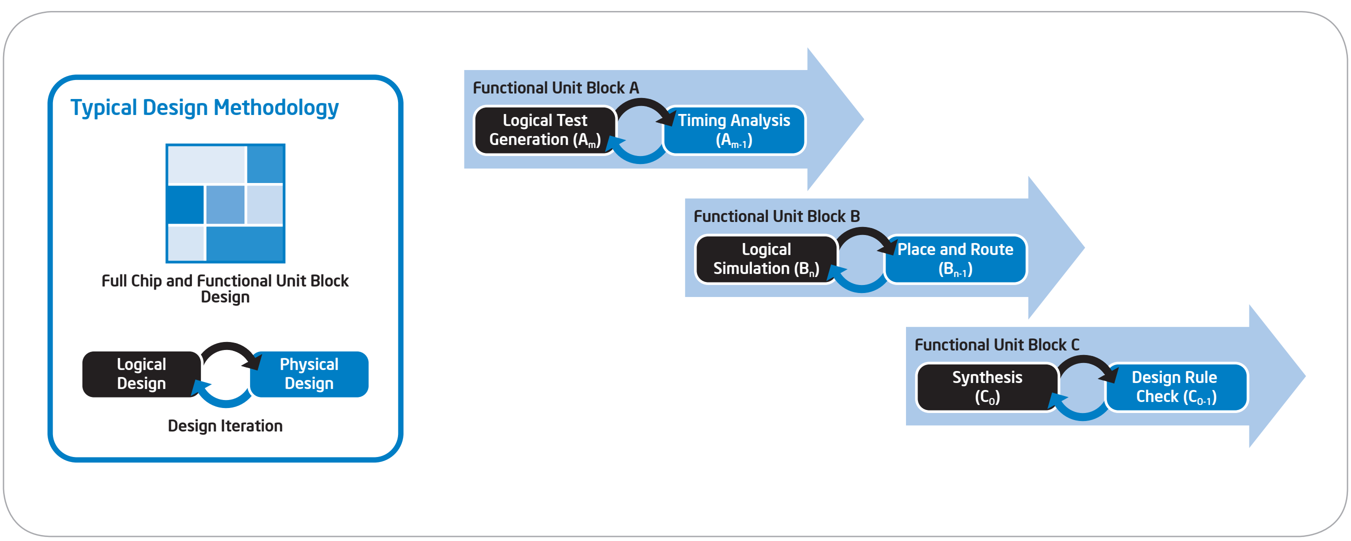

Figure 2. Day in the life of a silicon design engineer. An engineer typically works simultaneously on several of the functional blocks in each silicon design; each block is designed using an iterative process supported by front-end and back-end EDA applications.

Test Method

We designed our tests to represent a typical silicon design engineer's work day. We tested performance with up to eight concurrent front-end and back-end 32-bit and 64-bit EDA applications or threads operating on real Intel processor and chipset design workloads. We recorded each individual application runtime and the elapsed time required to complete all the workloads.

We compared three dual-processor workstations, each based on a different processor generation.

Intel Xeon processor 5160-based workstation. This workstation included two dual-core processors, for a total of four cores. Running one application process per core to optimize performance and efficiency, an engineer working on multiple functional blocks could run up to four concurrent front-end applications in the morning, followed by a second run of multiple back-end applications in the afternoon. Our test reflected this: We ran four front-end applications concurrently and when all had completed, we ran four back-end application processes (one dual-threaded and two single-threaded jobs).

Intel Xeon processor X5472-based workstation. This workstation included two quad-core processors, for a total of eight cores. This enabled us to run up to eight application processes simultaneously with a ratio of one process per core. Accordingly, we tested the workstation running all eight front-end and back-end application processes concurrently.

Digital workbench: Intel Xeon processor W5580-based workstation. This workstation included two quad-core processors, built on the latest Intel microarchitecture, Nehalem, for a total of eight cores. Accordingly, we tested the workstation running all the front-end and back-end applications concurrently.

System specifications are shown in Table 1.

Table 1. Test System Specifications

	Intel® Xeon® Processor 5100 Series	Intel® Xeon® Processor 5400 Series	Intel® Xeon® Processor 5500 Series
Processor	2x Intel® Xeon® processor 5160	2x Intel® Xeon® processor X5472	2x Intel® Xeon® processor W5580
Cores per processor	2	4	4
Speed	3.0 GHz	3.0 GHz	3.2 GHz
Turbo Mode	N/A	N/A	Enabled
Hyperthreading	N/A	N/A	Disabled
Chipset	Intel® 5000X Chipset	Intel® 5400 Chipset	Intel® 5520 Chipset
Interconnects	1333 MHz FSB	1600 MHz FSB	6.4 GT/s Intel® QuickPath Interconnect
RAM	32 GB (8x 4 GB)	32 GB (8x 4 GB)	48 GB (12x 4 GB)
RAM Type	DDR2-667/Fully Buffered DIMM	DDR2-667/Fully Buffered DIMM	DDR3-1333 MHz (operating at 1066 MHz)
Hard Drive	500 GB, 7200 RPM SATA 3.0 Gb/S	500 GB, 7200 RPM SATA 3.0 Gb/S	500 GB, 7200 RPM SATA 3.0 Gb/S
OS	64-bit Linux*	64-bit Linux	64-bit Linux

Table 2. Electronic Design Automation (EDA) Performance Test Results

Design Stage and EDA Application (One EDA application process/thread running per core)		Application Type	Peak Memory	Total Memory	Intel® Xeon® Processor 5160	Intel® Xeon® Processor X5472	Intel® Xeon® Processor W5580
Front-end (FE) Design	Logic Simulation - Tool B (Workload 1)	32-bit	3.71 GB	17.08 GB	0:56:57	1:10:35	0:40:26
	Logic Simulation - Tool B (Workload 2)[1]	32-bit	4.93 GB[1]		2:41:01	3:05:55	1:52:34
	Logic Test Generation -Tool A	64-bit	937 MB		4:08:06	3:52:37	2:40:31
	Synthesis - Tool B-2	64-bit	7.5 GB		3:18:18	3:36:36	2:26:02
Back-end (BE) Design	Place & Route - Tool A	64-bit	6.15 GB	11.96 GB	2:50:26	3:05:52	2:11:12
	Timing Analysis - Tool B-2	32-bit	3.73 GB		0:53:26	0:39:39	0:30:55
	Design Rule Check (DRC) - Tool B (2 Threads)	64-bit	2.08 GB		4:03:42	4:19:17	2:49:44
				FE Design Flow Time	4:08:06	3:52:37	2:40:31
				BE Design Flow Time	4:03:42	4:19:17	2:49:44
				Combined FE and BE Design Time	8:11:48	4:19:17	2:49:44
				Normalized Throughput of Workstations	1.00	1.90	2.90

[1] Multiple 32-bit application processes are in execution and the memory used is a sum total of all the processes.
Note: Smaller runtime applications were running in loop to keep each CPU core busy.

Results

The digital workbench based on Intel Xeon processor W5580 completed the test 2.90x faster than the workstation based on Intel Xeon processor 5160, and 1.53x faster than the workstation based on Intel Xeon processor X5472. Results are shown in Table 2 and Figure 1.

The faster test completion was due to the fact that the system based on Intel Xeon processor W5580 completed each application workload more quickly than either of the other two workstations; in addition, with eight cores, it was able to run twice as many front-end and back-end applications concurrently as the workstation based on Intel Xeon processor 5160.

This increased performance enables silicon design engineers to be more efficient and productive; a set of design workloads that required a full eight-hour day to process using Intel Xeon processor 5160 can be completed in less than three hours using Intel Xeon processor W5580.

The availability of the digital workbench based on Intel Xeon processor 5500 series has broad implications for silicon design. In the past, design engineers staggered design tasks due to limitations in processing power and the number of cores available. Now, with twice as many cores available, design engineers can run twice as many jobs concurrently. In addition, each processing core offers faster performance, reducing total design time.

This allows engineers to analyze the results of each design stage sooner, make necessary design changes, and quickly run the next design iteration. This results in increased design engineer productivity, which enables faster semiconductor product design. Engineers can also run more validation cycles, identifying problems earlier in product development to improve quality.

For more information about Intel® Xeon® processor-based workstation technology, visit www.intel.com/go/workstation.

Learn more about Intel IT's best practices at www.intel.com/IT.

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