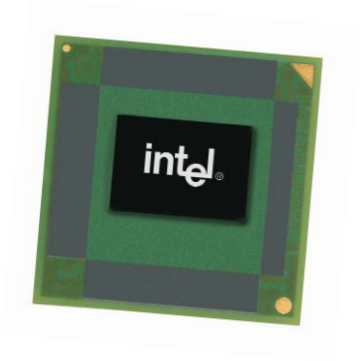
Intel® 82571EB Gigabit Ethernet Controller

High-performance, Dual-Port Gigabit Network Connectivity for Servers and Embedded System Designs

- **High-performing, PCI Express* 10/100/1000 Ethernet connection**
- **Dual-port, single-chip configuration simplifies designs**
- **Footprint compatibility with single-port Gigabit Ethernet (GbE) controllers for flexible designs**



The Intelligent Way to Connect

The Intel® 82571EB Gigabit Ethernet Controller is a single, compact component with two fully integrated Gigabit Ethernet Media Access Control (MAC) and physical layer (PHY) ports. This device uses the PCI Express architecture (Rev. 1.0a), and also enables a dual-port Gigabit Ethernet implementation in a very small area, which is useful for server and workstation network designs with critical space constraints. The Intel 82571EB Gigabit Ethernet Controller provides two IEEE 802.3* Ethernet interfaces for 1000BASE-T, 100BASE-TX, and 10BASE-T applications. Both ports also integrate a Serializer-Deserializer (SerDes) to support 1000BASE-SX or 1000BASE-LX (optical fiber) and Gigabit backplane applications. In addition to managing MAC and PHY Ethernet layer functions, the controller manages PCI Express packet traffic across its transaction, link, and physical/logical layers.

On-Board Management Features

The on-board System Management Bus (SMB) and Fast Management Link (FML) ports of the Intel 82571EB Gigabit Ethernet Controller enable network manageability implementations required by IT personnel for remote control and for alerting via the LAN. With SMB, management network packets can be routed to or from a management processor. The SMB port enables industry standards, such as the Intelligent Platform Management Interface (IPMI) and Alert Standard Format (ASF) 2.0, to be implemented using the controller. In addition, connecting to a management processor via the controller's FML port allows higher-speed management traffic, such as keyboard, video and mouse (KVM) data, to be sent via the LAN to a remote management console. Both SMB and FML operation use the standard SMB protocol and allow enhanced pass-through implementations using standardized interfaces.

Intel® PRO Network Connections

Features	Benefits
PCI Express* Features	
Uses x4 PCI Express interface on Memory Control Hub (MCH) device	• Bus sharing not required • Low latency path to memory
2 Gbps peak bandwidth per direction per PCI Express lane	• Supports dual-port Gigabit Ethernet at wire speed
Complies with peripheral component interconnect (PCI) Power Management 1.1 and advanced configuration and power interface (ACPI) 2.0 register set (D0 & D3 power states, Network Device Class Power Management Specification 1.1)	• Provides PCI Express power management capabilities for PC and embedded applications
High bandwidth density per pin	• Less congested board routing
Gigabit MAC/PHY Advanced Features	
Wide, pipelined internal data path architecture	• Low-latency data handling • Superior direct memory access (DMA) transfer-rate performance
Multiple, optimized transmit (Tx) and receive (Rx) queues	• Network packet handling without waiting or buffer overflow • Efficient packet prioritization
Dual 48 KB configurable Rx and Tx first-in/first-out (FIFO) buffers with support for error correction code (ECC)	• No external FIFO memory requirements • FIFO size adjustable to application • Error detection and correction for FIFO data
Support for transmission and reception of packets up to 9 Kbytes	• Enables use of jumbo frames
IEEE 802.3* compliant flow-control support with software-controllable pause times and threshold values	• Frame loss reduced from receive overruns • Hardware or software control over transmission of pause frames
Caches up to 64 packet descriptors per queue	• Efficient use of PCI Express bandwidth
Programmable host memory receive buffers (256 Bytes to 16 KBytes) and cache line size (64 Bytes to 128 Bytes)	• Efficient use of PCI Express bandwidth
Descriptor ring management hardware for Tx/Rx with optimized descriptor fetching and write-back mechanisms	• Simple software programming model • Efficient use of system memory and PCI Express
Mechanism for reducing interrupts from Tx/Rx operations	• Maximizes system performance and throughput
Integrated PHY for 10/100/1000 Mbps (full- and half-duplex)	• Smaller footprint, lower power dissipation compared to multi-chip MAC and PHY solutions
IEEE 802.3 auto-negotiation support	• Automatic link configuration for speed, duplex, flow control
IEEE 802.3 PHY compliance and compatibility	• Robust operation over installed base of Category-5 twisted-pair cabling
Built-in cable diagnostics and adjustments for cable faults	• Improved end-user troubleshooting • Tolerance of common wiring faults
Host Offloading Features	
Tx/Rx IP, TCP, and UDP checksum offloading (IPv4, IPv6)	• Lower processor utilization
Tx TCP segmentation (IPv4, IPv6)	• Increased throughput and lower processor utilization • Compatible with large send offload (in Microsoft Windows* operating systems)
Packet filtering including: • 16 exact-matched packets (unicast or multicast) • 4096-bit hash filter for multicast frames • Promiscuous (unicast and multicast) transfer mode support • Filtering of invalid frames	• Ability to use advanced packet filtering in software • Lower processor utilization
IEEE 802.1q* virtual local area network (VLAN) support with VLAN tag insertion, stripping, and packet filtering for up to 4096 VLAN tags	• Ability to create multiple VLAN segments
Manageability Features	
Two SMB ports, one with Fast Management Link capability	• Allows packet routing to and from either LAN port and a Board Management Controller (BMC) such as IPMI • Manageability data transfers up to 8 Mbps peak rate
Alerting Standards Format 2.0	• Standard alerting capability to notify IT of system events
Advanced pass through	• Filtering and redirection for management packets • Support for serial text and keyboard redirection and remote floppy/CD
Preboot eXecution Environment (PXE) flash interface support (32 bit and 64 bit)	• Enables system boot up via the LAN • Flash interface for PXE image
Simple Network Management Protocol (SNMP) and Remote Network Monitoring (RMON) statistic counters	• Easy system monitoring with industry-standard consoles
SDG 3.0, Wired for Management (WfM) 3.0 and PC2001 compliant	• Remote network management through Desktop Management Interface (DMI) 2.0 and SNMP
Wake on LAN support	• Packet recognition and wake-up for LAN on motherboard applications without software configuration

Additional Device Features	
Dual Integrated SerDes	• Supports backplane and fiber optic applications
Four outputs on each port that directly drive LEDs with programmable LED functionality	• Software-definable function (speed, link, activity) and blinking allow flexible LED signaling implementations
Internal phase-locked loop (PLL) for clock generation can use 25-MHz crystal	• Lower component count and reduced system cost
JTAG (IEEE 1149.1*) test access port built-in silicon	• Simplified testing using boundary scan
Loop-back capability	• Built-in tests for silicon integrity
Characteristics	
Electrical	
PCI Express signaling	• 3.3 V
Typical targeted power dissipation (in active link state)	• 2.8 W @ D0 1000 Mbps • 730 mW @ D3 100 Mbps (wakeup enabled) • 350 mW @ D3 wakeup disabled
Environmental	
Operating temperature	• 1000BASE-T, 0° to 70° C (with thermal management) • 1000BASE-SX/LX (or SerDes backplane), 0° to 70° C
Storage temperature	• –65° C to 140° C
Physical	
Implemented in 90nm complementary metal-oxide semiconductor (CMOS) process	• Offers lowest geometry to minimize power and size while maintaining quality and reliability
Package	• Lead-free[1] 256-pin Flip-Chip Ball Grid Array (FC-BGA) package

High-Performance Design Features

The Intel 82571EB Gigabit Ethernet Controller for PCI Express is designed for high performance and low memory latency. The device is optimized to connect to a system Memory Control Hub (MCH) using up to four PCI Express lanes. Alternatively, the controller can connect to an Input/Output (I/O) Control Hub (ICH) that has a PCI Express interface. Wide internal data paths eliminate performance bottlenecks by efficiently handling large address and data words. Combining a parallel and pipelined logic architecture optimized for Gigabit Ethernet and for independent transmit and receive queues, the controller efficiently handles packets with minimum latency. The controller includes advanced interrupt-handling features and uses efficient ring-buffer descriptor data structures, with up to 64 packet descriptors cached on chip. A large 48 KByte per port on-chip packet buffer maintains superior performance. In addition, using hardware acceleration, the controller offloads tasks from the host, such as checksum calculations for transmission control protocol (TCP), user datagram protocol (UDP), and Internet protocol (IP); header and data splitting; and TCP segmentation.

The Intel 82571EB Gigabit Ethernet Controller package is a 17 mm x 17 mm, 256-ball grid array.

Order Codes

82571EB	• HL82571EB
82571EB lead-free[1]	• JL82571EB

PCI EXPRESS®

For more information, contact your Intel sales representative.

[1]Lead has not been intentionally added, but lead may still exist as an impurity below 1000 ppm, or an approved RoHS exemption applies.

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