PCI Express* 3.0 Technology: Device Architecture Optimizations on Intel Platforms

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TCIS006

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Agenda

- Next Generation PCI Express* (PCIe*) Protocol Extensions Summary
- Device Architecture Considerations
  - Energy Efficient Performance
  - Power Management
- Software Development
- Summary
- Call to action

PCI Express* (PCIe*) 2.1 Protocol Extensions Summary

Extensions	Explanation	Benefit
Transaction Layer Packet (TLP) Processing Hints	Request hints to enable optimized processing within host memory/cache hierarchy	Reduce access latency to system memory. Reduce System Interconnect & Memory Bandwidth & Associated Power Consumption Application Class: NIC, Storage, Accelerators/GP-GPU
Latency Tolerance Reporting	Mechanisms for platform to tune PM	Reducing Platform Power based on device service requirements, Application Class: All devices/Segments
Opportunistic Buffer Flush and Fill	Mechanisms for platform to tune PM and to align device activities	Reducing Platform Power based aligning device activity with platform PM events to further reduce platform power Application Class: All devices/Segments
Atomics	Atomic Read-Modify-Write mechanism	Reduced Synchronization overhead, software library algorithm and data structure re-use across core and accelerators/devices. Application Class: (Graphics, Accelerators/GP-GPU))
Resizable BAR	Mechanism to negotiate BAR size	System Resource optimizations - breakaway from “All or Nothing device address space allocation” Application Class: – Any Device with large local memory (Example: Graphics)
Multicast	Address Based Multicast	Significant gain in efficiency compared to multiple unicasts Application Class: (Embedded, Storage & Multiple Graphics adapters)

Continued…

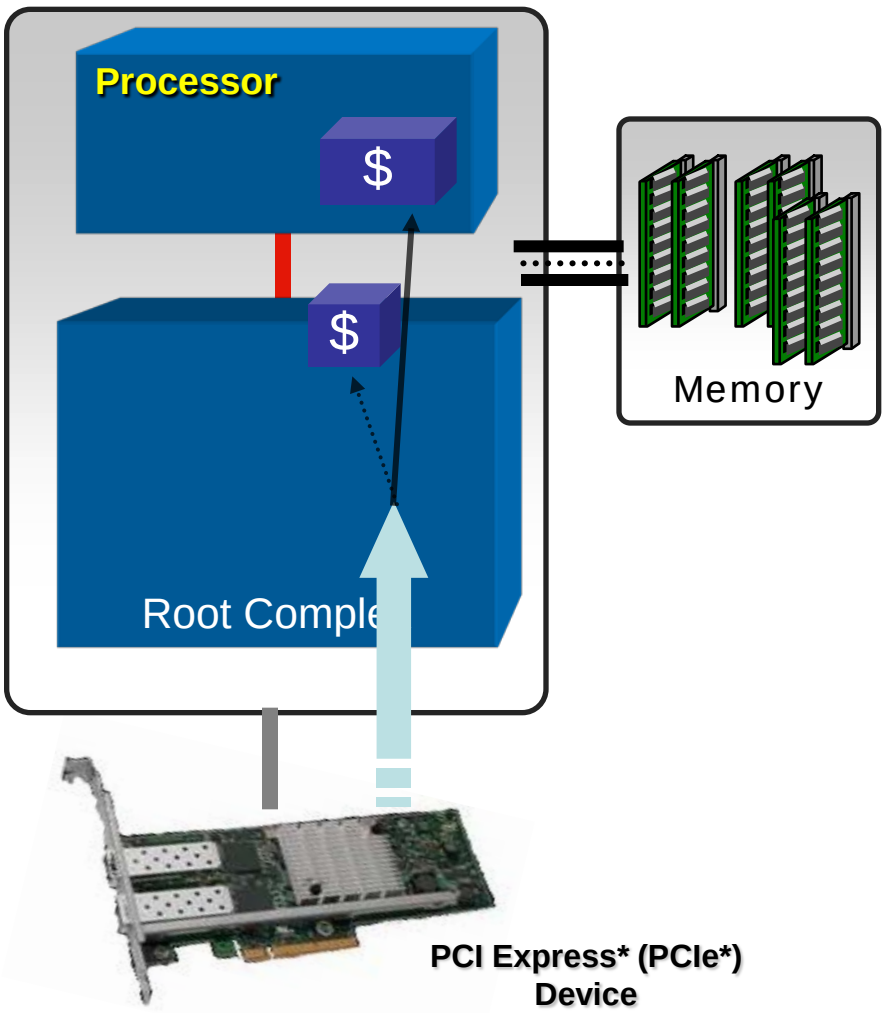
Extensions	Explanation	Benefit
I/O Page Faults	Extends IO address remapping for page faults – (Address Translation Services 1.1)	System Memory Management optimizations Application Class: Accelerators, GP-GPU usage models
Ordering Enhancements	New ordering semantic to improve performance	Improved performance (latency reduction) ~ (IDO) 20% read latency improvement by permitting unrelated reads to pass writes. Application Class: All Devices with two party communication
Dynamic Power Allocation (DPA)	Mechanisms to allow dynamic power/performance management of D0 (active) substates.	Dynamic component power/thermal control, manage endpoint function power usage to meet new customer or regulatory operation requirements Application Class: GP-GPU
Internal Error Reporting	Extend AER to report component internal errors (Correctable/ uncorrectable) and multiple error logs	Enables software to implement common and interoperable error handling services. Improved error containment and recovery. Application Class: RAS for Switches
TLP Prefix	Mechanism to extend TLP headers	Scalable Architecture headroom for TLP headers to grow with minimal impact to routing elements. Support Vendor Specific header formats. Application Class: MR-IOV, Large Topologies and provisioning for future use models

New Features with Broad Applicability

Device Architecture Considerations

- TLP Processing Hints (TPH)
- Power Management Extensions

TLP Processing Hints (TPH)



TLP Processing Hints (PCIe Base 2.1 specification)

- Memory Read, Memory Write and Atomic Operations

System Specific Steering Tags (ST)

- Identify targeted resource e.g. System Cache Location
- 256 unique Steering Tags

Benefits

Effective Use of System Resources

- Reduce Access latency to system memory
- Reduce Memory & system interconnect BW & Power

Improves System Efficiency

Effective use of System Fabric and Resources

Requirements Checklist

Ecosystem

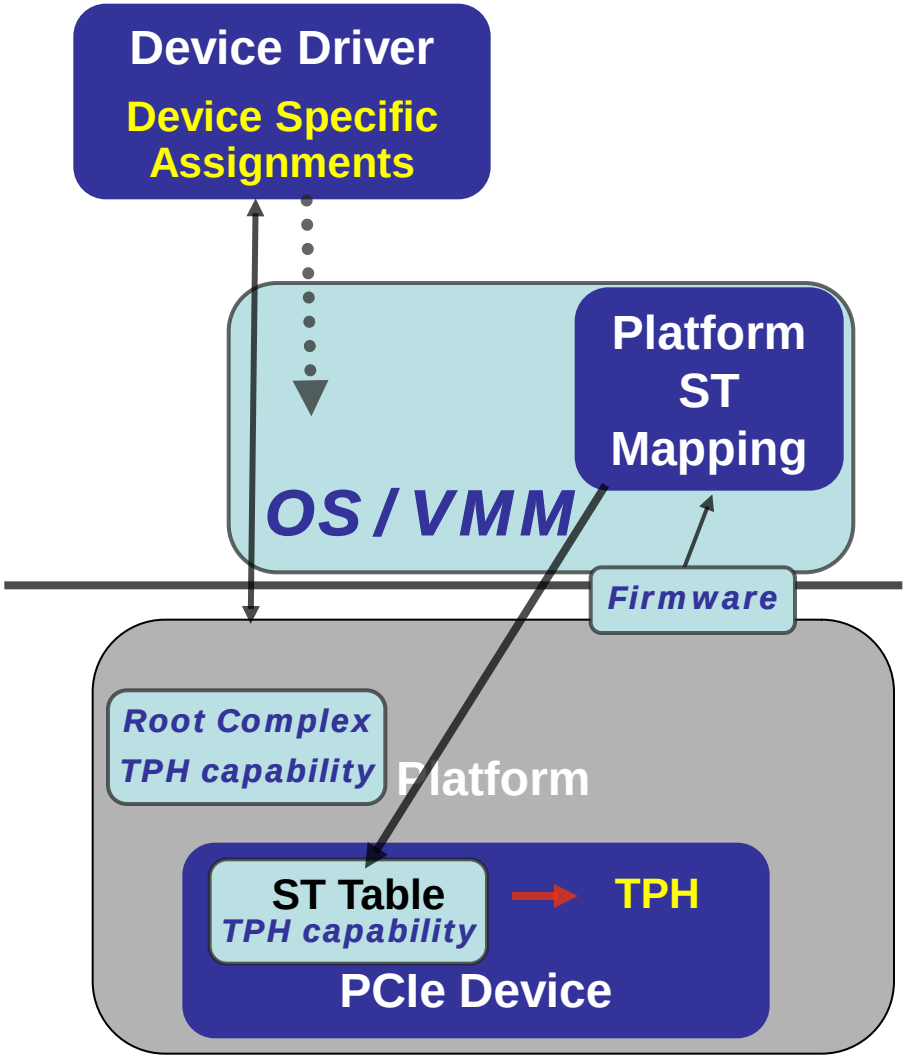
- *Platform support (Root Complex, Routing Elements)*
- *System specific Steering Tag advertisement*

Device Architecture

- *Characterize workloads*
- *Application processor Affinity*
- *Steering Tag to Workload association*
- *Select Modes of Operation*

Software Development

- *Basic Capability Discovery, Identification and Management*
- *System specific Steering Tag advertisement and assignment*
- *Device Driver enhancements*



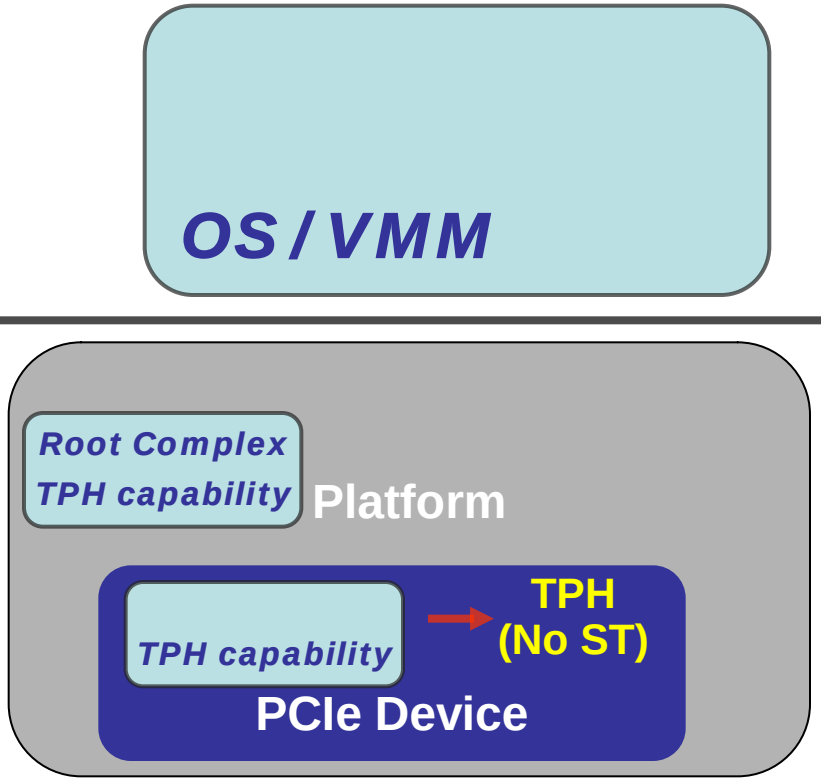
No ST Mode

No Steering Tags used

Request Steering is Platform Specific

Basic Capability Enablement

Minimal Implementation cost and complexity



Basic support

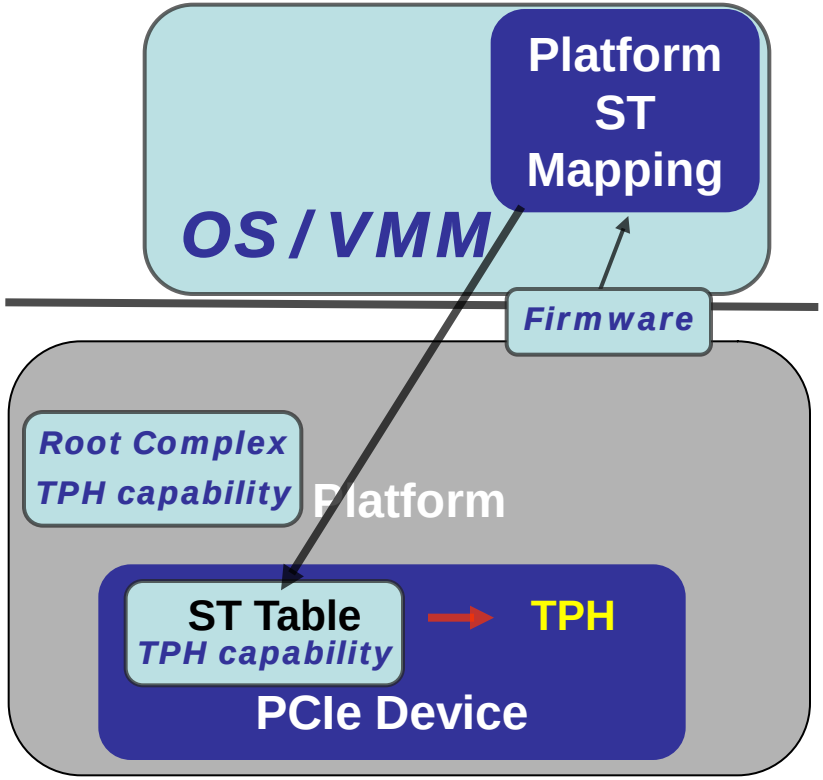
Interrupt Vector Mode

ST associated with Interrupt (MSI / MSI-X)

Firmware provides Platform specific ST information to OS / Hypervisor

OS / Hypervisor assigns ST along with Interrupt vector assignment

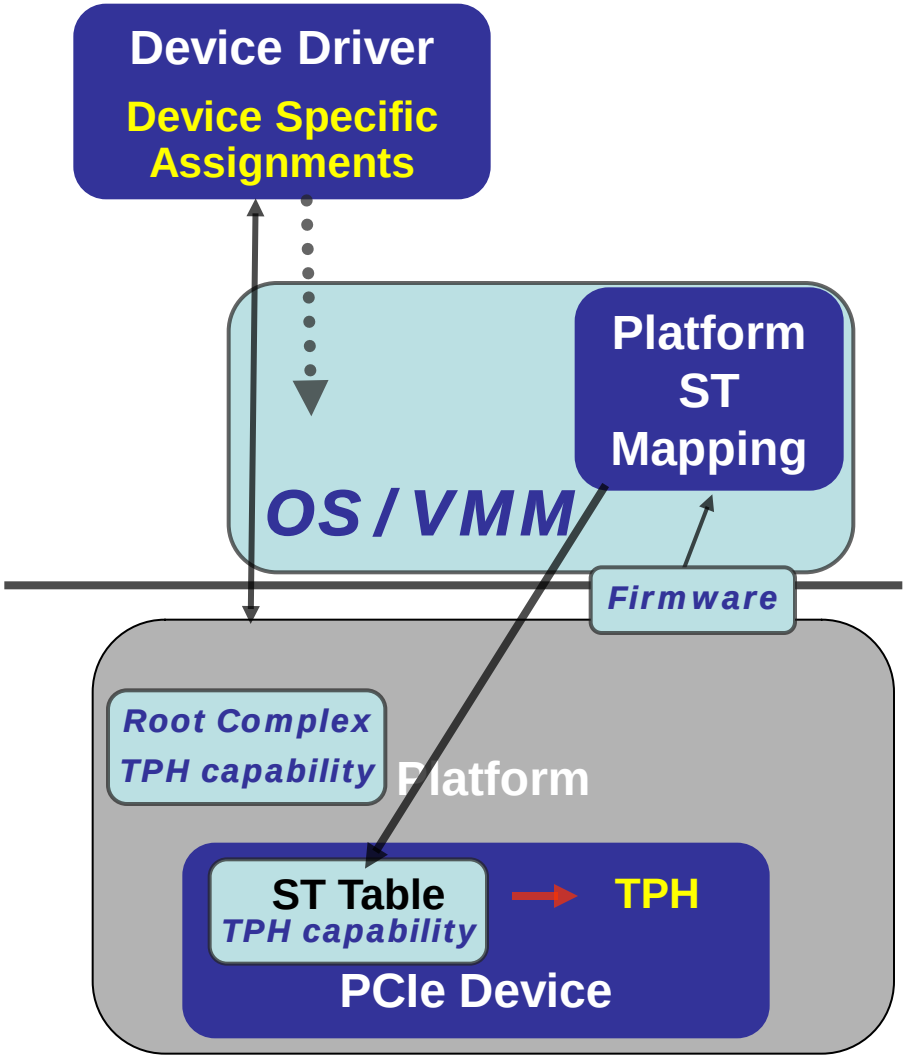
Suitable for devices with workload / Interrupt affinity to cores



TTM Advantage

Device Specific Mode

- Device Specific ST association
- Builds upon Interrupt vector mode s/w support
- Device Driver determines processor affinity
- New API required to request ST assignments
- Independent of Interrupt association



Scalable & Flexible Solution

TPH Aware Device Architecture

Classify device initiated transactions:

Bulk vs. Control

- **Select hints based on Data Struct. Use models**

Control Struct. (Descriptors)
Headers for Pkt. Processing
Data Payload (Copies)

Steering Tag Modes

- ✓ **No ST:** Basic Hints only, No ST used
- ✓ **Interrupt Vector Mode**: Faster TTM with Interrupt association
- ✓ **Device Specific Mode:** Scalable, Flexible & Dynamic, can provide TTM advantage

Software Development

- ✓ **Basic TPH Capability Identification, Discovery and Management**
- ✓ **Firmware Support to advertise ST assignments**
- ✓ **OS/Hypervisor ST assignment support**
- ✓ **Optional API support**

TPH permits Device Architecture Specific Trade-Offs

Device Architecture Considerations

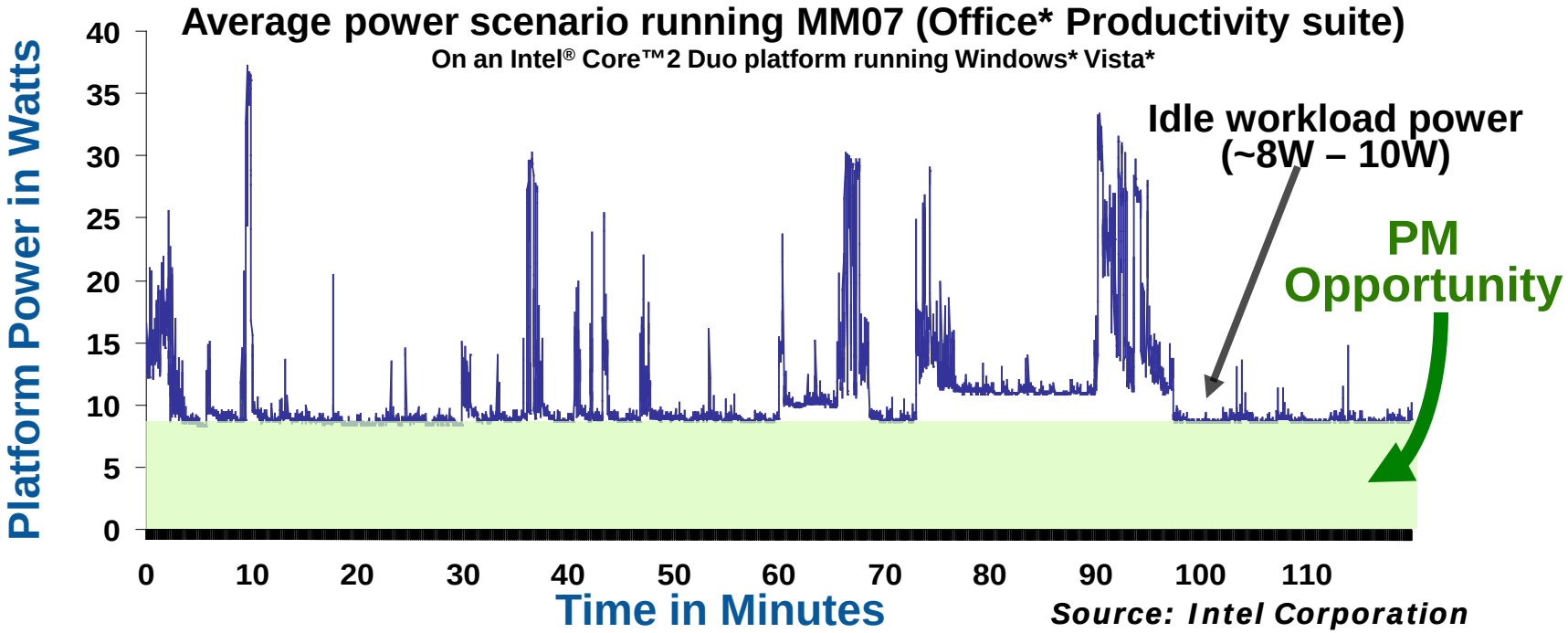
- TLP Processing Hints
- Power Management Extensions

System Perspective

- **Device behavior impacts power consumption of other system components**
  - Devices should consider their system power impact, not just their own device level power consumption
    - Extreme example: Enhanced Host Controller Interface (EHCI)
- **Systems (and devices) are idle most of the time**
  - There's a big opportunity for devices and systems to take advantage of that
- **Latency Tolerance Reporting (LTR) enables lower power, longer exit latency system power states *when devices can tolerate it***
- **Optimized Buffer Flush/Fill (OBFF) enables platform activity alignment, resulting in system power savings**

Opportunity for Devices to Differentiate on Platform Power Savings

Platform Power Savings Opportunity



- Usage Analysis: Typical mobile platform in S0 state is ~90% idle
- When idle, platform components are kept in high power state to meet the service latency requirements of devices & applications

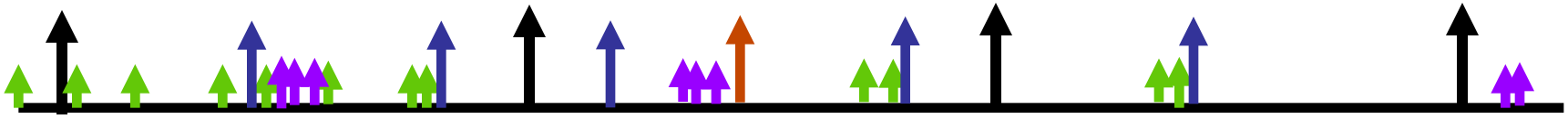
Power consumption for idle workload is high

Optimized Buffer Flush / Fill

- Next several foils describe:
  - Platform activity alignment
  - PCI Express* (PCIe*) OBFF mechanisms
  - OBFF within context of platform activity alignment
  - Device implementation impacts for OBFF

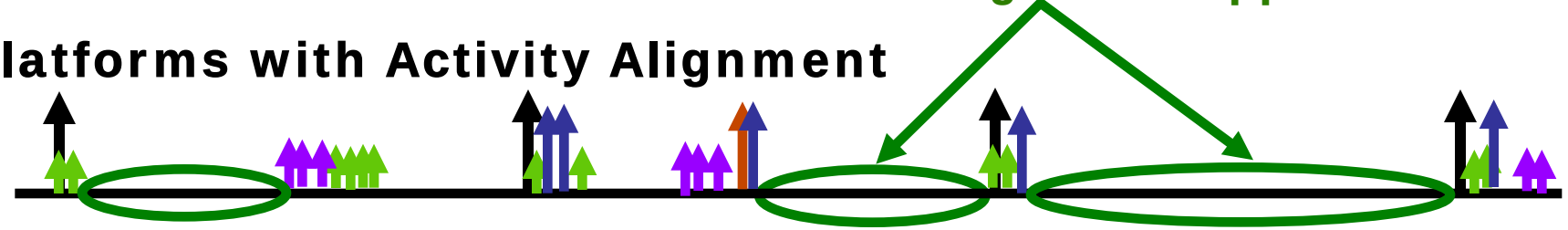
Platform Activity Alignment

Current Platforms



Power Management Opportunities

Platforms with Activity Alignment



OS tick inter-rupts

Device interrupts (critical)

- Time Critical
- Buffer replenish
- Performance / Throughput

Device interrupts (deferrable)

- Not time critical
- Status Notifications
- User Command Completions
- Debug, Statistics

Device traffic (critical)

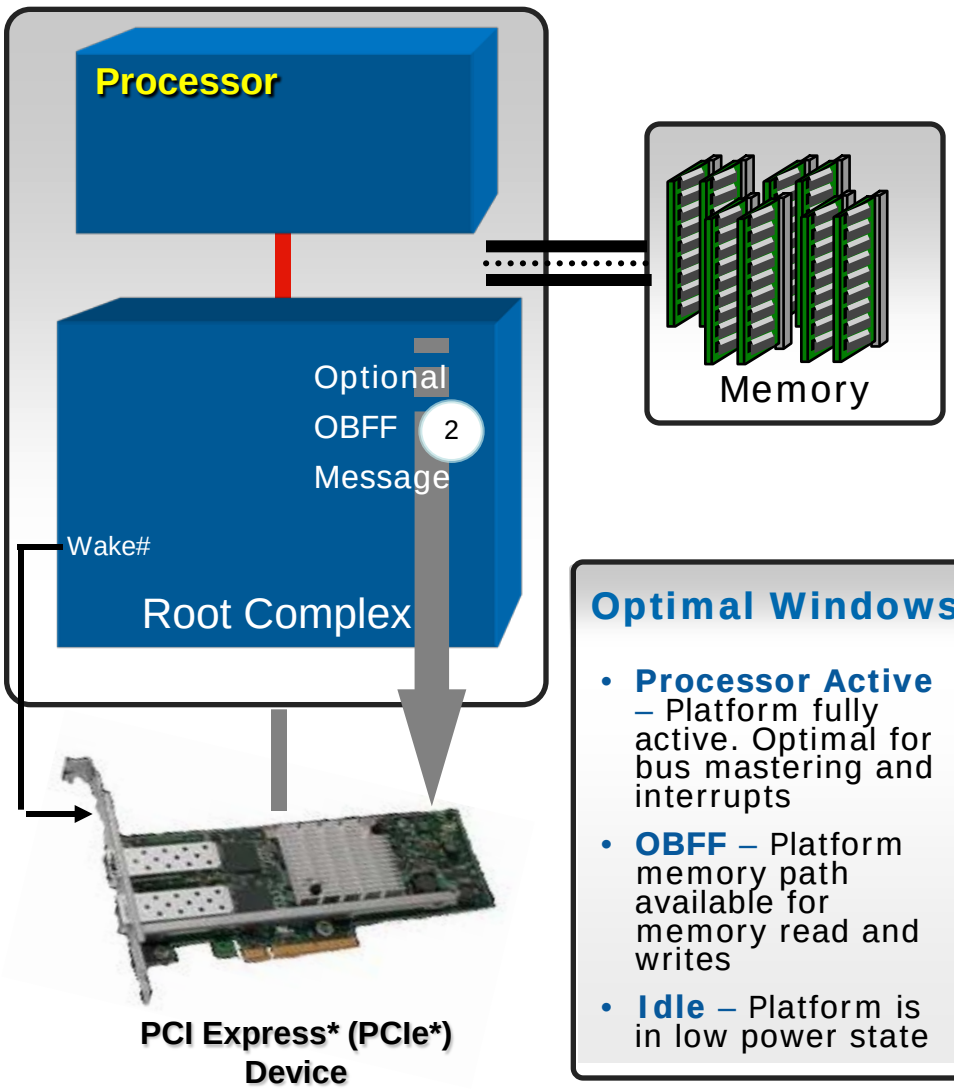
- Buffer over-(under-) run
- Throughput / Performance

Device traffic (deferrable)

- No Buffering constraints
- Debug dumps

Creates PM Opportunities for Semi-active workloads

Optimized Buffer Flush / Fill (OBFF)



OBFF

- Notify all Endpoints of optimal windows with minimal power impact

Solution1: When possible, use WAKE# with new wire semantics

Solution2: WAKE# not available – Use PCIe Message

Optimal Windows

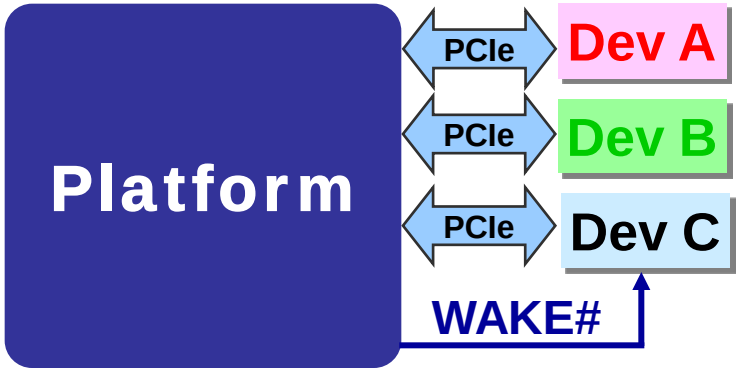
- **Processor Active** – Platform fully active. Optimal for bus mastering and interrupts
- **OBFF** – Platform memory path available for memory read and writes
- **Idle** – Platform is in low power state

WAKE# Waveforms

Transition Event	WAKE#
Idle → OBFF	
Idle → Proc. Active	
OBFF/Proc. Active → Idle	
OBFF → Proc. Active	
Proc. Active → OBFF	

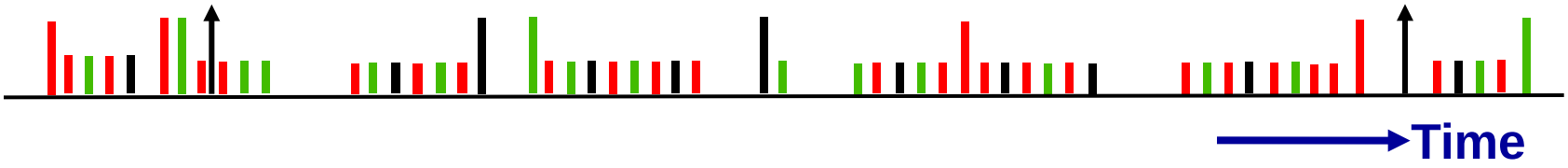
Greatest Potential Improvement When Implemented by All Platform Devices

OBFF and Activity Alignment

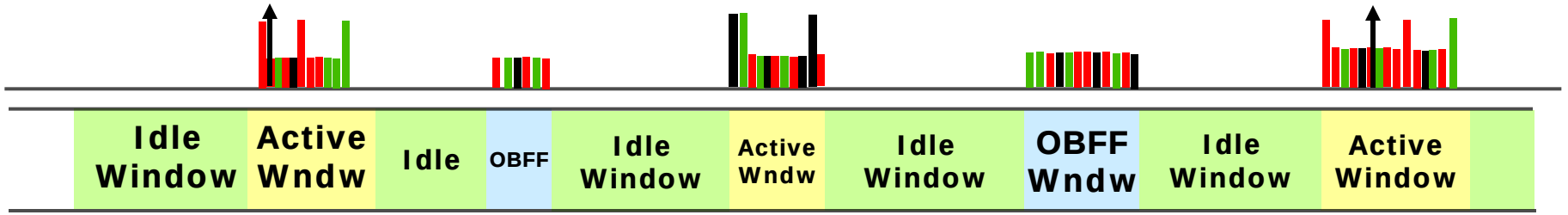


	Interrupts	DMAs
Device A		
Device B		
Device C		
OS Timer Tick (intrpt)		

Traffic Pattern with No OBFF



Traffic Pattern with OBFF



OBFF Device Implementation Impacts

Maximize idle window duration for platform

- Align transactions with other devices in system
- Coalesce transactions into groups where possible
  - Perform groups of transactions all at once, don't trickle all the time

Classify device initiated transactions: critical vs. deferrable

- Perform critical transactions as necessary
- Defer other transactions to align with platform activity
  - Decode platform idle / active / OBFF window signaling

Select data buffer depths to tolerate platform activity alignment

- 300µs of deferral buffering recommended for Intel mobile platforms

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Latency Tolerance Reporting

- The next several foils describe:
  - Power vs. response latency
  - PCI Express* (PCIe*) LTR mechanisms, semantics
  - Examples of device implementation schemes
    - Application state driven LTR reporting
    - Data buffer depth driven LTR reporting
    - Software guided LTR reporting
  - Device implementation impact summary for LTR

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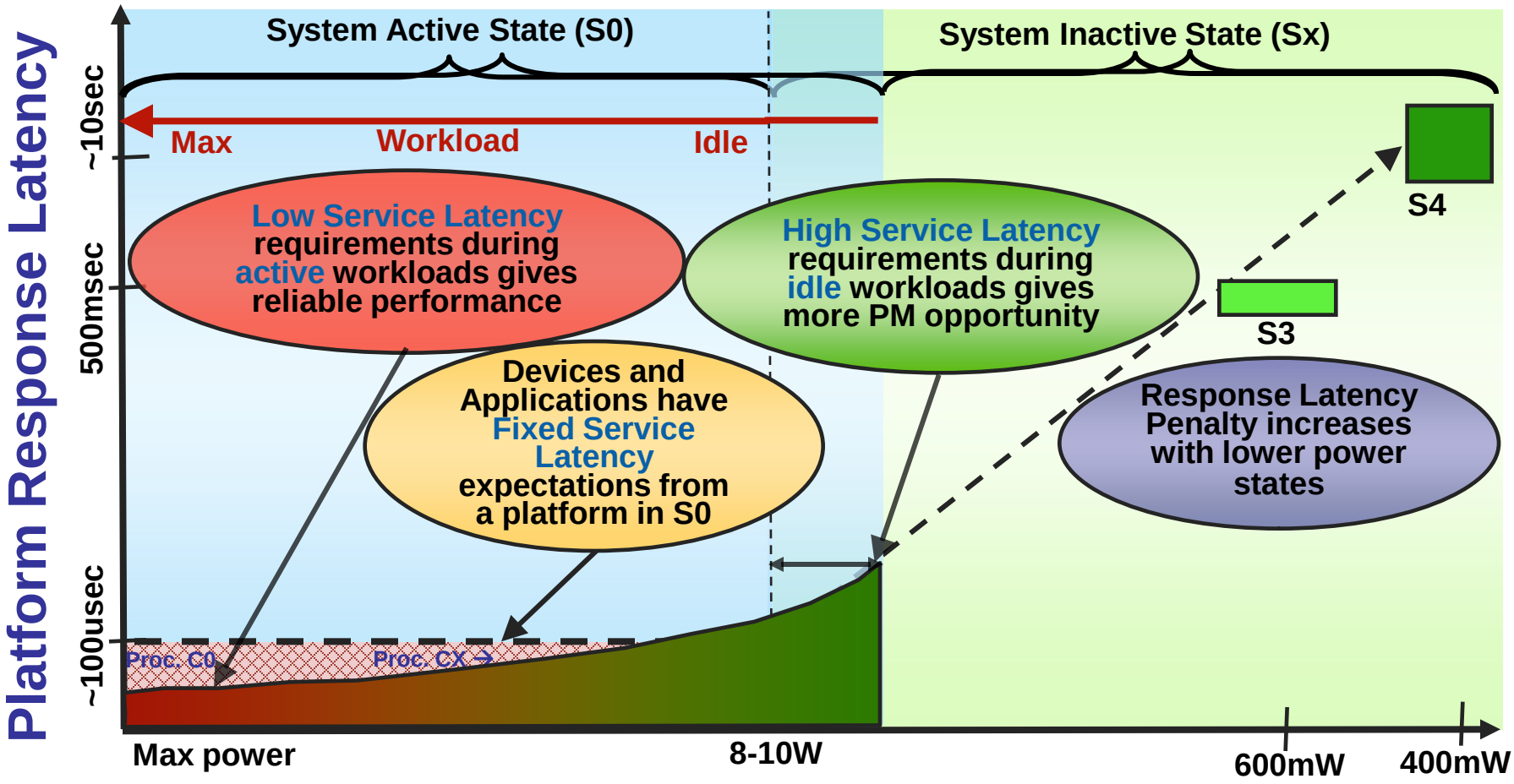
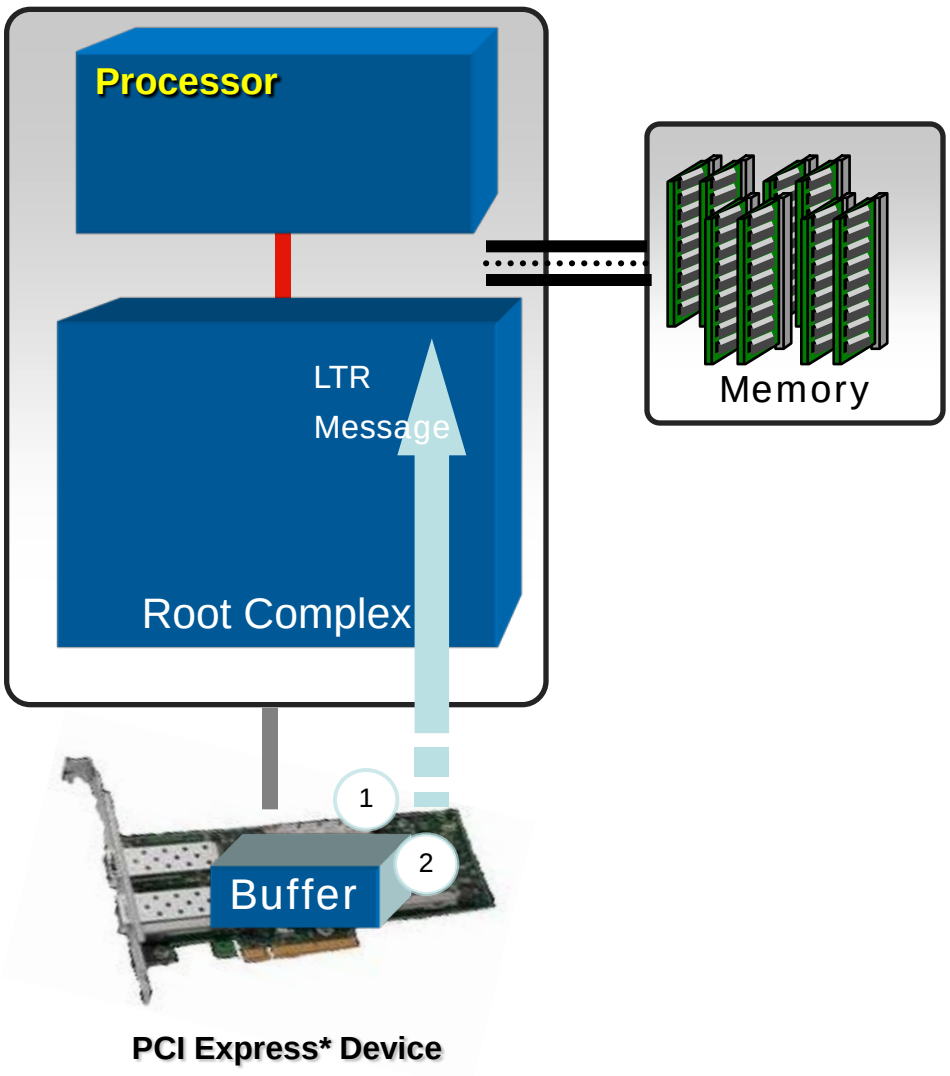
Power Vs Response Latency (Mobile)



Variable Service Latency requirements in S0 is Optimal

Latency Tolerance Reporting (LTR)



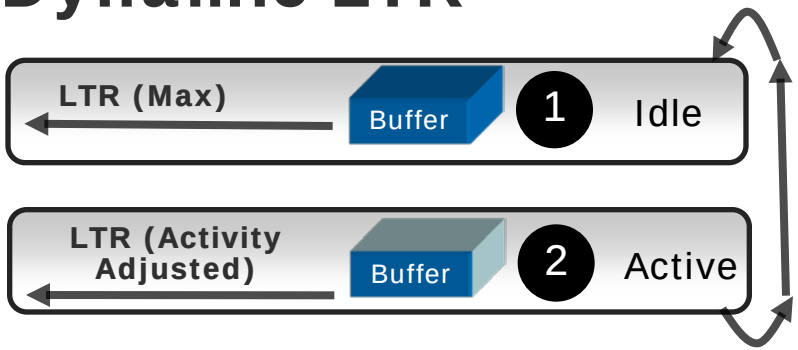
LTR Mechanism

- PCI Express* (PCIe*) Message sent by Endpoint with tolerable latency
  - Capability to report both snooped & non-snooped values
  - "Terminate at Receiver" routing, MFD & Switch send aggregated message

Benefits

- Provides Device Benefit: Dynamically tune platform PM state as a function of Device activity level
- Platform benefit: Enables greater power savings without impact to performance/functionality

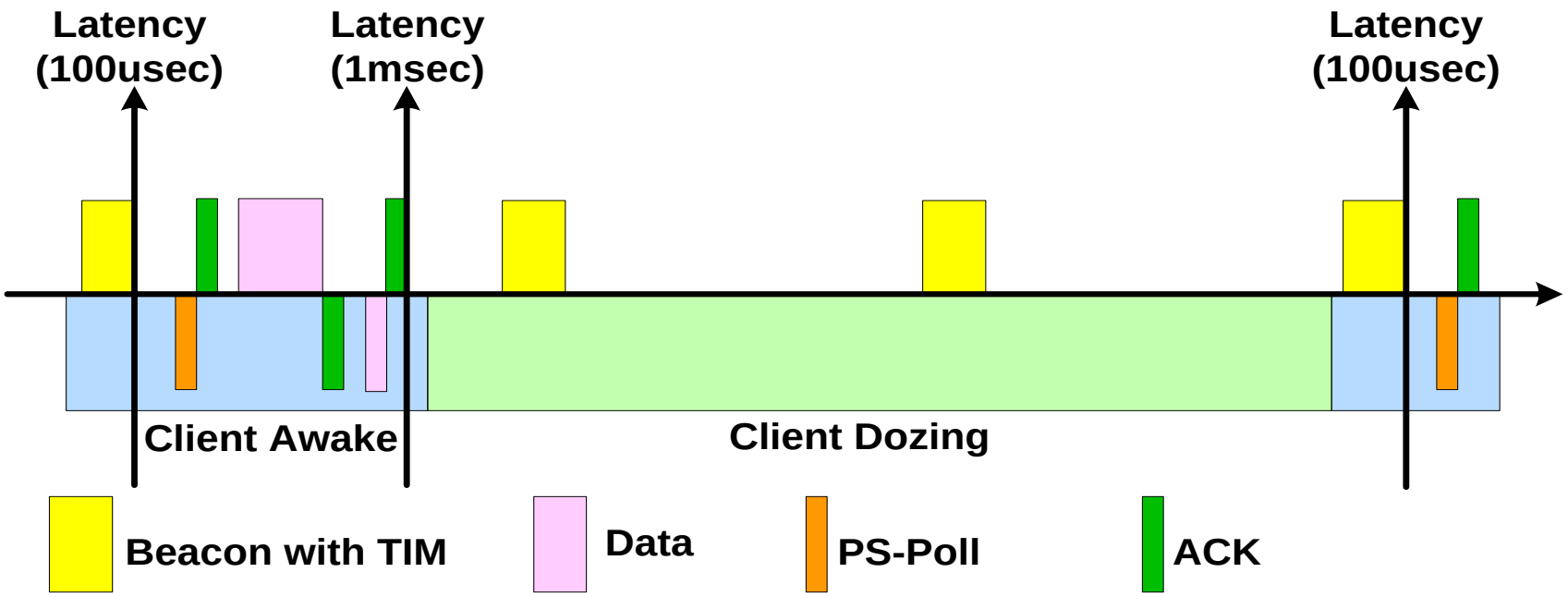
Dynamic LTR



LTR enables dynamic power vs. performance tradeoffs at minimal cost impact

Application State Driven LTR

Example: WLAN Device Sending LTR

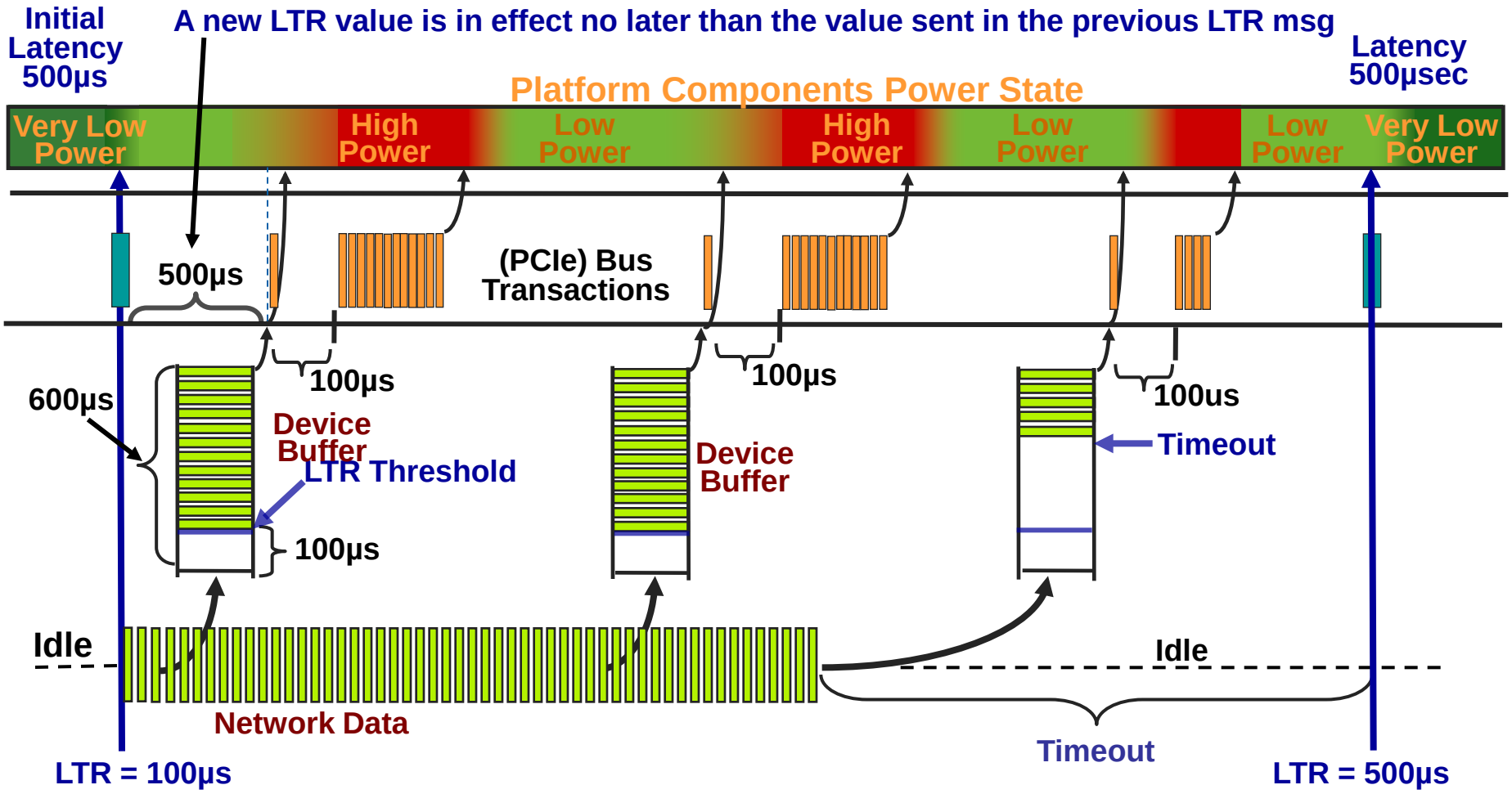


Latency information with Wi-Fi Legacy Power Save

Example use of device PM states to give latency guidance

Data Buffer Utilization Guided LTR

Example: Active Ethernet NIC Sending LTR

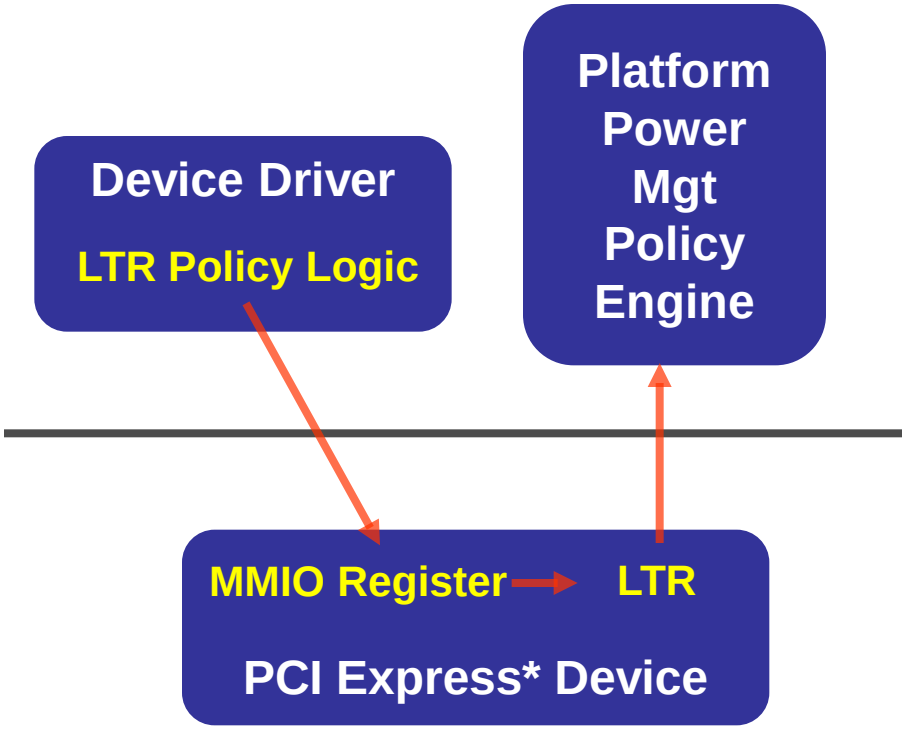


Example use of buffering to give latency guidance

Software Guided Latency

SW Guided Latency

- Three device categories
  - ✓ **Static:** Device can always support max platform latency
  - ✓ **Slow Dynamic**: Latency requirements change infrequently
  - ✓ **Fast Dynamic:** Latency requirements change frequently
- Static and Slow Dynamic types of devices may choose SW guided messaging
  - ✓ Policy logic for determination of when to send latency messages (and what values) in software
  - ✓ E.g. use an MMIO register
    - ➢ A write to the register would trigger an LTR message



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LTR Device Implementation Impacts

When idle, let platform enter deep power saving states

- Use MaxLatency (LTR Extended Capabilities field) when idle
- Require low latencies only when necessary – don't keep platform in high power state longer than necessary

Dynamic, hardware driven LTR

- Leverage application based opportunities to tolerate more latency
  - E.g. WLAN radio off between beacons
- Implement data buffering mechanism to comprehend LTR

Software guided LTR

- Implement simple MMIO register interface
  - Register writes cause LTR message to be sent

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Software Enabling

Features requiring basic software support

Capability Discovery, Identification and Management

- 8GT/s speed upgrade
- Atomics
- Transaction Ordering Relaxations
- Internal Error Reporting
- TLP Prefix

Features requiring additional support

Above and beyond capability enablement

Resource Allocation, Enumeration & API

- Transaction Processing Hints
- LTR & OBFF
- Resizable BAR
- IO Page Faults
- Dynamic Power Allocation
- Multicast

Summary

- Next Generation PCI Express* (PCIe*) Protocol Extensions Deliver Energy Efficient Performance
  - Protocol Extensions with Broad Applicability
- Ecosystem Development is essential
  - Platform Support
  - Device architectures optimized around protocol features
  - Software support and Enabling

Call to Action

- Device Architecture Considerations
  - Develop Device Architecture to make the most of the most of proposed protocol extensions
- Differentiate products utilizing TPH
  - Select Hints/ST modes based on device/market segment requirements
- Differentiate products utilizing LTR and OBFF
  - Can differentiate by platform power impact not just device power
  - Power Savings opportunity is huge
- Keep track of Next Generation PCI Express* Technology development
  - PCI-SIG www.pcisig.com
- Engage with Intel on Next Generation PCI Express product development
  - www.intel.com/technology/pciexpress/devnet

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Additional Sources of Information on This Topic

- Other Sessions
  - **TSIS007** –PCI Express* 3.0 Technology: PHY Implementation Considerations on Intel Platforms
  - **TSIS008** – PCI Express* 3.0 Technology: Electrical Requirements for Designing ASICs on Intel Platforms
  - **TCIQ002:** Q&A: PCI Express* 3.0 Technology

- www.intel.com/technology/pciexpress/devnet

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