High-Performance 40nm Gate Length InSb P-Channel Compressively Strained Quantum Well Field Effect Transistors for Low-Power (V_{CC}=0.5V) Logic Applications

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Outline

- Motivation
- Materials
- Transistors
- Benchmarking
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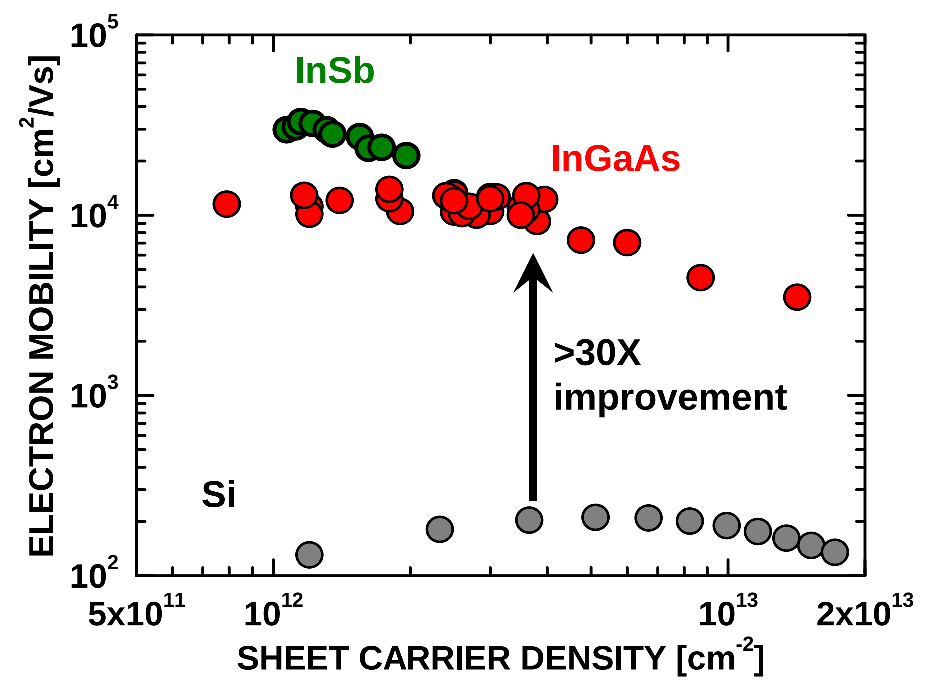
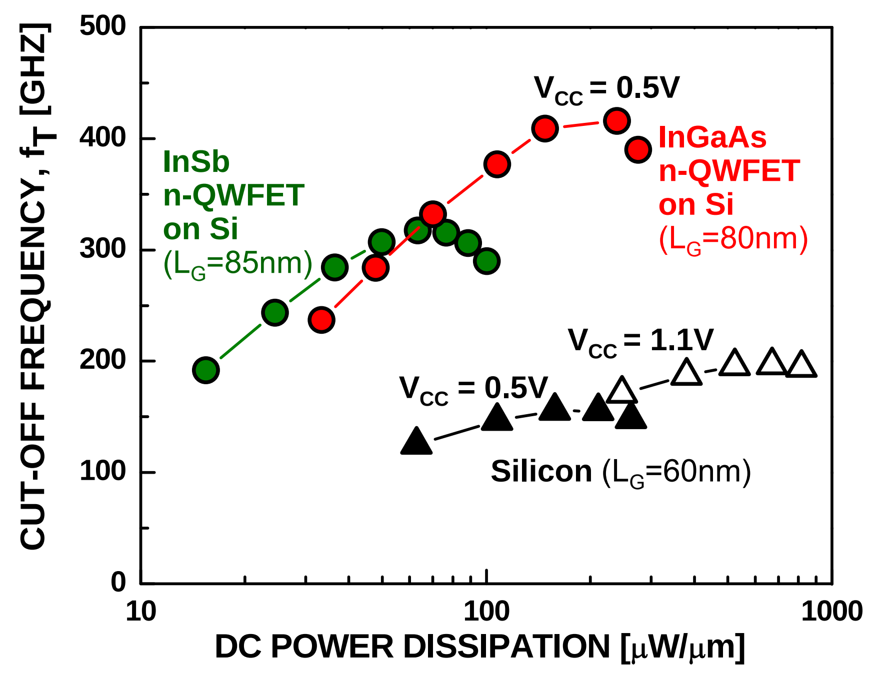
Advantages of III-V n-QWFETs for Low V_{CC} Logic (e.g. 0.5V)

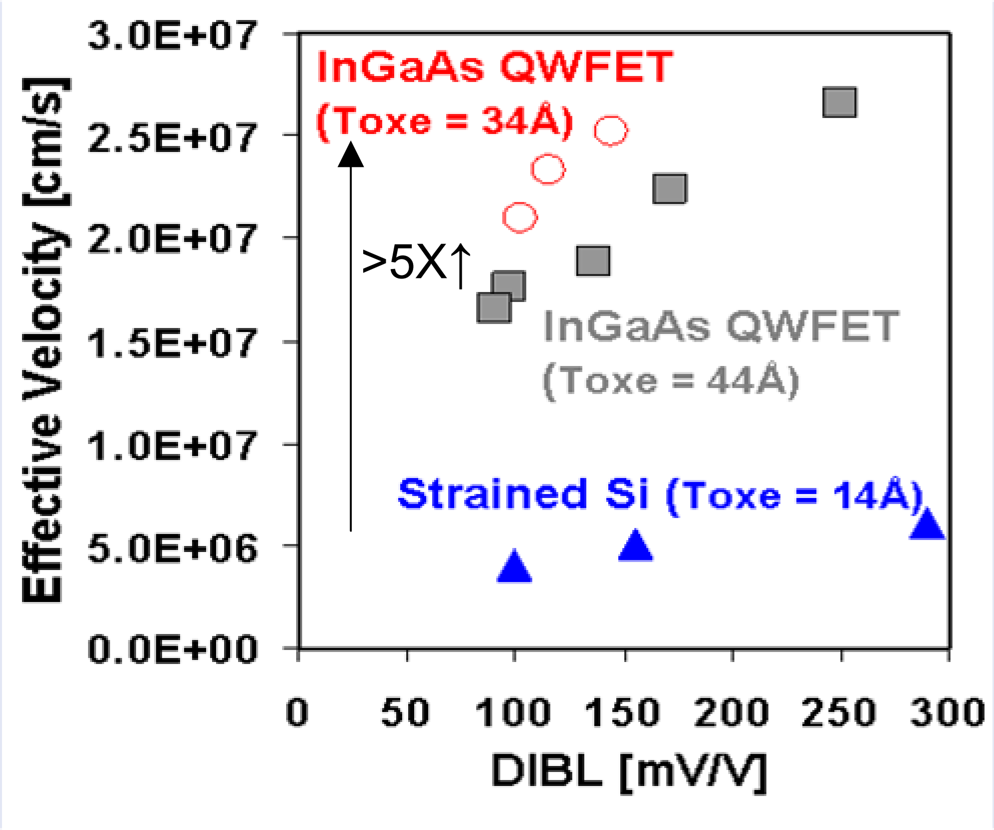




- III-V n-channel has >30X higher electron mobility over Si
- III-V on Si achieves f_T > 400GHz at V_{CC}=0.5V

Advantages of III-V n-QWFETs for Low V_{CC} Logic (e.g. 0.5V)

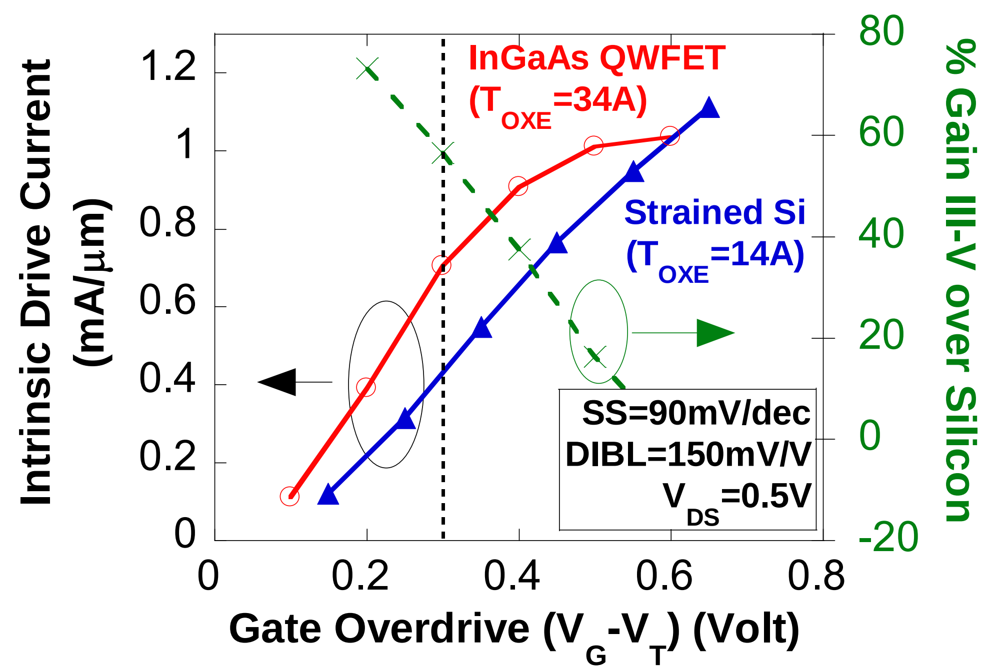
Measurement Data at V_G-V_T=0.3V



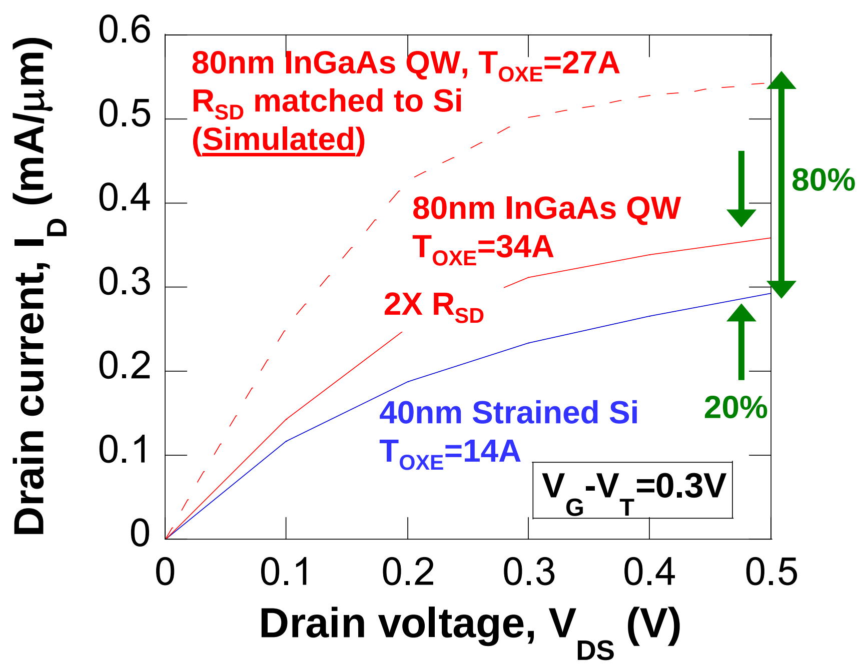
- **Veff=Gmi/Cgi, extracted from RF measurements**
- **Further improvement in Veff via shorter gate-to-QW separation and continued L_G scaling**

Advantages of III-V n-QWFETs for Low V_{CC} Logic (e.g. 0.5V)

Experimental Data:



Experiment & Simulation:



- Intrinsic drive current = (q*Veff * n_S)
- At V_G - V_T = 0.3V, III-V shows >50% gain in intrinsic drive current over Si
- Measured I_{DSAT} gain in current devices >20% over Si

Advantages of III-V n-QWFETs for Low V_{CC} Logic (e.g. 0.5V)

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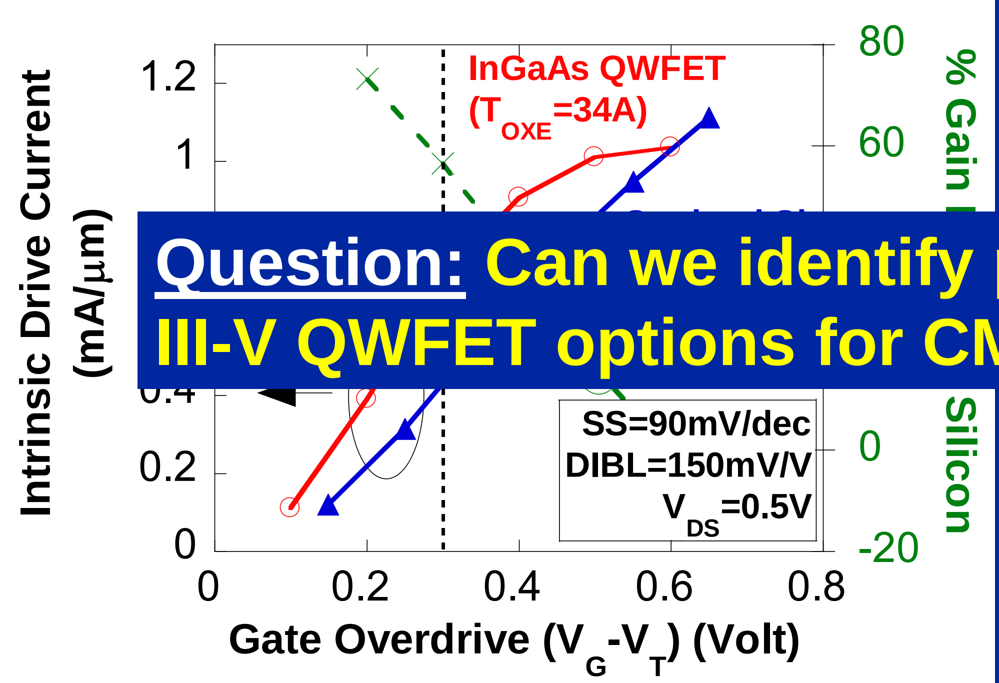
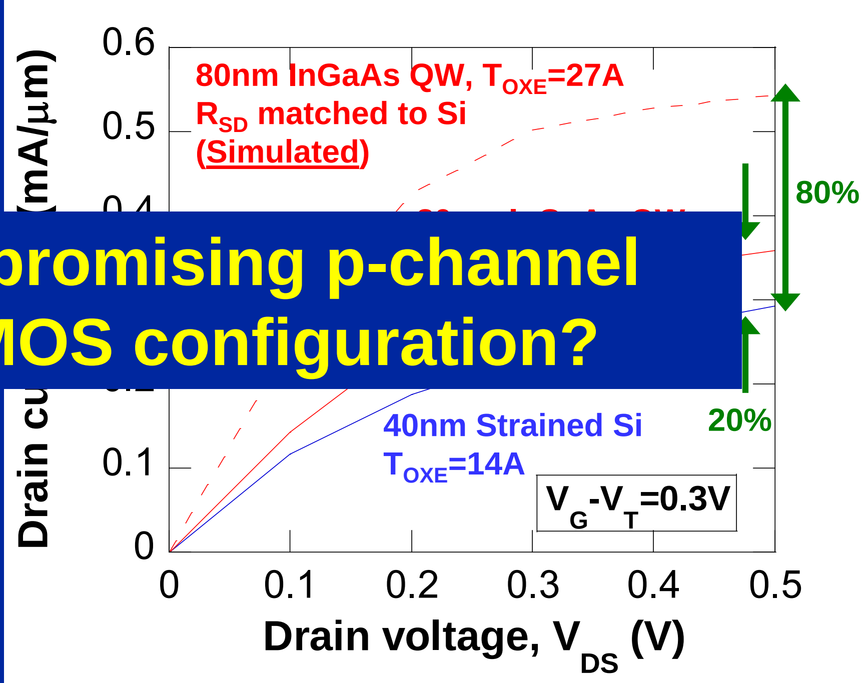
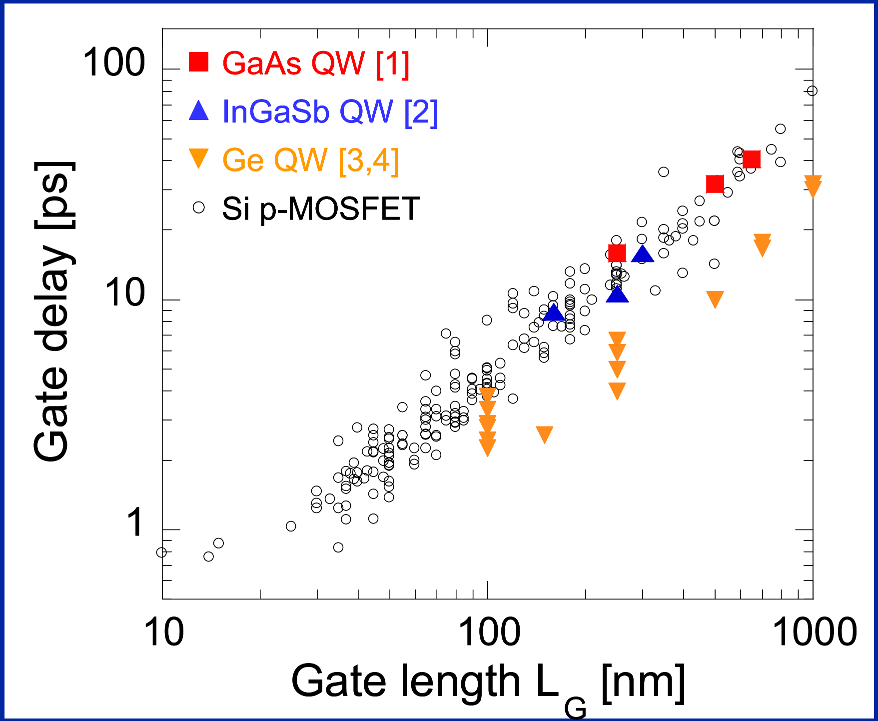


Experiment & Simulation:



Question: Can we identify promising p-channel III-V QWFET options for CMOS configuration?

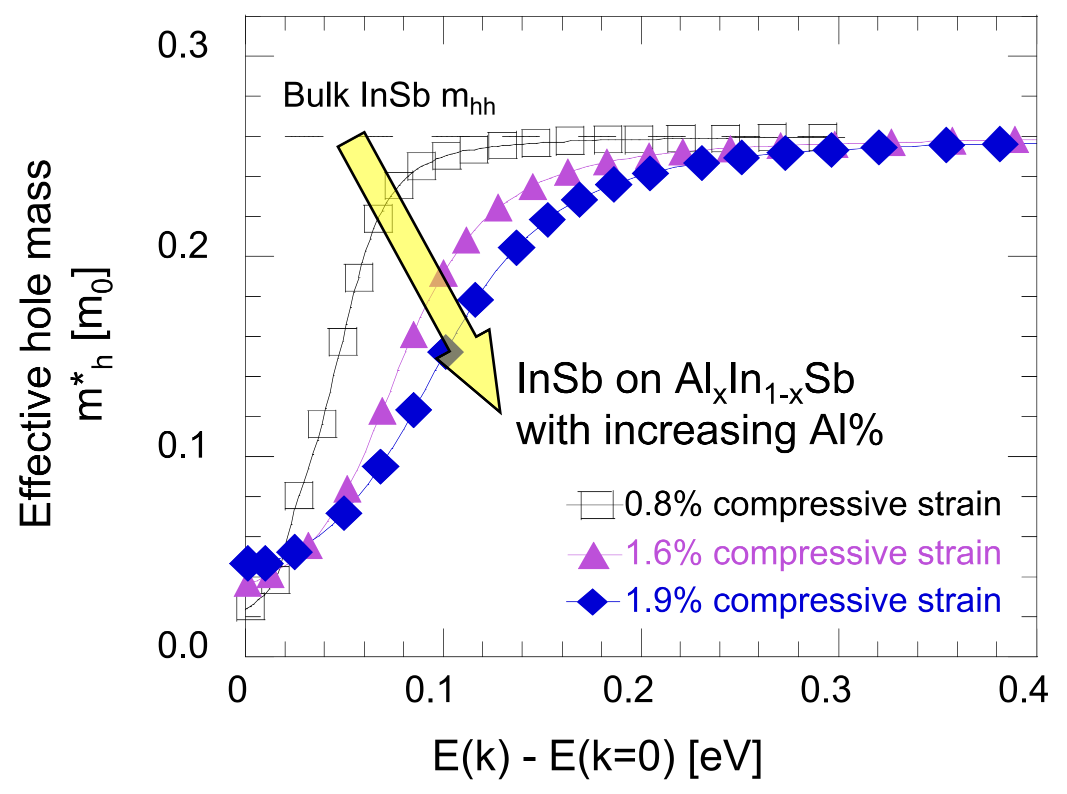
P-channel QW Materials Options



- Ge p-QWFET is an option under investigation
  - ❑ Parallel conduction is a major issue
- Existing III-V p-QWFET data matched to Si at best
  - ❑ Can p-channel performance in III-V be improved?
  - ❑ InSb has highest hole mobility in III-V

[1] Park, Proc. IEEE 1989; [2] Boos, EL 2007;
[3] Koester, EDL 2000; [4] Arafa, EDL 1996.

Enhancing InSb Hole Mobility via Biaxial Compressive Strain



- **K.P simulations show that biaxial compressive strain significantly reduces in-plane hole effective mass in InSb**

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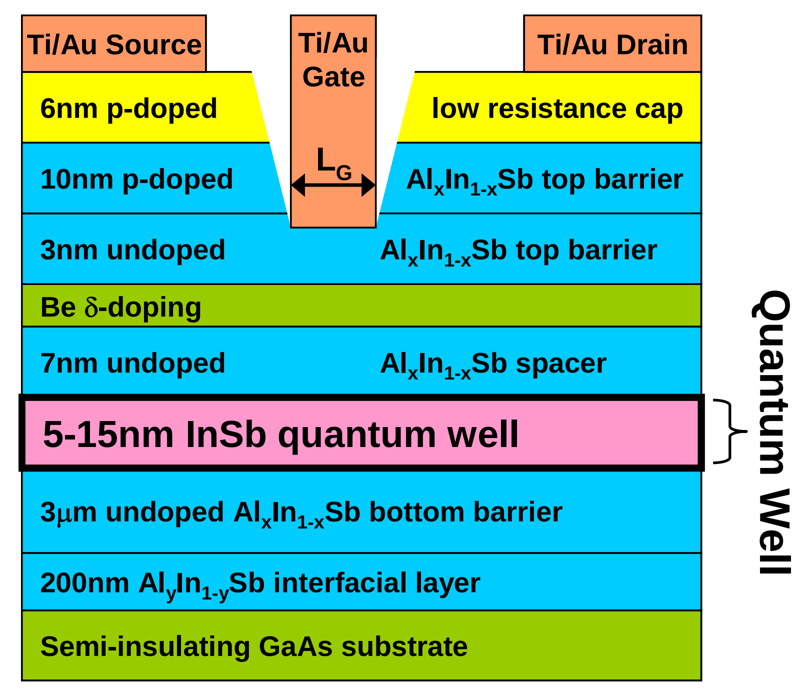
InSb Quantum Well Device Structure



Ti/Au Source

Ti/Au Gate

Ti/Au Drain

6nm p-doped — low resistance cap

L_G

10nm p-doped — $Al_xIn_{1-x}Sb$ top barrier

3nm undoped — $Al_xIn_{1-x}Sb$ top barrier

Be δ-doping

7nm undoped — $Al_xIn_{1-x}Sb$ spacer

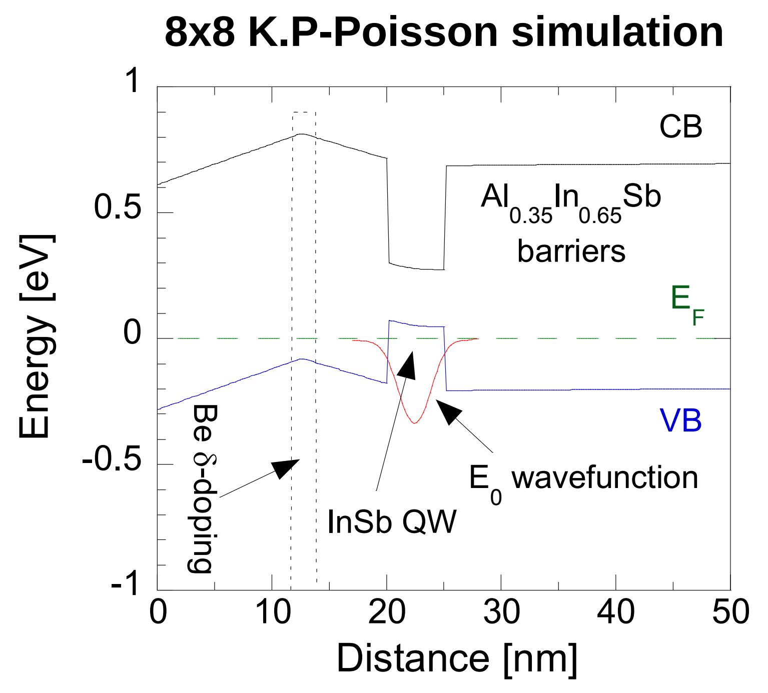
5-15nm InSb quantum well

3µm undoped $Al_xIn_{1-x}Sb$ bottom barrier

200nm $Al_yIn_{1-y}Sb$ interfacial layer

Semi-insulating GaAs substrate

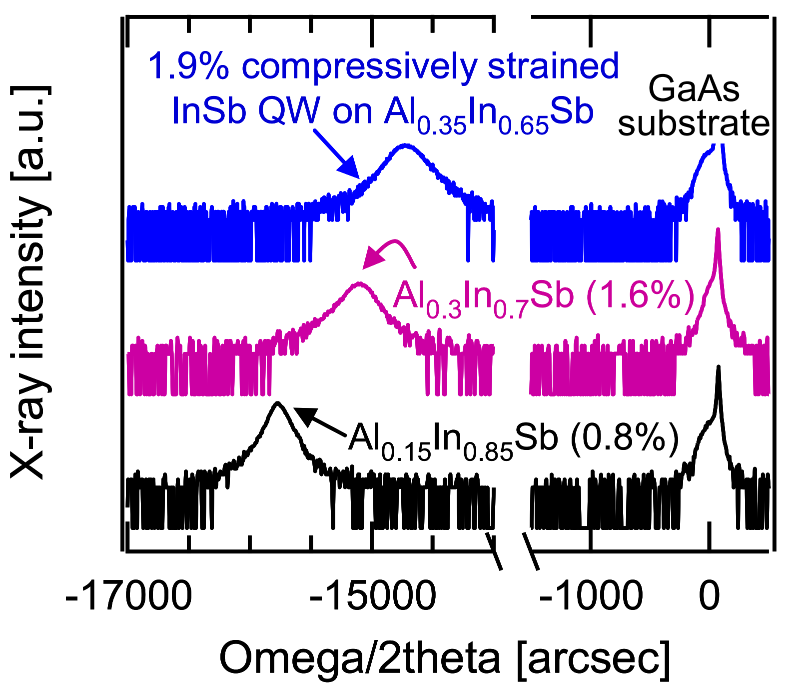
Quantum Well

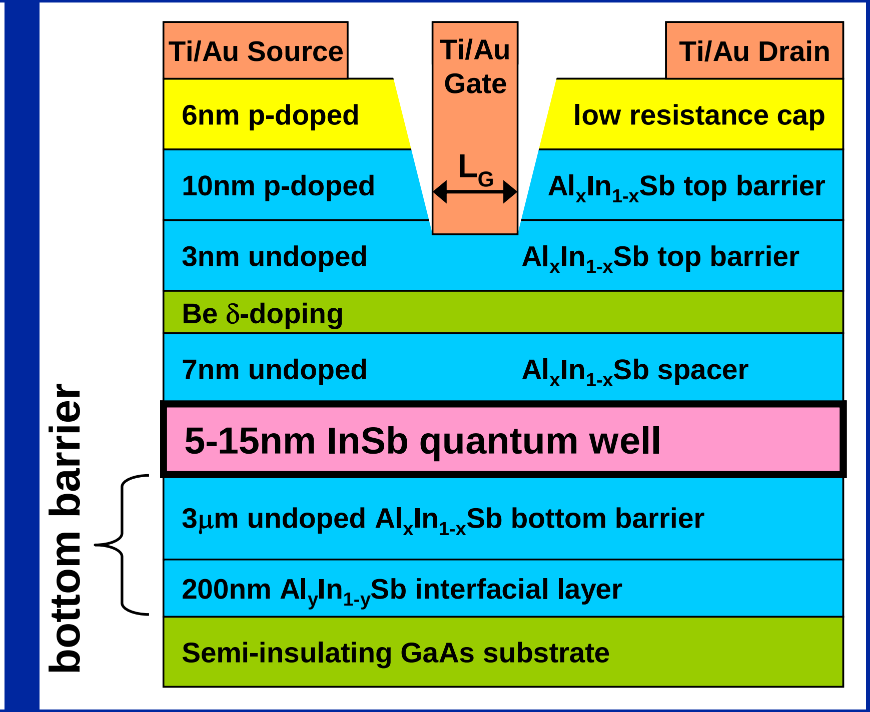


8x8 K.P-Poisson simulation

- Simulations indicate hole confinement in InSb QW
- Remote doping is utilized to reduce Coulomb scattering
- Larger biaxial strain requires reduction in QW thickness

Modulating Biaxial Compressive Strain in InSb Quantum Well Device Structure





6nm p-doped | low resistance cap

10nm p-doped | $Al_xIn_{1-x}Sb$ top barrier

3nm undoped | $Al_xIn_{1-x}Sb$ top barrier

Be δ-doping

7nm undoped | $Al_xIn_{1-x}Sb$ spacer

5-15nm InSb quantum well

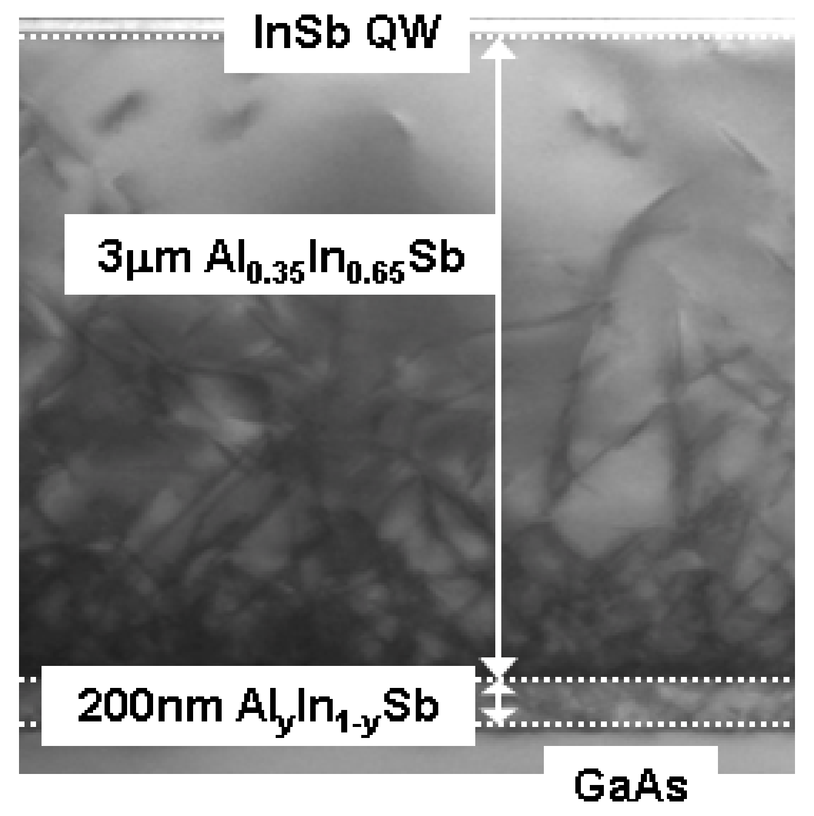
3μm undoped $Al_xIn_{1-x}Sb$ bottom barrier

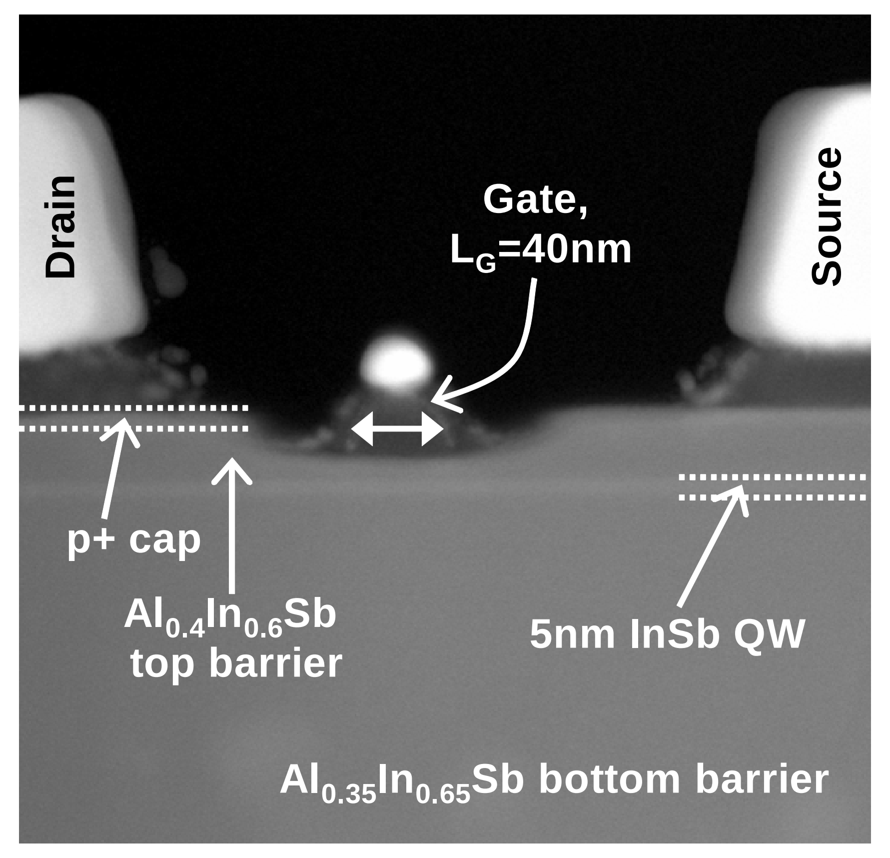
200nm $Al_yIn_{1-y}Sb$ interfacial layer

Semi-insulating GaAs substrate

- **XRD validates the full relaxation of bottom barrier layers**
- **Resulting biaxial compressive strain in QW is increased with increasing Al%**

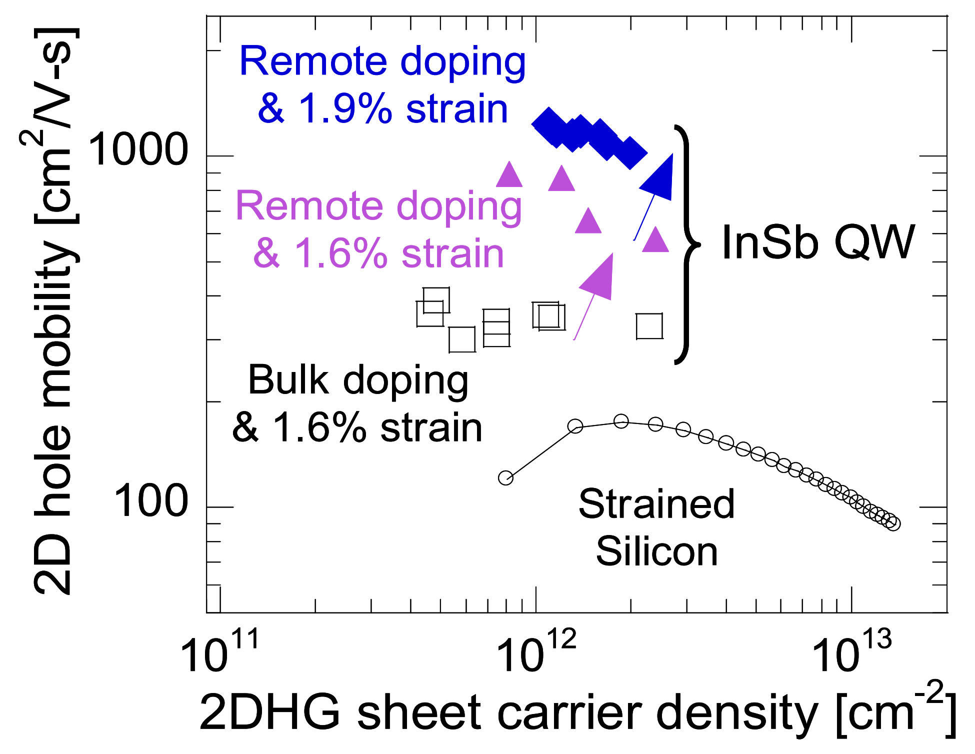
XTEM Micrographs of InSb QW Device Structure





- 5nm QW with 1.9% biaxial compressive strain

Mobility of InSb p-QW Device Structure



- **Mobility improves with increased biaxial compressive strain and remote doping**
- **Highest p-QW device structure mobility:**

  μ=1230cm^2/V-s at n_s=1.1e12/cm^2
- **InSb QW hole mobility is 5X higher than strained Si**

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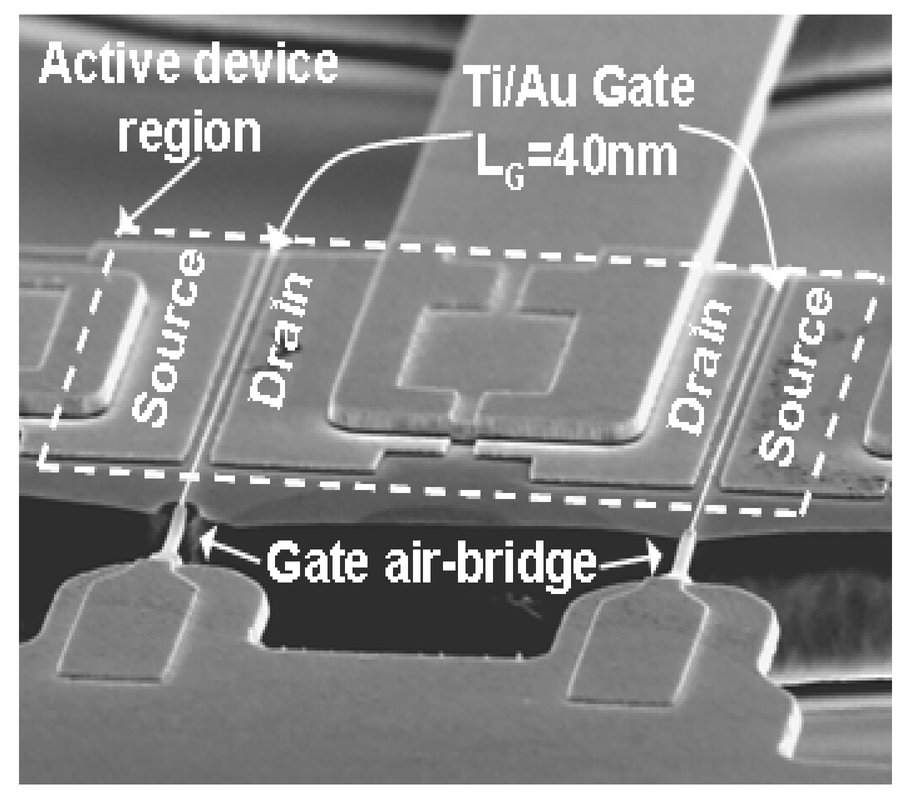
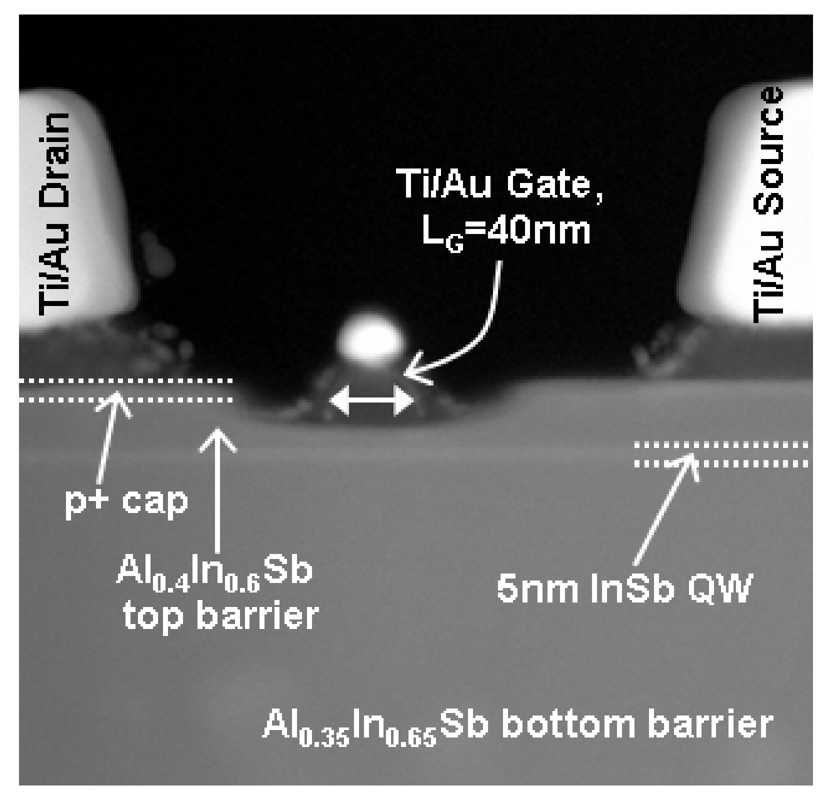
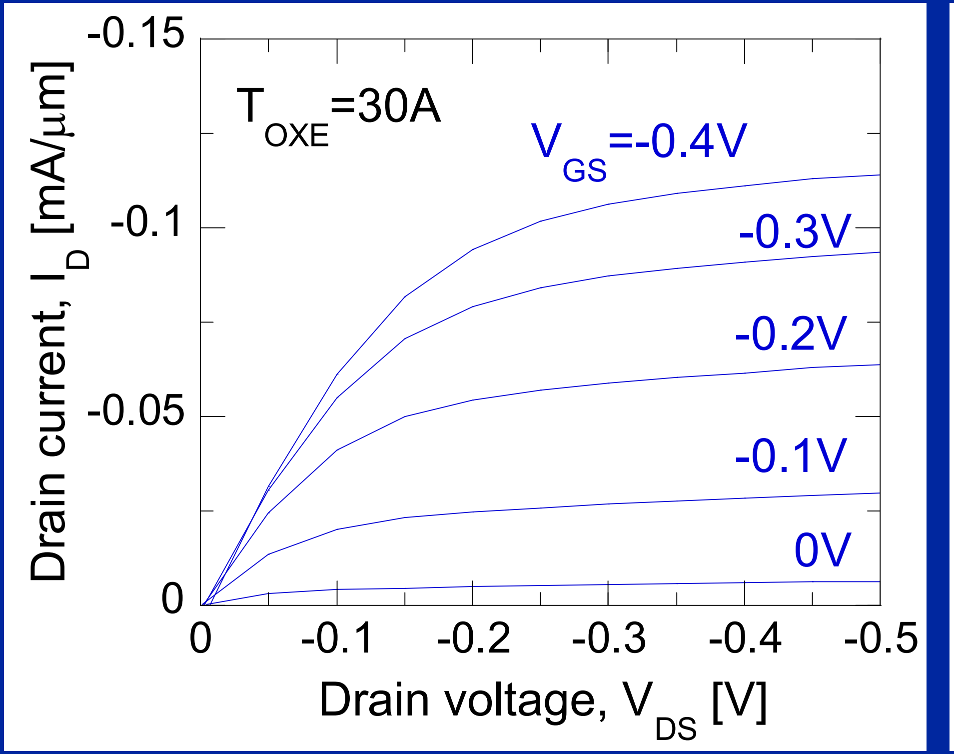
InSb p-QWFET Fabrication

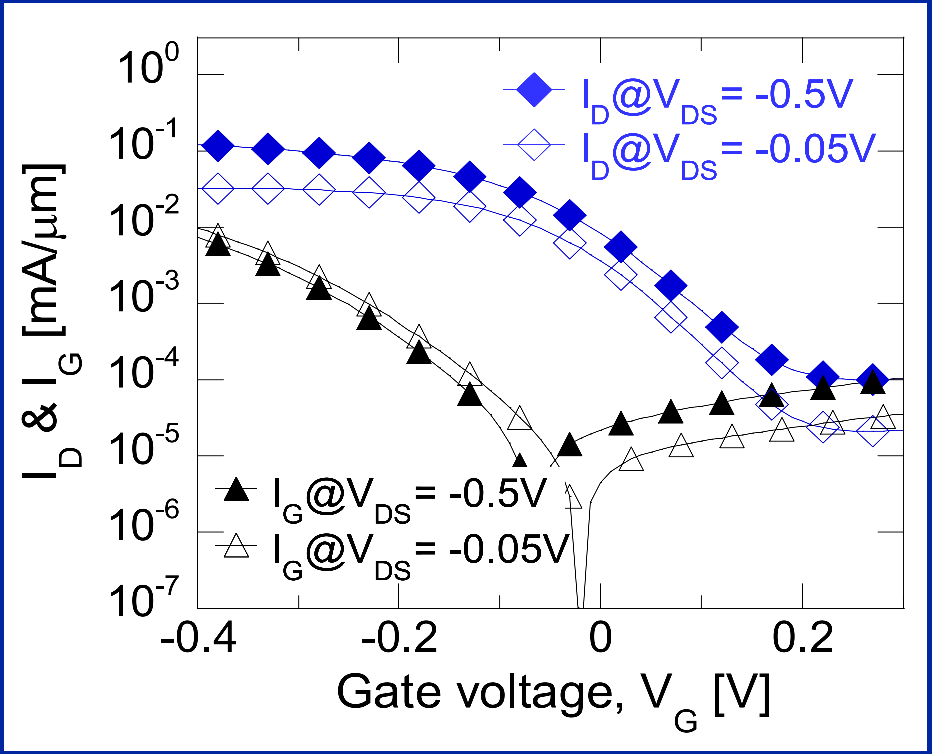




- **A two gate finger InSb QWFET is fabricated with gate air-bridge using mesa isolation**
- **L_G=40-125nm fabricated with recess etch Schottky gate**
- **Gate-to-QW separation in SiO_2 equivalent thickness, T_{OXE} = 30A at V_G-V_T= -0.3V**

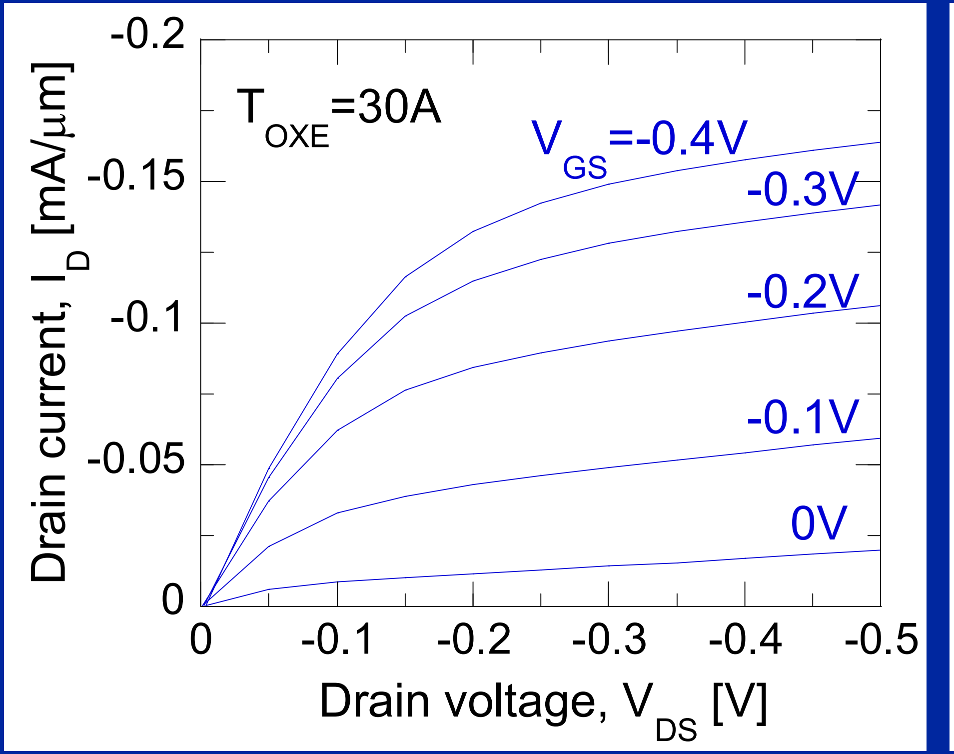
InSb p-QWFET L_G=125nm

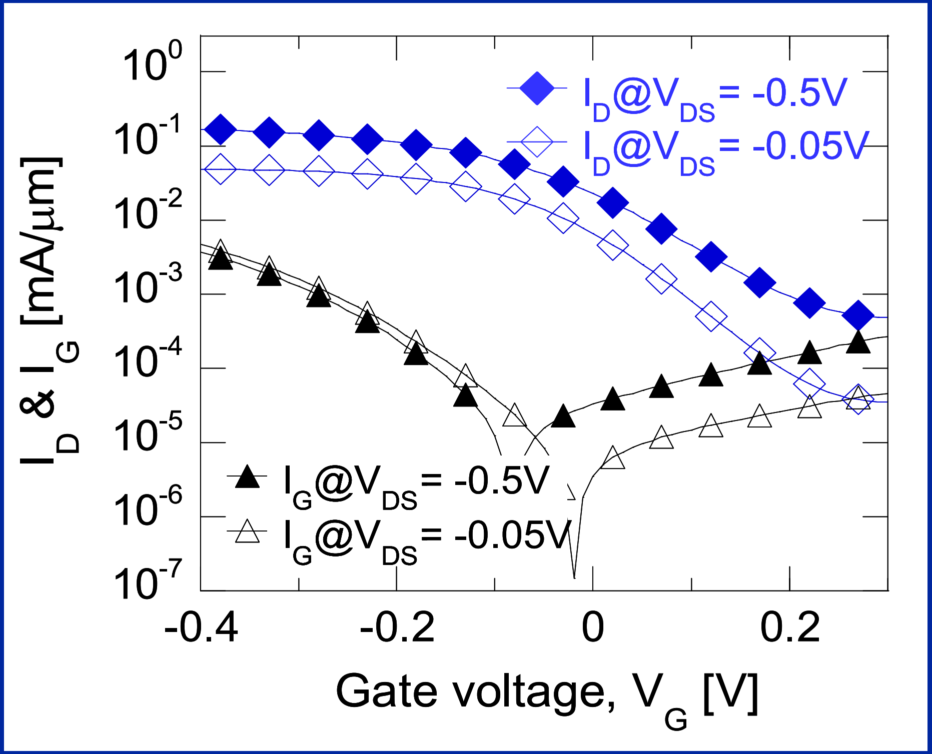




- **L_G=125nm device has SS =90mV/dec, and DIBL =80mV/V**
- **I_{ON}/I_{OFF} > 700 at V_{DS}= -0.5V with 0.5V V_G swing**

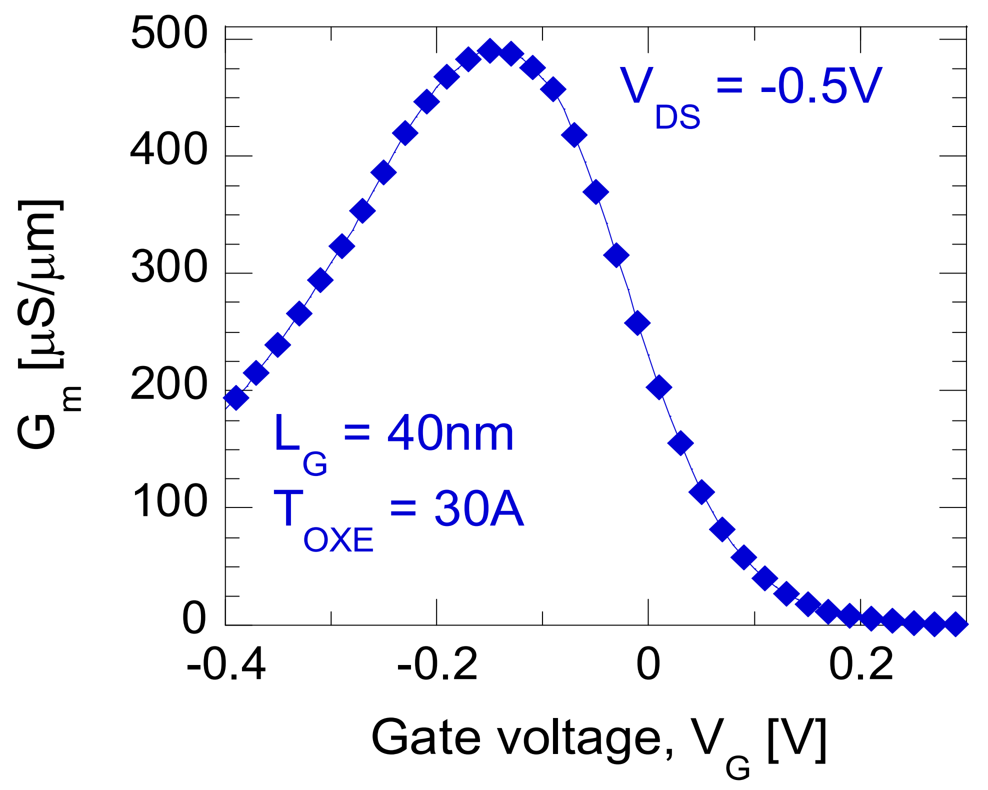
InSb p-QWFET L_G=40nm





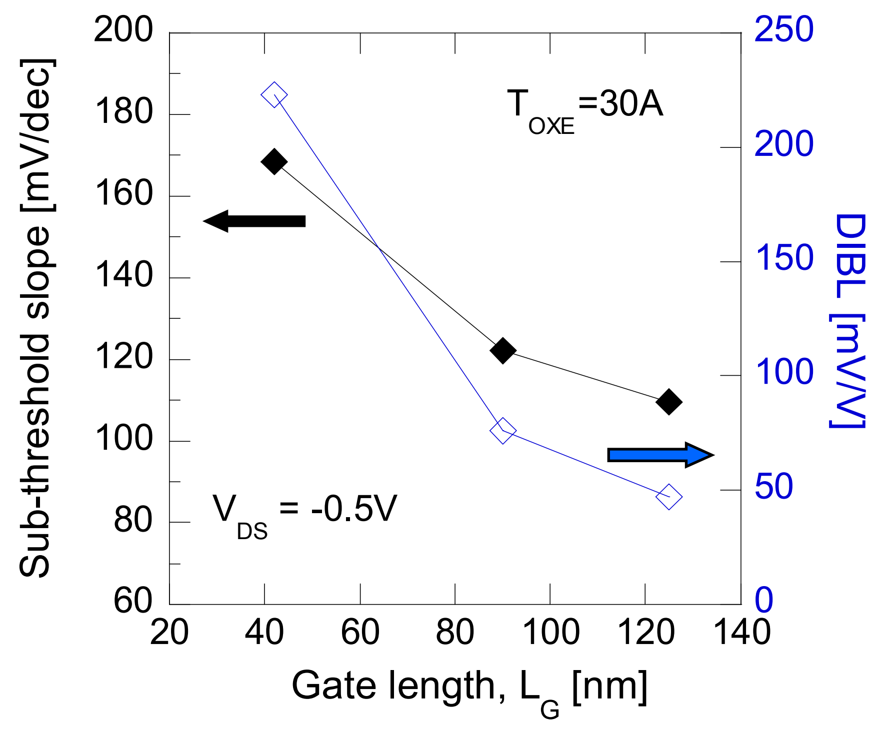
- L_G=40nm device has SS=160mV/dec, and DIBL=220mV/V
- I_{ON}/I_{OFF} =150 at V_{DS}= -0.5V with 0.5V V_G swing
- T_{OXE} reduction required for SS and DIBL improvement

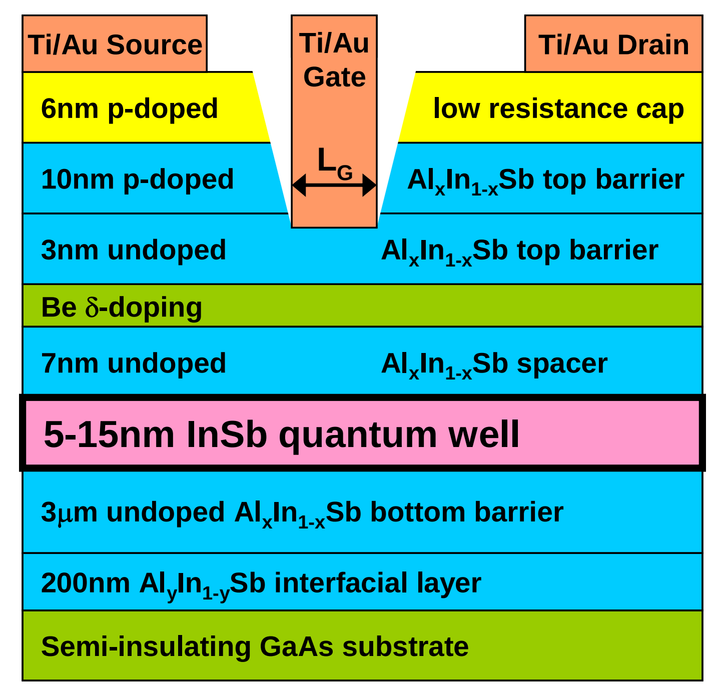
InSb p-QWFET L_G=40nm



- L_G=40nm device achieves G_m=500µS/µm at V_{CC}=0.5V, the highest reported for III-V p-QWFET

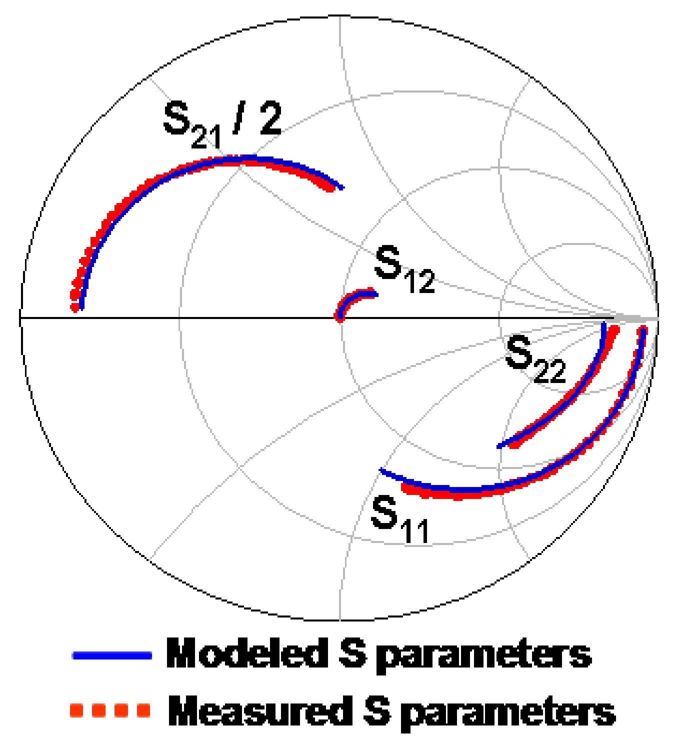
InSb p-QWFET Short-Channel Effects

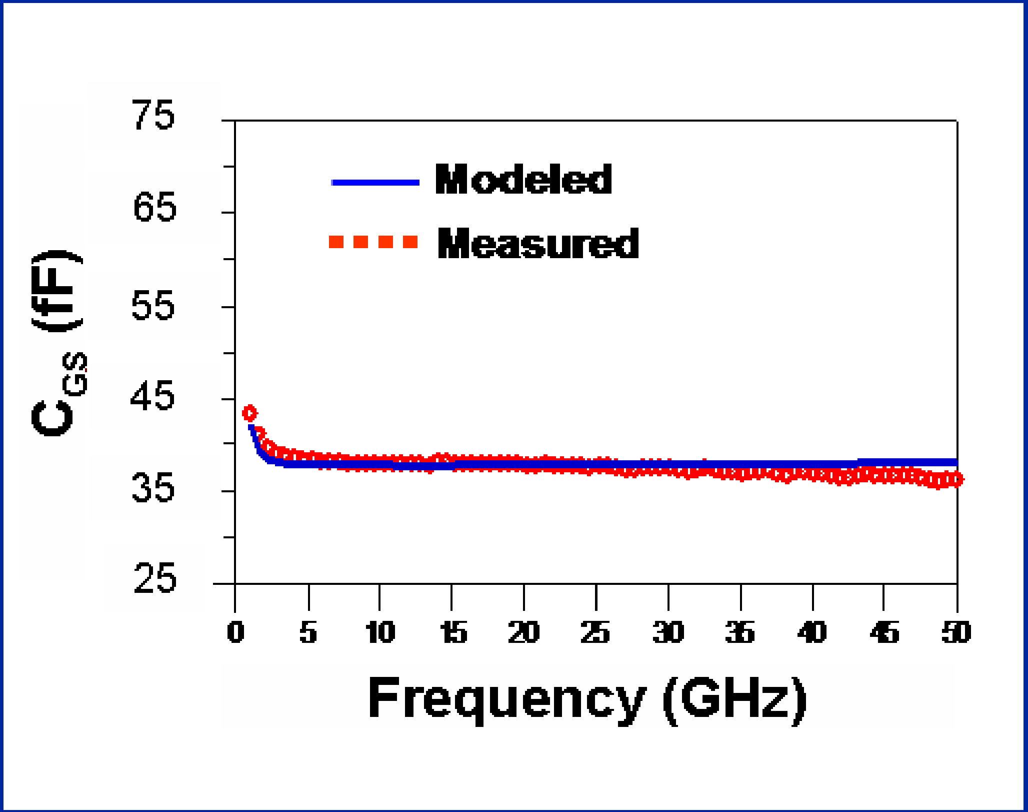




- Short channel effects can be improved by further reducing gate to channel separation

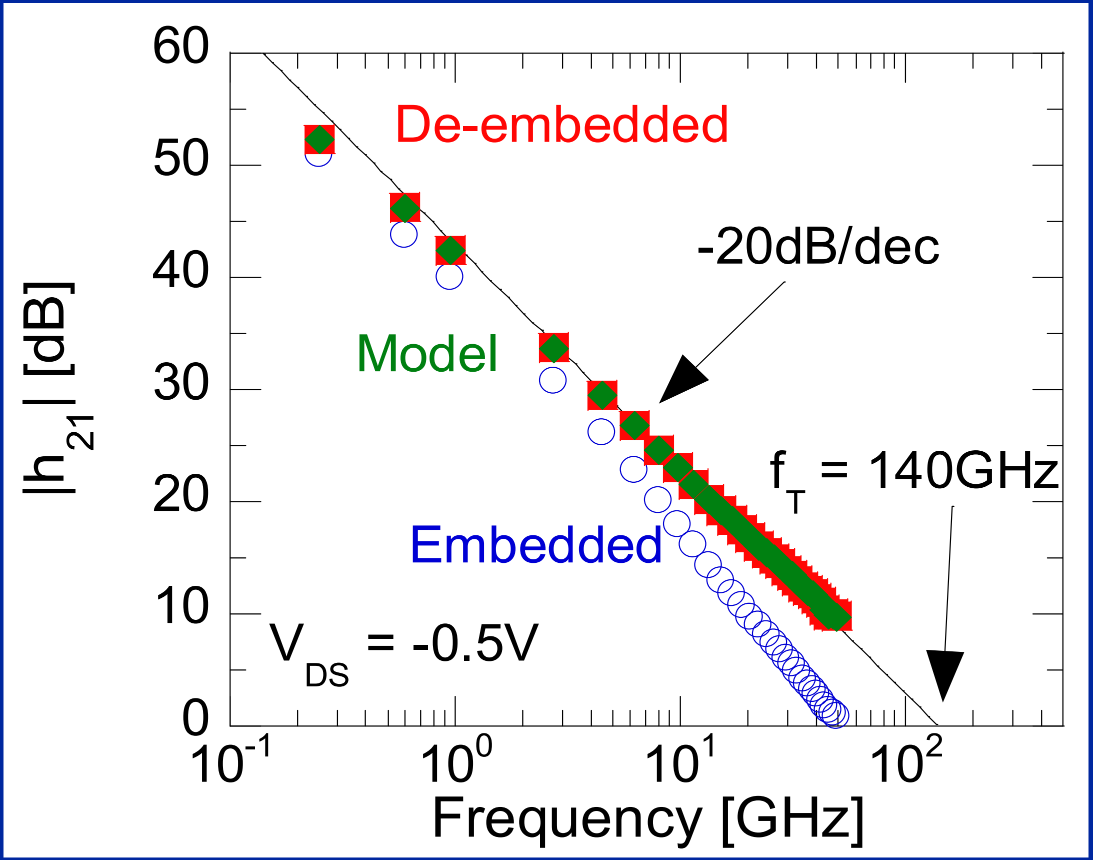
InSb p-QWFET RF Measurements and Modeling





- Measured and modeled S-parameters fit each other with RMS error <2%
- Extracted gate capacitance is independent of frequency

InSb p-QWFET RF Performance



- L_G=40nm device achieves f_T=140GHz at V_{CC}=0.5V, the highest reported for III-V p-QWFET

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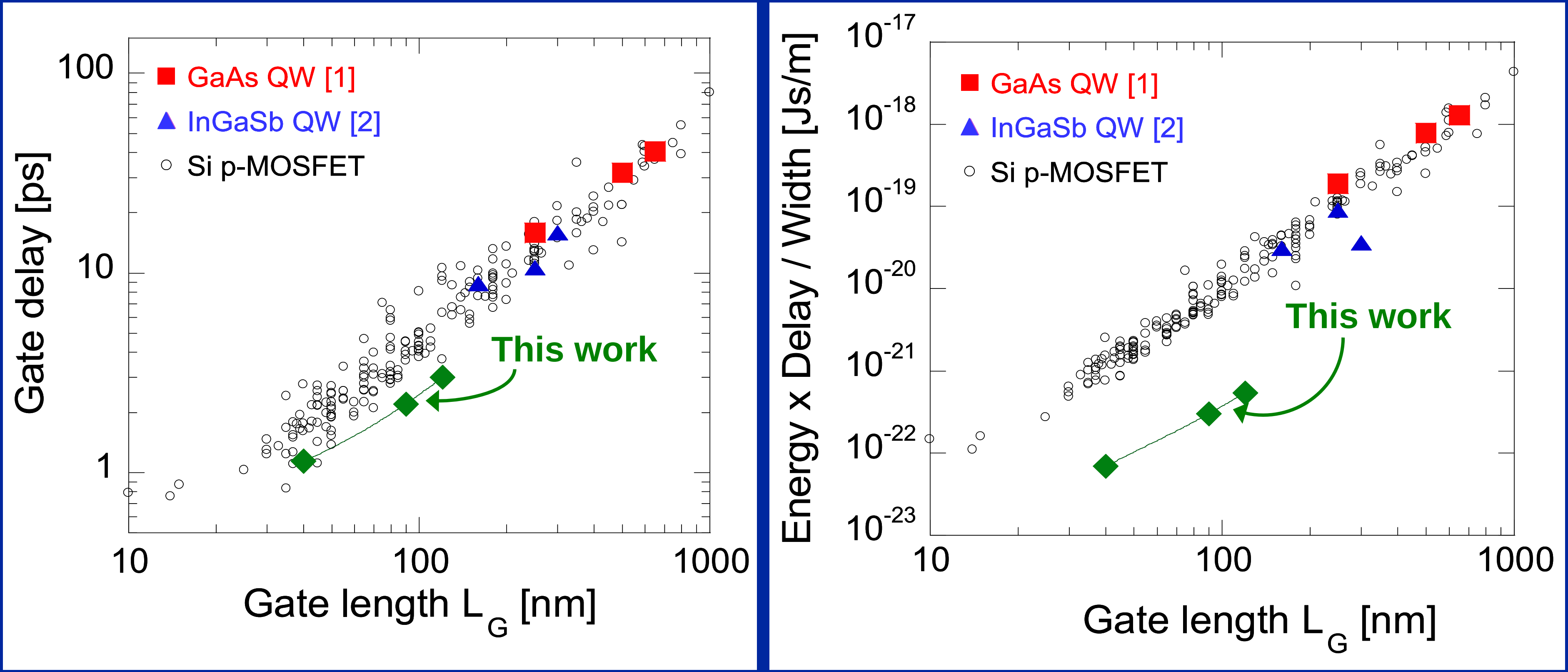
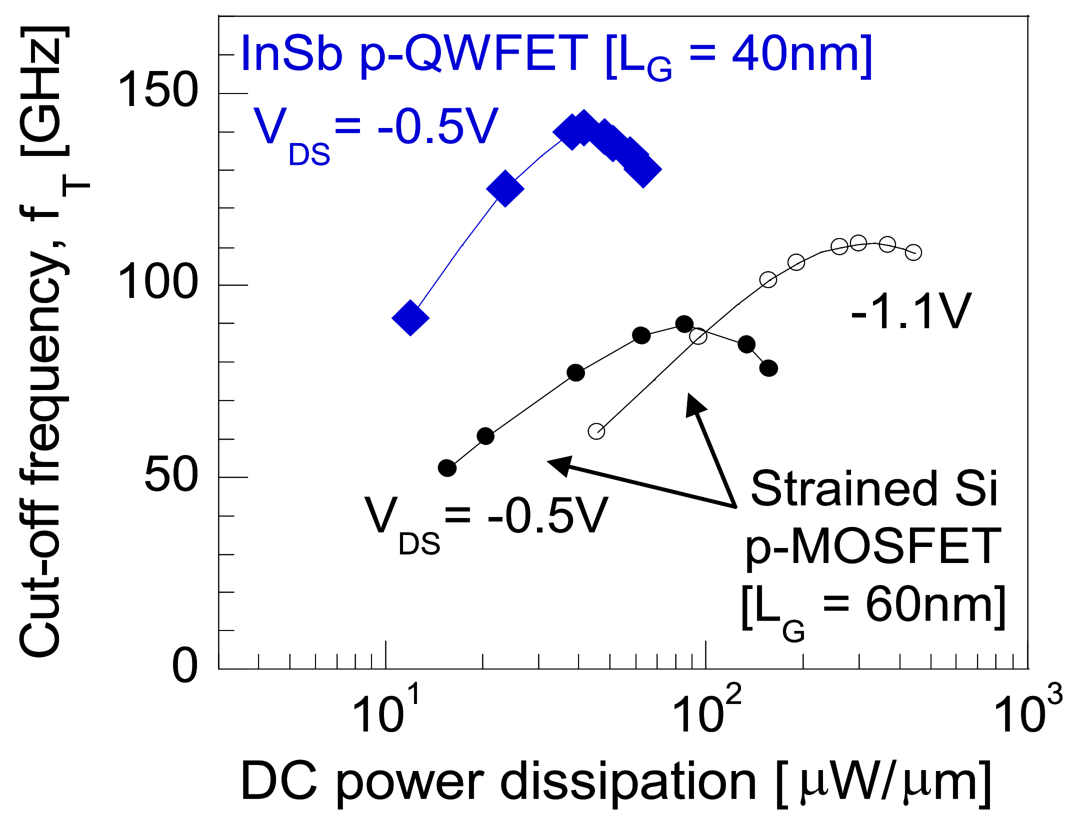
Benchmarking of InSb p-QWFET



- InSb p-QWFETs exhibit significant improvement in gate delay and energy-delay product

[1] Park, Proc. IEEE 1989; [2] Boos, EL 2007

Speed-Power Performance of InSb p-QWFET



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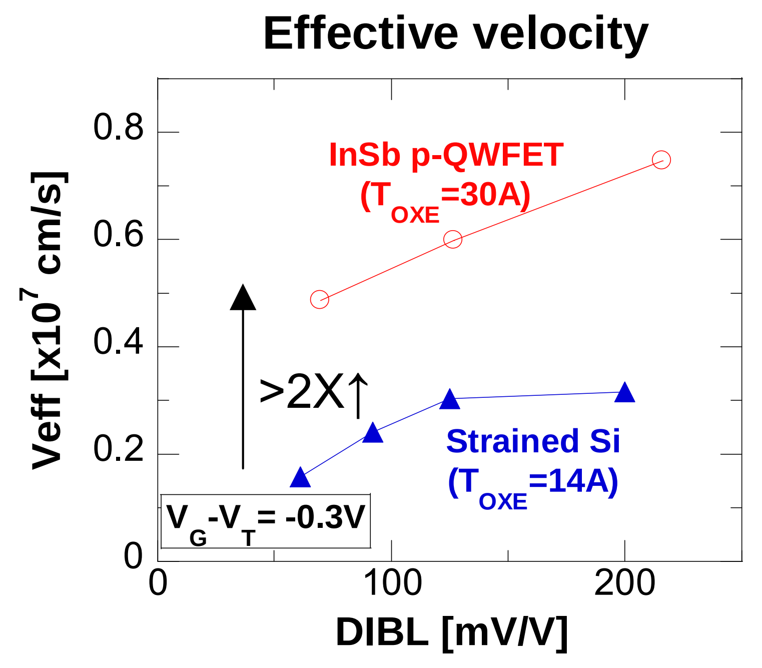
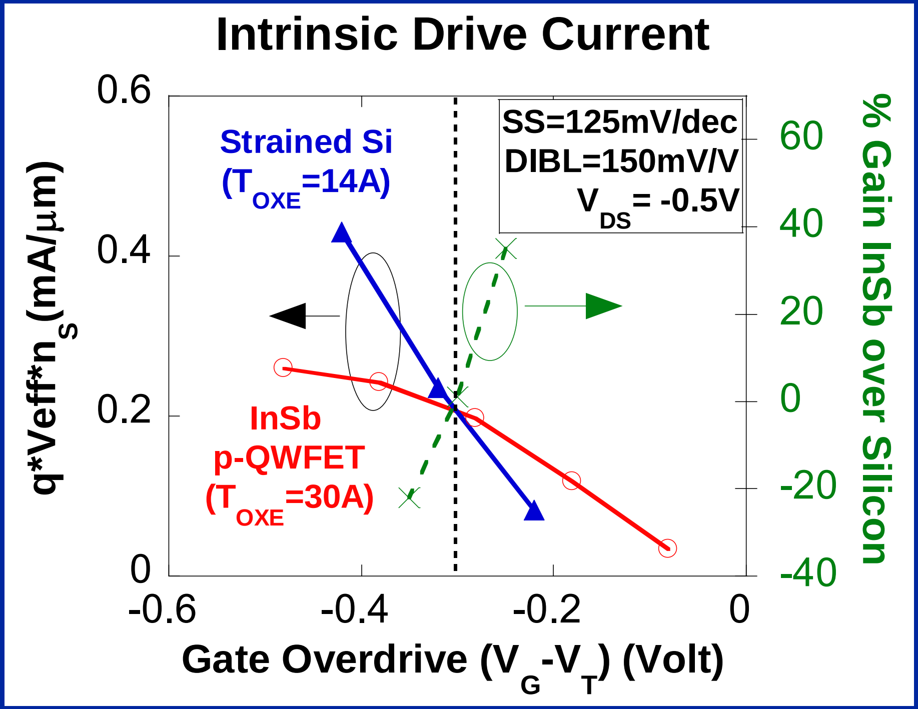
InSb p-QWFET Effective Velocity and Intrinsic Drive Current





- InSb p-QWFETs show >2X Veff gain over strained Si p-MOSFETs at matched DIBL
- At V_G - V_T = -0.3V, InSb p-QWFET is matched in intrinsic drive current to Si despite less gate control
- Further improvement via T_{OXE} reduction or strain increase

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Summary

- InSb p-QW device structure demonstrates
  - ❑ 1.9% biaxial compressive strain
  - ❑ hole mobility of 1,230cm^2/V-s at n_s=1.1e12/cm^2
- InSb device with L_G=40nm achieves
  - ❑ peak G_m=500 µS/µm at V_{CC}=0.5V, highest reported for III-V p-QWFETs
  - ❑ peak f_T=140GHz at V_{CC}=0.5V, highest reported for III-V p-QWFETs
- Benchmarking InSb p-QWFETs to standard strained Si
  - ❑ >2X Veff gain at same DIBL
  - ❑ Intrinsic I_{DSAT} ($q*n_S*$Veff) matched at V_{CC}=0.5V despite thicker T_{OXE}

Strained InSb p-QWFET intrinsic transport advantages make it a promising option for the III-V CMOS configuration

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