Voltage Regulator-Down (VRD) 11.0

Processor Power Delivery Design Guidelines

– For Desktop LGA775 Socket

November 2006

Contents

Figures

Tables

Revision History

Revision Number	Description	Revision Date
-001	Initial release.	June 2006
-002	Added socket simulation model. Corrected socket loadline window for 775_VR_CONFIG_04A. Updated DVID validation section.	November 2006

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1 Introduction

1.1 Applications

This document defines the power delivery feature set necessary to support Intel processors' Vcc power delivery requirements for desktop computer systems using the LGA775 socket. This includes design recommendations for DC to DC regulators, which convert the input supply voltage to a processor consumable Vcc voltage along with specific feature set implementation such as thermal monitoring and dynamic voltage identification.

Hardware solutions for the Vcc regulator are dependent upon the processors to be supported by a specific motherboard. Vcc regulator design on a specific board must meet the specifications of all processors supported by that board. The voltage regulator configuration for a given processor is defined in that processor's datasheet. In some instances, this data is not published and the proper mapping of processor to VRD configuration can be found from an authorized Intel representative.

The voltage regulator-down (VRD) designation of this document refers to a regulator with all components mounted directly on the motherboard for intent of supporting a single processor. For the corresponding documentation detailing voltage regulator modules (VRM) or a multiple-processor VRD, please refer to the VRM 10, EVRD 10 and EVRD 11 design guidelines documents.

VR11 PWM incorporates all of the VR10 functions plus the following enhancements:

- Extended VR10 VID table with a 7^{th} bit for 6.25 mV resolution
- Support of a second, linear 8 bit VID table with 6.25 mV resolution, 1.6 V max VID, and minimum VID defined to 31.25 mV.
- New power sequence definition
- Tighter VR Load Line tolerance from ±19 mV to < ±15 mV
- Flexible number of phases to support VR designs from 60 A to 140 A
- Integrated Thermal Monitor circuitry
- Integrated VIDPWRGD circuit

1.2 Terminology

Table 1. Feature Support Terminology

Categories	Description
REQUIRED	An essential feature of the design that must be supported to ensure correct processor and VRD functionality.
EXPECTED	A feature to ensure correct VRD and processor functionality that can be supported using an alternate solution. The feature is necessary for consistency among system and power designs and is traditionally modified only for custom configurations. The feature may be modified or expanded by system OEMs if the intended functionality is fully supported.
PROPOSED	A feature that adds optional functionality to the VRD and, therefore, is included as a design target. May be specified or expanded by system OEMs.

Table 2. Glossary

Term	Description
AVP	Adaptive voltage positioning
BJT	Bi-Polar Junction Transistor
CMRR	Common-mode rejection ratio.
D-VID	Dynamic Voltage Identification. A low power mode of operation where the processor instructs the VRD to operate at a lower voltage.
DAC	Digital to Analog Converter.
DCR	Direct Current Resistance.
Die Loadline	A mathematical model that describes voltage current relationship given system impedance (R_{DLL}). The load line equations is V_{cc} = VID – I*R_{DLL}. Measured at AN3, Vcc_Die_Sense and AN4, Vss_Die_Sense reference lands. The processor die loadlines are defined in the applicable processor datasheet.
ESL	Effective series inductance.
ESR	Effective series resistance.
FET	Field Effect Transistor.
FR4	A type of printed circuit board (PCB) material.
HVM	High volume manufacturing.
I_{cc}	Processor current.
Itt	Bus current associated with the Vtt supply.

Term	Description
LGA775 Socket	The surface mount Zero Insertion Force (ZIF) socket designed to accept the Intel Pentium® 4 processor in the LGA 775 land grid array package.
Load Line	A mathematical model that describes voltage current relationship given system impedance (R_{LL}). The load line equations is V_{cc} = VID – I*R_{LL}. In this document, the load line is referenced at the socket unless otherwise stated.
MLCC	Multi-layer ceramic capacitor.
MOSFET	Metal Oxide Semiconductor Field Effect Transistor.
PWM	Pulse width modulation.
OCP	Over current protection.
OVP	Over voltage protection.
Processor Datasheet	A document that defines the processor electrical, mechanical, and thermal specifications.
PROCHOT#	Under thermal monitoring, the VRD asserts this processor input to indicate an over-temperature condition has occurred. Assertion of this signal places the processor in a low power state, thereby cooling the voltage regulator.
RDS	FET source to drain channel resistance
RDS-ON	FET source to drain channel resistance when bias on.
R_{LL}	Load line impedance. Defined as the ratio: Voltage droop/current step. This is the load line slope. In this document, the load line is referenced at the socket unless otherwise stated.
RSS	Root Sum Square. A method of adding statistical variables.
Slope	Load line resistance. See R_{LL}. In this document, the load line is referenced at the socket unless otherwise stated.
Socket Load Line	Defines the characteristic impedance of the motherboard power delivery circuit to the node of regulation. Not the same as the processor load line that is published in the processor datasheet, which is defined across the processor Vccsense and Vsssense lands. In conjunction with mid-frequency decoupling, bulk decoupling, and robust power plane routing, design compliance to this parameter ensures that the processor voltage specifications are satisfied.
Static Load Line	DC resistance at the defined regulation node. Defined as the quotient of voltage and current (V/I) under steady state conditions. This value is configured by proper tuning of the PWM controller voltage positioning circuit. In this document, the static load line is referenced at the socket unless otherwise stated.
Thermal Monitor	A feature of the voltage regulator that places the processor in a low power state when critical VRD temperatures are reached, thereby reducing power and VRD temperature.

Term	Description
TOB	Vcc regulation tolerance band. Defines the voltage regulator's 3-σ voltage variation across temperature, manufacturing variation, and age factors. Must be ensured by design through component selection. Defined at processor maximum current and maximum VID levels.
Transient Load Line	Equal to dV/di or Vdroop/Istep and is controlled by switching frequency, decoupling capacitor selection, motherboard layout parasitics. In this document, the transient load line is referenced at the socket unless otherwise stated.
UVLO	Under-voltage lock-out
Vcc	Processor core voltage defined in the processor datasheet.
VID	Voltage Identification: A code supplied by the processor that determines the reference output voltage to be delivered to the processor Vcc lands. At zero amperes and the tolerance band at + 3-σ, VID is the voltage at the processor.
VR_TDC	Voltage Regulator Thermal Design Current. The sustained DC current which the voltage regulator must support under the system defined cooling solution.
VRD	Voltage regulator down. A VR circuit resident on the motherboard.
VRM	Voltage regulator module that is socketed to a motherboard.
Vtt	Voltage provided to the processor to initiate power up and drive I/O buffer circuits.

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2 Processor Vcc Requirements

2.1 Voltage and Current (REQUIRED)

An 8-bit VID code supplied by the processor to the VRD determines a reference output voltage as described in Section 6.1. The socket load lines in Section 2.2 show the relationship between Vcc and Icc for the processor at the motherboard-socket interface.

Intel performs testing against multiple software applications and software test vectors to identify valid processor Vcc operating ranges. Failure to satisfy the socket load line, load line tolerance band, and overshoot voltage specifications (sections 2.3 and 2.7) may invalidate Intel warranties and lead to premature processor failure, intermittent system lock-up, and/or data corruption.

2.2 Socket Loadline Definitions (REQUIRED)

To maintain processor reliability and performance, platform DC voltage regulation and transient-droop noise levels must always be contained within the Vccmin and Vccmax socket load line boundaries (known as the load line window). Socket load line compliance must be ensured across 3-σ component manufacturing tolerances, thermal variation, and age degradation. Socket load line boundaries are defined by the following equations in conjunction with the Vcc regulator design parameter values defined in Table 4. Load line voltage tolerance is defined in Section 2.4. In these equations, VID, R_{LL}, and TOB are known. Plotting Vcc while varying Icc from 0 A to Iccmax establishes the Vccmax and Vccmin socket load lines. Vccmax establishes the maximum DC socket load line boundary. Vccmin establishes the minimum AC and DC voltage boundary. Short transient bursts above the Vccmax load line are permitted; this condition is defined in Section 2.7.

Table 3. Socket Loadline Equations

Socket load line	Equation
Equation 1: Vccmax Socket load line	$Vcc = VID – (R_{LL} * I_{cc})$
Equation 2: Vcctyp Socket load line	$Vcc = VID – TOB - (R_{LL} * I_{cc})$
Equation 3: Vccmin Socket load line	$Vcc = VID – 2*TOB - (R_{LL} * I_{cc})$

Socket load line recommendations are established to provide guidance for satisfying processor die load line specifications, which are defined in processor datasheets. Die load line requirements must be satisfied at all times and may require adjustment in the socket load line value. The processor die loadlines are defined in the applicable processor datasheet.

Table 4. Vcc Regulator Design Parameters

VR Configuration	Iccmax	VR TDC	Dynamic Icc	RLL	TOB	Maximum VID
775_VR_CONFIG_04A	78 A	68 A	55 A	1.40 mΩ	+/-25 mV	1.4 V
775_VR_CONFIG_04B	119 A	101 A	95 A	1.00 mΩ	+/-19 mV	1.4 V
775_VR_CONFIG_05A	100 A	85 A	65 A	1.00 mΩ	+/-19 mV	1.4 V
775_VR_CONFIG_05B	125 A	115 A	95 A	1.00 mΩ	+/-19 mV	1.4 V
775_VR_CONFIG_06	75 A	60 A	50 A	1.00 mΩ	+/-19 mV	1.425 V

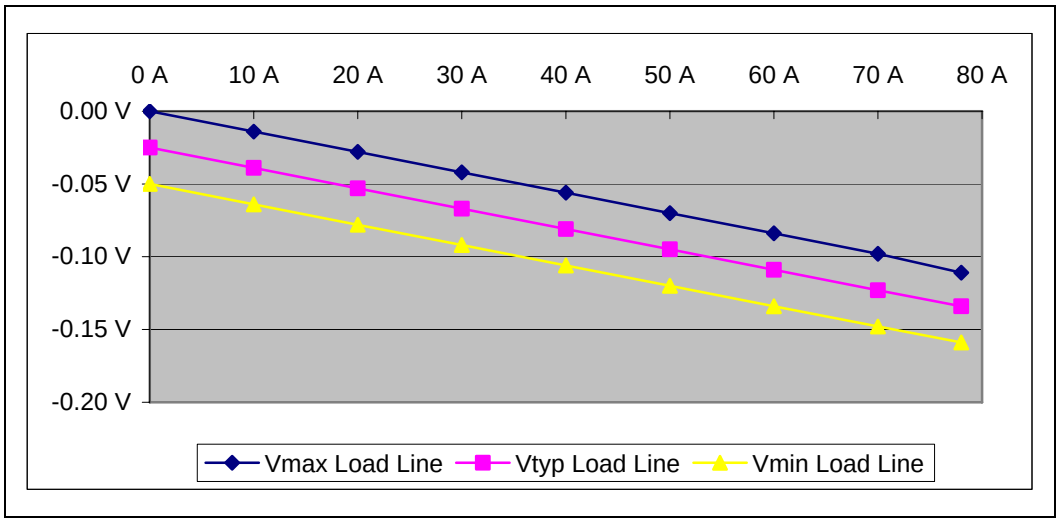
VRD transient socket load line circuits should be designed to meet or exceed rated conditions defined in Table 4. For example, 775_VR_CONFIG_04A requires a socket load line slope of 1.40 mΩ. A transient socket load line slope of 1.0 mΩ will satisfy this requirement without adversely impacting system performance or processor lifespan. This condition may be necessary when supporting multiple processors with a single VRD design. However, the static load line condition must be set to the recommended value unless explicitly stated otherwise in the processor datasheet. Operating at a low load line resistance will result in higher processor operating temperature, which may result in damage or a reduced processor life span. Processor temperature rise from higher functional voltages may lead to operation at low power states which directly reduces processor performance. Operating at a higher load line resistance will result in minimum voltage violations which may result in system lock-up, “blue screening”, or data corruption.

Table 4 provides a comprehensive list of VRD11 LGA775 voltage regulator design configurations. The configurations to be adopted by VRD hardware will depend on the specific processors the design is intended to support. It is common for a motherboard to support processors that require different VR configurations. In this case, the Vcc regulator design must meet the specifications of all processors supported by that board. For example, If a motherboard is targeted to support processors that require 775_VR_CONFIG_04A and 775_VR_CONFIG_04B, then the voltage regulator must have the ability to support 101 A of VR TDC, 119 A of electrical peak current, satisfy overshoot requirements of Section 2.7 with a dynamic load step of 95 A, satisfy a VRD tolerance band of +/-19 mV.

The following tables and figures show minimum and maximum voltage boundaries for each socket load line design configuration defined in Table 4. V_{CCTYP} socket load lines are provided for design reference; designs should calibrate the socket load line to this case (centered in the load line window, at the mean of the tolerance band). Different processors discussed in this design guide can be shipped with different VID values. The reader should not assume that processors with similar characteristics will have the same VID value. Typical values will range from 1.1 V to 1.6 V in 6.25 mV increments. A single load line chart and figure for each VRD design configuration can represent functionality for each possible VID value. Tables and figures presented as voltage deviation from VID provide the necessary information to identify voltage requirements at any reference VID. This avoids the redundancy of publishing tables and figures for each of the multiple cases.

2.2.1 Socket Loadline Definition for 775_VR_CONFIG_04A

Figure 2-1. Socket Loadline Window for 775_VR_CONFIG_04A



NOTES:
1. Presented as a deviation from VID
2. Socket load line Slope = 1.4 mΩ, TOB = +/-25 mV
3. Consult Table 4 for VR configuration parameter details

Table 5. Socket Loadline Window for 775_VR_CONFIG_04A

Icc	Maximum	Typical	Minimum
0 A	0.000 V	-0.025 V	-0.050 V
10 A	-0.014 V	-0.039 V	-0.064 V
20 A	-0.028 V	-0.053 V	-0.078 V
30 A	-0.042 V	-0.067 V	-0.092 V
40 A	-0.056 V	-0.081 V	-0.106 V
50 A	-0.070 V	-0.095 V	-0.120 V
60 A	-0.084 V	-0.109 V	-0.134 V
70 A	-0.098 V	-0.123 V	-0.148 V
78 A	-0.111 V	-0.134 V	-0.159 V

NOTES:
1. Presented as a deviation from VID
2. Socket load line Slope = 1.4 mΩ, TOB = +/-25 mV
3. Consult Table 4 for VR configuration parameter details

2.2.2 Socket Loadline Definition for 775_VR_CONFIG_04B, 05A, 05B, 06

The socket loadline for 775_VR_CONFIG_04B, 05A, 05B and 06 can be implemented in a piece-wise linear fashion. The socket loadline should have a 1 mΩ slope when the

load frequency content is in the range of 0 to 100 kHz. When the load frequency is in the range of >100 kHz to 1 MHz, a loadline slope of up to 1.2 mΩ is allowed. See Figure 2-2.

Figure 2-2. Piece-wise Linear Socket Loadline

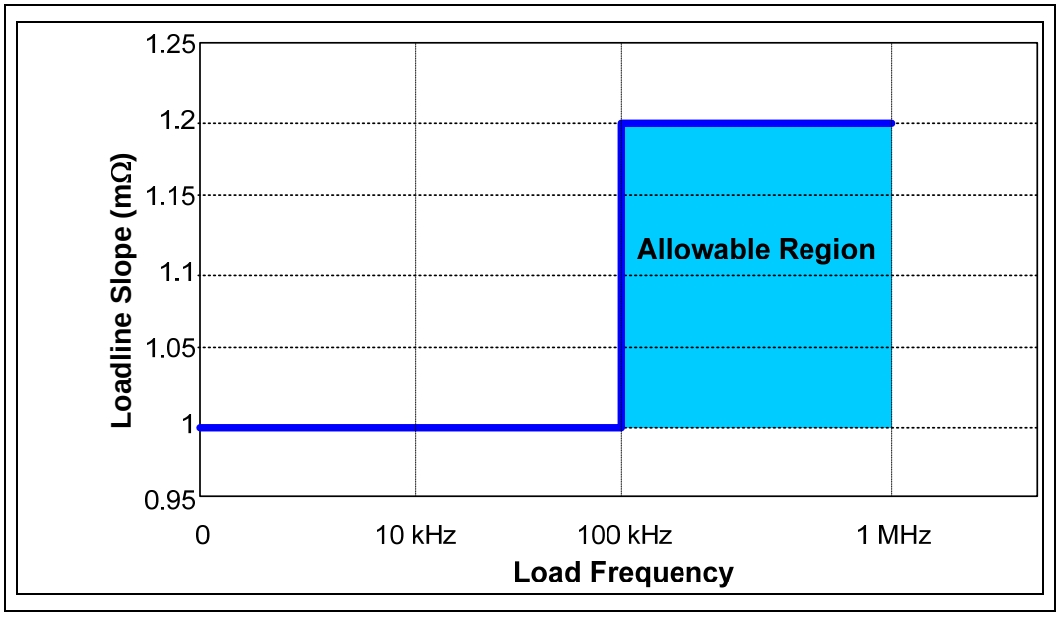
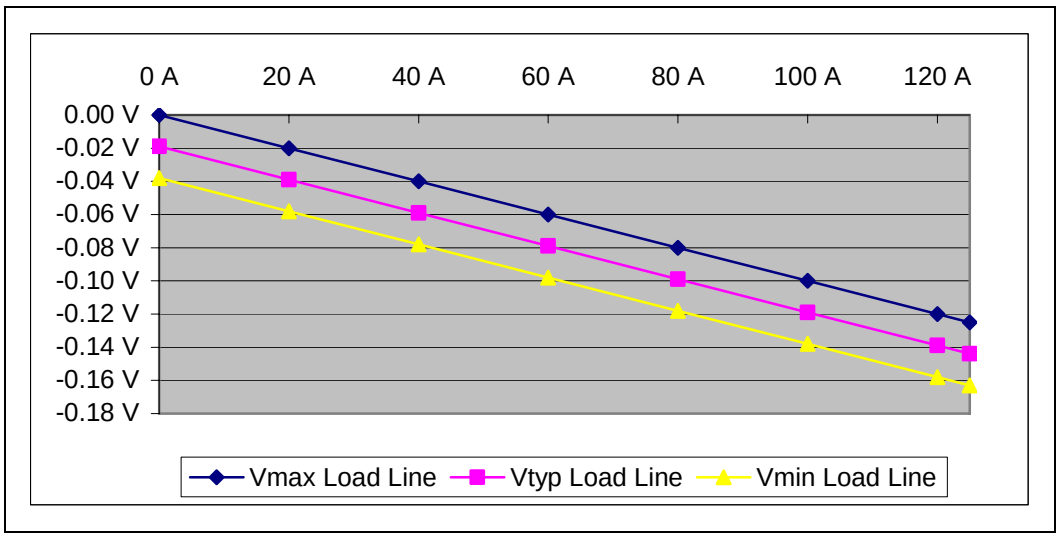


Figure 2-3. Socket Loadline Window for 775_VR_CONFIG_04B, 05A, 05B (0-100 kHz loadstep rate)



NOTES:

1. Presented as a deviation from VID
2. Socket load line Slope = 1.0 mΩ, TOB = +/-19 mV
3. Consult Table 4 for VR configuration parameter details

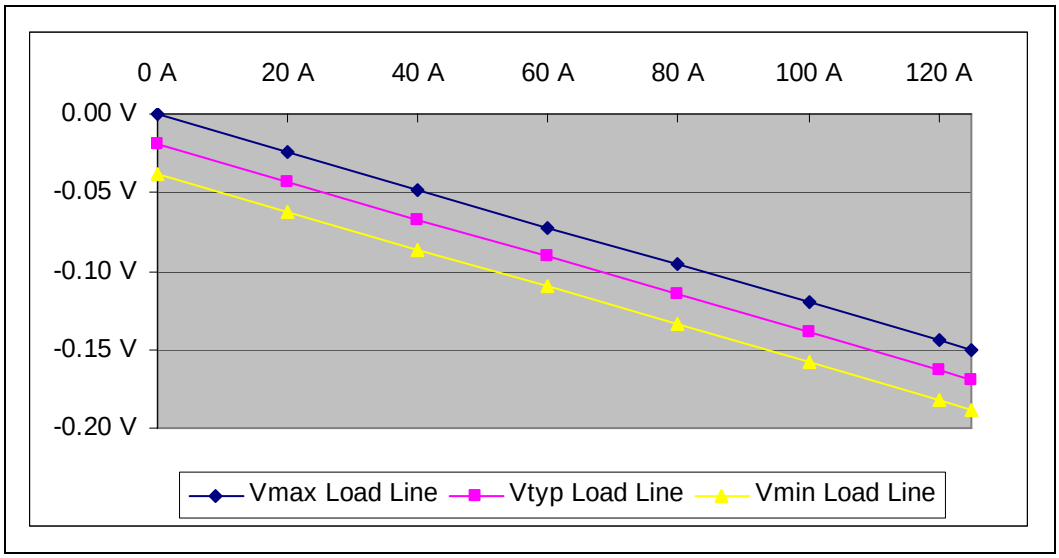
Table 6. Socket Loadline Window for 775_VR_CONFIG_04B, 05A, 05B (0-100 kHz loadstep rate)

Icc	Maximum	Typical	Minimum
0 A	0.000 V	-0.019 V	-0.038 V
20 A	-0.020 V	-0.039 V	-0.058 V
40 A	-0.040 V	-0.059 V	-0.078 V
60 A	-0.060 V	-0.079 V	-0.098 V
80 A	-0.080 V	-0.099 V	-0.118 V
100 A	-0.100 V	-0.119 V	-0.138 V
120 A	-0.120 V	-0.139 V	-0.158 V
125 A	-0.125 V	-0.144 V	-0.163 V

NOTES:

1. Presented as a deviation from VID
2. Socket load line Slope = 1.0 mΩ, TOB = +/-19 mV
3. Consult Table 4 for VR configuration parameter details

Figure 2-4. Socket Loadline Window for 775_VR_CONFIG_04B, 05A, 05B (>100 kHz-1 MHz loadstep rate)



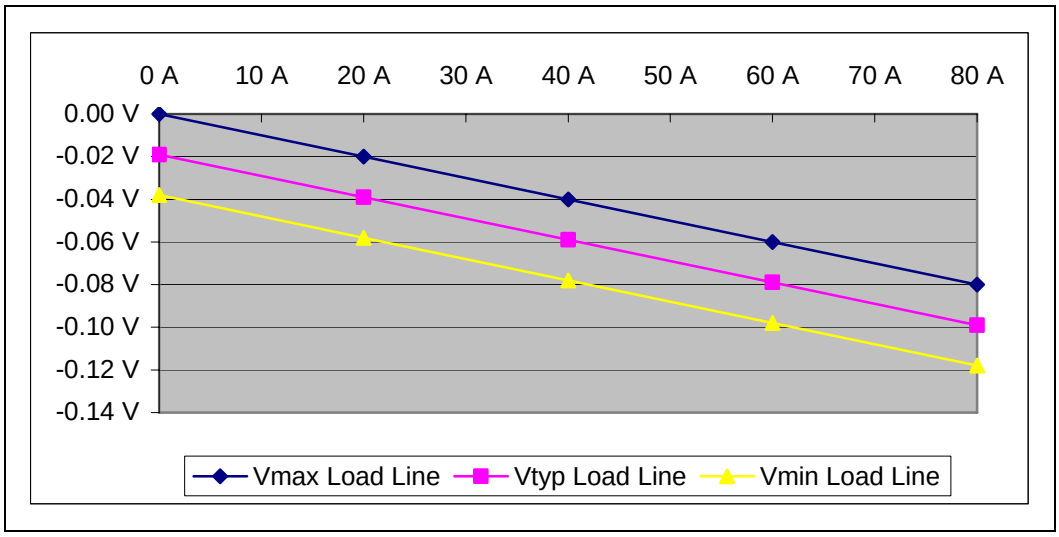
NOTES:
1. Presented as a deviation from VID
2. Socket load line Slope = 1.2 mΩ, TOB = +/-19 mV
3. Consult Table 4 for VR configuration parameter details

Table 7. Socket Loadline Window for 775_VR_CONFIG_04B, 05A, 05B (>100 kHz-1 MHz loadstep rate)

Icc	Maximum	Typical	Minimum
0 A	0.000 V	-0.019 V	-0.038 V
20 A	-0.024 V	-0.043 V	-0.062 V
40 A	-0.048 V	-0.067 V	-0.086 V
60 A	-0.072 V	-0.091 V	-0.110 V
80 A	-0.096 V	-0.115 V	-0.134 V
100 A	-0.120 V	-0.139 V	-0.158 V
120 A	-0.144 V	-0.163 V	-0.182 V
125 A	-0.150 V	-0.169 V	-0.188 V

NOTES:
1. Presented as a deviation from VID
2. Socket load line Slope = 1.2 mΩ, TOB = +/-19 mV
3. Consult Table 4 for VR configuration parameter details

Figure 2-5. Socket Loadline Window for Design Configurations 775_VR_CONFIG_06 (0-100 kHz loadstep rate)



NOTES:

1. Presented as a deviation from VID
2. Socket load line Slope = 1.0 mΩ, TOB = +/-19 mV
3. Consult Table 4 for VR configuration parameter details

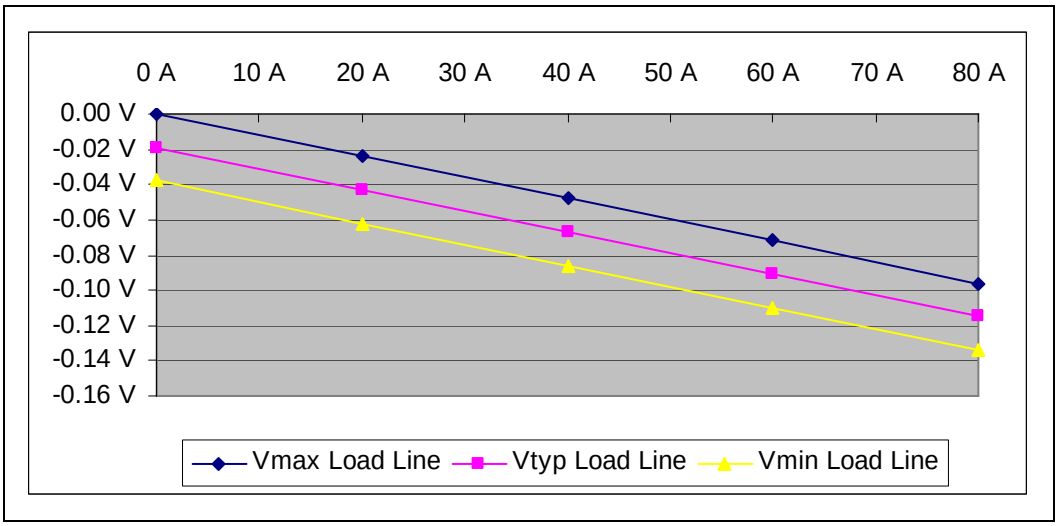
Table 8. Socket Loadline Window for 775_VR_CONFIG_06 (0-100 kHz loadstep rate)

Icc	Maximum	Typical	Minimum
0 A	0.000 V	-0.019 V	-0.038 V
20 A	-0.020 V	-0.039 V	-0.058 V
40 A	-0.040 V	-0.059 V	-0.078 V
60 A	-0.060 V	-0.079 V	-0.098 V
80 A	-0.080 V	-0.099 V	-0.118 V

NOTES:

1. Presented as a deviation from VID
2. Socket load line Slope = 1.0 mΩ, TOB = +/-19 mV
3. Consult Table 4 for VR configuration parameter details

Figure 2-6. Socket Load Line Window for Design Configurations 775_VR_CONFIG_06 (>100 kHz-1 MHz loadstep rate)



NOTES:
1. Presented as a deviation from VID
2. Socket load line Slope = 1.2 mΩ, TOB = +/-19 mV
3. Consult Table 4 for VR configuration parameter details

Table 9. Socket Loadline Window for 775_VR_CONFIG_06 (>100 kHz-1 MHz loadstep rate)

Icc	Maximum	Typical	Minimum
0 A	0.000 V	-0.019 V	-0.038 V
20 A	-0.024 V	-0.043 V	-0.062 V
40 A	-0.048 V	-0.067 V	-0.086 V
60 A	-0.072 V	-0.091 V	-0.110 V
80 A	-0.096 V	-0.115 V	-0.134 V

NOTES:
1. Presented as a deviation from VID
2. Socket load line Slope = 1.2 mΩ, TOB = +/-19 mV
3. Consult Table 4 for VR configuration parameter details

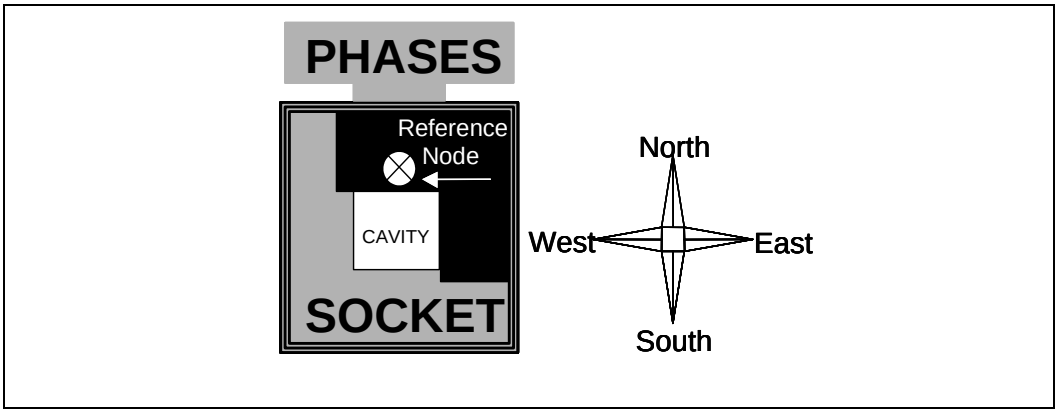
Reference nodes for socket load line measurements and voltage regulation are located in the land field between the socket cavity and the voltage regulator region. See Figure 2-7 VRD Phase Orientation. References for north phase configurations are identified in Table 10. It is recommended to place motherboard test points at this location to enable load line calibration.

VRD layout studies indicate that the highest phase count is best located north of the processor with the controller to the southeast.

Table 10. Socket Load Line Reference Lands

Orientation	Land
VCC_MB_SENSE (North Vcc)	U27
VSS_MB_SENSE (North Vss)	V26
VCC_MB_REGULATION (SE Vcc Jumper)	AN5
VSS_MB_REGULATION (SE Vss Jumper)	AN6
VCC_DIE_SENSE	AN3
VSS_DIE_SENSE	AN4

Figure 2-7. VRD Phase Orientation



To properly calibrate the socket load line parameter, the VR designer must excite the processor socket with a current step that generates a voltage droop which must be checked against the load line window requirements. Table 11 identifies the steady state and transient current values to use for this calibration.

Table 11. Intel Processor Current Step Values for Transient Socket load line Testing

VR Configuration	Starting Current	Ending Current	Dynamic Current Step	Icc Rise Time
775_VR_CONFIG_04A	23 A	78 A	55 A	83 A/µs
775_VR_CONFIG_04B	24 A	119 A	95 A	83 A/µs
775_VR_CONFIG_05A[1]	20 A	85 A	65 A	50 ns
775_VR_CONFIG_05B[1]	30 A	125 A	95 A	50 ns
775_VR_CONFIG_06[1]	25 A	75 A	50 A	50 ns

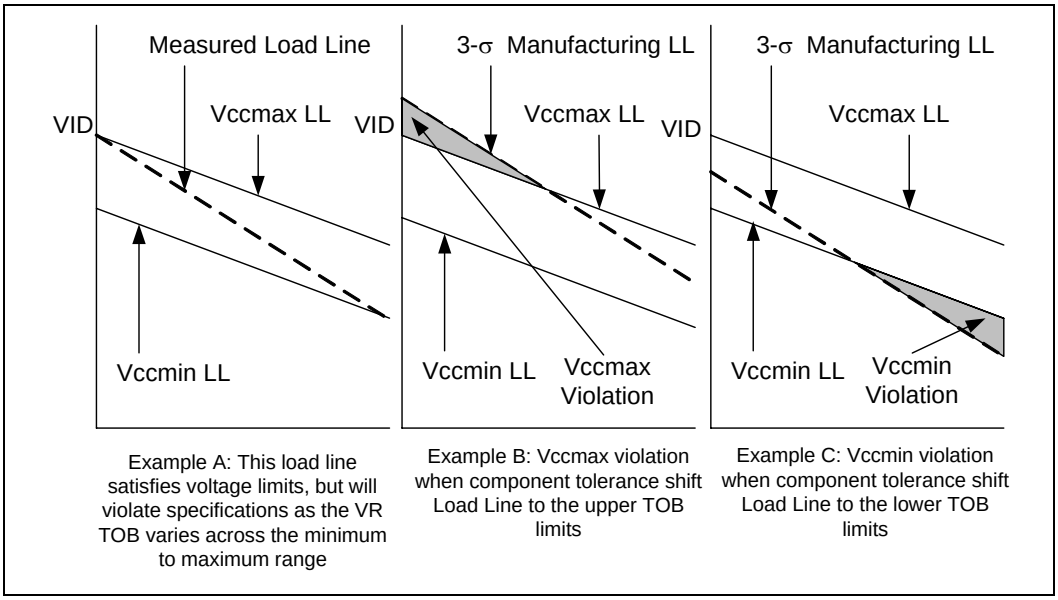
NOTES:

1. 775_VR_CONFIG_05A and 775_VR_CONFIG_05B configurations may be used with some board configurations

VRD designs must be socket load line compliant across the full tolerance band window to avoid data corruption, system lock-up, and reduced performance. When validating a system's socket load line, a single measurement is statistically insignificant and cannot represent the response variation seen across the entire high volume manufacturing population of VRD designs. A typical socket load line may fit in the specification window; however designs residing elsewhere in the tolerance band distribution may violate the specifications. Figure 2-8 Example A shows a load line that is contained in the specification window and, this single instance, complies with Vccmin and Vccmax specifications. The positioning of this socket load line will shift up and down as the tolerance drifts from typical to the design limits. Figure 2-8 Example B shows that Vccmax limits will be violated as the component tolerances shift the load line to the upper tolerance band limits. Figure 2-8 Example C shows that the Vccmin limits will be violated as the component tolerances shift the load line to the lower tolerance band limits.

To satisfy specifications across high volume manufacturing variation, a typical socket load line must be centered in the load line window and have a slope equal to the value specified in Table 4. Figure 2-9 Example A shows a socket load line that meets this condition. Under full 3-σ tolerance band variation, the load line slope will intercept the Vccmax load line (Figure 2-8 Example B) or Vccmin load line (Figure 2-8 Example C) limits.

Figure 2-8. Examples of High Volume Manufacturing Load Line Violations

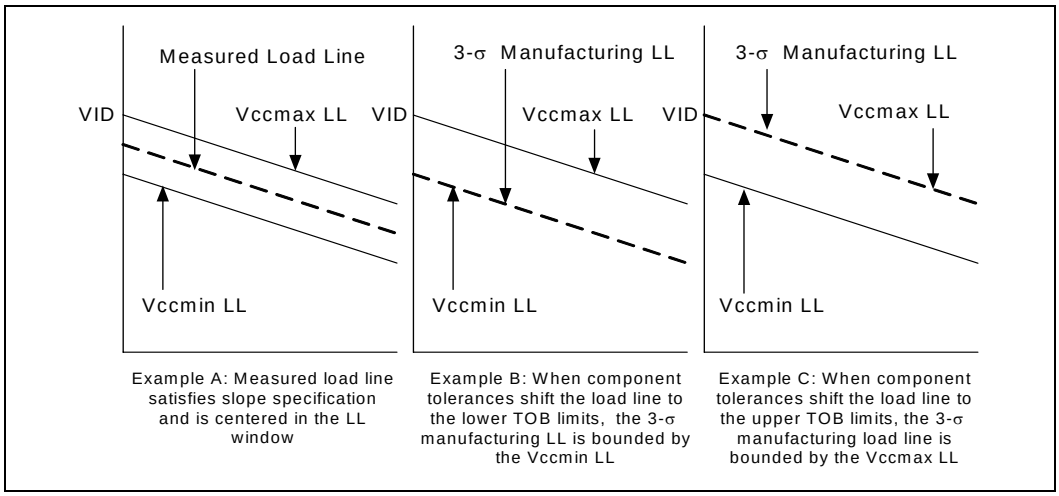


Example A: This load line satisfies voltage limits, but will violate specifications as the VR TOB varies across the minimum to maximum range

Example B: Vccmax violation when component tolerance shift Load Line to the upper TOB limits

Example C: Vccmin violation when component tolerance shift Load Line to the lower TOB limits

Figure 2-9. High Volume Manufacturing Compliant Load Line



2.3 VRD Output Filter (REQUIRED)

Desktop processor voltage regulators include an output filter consisting of large bulk decoupling capacitors to compensate for large transient voltage swings and small value ceramic capacitors to provide mid-frequency decoupling. This filter must be designed to stay within load line specifications (see section 2.2) across tolerances due to age degradation, manufacturing variation, and temperature drift.

The VRD output filter needs to be designed for the VR controller that is used. Different controllers can have different filter requirements for meeting the loadline requirements.

2.3.1 Bulk Decoupling

Bulk decoupling is necessary to maintain Vcc within load line limits prior to the VRD controller response. Design analysis shows that bulk decoupling requirements will vary with the number of VRD phases and the FET switching frequency. Design analysis determined that the most cost efficient filter solution incorporates 560 or 820 µF bulk capacitors with low (5 mΩ) average ESR per capacitor.

The D-VID mode of operation is directly impacted by the choice of bulk capacitors and output inductor value in the VRD output filter. It is necessary to minimize Vcc settling time during D-VID operation to hasten the speed of core power reduction. The speed of recovery is directly related to the RCL time constant of the output filter. To ensure an adequate thermal recovery time, it is recommended to design the output filter with a minimal output inductor value and a minimal amount of bulk capacitance with minimum ESR, while providing a sufficient amount of decoupling to maintain load line and ripple requirements. At this time, high-density aluminum poly capacitors with 5 mΩ average ESR have been identified as the preferred solution. Failure to satisfy the Vcc settling time requirements defined in section 2.6 may invalidate processor thermal modes.

It is common for a motherboard to support processors that require different VRD configurations (see Table 4). In this case, the Vcc regulator design must meet the specifications of all processors supported by that board. This requires the VRD to adopt an output filter design that satisfies the lowest socket load line value of all supported processors. For example, if a motherboard is to support processors requiring 775_VR_CONFIG_04A with a 1.4 mΩ socket load line slope and 775_VR_CONFIG_04B requiring a 1.0 mΩ socket load line slope, the VRD output filter must have a transient socket load line value of 1.0 mΩ to satisfy the noise requirements of each processor.

Consult the appropriate platform design guideline for an output filter design capable of satisfying load line and D-VID constraints.

2.3.2 Mid-frequency Decoupling

The output filter includes mid-frequency decoupling to ensure ripple and package noise is suppressed to specified levels. Ripple limits are defined in Section 2.4.3 and package noise limits are defined in appropriate processor datasheets in the form of a processor die load line.

High Mid-frequency noise and ripple suppression are best minimized by 10 µF, 22 µF or 47 µF multi-layer ceramic capacitors (MLCC's). It is recommended to maximize the MLCC count in the socket cavity to help suppress transients induced by processor packaging hardware. Remaining MLCC's should be first placed adjacent to the socket edge in the region between the socket cavity and the voltage regulator.

Intel recommends a mid-frequency filter consisting of MLCC's distributed uniformly through the socket cavity region with total capacitance of 396 µF (18 x 22 µF). The cavity-capacitor ESL value needs to be low enough to ensure the VR filter impedance is at or below the load line target up to F_{break} frequency in Table 12. See section 2.3.4 for a method to measure the mid frequency MLCC impedance. To ensure functionality with all Intel processors, adoption of the reference solution (defined in appropriate Platform Design Guidelines) accompanied by full processor load line validation is strongly recommended.

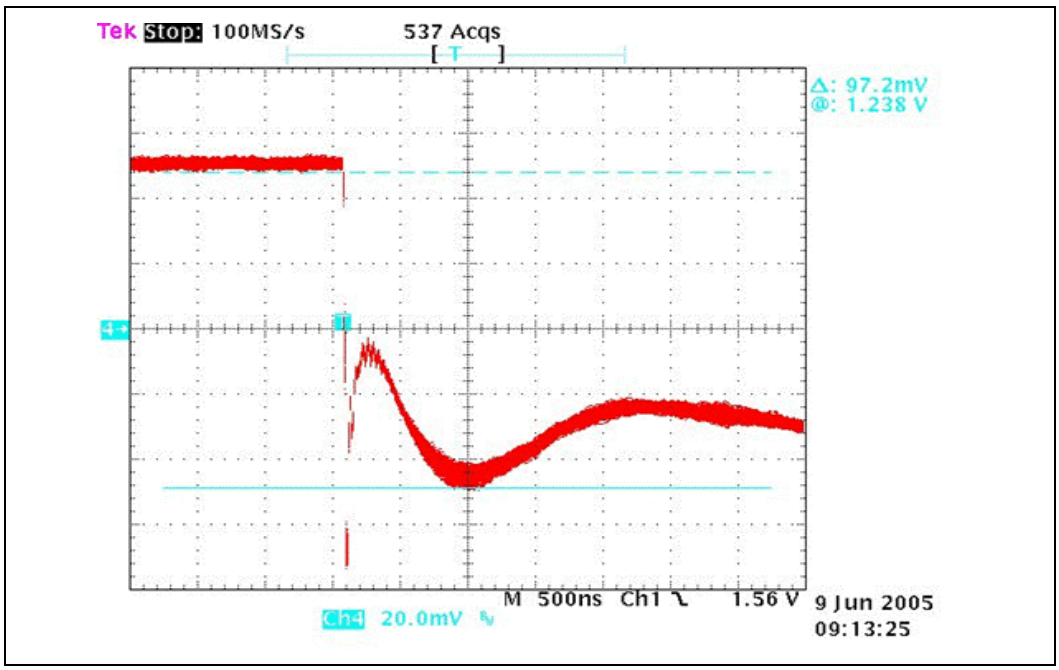
Noise is directly dependent upon the processor core frequency, so the filter must ensure adequate decoupling to support all frequencies the board is to support. Impedance measurements as described in section 2.3.4 will help the designer analyze the MLCC decoupling solution.

2.3.3 Time Domain Validation

To ensure processor reliability and performance, platform transient-droop and overshoot noise levels must always be contained within the Vccmin and Vccmax socket load line boundaries (known as the load line window). The load generates a voltage droop, or overshoot, which must be checked against the load line window requirements. The current step must have a fast enough slew rate to excite the impedance across the frequency range of the VR. In addition, the VR needs to be tested at different load frequencies and load steps to prevent any non-linear, resonant, or beating effects that could cause functional issues or load line violations. Intel recommends sweeping the load frequency from DC to 1 MHz, using two different load steps.

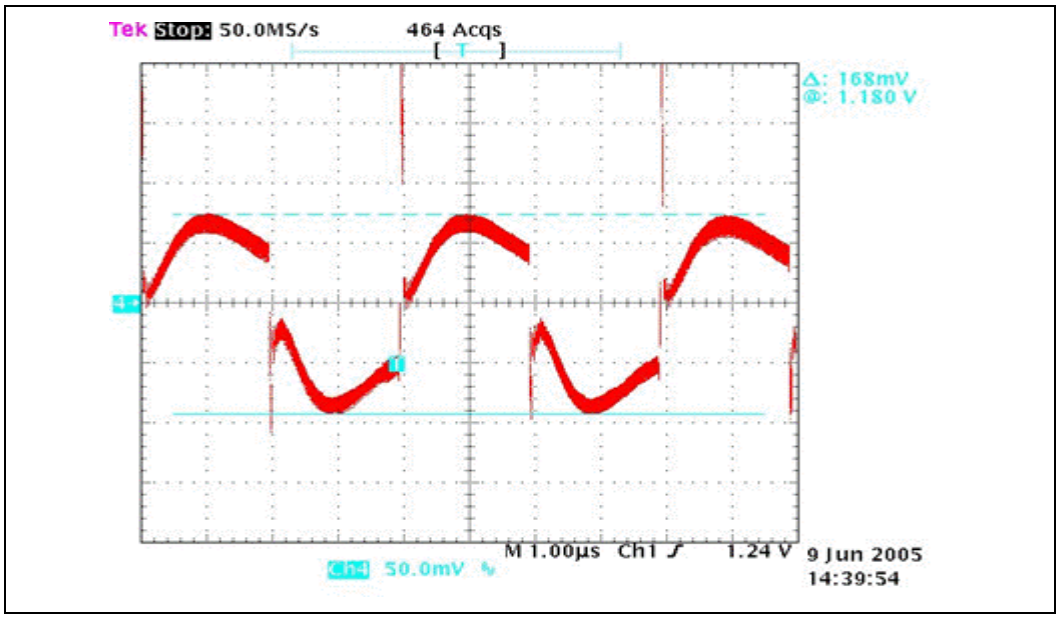
Intel recommends testing using different VID levels for each of the supported VR configurations. In particular the highest and lowest VIDs should be checked. The VID ranges for each processor is available in the processor datasheet.

Figure 2-10. 200 Hz, 100 A step droop waveform



NOTE: The cursor indicates the droop area of interest. A falling edge with a width less than 100 ns can be ignored.

Figure 2-11. 250 kHz, 100 A step waveform.



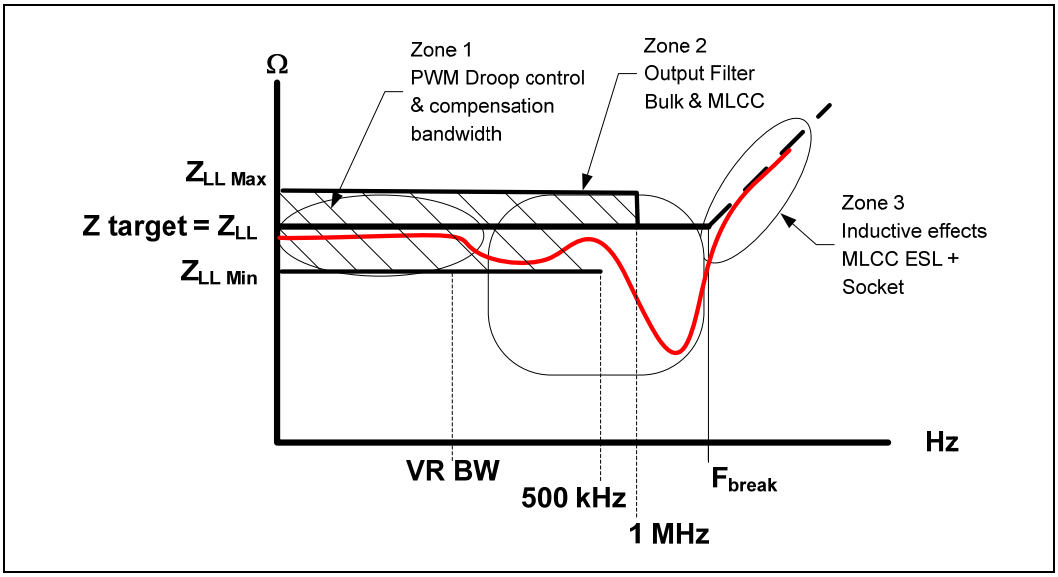
NOTE: Note: The cursor indicates the droop area of interest. A falling edge with a width less than 100 ns can be ignored.

2.3.4 Platform Impedance Measurement and Analysis (Expected)

In addition to the tuning of the load line with Vdroop testing and DC load line testing, the decoupling capacitor selection needs to be analyzed to make sure the impedance of the decoupling is below the load line target up to the frequency F_{break} as defined in Figure 2-12. This analysis can be done with impedance testing or through power delivery simulation if the designer can extract the parasitic resistance and inductance of the power planes on the motherboard and they have good models for the decoupling capacitors.

Measured power delivery impedance should be with in the tolerance band shown in Figure 2-12. For Load Line compliance, time domain validation is required and the VR tolerance band must be met at all times. Above 500 kHz, the minimum impedance tolerance is not defined and is determined by the MLCC capacitors required to get the ESL low enough to meet the load line impedance target at the F_{break} frequency. At 1 MHz, the Zmax tolerance drops to the load line target impedance. Any resonance points that are above the Zmax line need to be carefully evaluated with time domain method defined in 2.3.3 by applying transient loads at that frequency and looking for Vmin violations. Maintaining the impedance profile up to F_{break} is important to ensure the package level decoupling properly matches the mother board impedance. After F_{break}, the impedance measurement is permitted to rise at a inductive slope. The motherboard VR designer does not need to design for frequencies over F_{break} as the processor package decoupling takes over in the region above F_{break}.

Figure 2-12. Power Distribution Impedance vs. Frequency



NOTES:

1. See Table 12. Impedance Measurement Parameters definitions
2. Zone 1 is defined by the VR closed loop compensation bandwidth (VR BW) of the voltage regulator. Typically 30-40 kHz for a 300 kHz voltage regulator design.
3. Zones 2 and 3 are defined by the output filter capacitors and interconnect parasitic resistance and inductance. The tolerance is relaxed over 500 kHz allowing the VR designer freedom to select output filter capacitors. The goal is to keep Z(f) below Z_{LL} up to Fbreak and as flat as practical, by selection of bulk capacitor values and type and number of MLCC capacitors. The ideal impedance would be between Z_{LL} and Z_{LL} Min but this may not be achieved with standard decoupling capacitors.

Table 12. Impedance Measurement Parameters

Parameter	Value	Notes:
Z_{LL}	1 mΩ	LGA775 Desktop LL target
$Z_{LL\ max}$	1.2 mΩ	Based on VR11 PWM tolerance band
$Z_{LL\ min}$	0.8 mΩ	Based on VR11 PWM tolerance band
F_{break}	2.0 MHz	-

2.4 TOB: Voltage Tolerance Band (REQUIRED)

Processor load line specifications must be ensured across component process variation, system temperature extremes, and age degradation limits. The VRD topology and component selection must maintain a 3-σ tolerance of the VRD Tolerance Band around the typical load line (see Section 2.2). The critical parameters include voltage ripple, VRD controller tolerance, and current sense tolerance under both static and transient conditions. Individual tolerance components will vary among designs; the processor requires only that the total error stack-up stay within the defined VR configuration tolerance band under the conditions defined in Table 4.

2.4.1 PWM Controller Requirements:

To ensure designers can satisfy the required VRD tolerance band across all modes of operation, PWM controller vendors must publish data and collateral that is critical for satisfying design requirements. This includes support of the following:

- The PWM vendor is to define equations for calculating the VRD TOB with Inductor DCR sensing and resistor sensing. The equation is to include all parameter dependencies such as AVP tolerance, age degradation, thermal drift, sense element DC and AC accuracy, etc under 3-σ variation. These equations are to be published in the PWM controller data sheet. The vendor is to distribute and support a tolerance band calculator that communicates the VRD TOB for each valid VID under each VID table.

- Total PWM controller DC set point accuracy is typically <0.5% over temperature, component age, and lot to lot variation over the 1.0 – 1.6 V VID range. DAC error may be larger for voltages below 1 V under the assumption that the required Vmin TOB requirements are always satisfied. Typical low voltage accuracy is +-5 mV for 0.8 V-1.0 V and +-8 mV < 0.8 V. Each vendor is to publish PWM controller DAC accuracy by VID value in the component data sheet.

- The PWM controller must support voltage amplitudes read across sense elements with a DCR of 0.1-2.0 mΩ. PWM controller vendors must define the minimum sense signal voltage necessary to satisfy PWM signal to noise ratio requirements. These requirements are to be published by the vendor in their PWM controller data sheet.

- Vendors must establish an Inductor DCR sense topology that supports a ±10 mV TOB at 1.3 VID, 115 A VRTDC, 125 A Iccmax, 1.00 mΩ socket load line slope excluding voltage ripple. The topology and component values are to be published in the PWM controller data sheet.

2.4.2 Dynamic Voltage Identification (D-VID) TOB

During the D-VID (see section 2.6) mode of operation, VRD tolerance band requirements must be satisfied. Minimum voltage cannot fall below the values predicted by Equation 3 assuming any possible VID setting along with the R_{LL} a TOB values defined in Table 4. Current values to be used for assessing TOB during dynamic VID should be linearly scaled with voltage. For example, if a 90 A of current is defined at a VID of 1.35 V and the functional VID value is 0.9 V, then the TOB should be calculated assuming (0.9 V/1.35 V)*90 A = 60 A.

Vccmax VRD TOB can be relaxed during dynamic VID. Positive tolerance variation is permitted and is to be bounded by the voltages predicted by Equation 1, where VID is the standard VID value in regulation when not in the D-VID mode. Consult Section 2.4.2, for D-VID specifications.

2.4.3 Ripple Voltage

To meet tolerance band specifications, high and low frequency ripple is to be limited to 10 mV peak to peak. Measurements must be taken carefully to ensure that superposition of high frequency with low frequency oscillations do not sum to a value greater than 10 mV peak to peak. Measurements are to be taken with a 20 MHz band limited oscilloscope. Ripple testing is to be performed at 5 A minimum loading and at VR TDC.

2.4.4 Sense Topology Requirements

VRD designers must construct a sense topology that ensures compliance to tolerance band specifications under standard operation and under the D-VID mode of operation. This includes selection of sense elements and supporting components that satisfy tolerance requirements with the chosen PWM controller and ripple amplitude.

Inductor DCR or resistor sensing topologies are required to satisfy tolerance band requirements. Current sensing across MOSFET Rds-on is not suitable for load line AVP functions due to the large variation in this parameter. Evaluation of this sense method has shown that the TOB requirements cannot be satisfied unless expensive, <10% tolerance MOSFETs are chosen.

2.4.5 Error Amplifier Specification

The PWM error amplifier should be designed with a sufficient gain bandwidth product to ensure duty cycle saturation does not occur with large signal current transients. Typical target closed loop VR bandwidths of 30-200 kHz (20% of switching frequency target) are expected in VR11 system designs. The output of the error amplifier should also have high slew rates to avoid duty cycle saturation. Performance limitations must be included in the VRD TOB equations.

2.4.6 PWM Operating Frequency

VR11 PWM must be designed to work across a wide range of switching frequencies. For the desktop market, this can range from 200 kHz up to 1 MHz and corresponding loop bandwidths of 30 kHz to 250 kHz respectively. The tolerance of the PWM oscillator should be <10%. Performance limitations must be included in the VRD TOB equations.

2.5 Stability (REQUIRED)

The VRD must be unconditionally stable under all DC and transient conditions across the voltage and current ranges defined in Table 4 and Figure 2-1. The VRD must also

operate in a no-load condition: i.e., with no processor installed. Normally the no-processor VID code will be 11111, disabling the VRD (see Table 21).

2.6 Dynamic Voltage Identification (REQUIRED)

2.6.1 Dynamic-Voltage Identification Functionality

VRD11 architecture includes the Dynamic Voltage Identification (D-VID) feature set, which enables the processor to reduce power consumption and processor temperature. Reference VID codes are dynamically updated by the processor to the VRD controller via the VID bus when a low power state is initiated. VID codes are updated sequentially in 12.5 mV steps and are transmitted every 5 microseconds until the final voltage code is encountered. Processors are capable of transitioning from standard operational VID levels to either the VR11 or extended VR10 VID table minimum values. They are also capable of returning to a higher VID code in a similar manner. The low voltage code will be held for a minimum of 50 microseconds prior to sequentially transitioning through the VID table to a new voltage reference which can be any higher VID code, but is generally the original reference VID.

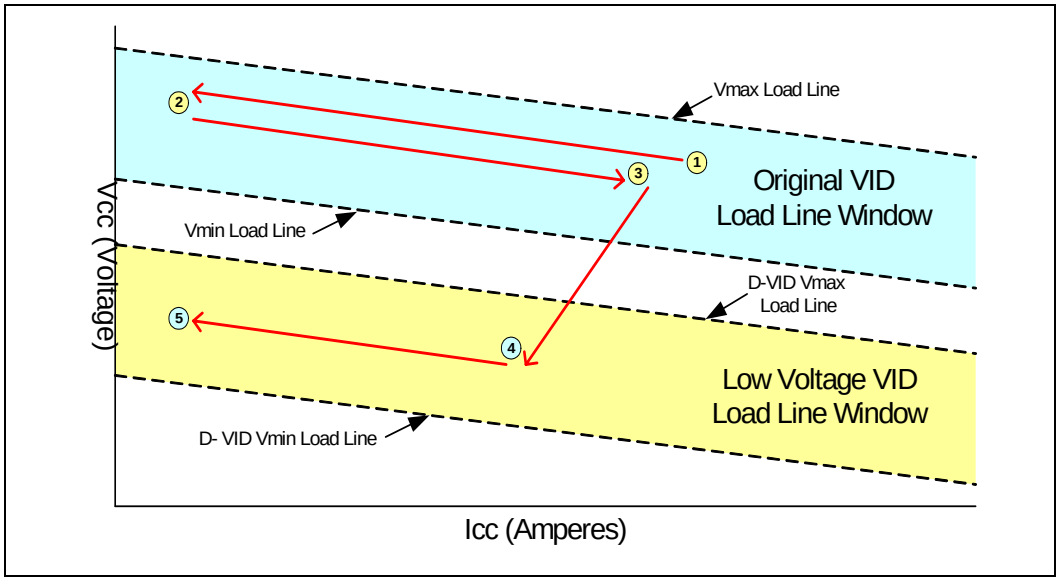
Figure 2-13 illustrates processor-operating states as the VID level is lowered. The diagram assumes steady state, maximum current during the transition for ease of illustration. In this figure, the processor begins in a high-load condition. Upon entering D-VID, the processor will shift to a low power state and stop executing code (sequence 1 => 2). After reaching state 2, the processor encounters a brief delay to prepare for low power operation then re-initiates code, resulting in current draw and a load line drop to state 3. Sequencing from state 3 to 4 is a simplification of the multiple steps from the original VID load line window to the low-voltage VID window. Transition from state 4 to state 5 is an example of a load change during normal operation in the low voltage VID setting. Transition from a low to high VID reference follows the reverse sequence.

During a D-VID transition, Vcc must always reside above the minimum load line of the current VID setting (see Figure 2-13). The load line values of each VID increment are required to match the slope defined in Table 4. In addition, the voltage tolerance band and ripple specifications defined in Table 4 and Section 2.4 must be satisfied in this state. To expedite power reduction and processor cooling, the VRD must lower the maximum Vcc value to reside within the low voltage VID window within 50 microseconds of the final VID code transmission see . The VRD must respond to a transition from low VID to high VID by regulating the Vcc output to the range defined by the new VID code within 50 microseconds of the final code transmission. Note: the minimum VID is not constant among all processors; the value will vary with frequency and standard VID settings. This results in numerous possible D-VID states. A simple and direct D-VID validation method is defined at the end of this section.

During a D-VID event, the processor load may not be capable of absorbing output capacitor energy when the VID reference is lowered. As a result, reverse current may flow into the AC-DC regulator's input filter, potentially charging the input filter to a voltage above the over voltage value. Upon detection of this condition, the AC-DC regulator will react by shutting down the AC-DC regulator supply voltage. The VRD and AC-DC filter must be designed to ensure this condition does not occur. In addition, reverse current into the AC-DC regulator must not impair the operation of the VRD, the AC-DC supply, or any other part of the system.

Under all functional conditions, including D-VID, the Vcc supply must satisfy load line and overshoot constraints to avoid data corruption, system lock-up events, or system blue-screen failures.

Figure 2-13. Processor D-VID Load Line Transition States



2.6.2 D-VID Validation

Intel processors are capable of generating numerous D-VID states and the VRD must be designed to properly transition to and function at each possible VID voltage. However, exhaustive validation of each state is unnecessary and impractical. Validation can be simplified by verifying the VRD conforms to socket load line requirements, tolerance band specifications, and D-VID timing requirements. Then, by default, each processor D-VID state will be valid. The key variables for Vcc under D-VID conditions are processor loading, starting VID, ending VID, and Vcc slew rate. The Vcc slew rate is defined by VRD bulk decoupling, the output inductors, the switching FET resistance and the processor load. This indicates that the Vcc slewing will have an exponential behavior, where the response to code 'n+1' takes longer to settle than code 'n'. As a result, a test from maximum to minimum and from minimum to maximum will be sufficient to ensure slew rate requirements and VID code regulation.

To ensure support for any valid VID reference, testing should be performed from the maximum table entry of 1.6V to the minimum VID table value. For VR11, use 0.8375 V for the minimum value. The VRD must ensure that the full table transition occurs within 50 microseconds of the final VID code transmission. Slew rate timing is referenced from 0.4 V on the rising edge of the initial VID code to the time the final voltage is settled within 5 mV of the final Vcc value. Intel testing has noted a 10% change to the Vcc slew rate between VRD no load (5 A) and full load (VR TDC) conditions. For this reason, the Vcc slewing must be tested under both loading conditions.

During the D-VID test defined in the previous paragraph, Vcc droop and undershoot amplitudes must be limited to avoid processor damage and performance failures. If the processor experiences a voltage undershoot due to D-VID transitions, an application initiated di/dt droop can superimpose with this event and potentially violate minimum voltage specifications. Droop during this D-VID test must be limited

to 5 mV. This value was derived by calculating VRD tolerance band improvements at the low D-VID current and voltage values.

2.6.2.1 VR11 Validation Summary

This exercise tests VRD11 functionality with 12.5 mV VID resolution. Consult Figure 2-13 and Figure 2-15 for graphic representation of validation requirements.

1. Constraints:
    a. 0.7625 V +/-5 mV transition must occur within 350 µs (see Figure 2-13).
    b. Start time is referenced to 0.4 V on the rising edge of the initial D-VID code.
    c. End time is referenced to the steady state Vcc voltage after the final D-VID code.
    d. Undershoot during maximum to minimum VID transition must be limited to 5 mV. This 5 mV is included within the +/-5 mV tolerance on the final VID value defined under test condition a.
    e. Care must be taken to avoid motherboard and component heat damage resulting from extended operations with high current draw.

2. Validation exercises:
    a. D-VID transition must be validated against above constraints from a starting VID of 1.6 V to an ending VID of 0.8375 V with an applied 5A Load.
    b. D-VID transition must be validated against above constraints from a starting VID of 1.6 V to an ending VID of 0. 8375 V with an applied VR TDC Load.
    c. D-VID transition must be validated against above constraints from a starting VID of 0.8375 V to an ending VID of 1.6 V with an applied 5 A Load.
    d. D-VID transition must be validated against above constraints from a starting VID of 0.8375 V to an ending VID of 1.6 V with an applied VR TDC Load.

Figure 2-14 VRD11 DVID Transition Timing States (12.5 mV VID Resolution)

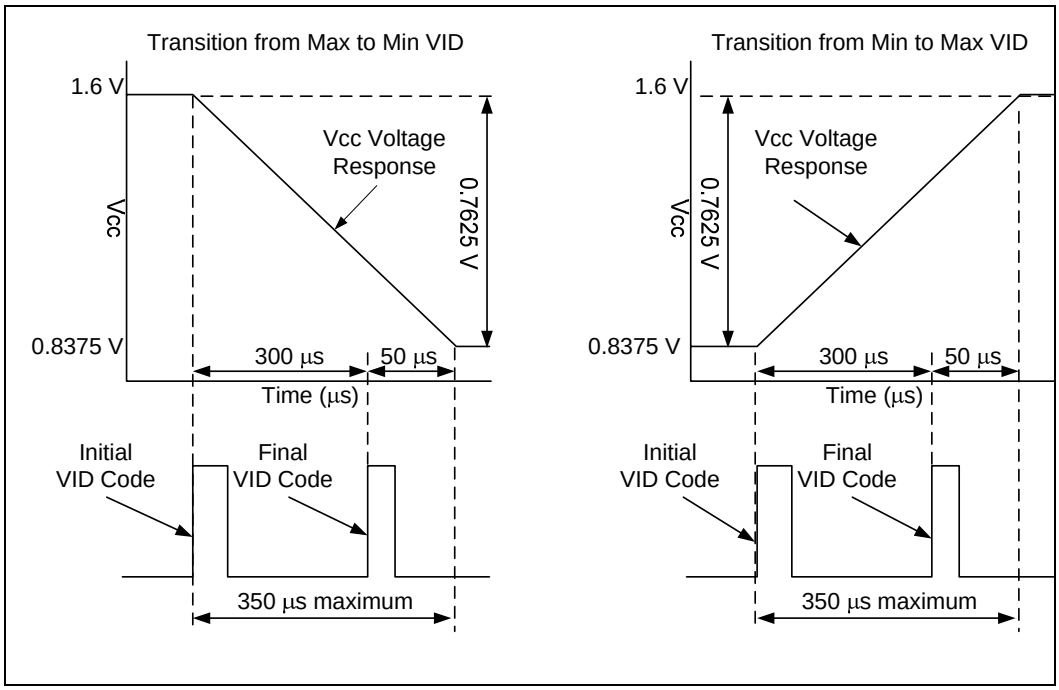
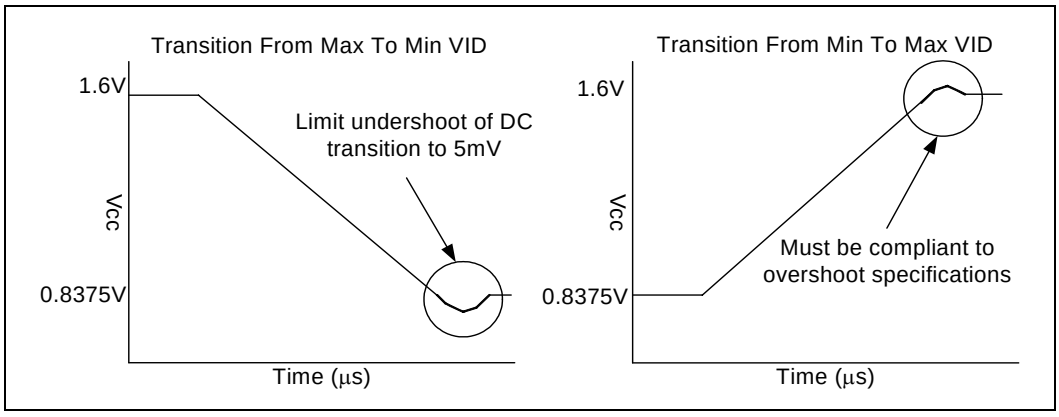


Figure 2-15. Overshoot and Undershoot During Dynamic VID Validation



2.7 Processor Vcc Overshoot (REQUIRED)

2.7.1 Specification Overview

Intel desktop processors in VRD11 systems are capable of tolerating short transient overshoot events above VID on the Vcc supply that will not impact processor lifespan or reliability. Maximum processor Vcc overshoot, V_{OS}, cannot exceed VID+V_{OS_MAX}. Overshoot duration, T_{OS}, cannot stay above VID for a time more than T_{OS_MAX}. See Table 13 and Table 14 for details.

Table 13. Vcc Overshoot Terminology

Parameter	Definition
VOS	Measured peak overshoot voltage
V_{OS_MAX}	Maximum specified overshoot voltage allowed above VID
TOS	Measured overshoot time duration
T_{OS_MAX}	Maximum specified overshoot time duration above VID
Vzc	Zero current voltage: The voltage where the measured load line intercepts the voltage axis
Vzco	Zero current offset from VID: Vzco = VID – Vzc

Table 14. Vcc Overshoot Specifications

Parameter	Specification
VOS_MAX	50 mV
TOS_MAX	25 µs
VOS	Maximum = VID + VOS_MAX
TOS	Maximum = TOS_MAX

Maximum overshoot is validated by monitoring the voltage across the recommended test lands (defined in Section 2.2) while applying a current load release across the socket Vcc and Vss land field. Amperage values for performing this validation under each VRD design configuration are identified in Table 15. The platform voltage regulator output filter must be stuffed with a sufficient quality and number of capacitors to ensure that overshoot stays above VID for a time no longer than T_{OS_MAX} and never exceeds the maximum amplitude of VID+V_{OS_MAX}. Measurements are to be taken using an oscilloscope with a 20 MHz bandwidth. Boards in violation must be redesigned for compliance to avoid processor damage.

Table 15. Intel Processor Current Release Values For Overshoot Testing

VR Configuration	Starting Current	Ending Current	Dynamic Current Step
775_VR_CONFIG_04A	60 A	5 A	55 A
775_VR_CONFIG_04B	100 A	5 A	95 A
775_VR_CONFIG_05A	70 A	5 A	65 A
775_VR_CONFIG_05B	100 A	5 A	95 A
775_VR_CONFIG_06	55 A	5 A	50 A

To prevent processor damage, VRD designs should comply to overshoot specifications across the full socket load line tolerance band window (see Section 2.2). When validating a system's overshoot, a single measurement is statistically insignificant and cannot represent the response variation seen across the entire high volume manufacturing population of VRD designs. A typical design may fit in the socket load line window; however designs residing elsewhere in the tolerance band distribution may violate the Vcc overshoot specifications. Figure 2-17 provides an illustration of this concept. A typical board will have the Vcc zero current voltage (Vzc) centered in the socket load line window at VID-TOB; for this example consider waveform A and

assume TOB is 20 mV. Now assume that the VRD has maximum overshoot amplitude of VOS_MAX = 50 mV above VID. Under this single case, the overshoot aligns with the specification limit and there is zero margin to violation. Under manufacturing variation Vzc can drift to align with VID (waveform B). This drift will shift the overshoot waveform by the same voltage level. Since waveform A has zero overshoot amplitude margin, this increase in Vzc due to manufacturing drift will yield a 20 mV overshoot violation which will reduce the processor life span. To address this issue in validation, a voltage margining technique can be employed to ensure overshoot amplitudes stay below a safe value. This technique translates the specification baseline from VID to a VRD validation baseline of Vzc + VOS_MAX, which defines a test limit for specification compliance across the full TOB range:

Equation 4. Overshoot Voltage Limit

$$VOS < Vzc + VOS\_MAX$$

This equation is to be used during validation to ensure overshoot is in compliance to specifications across high volume manufacturing variation. In addition, the overshoot duration must be reference to Vzc and cannot exceed this level by more than 25 μS.

Figure 2-16. Graphical Representation of Overshoot Parameters

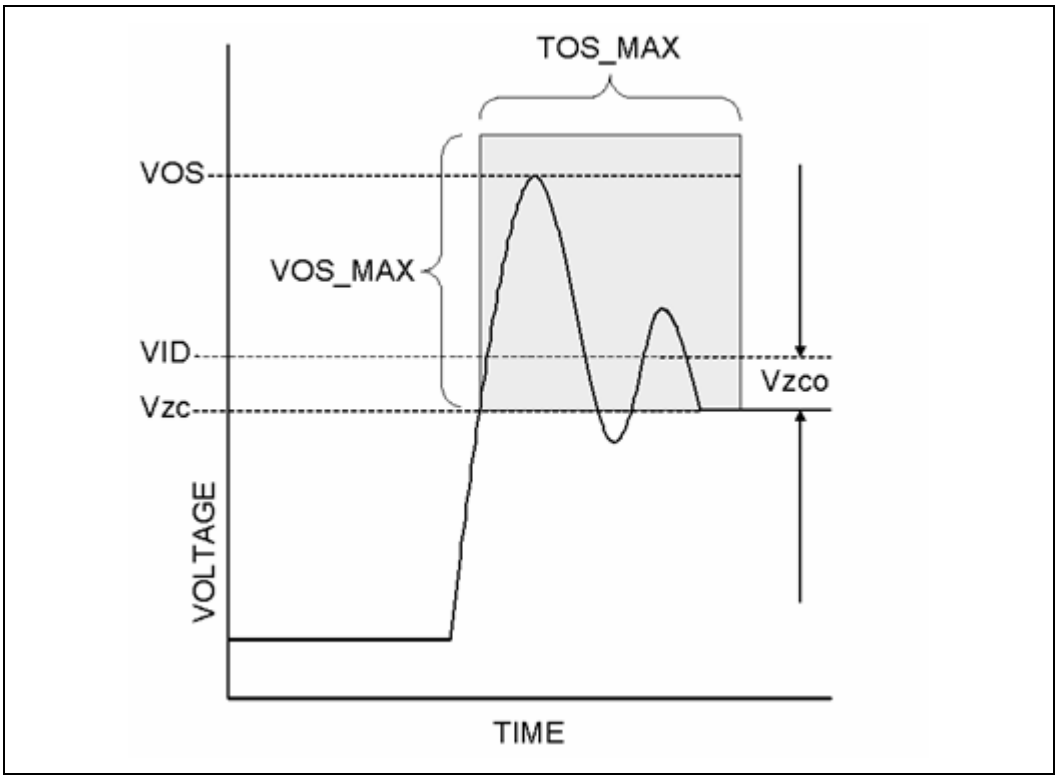


Figure 2-17. Processor Overshoot in High Volume Manufacturing

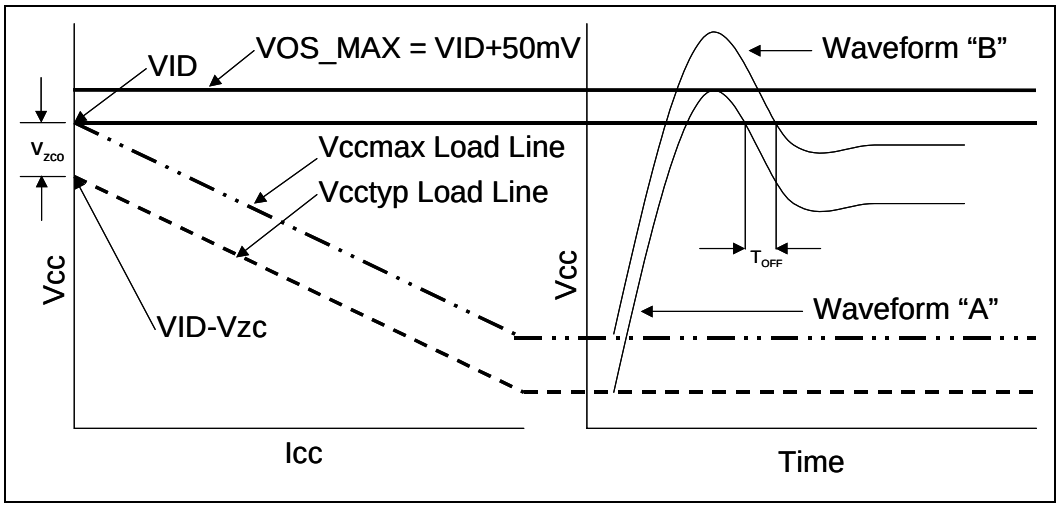
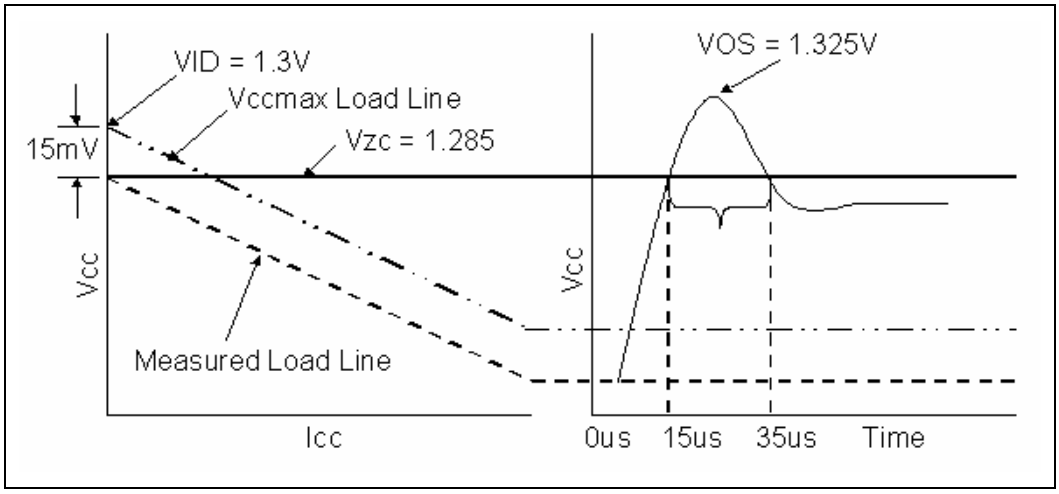


Figure 2-18. Example Socket Vcc Overshoot Waveform



2.7.2 Example: Socket Vcc Overshoot Test

To pass the overshoot specification, the amplitude constraint of Equation 4 and time duration requirement of TOS_MAX must be satisfied. This example references Figure 2-18.

Amplitude Test Constraint: Overshoot amplitude, VOS, must be less than Vzc + VOS_MAX

Input parameters

- VOS= 1.325 V – Obtained from direct measurement
- V_{ZC} = 1.285 V – Obtained from direct measurement
- VOS_Max = 0.050 V – An Intel specified value

Amplitude Analysis:

- V_{ZC} + VOS_MAX = 1.285 V + 0.050 V = 1.335 V
- VOS = 1.325 < 1.335 V

Amplitude Test Satisfied

Time Duration Test Constraint: Overshoot duration above Vzc must be less than 25μs

Input Parameters

- Initial crossing of overshoot: 15 μs – Obtained from direct measurement
- Final crossing of overshoot: 35 μs – Obtained from direct measurement
- TOS_MAX = 25μs – An Intel specified value

Overshoot Duration Analysis

- TOS = Final Crossing of Vzc – Initial Crossing of Vzc
- TOS = 35 μs – 15 μs = 20 μs < 25 μs = TOS_MAX

Time duration test passed

Amplitude and Time Duration Tests Passed => Overshoot specification is satisfied

§

3 Vtt Requirements (REQUIRED)

The Vtt regulator provides power to the processor VID circuitry, the chipset - processor front side bus, and miscellaneous buffer signals. This rail voltage must converge to the amplitude defined in Table 16 to begin power sequencing. The VR11 PWM controller will sense the amplitude of the Vtt rail and initiate power sequencing upon crossing a defined threshold voltage. The Vtt regulator controller does not include an enable signal; valid output voltage of Table 16 must be ensured by the timing protocol defined in Figure 4-2.

3.1 Electrical Specifications

A linear regulator is recommended for the Vtt supply with adequate decoupling capacitors to ensure the sum of AC bus noise and DC tolerance satisfy limits identified in Table 16. The processor and chipset Vtt supply must be maintained within these tolerance limits across full operational thermal limits, part-to-part component variation, age degradation, and regulator accuracy. Full bandwidth bus noise amplitude must be ensured across all Vcc/Vss land pairs defined in Table 17.

The Vtt supply must be unconditionally stable under all DC and transient conditions across the voltage and current ranges defined in Table 16. The Vtt supply must also operate in a no-load condition: i.e., with no processor installed.

Vtt_SEL is an output from the processor that indicates to the Vtt regulator the appropriate output voltage. The Vtt_SEL output is either an open circuit (Vtt_SEL = 1) or directly tied to the processor Vss (Vtt_SEL = 0).

Table 16. Vtt Specifications

Processor	Vtt Min	Vtt Typ	Vtt Max	Itt Min	Itt Typ	Itt Max
775_VR_CONFIG_04A 775_VR_CONFIG_04B 775_VR_CONFIG_05A 775_VR_CONFIG_05B 775_VR_CONFIG_06 Vtt_SEL = 1	1.140 V	1.200 V[1]	1.260 V	0.15 A	3.4 A	5.25 A[2]
Future LGA775 configurations Vtt_SEL = 0	1.045 V	1.100 V[1]	1.155 V	0.15 A	3.4 A	5.25 A[2]

NOTES:
1. Combined DC and Transient voltage tolerance is 5%, with a maximum 2% DC tolerance.
2. Itt can be up to 7.5 A at power-up. This is applicable when Vcc is low and Vtt is high.

Table 17. Vtt Measurement Lands

Device	Supply	Land
Processor	Vtt	D25
Processor	Vss	E25

§

4 Power Sequencing (REQUIRED)

VR11 features a power sequence that is compatible with both VR11 and VR10 processors. To avoid compatibility problems with VR11 architecture, VR11 designs must not use the legacy VR10 start sequence.

Desktop VR11 systems use a pull-up resistor tied to the Vtt supply as an enable signal. Once the PWM Vcc voltage is above its under voltage lockout (UVLO) threshold, out of configuration states such as reset, and a valid enable signal is received, the PWM is to initiate the start up sequence with TD1.

The PWM should ramp Vcc to the default 'Vboot' value and start a timer. It will remain at the Vboot voltage during TD3 and then read in the VID lines and ramp to the programmed VID voltage. See timing diagram Figure 4-2 for details on the power-on sequence requirements.

4.1 VR_ENABLE

VR_ENABLE pin is a level sensitive logic input that is externally pulled up to the front side bus termination voltage rail (Vtt) rail in the system. The threshold for turn on is V_{TH} with a hysteresis of V_{HYS} as shown in Table 18. The VR_ENABLE input should have a 3-dB bandwidth of approximately 20 MHz to reject high frequency noise. If enable goes low during the start up sequence the PWM should re-start the start up sequence.

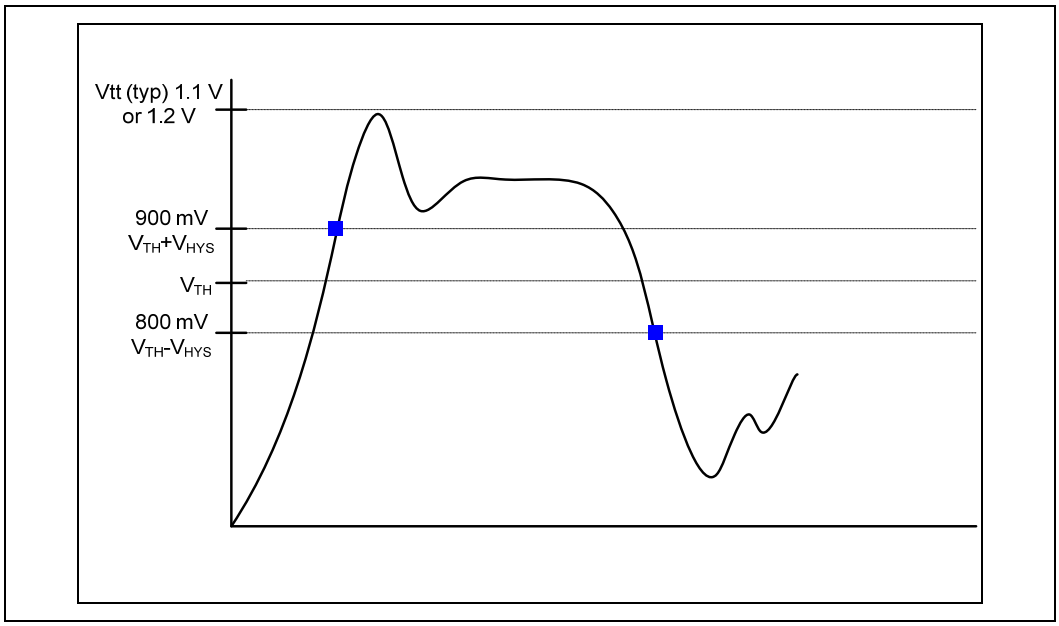
An example of the switching thresholds for the typical case is shown in Figure 4-1 below.

When VR_ENABLE is pulled low or disabled, VR_READY should be de-asserted and the DC-DC output should be in a high-impedance state and should not sink current. During the shut down process, no negative voltage below –100 mV may be present at the DC-DC output when loaded with a resistive load or microprocessor in the system. Some electronic loads with long leads may cause false readings at turn off.

Table 18. VR_ENABLE Input Threshold

Parameter	Description	Min	Typ	Max	Units
V_{TH}	Threshold voltage	800	850	900	mV
V_{HYS}	Hysteresis	70	100	130	mV

Figure 4-1. VR_ENABLE Typical Levels Example



4.2 Vboot voltage level

Vboot is a default power-on Vcc value. Upon detection of a valid Vtt supply, the PWM controller is to regulate the VRD to this value until VID codes are read. The Vboot voltage is 1.1 V. During Vboot, the output should operate with a load line as if the VID=1.1 V.

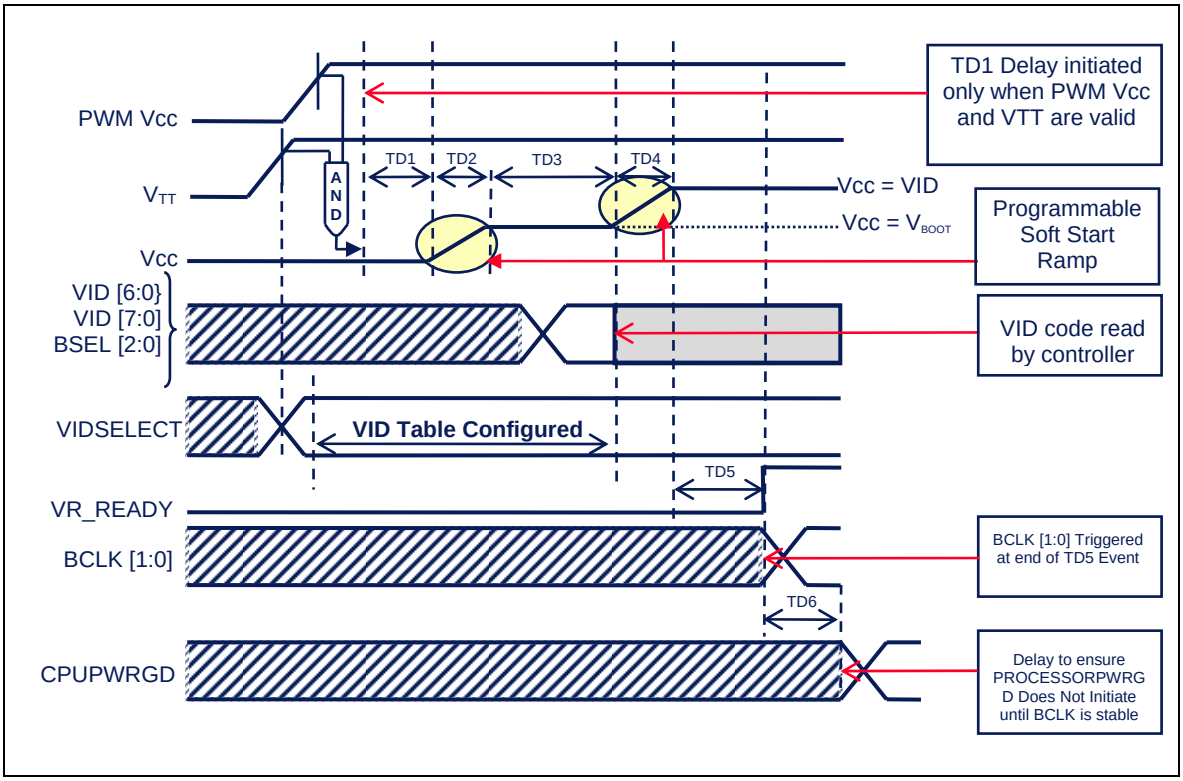
4.3 Under Voltage Lock Out (UVLO)

The PWM IC should detect its voltage rail and remain in the disabled state until a valid voltage level is available or reached. The voltage level is typically 3.0 V in a 3.3 V system, 4.0 V in a 5 V system or 7-8 V in a 12 V system. Ultimately the PWM vendor should set the level to meet his market segment requirements. However, the PWM and MOSFET driver components should coordinate start up such that both the PWM input voltage rail and power conversion input voltage rail (typically +12 V) of the buck converter are both up and valid prior to enabling the PWM function. The PWM and MOSFET driver component combinations need to be tolerant of any sequencing combination of 3.3 V, 5 V or 12 V input rails. If the PWM IC voltage rail, MOSFET driver voltage rail or power conversion rail fall below the UVLO thresholds, the PWM should shut down in an orderly manner and restart the start up sequence.

4.4 Soft Start (SS)

The PWM controller should have a soft start function to limit inrush current into the output capacitor bank and prevent false over current protection (OCP) trips. The soft start should have a ramp of 500 µs as an internally programmed default. A SS pin for user programmability of SS ramp to extend the ramp to 1-5 ms is required. Consult TD2 and TD4 parameters in Figure 4-2 for further details.

Figure 4-2 Start up sequence (Timing is not to scale, details in Table 19)



NOTE: Consult platform design guidelines for further details regarding BCLK and CPUPWRGD

Figure 4-3 Power-off timing sequence (Timing is not to scale, details in Table 19)

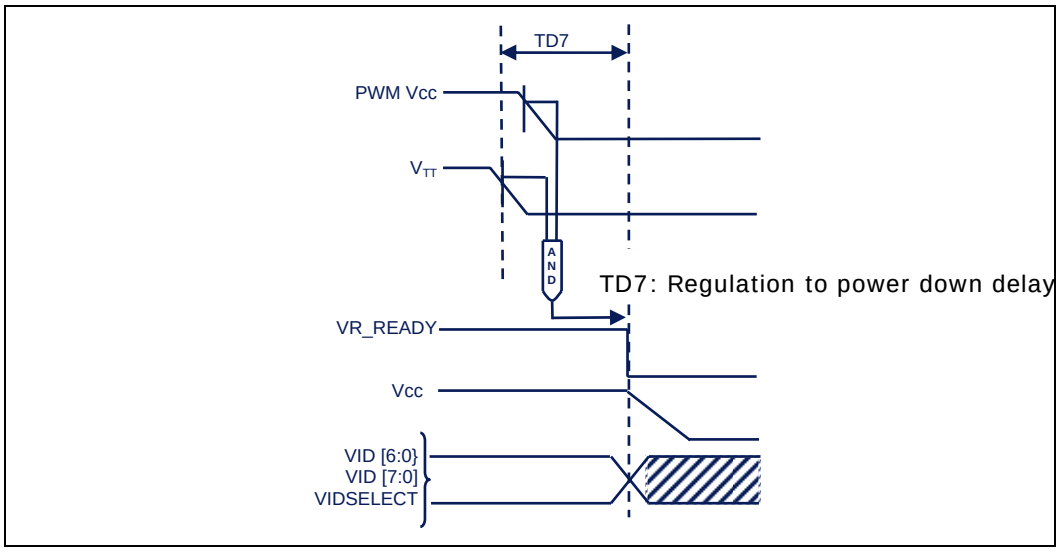


Figure 4-4. TD7 Reference Levels

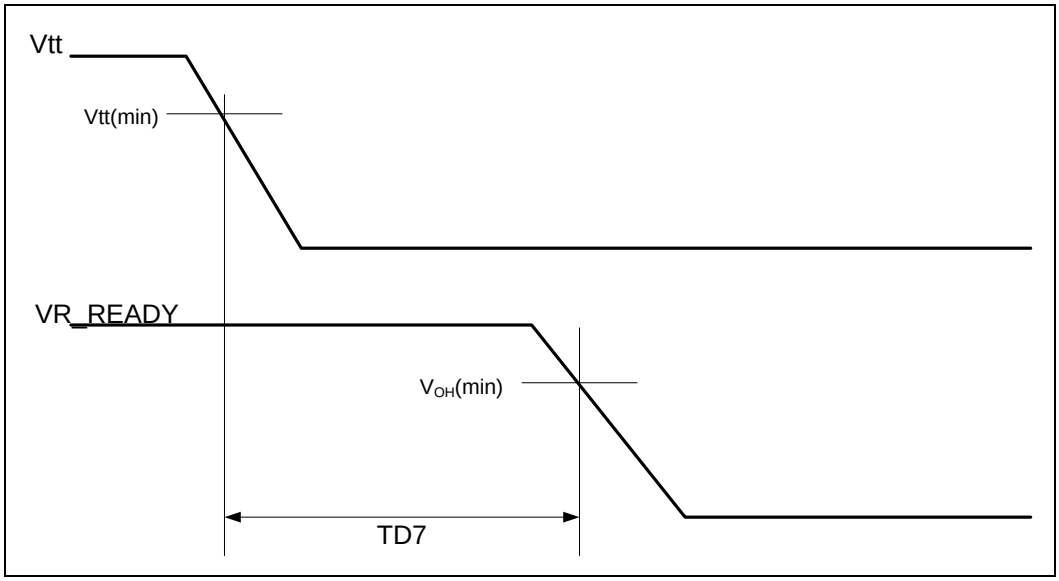
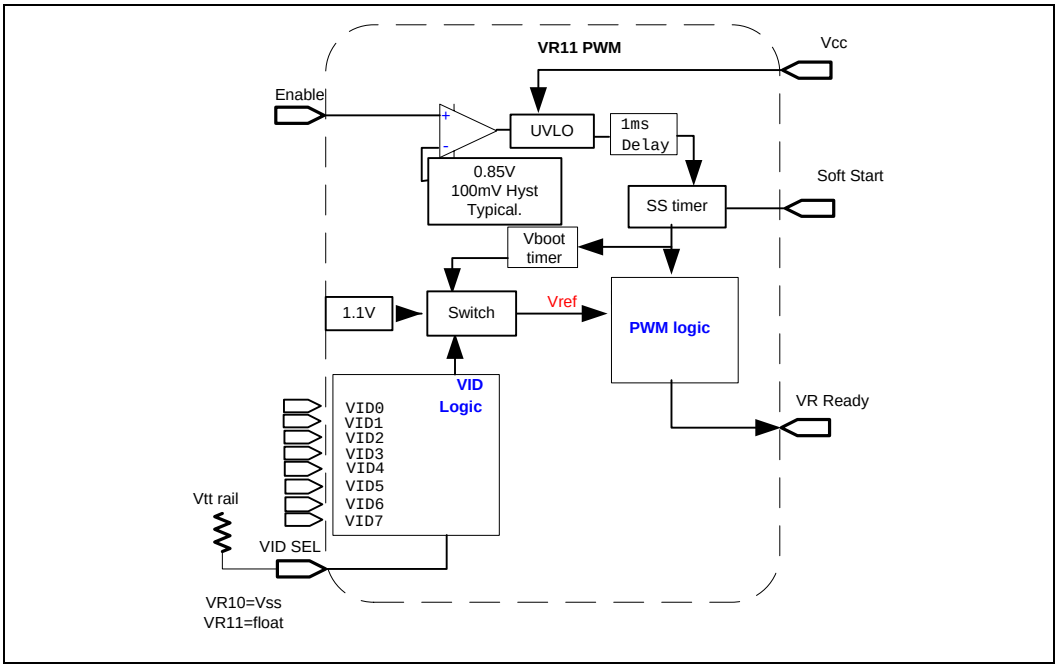


Table 19. Start Up Sequence Timing

Start up Delay Parameters			
Parameter	**Minimum**	**Typical, Default**	**Maximum**
TD1	1 ms	-	5 ms
TD2	0 ms	500 µs	5 ms
TD3	50 µs	-	3 ms
TD4	0 µs	250 µs	2.5 ms
TD5	0 ms	-	3 ms
TD6	1.8 ms	-	-
TD7	0 ms	-	1 ms

Figure 4-5. Start Up Sequence Functional Block Diagram



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5 VRD Current Support (Required)

System boards supporting LGA775 socket processors must have voltage regulator designs compliant to electrical and thermal standards defined in Table 4. This includes full electrical support of Iccmax specifications and robust cooling solutions to support defined thermal design current (VR TDC) indefinitely within the envelope of system operating conditions. This includes regulator layout, processor fan selection, ambient temperature, chassis configuration, etc. Consult Table 4 and Table 16 for processor Vcc and Vtt current limits.

Intel processor VR TDC is the sustained (DC equivalent) current that is to be used for voltage regulator thermal design with supporting Thermal Monitor circuitry (see section 9.3). At VR TDC, components such as switching FETs and inductors reach maximum temperature, heating the motherboard layers and neighboring components to the pass/fail boundary of thermal limits. Thermal analysis must include current contributions of both the Vcc and Vtt regulators. In some instances the processor VRD will also power other motherboard components. Under this condition the VRD will supply current above the VR TDC limits; system designers must budget this additional current support in final VRD designs while remaining compliant to electrical and thermal specifications.

To avoid heat related failures, desktop computer systems should be validated for thermal compliance under the envelope of system operating conditions.

5.1 Phase Count Requirement

The PWM controller will be used in DC-DC converters that support processors from 60 A to 140 A TDC. It is expected that the PWM chip manufacturer will determine the optimal number of phases for a low cost design and allow for flexible implementations to meet various market segment requirements.

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6 Control Inputs

6.1 Voltage Identification (VID [7:0]) (REQUIRED)

The VRD must accept an 8-bit code transmitted by the processor to establish the reference Vcc operating voltage. Two VID Code standards must be supported. The first VID code standard is an extended VR10 table (Table 21) that is fully compliant to the VR10 standard, but adds an additional (least significant) bit for 6.25 mV VID resolution. The second VID code standard is the VR11 standard defined in Table 22. The processor will identify which table is to be used by configuring the logic state bias on the VID_SEL pin.

When an 'OFF' VID code appears at the input to the PWM controller, the DC-DC is to turn off the Vcc output within 0.5 seconds and latch off until power is cycled.

While operating in the D-VID mode, Intel processors can transmit VID codes across the eight bit bus with a 5 μs data transmission rate. To properly design this bus against timing and signal integrity requirements (Table 20), the following information is provided. The VID buffer circuit varies with processor generation and can be an open-drain or push-pull CMOS circuit configuration. The VID bus must be designed to be compatible with each circuit; therefore a pull-up resistor is required to bias the open drain configuration. The worst-case settling time requirement for code transmission at each load is 400 nanoseconds, including line-to-line skew. VRD controller VID inputs should contain circuitry to detect a change and prevent false tripping or latching of VID codes during this 400-nanosecond window.

Intel recommends use of the D-VID bus topology described in Figure 6-1 and Table 20. Under these conditions, traces can be routed with micro strip, strip line, or a combination with a maximum of four layer transitions. The main trace length can vary between ½ inch and 15 inches with a maximum recommended line to line skew of 1 inch. The 680 Ω +/-10% pull-up resistor can be placed at any location on the trace with a maximum stub length of 1 inch.

Some designs may require additional VID bus loads. In this case, care should be taken to design the topology to avoid excessive undershoot and overshoot at each load. Failure to comply with these limits may lead to component damage or cause premature failure. The responsible engineer must identify minimum and maximum limits of each component and design a topology that ensures voltages stay within these limits at all times.

Figure 6-1. D-VID Bus Topology

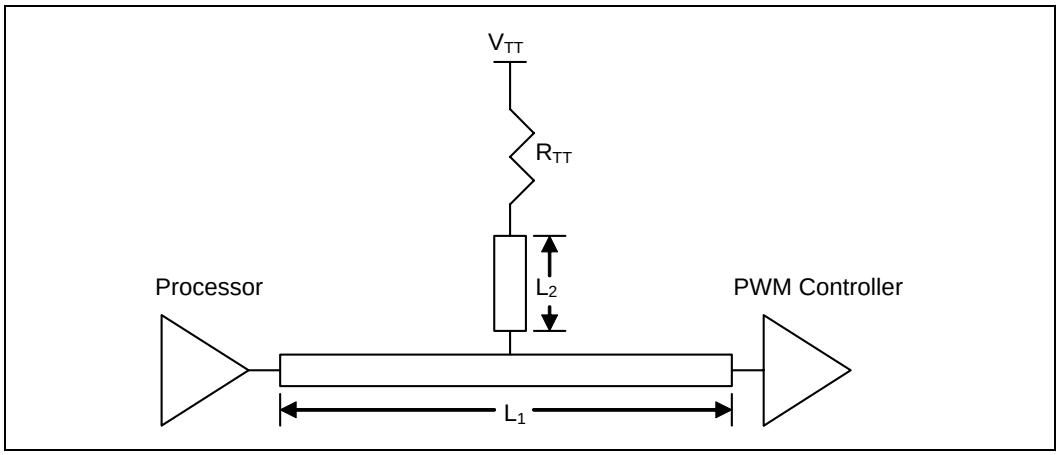


Table 20. VID Buffer and VID Bus Electrical Parameters

Design Parameter	Minimum	Typical	Maximum
VID Bus Voltage	-	Vtt[1]	-
Voltage Limits At Processor VID Lands	- 0.100 V	-	Vtt[2]
V_{IH}	0.8 V	-	-
V_{IL}	-	-	0.3 V
L_1, VID trace length	0.5 inch	-	15 inches
L_2, Vtt Stub Length	0 inch	-	1 inch
VID trace length skew	-	1.0 inch	-
VID trace width	5 mils	-	-
VID trace separation	5 mils	-	-
R_{TT}, Pull-Up Resistor	620 Ω[3]	680 Ω	750 Ω[4]

NOTES:
1: Consult Table 16 for Vtt specifications
2: Consult the processor datasheet for signal overshoot limits
3: Value represents minimum resistance at tolerance limits
4: Value represents maximum resistance at tolerance limits

Table 21. Extended VRD10 Voltage Identification (VID) Table

VID6	VID5	VID4	VID3	VID2	VID1	VID0	Voltage
0	1	1	1	1	1	1	OFF
1	1	1	1	1	1	1	OFF
0	0	1	1	1	1	1	OFF
1	0	1	1	1	1	1	OFF
1	1	0	1	0	1	0	1.60000
0	1	0	1	0	1	0	1.59375
1	0	0	1	0	1	1	1.58750
0	0	0	1	0	1	1	1.58125
1	1	0	1	0	1	1	1.57500
0	1	0	1	0	1	1	1.56875
1	0	0	1	1	0	0	1.56250
0	0	0	1	1	0	0	1.55625
1	1	0	1	1	0	0	1.55000
0	1	0	1	1	0	0	1.54375
1	0	0	1	1	0	1	1.53750
0	0	0	1	1	0	1	1.53125
1	1	0	1	1	0	1	1.52500
0	1	0	1	1	0	1	1.51875
1	0	0	1	1	1	0	1.51250
0	0	0	1	1	1	0	1.50625
1	1	0	1	1	1	0	1.50000
0	1	0	1	1	1	0	1.49375
1	0	0	1	1	1	1	1.48750
0	0	0	1	1	1	1	1.48125
1	1	0	1	1	1	1	1.47500
0	1	0	1	1	1	1	1.46875
1	0	1	0	0	0	0	1.46250
0	0	1	0	0	0	0	1.45625
1	1	1	0	0	0	0	1.45000
0	1	1	0	0	0	0	1.44375
1	0	1	0	0	0	1	1.43750
0	0	1	0	0	0	1	1.43125
1	1	1	0	0	0	1	1.42500
0	1	1	0	0	0	1	1.41875
1	0	1	0	0	1	0	1.41250
0	0	1	0	0	1	0	1.40625
1	1	1	0	0	1	0	1.40000
0	1	1	0	0	1	0	1.39375
1	0	1	0	0	1	1	1.38750

VID6	VID5	VID4	VID3	VID2	VID1	VID0	Voltage
0	0	1	0	0	1	1	1.38125
1	1	1	0	0	1	1	1.37500
0	1	1	0	0	1	1	1.36875
1	0	1	0	1	0	0	1.36250
0	0	1	0	1	0	0	1.35625
1	1	1	0	1	0	0	1.35000
0	1	1	0	1	0	0	1.34375
1	0	1	0	1	0	1	1.33750
0	0	1	0	1	0	1	1.33125
1	1	1	0	1	0	1	1.32500
0	1	1	0	1	0	1	1.31875
1	0	1	0	1	1	0	1.31250
0	0	1	0	1	1	0	1.30625
1	1	1	0	1	1	0	1.30000
0	1	1	0	1	1	0	1.29375
1	0	1	0	1	1	1	1.28750
0	0	1	0	1	1	1	1.28125
1	1	1	0	1	1	1	1.27500
0	1	1	0	1	1	1	1.26875
1	0	1	1	0	0	0	1.26250
0	0	1	1	0	0	0	1.25625
1	1	1	1	0	0	0	1.25000
0	1	1	1	0	0	0	1.24375
1	0	1	1	0	0	1	1.23750
0	0	1	1	0	0	1	1.23125
1	1	1	1	0	0	1	1.22500
0	1	1	1	0	0	1	1.21875
1	0	1	1	0	1	0	1.21250
0	0	1	1	0	1	0	1.20625
1	1	1	1	0	1	0	1.20000
0	1	1	1	0	1	0	1.19375
1	0	1	1	0	1	1	1.18750
0	0	1	1	0	1	1	1.18125
1	1	1	1	0	1	1	1.17500
0	1	1	1	0	1	1	1.16875
1	0	1	1	1	0	0	1.16250
0	0	1	1	1	0	0	1.15625
1	1	1	1	1	0	0	1.15000
0	1	1	1	1	0	0	1.14375
1	0	1	1	1	0	1	1.13750
0	0	1	1	1	0	1	1.13125

VID6	VID5	VID4	VID3	VID2	VID1	VID0	Voltage
1	1	1	1	1	0	1	1.12500
0	1	1	1	1	0	1	1.11875
1	0	1	1	1	1	0	1.11250
0	0	1	1	1	1	0	1.10625
1	1	1	1	1	1	0	1.10000
0	1	1	1	1	1	0	1.09375
1	0	0	0	0	0	0	1.08750
0	0	0	0	0	0	0	1.08125
1	1	0	0	0	0	0	1.07500
0	1	0	0	0	0	0	1.06875
1	0	0	0	0	0	1	1.06250
0	0	0	0	0	0	1	1.05625
1	1	0	0	0	0	1	1.05000
0	1	0	0	0	0	1	1.04375
1	0	0	0	0	1	0	1.03750
0	0	0	0	0	1	0	1.03125
1	1	0	0	0	1	0	1.02500
0	1	0	0	0	1	0	1.01875
1	0	0	0	0	1	1	1.01250
0	0	0	0	0	1	1	1.00625
1	1	0	0	0	1	1	1.00000
0	1	0	0	0	1	1	0.99375
1	0	0	0	1	0	0	0.98750
0	0	0	0	1	0	0	0.98125
1	1	0	0	1	0	0	0.97500
0	1	0	0	1	0	0	0.96875
1	0	0	0	1	0	1	0.96250
0	0	0	0	1	0	1	0.95625
1	1	0	0	1	0	1	0.95000
0	1	0	0	1	0	1	0.94375
1	0	0	0	1	1	0	0.93750
0	0	0	0	1	1	0	0.93125
1	1	0	0	1	1	0	0.92500
0	1	0	0	1	1	0	0.91875
1	0	0	0	1	1	1	0.91250
0	0	0	0	1	1	1	0.90625
1	1	0	0	1	1	1	0.90000
0	1	0	0	1	1	1	0.89375
1	0	0	1	0	0	0	0.88750
0	0	0	1	0	0	0	0.88125
1	1	0	1	0	0	0	0.87500

VID6	VID5	VID4	VID3	VID2	VID1	VID0	Voltage
0	1	0	1	0	0	0	0.86875
1	0	0	1	0	0	1	0.86250
0	0	0	1	0	0	1	0.85625
1	1	0	1	0	0	1	0.85000
0	1	0	1	0	0	1	0.84375
1	0	0	1	0	1	0	0.83750
0	0	0	1	0	1	0	0.83125

NOTES:
1. The Vcc output is disabled upon communication of an OFF VID code.
2. VID [4:0] are compatible with Intel desktop processors using five-bit VID codes.
3. VID [5:0] will be used on processors with six-bit codes.

Table 22. VR11 VID Table

VID7	VID6	VID5	VID4	VID3	VID2	VID1	VID0	Voltage
0	0	0	0	0	0	0	0	OFF
0	0	0	0	0	0	0	1	OFF
0	0	0	0	0	0	1	0	1.60000
0	0	0	0	0	0	1	1	1.59375
0	0	0	0	0	1	0	0	1.58750
0	0	0	0	0	1	0	1	1.58125
0	0	0	0	0	1	1	0	1.57500
0	0	0	0	0	1	1	1	1.56875
0	0	0	0	1	0	0	0	1.56250
0	0	0	0	1	0	0	1	1.55625
0	0	0	0	1	0	1	0	1.55000
0	0	0	0	1	0	1	1	1.54375
0	0	0	0	1	1	0	0	1.53750
0	0	0	0	1	1	0	1	1.53125
0	0	0	0	1	1	1	0	1.52500
0	0	0	0	1	1	1	1	1.51875
0	0	0	1	0	0	0	0	1.51250
0	0	0	1	0	0	0	1	1.50625
0	0	0	1	0	0	1	0	1.50000
0	0	0	1	0	0	1	1	1.49375
0	0	0	1	0	1	0	0	1.48750
0	0	0	1	0	1	0	1	1.48125
0	0	0	1	0	1	1	0	1.47500

VID7	VID6	VID5	VID4	VID3	VID2	VID1	VID0	Voltage
0	1	0	1	1	0	1	1	1.04375
0	1	0	1	1	1	0	0	1.03750
0	1	0	1	1	1	0	1	1.03125
0	1	0	1	1	1	1	0	1.02500
0	1	0	1	1	1	1	1	1.01875
0	1	1	0	0	0	0	0	1.01250
0	1	1	0	0	0	0	1	1.00625
0	1	1	0	0	0	1	0	1.00000
0	1	1	0	0	0	1	1	0.99375
0	1	1	0	0	1	0	0	0.98750
0	1	1	0	0	1	0	1	0.98125
0	1	1	0	0	1	1	0	0.97500
0	1	1	0	0	1	1	1	0.96875
0	1	1	0	1	0	0	0	0.96250
0	1	1	0	1	0	0	1	0.95625
0	1	1	0	1	0	1	0	0.95000
0	1	1	0	1	0	1	1	0.94375
0	1	1	0	1	1	0	0	0.93750
0	1	1	0	1	1	0	1	0.93125
0	1	1	0	1	1	1	0	0.92500
0	1	1	0	1	1	1	1	0.91875
0	1	1	1	0	0	0	0	0.91250
0	1	1	1	0	0	0	1	0.90625

VID7	VID6	VID5	VID4	VID3	VID2	VID1	VID0	Voltage
0	0	0	1	0	1	1	1	1.46875
0	0	0	1	1	0	0	0	1.46250
0	0	0	1	1	0	0	1	1.45625
0	0	0	1	1	0	1	0	1.45000
0	0	0	1	1	0	1	1	1.44375
0	0	0	1	1	1	0	0	1.43750
0	0	0	1	1	1	0	1	1.43125
0	0	0	1	1	1	1	0	1.42500
0	0	0	1	1	1	1	1	1.41875
0	0	1	0	0	0	0	0	1.41250
0	0	1	0	0	0	0	1	1.40625
0	0	1	0	0	0	1	0	1.40000
0	0	1	0	0	0	1	1	1.39375
0	0	1	0	0	1	0	0	1.38750
0	0	1	0	0	1	0	1	1.38125
0	0	1	0	0	1	1	0	1.37500
0	0	1	0	0	1	1	1	1.36875
0	0	1	0	1	0	0	0	1.36250
0	0	1	0	1	0	0	1	1.35625
0	0	1	0	1	0	1	0	1.35000
0	0	1	0	1	0	1	1	1.34375
0	0	1	0	1	1	0	0	1.33750
0	0	1	0	1	1	0	1	1.33125
0	0	1	0	1	1	1	0	1.32500
0	0	1	0	1	1	1	1	1.31875
0	0	1	1	0	0	0	0	1.31250
0	0	1	1	0	0	0	1	1.30625
0	0	1	1	0	0	1	0	1.30000
0	0	1	1	0	0	1	1	1.29375
0	0	1	1	0	1	0	0	1.28750
0	0	1	1	0	1	0	1	1.28125
0	0	1	1	0	1	1	0	1.27500
0	0	1	1	0	1	1	1	1.26875
0	0	1	1	1	0	0	0	1.26250
0	0	1	1	1	0	0	1	1.25625

VID7	VID6	VID5	VID4	VID3	VID2	VID1	VID0	Voltage
0	1	1	1	0	0	1	0	0.90000
0	1	1	1	0	0	1	1	0.89375
0	1	1	1	0	1	0	0	0.88750
0	1	1	1	0	1	0	1	0.88125
0	1	1	1	0	1	1	0	0.87500
0	1	1	1	0	1	1	1	0.86875
0	1	1	1	1	0	0	0	0.86250
0	1	1	1	1	0	0	1	0.85625
0	1	1	1	1	0	1	0	0.85000
0	1	1	1	1	0	1	1	0.84375
0	1	1	1	1	1	0	0	0.83750
0	1	1	1	1	1	0	1	0.83125
0	1	1	1	1	1	1	0	0.82500
0	1	1	1	1	1	1	1	0.81875
1	0	0	0	0	0	0	0	0.81250
1	0	0	0	0	0	0	1	0.80625
1	0	0	0	0	0	1	0	0.80000
1	0	0	0	0	0	1	1	0.79375
1	0	0	0	0	1	0	0	0.78750
1	0	0	0	0	1	0	1	0.78125
1	0	0	0	0	1	1	0	0.77500
1	0	0	0	0	1	1	1	0.76875
1	0	0	0	1	0	0	0	0.76250
1	0	0	0	1	0	0	1	0.75625
1	0	0	0	1	0	1	0	0.75000
1	0	0	0	1	0	1	1	0.74375
1	0	0	0	1	1	0	0	0.73750
1	0	0	0	1	1	0	1	0.73125
1	0	0	0	1	1	1	0	0.72500
1	0	0	0	1	1	1	1	0.71875
1	0	0	1	0	0	0	0	0.71250
1	0	0	1	0	0	0	1	0.70625
1	0	0	1	0	0	1	0	0.70000
1	0	0	1	0	0	1	1	0.69375
1	0	0	1	0	1	0	0	0.68750

VID7	VID6	VID5	VID4	VID3	VID2	VID1	VID0	Voltage
0	0	1	1	1	0	1	0	1.25000
0	0	1	1	1	0	1	1	1.24375
0	0	1	1	1	1	0	0	1.23750
0	0	1	1	1	1	0	1	1.23125
0	0	1	1	1	1	1	0	1.22500
0	0	1	1	1	1	1	1	1.21875
0	1	0	0	0	0	0	0	1.21250
0	1	0	0	0	0	0	1	1.20625
0	1	0	0	0	0	1	0	1.20000
0	1	0	0	0	0	1	1	1.19375
0	1	0	0	0	1	0	0	1.18750
0	1	0	0	0	1	0	1	1.18125
0	1	0	0	0	1	1	0	1.17500
0	1	0	0	0	1	1	1	1.16875
0	1	0	0	1	0	0	0	1.16250
0	1	0	0	1	0	0	1	1.15625
0	1	0	0	1	0	1	0	1.15000
0	1	0	0	1	0	1	1	1.14375
0	1	0	0	1	1	0	0	1.13750
0	1	0	0	1	1	0	1	1.13125
0	1	0	0	1	1	1	0	1.12500
0	1	0	0	1	1	1	1	1.11875
0	1	0	1	0	0	0	0	1.11250
0	1	0	1	0	0	0	1	1.10625
0	1	0	1	0	0	1	0	1.10000
0	1	0	1	0	0	1	1	1.09375
0	1	0	1	0	1	0	0	1.08750
0	1	0	1	0	1	0	1	1.08125
0	1	0	1	0	1	1	0	1.07500
0	1	0	1	0	1	1	1	1.06875
0	1	0	1	1	0	0	0	1.06250
0	1	0	1	1	0	0	1	1.05625
0	1	0	1	1	0	1	0	1.05000

VID7	VID6	VID5	VID4	VID3	VID2	VID1	VID0	Voltage
1	0	0	1	0	1	0	1	0.68125
1	0	0	1	0	1	1	0	0.67500
1	0	0	1	0	1	1	1	0.66875
1	0	0	1	1	0	0	0	0.66250
1	0	0	1	1	0	0	1	0.65625
1	0	0	1	1	0	1	0	0.65000
1	0	0	1	1	0	1	1	0.64375
1	0	0	1	1	1	0	0	0.63750
1	0	0	1	1	1	0	1	0.63125
1	0	0	1	1	1	1	0	0.62500
1	0	0	1	1	1	1	1	0.61875
1	0	1	0	0	0	0	0	0.61250
1	0	1	0	0	0	0	1	0.60625
1	0	1	0	0	0	1	0	0.60000
1	0	1	0	0	0	1	1	0.59375
1	0	1	0	0	1	0	0	0.58750
1	0	1	0	0	1	0	1	0.58125
1	0	1	0	0	1	1	0	0.57500
1	0	1	0	0	1	1	1	0.56875
1	0	1	0	1	0	0	0	0.56250
1	0	1	0	1	0	0	1	0.55625
1	0	1	0	1	0	1	0	0.55000
1	0	1	0	1	0	1	1	0.54375
1	0	1	0	1	1	0	0	0.53750
1	0	1	0	1	1	0	1	0.53125
1	0	1	0	1	1	1	0	0.52500
1	0	1	0	1	1	1	1	0.51875
1	0	1	1	0	0	0	0	0.51250
1	0	1	1	0	0	0	1	0.50625
1	0	1	1	0	0	1	0	0.50000
1	1	1	1	1	1	1	0	OFF
1	1	1	1	1	1	1	1	OFF

6.2 VID_SEL: VID Table Selection (REQUIRED)

VID_SEL is an input that determines which VID code table to use. It is a static line that is programmed by the processor package pin bonding. A logic 0 = VR10 VID mode, logic 1= VR11 VID mode. This line will be pulled up externally to Vtt rail with a 680 Ω +/-10% pull-up resistor. The PWM should sample VID_SEL during the TD1 time period at startup and select the proper VID table definition. See Figure 4-2.

Note that VR10 and VR11 VID pins do not have the same voltage weight. The VID_SEL line will select the appropriate VR10 or VR11 table and remap the external VID (0-7) pins to the appropriate DAC input. The VID select will not toggle during normal operation.

6.3 Differential Remote Sense Input (REQUIRED)

The PWM controller must include differential sense inputs (remote sense, remote sense return) to compensate for an output voltage offset of ≤ 300 mV in the power distribution path and in the return path loop. The remote sense lines should draw no more than 2.0 mA to minimize offset errors. The remote sense input needs to have sufficient CMRR to not pass and amplify high frequency processor noise to the VR output. Refer to Section 2.2 for the measurement location.

§

7 Input Voltage and Current

7.1 Input Voltages (EXPECTED)

VRD output voltage is supplied via DC-to-DC power conversion. To ensure proper operation, the input supplies to these regulators must satisfy the following conditions.

7.1.1 Desktop Input Voltages

The main power source for the Vcc VRD is 12 V ±15% and 3.3 V ±5% for the Vtt supply. These voltages are supplied by an AC-DC power supply through a dedicated 12 V cable to the motherboard VRD input. For input voltages outside the normal operating range, the VRD should either operate properly or shut down. The 1 A/µs slew rate specification for the input current is no longer a design requirement. Intel recommends a DC-DC regulator input filter with a minimum 1000 µF to ensure proper loading of the 12 V power source.

7.1.2 Efficiency (EXPECTED)

Table 23 shows the expected VR efficiency for each of the VR configurations. The input voltage of efficiency testing should be 11 VDC. This input voltage will represent the worst case input voltage to the VRD under a high load condition.

Voltage regulator efficiency is measured from the 12 V voltage regulator input to the socket loadline reference node. See Table 10 and Figure 2-7 for more details on the socket loadline reference node.

Table 23. VR Efficiency Guidelines

	VR Efficiency per loading level		
Configuration	**Idle (20% of Icc(max))**	**VR_TDC**	**Icc(max)**
775_VR_CONFIG_04A	-	75%	-
775_VR_CONFIG_04B	-	75%	-
775_VR_CONFIG_05A	-	75%	-
775_VR_CONFIG_05B	-	75%	75% (80% preferred)
775_VR_CONFIG_06	75%	-	-

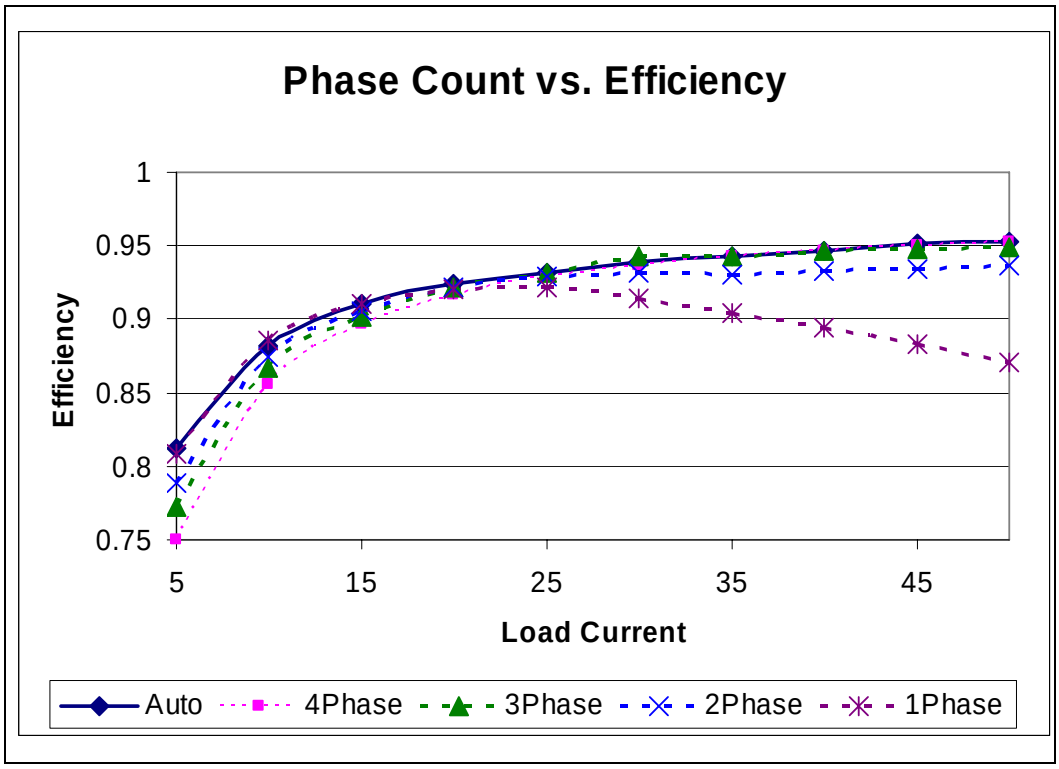
7.1.3 Dynamic Phase Enabling (PROPOSED)

Light load efficiency and power loss improvements can be accomplished by adopting a mode of operation known as dynamic phase enabling. In this mode, the VR controller turns phases on or off as a function of current. At light load conditions, current can be supported with a fewer number of phases; turning off the unnecessary phases will reduce the FET switching power loss. During this mode of operation, the controller will need to realign the phase timing to ensure proper firing at 360°/n (where n is the number of 'on' phases). The figures below show roughly a 2% efficiency improvement for each phase turned off during light load conditions.

The control algorithm for Dynamic Phase Enabling is resident in the VR controller. The voltage regulator must remain stable and satisfy all load line and tolerance band requirements when switching phases on and off. The controller must include features that enable the design engineer to configure the current values where phases switch on or off. This allows the VR design to be optimized for efficiency based on board and component values. In addition, the controller must include hooks to enable validation with the ability to configure the VR functionality in any phase configuration (forced one phase on, forced two phases on, etc; auto mode with one phase on, auto mode with two phases on, etc.).

This topic is essential as computers spend a majority of their time in low utilization conditions. Improving the efficiency at light loads will reduce the energy used by the computer, thereby lowering the user's total cost of ownership and heat generation.

Figure 7-1. DPE Efficiency Example



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8 Output Protection

This section describes features built into the DC-DC regulator to prevent damage to itself, the processor, validation tools, or other system components.

8.1 Over-Voltage Protection (OVP) (PROPOSED)

OVP is proposed to protect the processor from high voltage damage that may lead to failure, or a reduced processor life span. The OVP circuit is to monitor Vcc for an over-voltage condition at the defined regulation lands. This voltage must never exceed VID+200 mV under any condition and operation above this level defines an OVP violation. In the event of an OVP violation, the Vcc VR low side MOSFETs should be driven on to protect the processor and the VR should de-assert VR_READY to shut down the core supply voltage. Power cycling is required to re-start the system.

OVP at start-up should be fully functional with a trip level referenced to the boot VID of 1.1 V.

Operating at lower VID codes during Dynamic VID establishes low (invalid) OVP thresholds which must not be used to initiate a system shut down. For example, there is a time delay from transmission of a VID code to the VR reaction; this time lag may result in a 200 mV delta from the reference VID at a functional voltage that will not damage the processor. Because of these conditions, OVP functionality must be blanked during the Dynamic VID state.

8.2 Over-Current Protection (OCP) (PROPOSED)

The DC-DC should be capable of withstanding a continuous, abnormally low resistance on the output without damage or over-stress to the DC-DC. The OCP trip level should be programmable by the DC-DC designer, typically 130% of rated output current. If an OCP fault is detected, the VR should fold back or shut down, de-assert VR_READY and reset the start up sequence.

Output current under this condition must be limited to avoid component damage and violation of the VRD thermal specifications (see Section 5).

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9 Output Indicators

9.1 VR_READY: Vcc Regulator Is 'ON' (REQUIRED)

VR_READY is an active high output that indicates the start up sequence is complete and the output voltage has moved to the programmed VID value. This signal will be used for start up sequencing for other voltage regulators, the clock, microprocessor reset, etc. It will be tied to processor Vtt_PWRGD input pin. This signal should not be de-asserted by low voltages that occur during D-VID operation. The signal should remain asserted during normal DC-DC operating conditions and only de-assert for fault or shutdown conditions. This signal is not a representation of the accuracy of the DC output to its VID value; it is simply a flag to indicate the VRD is functioning. See Figure 4-2 for timing and Table 24 for signal specifications.

Table 24. VR_Ready output signal Specifications

Signal Type		Open Collector/Drain Logic output from PWM IC, with external pull-up resistor and reference voltage.			
VR_Ready = HIGH		Active / Asserted			
VR_Ready = LOW		Not Active / De-Asserted			
Symbol	**Parameter**	**Min**	**Max**	**Units**	**Remarks**
V_{OH}	Output Voltage High	0.8	1.6	VDC	Vtt rail is expected; Open Coll. /Drain Trans. OFF, Imp. >100 kΩ depending on system implementation
V_{OL}	Output Voltage Low	0	0.3	VDC	With external pull-up resistor; Open Coll./Drain Trans. ON
I_{OL}	Output Low Sink Current	1.0	4.0	mA DC	Current limit set by external pull-up resistor
	Transition Edge Rate	-	150	ns	From 10-90% rise

9.2 Load Indicator Output (EXPECTED)

To assist VRD circuit debug and validation, the PWM controller supplier may choose to include an output voltage that is a defined function of the VRD output current.

9.3 Thermal Monitoring (EXPECTED)

Each customer is responsible for identifying maximum temperature specifications for all components in the voltage regulator design and ensuring that these specifications are not violated while continuously drawing specified VR TDC levels. In the event of a catastrophic thermal failure, the thermal monitoring circuit is to assert the VR_HOT signal to drive the processor PROCHOT# and FORCEPR# inputs immediately prior to exceeding maximum temperature ratings to prevent heat damage. Assertion of these signals will lower processor power consumption and reduce current draw through the voltage regulator, resulting in lower component temperatures. Assertion of PROCHOT# and FORCEPR# degrades system performance and must never occur when drawing less than specified thermal design current.

Both VR_HOT and VR_FAN are active high outputs. See PWM IC vendor's data sheets for signal interface specifications (open drain or push-pull). VR_HOT cannot be tied directly to PROCHOT# and FORCEPR#; the signals must be inverted and buffered. See Table 25 for PROCHOT# and FORCEPR# signal requirements.

To avoid performance degradation resulting from VRD over-temperature conditions, VR11 PWM controllers include a signal called VR_FAN. This signal is activated at 10 degrees Celsius below the VR_HOT trip point, or at 90% of the max VR_HOT trip point. It provides the system designer with options to perform thermal management activities, such as fan speed control, in order to avoid initiating performance degradation.

The PWM controller is located away from the VRD 'hot spot'; therefore, external thermistors are needed to sense temperature. Thermistors are placed in the temperature sensitive region of the voltage regulator. The location must be chosen carefully and is to represent the position where initial thermal violations are expected to occur. When exceeded, the thermal monitor circuit is to initiate PROCHOT# and FORCEPR# to protect the voltage regulator from heat damage.

Figure 9-1 presents a possible load for the PROCHOT# and FORCEPR# signals. These signals may see this full load, or any combination of the two identified loads.

Figure 9-1. PROCHOT# and FORCEPR# Load internal to Processor

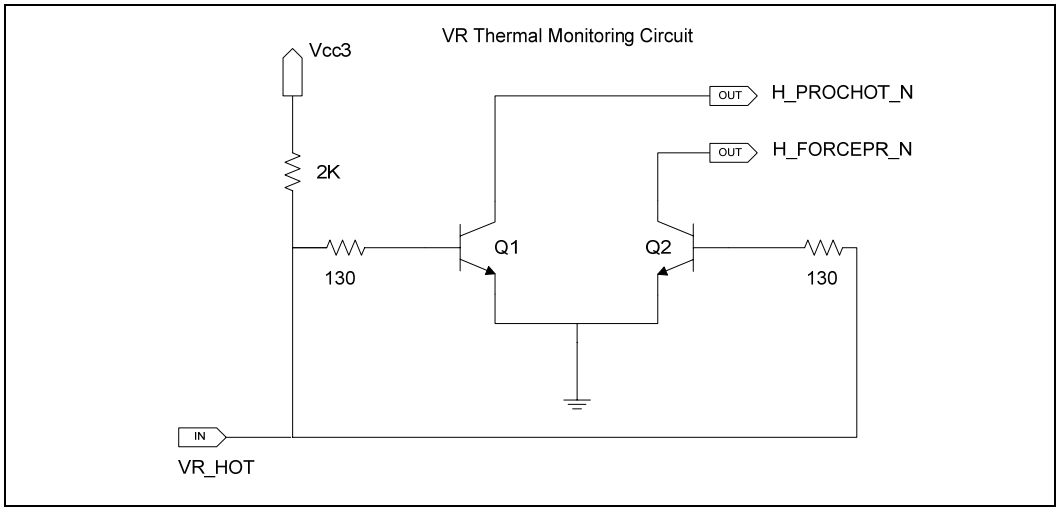

Table 25. Thermal Monitor Specifications

Parameter	Minimum	Typical	Maximum
Vtt	-	Vtt[1]	-
Q1 'on' resistance	-	-	11 Ω
PROCHOT# leakage current	-	-	200 µA
PROCHOT# transition time	1.10 ns	100 ns	-
FORCEPR# leakage current	-	-	200 µA
FORCEPR# transition time	1.10 ns	100 ns	-
PROCHOT# VOL (Maximum low voltage threshold)	-	-	0.4 V
FORCEPR# VOL (Maximum low voltage threshold)	-	-	0.4 V
Minimum time to toggle in and out of D-VID	0.5 ms	-	-

NOTE:
1. Consult Table 16 for Vtt specifications.

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10 MB Power Plane Layout (REQUIRED)

The motherboard layer stack-up must be designed to ensure robust, noise-free power delivery to the processor. Failure to minimize and balance power plane resistance may result in non-compliance to the die load line specification. A poorly planned stack-up or excessive holes in the power planes may increase system inductance and generate oscillation on the Vcc voltage rail at the processor. Both of these types of design errors can lead to processor failure and must be avoided by careful Vcc and Vss plane layout and stack-up. The types of noise introduced by these errors may not be immediately observed on the processor power lands or during system-board voltage transient validation, so issues must be resolved by design, prior to layout, to avoid unexpected failures.

Following basic layout rules can help avoid excessive power plane noise. All motherboard layers in the area surrounding the processor socket should be used for Vcc power delivery; copper shapes that encompass the power delivery region of the processor land field are required. A careful motherboard design will help ensure a well-functioning system that minimizes the noise profile at the processor die. The following subsections provide further guidance.

10.1 Minimize Power Path DC Resistance

Power path resistance can be minimized by ensuring that the copper layout area is balanced between Vcc and Vss planes. A good four layer board design will have two Vcc layers and two Vss layers. Because there is generally more Vss copper in the motherboard stack-up, care should be taken to maximize the copper in Vcc floods. This includes care to minimize unnecessary plane splits and holes when locating through hole components, vias, and connection pads. Refer to Table 26 for more details on the reference board layer stackup.

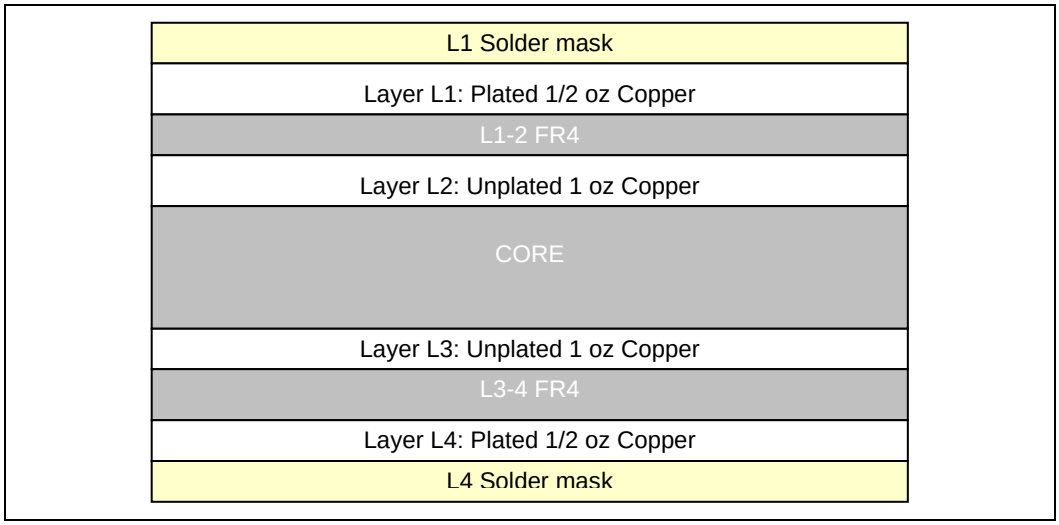
10.2 Minimize Power Delivery Inductance

At higher frequencies the ordering of the motherboard layers becomes critical as it is Vcc/Vss **plane pairs** which carry current and determine power plane inductance. The layer stack-up should maximize adjacent (layer-to-layer) planes at a minimized spacing to achieve the smallest possible inductance. Care must be taken to minimize unnecessary plane splits and holes when locating through-hole components, vias, and connection pads. Minimized inductance will ensure that the board does not develop low frequency noise which may cause the processor to fail (load line violation).

10.3 Four-Layer Boards

A well-designed 4-layer board will feature generous Vcc shapes on the outer layers and large Vss shapes on the inner layers. The Vss-reference requirements for the front side bus are best accommodated with this layer ordering. The power plane area should be maximized and cut-out areas should be carefully placed to minimize parasitic resistance and inductance. Examples power plane layout of Intel's reference board are provided in Table 26 and Figure 10-1 through Figure 10-5.

Figure 10-1. Reference Board Layer Stack-up



NOTE: Drawing is not to scale

Table 26. Reference Board Layer Thickness (Prepreg 1080)

Layer	Minimum	Typical	Maximum
L1 Solder mask	0.2 mils	0.7 mils	1.2 mils
L1	1.1 mils	1.9 mils	2.7 mils
L1-2 FR4	2.0 mils	2.7 mils	3.5 mils
L2	1.0 mils	1.2 mils	1.4 mils
Core	45 mils	50 mils	55 mils
L3	1.0 mils	1.2 mils	1.4 mils
L3-4 FR4	2.0 mils	2.7 mils	3.5 mils
L4	1.1 mils	1.9 mils	2.7 mils
L4 Solder mask	0.2 mils	0.7 mils	1.2mils

NOTES:

1. Consult Figure 10-1 for layer definition
2. Impedance Target: 50 Ω +/- 15%; based on nominal 4 mil trace
3. Overall board thickness is 62 mils +8, -5 mils

Figure 10-2. Layer 1 Vcc Shape for Intel's Reference Four Layer Motherboard

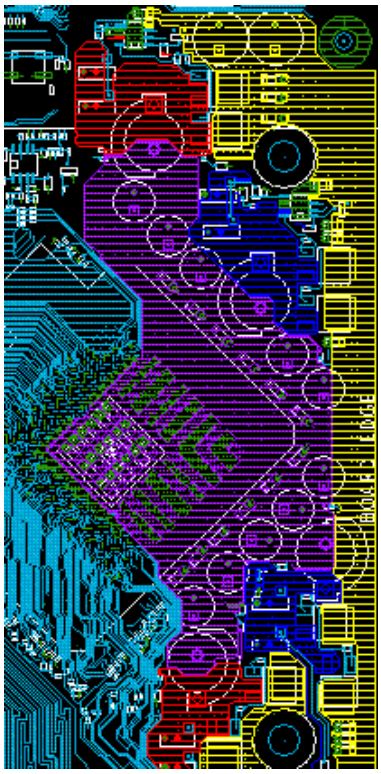


Figure 10-3. Layer 2 Vss Routing for Intel's Reference Four Layer Motherboard

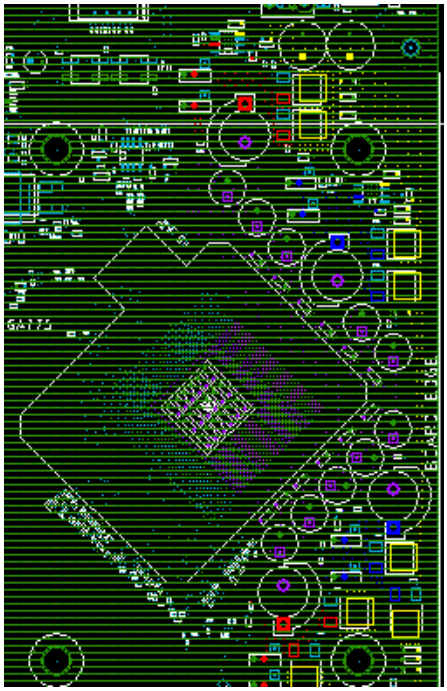


Figure 10-4. Layer 3 Vss Routing for Intel's Reference Four Layer Motherboard

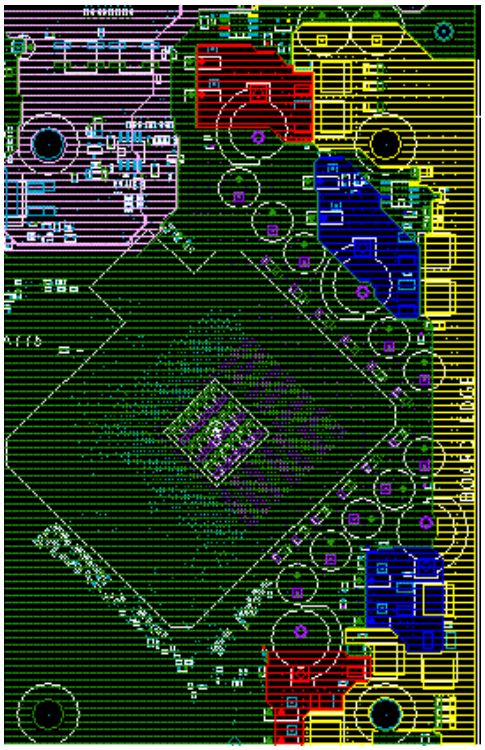
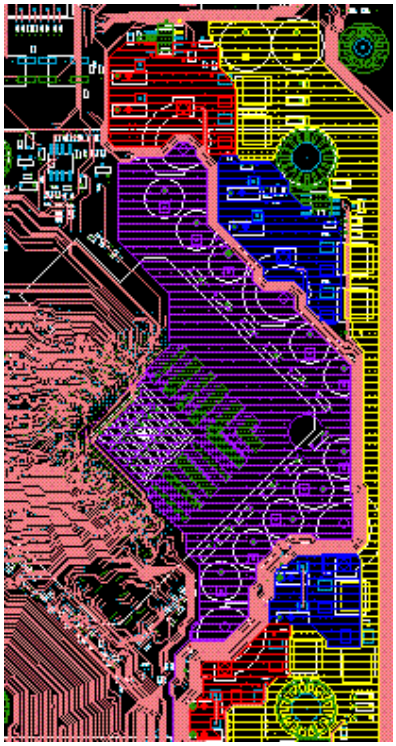


Figure 10-5. Layer 4 Vcc Shape for Intel's Reference Four Layer Motherboard



10.4 Six-Layer Boards

Six layer boards provide layout engineers with greater design flexibility compared to the four layer standard. Adjacent plane pairs of the same potential are not useful at higher frequencies, so the best approach is to maximize adjacent, closely spaced Vcc/Vss plane pairs. The plane pair separated by the PCB core material is of lesser importance since it is generally an order of magnitude larger in spacing than other plane pairs in the stack-up. Because the Vss planes are typically full floods of copper, an example of a well-designed 6-layer stack-up will have 4 Vcc layers and 2 layers for Vss. The DC resistive requirements (Section 10.1) of the power delivery loop can still be met because the Vss floods are larger than the Vcc floods, and the higher frequency needs are considered as there are 4 Vcc/Vss plane pairs to deliver current and reduce inductance.

10.5 Resonance Suppression

Vcc power delivery designs can be susceptible to resonance phenomena capable of creating droop amplitudes in violation of load line specifications. This is due to the interleaved levels of inductively-separated decoupling capacitance. Furthermore, these resonances may not be detected through standard validation and require engineering analysis to identify and resolve. If not identified and corrected in the design process, these resonant phenomena may yield droop amplitudes in violation of load line specifications by superimposing with standard VRD droop behavior. Frequency-dependent power delivery network impedance simulations and validation are strongly recommended to identify and resolve power delivery resonances before board are actually built. Careful modeling and validation can help to avoid voltage violations responsible for data corruption, system lock-up, or system ‘blue-screening’.

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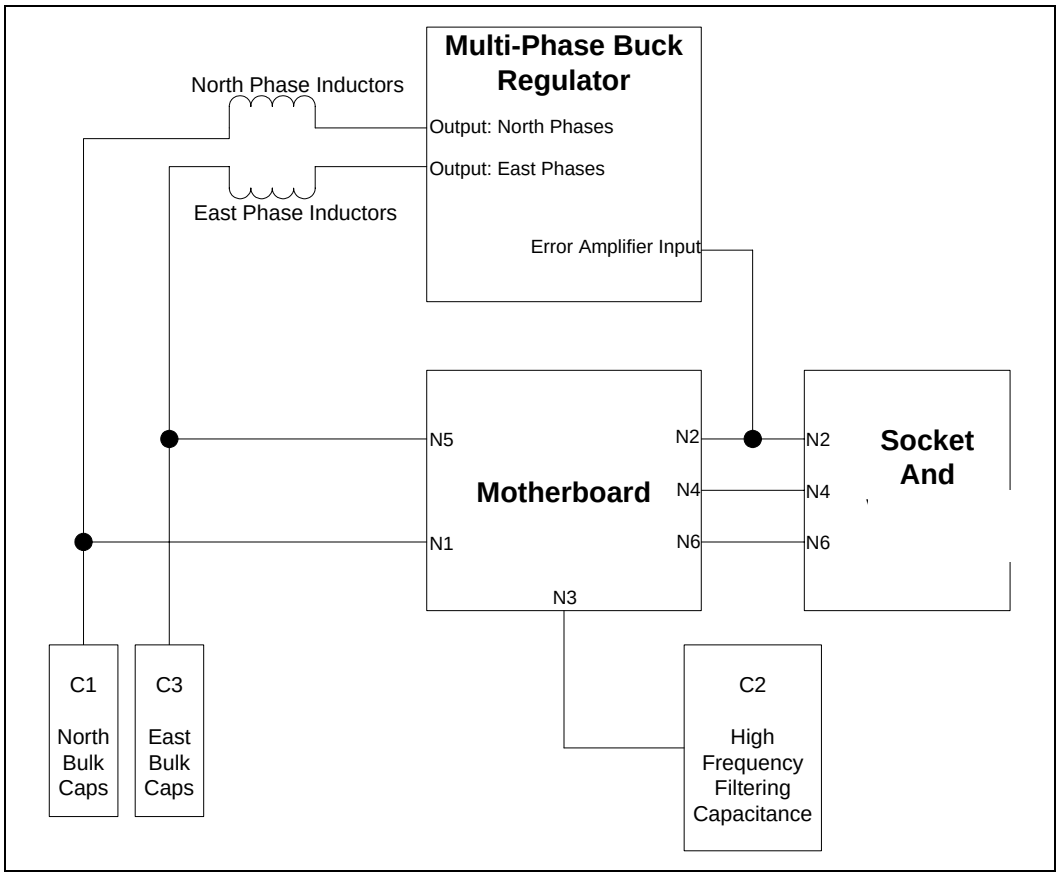
11 Electrical Simulation (EXPECTED)

The following electrical models are enclosed to assist with VRD design analysis and component evaluation for load line compliance. The block diagram shown in Figure 11-1 is a simplified representation of the Vcc power delivery network of the Intel four-layer reference board). The board model, detailed in Figure 11-4, characterizes the power plane layout of Figure 10-2 to
Figure 10-5. The multiphase buck regulator and capacitor models should be obtained from each selected vendor. When fully integrated into electrical simulation software, this model can be used to evaluate PWM controller, capacitor, and inductor performance against the load line and tolerance band requirements detailed in section 2.2. To obtain accurate results, it is strongly recommended to create and use a custom model that represents the specific board design, PWM controller, and passive components that are under evaluation.

Figure 11-1. Simplified Reference Block Diagram



NOTE: Consult Figure 10-2 to Figure 10-5 for reference layout.

The motherboard model of Figure 11-4 represents the power delivery path of Intel's reference four-layer motherboard design. Input and output node locations are identified in Figure 11-5. Feedback to the PWM controller error amplifier should be tied to node 'N2', the socket-motherboard interface. Node 'N1' is the location where the 'north' phase inductors of the buck regulator ties to the 'north' motherboard power plane. If the design incorporates more than one 'north' phase, the inductors of each should be tied to this node. 'North' bulk capacitors, C1, are also connected to node 'N1'. C1 represents the parallel combination of all capacitors and capacitor parasitics at this location. Node 'N5' is the location where the output inductors of the 'east' side phases tie to the 'east' motherboard power plane. If the design incorporates more than one 'east' phase, the inductors of each should be tied to this node. 'East' bulk capacitors, C3, are also connected to 'N5'. C3 represents the parallel combination of all capacitors and capacitor parasitics at this location. Node 'N3' represents the socket cavity and is connected to the mid-frequency filter, C2. C2 represents the parallel combination of all capacitors and capacitor parasitics at this location.

Typical capacitor models are identified in Figure 11-6. Each model represents the parallel combination of the local capacitor placement as identified in the previous paragraph. Recommended parallel values of each parameter are identified in Table 28. Consult section 1.1 for further details regarding bulk and mid-frequency capacitor selection.

The LGA775 socket is characterized by three impedance paths that connect to the motherboard at 'N2' ('north' connection), 'N4' ('south' cavity connection), and 'N6' ('east' connection). I_PWL is a piece-wise linear current step that is used to stimulate the voltage droop as seen at the motherboard-socket interface and is defined in Figure 11-8 and Table 30. This load step approximates the low frequency current spectrum that is necessary to evaluate bulk capacitor, mid-frequency capacitor and PWM controller performance. It does not provide high frequency content to excite package noise. The cavity capacitor solution, C2, is used as a reference for designing processor packaging material and should not be modified except to reduce ESR/ESL or increase total capacitance. Failure to observe this recommendation may make the motherboard incompatible with some processor designs.

The primary purpose of the simulation model is to identify options in supporting the socket load line specification. Evaluation of the full power-path model will allow the designer to perform what-if analysis to determine the cost optimal capacitor and PWM controller configuration. This is especially useful in determining the capacitor configuration that can support load line specifications across variation such as manufacturing tolerance, age degradation, and thermal drift. The designer is encouraged to evaluate different capacitor configurations and PWM controller designs. However, the designer should be aware that the feedback compensation network of most PWM controllers requires modification when the capacitor solution changes. Consult the PWM controller datasheet for further information.

Figure 11-2. Example Voltage Droop Observed At Node 'N2'

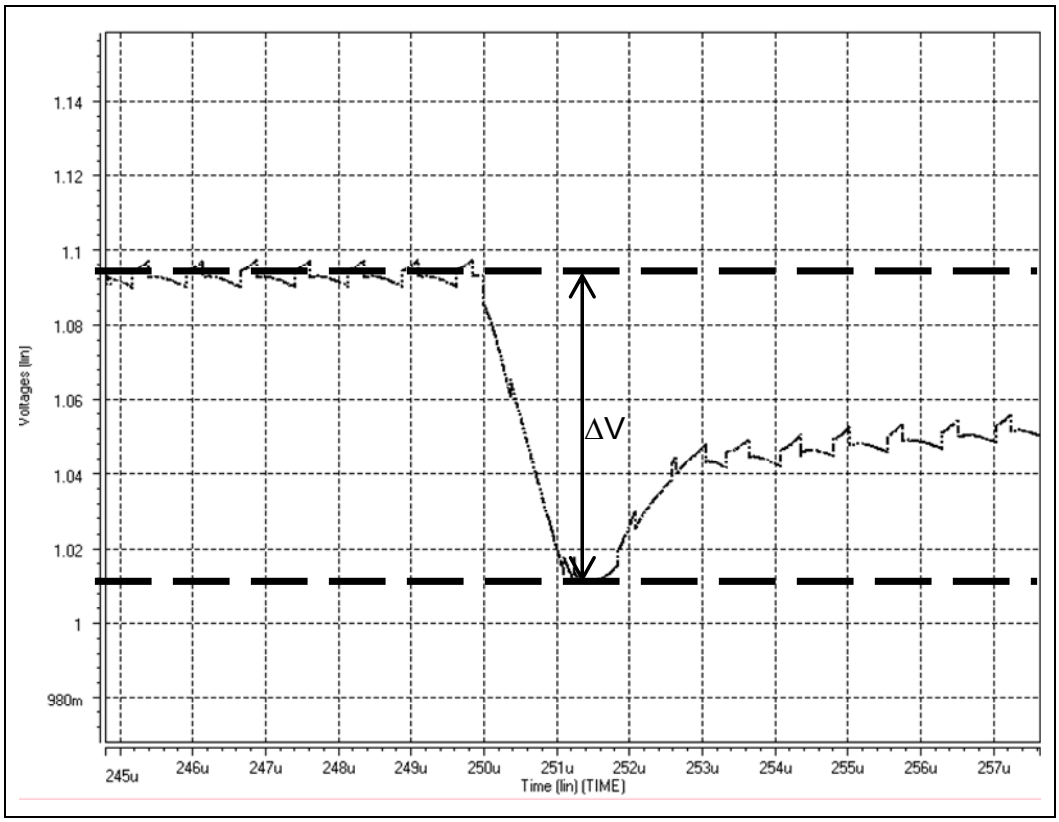
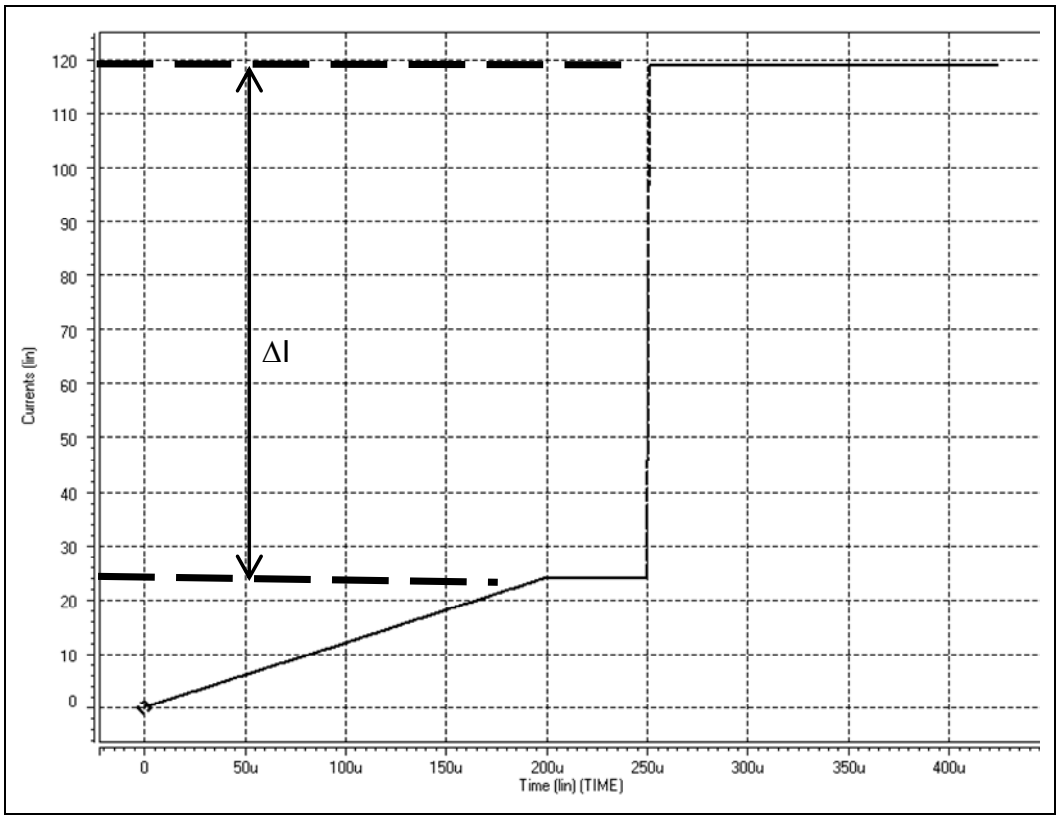


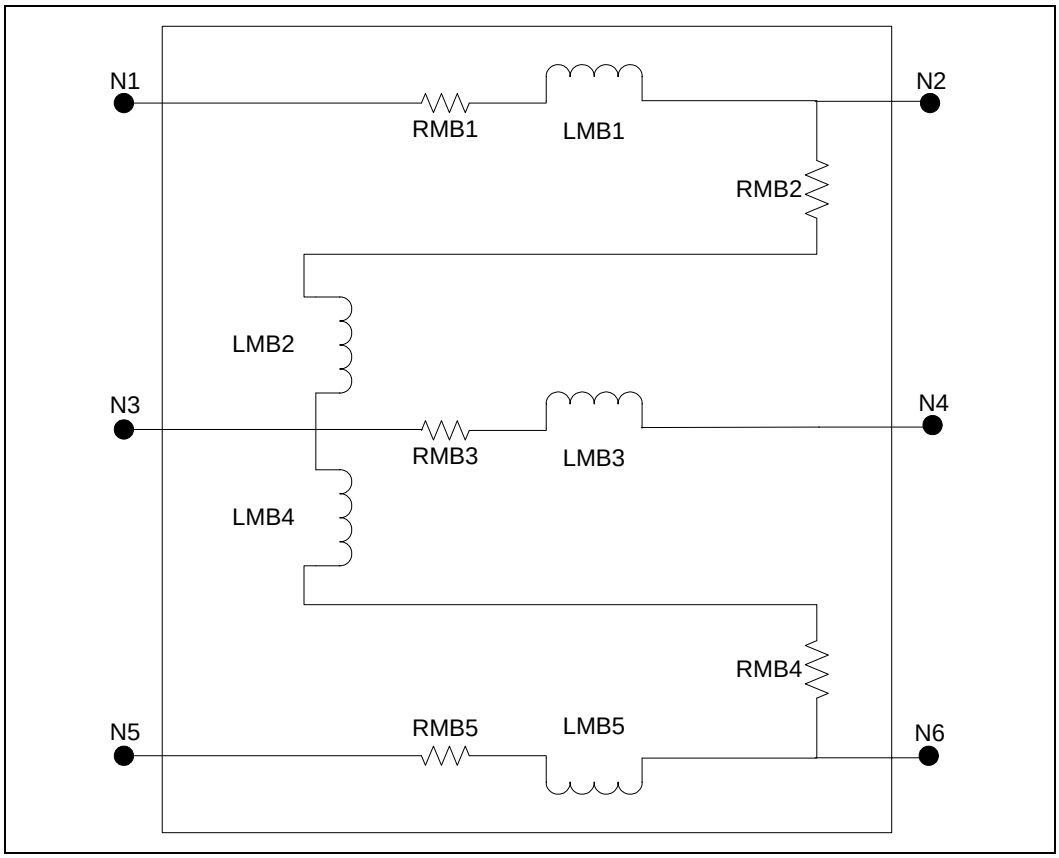
Figure 11-2 provides an example voltage droop waveform at node 'N2', the socket-motherboard interface. The load line value is defined as $\Delta V/\Delta I$ with ΔV measured at this node and the current step observed through I_PWL. The voltage amplitude is defined as the difference in the steady state voltage (prior to the transient) and the minimum voltage droop (consult Figure 11-2). Care must be taken to remove all ripple content in this measurement to avoid a pessimistic load line calculation that will require additional capacitors (cost) to correct. Figure 11-3 provides an example current stimulus. The amplitude is measured as the difference in maximum current and steady state current prior to initiation of the current step. With ΔV and ΔI known, the load line slope is simply calculated using Ohm's Law: $R_{LL} = \Delta V/\Delta I$.

Figure 11-3. Current Step Observed Through I_PWL



NOTE: To avoid excessive ringing in simulation, the system current should be slowly ramped from zero amps to the minimum recommended DC value prior to initiating the current step.

Figure 11-4. Schematic Diagram for the Four Layer Intel Reference Motherboard.



NOTE: Consult Figure 10-2 to Figure 10-5 for reference layout.

Table 27. Parameter Values for the Schematic of Figure 11-4

Parameter	Value	Comments
RMB1	0.64 mΩ	'North' power plane parasitic resistance from the buck regulator output inductor to the LGA775 socket connection.
RMB2	0.56 mΩ	Power plane parasitic resistance from 'north' LGA775 motherboard connection to the center of the LGA775 cavity.
RMB3	0.59 mΩ	Power plane parasitic resistance from the center of the LGA775 cavity to the 'south' LGA775 socket connection.
RMB4	0.59 mΩ	Power plane parasitic resistance from the center of the LGA775 cavity to the 'east' LGA775 socket connection.
RMB5	0.58 mΩ	'East' power plane parasitic resistance from the buck regulator output inductor to the LGA775 connection.

Parameter	Value	Comments
LMB1	120 pH	'North' power plane parasitic inductance from the buck regulator output inductor to the LGA775 socket connection
LMB2	166 pH	Power plane parasitic inductance from 'north' LGA775 motherboard connection to the center of the LGA775 cavity.
LMB3	166 pH	Power plane parasitic inductance from the center of the LGA775 cavity to the 'south' LGA775 socket connection.
LMB4	247 pH	Power plane parasitic inductance from 'east' LGA775 motherboard connection to the center of the LGA775 cavity.
LMB5	138 pH	'East' power plane parasitic inductance from the buck regulator output inductor to the LGA775 connection.

Figure 11-5. Node Location for the Schematic of Figure 11-4

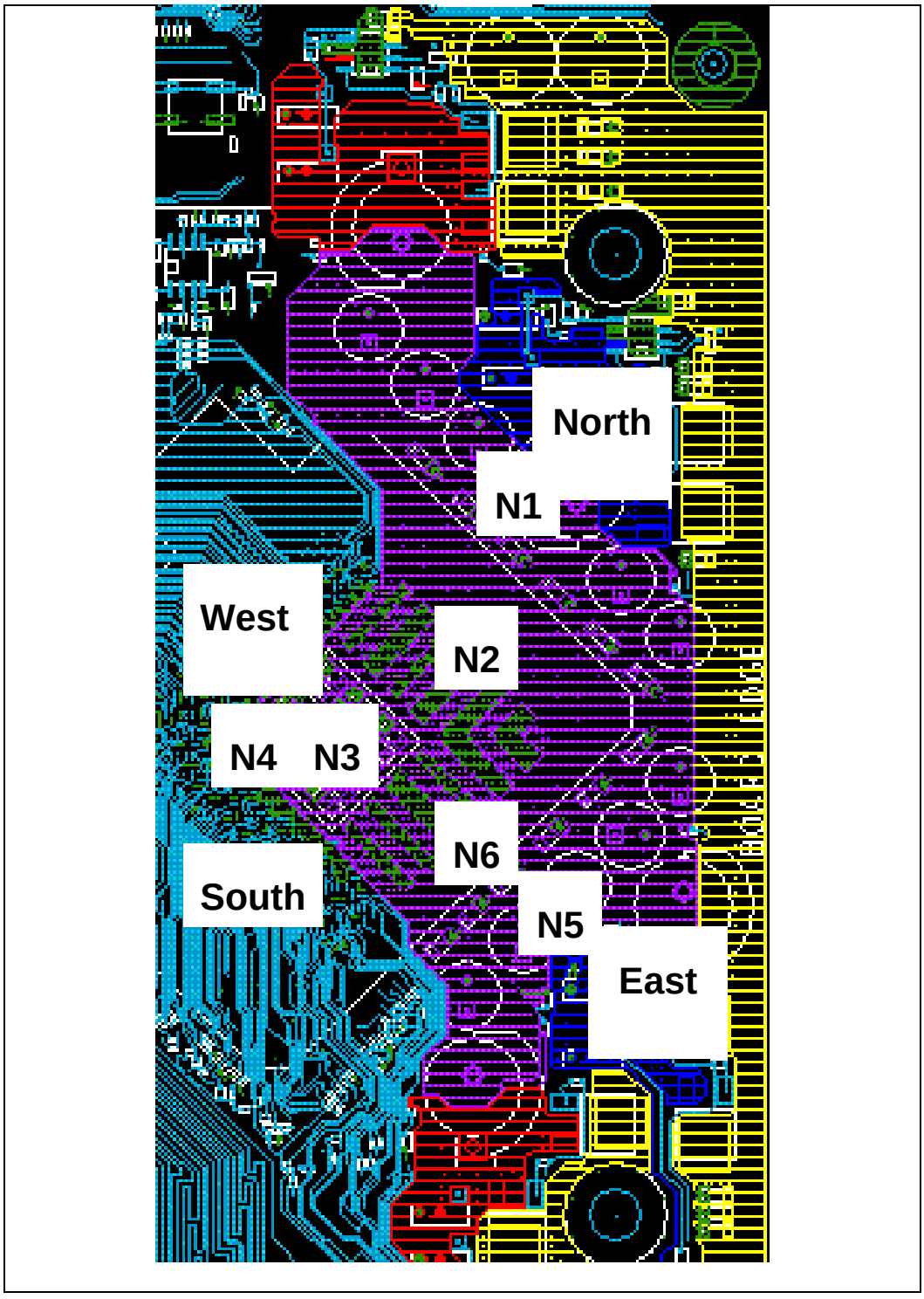
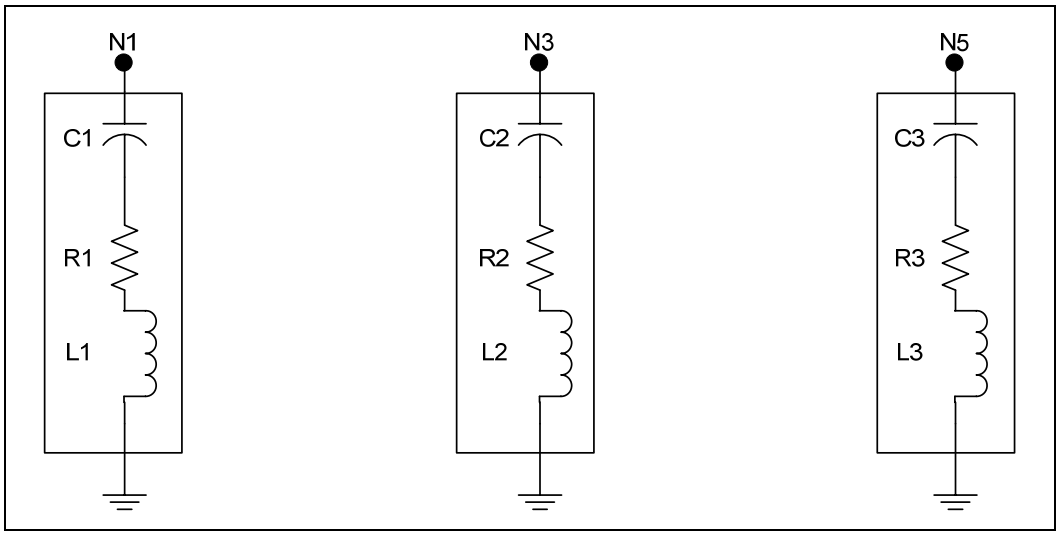


Figure 11-6. Schematic Representation of Decoupling Capacitors



NOTES:
1. C1 represents the parallel model for 'north' location bulk decoupling
2. C2 represents the parallel model for mid-frequency decoupling located in the socket cavity
3. C3 represents the parallel model for 'east' location bulk decoupling

Table 28. Recommended Parameter Values for the Capacitors Models in Figure 11-6

Parameter	Value	Comments
C1	2800 μF[2]	Parallel equivalent for 'north' capacitors prior to age, thermal, and manufacturing degradation.
R1	1.2 mΩ	Parallel equivalent for 'north' capacitor maximum ESR.
L1	600 pH[1, 2]	Parallel equivalent for 'north' capacitor maximum ESL.
C2	328 μF[2]	Parallel equivalent for 'cavity' capacitors prior to age, thermal, and manufacturing degradation.
R2	16.7 μΩ[2]	Parallel equivalent for 'cavity' capacitor maximum ESR.
L2	29 pH[1, 2]	Parallel equivalent for 'cavity' capacitor maximum ESL.
C3	2800 μF[2]	Parallel equivalent for 'east' capacitors prior to DC bias, age, thermal, and manufacturing degradation.
R3	1.2 mΩ[2]	Parallel equivalent for 'east' capacitor maximum ESR.
L3	600 pH[1, 2]	Parallel equivalent for 'east' capacitor maximum ESL.

NOTES:
1. Higher values of ESL may satisfy design requirements.
2. Contact capacitor vendors to identify values for the specific components used in your design

Figure 11-7. Schematic Representation of Decoupling Capacitors

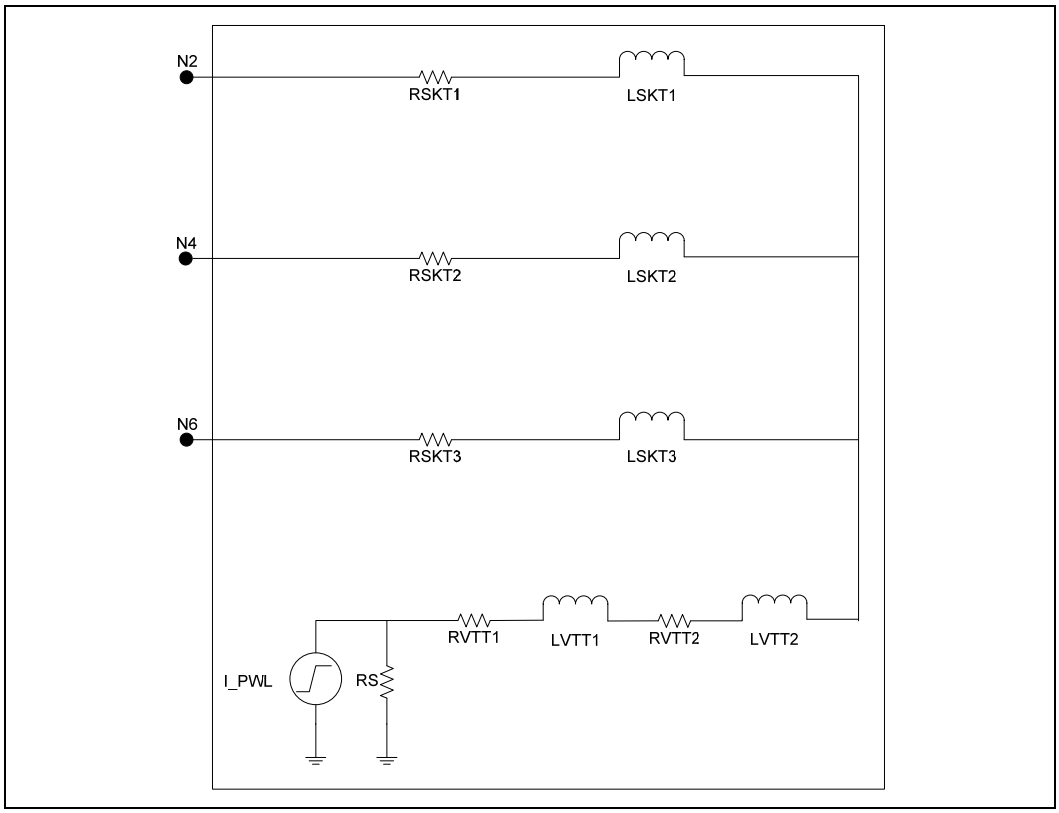


Table 29. Recommended Parameter Values for the Capacitors Models in Figure 11-6

Parameter	Value	Comments
RSKT1	0.38 mΩ	LGA775 ‘north’ segment resistance
RSKT2	1.13 mΩ	LGA775 ‘center’ segment resistance
RSKT3	0.29 mΩ	LGA775 ‘east’ segment resistance
RVTT1	0.42 mΩ	Resistance of VTT Tool load board
RVTT2	0.91 mΩ	Resistance of VTT Tool socket adapter (interposer)
RS	100 kΩ	VTT Tool current source resistance
LSKT1	40 pH	LGA775 ‘north’ segment inductance
LSKT2	120pH	LGA775 ‘center’ segment inductance
LSKT3	30 pH	LGA775 ‘east’ segment inductance
LVTT1	240 pH	Inductance of VTT Tool load board
LVTT2	42 pH	Inductance of VTT Tool socket adapter (interposer)

Figure 11-8. Current Load Step Profile for I_PWL

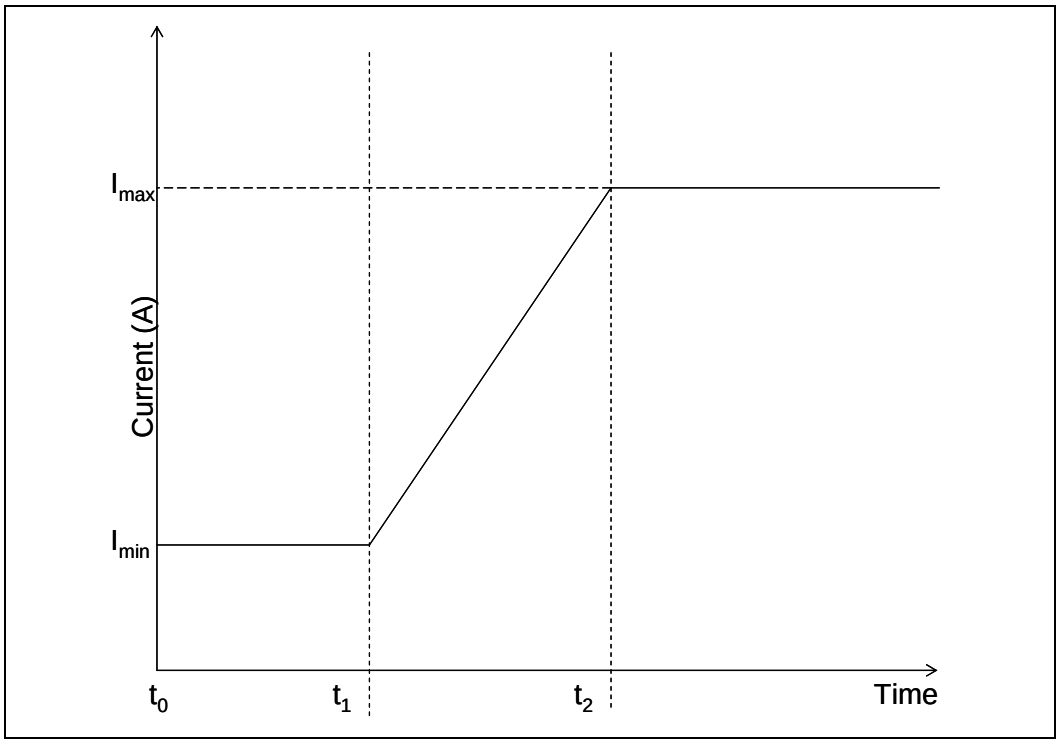


Table 30. I_PWL Current Parameters for Figure 11-8

Parameter	Value	Comments
t_0	0 s	Simulation 'time zero'
t_1	250 µs	Time to initiate the current step. This parameter must be chosen at a time that the Vcc rail is residing at steady state.
t_2	t_1 + 50 µs	Time of maximum current[1]
Istep	95 A	Current step for load line testing[1]
Imin	30 A	Minimum current for simulation analysis[1]
Imax	125 A	Maximum current for simulation analysis[1]

NOTE:
1. See Table 11. Intel Processor Current Step Values for Transient Socket load line Testing

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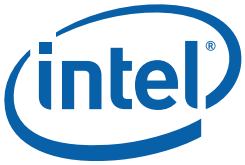

Appendix A LGA775 Loadline Testing Parameters

A.1 Overview

This document provides the parameter for loadline testing used to characterize the performance of the voltage regulator for the mainboard supporting LGA775 processor.

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Document Number: 313214-002

Appendix B LGA775 Voltage Regulator Configuration Parameters

B.1 775_VR_CONFIG_04A

Table 31. 775_VR_CONFIG_04A Specification Input Parameters

Definition	Variable Name	Value
Socket Load Line Slope	SKT_LL	1.40 mΩ
Socket Load Line Tolerance Band	TOB	25 mV
Maximum Overshoot Above VID	OS_AMP	50 mV
Maximum Overshoot Time Duration Above VID	OS_TIME	25 us
Peak To Peak Ripple Amplitude	RIPPLE	10 mV
Thermal Compensation Voltage Drift	THERMAL_DRIFT	4 mV
Iccmax	Iccmax	78 A
Dynamic Current Step	I_STEP	55 A
Maximum DC Test Current	I_DC_MAX	23 A
Minimum DC Test Current	I_DC_MIN	5 A
Voltage Regulator Thermal Design Current	VR_TDC	68 A
Current step rise time	I_RISE	83 A/µs

B.2 775_VR_CONFIG_04B

Table 32. 775_VR_CONFIG_04B Specification Input Parameters

Definition	Variable Name	Value
Socket Load Line Slope	SKT_LL	1.00 mΩ
Socket Load Line Tolerance Band	TOB	19 mV
Maximum Overshoot Above VID	OS_AMP	50 mV
Maximum Overshoot Time Duration Above VID	OS_TIME	25 us
Peak To Peak Ripple Amplitude	RIPPLE	10 mV
Thermal Compensation Voltage Drift	THERMAL_DRIFT	4 mV
Iccmax	Iccmax	119 A
Dynamic Current Step	I_STEP	95 A
Maximum DC Test Current	I_DC_MAX	24 A
Minimum DC Test Current	I_DC_MIN	5 A

Definition	Variable Name	Value
Voltage Regulator Thermal Design Current	VR_TDC	101 A
Current step rise time	I_RISE	83 A/µs

B.3 775_VR_CONFIG_05A

Table 33. 775_VR_CONFIG_05A Specification Input Parameters

Definition	Variable Name	Value
Socket Load Line Slope	SKT_LL	1.0 mΩ
Socket Load Line Tolerance Band	TOB	19 mV
Maximum Overshoot Above VID	OS_AMP	50 mV
Maximum Overshoot Time Duration Above VID	OS_TIME	25 us
Peak To Peak Ripple Amplitude	RIPPLE	10 mV
Thermal Compensation Voltage Drift	THERMAL_DRIFT	4 mV
Iccmax	Iccmax	100 A
Dynamic Current Step	I_STEP	65 A
Maximum DC Test Current	I_DC_MAX	35 A
Minimum DC Test Current	I_DC_MIN	5 A
Voltage Regulator Thermal Design Current	VR_TDC	85 A
Current step rise time	I_RISE	50 ns

B.4 775_VR_CONFIG_05B

Table 34. 775_VR_CONFIG_05B Specification Input Parameters

Definition	Variable Name	Value
Socket Load Line Slope	SKT_LL	1.00 mΩ
Socket Load Line Tolerance Band	TOB	19 mV
Maximum Overshoot Above VID	OS_AMP	50 mV
Maximum Overshoot Time Duration Above VID	OS_TIME	25 us
Peak To Peak Ripple Amplitude	RIPPLE	10 mV
Thermal Compensation Voltage Drift	THERMAL_DRIFT	4 mV
Iccmax	Iccmax	125 A
Dynamic Current Step	I_STEP	95 A
Maximum DC Test Current	I_DC_MAX	30 A
Minimum DC Test Current	I_DC_MIN	5 A
Voltage Regulator Thermal Design Current	VR_TDC	115 A
Current step rise time	I_RISE	50 ns

B.5 775_VR_CONFIG_06

Table 35. 775_VR_CONFIG_06 Specification Input Parameters

Definition	Variable Name	Value
Socket Load Line Slope	SKT_LL	1.00 mΩ
Socket Load Line Tolerance Band	TOB	19 mV
Maximum Overshoot Above VID	OS_AMP	50 mV
Maximum Overshoot Time Duration Above VID	OS_TIME	25 us
Peak To Peak Ripple Amplitude	RIPPLE	10 mV
Thermal Compensation Voltage Drift	THERMAL_DRIFT	4 mV
Iccmax	Iccmax	75 A
Dynamic Current Step	I_STEP	50 A
Maximum DC Test Current	I_DC_MAX	25 A
Minimum DC Test Current	I_DC_MIN	5 A
Voltage Regulator Thermal Design Current	VR_TDC	60 A
Current step rise time	I_RISE	50 ns

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Appendix C Z(f) Impedance References

"Microprocessor Platform Impedance Characterization using VTT tools" by S Chickamenahalli, K. Aygün, M.J. Hill, K. Radhakrishnan, K. Eilert, E. Stanford in the proceedings of the *20th Annual IEEE Applied Power Electronics Conference and Exposition,* Vol. 3. pp. 1466-1469, March 2005.

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