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Mobile Intel® Pentium® 4 Processor-M and Intel® 852PM/GME/GMV Chipset Platform

Design Guide Update

April 2005

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Contents

Revision History

Revision Number	Description	Revision Date
-001	Initial Release	December 2004
-002	Updates Include: o Clarification on USB ESD protection	March 2005

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Preface

This Design Guide Update document is an update to the specifications and information contained in *Intel® 852GME, Intel® 852GMV and Intel® 852PM Chipset Platforms Design Guide*, Document Number 253026. This Design Guide Update may reference other documents listed in the following Affected Documents/Related Documents table. This document is a compilation of updates to the general design considerations; schematic, layout, and routing updates; and documentation changes. This document is intended for hardware system manufacturers and for software developers of applications, operating systems, and tools. The design guide (and this design guide update) is primarily targeted at the PC market segment and was first published in 2003. Those using this design guide and update should check for device availability before designing in any of the components included in this document.

Information types defined in the Nomenclature section of this document are consolidated into the public design guide update document when the public design guide document is first published. This design guide update document contains a complete list of all known information types. However, only the detail for new material is included in this document. Both the public design guide document and this design guide update document are required to allow the users to have a complete list of information types and the associated details. This design guide update document will contain information that has not been previously published.

Affected Documents

Document Title/Document Number/	Document Location
Intel® 852GME, Intel® 852GMV and Intel® 852PM Chipset Platforms Design Guide, 253026-004	http://www.intel.com/design/mobile/desguide/253026.htm

Related Documents

Document Title	Document Location
Intel® 852GME Chipset GMCH and Intel® 852PM Chipset MCH Datasheet	http://www.intel.com/design/chipsets/datashts/253027.htm
Intel® 82801DB I/O Controller Hub 4 Mobile (ICH4-M) Datasheet	http://www.intel.com/design/mobile/datashts/252337.htm

Nomenclature

General Design Considerations include system level considerations that the system designer should account for when developing hardware or software products using the Intel® 852GM chipset.

Schematic, Layout, and Routing Updates include suggested changes to the current published schematics or layout, including typos, errors, or omissions from the current published documents.

Documentation Changes include suggested changes to the current published design guide not including the above.

Summary Tables of Changes

Codes Used in Summary Table

Doc: Document change or update that will be implemented.

Shaded: This item is either new or modified from the previous version of the document.

NO.	Plans	GENERAL DESIGN CONSIDERATIONS
		There are no General Design Considerations in this Design Guide Update revision

NO.	Plans	SCHEMATIC, LAYOUT, AND ROUTING UPDATES
1	Doc	Correction on pin-out/connection for Processor power

NO.	Plans	DOCUMENTATION CHANGES
1	Doc	Clarification on USB ESD protection

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General Design Considerations

There are no General Design Considerations in this Design Guide Update revision.
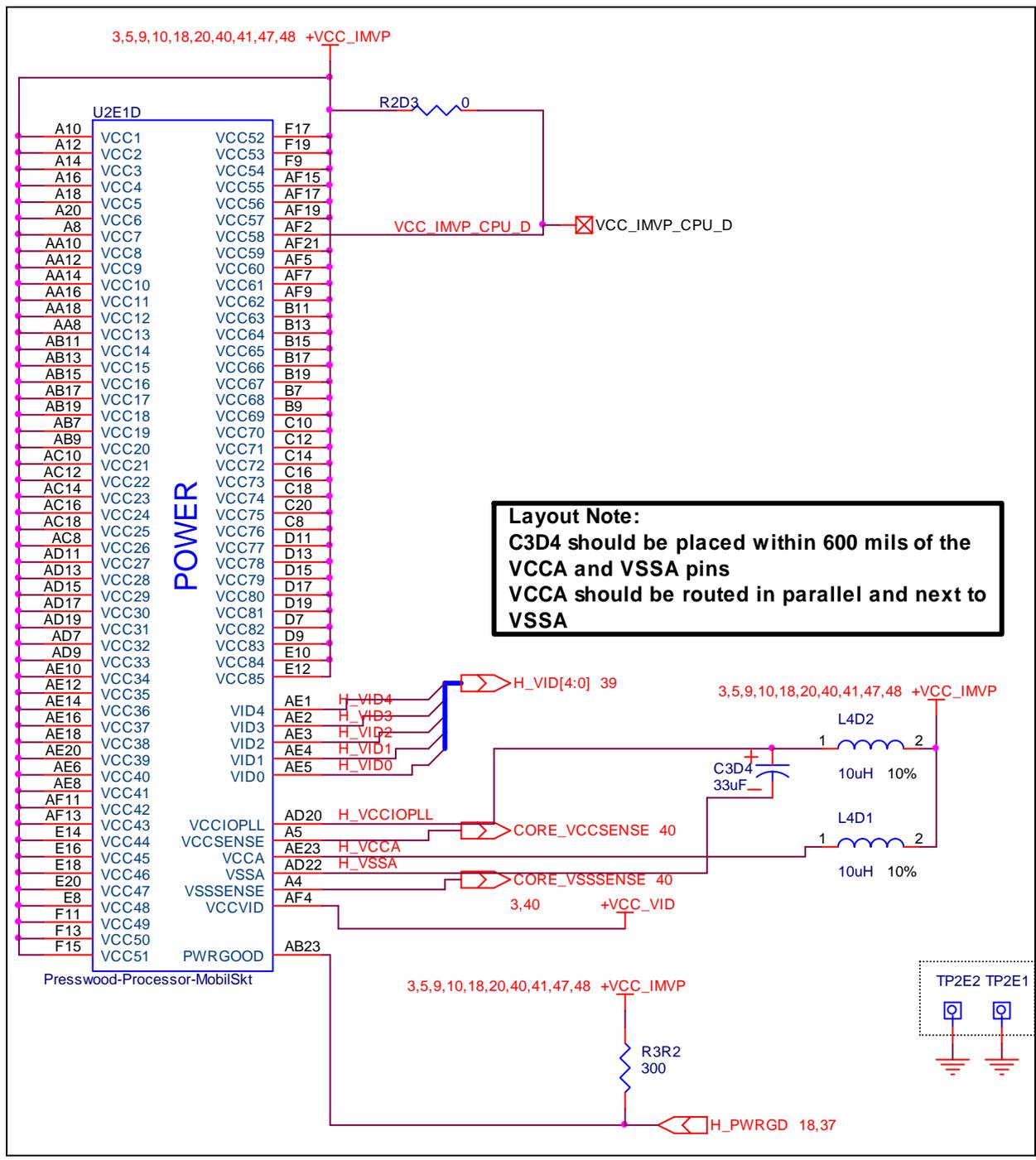
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Schematic, Layout, and Routing Updates

1. **Correction on Pinout/Connection for Processor Power**

Schematics net connections for VCCA and VCCIOPLL for the processor power should be corrected as follows (schematics sheet 4).

3,5,9,10,18,20,40,41,47,48 +VCC_IMVP

U2E1D

R2D3   0

Pin	Name		Name	Pin
A10	VCC1		VCC52	F17
A12	VCC2		VCC53	F19
A14	VCC3		VCC54	F9
A16	VCC4		VCC55	AF15
A18	VCC5		VCC56	AF17
A20	VCC6		VCC57	AF19
A8	VCC7		VCC58	AF2
AA10	VCC8		VCC59	AF21
AA12	VCC9		VCC60	AF5
AA14	VCC10		VCC61	AF7
AA16	VCC11		VCC62	AF9
AA18	VCC12		VCC63	B11
AA8	VCC13		VCC64	B13
AB11	VCC14		VCC65	B15
AB13	VCC15		VCC66	B17
AB15	VCC16		VCC67	B19
AB17	VCC17		VCC68	B7
AB19	VCC18		VCC69	B9
AB7	VCC19		VCC70	C10
AB9	VCC20		VCC71	C12
AC10	VCC21		VCC72	C14
AC12	VCC22		VCC73	C16
AC14	VCC23		VCC74	C18
AC16	VCC24		VCC75	C20
AC18	VCC25		VCC76	C8
AC8	VCC26		VCC77	D11
AD11	VCC27		VCC78	D13
AD13	VCC28		VCC79	D15
AD15	VCC29		VCC80	D17
AD17	VCC30		VCC81	D19
AD19	VCC31		VCC82	D7
AD7	VCC32		VCC83	D9
AD9	VCC33		VCC84	E10
AE10	VCC34		VCC85	E12
AE12	VCC35			
AE14	VCC36		VID4	AE1
AE16	VCC37		VID3	AE2
AE18	VCC38		VID2	AE3
AE20	VCC39		VID1	AE4
AE6	VCC40		VID0	AE5
AE8	VCC41			
AF11	VCC42			
AF13	VCC43		VCCIOPLL	AD20
E14	VCC44		VCCSENSE	A5
E16	VCC45		VCCA	AE23
E18	VCC46		VSSA	AD22
E20	VCC47		VSSSENSE	A4
E8	VCC48		VCCVID	AF4
F11	VCC49			
F13	VCC50			
F15	VCC51		PWRGOOD	AB23

POWER

Presswood-Processor-MobilSkt

VCC_IMVP_CPU_D   VCC_IMVP_CPU_D

Layout Note:
C3D4 should be placed within 600 mils of the VCCA and VSSA pins
VCCA should be routed in parallel and next to VSSA

H_VID4   H_VID[4:0] 39
H_VID3
H_VID2
H_VID1
H_VID0

H_VCCIOPLL   CORE_VCCSENSE 40
H_VCCA
H_VSSA   CORE_VSSSENSE 40

3,40   +VCC_VID

3,5,9,10,18,20,40,41,47,48 +VCC_IMVP

L4D2
1   2
10uH 10%

C3D4
33uF

L4D1
1   2
10uH 10%

TP2E2 TP2E1

3,5,9,10,18,20,40,41,47,48 +VCC_IMVP

R3R2
300

H_PWRGD 18,37

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Documentation Changes

1.	Clarification on USB ESD Protection

Added reference to USB ESD Application Note.

Classic USB (1.0/1.1) provided ESD suppression using in line ferrites and capacitors that formed a low pass filter. This technique doesn't work for USB 2.0 due to the much higher signal rate of high-speed data. ESD protection is needed for USB lines. Refer to the *Intel® ICH Family USB ESD Considerations Application Note* for ESD protection implementation guidelines. A device that has been tested successfully is based on spark gap technology. Proper placement of any ESD protection device is on the data lines between the common-mode choke and the USB connector data pins as shown in Figure 108. Other types of low-capacitance ESD protection devices may work as well but were not investigated. As with the common mode choke solution, Intel recommends including footprints for some type of ESD protection device as a stuffing option in case it is needed to pass ESD testing.

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