Intel® E7500 Chipset

Design Guide

E7500 Memory Controller Hub (MCH) Thermal and Mechanical Design Guidelines

February 2002
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## Revision History

<table>
<thead>
<tr>
<th>Revision Number</th>
<th>Description</th>
<th>Date</th>
</tr>
</thead>
<tbody>
<tr>
<td>-001</td>
<td>Initial Release.</td>
<td>February 2002</td>
</tr>
</tbody>
</table>
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1 Introduction

As the complexity of computer systems increases, so do the power dissipation requirements. Care must be taken to ensure that the additional power is properly dissipated. Heat can be dissipated using improved system cooling, selective use of ducting, and/or passive heatsinks.

The objective of thermal management is to ensure that the temperatures of all components in a system are maintained within functional limits. The functional temperature limit is the range within which the electrical circuits can be expected to meet specified performance requirements. Operation outside the functional limit can degrade system performance, cause logic errors, or cause component and/or system damage. Temperatures exceeding the maximum operating limits may result in irreversible changes in the operating characteristics of the component.

The simplest and most cost effective method is to improve the inherent system cooling characteristics through careful design and placement of fans, vents, and ducts. When additional cooling is required, component thermal solutions may be implemented in conjunction with system thermal solutions. The size of the fan or heatsink can be varied to balance size and space constraints with acoustic noise.

The goal of this document is to provide an understanding of the operating limits of the Intel® E7500 chipset MCH and describe a reference thermal solution. Properly designed solutions provide adequate cooling to maintain the MCH die temperatures within thermal specifications. This is accomplished by providing a low local-ambient temperature, ensuring adequate local airflow, and minimizing the die to local-ambient thermal resistance. By maintaining the MCH die temperature within the range recommended in this document, the system designer can ensure the proper functionality, performance, and reliability of the chipset.

This document addresses thermal design and specifications for the MCH component only. For thermal design information on other chipset components, refer to the respective component datasheet. For the P64H2, refer to the Intel® PCI/PCI-X 64-bit Hub 2 (P64H2) Thermal and Mechanical Design Guidelines.
1.1 Design Flow

To develop a reliable, cost-effective thermal solution, several tools have been provided to the system designer. Figure 1 illustrates the design process implicit to this document and the tools appropriate for each step.

Figure 1. Thermal Design Process
1.2 Definition of Terms

<table>
<thead>
<tr>
<th>Term</th>
<th>Definition</th>
</tr>
</thead>
<tbody>
<tr>
<td>BGA</td>
<td>Ball Grid Array. A package type defined by a resin-fiber substrate, onto which a die is mounted, bonded and encapsulated in molding compound. The primary electrical interface is an array of solder balls attached to the substrate opposite the die and molding compound.</td>
</tr>
<tr>
<td>ICH3-S</td>
<td>I/O Controller Hub. The chipset component that contains the primary PCI interface, LPC interface, USB, ATA-33, and other legacy functions.</td>
</tr>
<tr>
<td>MBGA</td>
<td>Mini Ball Grid Array. A version of the BGA with a smaller ball pitch.</td>
</tr>
<tr>
<td>MCH</td>
<td>Memory Controller Hub. The chipset component that contains the processor interface and the memory interface.</td>
</tr>
<tr>
<td>FC-BGA</td>
<td>Flip Chip Ball Grid Array. A packaging technology used for the MCH.</td>
</tr>
<tr>
<td>P64H2</td>
<td>Bus Controller Hub. The chipset component that interfaces the PCI-X buses.</td>
</tr>
<tr>
<td>$T_{\text{case-nhs}}$</td>
<td>The maximum package case temperature without any package thermal solution. This temperature is measured at the geometric center of the top of the package case.</td>
</tr>
<tr>
<td>$T_{\text{die-nhs}}$</td>
<td>The maximum die temperature without any package thermal solution. This temperature is measured at the geometric center of the top of the package die.</td>
</tr>
<tr>
<td>$T_{\text{die-hs}}$</td>
<td>The maximum die temperature with the reference thermal solution attached. This temperature is measured at the geometric center of the top of the package die.</td>
</tr>
<tr>
<td>TDP</td>
<td>Thermal Design Power. Thermal solutions should be designed to dissipate this target power level.</td>
</tr>
</tbody>
</table>
## 1.3 Reference Documents

<table>
<thead>
<tr>
<th>Document</th>
<th>Document Number</th>
</tr>
</thead>
<tbody>
<tr>
<td>Intel® Xeon™ Processor Thermal Design Guidelines</td>
<td>298348</td>
</tr>
<tr>
<td><a href="http://www.intel.com/design/Xeon/guides/298348.htm">http://www.intel.com/design/Xeon/guides/298348.htm</a></td>
<td></td>
</tr>
<tr>
<td>Intel® PCI/PCI-X 64-bit Hub 2 (P64H2) Thermal and Mechanical Design Guidelines</td>
<td>298648</td>
</tr>
<tr>
<td>Intel® Xeon™ Processor with 512 KB L2 Cache and Intel® E7500 Chipset Platform Design Guide</td>
<td>298649</td>
</tr>
<tr>
<td>Intel® E7500 Chipset Datasheet: E7500 Memory Controller Hub (MCH)</td>
<td>290730</td>
</tr>
<tr>
<td>Intel® 82801CA I/O Controller Hub 3 (ICH3-S) Datasheet</td>
<td>290733</td>
</tr>
<tr>
<td>Intel® 82870P2 PCI/PCI-X 64-bit Hub 2 (P64H2) Datasheet</td>
<td>290732</td>
</tr>
<tr>
<td>BGA/OLGA Assembly Development Guide</td>
<td>Note 1</td>
</tr>
<tr>
<td>Thermal Design Suggestions for various form factors</td>
<td></td>
</tr>
<tr>
<td><a href="http://www.formfactors.org">http://www.formfactors.org</a></td>
<td></td>
</tr>
</tbody>
</table>

**NOTES:**

1. Contact your Intel Field Sales representative.
2 Packaging Technology

The E7500 chipset consists of three individual components: E7500 MCH, 82870P2 P64H2, and 82801CA ICH3-S. The E7500 MCH utilizes a 42.5 mm, 6-layer FC-BGA package shown in Figure 3 and Figure 2. For information on the P64H2 package, refer to the Intel® 82870P2 PCI/PCI-X 64-bit Hub 2 (P64H2) Thermal and Mechanical Design Guidelines and the Intel® 82870P2 PCI/PCI-X 64-bit Hub 2 (P64H2) Datasheet. For information on the ICH3-S package, refer to the Intel® 82801CA I/O Controller Hub 3 (ICH3-S) Datasheet.

Figure 2. Intel® E7500 MCH Package Dimensions (Side View)

NOTES:

1. All dimensions are in millimeters.
2. Substrate thickness and package overall height are thicker than standard 492-L PBGA.
3. Primary datum –C– and seating plane are defined by the spherical crowns of the solder balls.
4. All dimensions and tolerances conform to ANSI Y14.5M–1982.
Figure 3. Intel® E7500 MCH Package Dimensions (Top View)

NOTES:
1. All dimensions are in millimeters.
2. All dimensions and tolerances conform to ANSI Y14.5M–1982.
3 Thermal Simulation

Intel provides thermal simulation models of the MCH and associated user’s guides to aid system designers in simulating, analyzing, and optimizing their thermal solutions in an integrated system-level environment. The models are for use with the commercially available Computational Fluid Dynamics (CFD)-based thermal analysis tool “FLOTHERM®” (version 3.1 or higher) by Flomerics® Inc. Contact your Intel Field Sales representative to order the thermal models and user’s guides.
4 Thermal Specifications

4.1 Power

See Table 1 for TDP specifications for the E7500 MCH. FC-BGA packages have poor heat transfer capability into the board and have minimal thermal capability without thermal solutions. Intel recommends that system designers plan for one or more heatsinks when using the E7500 chipset.

4.2 Die Temperature

To ensure proper operation and reliability of the MCH, the die temperatures must be at or below the values specified for the MCH in Table 1. System or component level thermal solutions are required to maintain die temperatures below the maximum temperature specifications. Refer to Chapter 5 for guidelines on accurately measuring package die temperatures.

Table 1. Intel® E7500 MCH Thermal Specifications

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Maximum</th>
</tr>
</thead>
<tbody>
<tr>
<td>$T_{\text{die-hs}}$</td>
<td>102 °C</td>
</tr>
<tr>
<td>TDP</td>
<td>9.0 W</td>
</tr>
</tbody>
</table>

NOTE: $T_{\text{die-hs}}$ is defined as the maximum die temperature with the reference thermal solution attached.
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5 Thermal Metrology

The system designer must make temperature measurements to accurately determine the thermal performance of the system. Intel has established guidelines for proper techniques of measuring the MCH die temperature. Section 5.1 provides guidelines on how to accurately measure the MCH die temperatures. Section 5.2 contains information on running an application program that will emulate anticipated maximum thermal design power. The flowchart in Figure 7 offers useful guidelines for thermal performance and evaluation.

5.1 Die Temperature Measurements

To ensure functionality and reliability, the MCH is specified for proper operation when $T_{\text{die}}$ is maintained at or below their respective maximum temperatures listed in Table 1. The surface temperature at the geometric center of the die corresponds to $T_{\text{die}}$. Measuring $T_{\text{die}}$ requires special care to ensure an accurate temperature measurement.

Temperature differences between the temperature of a surface and the surrounding local ambient air can introduce error in the measurements. The measurement errors could be due to a poor thermal contact between the thermocouple junction and the surface of the package, heat loss by radiation and/or convection, conduction through thermocouple leads, or contact between the thermocouple cement and the heatsink base (if a heatsink is used). To minimize these measurement errors, the following approaches are recommended for thermocouple attach.

5.1.1 90° Angle Attach Methodology

1. Use 36 gauge or smaller diameter K-type thermocouples.
2. Ensure that the thermocouple has been properly calibrated.
3. Attach the thermocouple bead or junction to the top surface of the die in the center using high thermal conductivity cement. It is critical that the thermocouple bead makes contact with the die.
4. The thermocouple should be attached at a 90° angle if no interference exists between the thermocouple wire and retention mechanism (see Figure 4). This is the preferred method and is recommended for use with both bare packages as well as packages employing a thermal solution.
5. The hole size through the heatsink base to route the thermocouple wires out should be no larger than 3.3 mm (0.13 in.) in diameter.
6. Make sure no contact exists between the thermocouple cement and heatsink base. This contact will affect the thermocouple reading.
5.1.2 0° Angle Attach Methodology

1. Mill a 3.3 mm (0.13 in.) diameter hole centered on bottom of the heatsink base. The milled hole should be approximately 1.5 mm (0.06 in.) deep.

2. Mill a 1.3 mm (0.05 in.) wide slot, 0.5 mm (0.02 in.) deep, from the centered hole to one edge of the heatsink. The slot should be in the direction parallel to the heatsink fins (see Figure 6).

3. Attach thermal interface material (TIM) to the bottom of the heatsink base.

4. Cut out portions of the TIM to make room for the thermocouple wire and bead. The cutouts should match the slot and hole milled into the heatsink base.

5. Attach a 36 gauge or smaller calibrated K-type thermocouple bead or junction to the center of the top surface of the die using high thermal conductivity cement. During this step, make sure no contact is present between the thermocouple cement and the heatsink base because any contact will affect the thermocouple reading. It is critical that the thermocouple bead makes contact with the die (see Figure 5).

6. Attach heatsink assembly to the MCH, and route thermocouple wires out through the milled slot.
Figure 5. 0° Angle Attach Methodology (Top View)

![Diagram showing 0° Angle Attach Methodology](angle_attach_1)

**NOTE:** Not to scale.

Figure 6. 0° Angle Attach Heatsink Modifications

![Diagram showing 0° Angle Attach Heatsink Modifications](Angle_Attach_Heatsink_Mod)

**NOTE:** Not to scale.
5.2 Power Simulation Software

The power simulation software is a utility designed to dissipate the thermal design power on a MCH when used in conjunction with an Intel® Xeon™ processor with 512-KB L2 cache. The combination of the Intel® Xeon™ processor with 512-KB L2 cache and the higher bandwidth capability of the E7500 chipset enables new levels of system performance. To assess the thermal performance of an MCH thermal solution under “worst-case realistic application” conditions, Intel has developed a software utility that operates the chipset at near worst-case power dissipation.

The utility has been developed solely for testing customer thermal solutions at near the thermal design power. Figure 7 shows a decision flowchart for determining thermal solution needs. Real future applications may exceed the thermal design power limit for transient time periods. For power supply current requirements under these transient conditions, refer to each component’s datasheet for the \( I_{CC} \) (Max Power Supply Current) specification. Contact your Intel Field Sales representative to obtain a copy of this software.

**Figure 7. Thermal Solution Decision Flowchart**
6 Reference Thermal Solutions

Intel has developed a reference thermal solution designed to meet the cooling needs of the MCH at worst-case conditions. This chapter describes the overall requirements for the reference thermal solution, including critical-to-function dimensions, operating environment, and validation criteria. Other chipset components may or may not need thermal solutions, depending on specific system local-ambient operating conditions. For information on the P64H2 thermal solutions, refer to the Intel® 82870P2 PCI/PCI-X 64-bit Hub 2 (P64H2) Thermal and Mechanical Design Guidelines.

6.1 Operating Environment

The reference thermal solution was designed assuming a maximum local-ambient temperature of 50°C. The minimum recommended airflow velocity at the heatsink is 200 lfm (linear feet per minute). The approaching airflow temperature is assumed to be equal to the local-ambient temperature. The thermal designer must carefully select the location to measure airflow to obtain an accurate estimate. These local-ambient conditions are based on a 35 °C external-ambient temperature at sea level. (External-ambient refers to the environment external to the system.)

6.2 Mechanical Design Envelope

Though each design may have unique mechanical volume and height restrictions or implementation requirements, the height, width, and depth constraints typically placed on the E7500 MCH thermal solution is shown in Figure 8.

When using heatsinks that extend beyond the MCH reference heatsink envelope shown in Figure 8, any motherboard components placed between the heatsink and motherboard cannot exceed 2.286 mm (0.090 in.) in height.
Figure 8. Reference Heatsink Volumetric Envelope for the MCH

NOTE: Not to scale.
6.3 Thermal Solution Assembly

The reference thermal solution is a passive extruded heatsink with thermal and mechanical interfaces. It is attached using a clip with each end hooked through an anchor soldered to the board. Figure 9 shows the reference thermal solution assembly and associated components.

Figure 9 and Figure 10 show alternate views of the reference solution. Full mechanical drawings of the thermal solution assembly and the heatsink clip are provided in Appendix B.

Appendix A contains vendor information for each thermal solution component.

Figure 9. Reference Thermal Solution Assembly
Figure 10. Reference Thermal Solution Assembly (Side View)

Figure 11. Reference Thermal Solution (Top View)
6.3.1 Heatsink Orientations

To enhance the efficiency of the reference thermal solution, it is important for the designer to orient the fins properly with respect to the mean airflow direction. Simulation and experimental evidence have shown that the MCH heatsink thermal performance is enhanced when the fins are aligned with the mean airflow direction (Figure 12). Aligning the heatsink 45° relative to the airflow is acceptable but delivers reduced thermal performance.

Figure 12. Preferred Heatsink Orientation
6.3.2 Extruded Heatsink Profiles

The E7500 chipset reference thermal solution uses an extruded heatsink for cooling the MCH. Figure 13 shows the heatsink profile. This document does not provide tolerance information. Check with your heatsink supplier for specific tolerances. Appendix A lists suppliers for the extruded heatsink. Other heatsinks with similar dimensions and increased thermal performance may be available, including the tall heatsink shown in Figure 14. Contact your heatsink supplier for information on alternate heatsinks.

Figure 13. Extruded Heatsink Profile

![Extr_Heatsink_Profile](image1)

**NOTE:** Not to scale.

Figure 14. Alternate Tall Heatsink Profile

![Alt_Extr_Heatsink_Profile](image2)

**NOTE:** Not to scale.
6.3.3 Mechanical Interface Material

Intel recommends the use of a mechanical interface material to avoid cracking of the exposed die under loading. The interface material reduces mechanical loads experienced by the die. The reference thermal solution uses a picture frame gasket of 0.813 mm (0.032 in.) thick Poron* foam. The foam gasket is a two-piece design with diagonal cuts at two corners as shown in Figure 15. A one-piece gasket design may be used instead without any impact to mechanical performance.

Figure 15. Heatsink Mechanical Gasket, Optional Two-Piece

![Diagram of Heatsink Mechanical Gasket](Heatsink_Gasket)

NOTE: Not to scale.

6.3.4 Thermal Interface Material

A thermal interface material provides improved conductivity between the die and heatsink. The reference thermal solution uses Chomerics* T-710, 0.127 mm (0.005 in.) thick, 25.4 mm x 25.4 mm (1.0 in. x 1.0 in.) square.

6.3.5 Heatsink Clip

The reference solution uses a wire clip with hooked ends. The hooks attach to wire anchors to fasten the clip to the board. See Figure 19 in Appendix B for a mechanical drawing of the clip.
6.3.6 Clip Retention Anchors

For E7500 chipset-based platforms that have very limited board space, a clip retention anchor has been developed to minimize the impact of clip retention on the board. It is based on a standard three-pin jumper and is soldered to the board like any common through-hole header. A new anchor design is available with 45° bent leads to increase the anchor attach reliability over time. See Appendix A for the part number and supplier information.

6.3.7 Board Level Component Keep-out Dimensions

The locations of hole patterns and keep-out zones for the reference thermal solution are shown in Figure 16 and Figure 17.

Figure 16. Heatsink Retention Mechanism Layout

NOTES:
1. Dimensions are in inches.
2. Not to scale.
**Figure 17. Retention Mechanism Component Keep-out Zones**

**NOTES:**
1. Dimensions are in inches.
2. Not to scale.
6.4 Reliability Requirements

Each motherboard, heatsink and attach combination may vary the mechanical loading of the component. The user should carefully evaluate the reliability of the completed assembly prior to use in high volume. Some general recommendations are shown in Table 2.

Table 2. Reliability Requirements

<table>
<thead>
<tr>
<th>Test</th>
<th>Requirement</th>
<th>Pass/Fail Criteria</th>
</tr>
</thead>
<tbody>
<tr>
<td>Mechanical Shock</td>
<td>50 g, board level, 11 msec, 3 shocks/axis</td>
<td>Visual Check and Electrical Functional Test</td>
</tr>
<tr>
<td>Random Vibration</td>
<td>7.3 g, board level, 45 min/axis, 50 Hz to 2000 Hz</td>
<td>Visual Check and Electrical Functional Test</td>
</tr>
<tr>
<td>Temperature Life</td>
<td>85 °C, 2000 hours total, checkpoints at 168, 500, 1000, and 2000 hours</td>
<td>Visual Check</td>
</tr>
<tr>
<td>Thermal Cycling</td>
<td>-5 °C to +70 °C, 500 cycles</td>
<td>Visual Check</td>
</tr>
<tr>
<td>Humidity</td>
<td>85% relative humidity, 55 °C, 1000 hours</td>
<td>Visual Check</td>
</tr>
</tbody>
</table>

NOTES:
1. The tests should be performed on a sample size of at least 12 assemblies from 3 lots of material.
2. Additional Pass/Fail Criteria may be added at the discretion of the user.
## Appendix A: Thermal Solution Component Suppliers

### Table 3. Complete Thermal Solution Kits

<table>
<thead>
<tr>
<th>Part</th>
<th>Intel Part Number</th>
<th>Supplier</th>
<th>Contact Information</th>
</tr>
</thead>
<tbody>
<tr>
<td>Pin Fin Heatsink Kit (31gm, 42 x 42 x 23 mm)</td>
<td>A69225-001</td>
<td>CCI</td>
<td>Dr. Dah-Chyi (DC) Kuo 886-2-2995-2666, x131 <a href="mailto:kuo@ccic.com.tw">kuo@ccic.com.tw</a></td>
</tr>
<tr>
<td></td>
<td></td>
<td>Foxconn</td>
<td>Bob Hall (503) 693-3509, x235 <a href="mailto:bhall@foxconn.com">bhall@foxconn.com</a></td>
</tr>
<tr>
<td>Alternate Pin Fin Heatsink Kit (43gm, 42 x 42 x 35 mm)</td>
<td>A69225-002</td>
<td>CCI</td>
<td>Dr. Dah-Chyi (DC) Kuo 886-2-2995-2666, x131 <a href="mailto:kuo@ccic.com.tw">kuo@ccic.com.tw</a></td>
</tr>
<tr>
<td></td>
<td></td>
<td>Foxconn</td>
<td>Bob Hall (503) 693-3509, x235 <a href="mailto:bhall@foxconn.com">bhall@foxconn.com</a></td>
</tr>
</tbody>
</table>

### Table 4. Extruded Heatsinks

<table>
<thead>
<tr>
<th>Part</th>
<th>Intel Part Number</th>
<th>Supplier</th>
<th>Contact Information</th>
</tr>
</thead>
<tbody>
<tr>
<td>Pin Fin Heatsink Kit (31gm, 42 x 42 x 23 mm)</td>
<td>A20930-001</td>
<td>CCI</td>
<td>Dr. Dah-Chyi (DC) Kuo 886-2-2995-2666, x131 <a href="mailto:kuo@ccic.com.tw">kuo@ccic.com.tw</a></td>
</tr>
<tr>
<td></td>
<td></td>
<td>Foxconn</td>
<td>Bob Hall (503) 693-3509, x235 <a href="mailto:bhall@foxconn.com">bhall@foxconn.com</a></td>
</tr>
<tr>
<td>Alternate Pin Fin Heatsink Kit (43gm, 42 x 42 x 35 mm)</td>
<td>A13506-001</td>
<td>CCI</td>
<td>Dr. Dah-Chyi (DC) Kuo 886-2-2995-2666, x131 <a href="mailto:kuo@ccic.com.tw">kuo@ccic.com.tw</a></td>
</tr>
<tr>
<td></td>
<td></td>
<td>Foxconn</td>
<td>Bob Hall (503) 693-3509, x235 <a href="mailto:bhall@foxconn.com">bhall@foxconn.com</a></td>
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</tbody>
</table>
**Appendix A: Thermal Solution Component Suppliers**

Table 5. Interface Materials

<table>
<thead>
<tr>
<th>Part</th>
<th>Intel Part Number</th>
<th>Supplier (Part Number)</th>
<th>Contact Information</th>
</tr>
</thead>
</table>
| Thermal Interface (T-710)     | —                 | Chomerics (69-12-22315-T710) | Todd Sousa  
(360) 891-2018  
tsousa@parker.com |
| Mechanical Interface (Poron*) | A69141-001        | Boyd                   | Rhoda Kennedy  
(503) 972-3170 |

Table 6. Attach Hardware

<table>
<thead>
<tr>
<th>Part</th>
<th>Intel Part Number</th>
<th>Supplier</th>
<th>Contact Information</th>
</tr>
</thead>
</table>
| Heatsink Attach Clip          | A69230-001        | CCI               | Dr. Dah-Chyi (DC) Kuo  
886-2-2995-2666, x131  
kuo@ccic.com.tw |
|                               |                   | Foxconn           | Bob Hall  
(503) 693-3509, x235  
bhall@foxconn.com |
| Solder-Down Anchor            | A13494-005        | Foxconn           | Julia Jiang  
(408) 919-6178  
jlaliaj@foxconn.com |

*Note:* The enabled components may not be currently available from all suppliers. Contact the supplier directly to verify time of component availability.
Appendix B: Mechanical Drawings

This appendix contains the following drawings:

- MCH Heatsink Assembly
- MCH Heatsink Clip
Figure 18. MCH Heatsink Assembly
Figure 19. MCH Heatsink Clip

NOTES:
1. ITEM IDENTIFICATION NUMBER IS A63230-001.
2. INSIDE BEND RADIUS TO BE .0625 UNLESS OTHERWISE SPECIFIED.
3. PART SHALL BE DEGREASED, WASHED, AND FREE OF OIL AND/OR DIRT MARKS.
4. INTEL PROCUREMENT SPECIFICATION A82140 SHALL APPLY.
5. ELECTRONIC DATA FOR THIS FILE EXISTS.
6. REMOVE ALL SHARP EDGES, REMOVE ALL BURRS.