Intel® E7221 Memory Controller Hub (MCH)

Thermal/Mechanical Design Guide

September 2004

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Revision History

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1 Introduction

As the complexity of computer systems increases, so do the power dissipation requirements. Care must be taken to ensure that the additional power is properly dissipated. Typical methods to improve heat dissipation include selective use of ducting, and/or passive heatsinks.

The goals of this document are to:

- Outline the thermal and mechanical operating limits and specifications for the Intel® E7221 chipset memory controller hub (MCH).
- Describe a reference thermal solution that meets the specification of the E7221 chipset MCH.

Properly designed thermal solutions provide adequate cooling to maintain the E7221 chipset MCH die temperatures at or below thermal specifications. This is accomplished by providing a low local-ambient temperature, ensuring adequate local airflow, and minimizing the die to local-ambient thermal resistance. By maintaining the E7221 chipset MCH die temperature at or below the specified limits, a system designer can ensure the proper functionality, performance, and reliability of the chipset. Operation outside the functional limits can degrade system performance and may cause permanent changes in the operating characteristics of the component.

The simplest and most cost effective method to improve the inherent system cooling characteristics is through careful chassis design and placement of fans, vents, and ducts. When additional cooling is required, component thermal solutions may be implemented in conjunction with system thermal solutions. The size of the fan or heatsink can be varied to balance size and space constraints with acoustic noise.

This document addresses thermal design and specifications for the E7221 chipset MCH component only. For thermal design information on other chipset components, refer to the respective component datasheet. For the PXH-V, refer to the *Intel® 6700PXH 64-bit PCI Hub (PXH) Thermal Design Guide*. For the ICH6, refer to the *Intel® I/O Controller Hub 6 (ICH6) Family Thermal Design Guide*.

Note: Unless otherwise specified, the term "MCH" refers to the E7221 chipset MCH.

1.1 Definition of Terms

BGA — Ball grid array. A package type, defined by a resin-fiber substrate, onto which a die is mounted, bonded and encapsulated in molding compound. The primary electrical interface is an array of solder balls attached to the substrate opposite the die and molding compound.

BLT — Bond line thickness. Final settled thickness of the thermal interface material after installation of heatsink.

ICH6 — I/O Controller Hub. The chipset component that contains the primary PCI interface, LPC interface, USB2, ATA-100, and other I/O functions. It communicates with the MCH over a proprietary interconnect called Direct Media Interface (DMI).

MCH — Memory controller hub. The chipset component that contains the processor interface, the memory interface, and the DMI interface.

PXH-V Intel® 6702PXH 64-bit PCI Hub. The chipset component that performs PCI bridging functions between the PCI Express* interface and the PCI Bus. It contains one PCI bus interface that can be independently configured to operate in PCI (33 or 66 MHz) or PCI-X mode 1 (66, 100 or 133 MHz), for either 32 or 64 bit PCI devices.

T_{case_max} Maximum die temperature allowed. This temperature is measured at the geometric center of the top of the package die.

T_{case_min} Minimum die temperature allowed. This temperature is measured at the geometric center of the top of the package die.

TDP Thermal design power. Thermal solutions should be designed to dissipate this target power level. TDP is not the maximum power that the chipset can dissipate.

1.2 Reference Documents

The reader of this specification should also be familiar with material and concepts presented in the following documents:

- *Intel® I/O Controller Hub 6 (ICH6) Family Datasheet*
- *Intel® I/O Controller Hub 6 (ICH6) Family Thermal Design Guide*
- *Intel®6700PXH 64-bit PCI Hub (PXH) Thermal/Mechanical Design Guide*
- *Intel® 6700PXH 64-bit PCI Hub (PXH) Datasheet*
- *Intel® E7221 Chipset Datasheet*
- *Intel® E7221 Chipset Specification Update*
- *Intel® Pentium® 4 Processor on 90 nm Process in the 775-Land LGA Package Thermal and Mechanical Design Guidelines*
- *Intel® Pentium® 4 Processor 560, 550, 540, 530 and 520 Datasheet On 90 nm Process in the 775-Land LGA Package Supporting Hyper-Threading Technology*
- *Intel® 82865G/82865GV GMCH and Intel® 82865PE/828865P MCH Thermal Design Guide*
- *BGA/OLGA Assembly Development Guide*
- Various system thermal design suggestions (http://www.formfactors.org)

Note: Unless otherwise specified, these documents are available through your Intel field sales representative. Some documents may not be available at this time.

2 Packaging Technology

The E7221 chipset consists of three individual components: the MCH, the PXH-V and the I/O controller hub (ICH6). The E7221 chipset MCH component uses a 37.5 mm, 6-layer flip chip ball grid array (FC-BGA) package (see Figure 2-1, Figure 2-2, and Figure 2-3). For information on the PXH-V package, refer to the *Intel® 6700PXH 64-bit PCI Hub (PXH) Thermal/Mechanical Design Guide*. For information on the ICH6 package, refer to *Intel® I/O Controller Hub 6 (ICH6) Family Thermal Design Guide*.

Figure 2-1. MCH Package Dimensions (Top View)

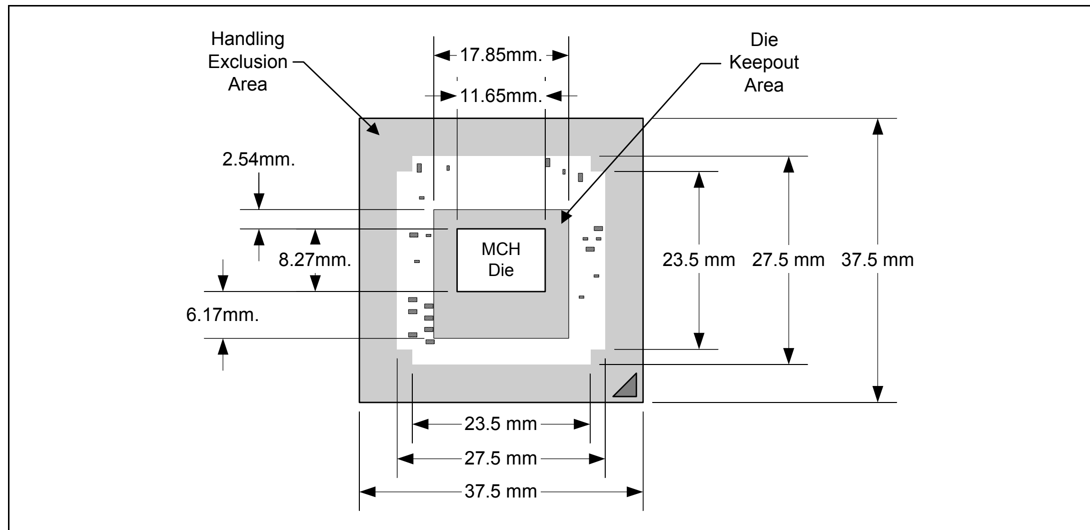
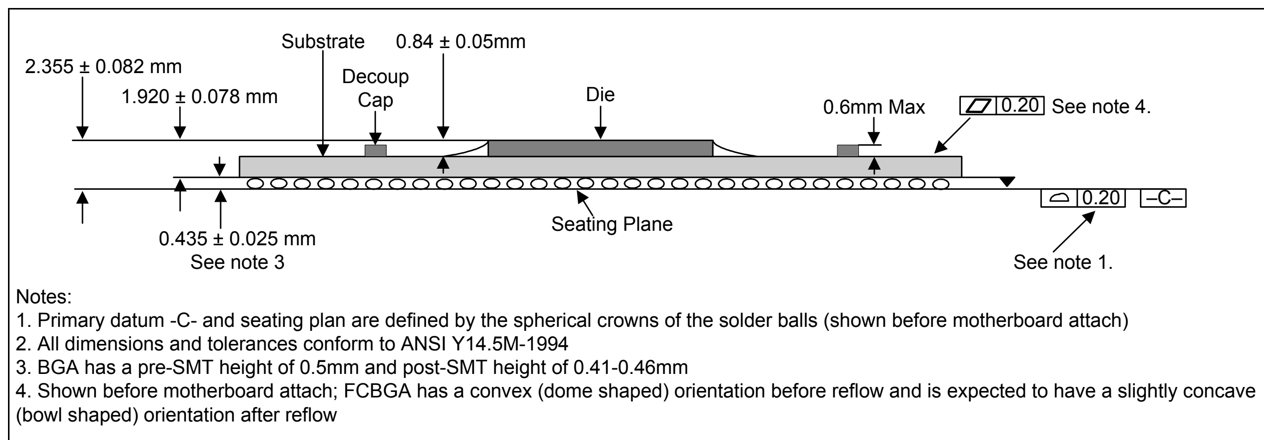
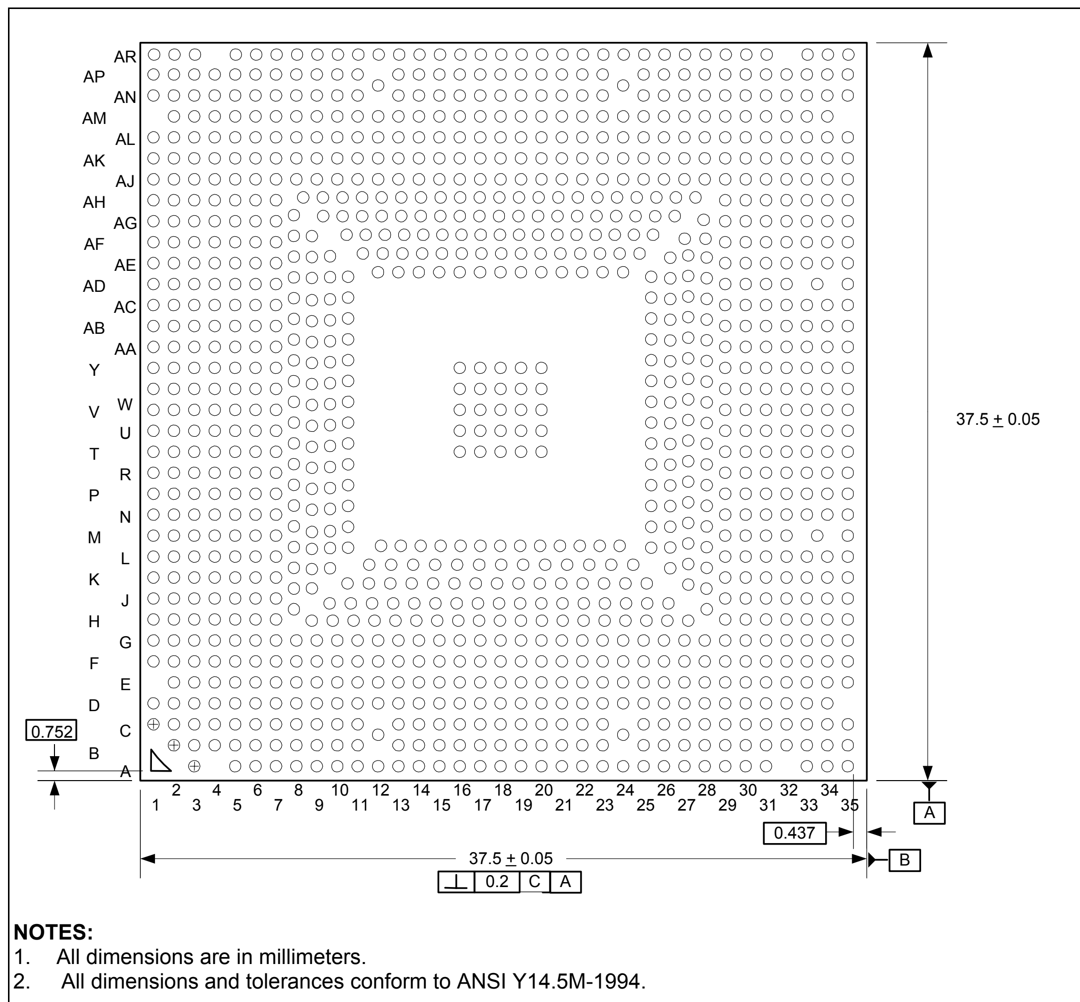


Figure 2-2. MCH Package Dimensions (Side View)



Notes:
1. Primary datum -C- and seating plan are defined by the spherical crowns of the solder balls (shown before motherboard attach)
2. All dimensions and tolerances conform to ANSI Y14.5M-1994
3. BGA has a pre-SMT height of 0.5mm and post-SMT height of 0.41-0.46mm
4. Shown before motherboard attach; FCBGA has a convex (dome shaped) orientation before reflow and is expected to have a slightly concave (bowl shaped) orientation after reflow

Figure 2-3. MCH Package Dimensions (Bottom View)



2.1 Package Mechanical Requirements

The E7221 chipset MCH package has an exposed bare die which is capable of sustaining a maximum static normal load of 15-lbf. The package is NOT capable of sustaining a dynamic or static compressive load applied to any edge of the bare die. These mechanical load limits must not be exceeded during heatsink installation, mechanical stress testing, standard shipping conditions and/or any other use condition.

Notes:

1. The heatsink attach solutions must not include continuous stress onto the chipset package with the exception of a uniform load to maintain the heatsink-to-package thermal interface.
2. These specifications apply to uniform compressive loading in a direction perpendicular to the bare die/IHS top surface.
3. These specifications are based on limited testing for design characterization. Loading limits are for the package only

3 Thermal Specifications

3.1 Thermal Design Power (TDP)

Analysis indicates that real applications are unlikely to cause the chipset MCH to consume maximum power dissipation for sustained time periods. Therefore, in order to arrive at a more realistic power level for thermal design purposes, Intel characterizes power consumption based on known platform benchmark applications. The resulting power consumption is referred to as the Thermal Design Power (TDP). TDP is the target power level that the thermal solutions should be designed to. TDP is not the maximum power that the chipset can dissipate.

For TDP specifications of the E7221 chipset MCH, see Table 3-1. FC-BGA packages have poor heat transfer capability into the board and have minimal thermal capability without a thermal solution. Intel recommends that system designers plan for a heatsink when using the E7221 chipsets

3.2 Die Case Temperature Specifications

To ensure proper operation and reliability of the E7221 chipset MCH, the die temperatures must be at or between the maximum/minimum operating temperature ranges as specified in Table 3-1. System and/or component level thermal solutions are required to maintain these temperature specifications. Refer to Chapter 5 for guidelines on accurately measuring package die temperatures.

Table 3-1. E7221 Chipset MCH Thermal Specifications

Parameter	Value	Notes
T_{case_max}	105°C	
T_{case_min}	5°C	
$TDP_{dual\ channel}$	16.9 W	DDR-333
$TDP_{dual\ channel}$	17.9 W	DDR-400
$TDP_{dual\ channel}$	14.8 W	DDR2-400
$TDP_{dual\ channel}$	15.7 W	DDR2-533

Note: These specifications are based on silicon characterization, however, they may be updated as further data becomes available.

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4 Thermal Simulation

Intel provides thermal simulation models of the E7221 chipset MCH and associated user's guides to aid system designers in simulating, analyzing, and optimizing their thermal solutions in an integrated, system-level environment. The models are for use with the commercially available Computational Fluid Dynamics (CFD)-based thermal analysis tool “ICEPAK”*. Contact your Intel field sales representative to order the thermal models and user's guides.

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5 Thermal Metrology

The system designer must make temperature measurements to accurately determine the thermal performance of the system. Intel has established guidelines for proper techniques to measure the MCH die temperatures. Section 5.1 provides guidelines on how to accurately measure the MCH die temperatures. The flowchart in Figure 5-1 offers useful guidelines for thermal performance and evaluation.

5.1 Die Case Temperature Measurements

To ensure functionality and reliability, the T_{case} of the MCH must be maintained at or between the maximum/minimum operating range of the temperature specification as noted in Table 3-1. The surface temperature at the geometric center of the die corresponds to T_{case}. Measuring T_{case} requires special care to ensure an accurate temperature measurement.

Temperature differences between the temperature of a surface and the surrounding local ambient air can introduce errors in the measurements. The measurement errors could be due to a poor thermal contact between the thermocouple junction and the surface of the package, heat loss by radiation and/or convection, conduction through thermocouple leads, and/or contact between the thermocouple cement and the heatsink base (if a heatsink is used). For maximize measurement accuracy, only the 0° thermocouple attach approach is recommended.

Zero Degree Angle Attach Methodology

1. Mill a 3.3 mm (0.13 in.) diameter and 1.5 mm (0.06 in.) deep hole centered on the bottom of the heatsink base.
2. Mill a 1.3 mm (0.05 in.) wide and 0.5 mm (0.02 in.) deep slot from the centered hole to one edge of the heatsink. The slot should be parallel to the heatsink fins (see Figure 5-2).
3. Attach thermal interface material (TIM) to the bottom of the heatsink base.
4. Cut out portions of the TIM to make room for the thermocouple wire and bead. The cutouts should match the slot and hole milled into the heatsink base.
5. Attach a 36 gauge or smaller calibrated K-type thermocouple bead or junction to the center of the top surface of the die using a high thermal conductivity cement. During this step, ensure no contact is present between the thermocouple cement and the heatsink base because any contact will affect the thermocouple reading. **It is critical that the thermocouple bead makes contact with the die** (see Figure 5-3).
6. Attach heatsink assembly to the MCH and route thermocouple wires out through the milled slot.

Figure 5-1. Thermal Solution Decision Flowchart

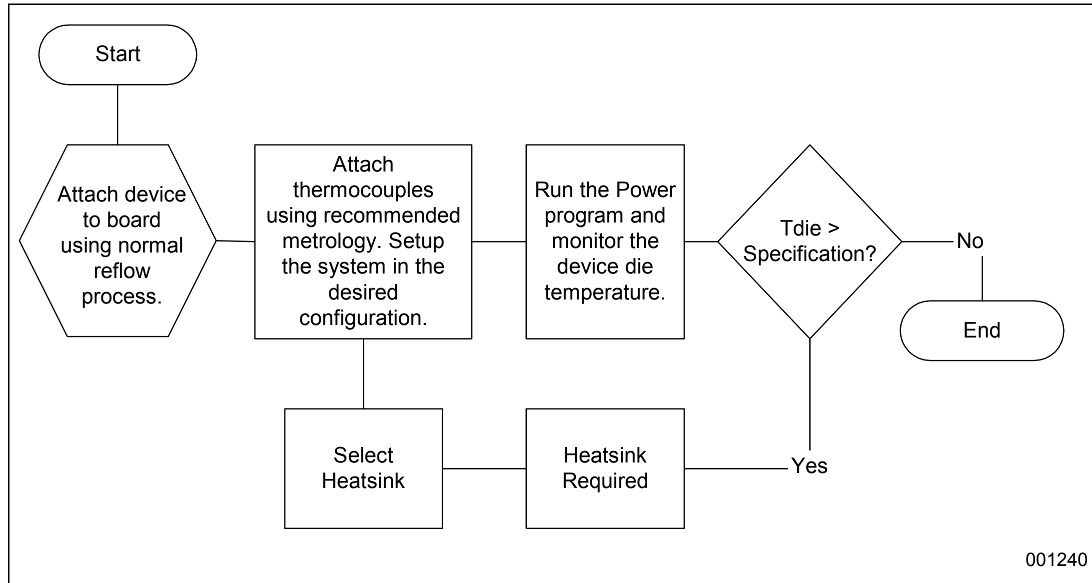
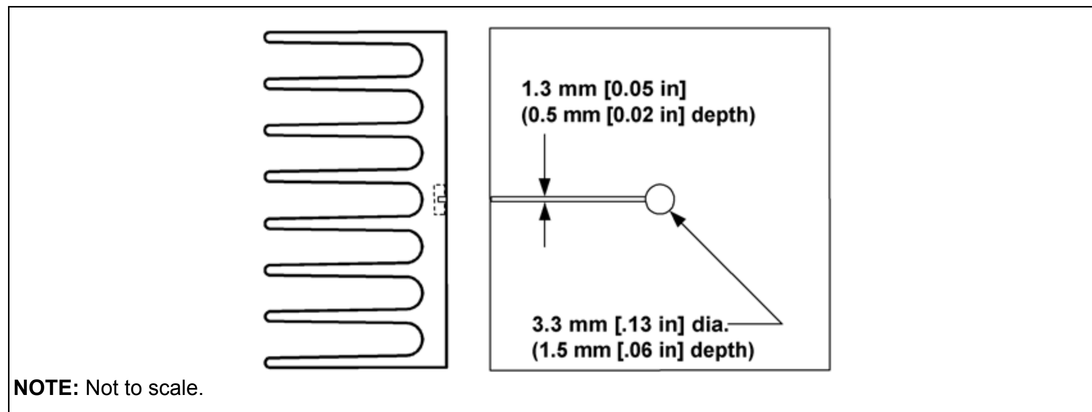
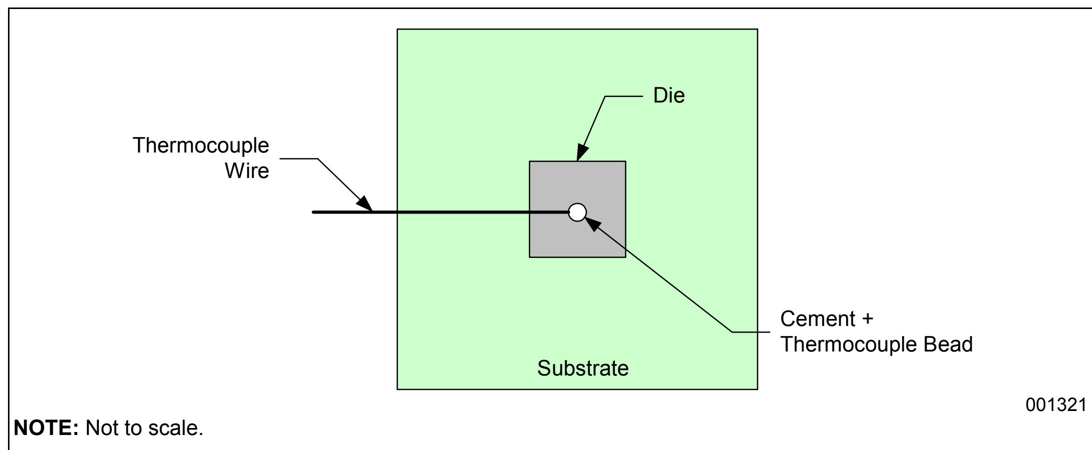


Figure 5-2. Zero Degree Angle Attach Heatsink Modifications



NOTE: Not to scale.

Figure 5-3. Zero Degree Angle Attach Methodology (Top View)



NOTE: Not to scale.

6 Reference Thermal Solution

Intel has developed a reference thermal solution designed to meet the cooling needs of the E7221 chipset MCH under operating environments and specifications defined in this document. This chapter describes the overall requirements for the wave solder heatsink (WSHS) reference thermal solution including critical-to-function dimensions, operating environment, and validation criteria. For manufacturing related information associated with this reference solution, refer to thermal solution section in the *Intel® 865G/865GV/865PE/865P Chipset Thermal Design Guide*. Other chipset components may or may not need attached thermal solutions, depending on your specific system local-ambient operating conditions. For information on the PXH-V, refer to thermal specification in the *Intel® 6700PXH 64-bit PCI Hub (PXH) Thermal/Mechanical Design Guide*. For information on the ICH6, refer to thermal specification in the *Intel® I/O Controller Hub 6 (ICH6) Family Thermal Design Guide*.

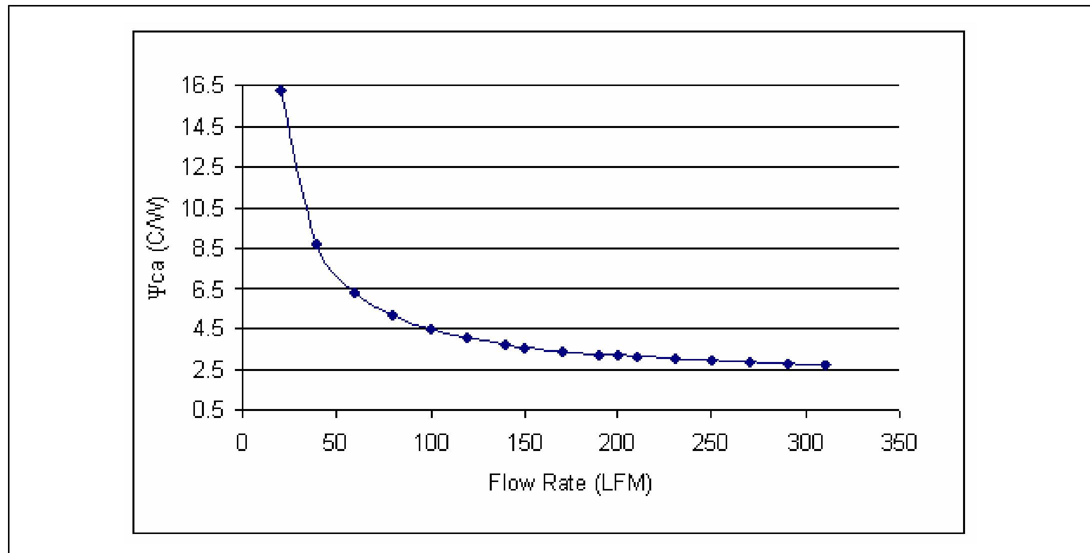
6.1 Operating Environment

The chipset MCH reference thermal solution was designed assuming a maximum local-ambient temperature of 45°C. The minimum recommended airflow velocity through the cross section of the heatsink fins is 200 linear feet per minute (lfm). The approaching airflow temperature is assumed to be equal to the local-ambient temperature. The thermal designer must carefully select the location to measure airflow to obtain an accurate estimate. These local-ambient conditions are based on a 35°C external-ambient temperature at sea level. (External-ambient refers to the environment external to the system.)

6.2 Heatsink Performance

Figure 6-1 depicts the measured thermal performance of the reference thermal solution versus approach air velocity. Since this data was measured at sea level, a correction factor would be required to estimate thermal performance at other altitudes.

Figure 6-1. MCH Heatsink Measured Thermal Performance vs. Approach Velocity

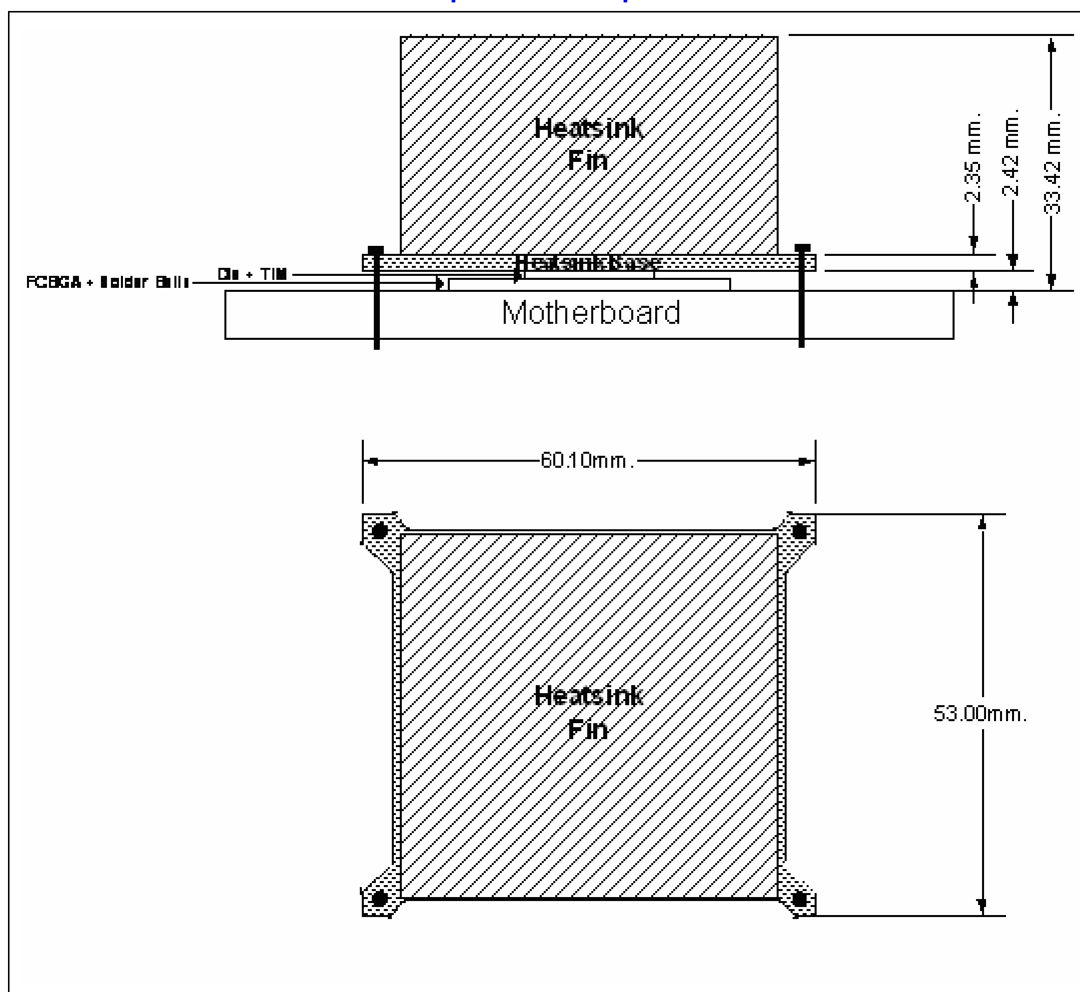


6.3 Mechanical Design Envelope

While each design may have unique mechanical volume and height restrictions or implementation requirements, the height, width, and depth constraints typically placed on the E7221 chipset MCH thermal solution are shown in Figure 6-2.

When using heatsinks that extend beyond the chipset MCH reference heatsink envelope shown in Figure 6-2, any motherboard components placed between the heatsink and motherboard cannot exceed 2.20 mm (0.087 in.) in height.

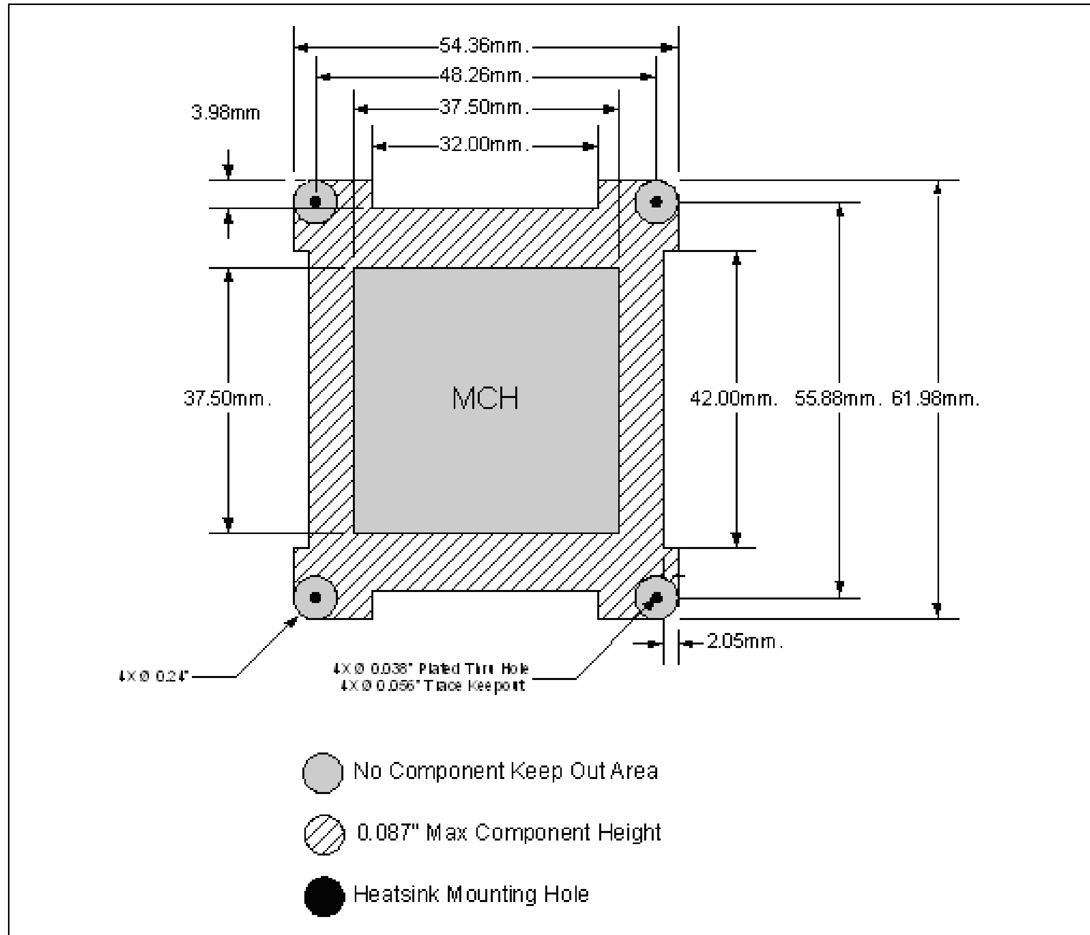
Figure 6-2. MCH Heatsink Volumetric Envelope for the Chipset MCH



6.4 Board-Level Components Keepout Dimensions

The location of hole pattern and keepout zones for the reference thermal solution are shown in Figure 6-3.

Figure 6-3. MCH Heatsink Board Component Keepout



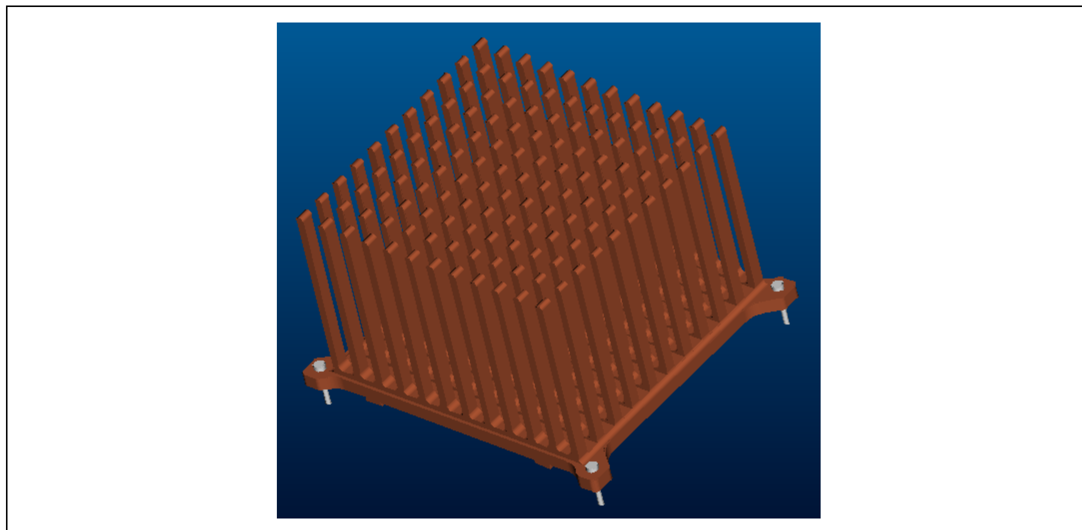
6.5 MCH Heatsink Thermal Solution Assembly

The reference thermal solution consists of a passively cooled WSHS. The heatsink is comprised of an extruded aluminum heatsink with four mounting pins pressed into each corner of the heatsink base. A TIM (Chomerics T-710*) is pre-applied to the heatsink bottom over an area in contact with the package die. A straight cut is performed on the heatsink base in order to create rails to reduce the possibility of tilt when assembling the WSHS.

Note: The rails do not touch the package substrate in the nominal position. The WSHS is shown in the installed configuration in Figure 6-4. (The Intel® E7221 chipset MCH cannot be seen in this view as it is hidden by the WSHS base).

Full mechanical drawings of the thermal solution assembly and the mounting pins are provided in Appendix B. Appendix A contains vendor information for each thermal solution component.

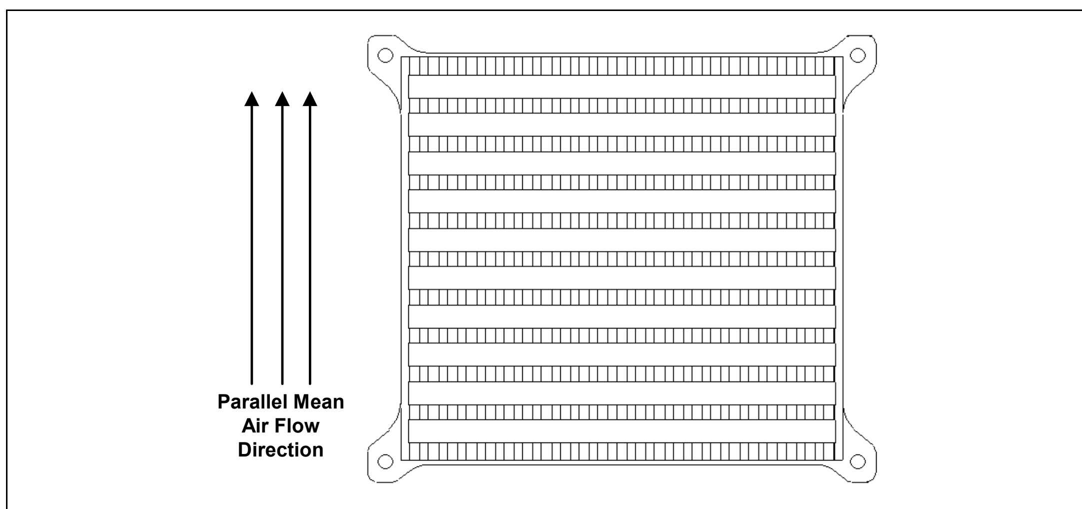
Figure 6-4. Wave Solder Heatsink Assembly



6.5.1 Heatsink Orientation

To enhance the efficiency of the reference thermal solution, it is important for the designer to orient the fins properly with respect to the mean airflow direction. Simulation and experimental evidence have shown that the MCH heatsink thermal performance is enhanced when the fins are aligned with the mean airflow direction (see Figure 6-5).

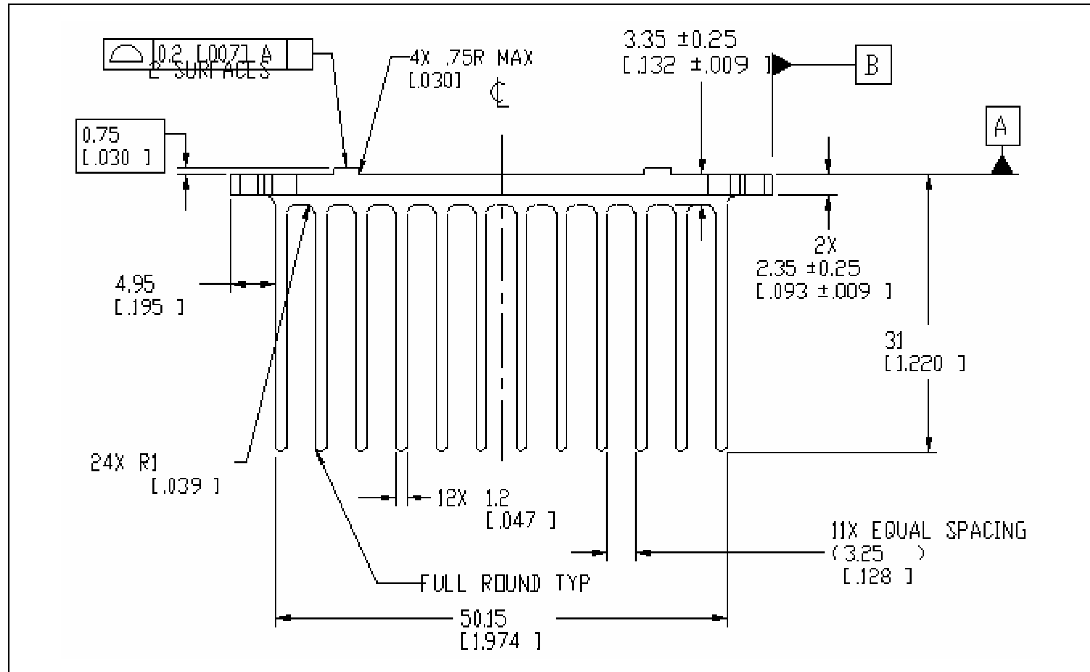
Figure 6-5. Preferred Heatsink Orientation



6.5.2 Extruded Heatsink Profiles

The reference thermal solution uses an extruded heatsink for cooling the chipset MCH. Figure 6-6 shows the heatsink profile. Appendix A lists a supplier for this extruded heatsink. Other heatsinks with similar dimensions and increased thermal performance may be available. Full mechanical drawing of this heatsink is provided in Appendix B.

Figure 6-6. Wave Solder Heatsink Extrusion Profile



6.5.3 Mechanical Interface Material

There is no mechanical interface material associated with this reference solution.

6.5.4 Thermal Interface Material

A TIM provides improved conductivity between the die and heatsink. The reference thermal solution uses Chomerics T-710*, 0.127 mm (0.005 in.) thick, 19 mm x 19 mm (0.75 in. x 0.75 in.) square.

Note: Unflowed or "dry" Chomerics T710 has a material thickness of 0.005 inch. The flowed or "wet" Chomerics T710 has a material thickness of ~0.0025 inch after it reaches its phase change temperature.

6.5.4.1 Effect of Pressure on TIM Performance

As mechanical pressure increases on the TIM, the thermal resistance of the TIM decreases. This phenomenon is due to the decrease of the bond line thickness (BLT). BLT is the final settled thickness of the thermal interface material after installation of heatsink. The effect of pressure on the thermal resistance of the Chomerics T710 TIM is shown in Table 6-1. The heatsink mounting pins provide enough pressure for the TIM to achieve a thermal conductivity of 0.17°C inch^2/W.

Table 6-1. Chomerics T710* TIM Performance as a Function of Attach Pressure

Pressure (psi)	Thermal Resistance (°C × in^2)/W
5	0.37
10	0.30
20	0.21
30	0.17

NOTE: All measured at 50°C.

6.5.5 Heatsink Clip

There is no heatsink clip associated with this reference solution.

6.5.6 Clip Retention Anchors

There are no clip retention anchors associated with this reference solution.

6.6 Reliability Guidelines

Each motherboard, heatsink and attach combination may vary the mechanical loading of the component. Based on the end user environment, the user should define the appropriate reliability test criteria and carefully evaluate the completed assembly prior to use in high volume. Some general recommendations are shown in Table 6-2.

Table 6-2. Reliability Guidelines

Test (1)	Requirement	Pass/Fail Criteria (2)
Mechanical Shock	50 g, board level, 11 msec, 3 shocks/axis	Visual Check and Electrical Functional Test
Random Vibration	7.3 g, board level, 45 min/axis, 50 Hz to 2000 Hz	Visual Check and Electrical Functional Test
Temperature Life	85°C, 2000 hours total, checkpoints at 168, 500, 1000, and 2000 hours	Visual Check
Thermal Cycling	–5°C to +70°C, 500 cycles	Visual Check
Humidity	85% relative humidity, 55°C, 1000 hours	Visual Check

NOTES:

1. It is recommended that the above tests be performed on a sample size of at least twelve assemblies from three lots of material.
2. Additional pass/fail criteria may be added at the discretion of the user.

A Thermal Solution Component Suppliers

Table A-1. MCH Heatsink Thermal Solution

Part	Intel Part Number	Supplier (Part Number)	Contact Information
Heatsink Assembly includes: • Pin Fin Heatsink • Solder Pin • Thermal Interface Material	C47021-001	CCI/ACK	Harry Lin (USA) 714-739-5797 hlinack@aol.com Monica Chih (Taiwan) (866) 2-29952666, x131 monica_chih@ccic.com.tw
		Foxconn	Kevin Tao (USA) 714-626-1278 kevintao@foxconn.com Cheow-Kooi Lee (Malaysia) (60) 4-6122122 leeck@foxconn.com
Pin Fin Heatsink (No Solder Pin)	C47020-001	CCI/ACK	Harry Lin (USA) 714-739-5797 hlinack@aol.com Monica Chih (Taiwan) (866) 2-29952666, x131 monica_chih@ccic.com.tw
		Foxconn	Kevin Tao (USA) 714-626-1278 kevintao@foxconn.com Cheow-Kooi Lee (Malaysia) (60) 4-6122122 leeck@foxconn.com
Solder Pin	A86593-001	CCI/ACK	Harry Lin (USA) 714-739-5797 hlinack@aol.com Monica Chih (Taiwan) (866) 2-29952666, x131 monica_chih@ccic.com.tw
		Foxconn	Kevin Tao (USA) 714-626-1278 kevintao@foxconn.com Cheow-Kooi Lee (Malaysia) (60) 4-6122122 leeck@foxconn.com
Thermal Interface (T-710)	–	Chomerics (69-12-22350-T710)	Todd Sousa (USA) 360-606-8171 tsousa@parker.com

Note: The enabled components may not be currently available from all suppliers. Contact the supplier directly to verify time of component availability.§

B Mechanical Drawings

Table B-1. Mechanical Drawing List

Drawing Description	Figure Number
MCH Waver Solder Heatsink Assembly Drawing	Figure B-1
MCH Wave Solder Heatsink Drawing	Figure B-2
MCH Heatsink Mounting Pin Drawing	Figure B-3

Figure B-1. MCH Waver Solder Heatsink Assembly Drawing

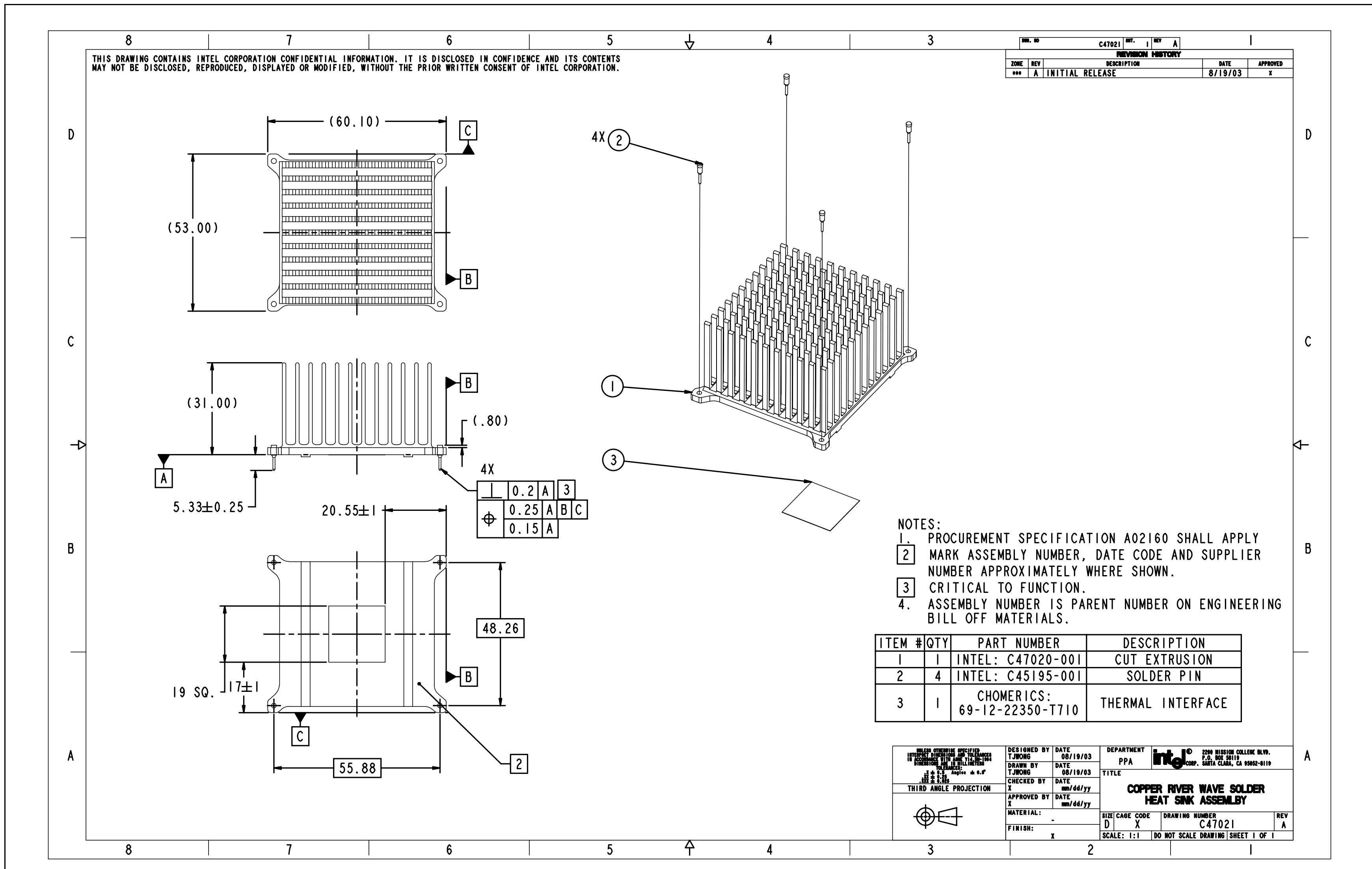


Figure B-2. MCH Wave Solder Heatsink Drawing

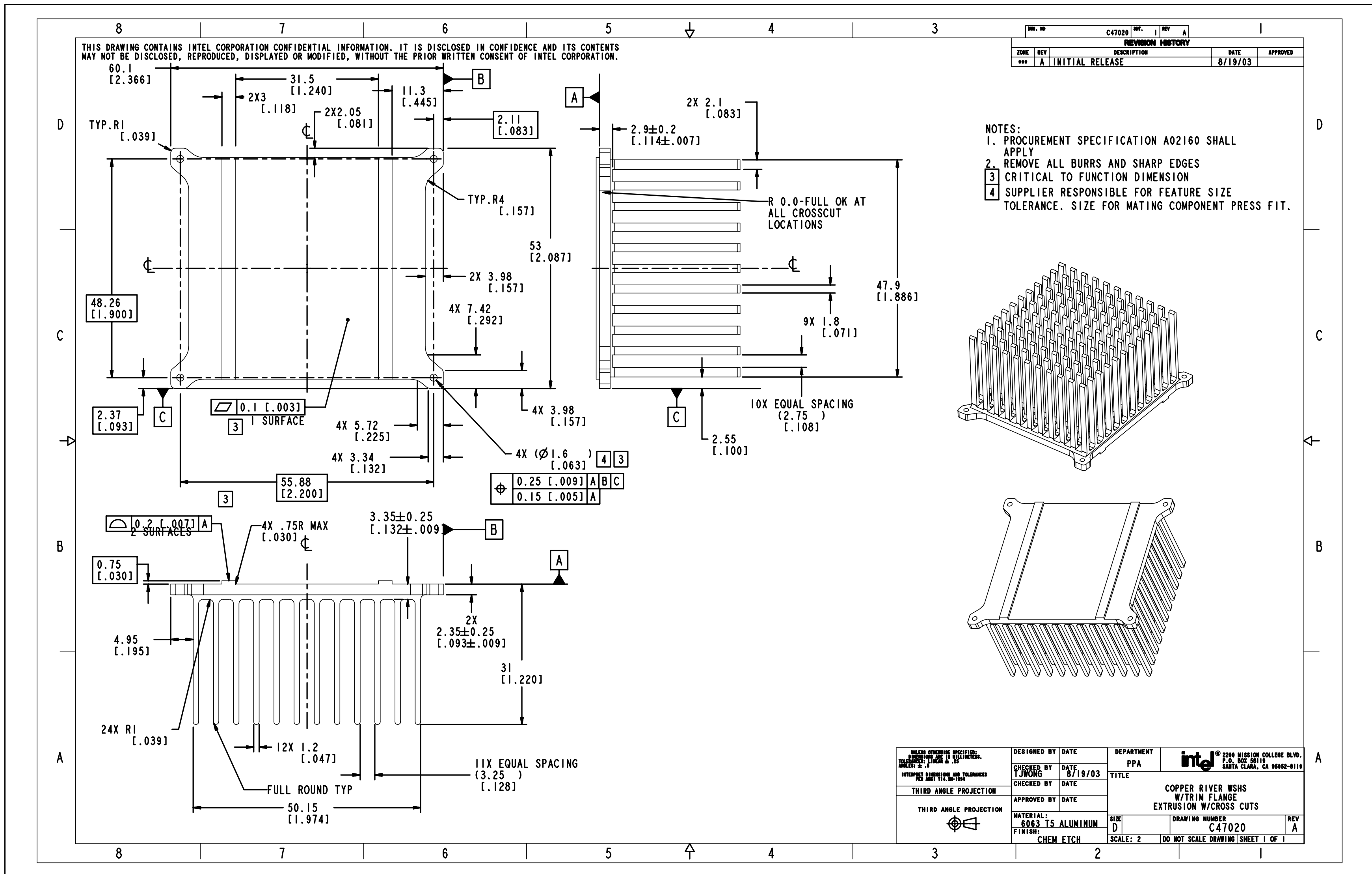


Figure B-3. MCH Heatsink Mounting Pin Drawing