Intel® E7205 Chipset

Thermal Design Guide

Intel® E7205 Chipset Memory Controller Hub (MCH) Thermal and Mechanical Design Guidelines

November 2002

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Revision History

Revision Number	Description	Date
-001	Initial Release	November 2002

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1 Introduction

As the complexity of computer systems increase, so do the power dissipation requirements. Care must be taken to ensure that the additional power is properly dissipated. Typical methods to improve heat dissipation include selective use of ducting, and/or passive heatsinks.

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The goals of this document are:

1. To specify the operating limits of the Intel® E7205 chipset MCH.
2. To describe e a reference thermal solutions that meets the thermal specifications of the Intel® E7205 chipset MCH.

Properly designed solutions provide adequate cooling to maintain the E7205 chipset MCH die temperatures at or below thermal specifications. This is accomplished by providing a low local-ambient temperature, ensuring adequate local airflow, and minimizing the die to local-ambient thermal resistance. By maintaining the MCH die temperature at or below the specified limits, a system designer can ensure the proper functionality, performance, and reliability of the chipset. Operation outside the functional limits can degrade system performance and may cause permanent changes in the operating characteristics of the component.

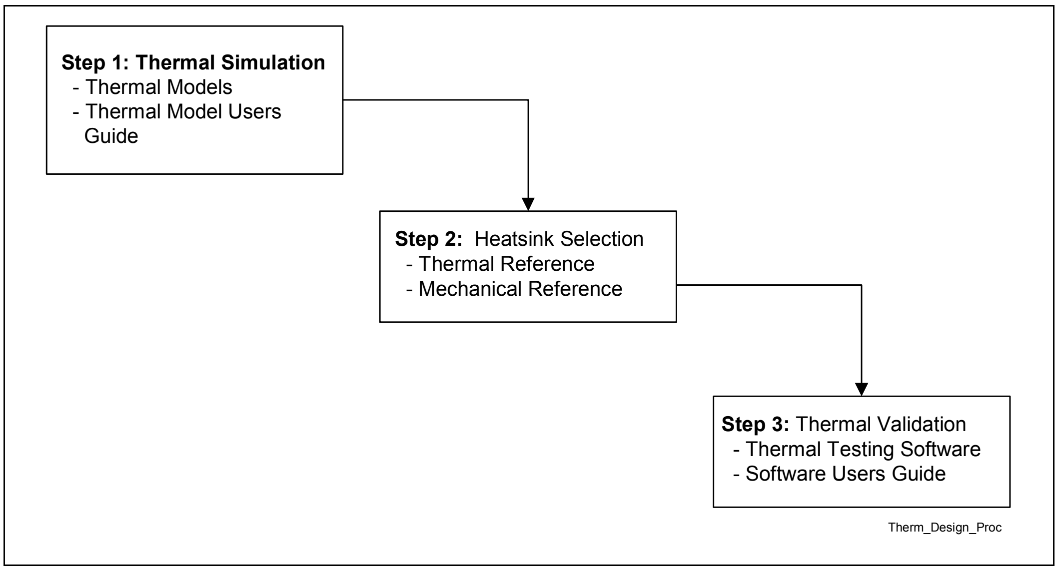
The simplest and most cost effective method is to improve the inherent system cooling characteristics through careful design and placement of fans, vents, and ducts. When additional cooling is required, component thermal solutions may be implemented in conjunction with system thermal solutions. The size of the fan or heatsink can be varied to balance size and space constraints with acoustic noise.

This document addresses thermal design and specifications for the E7205 chipset MCH component only. For thermal design information on other chipset components, refer to the respective component datasheet. For the ICH4, refer to the *Intel® 82801DB I/O Controller Hub 4 (ICH4) Datasheet*.

1.1 Design Flow

To develop a reliable, cost-effective thermal solution, several tools have been provided to the system designer. Figure 1 illustrates the design process implicit to this document and the tools appropriate for each step.

Figure 1. Thermal Design Process



1.2 Definition of Terms

Term	Definition
BGA	Ball Grid Array. A package type defined by a resin-fiber substrate, onto which a die is mounted, bonded and encapsulated in molding compound. The primary electrical interface is an array of solder balls attached to the substrate opposite the die and molding compound.
Intel® ICH4	I/O Controller Hub 4. The chipset component that contains the primary PCI interface, LPC interface, USB, ATA-33, and other legacy functions.
MCH	Memory Controller Hub. The chipset component that contains the processor interface and the memory interface.
FC-BGA	Flip Chip Ball Grid Array. A package type defined by a resin-fiber substrate where a die is mounted using an underfilled C4 (Controlled Collapse Chipset Connection) attach style. The primary electrical interface is an array of solder balls attached to the substrate opposite the die. The device arrives at the customer with solder balls attached. This is the packaging technology used for the MCH.
T_{case}	Maximum die temperature allows. This temperature is measured at the geometric center of the top of the package die.
TDP	Thermal Design Power. Thermal solutions should be designed to dissipate this target power level.

1.3 Reference Documents

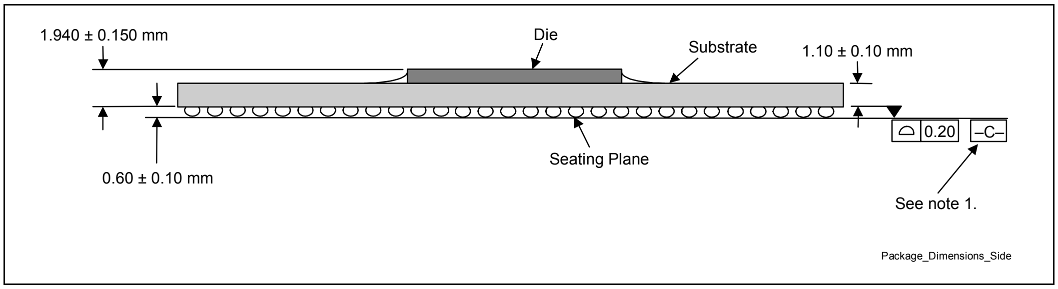
Document	Document Number/Location
Intel® Pentium 4 Processor with 512-KB L2 Cache on 0.13 Micron Process Datasheet	298643
Intel® Pentium 4 Processor and Intel® E7205 Chipset Platform Design Guide	251939
Intel® E7205 Chipset Memory Controller Hub (MCH) Datasheet	251937
Intel® 82801BA I/O Controller Hub 4 (ICH 4) Datasheet	290744
BGA/OLGA Assembly Development Guide	Note 1
Thermal Design Suggestions for various form factors	http://www.formfactors.org

NOTES:
1. Contact your Intel Field Sales representative.

2 Packaging Technology

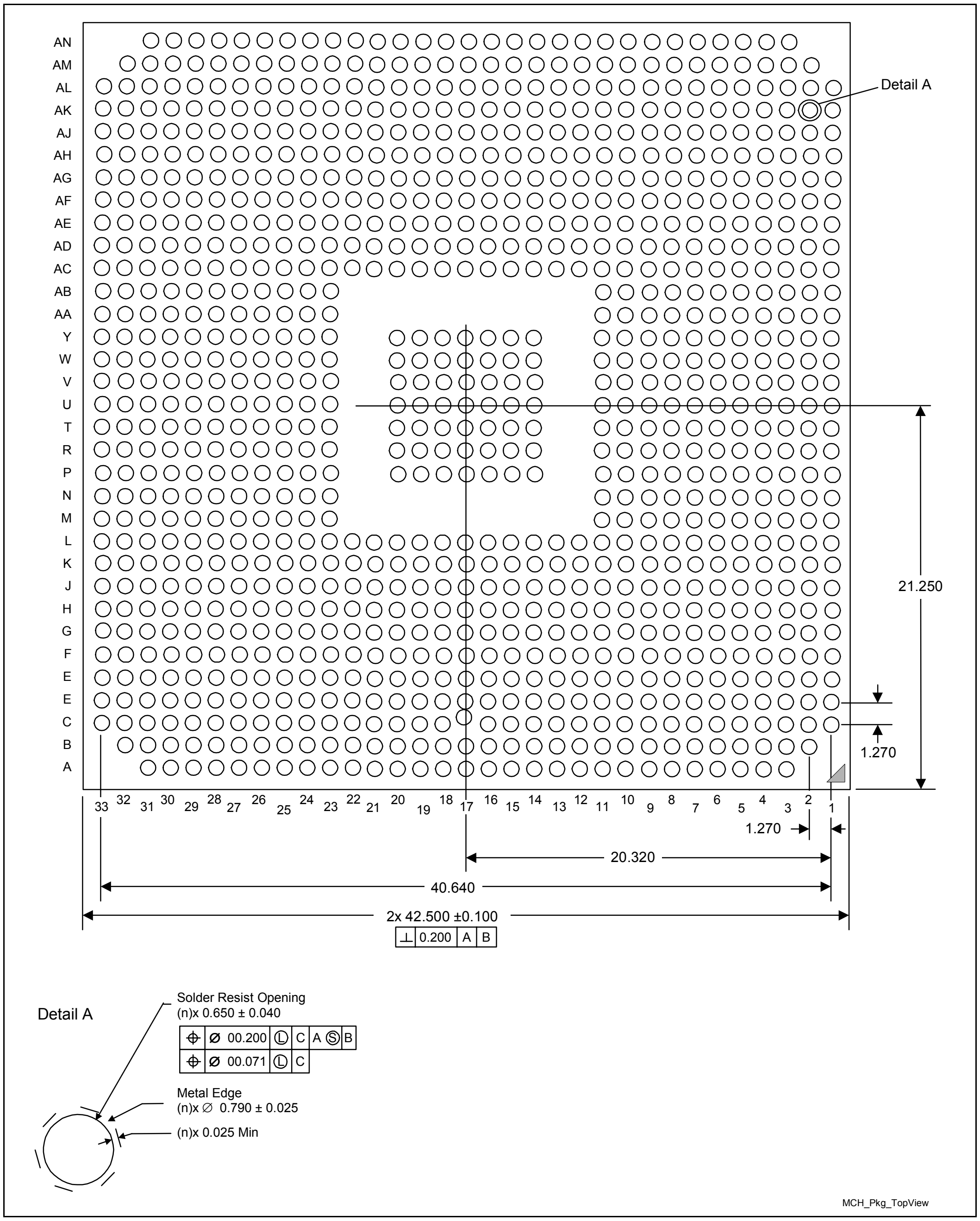
The E7205 chipset consists of three individual components: E7205 chipset MCH and 82801DB I/O Controller Hub 4 (ICH4). The MCH uses a 42.5 mm, 6-layer FC-BGA package shown in Figure 2 and Figure 3. For information on the ICH4 package, refer to the *Intel® 82801DB I/O Controller Hub 4 (ICH4) Datasheet*.

Figure 2. Intel® E7205 Chipset MCH Package Dimensions (Side View)



NOTES:
1. Primary datum –C– and seating plane are defined by the spherical crowns of the solder balls.
2. All dimensions and tolerances conform to ANSI Y14.5M–1982.

Figure 3. Intel® E7205 Chipset MCH Package Dimensions (Top View)



NOTES:
1. All dimensions are in millimeters.
2. All dimensions and tolerances conform to ANSI Y14.5M–1982.

3 Thermal Simulation

Intel provides thermal simulation models of the MCH and associated user's guides to aid system designers in simulating, analyzing, and optimizing their thermal solutions in an integrated system-level environment. The models are for use with the commercially available Computational Fluid Dynamics (CFD)-based thermal analysis tool "FLOTHERM*" (version 3.1 or higher) by Flomerics* Inc. Contact your Intel Field Sales representative to order the thermal models and user's guides.

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4 Thermal Specifications

4.1 Case Temperature and Thermal Design Power

See Table 1 for TDP specifications for the E7205 chipset MCH. FC-BGA packages do not have good heat transfer capability into the board and have minimal thermal capability without thermal solutions. Intel recommends that system designers plan for one heatsink when using the E7205 chipset.

4.2 Die Temperature

To ensure proper operation and reliability of the MCH, the die temperatures must be at or below the values specified in Table 1. System and/or component level thermal solutions are required to maintain die temperatures below the maximum temperature specification. Refer to Chapter 5 for guidelines on accurately measuring package die temperatures.

Table 1. MCH Thermal Specifications

Parameter	Maximum
T_{case}	102 °C
TDP	7.7 W

NOTE: T_{case} is defined as the maximum die temperature with the reference thermal solution attached.

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5 Thermal Metrology

The system designer must make temperature measurements to accurately determine the thermal performance of the system. Intel has established guidelines for proper techniques of measuring the E7205 chipset MCH die temperature. Section 5.1 provides guidelines on how to accurately measure the MCH die temperatures. Section 5.2 contains information on running an application program that will emulate anticipated maximum thermal design power. The flowchart in Figure 6 offers guidelines for thermal performance and evaluation.

5.1 Die Temperature Measurements

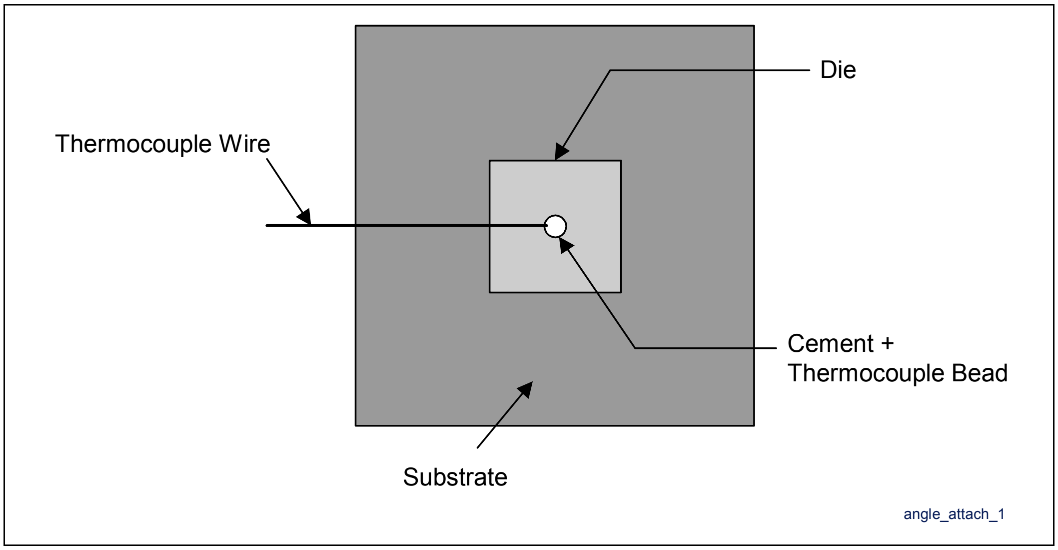
To ensure functionality and reliability, the T_{case} of the MCH must be maintained at or below the maximum temperatures specification as noted in Table 1. The surface temperature at the geometric center of the die corresponds to T_{case}. Measuring T_{case} requires special care to ensure an accurate temperature measurement.

Temperature differences between the temperature of a surface and the surrounding local ambient air can introduce errors in the measurements. The measurement errors could be due to a poor thermal contact between the thermocouple junction and the surface of the package, heat loss by radiation and/or convection, conduction through thermocouple leads, or contact between the thermocouple cement and the heatsink base (if a heatsink is used). To maximum measurement accuracy, only the 0° degree thermocouple attach approach is recommended for thermocouple attach.

5.1.1 0° Angle Attach Methodology

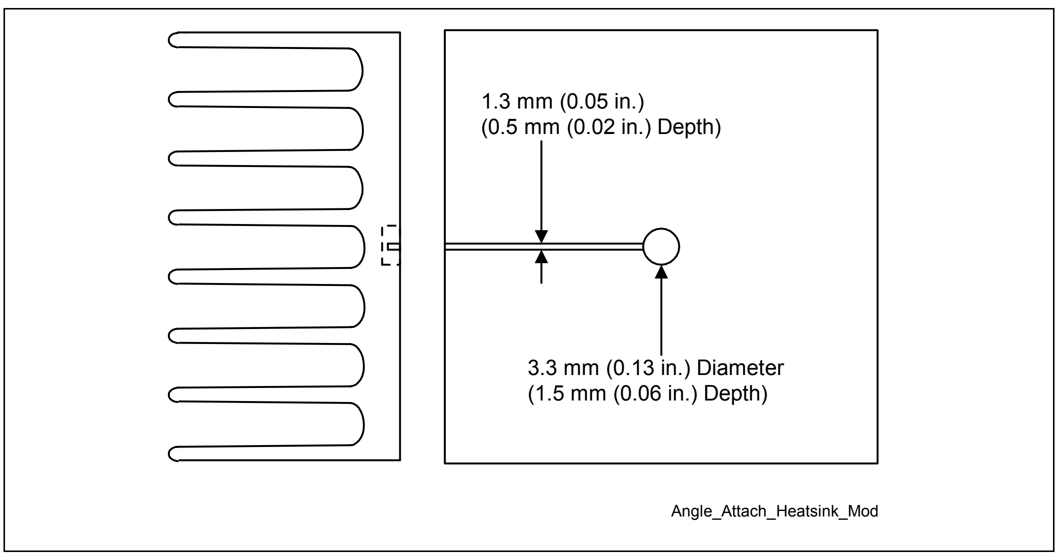
1. Mill a 3.3 mm (0.13 in.) diameter and 1.5mm (0.06 in.) deep hole centered on bottom of the heatsink base.
2. Mill a 1.3 mm (0.05 in.) wide and 0.5 mm (0.02 in.) deep slot, from the centered hole to one edge of the heatsink. The slot should be in the direction parallel to the heatsink fins (see Figure 5).
3. Attach thermal interface material (TIM) to the bottom of the heatsink base.
4. Cut out portions of the TIM to make room for the thermocouple wire and bead. The cutouts should match the slot and hole milled into the heatsink base.
5. Attach a 36 gauge or smaller calibrated K-type thermocouple bead or junction to the center of the top surface of the die using high thermal conductivity cement. During this step, make sure no contact is present between the thermocouple cement and the heatsink base because any contact will affect the thermocouple reading. **It is critical that the thermocouple bead makes contact with the die** (see Figure 4).
6. Attach heatsink assembly to the MCH, and route thermocouple wire out through the milled slot.

Figure 4. 0 Angle Attach Methodology (Top View)



NOTE: Not to scale.

Figure 5. 0° Angle Attach Heatsink Modifications



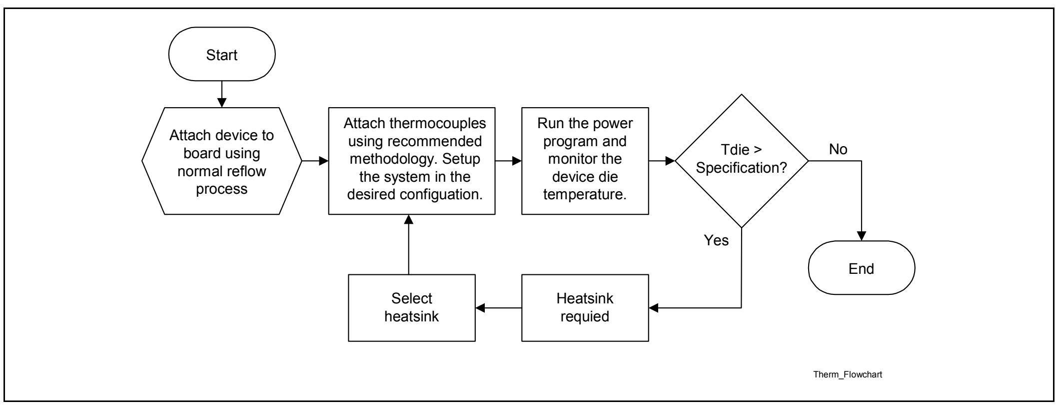
NOTE: Not to scale.

5.2 Power Simulation Software

The power simulation software is a utility designed to dissipate the thermal design power on an E7205 chipset MCH when used in conjunction with Intel Pentium processor with 512-KB L2 cache on 0.13 micron process. The combination of the Intel Pentium processor with 512-KB L2 cache on 0.13 micron process and the higher bandwidth capability of the E7205 chipset enable new levels of system performance. To assess the thermal performance of the chipset MCH thermal solution under "worst-case realistic application" conditions, Intel has developed a software utility that operates the chipset at near worst-case power dissipation.

The utility has been developed solely for testing customer thermal solutions at near the thermal design power. Figure 6 shows a decision flowchart for determining thermal solution needs. Real future applications may exceed the thermal design power limit for transient time periods. For power supply current requirements under these transient conditions, refer to each component's datasheet for the I_{CC} (Max Power Supply Current) specification. Contact your Intel Field Sales representative to obtain a copy of this software.

Figure 6. Thermal Solution Decision Flowchart



5.3 MCH Power Utility

The MCH power utility is designed to dissipate the TDP power value through the MCH when a system is populated with the memory listed in Table 2. These values have been validated for the configurations listed in Table 2 running the Processor System Bus (PSB) frequency at 533 MHz.

Table 2 Intel® E7205 Chipset MCH Thermal Design Power

TDP (Watts)	System Configuration
7.7 W*	533 MHz PSB, DDR-I 266, 133 MHz (4 slots of 512 MB unbuffered DIMMs)
7.6 W*	533 MHz PSB, DDR-I 266, 133 MHz (4 slots of 1 GB unbuffered DIMMs)

NOTE: Estimated to be within 10% for configurations running the processor system bus frequency at 533 MHz.

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6 Reference Thermal Solutions

Intel has developed a reference thermal solution designed to meet the cooling needs of the E7205 chipset MCH at worst-case conditions. This chapter describes the overall requirements for the reference thermal solution, including critical-to-function dimensions, operating environment, and validation criteria. Other chipset components may or may not need thermal solutions, depending on specific system local-ambient operating conditions. For the ICH4, refer to thermal specification in the *Intel® 82801DB I/O Controller Hub 4 (ICH4) Datasheet*.

6.1 Operating Environment

The reference thermal solution was designed assuming a maximum local-ambient temperature of 50°C. The minimum recommended airflow velocity at the heatsink is 200 lfm (linear feet per minute). The approaching airflow temperature is assumed to be equal to the local-ambient temperature. The thermal designer must carefully select the location to measure airflow to obtain an accurate estimate. These local-ambient conditions are based on a 35 °C external-ambient temperature at sea level. (External-ambient refers to the environment external to the system.)

6.2 Generic Thermal Solution Thermal Operation Point

The thermal operating point (TOP) is defined as the thermal resistance of the TIM at the design force of the clip and retention mechanism plus the thermal resistance of the heatsink (TRHS) at the specified airflow speed. The TRHS is given in the following equation:

$$TRHS = (Tcase - Tlocal\_ambient) / (\%\ TDP\ dissipated\ via\ heatsink)$$

Thermal simulation results show that as airflow increases upstream of the E7205 chipset generic thermal solution, the percentage of TDP that leaves via the top of the package increases (see Table 3).

Table 3. TDP Dissipation for Various Airflow Speeds

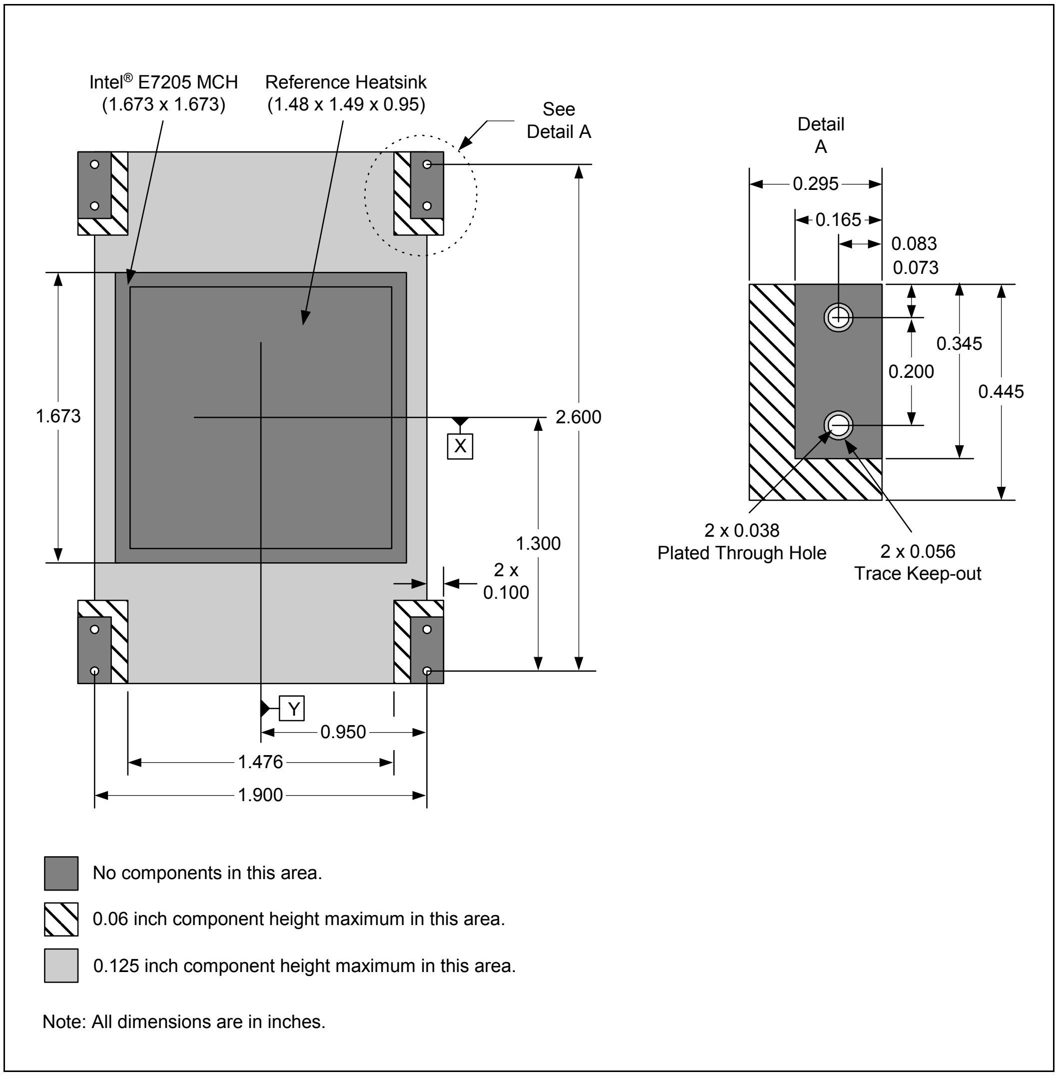
Upstream Airflow Speed (lfm)	Percentage of TDP Dissipated via Intel Thermal Solution	Percentage of TDP Dissipated via the 4-Layer JEDEC Board
50	70%	30%
100	75%	25%
150	77%	23%

6.3 Mechanical Design Envelope

Though each design may have unique mechanical volume and height restrictions or implementation requirements, the height, width, and depth constraints typically placed on the MCH thermal solution are shown in Figure 7.

When using heatsinks that extend beyond the MCH reference heatsink envelope shown in Figure 7, any motherboard components placed between the heatsink and motherboard cannot exceed 2.286 mm (0.090 in.) in height.

Figure 7. Reference Heatsink Volumetric Envelope for the MCH



NOTE: Not to scale.

6.4 Thermal Solution Assembly

The reference thermal solution is a passive extruded heatsink with thermal interfaces. It is attached using a clip frame assembly with each end hooked through an anchor soldered to the board. Figure 8 and Figure 9 shows the reference thermal solution assembly and associated components. Appendix A contains vendor information for each thermal solution component.

Figure 8. Heatsink Assembly (Heatsink, Clip Frame, Clip Lever)

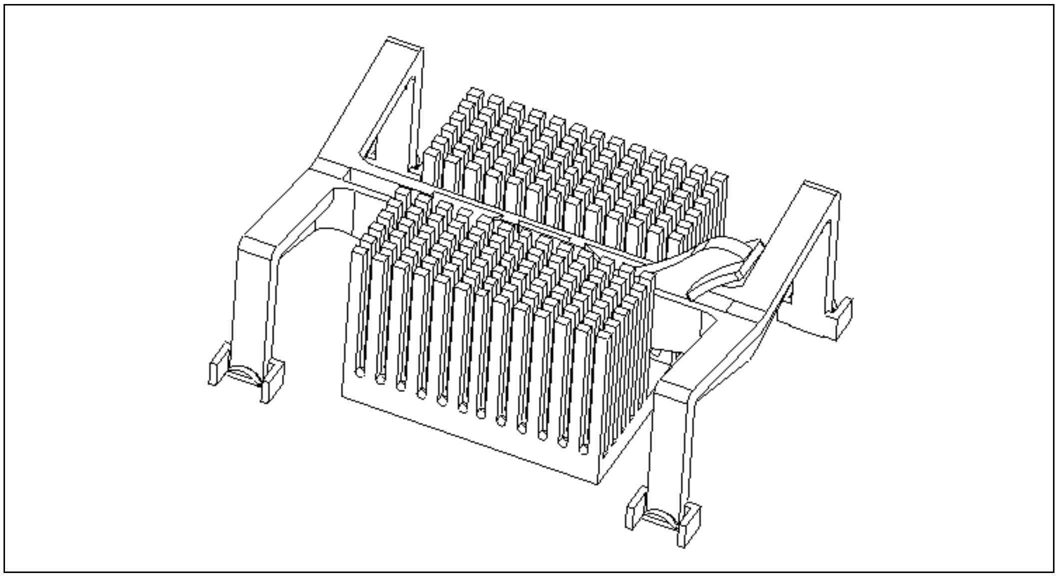
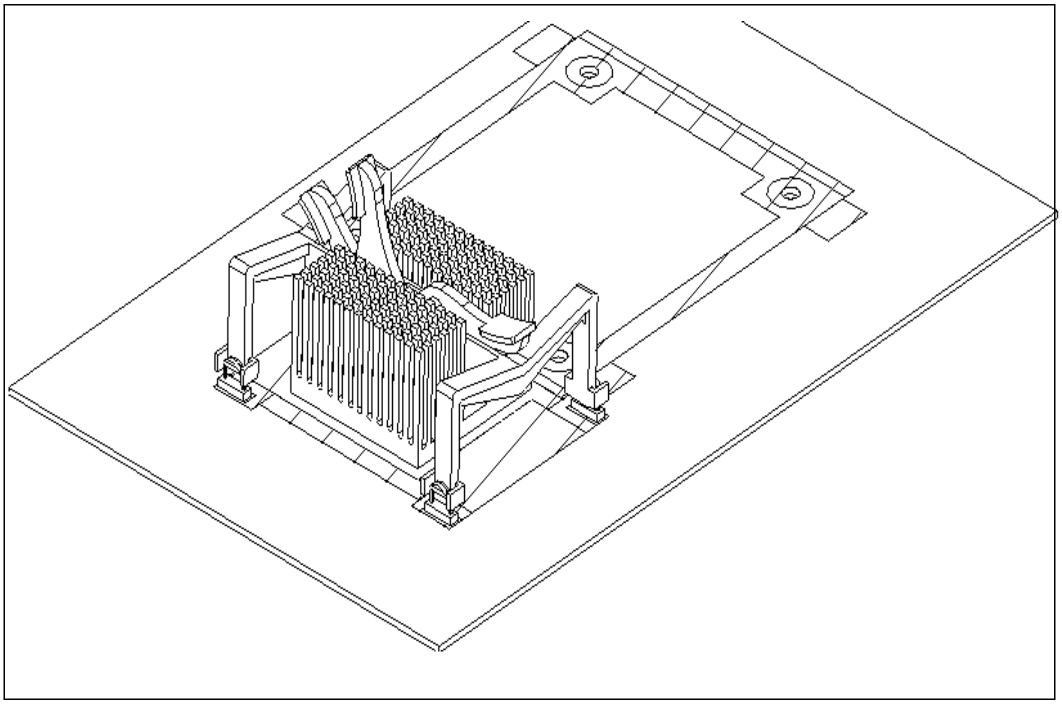


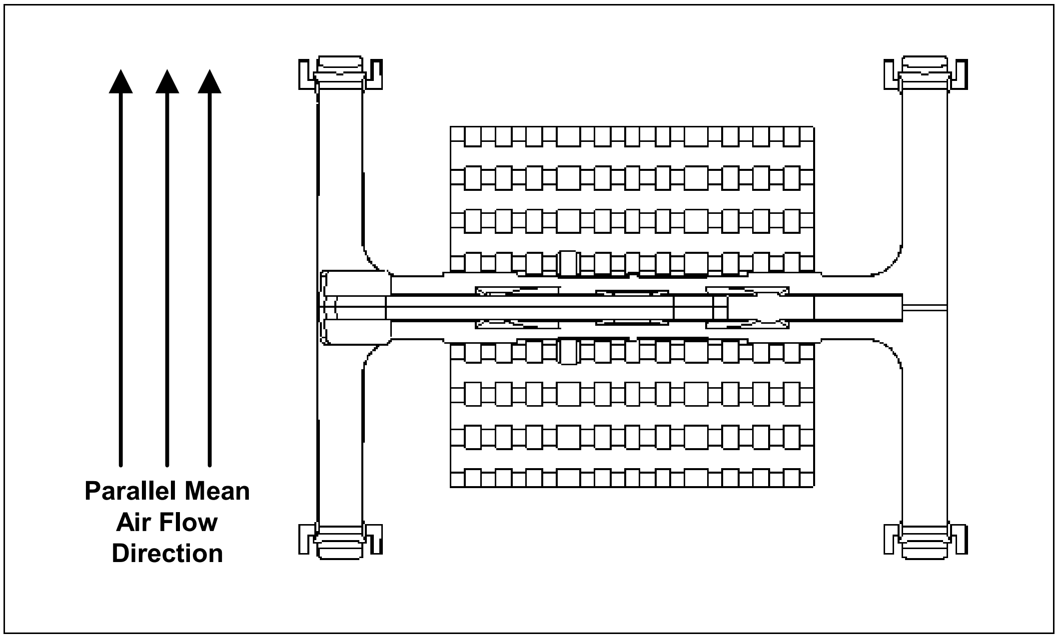
Figure 9. Heatsink Assembly Placement and Actuation



6.4.1 Heatsink Orientations

To enhance the efficiency of the reference thermal solution, it is important for the designer to orient the fins properly with respect to the mean airflow direction. Simulation and experimental evidence have shown that the MCH heatsink thermal performance is enhanced when the fins are aligned with the mean airflow direction (Figure 10). Aligning the heatsink 45° relative to the airflow is acceptable but delivers reduced thermal performance.

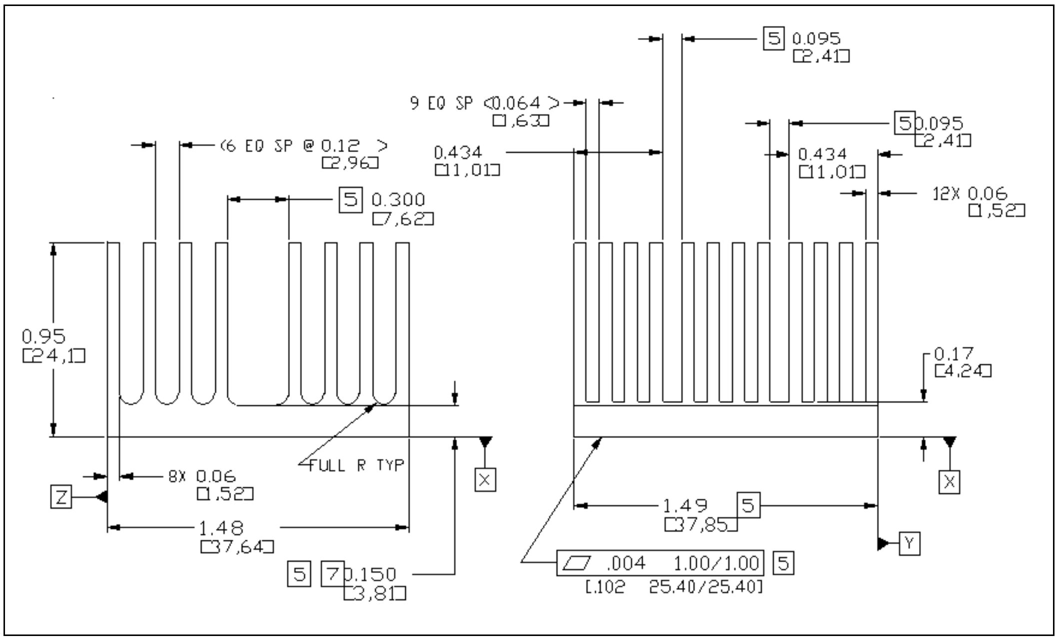
Figure 10. Preferred Heatsink Orientation



6.4.2 Extruded Heatsink Profiles

The reference thermal solution uses an extruded heatsink for cooling the MCH. Figure 11 shows the heatsink profile. This document does not provide tolerance information. Check with your heatsink supplier for specific tolerances. Appendix A lists suppliers for the extruded heatsink. Contact your heatsink supplier for information on alternate heatsinks.

Figure 11. Extruded Heatsink Profile

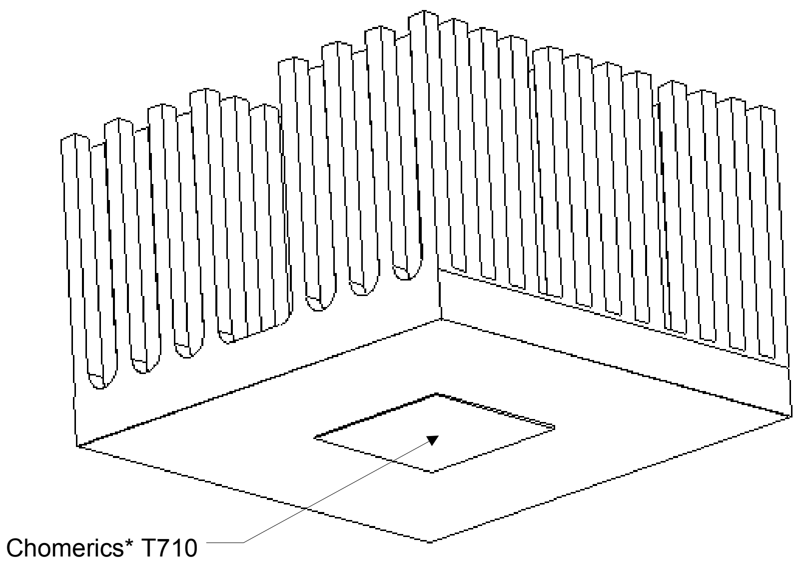


NOTE: Not to scale.

6.4.3 Thermal Interface Material

A thermal interface material provides improved conductivity between the die and heatsink. The reference thermal solution uses Chomerics* T-710, 0.127 mm (0.005 in.) thick, 12.7 mm x 12.7 mm (0.5 in. x 0.5 in.) square. Figure 12 shows the reference heatsink pre-applied with TIM.

Figure 12. Heatsink Pre-applied with TIM



6.4.3.1 The Effect of Pressure on TIM Performance

As mechanical pressure increases on the TIM, the thermal resistance of the TIM decreases. This phenomenon is due to the decrease of the bond line thickness (BLT). The effect of pressure on the thermal resistance of the Chomerics* T710 TIM is shown in Table 4. The heatsink clip (see Figure 8) provides enough pressure for the TIM to achieve a thermal conductivity of 0.9 W/mxK.

Table 4 Chromerics* T710 TIM Performance as a Function of Attach Pressure

Pressure (psi)	Thermal Resistance (°C*In^2)/W
5	0.37
10	0.3
20	0.21
50	0.17

Note: All measured at 50 °C.

6.4.4 Heatsink Clip

The heatsink is affixed to the die with a mechanism advantage clip. The clip consists of a clip frame that interfaces to the motherboard through four through-hole mount anchors and an integral lever (see Figure 9). The clip and lever serve three main purposes: to secure the heatsink in intimate contact with the die, to ensure a thermally good bond line between the heatsink and die, and to prevent damage at the package-to-motherboard solder joint during mechanical shock events. See Appendix A for the part number and supplier information.

6.4.4.1 Heatsink Retention

The heatsink must maintain close contact with the die for the life of the system. The generic clip retention mechanism design holds the heatsink to the die through a single point contact at the center of the heatsink. This ensures that the clip load is centered on the die, thus preventing heatsink tilt that may be caused by unbalanced loading (see Figure 13). The clip frame also restrains heatsink lateral motion through tabs located between the heatsink fins (see Figure 14).

Figure 13. MCH Clip Assembly

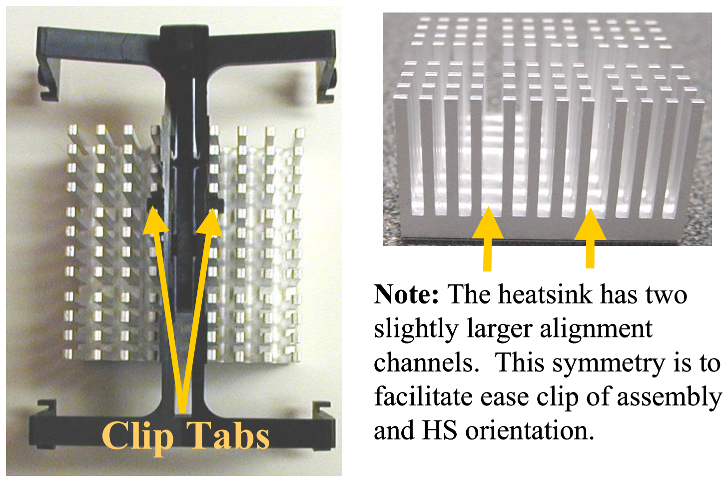
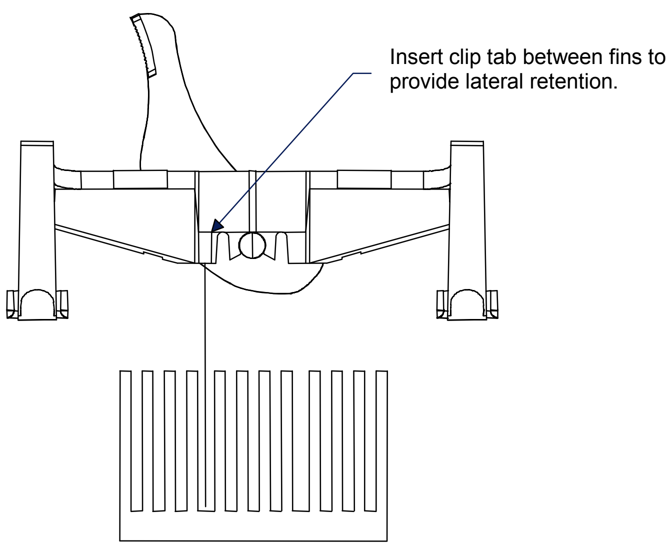


Figure 14. MCH Clip Lateral Retention Tab Feature



6.4.4.2 Thermal Bond Line

The thickness of the bond line between the heatsink and die is critical to thermal performance of the TIM. The bond line thickness is dependent on the pressure between the heatsink and the die. The clip retention mechanism is used to generate the pressure required to ensure thermal performance (see Table 4). The generic clip frame and lever design generates more than 50 psi pressure.

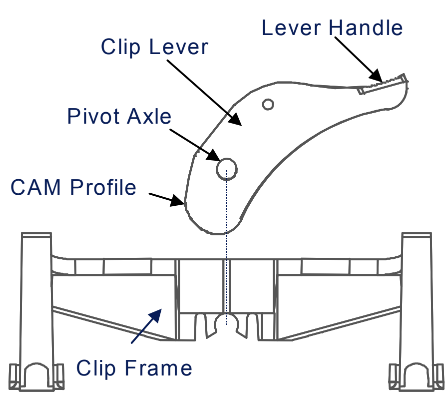
6.4.4.3 Solder Joint Protection

The solder joints between the package and the motherboard are susceptible to damage under mechanical shock conditions depending on the mass and proximity of the processor heatsink. Other elements (e.g., motherboard bending rigidity and the size and distribution of other mass components on the motherboard) can also affect solder joint susceptibility to damage.

The generic clip design uses mechanical preload on the package to protect the solder joint against damage under mechanical shock. The design features a rotating cam (see Figure 15) that generates substantial preload between the heatsink and package. The cam has a levered handle that provides a mechanical advantage during installation.

The preload serves to compress the solder ball array between the package and motherboard. The compression in the solder balls delays the onset of tensile load under critical shock conditions, and the magnitude of maximum tensile load is thereby reduced. In this manner, the critical solder balls are protected from tensile loading that may cause damage to the solder joint.

Figure 15. MCH Clip Frame and Lever



6.4.5 Clip Retention Anchors

For E7205 chipset-based platforms that have very limited board space, a clip retention anchor has been developed to minimize the impact of clip retention on the board. It is based on a standard three-pin jumper and is soldered to the board like any common through-hole header. A new anchor design is available with 45° bent leads to increase the anchor attach reliability over time. See Appendix A for the part number and supplier information.

6.4.6 Board Level Component Keep-out Dimensions

The locations of hole patterns and keep-out zones for the reference thermal solution are shown in Figure 7.

6.5 Reliability Guidelines

Each motherboard, heatsink and attach combination may vary the mechanical loading of the component. Based on the end user environment, the user should define the appropriate reliability test criteria and carefully evaluate the completed assembly prior to use in high volume. Some general recommendations are shown in Table 5.

Table 5. Reliability Guidelines

Test	Test Profile	Pass/Fail Criteria
Mechanical Shock	50 g, board level, 11 msec, 3 shocks/axis	Visual Check and Electrical Functional Test
Random Vibration	7.3 g, board level, 45 min/axis, 50 Hz to 2000 Hz	Visual Check and Electrical Functional Test
Temperature Life	85 °C, 2000 hours total, checkpoints at 168, 500, 1000, and 2000 hours	Visual Check
Thermal Cycling	-5 °C to +70 °C, 500 cycles	Visual Check
Humidity	85% relative humidity, 55 °C, 1000 hours	Visual Check

NOTES:

1. It is recommended that the above tests are performed on a sample size of at least 12 assemblies from 3 lots of material.
2. Additional Pass/Fail Criteria may be added at the discretion of the user.

Appendix A: Thermal Solution Component Suppliers

Table 6. Complete Thermal Solution Kits

Part	Intel Part Number	Supplier	Contact Information
MCH Enabling Assembly includes: • Heatsink • Thermal interface material • Clip frame • Clip level.	A67625-001	Foxconn (PHC029C02012)	Bob Hall 503-693-3509 x235 bhall@foxconn.com

Table 7. Extruded Heatsinks

Part	Intel Part Number	Supplier	Contact Information
Pin Fin Heatisnk (37.64 x 37.85 x 24.1 mm)	A54515-001	Foxconn	Bob Hall 503-693-3509x235 bhall@foxconn.com

Table 8. Interface Materials

Part	Intel Part Number	Supplier (Part Number)	Contact Information
Thermal Interface (T-710)	—	Chomerics (69-12-22315-T710)	Todd Sousa 360- 606-8171 tsousa@parker.com

Table 9. Attach Hardware

Part	Intel Part Number	Supplier	Contact Information
Heatsink Attach Clip Frame	A65066-001	Foxconn	Bob Hall 503-693-3509 x235 bhall@foxconn.com
Heasink Attach Clip Lever	A67031-001	Foxconn	Bob Hall 503-693-3509 x235 bhall@foxconn.com
Solder-Down Anchor	A13494-005	Foxconn (HB96030-DW)	Julia Jiang 408-919-6178 juliaj@foxconn.com

Note: The enabled components may not be currently available from all suppliers. Contact the supplier directly to verify time of component availability.

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Appendix B: Mechanical Drawings

This appendix contains the following drawings:

- Heatsink
- Heatsink Clip Frame
- Heatsink Clip Lever

Figure 16. MCH Heatsink

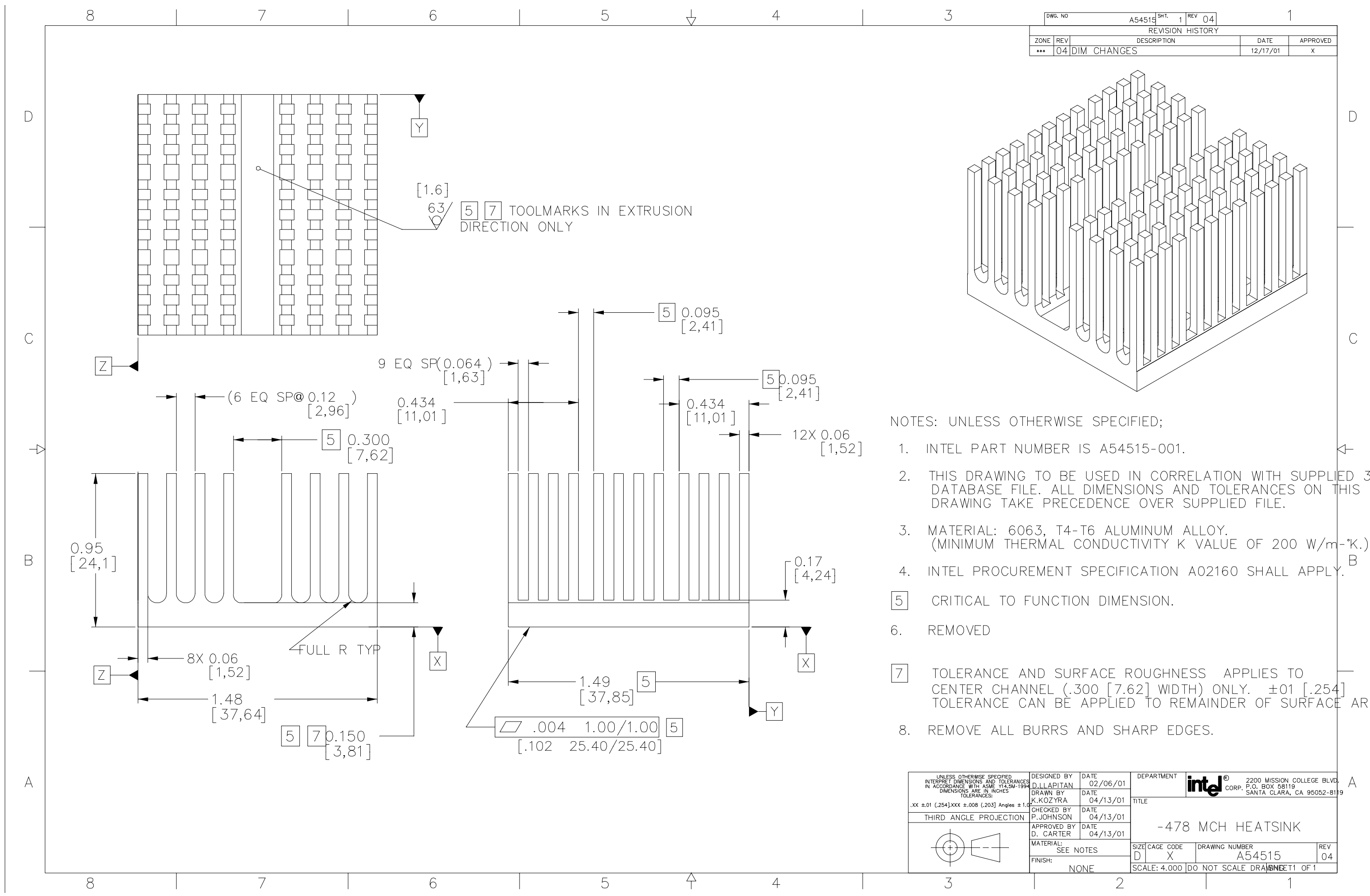

Figure 17. MCH Heatsink Clip Frame (Sheet 1 of 3)

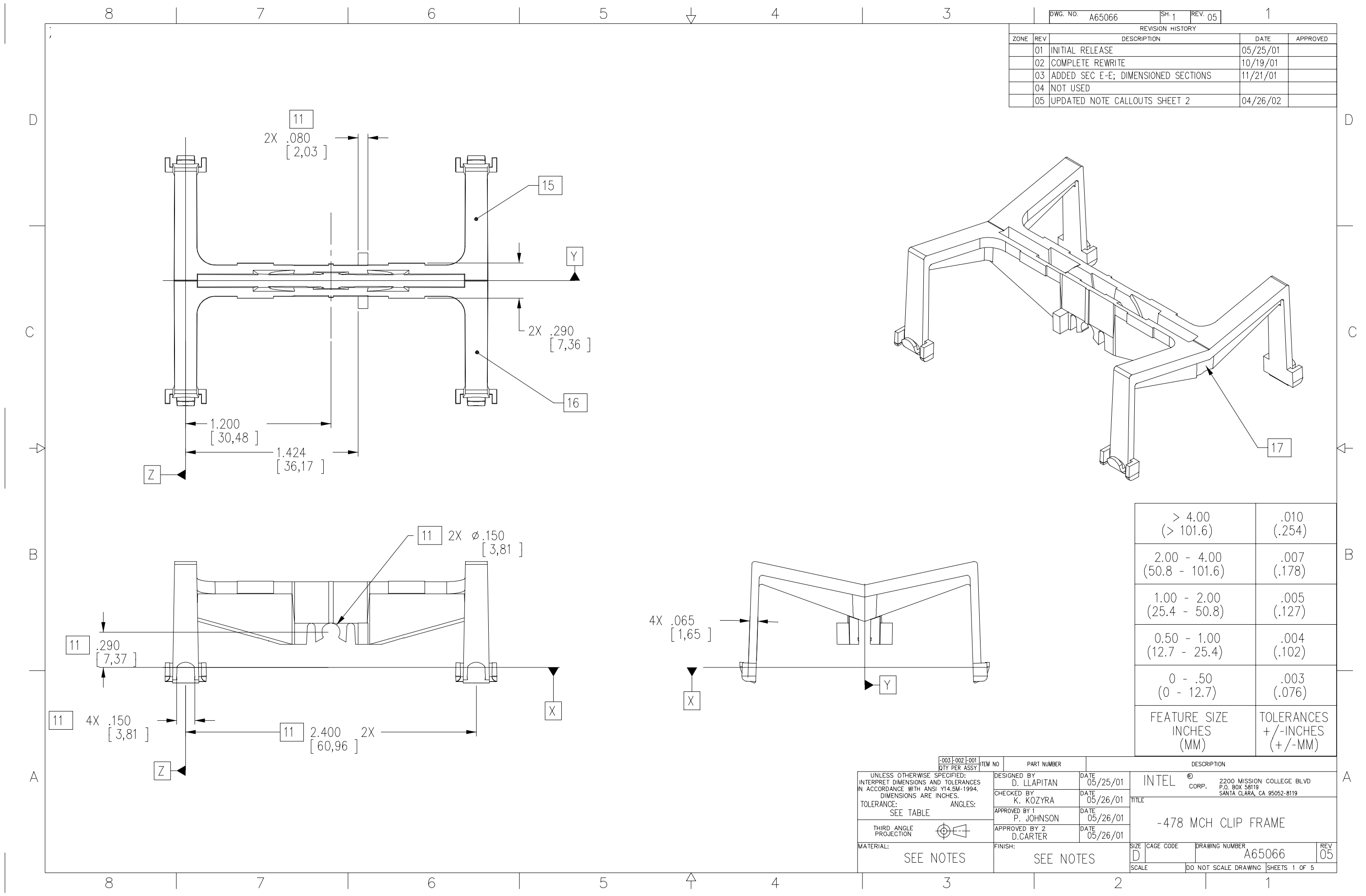

Figure 18. MCH Heatsink Clip Frame (Sheet 2 of 3)

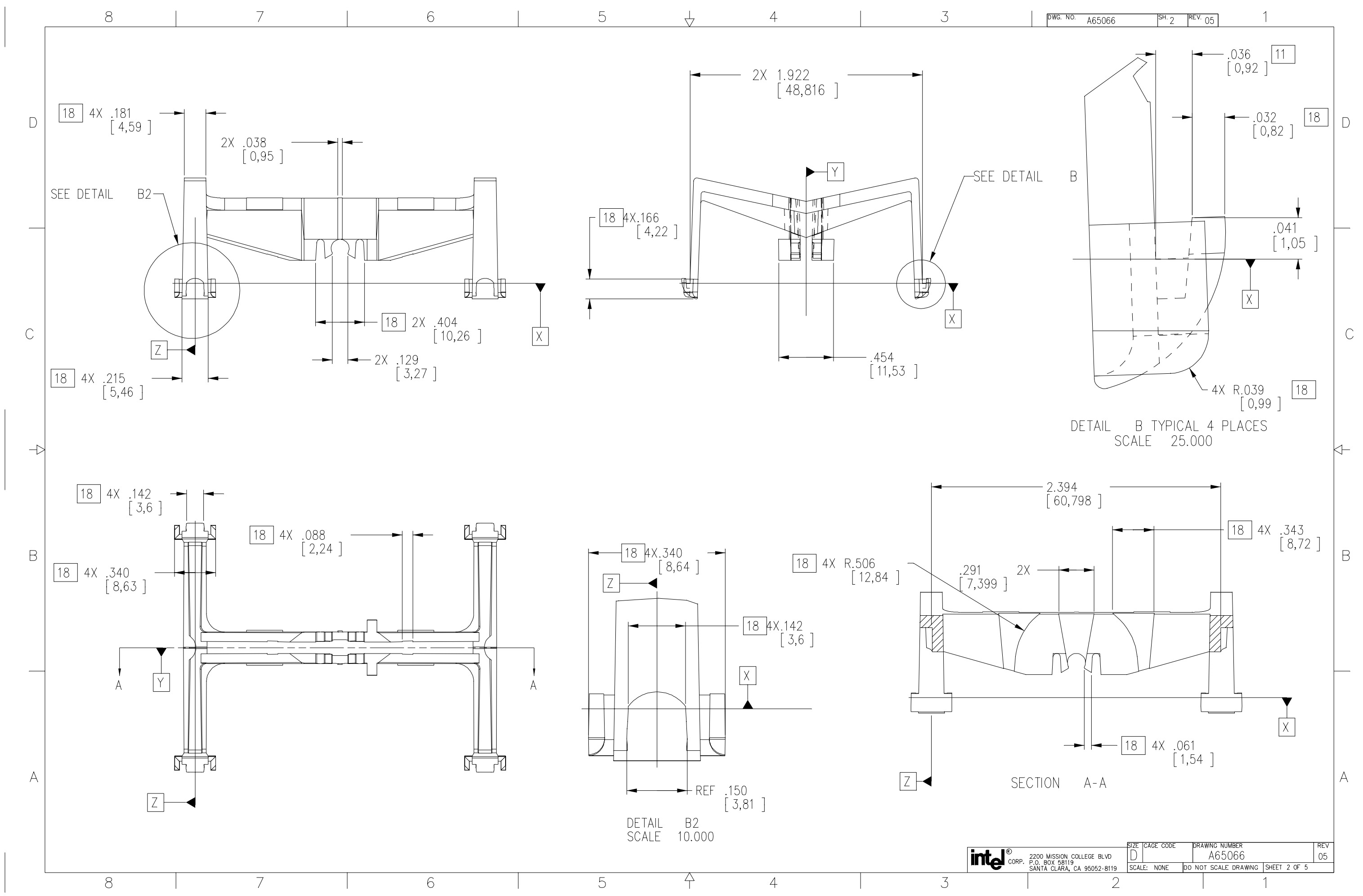

Figure 19. MCH Heatsink Clip Frame (Sheet 3 of 3)

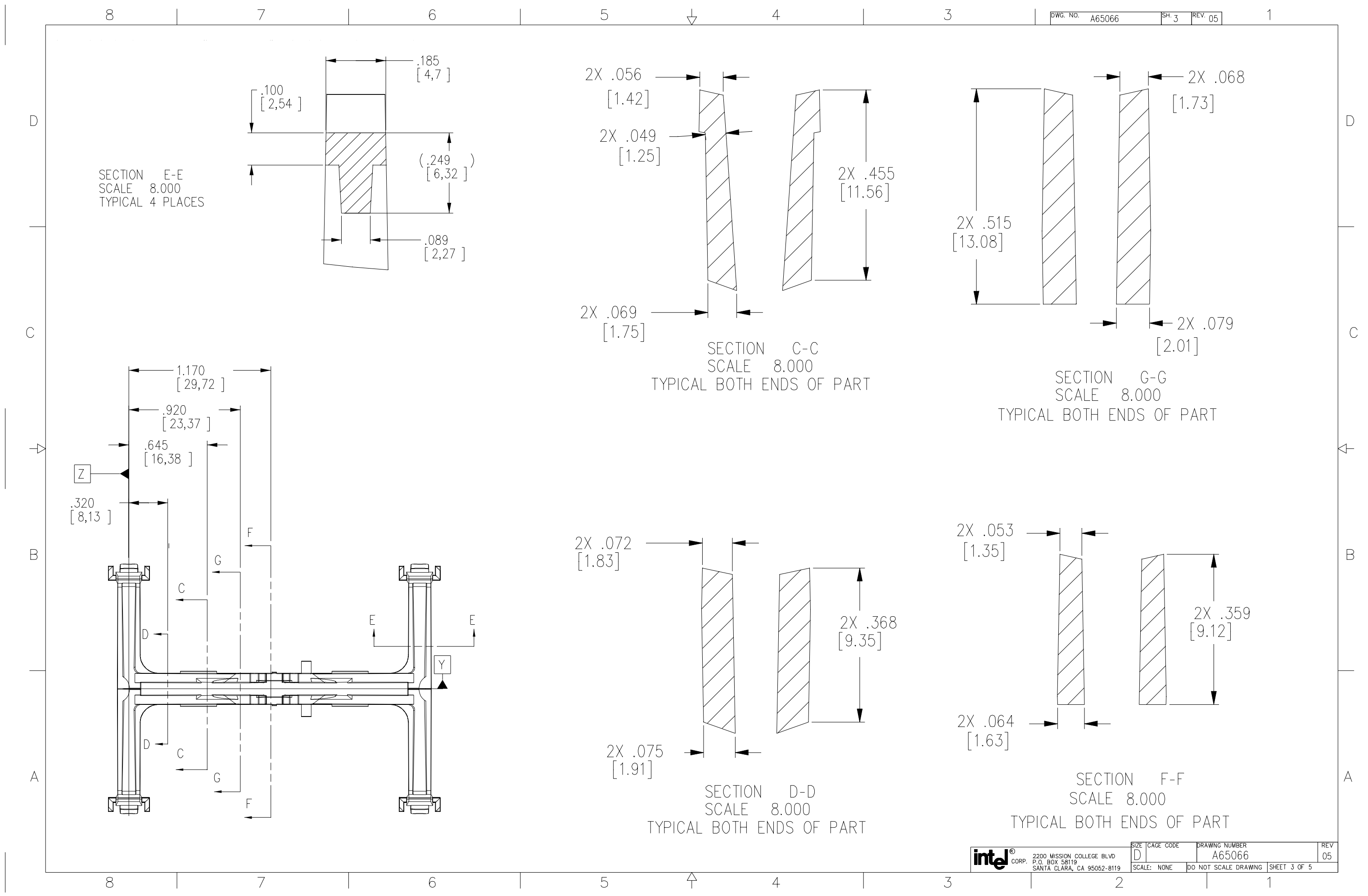

Figure 20. MCH Heatsink Clip Lever