# Intel® 852GME, Intel® 852GMV and Intel® 852PM Chipset Platforms

## Design Guide

***For Use with the Mobile Intel® Pentium® 4 Processor supporting Hyper-Threading Technology on 90-nm process technology, Mobile Intel® Pentium® 4 Processor, Intel® Celeron® Processor, and Intel® Celeron® D Processors on 90 nm Process and in the 478-pin Package***

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# Revision History

| Rev. | Document Number | Description | Date |
|---|---|---|---|
| -001 | 253026 | Initial Release | June 2003 |
| -002 | 253026 | Updates include:<br>Added information for 852GMV | February 2004 |
| -003 | 253026 | Updates include:<br>Added information for Mobile Intel Pentium 4 Processor supporting Hyper-Threading Technology on 90-nm process technology | May 2004 |
| -004 | 253026 | Updates include:<br>Added information for Intel Celeron D Processor on 90 nm process and in the 478-pin package | June 2004 |

# 1. Introduction

This design guide provides Intel design recommendations for the Intel® 852GME, Intel® 852GMV GMCH and the Intel® 852PM MCH chipset based systems. These design guidelines ensure maximum flexibility for board designers while reducing the risk of board related issues. The Intel 852GME, Intel 852GMV and Intel 852PM chipsets are pin compatible. Carefully follow the design information and debug recommendations in this document.

The Mobile Intel® Pentium® 4 processor, Mobile Intel® Pentium® 4 processor supporting Hyper-Threading Technology on 90-nm process technology, Intel® Celeron® processor, or the Intel® Celeron® D processor on 90 nm process and in the 478-pin package in combination with the 852GME, 852GMV or 852PM deliver high performance and professional mobile platform solution using internal and/or external graphics. Section 2 provides an overview of system features of supported processor and chipset combinations.

All recommendations will apply to all platforms unless specified. Any references to GMCH apply to all platforms unless otherwise specified. Any reference to Mobile Intel Pentium 4 processor apply to Mobile Intel Pentium 4 processor supporting Hyper-Threading Technology on 90-nm process technology unless specified. Any reference to the Intel® Celeron® processor applies to the Intel® Celeron® D processor on 90 nm process and in the 478-pin package unless specified.

## 1.1. Referenced Documents

| Document | Document No./Location |
|---|---|
| *Mobile Intel® Pentium® 4 Processor Datasheet* | http://developer.intel.com/ |
| *Mobile Intel® Pentium® 4 Processor supporting Hyper-Threading Technology on 90-nm process technology Datasheet* | http://developer.intel.com/ |
| *Intel® Celeron® Processor on .13 Micron Process Datasheet* | http://developer.intel.com/ |
| *Intel® Celeron® D Processor on 90 nm Process and in the 478-pin Package Datasheet* | http://developer.intel.com/ |
| *Intel® 852GME Chipset GMCH and Intel® 852PM Chipset MCH Datasheet* | http://developer.intel.com/ |
| *Intel® 852GME and Intel® 852PM Chipset GMCH Specification Update* | http://developer.intel.com/ |
| *Intel® 852GM/852GMV Chipset GMCH Datasheet* | http://developer.intel.com/ |
| *Intel® 852GM/852GMV Chipset GMCH Specification Update* | http://developer.intel.com/ |
| *Intel® I/O Controller Hub -Mobile(ICH4-M) Datasheet* | http://developer.intel.com/ |
| *Intel® I/O Controller Hub-Mobile (ICH4-M) Specification Update* | http://developer.intel.com/ |
| *Intel® DDR 200 JEDEC Spec Addendum Rev 0.9 or later* | http://developer.intel.com/ |
| *Application Note AP-728: ICH/ICH2/ICH2M/ICH4S/ICH4M Real Time Clock (RTC) Accuracy and Considerations Under Test Conditions* | http://developer.intel.com/ |
| *ITP700 Debug Port Design Guide* | http://developer.intel.com/ |
| *JEDEC Standard, JESD79, Double Data Rate (DDR) SDRAM Specification* | http://www.jedec.org/ |
| *PC2100 DDR SDRAM Unbuffered SO-DIMM Reference Design Specification* | http://www.jedec.org/ |

## 1.2. Conventions and Terminology

| Terminology | Definition |
|---|---|
| AC | Audio Codec |
| AGP | Accelerator Graphic Port |
| AMC | Audio/Modem Codec |
| Anti-Etch | Any plane-split, void or cutout in a VCC or GND plane is referred to as an anti-etch |
| BER | Bit Error Rate |
| CMC | Common Mode Choke |
| EMI | Electro Magnetic Interference |
| ESD | Electrostatic Discharge |
| FS | Full Speed – Refers to USB 1.1 full speed |
| FWH | Firmware Hub – A non-volatile memory device used to store the system BIOS. |
| FSB | Front Side Bus – processor to GMCH interface |
| GMCH | Graphics Memory Controller Hub |
| HS | High Speed – Refers to USB 2.0 |
| ICH4-M | I/O Controller Hub Fourth Generation – Mobile |
| LOM | LAN on Motherboard |
| LPC | Low Pin Count |
| LS | Low Speed – Refers to USB 1.0 low speed |
| MC | Modem Codec |
| MCH | Memory controller hub |
| PCM | Pulse Code Modulation |
| PLC | Platform LAN Connect |
| RTC | Real Time Clock |
| SMBus | System Management Bus – A two-wire interface through which various system components can communicate |
| SPD | Serial Presence Detect |
| S/PDIF | Sony*/Phillips* Digital Interface |
| STD | Suspend-To-Disk |
| STR | Suspend-To-Ram |
| TCO | Total Cost of Ownership |
| UBGA | Micro Ball Grid Array |
| USB | Universal Serial Bus |
| VRM | Voltage Regulator Module |

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# 2. System Overview

## 2.1. Intel 852GME Chipset Platform System Features

The 852GME chipset contains two core components: the Intel 852GME GMCH and the Intel ICH4-M. The GMCH integrates the following

400/533 MHz FSB controller

266/333 MHz DDR controller

DVO muxed AGP interface, integrated graphics controller provides 3D, 2D, and display capabilities while using a portion of system memory for graphics memory (UMA) to provide a cost effective, high performance graphics solution

High-speed Accelerated Hub Architecture interface for communication with the ICH4-M

The ICH4-M integrates the following:

Ultra ATA 100/66/33 controller

USB host controller that supports the USB 1.1 and USB 2.0 specification

LPC interface

FWH Flash BIOS interface controller

PCI interface controller

AC'97 digital controller and a hub interface for communication with the GMCH. The 852GME GMCH is a Graphics Memory Controller Hub (GMCH) designed for Mobile Intel Pentium 4 processor and Intel Celeron processor.

For further information about the 852GME platform features, refer to *the Intel® 852GME Chipset GMCH and Intel® 852PM Chipset MCH Datasheet* and the *Intel® 82801DBM I/O Controller Hub (ICH4-M) Datasheet.*

### 2.1.1. Host Interface

The Intel 852GME GMCH can utilize a single processor. It supports a FSB frequency of 400/533 MHz (100/133 MHz HCLK respectively) using scaleable FSB VCC.

#### 2.1.1.1. Mobile Intel Pentium 4 Processor supporting Hyper-Threading Technology on 90-nm process technology

Intel's Mobile Intel® Pentium® 4 processor supporting Hyper-Threading Technology on 90-nm process technology is a follow on to the Mobile Intel Pentium 4 processor in the 478-pin package with enhancements to the Intel® NetBurstTM microarchitecture. The processor utilizes Flip-Chip Pin Grid Array (FC-mPGA4) package technology, and plugs into a zero insertion force (ZIF) socket. The Mobile Intel Pentium 4 processor supporting Hyper-Threading Technology on 90-nm process technology, like

its predecessor, the Mobile Intel Pentium 4 processor in the 478-pin package, is based on the same Intel 32-bit microarchitecture and maintains the tradition of compatibility with IA-32 software.

The Mobile Intel Pentium 4 processor supporting Hyper-Threading Technology on 90-nm process technology supports Hyper-Threading Technology. Hyper-Threading Technology allows a single, physical processor to function as two logical processors. While some execution resources such as caches, execution units, and buses are shared, each logical processor has its own architecture state with its own set of general-purpose registers, control registers to provide increased system responsiveness in multitasking environments, and headroom for next generation multi threaded applications. Intel recommends enabling Hyper-Threading Technology with Microsoft Windows* XP Professional or Windows*XP Home, and disabling Hyper-Threading Technology via the BIOS for all previous versions of Windows operating systems. For more information on Hyper-Threading Technology, see www.intel.com/info/hyperthreading. Refer to Section 6.1 for Hyper-Threading Technology configuration details.

In addition to supporting all the existing Streaming SIMD Extensions 2 (SSE2), there are 13 new instructions, which further extend the capabilities of Intel processor technology. These new instructions are called Streaming SIMD Extensions 3 (SSE3).These new instructions enhance the performance of optimized applications for the digital home such as video, image processing and media compression technology. 3D graphics and other entertainment applications such as gaming will have the opportunity to take advantage of these new instructions as platforms with the Mobile Intel Pentium 4 processor supporting Hyper-Threading Technology on 90-nm process technology and SSE3 become available in the market place. The Mobile Intel Pentium 4 processor supporting Hyper-Threading Technology on 90-nm process technology's Intel NetBurst microarchitecture front side bus (FSB) utilizes a split-transaction, deferred reply protocol like the Mobile Pentium 4 processor. The Intel NetBurst microarchitecture front side bus uses Source-Synchronous Transfer (SST) of address and data to improve performance by transferring data four times per bus clock (4X data transfer rate, as in AGP 4X). Along with the 4X data bus, the address bus can deliver addresses two times per bus clock and is referred to as a "double-locked" or 2X address bus. Working together, the 4X data bus and 2X address bus provide a data bus bandwidth of up to 4.3 GB/s.

The processor will feature Enhanced Intel SpeedStep® technology, which will enable real-time dynamic switching between multiple voltages and operating frequency points. This results in optimal performance without compromising low power. The processor features the Auto Halt, Stop Grant, Deep Sleep, and Deeper Sleep low power states. The processor includes an address bus powerdown capability which removes power from the address and data pins when the FSB is not in use. This feature is always enabled on the processor.

Advanced transfer cache is a 1-MB, on-die level 2 (L2) cache

#### 2.1.1.2. Mobile Intel Pentium 4 Processor

The Mobile Intel Pentium 4 processor is based on the Intel NetBurst® micro-architecture. The Mobile Intel Pentium 4 processor utilizes a 478-pin, Micro Flip-Chip Pin Grid Array (Micro-FCPGA) package with Integrated Heat Spreader, and plugs into a surface-mount, Zero Insertion Force (ZIF) socket. The Mobile Intel Pentium 4 processor maintains full compatibility with IA-32 software.

The Mobile Intel Pentium 4 processor is designed for uni-processor based high-performance systems. Features of the processor include:

Hyper pipelined technology

533-MHz system bus quad-pumped bus running off a 133-MHz system clock making 4.3 GB/sec data transfer rates possible

The execution trace cache is a first level cache that stores approximately 12k decoded micro-operations, which removes the decoder from the main execution path.

Advanced transfer cache is a 512-kB, on-die level 2 (L2) cache

#### 2.1.1.3. Intel Celeron D Processor on 90 nm process and in the 478-pin package

The Intel® Celeron® D processor on 90 nm process and in the 478-pin package uses Flip-Chip Pin Grid Array 4 (FC-mPGA4) package technology, and plugs into a 478-pin surface mount, Zero Insertion Force (ZIF) socket, referred to as the mPGA478B socket. The Intel® Celeron® D processor on 90 nm process and in the 478-pin package is based on the same Intel 32-bit microarchitecture and maintains the tradition of compatibility with IA-32 software.

In addition to supporting all the existing Streaming SIMD Extensions 2 (SSE2), there are 13 new instructions that further extend the capabilities of Intel processor technology. These new instructions are called Steaming SIMD Extensions 3 (SSE3).

The Celeron D processor's Front Side Bus (FSB) uses a split-transaction, deferred reply protocol like the Intel® Pentium 4 processor. The FSB uses Source-Synchronous Transfer (SST) of address and data to improve performance by transferring data four times per bus clock (4X data transfer rate, as in AGP 4X). Along with the 4X data bus, the address bus can deliver addresses two times per bus clock and is referred to as a "double-clocked" or 2X address bus. Working together, the 4X data bus and 2X address bus provide a data bus bandwidth of up to 4.2 GB/s.

The processor includes an address bus powerdown capability that removes power from the address and data pins when the FSB is not in use. This feature is always enabled on the processor.

#### 2.1.1.4. Intel Celeron Processor

The Intel Celeron processor utilizes Flip-Chip Pin Grid Array (FC-PGA2) package technology, and plugs into a 478-pin surface mount, Zero Insertion Force (ZIF) socket, referred to as the mPGA478B socket. The Intel Celeron processor maintains the tradition of compatibility with IA-32 software.

The Intel Celeron processor is designed for uni-processor based value systems. Features of the processor include:

Hyper pipelined technology

400-MHz system bus quad-pumped bus running off a 100-MHz system clock making 3.2 GB/sec data transfer rates possible

The execution trace cache is a first level cache that stores approximately 12-k, decoded micro-operations, which removes the decoder from the main execution path.

### 2.1.2. Intel 852GME Graphics Memory Controller Hub (GMCH)

#### 2.1.2.1. Multiplexed AGP and Intel® DVO Interface

The 852GME GMCH multiplexes an AGP interface with two Intel DVOs. The DVO ports can each support a single channel DVO device. If both ports are active in single channel mode, they will have identical display timings and data. Alternatively the DVO ports can combine to support dual channel devices supporting higher resolutions and refresh rates. When an external AGP device is installed in the system, all internal graphics driver (IGD) functionality are disabled.

### 2.1.2.2. Accelerated Graphics Port (AGP) Interface

Supports AGP 2.0 data transfers

Supports a single AGP (1X/2X/4X) device (either via a connector or on the motherboard)

Only supports 1.5-V VDDQ for AGP electricals

PCI semantic (FRAME# initiated) accesses to DRAM are snooped

AGP semantic (PIPE# and SBA) traffic to DRAM is not snooped on the FSB and is therefore not coherent with the CPU caches

High priority access support

Delayed transaction support for AGP reads that cannot be serviced immediately

AGP Busy/Stop Protocol support

Support for D3 Hot and Cold Device states

AGP Clamping and Sense Amp control

### 2.1.2.3. Integrated System Memory DRAM Controller

Supports up to two double-sided SO-DIMMs (four rows populated) with unbuffered PC2100/PC2700 DDR-SDRAM (with or without ECC)

Supports 64 Mb, 128 Mb, 256 Mb, and 512 Mb technologies for x8 and x16 width devices

Up to 1 GB (with 256-Mb technology and two SO-DIMMs) of PC2100/2700 DDR (with ECC) and up to 2 GB (high density using 512-Mb technology)

Supports 266-MHz and 333-MHz DDR devices

64-bit data interface (72-bit with ECC)

Supports up to 16 simultaneous open pages

Support for SO-DIMM Serial Presence Detect (SPD) scheme via SMBus interface STR power management support via self refresh mode using CKE

### 2.1.2.4. Internal Graphics Controller

Graphics Core Frequency
- Display / Render frequency up to 266 MHz

3D Graphics Engine
- 3D Setup and Render Engine
- Zone Rendering
- High quality performance Texture Engine

Analog Display Support
- 350-MHz integrated 24-bit RAMDAC
- Hardware color cursor support
- Accompanying I2C and DDC channels provided through multiplexed interface
- Dual independent pipe for dual independent display
- Simultaneous display: same images and native display timings on each display device

Digital Video Out Port (DVOB & DVOC) support

DVOB & DVOC with 165-MHz dot clock support for each 12-bit interface
Compliant with DVI Specification 1.5

Dedicated LFP (local flat panel) support
Single or dual channel LVDS panel support up to UXGA panel resolution with frequency range from 25 MHz to 112 MHz per channel
SSC support of 0.5%, 1.0%, and 2.5% center and down spread with external SSC clock
Supports data format of 18 bpp
LCD panel power sequencing compliant with SPWG timing specification
Compliant with ANSI/TIA/EIA –644-1995 spec
Integrated PWM interface for LCD backlight inverter control
Bi-linear Panel fitting

### 2.1.3. Package/Power

732-pin Micro-FCBGA (37.5 mm x 37.5 mm)

VTTLF, VTTHF (1.05 V)

VCC, VCCASM, VCCHL, VCCAHPLL, VCCAGPLL, VCCADPLLA, VCCADPLLB (1.5 V)

VCCADAC, VCCDVO, VCCDLVDS, VCCALVDS, (1.5 V)

VCCSM, VCCQSM, VCCTXLVDS (2.5 V)

VCCGPIO (3.3 V)

### 2.1.4. Intel 82801DBM I/O Controller Hub 4-Mobile (ICH4-M)

Upstream Accelerated Hub Architecture interface for access to the GMCH

PCI 2.2 interface (6 PCI Request/Grant Pairs)

Bus Master IDE controller (supports Ultra ATA 100/66/33)

USB 1.1 and USB 2.0 Host Controllers

I/O APIC

SMBus 2.0 Controller

FWH Interface

LPC Interface

AC'97 2.2 / 2.3 Interface

Alert-On-LAN*

IRQ Controller

Package/Power
421-pin, BGA package (31 mm x 31 mm)
VCC1_5 (1.5 V main logic voltage), VCC3_3 (3.3 V main I/O voltage)
VCCSUS1_5 (1.5 V resume logic voltage), VCCSUS3_3 (3.3 V resume I/O voltage)
VCCLAN1_5 (1.5 V LAN logic voltage), VCCLAN3_3 (3.3 V LAN I/O voltage)
V5REF (5 V) , V5REF_SUS (5 V)
VCCRTC (2.0V – 3.3V)

VCCHI (1.5 V)

### 2.1.5. Firmware Hub (FWH)

An integrated hardware Random Number Generator (RNG)

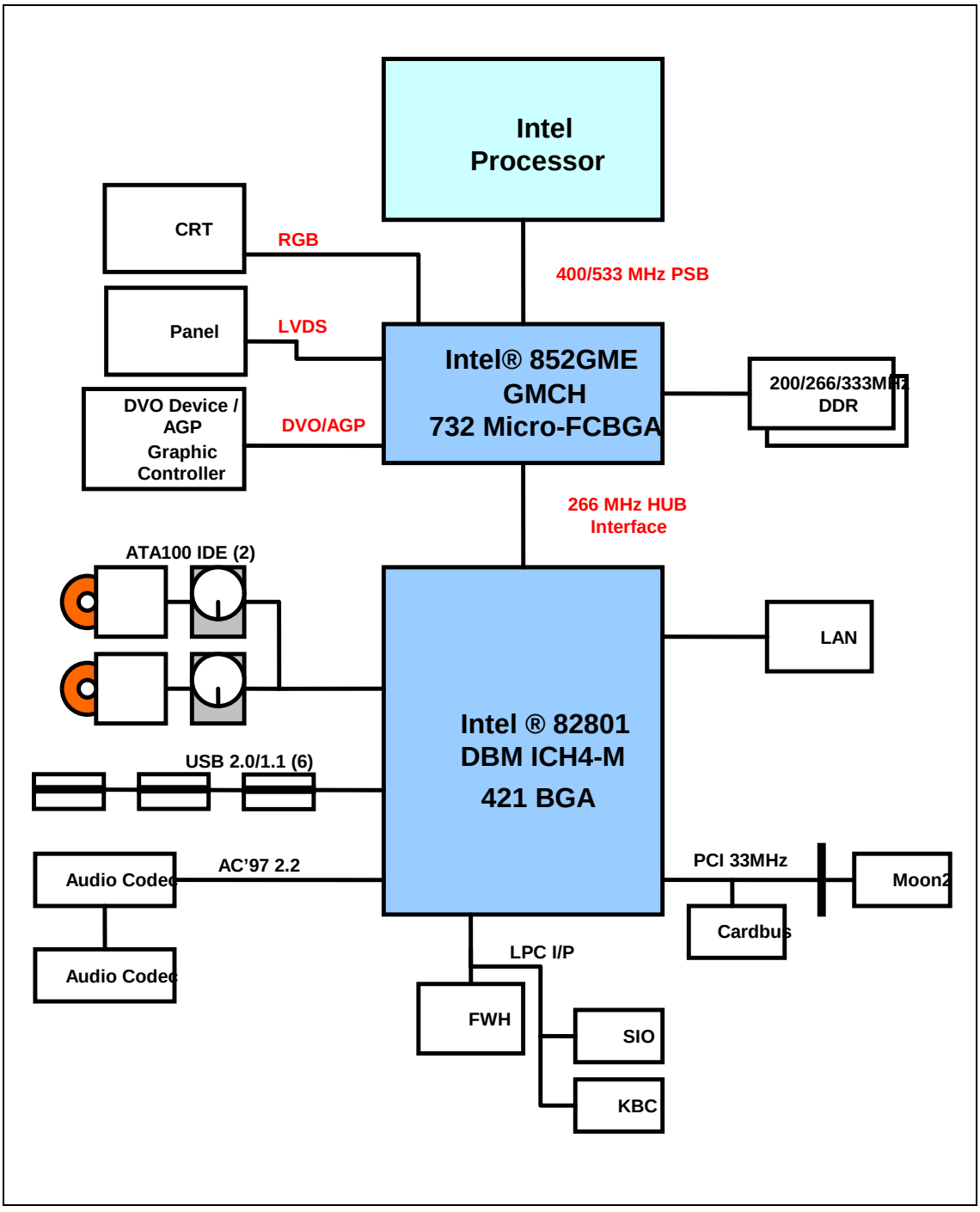
Register-based locking

Hardware-based locking

5 GPIs

Package/Power
- 32-pin TSOP/PLCC
- 3.3-V core and 3.3 V/12 V for fast programming

**Figure 1. Intel 852GME GMCH System Block Diagram**



## 2.2. Intel 852PM Chipset Platform System Features

The 852PM chipset contains two core components: the Intel 852PM GMCH and the Intel ICH4-M. The MCH integrates following:

533 MHz FSB controller

266/333 MHz DDR controller

DVO muxed AGP interface

High-speed Accelerated Hub Architecture interface for communication with the ICH4-M

The ICH4-M integrates the following:

Ultra ATA 100/66/33 controller

USB host controller that supports the USB 1.1 and USB 2.0 specification

LPC interface

FWH Flash BIOS interface controller

PCI interface controller

AC'97 digital controller and a hub interface for communication with the GMCH. The 852PM MCH is a Memory Controller Hub (MCH) designed for Mobile Intel Pentium 4 processor.

For further information about the 852PM platform features, reference *the Intel® 852GME Chipset GMCH and Intel® 852PM Chipset MCH Datasheet and the Intel® 82801DBM I/O Controller Hub (ICH4-M) Datasheet.*

### 2.2.1. Host Interface

The 852PM MCH can utilize a single processor. It supports a FSB frequency of 400/533 MHz (100/133 MHz HCLK respectively) using scaleable FSB VCC.

#### 2.2.1.1. Mobile Intel Pentium 4 Processor

Please refer to Section 2.1.1.1 and Section 2.1.1.2

#### 2.2.1.2. Intel Celeron Processor

Please refer to Section2.1.1.3 and Section 2.1.1.4.

### 2.2.2. 852PM Memory Controller Hub (MCH)

#### 2.2.2.1. Accelerated Graphics Port (AGP) Interface

Supports AGP 2.0 data transfers

Supports a single AGP (1X/2X/4X) device (either via a connector or on the motherboard)

Only supports 1.5-V VDDQ for AGP electrical

PCI semantic (FRAME# initiated) accesses to DRAM are snooped

AGP semantic (PIPE# and SBA) traffic to DRAM is not snooped on the FSB and is therefore not coherent with the CPU caches

High priority access support

Delayed transaction support for AGP reads that cannot be serviced immediately

AGP Busy/Stop Protocol support

Support for D3 Hot and Cold Device states

AGP Clamping and Sense Amp control

#### 2.2.2.2. Integrated System Memory DRAM Controller

Supports up to two double-sided SO-DIMMs (4 rows populated) with unbuffered PC2100/PC2700 DDR-SDRAM (with or without ECC)

Supports 64 Mb, 128 Mb, 256 Mb, and 512 Mb technologies for x8 and x16 width devices

Up to 1 GB (with 256-Mb technology and two SO-DIMMs) of PC2100/2700 DDR (with ECC) and up to 2 GB (high density using 512-Mb technology)

Supports 266-MHz and 333-MHz DDR devices

64-bit data interface (72-bit with ECC)

Supports up to 16 simultaneous open pages

Support for SO-DIMM Serial Presence Detect (SPD) scheme via SMBus interface STR power management support via self refresh mode using CKE

### 2.2.3. Package/Power

732-pin Micro-FCBGA (37.5 mm x 37.5 mm)

VTTLF, VTTHF (1.05 V)

VCC, VCCASM, VCCHL, VCCAHPLL, VCCAGPLL, VCCADPLLA, VCCADPLLB (1.5 V)

VCCADAC, VCCDVO, VCCDLVDS, VCCALVDS, (1.5 V)

VCCSM, VCCQSM, VCCTXLVDS (2.5 V)

VCCGPIO (3.3 V)

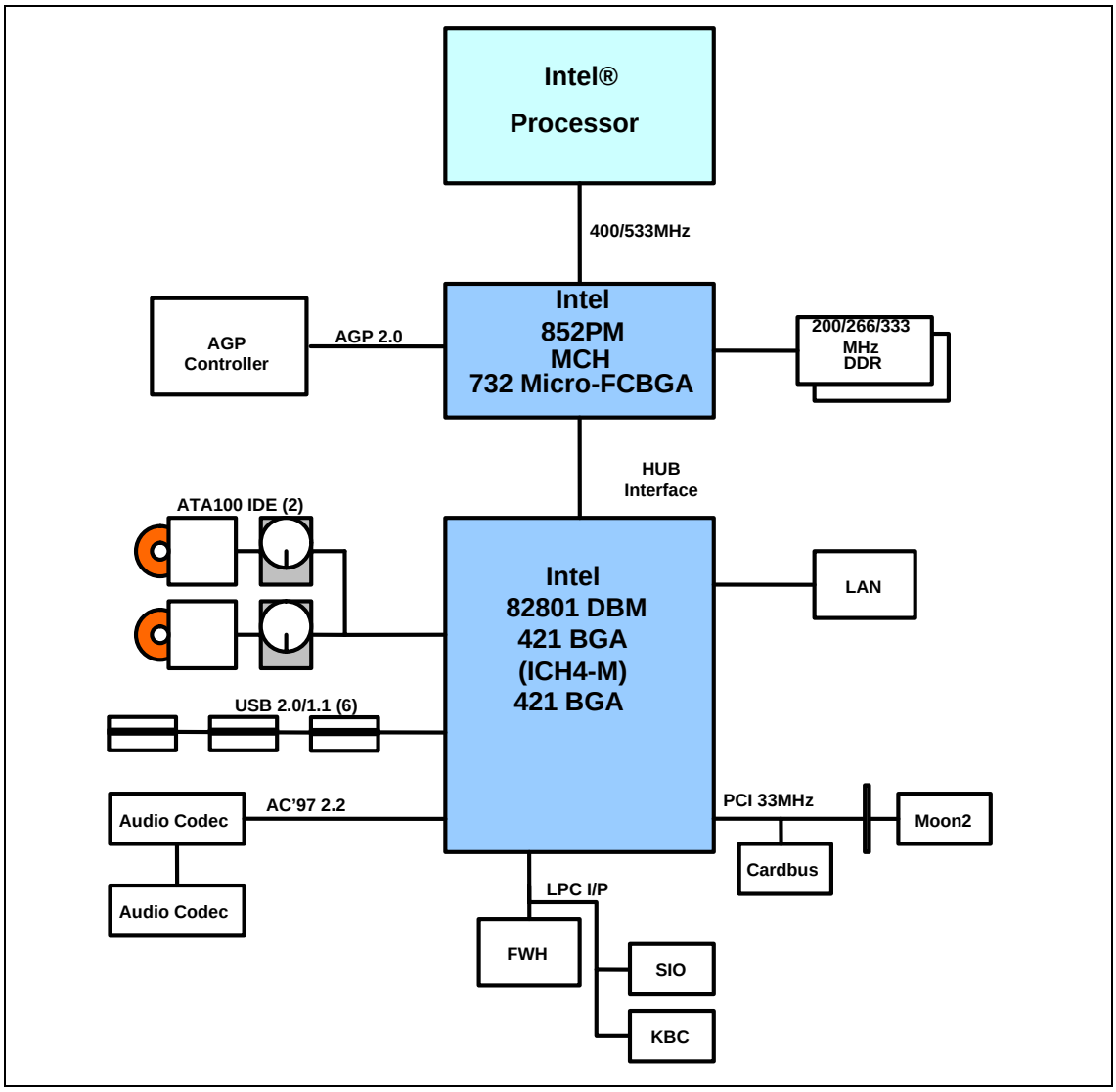
### 2.2.4. Intel 82801DBM I/O Controller Hub 4-Mobile (ICH4-M)

Please refer to Section 2.1.4.

### 2.2.5. Firmware Hub (FWH)

Please refer to Section 2.1.5.

**Figure 2. Intel 852PM Chipset System Block Diagram**



## 2.3. Intel 852GMV Chipset Platform System Features

The 852GMV chipset contains two core components: the Intel 852GMV GMCH and the Intel ICH4-M. The GMCH integrates the following

400/533 MHz FSB controller

200/266 MHz DDR controller

Integrated graphics controller provides 3D, 2D, and display capabilities while using a portion of system memory for graphics memory (UMA) to provide a cost effective, high performance graphics solution

High-speed Accelerated Hub Architecture interface for communication with the ICH4-M

The ICH4-M integrates the following:

Ultra ATA 100/66/33 controller

USB host controller that supports the USB 1.1 and USB 2.0 specification

LPC interface

FWH Flash BIOS interface controller

PCI interface controller

AC'97 digital controller and a hub interface for communication with the GMCH. The 852GME GMCH is a Graphics Memory Controller Hub (GMCH) designed for Mobile Intel Pentium 4 processor, Intel Celeron processor and Intel Celeron D processor on 90 nm process and in the 478-pin package..

For further information about the 852GMV platform features, refer to *the Intel® 852GM/GMV Chipset GMCH Datasheet* and the *Intel® 82801DBM I/O Controller Hub (ICH4-M) Datasheet.*

### 2.3.1. Host Interface

The Intel 852GMV GMCH can utilize a single processor. It supports a FSB frequency of 400/533 MHz (100/133 MHz HCLK respectively) using scaleable FSB VCC.

#### 2.3.1.1. Intel Celeron Processor

Please refer to Section2.1.1.3 and Section 2.1.1.4.

### 2.3.2. Intel 852GMV Graphics Memory Controller Hub (GMCH)

#### 2.3.2.1. Multiplexed AGP and Intel® DVO Interface

The 852GME GMCH multiplexes an AGP interface with two Intel DVOs. The DVO ports can each support a single channel DVO device. If both ports are active in single channel mode, they will have identical display timings and data. Alternatively the DVO ports can combine to support dual channel devices supporting higher resolutions and refresh rates.

#### 2.3.2.2. Integrated System Memory DRAM Controller

Supports up to two double-sided SO-DIMMs (four rows populated) with unbuffered PC2100 DDR-SDRAM (with or without ECC)

Supports 64 Mb, 128 Mb, 256 Mb, and 512 Mb technologies for x8 and x16 width devices

Up to 1 GB (with 256-Mb technology and two SO-DIMMs) of PC2100 DDR (with ECC) and up to 2 GB (high density using 512-Mb technology)

Supports 200-MHz and 266-MHz DDR devices

64-bit data interface (72-bit with ECC)

Supports up to 16 simultaneous open pages

Support for SO-DIMM Serial Presence Detect (SPD) scheme via SMBus interface STR power management support via self refresh mode using CKE

#### 2.3.2.3. Internal Graphics Controller

Graphics Core Frequency
- Display / Render frequency up to 133 MHz

3D Graphics Engine
- 3D Setup and Render Engine
- Zone Rendering
- High quality performance Texture Engine

Analog Display Support
- 350-MHz integrated 24-bit RAMDAC
- Hardware color cursor support
- Accompanying I2C and DDC channels provided through multiplexed interface
- Dual independent pipe for dual independent display
- Simultaneous display: same images and native display timings on each display device

Digital Video Out Port (DVOB & DVOC) support
- DVOB & DVOC with 165-MHz dot clock support for each 12-bit interface
- Compliant with DVI Specification 1.5

Dedicated LFP (local flat panel) support
- Single or dual channel LVDS panel support up to UXGA panel resolution with frequency range from 25 MHz to 112 MHz per channel
- SSC support of 0.5%, 1.0%, and 2.5% center and down spread with external SSC clock
- Supports data format of 18 bpp
- LCD panel power sequencing compliant with SPWG timing specification
- Compliant with ANSI/TIA/EIA –644-1995 spec
- Integrated PWM interface for LCD backlight inverter control
- Bi-linear Panel fitting

### 2.3.3. Package/Power

732-pin Micro-FCBGA (37.5 mm x 37.5 mm)

VTTLF, VTTHF (1.05 V)

VCC, VCCASM, VCCHL, VCCAHPLL, VCCAGPLL, VCCADPLLA, VCCADPLLB (1.5 V)

VCCADAC, VCCDVO, VCCDLVDS, VCCALVDS, (1.5 V)

VCCSM, VCCQSM, VCCTXLVDS (2.5 V)

VCCGPIO (3.3 V)

### 2.3.4. Intel 82801DBM I/O Controller Hub 4-Mobile (ICH4-M)

Upstream Accelerated Hub Architecture interface for access to the GMCH

PCI 2.2 interface (6 PCI Request/Grant Pairs)

Bus Master IDE controller (supports Ultra ATA 100/66/33)

USB 1.1 and USB 2.0 Host Controllers

I/O APIC

SMBus 2.0 Controller

FWH Interface

LPC Interface

AC'97 2.2 / 2.3 Interface

Alert-On-LAN*

IRQ Controller

Package/Power

- 421-pin, BGA package (31 mm x 31 mm)
- VCC1_5 (1.5 V main logic voltage), VCC3_3 (3.3 V main I/O voltage)
- VCCSUS1_5 (1.5 V resume logic voltage), VCCSUS3_3 (3.3 V resume I/O voltage)
- VCCLAN1_5 (1.5 V LAN logic voltage), VCCLAN3_3 (3.3 V LAN I/O voltage)
- V5REF (5 V) , V5REF_SUS (5 V)
- VCCRTC (2.0V – 3.3V)
- VCCHI (1.5 V)

### 2.3.5. Firmware Hub (FWH)

An integrated hardware Random Number Generator (RNG)

Register-based locking

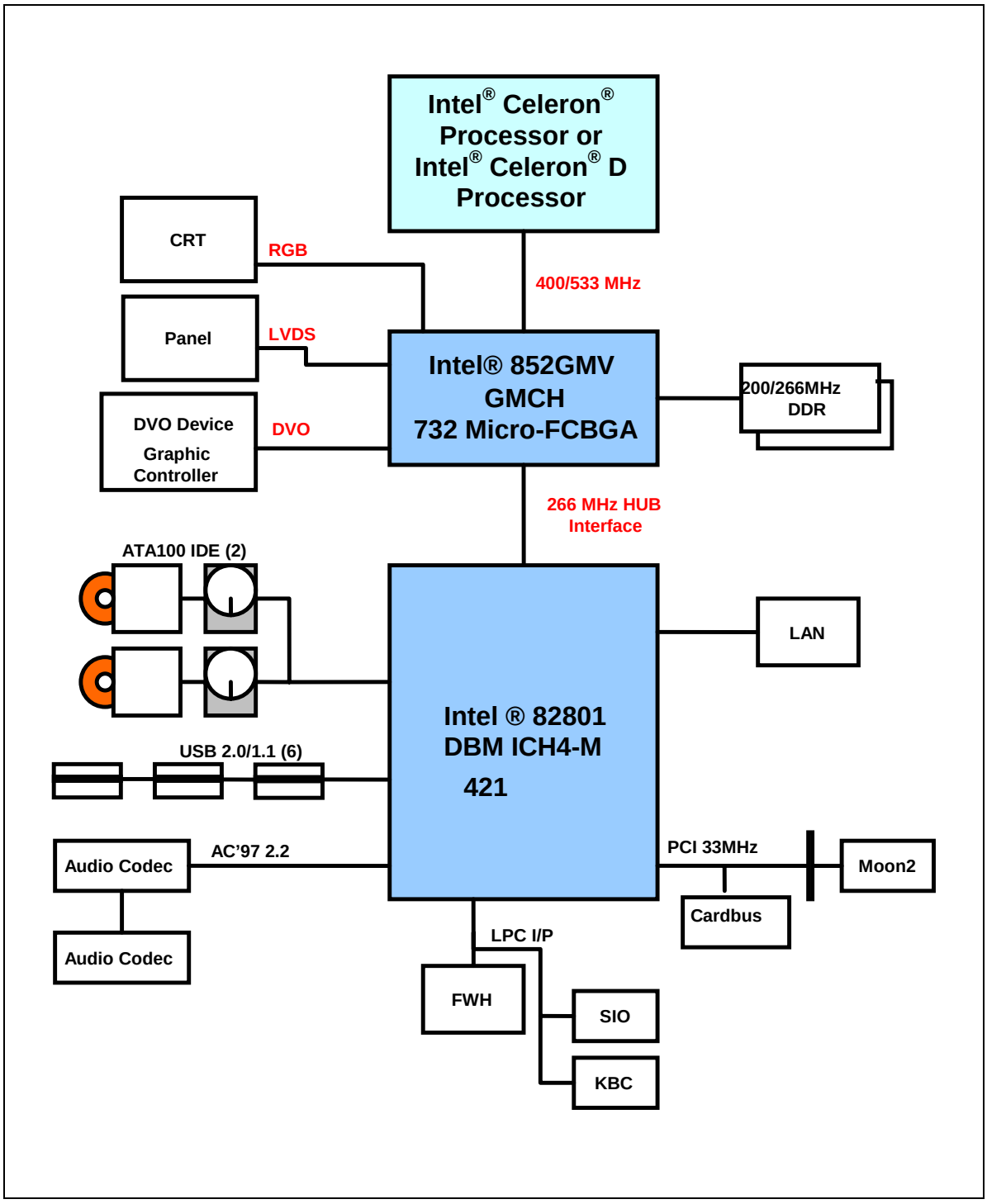
Hardware-based locking

5 GPIs

Package/Power

- 32-pin TSOP/PLCC
- 3.3-V core and 3.3 V/12 V for fast programming

**Figure 3. Intel 852GMV GMCH System Block Diagram**



# 3. General Design Considerations

This section documents motherboard layout and routing guidelines. It does not discuss the functional aspects of a bus or the layout guidelines for an add-in device.

***Note:*** If the guidelines listed in this document are not followed, then thorough signal integrity and timing simulations should be completed for each design. Even when the guidelines are followed, Intel recommends that critical signals be simulated to ensure proper signal integrity and flight time. Any deviation from the guidelines should be simulated.

The trace impedance typically noted (i.e. 55 ± 15% except for FSB signals 53 ± 15%) is the "nominal" trace impedance for a 5-mil wide external trace and a 4-mil wide internal trace. However, some stack-ups may lead to narrower or wider traces on internal or external layers in order to meet the 55- impedance target. It is important to consider the minimum and maximum impedance of a trace based on the switching of neighboring traces when calculating flight times. Using wider spaces between the traces can minimize this trace-to-trace coupling. In addition, these wider spaces reduce settling time.

Coupling between two traces is a function of the coupled length, the distance separating the traces, the signal edge rate, and the degree of mutual capacitance and inductance. In order to minimize the effects of trace-to-trace coupling, the routing guidelines documented in this section should be followed. Also, all high speed, impedance controlled signals (e.g. FSB signals) should have continuous GND referenced planes and cannot be routed over or under power/GND plane splits.

## 3.1. Recommended Board Stack-Up

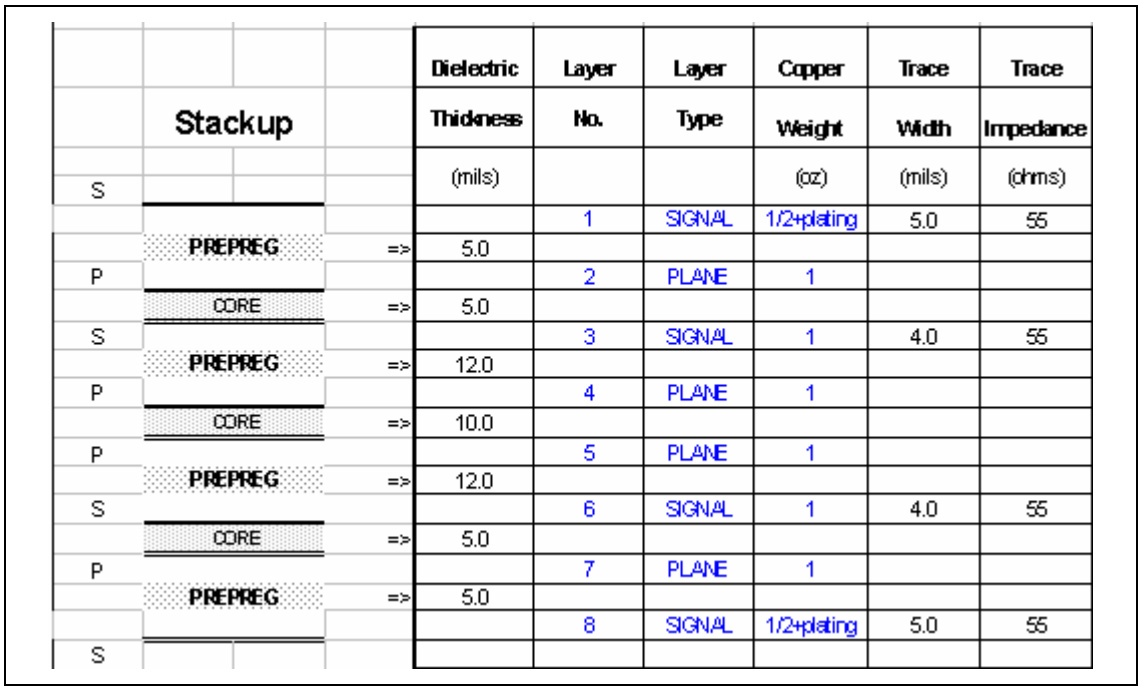
The Intel® 852GME/852GMV/852PM chipset based platforms require a board stack-up yielding a target impedance of 55 ± 15%. Figure 4 shows an example of an 8-layer board stack-up. The left side of the figure illustrates the starting dimensions of the metal and dielectric material thickness as well as drawn trace width dimensions prior to lamination, conductor plating, and etching. After the motherboard materials are laminated, conductors plated, and etched, somewhat different dimensions result. Dielectric materials become thinner, under/over etching of conductors alters their trace width, and conductor plating makes them thicker. It is important to note that for the purpose of extracting electrical models from transmission line properties, the final dimensions of signals after lamination, plating, and etching should be used.

The stack-up uses 1.2-mil (1 oz) copper on power planes to reduce I*R drops and 0.6-mil copper thickness on signal layers L1, L3, L6, and L8. After plating, the external layers become 1.2 to 2 mils thick.

To meet the nominal 55- characteristic impedance L1 and L8 micro-strip lines are drawn at 5-mil trace width but end up with a 5.5-mil final trace width after etching. For the same reason, the 5-mil thick prepreg between L1 and L2 starts at 5 mils but becomes 4.5 mils after lamination. This situation and result also applies to L7 and L8.

To ensure impedance control of 55- , L1, and L8 micro-strip lines should reference solid ground planes on L2 and L7, respectively.

**Figure 4. Recommended Board Stack-Up Dimensions**



| | Stackup | | Dielectric Thickness (mils) | Layer No. | Layer Type | Copper Weight (oz) | Trace Width (mils) | Trace Impedance (ohms) |
|---|---|---|---|---|---|---|---|---|
| S | | | | 1 | SIGNAL | 1/2+plating | 5.0 | 55 |
| | PREPREG | => | 5.0 | | | | | |
| P | | | | 2 | PLANE | 1 | | |
| | CORE | => | 5.0 | | | | | |
| S | | | | 3 | SIGNAL | 1 | 4.0 | 55 |
| | PREPREG | => | 12.0 | | | | | |
| P | | | | 4 | PLANE | 1 | | |
| | CORE | => | 10.0 | | | | | |
| P | | | | 5 | PLANE | 1 | | |
| | PREPREG | => | 12.0 | | | | | |
| S | | | | 6 | SIGNAL | 1 | 4.0 | 55 |
| | CORE | => | 5.0 | | | | | |
| P | | | | 7 | PLANE | 1 | | |
| | PREPREG | => | 5.0 | | | | | |
| | | | | 8 | SIGNAL | 1/2+plating | 5.0 | 55 |
| S | | | | | | | | |

Internal signal traces on L3 and L6 are unbalanced strip-lines. To meet the nominal 55- characteristic impedance for these traces, they reference solid ground plane on L2 and L7. Since the coupling to L4 and L5 is still significant, (especially true when thinner stack-ups use balanced strip- lines on internal layers) these layers are converted to ground floods in the areas of the motherboard where the speed critical interfaces like the FSB or DDR system memory are routed. In the remaining sections of the motherboard layout the L4 and L5 layers are used for power delivery.

For 55- characteristic impedance L3 (L6) strip-lines have a 4-mil final trace width and are separated by a core dielectric thickness of 4.8 mils after lamination from the L2 (L7) ground plane and 11.2-mil thickness prepreg after lamination to separate it from L4 (L5). The starting thickness of these core and prepreg dielectric layers before lamination is 5 mils and 12 mils, respectively.

L8 is also used for power delivery in many cases since it benefits from the thick copper plating of the external layer plating as well as referencing the close (4.5-mil prepeg thickness) L7 ground plane. The benefit of such a stack-up is low inductance power delivery.

## 3.2. Alternate Stack Ups

OEMs may choose to use different stack-ups (number of layers, thickness, trace width, etc.) from the one example outlined in. Figure 4. However, the following key elements should be observed:

Final post lamination, post etching, and post plating dimensions should be used for electrical model extractions.

Power plane layers should be 1-oz thick and signal layers should be ½ oz thick.

External l layers become 1 – 1.5 oz (1.2 – 2 mils) thick after plating

All high-speed signals should reference solid ground planes through the length of their routing and should not cross plane splits. To guarantee this, both planes surrounding strip-lines should be GND.

Intel recommends that high-speed signal routing be done on internal, strip-line layers.

High-speed signals transitioning between layers next to the component, signal pins should be accounted for by the GND stitching vias that would stitch all the GND plane layers in that area of the motherboard. Due to the arrangement of processor and GMCH/MCH pin-maps, GND vias placed near all GND lands will also be very close to high-speed signals that may be transitioning to an internal layer. Thus, no additional ground stitching vias (besides the GND pin vias) are required in the immediate vicinity of the processor and GMCH/MCH packages to accompany the signal transitions from the component side into an internal layer.

High-speed routing on external layers should be minimized in order to avoid EMI. Routing on external layers also introduces different delays compared to internal layers, making it extremely difficult to do length matching if some routing is done on both internal and external layers.

***Note:*** If Intel's recommended stackup guidelines are not used, then the OEM is liable for all aspects of their board design (for example, understanding impacts of SI and power distribution, etc.)

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# 4. FSB Design Guidelines

The following layout guidelines support designs using the Mobile Intel Pentium 4 processor and the Intel® 852GME/852GMV/852PMchipset.

Due to on-die Rtt resistors on both the processor and the chipset, additional resistors do not need to be placed on the motherboard for most FSB signals. The exception to these are RESET#, BPM[5:0]# signals which requires a 51.1 pull-up, and BR0 signal requires 220 + 5% pull-up to Vtt on the processor end of the transmission line.

## 4.1. FSB Routing Guidelines

Table 1 summarizes the FSB layout recommendations and provides detail on specific design issues.

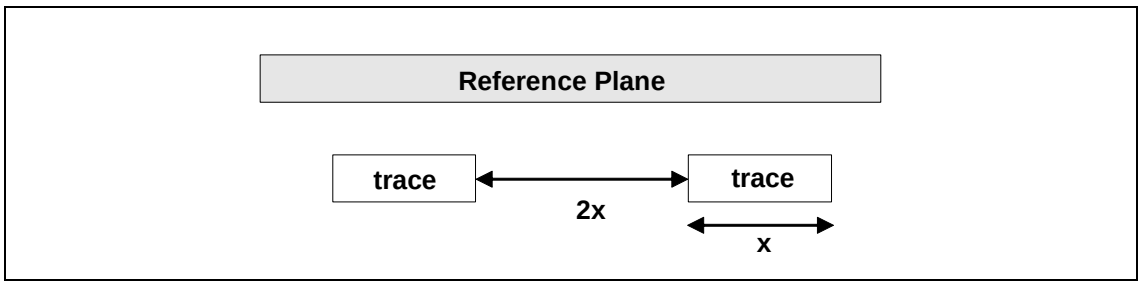
**Table 1. System Bus Routing Summary for the Processor**

| Parameter | Processor Routing Guidelines |
|---|---|
| Line to line spacing | Greater than or equal to 2:1 edge-to-edge spacing versus trace width for address and address strobes. Greater than or equal to 2.5:1 edge-to-edge spacing versus trace width or greater for data and data strobes.<br>See Figure 5 or an illustration of this recommendation. |
| Data Line lengths (agent to agent spacing) | 1.0 inches– 6.0 inches from pin-to-pin. Data signals of the same source synchronous group should be routed to the same pad-to-pad length within ± 0.100 inches of the associated strobes. The pad is defined as the attach point of the silicon die to the package substrate. Length must be added to the system board to compensate for package length differences. Signals in the same source synchronous group should be routed on the same layer and referenced to Vss. |
| DSTBn/p[3:0]# | A data strobe and its complement should be routed within ±0.025 inches of the same pad-to-pad length. The pad is defined as the attach point of the silicon die to the package substrate. Length must be added to the system board to compensate for package length differences. DSTBn/p# should be routed on the same layer as their associated data group and referenced to Vss. |
| Address line lengths (agent to agent spacing) | 1.0 inches – 6.0 inches from pin-to-pin address signals of the same source synchronous group should be routed to the same Pad-to-Pad length within± 0.200 inches of the associated strobes. The pad is defined as the attach point of the silicon die to the package substrate. Length must be added to the system board to compensate for package length differences. A layer transition may occur if the reference plane remains the same (Vss) and the layers are of the same configuration (all stripline or all microstrip). |
| ADSTBn/p[1:0]# | An address strobe should be routed to associated data signal within ± 0.200 “ of the same Pad-to-Pad length. The pad is defined as the attach point of the silicon die to the package substrate. Length must be added to the system board to compensate for package length |

| Parameter | Processor Routing Guidelines |
|---|---|
| | differences. A layer transition may occur if the reference plane remains the same (Vss) and the layers are all of the same configuration (all stripline or all microstrip). |
| Common Clock line lengths | 2.0 inches – 6.0 inches |
| Topology | Stripline |
| Routing priorities | All associated signals and strobes should be routed on same layer for entire length of bus. All signals should be referenced to Vss. Ideally, layer changes should not occur for any signals. If a layer change must occur, reference plane must be Vss and the layers must all be of the same configuration (all stripline or all microstrip for example). |
| Clock keepout zones | A spacing requirement of 16-20 mils should be maintained around all clocks. |
| Trace Impedance | 53 ohms ± 15% |
| Source Synchronous routing restrictions | There are no length-matching routing restrictions between (or within) either the source-synchronous data or address groups. As long as the strobe and associated line length routing guidelines are met for each group, there is no need to length-match between the groups. For example, one data group may be routed to the minimum allowable length while another data group could be routed to the maximum allowable length. Simulations have verified that the FSB will still function correctly even under this extreme condition. |

Refer to *Intel®852GME Chipset GMCH and Intel® 852PM Chipset MCH Datasheet* for GMCH package dimensions and refer to the *Mobile Intel® Pentium® 4 Processor Datasheet or Mobile Intel® Pentium® 4 Processor supporting Hyper-Threading Technology on 90-nm process technology Datasheet* for processor package dimensions.

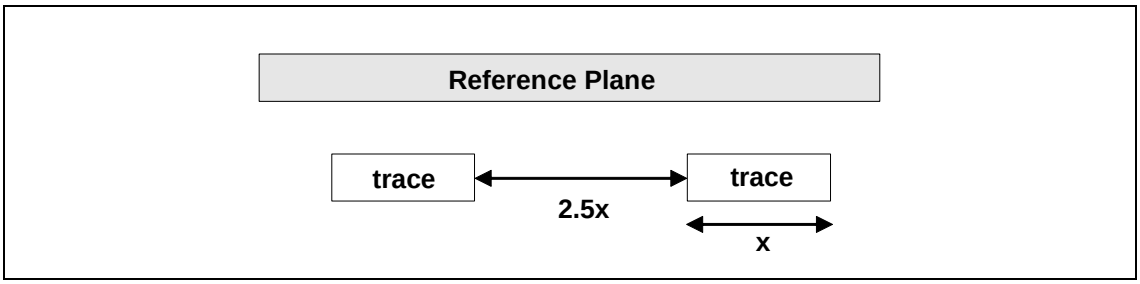
**Figure 5. Cross-Sectional View of 2:1 Ratio**




**NOTE:** This is the edge-to-edge trace spacing versus width.

For address and address strobes; a trace spacing to width ratio of 2 to 1 ensures a low crosstalk coefficient (based on geometries defined in 8 layer reference stackup). For data and data strobes; a trace spacing to width ratio of 2.5 to 1 (or greater) ensures a low crosstalk coefficient (based on geometries defined in 8 layer reference stackup). All the effects of crosstalk are difficult to simulate. A smaller ratio would have an unpredictable impact due to crosstalk.

Figure 6. Cross-Sectional View of 2.5:1 Ratio




### 4.1.1. Return Path Evaluation

The return path is the route current takes to return to its source. It may take a path through ground planes, power planes, other signals, integrated circuits, vias, VRMs, etc. Consider it as following a path of least impedance back to the original source. Discontinuities in the return path often have signal integrity and timing effects that are similar to the discontinuities in the signal conductor. Therefore, the return paths need to be given similar considerations. A simple way to evaluate return path parasitic inductance is to draw a loop that traces the current from the driver through the signal conductor to the receiver, and then back through the ground/power plane to the driver again. The smaller the area of the loop, the lower the parasitic inductance will be.

The following set of return path rules apply:

Always trace out the return current path and provide as much care to the return path as the path of the signal conductor.

Decoupling capacitors do not adequately compensate for a plane split.

Do not allow splits in the reference planes in the path of the return current.

Do not allow routing of signals on the reference planes near system bus signals.

Maintain Vss as a reference plane for all system bus signals.

Do not route over via anti-pads or socket anti-pads.

## 4.2. OPTIMIZED/COMPAT# Topology for Intel® 852GME/852GMV/852PM Only Platforms

The OPITIMIZED/COMPAT# pin tells the processor if the internal FSB signal impedance is set to 50 or 60 . By connecting the processor's OPTIMIZED/COMPAT# pin AE26 pin to GND, the internal FSB signal impedance is set to 50 . By leaving the pin as NC, the internal FSB signal impedance is set to 60 . In order for the platform to be compatible with the Mobile Intel Pentium 4 processor, this pin should be left as NC. If a platform is only used with the Mobile Intel Pentium 4 processor, then this pin can be connected to GND.

# 4.3. General Topology and Layout Guidelines

The following topology and layout guidelines are subject to change. The guidelines are derived from empirical testing with Intel® 852GME/852GMV/852PM chipset package models.

Below are the design recommendations for the data, address, strobes, common clock signals and others. For the following discussion, the pad is defined as the attach point of the silicon die to the package substrate.

## 4.3.1. Data Signals

Data signals of the same source synchronous group should be routed to the same **pad-to-pad** length within ± 0.100 inches of the associated strobes. As a result, additional trace will be added to some data nets on the system board in order for all trace lengths within the same data group to be the same length (± 0.100 inches) from the **pad** of the processor to the **associated pad** of the chipset.

**Equation 1. Calculation to Determine Package Delta Addition to Motherboard Length for UP Systems**

$$delta_{net,strobe} = (cpu_pkglen_{net} - cpu_pkglen_{strobe*}) + (cs_pkglen_{net} - cs_pkglen_{strobe})$$

Refer to the *Intel® 852GME Chipset GMCH and Intel® 852PM Chipset MCH Datasheet* for GMCH package dimensions and refer to the *Mobile Intel® Pentium® 4 Processor Datasheet* and the *Mobile Intel® Pentium® 4 Processor supporting Hyper-Threading Technology on 90-nm process technology Datasheet* for package dimensions.

***Note:*** Strobe package length is the average of the strobe pair.

## 4.3.2. Address Signals

Address signals follow the same rules as data signals except address signals should be routed to the same **pad-to-pad** length within ± 0.200 inches of the associated strobes. Address signals may change layers if the reference plane remains Vss.

## 4.3.3. Strobe Signals

A strobe and its complement should be routed to a length equal to their corresponding data group's mean **pad-to-pad** length ± 0.025 inches.

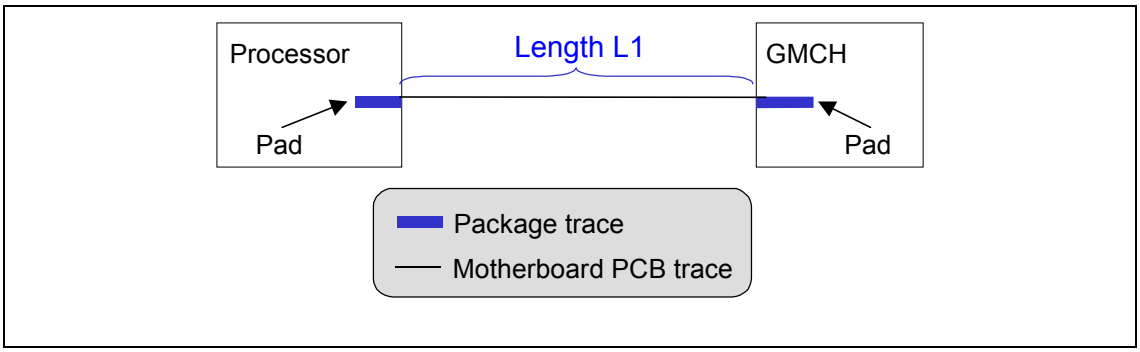
## 4.3.4. Common Clock Signals

Common clock signals should be routed to a minimum pin-to-pin motherboard length of **2.0** inches and a maximum motherboard length of **6.0** inches.

Source synchronous groups and associated strobes should be routed on the same layer for the entire length of the bus. This results in a significant reduction of the flight time skew since the dielectric

thickness, line width, and velocity of the signals will be uniform across a single layer of the stackup. There is no guarantee of a relationship of dielectric thickness, line width, and velocity between layers.

**Figure 7. Processor Topology**




## 4.3.5. Source Synchronous (SS) Signals

**Table 2. Processor System Bus Data Signal Routing Guidelines**

| Signal Names | | Transmission Line Type | Total Trace Length | | Nominal Impedance ( ) | Width & Spacing (mils) |
|---|---|---|---|---|---|---|
| CPU | GMCH | | Min (inches) | Max (inches) | | |
| DBI[3:0]# | DINV[3:0]# | Strip-line | 1.0 | 6.0 | 53 ± 15% | 4.5 & 11.5 |
| D[63:0]# | HD[63:0]# | Strip-line | 1.0 | 6.0 | 53 ±15% | 4.5 & 11.5 |
| DSTBN[3:0]# | HDSTBN[3:0]# | Strip-line | 1.0 | 6.0 | 53 ± 15% | 4.5 & 11.5 |
| DSTBP[3:0]# | HDSTBP[3:0]# | Strip-line | 1.0 | 6.0 | 53 ±15% | 4.5 & 11.5 |

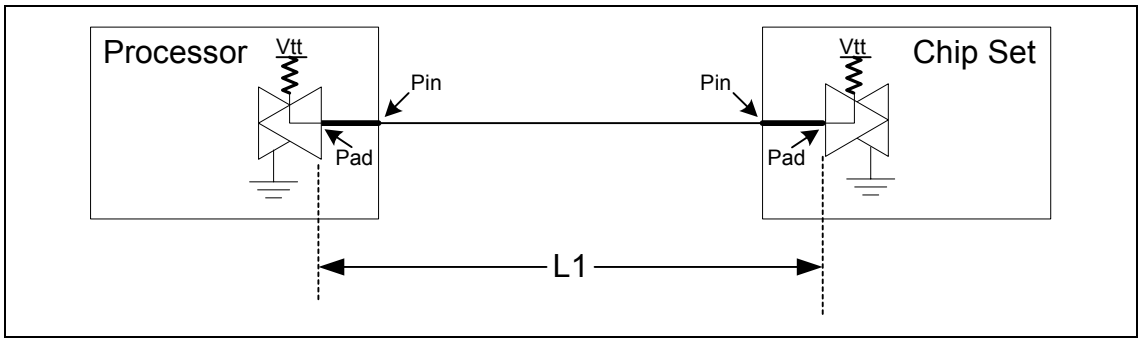
**NOTE:** The Data signals within each group must be routed to within ± 0.100 inches of its associated “reference” strobe. The complement strobe must be routed to within ± 0.025 inches of the associate “reference” strobe. All traces within each signal group must be routed on the same layer (required). Intel recommends that length of the strobes be centered to the average length of associated data or address traces to maximize setup/hold time margins.

**Table 3. Processor System Bus Address Signal Routing Guidelines**

| Signal Names | | Transmission Line Type | Total Trace Length | | Nominal Impedance ( ) | Width & Spacing (mils) |
|---|---|---|---|---|---|---|
| CPU | GMCH | | Min (inches) | Max (inches) | | |
| A[31:3]# | HA[31:3]# | Strip-line | 1.0 | 6.0 | 53 ± 15% | 4.5 & 9 |
| REQ[4:0]# | HREQ[4:0]# | Strip-line | 1.0 | 6.0 | 53 ± 15% | 4.5 & 9 |
| ADSTB[1:0]# | HADSTB[1:0]# | Strip-line | 1.0 | 6.0 | 53 ± 15% | 4.5 & 9 |

**NOTE:** The Address signals within each group must be routed to within ± 0.200 of its associated strobe. All traces within each signal group must be routed on the same layer (required). It is recommended that length of the strobes be centered to the average length of associated data or address traces to maximize setup/hold time margins. Please refer to *Mobile Intel® Pentium® 4 Processor Datasheet* or*Mobile Intel® Pentium® 4 Processor supporting Hyper-Threading Technology on 90-nm process technology Datasheet* for signals and associated strobe.

**Figure 8. SS Topology for Address and Data**




## 4.3.6. Common Clock (CC) AGTL+ Signals

**Table 4. Processor System Bus Control Signal Routing Guidelines**

| Signal Names | | Topology | Routing Trace Length (Pin-to-Pin) | | Nominal Impedance (ohms) | Width & spacing (mils) |
|---|---|---|---|---|---|---|
| CPU | GMCH | | Max (inches) | Min (inches) | | |
| RESET# | CPURST# | Stripline | 6.0 | 2.0 | 53 ± 15% | 4.5 & 11.5 |
| BR0# | BREQ0# | Stripline | 6.0 | 2.0 | 53 ± 15% | 4.5 & 11.5 |
| BNR# | BNR# | Stripline | 6.0 | 2.0 | 53 ± 15% | 4.5 & 11.5 |
| REQ[4:0]# | HREQ[4:0]# | Stripline | 6.0 | 2.0 | 53 ± 15% | 4.5 & 11.5 |
| BPRI# | BPRI# | Stripline | 6.0 | 2.0 | 53 ± 15% | 4.5 & 11.5 |
| DEFER# | DEFER# | Stripline | 6.0 | 2.0 | 53 ± 15% | 4.5 & 11.5 |
| LOCK# | HLOCK# | Stripline | 6.0 | 2.0 | 53 ± 15% | 4.5 & 11.5 |
| TRDY# | HTRDY# | Stripline | 6.0 | 2.0 | 53 ± 15% | 4.5 & 11.5 |
| DRDY# | DRDY# | Stripline | 6.0 | 2.0 | 53 ± 15% | 4.5 & 11.5 |
| ADS# | ADS# | Stripline | 6.0 | 2.0 | 53 ± 15% | 4.5 & 11.5 |
| DBSY# | DBSY# | Stripline | 6.0 | 2.0 | 53 ± 15% | 4.5 & 11.5 |
| HIT# | HIT# | Stripline | 6.0 | 2.0 | 53 ± 15% | 4.5 & 11.5 |
| HITM# | HITM# | Stripline | 6.0 | 2.0 | 53 ± 15% | 4.5 & 11.5 |
| RS[2:0]# | RS[2:0]# | Stripline | 6.0 | 2.0 | 53 ± 15% | 4.5 & 11.5 |

**NOTE:** Trace width of 4.5 mils and trace spacing of 11.5 mils within signal groups. Entire trace for each signal routed on one layer (recommended) RESET# and BR0# are CC AGTL+ signals without ODT (On die termination). For these signals Rtt should be placed near CPU: L2<= 0.5 inches. Rtt = 51.1 ±1%. Routing these signals to 4.0 inches ± 0.5 inches should maximize the setup and hold margin parameters while adhering to expected mobile solution design constraints.

## 4.3.7. Asynchronous AGTL+ Signals

All signals must meet the AC and DC specifications as documented in the *Mobile Intel® Pentium® 4 Processor Datasheet* or the *Mobile Intel® Pentium® 4 Processor supporting Hyper-Threading Technology on 90-nm process technology Datasheet.*

***Note:*** All AGTL+ signals within this document are same as GTL+.

### 4.3.7.1. Topologies

#### 4.3.7.1.1. Topology 1A: Open Drain (OD) Signals Driven by the Processor – IERR# and FERR#

The topology 1A OD signals IERR# and FERR# should adhere to the following routing and layout recommendations. Table 5 lists the recommended routing requirements for the IERR# and FERR# signals of the Mobile Intel Pentium 4 processor. The routing guidelines allow the signal to be routed as either micro-strip or strip-lines using 53 ± 5% characteristic trace impedance. The pull-up voltage for termination resistor Rtt is VCC_CORE.

Due to the dependencies on system design implementation, IERR# can be implemented in a number of ways to meet design goals. IERR# can be routed as a test point or to any optional system receiver. Intel recommends that the FERR# signal of the Mobile Intel Pentium 4 processor be routed to the FERR# signal of the Intel ICH4-M.

**Figure 9. Routing Illustration for Topology 1A**

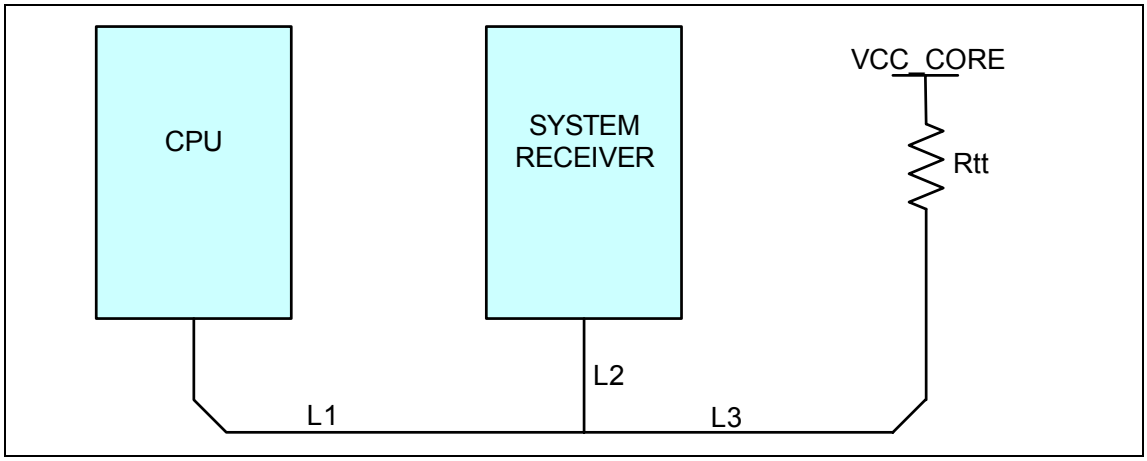



**Table 5. Layout Recommendations for Topology 1A**

| L1 | L2 | L3 | Rtt | Transmission Line Type |
|---|---|---|---|---|
| 0.5” – 12.0” | 0” – 3.0” | 0” – 3.0” | 56 ± 5% | Micro-strip |
| 0.5” – 12.0” | 0” – 3.0” | 0” – 3.0” | 56 ± 5% | Strip-line |

#### 4.3.7.1.2. Topology 1B: Open Drain (OD) Signals Driven by the Processor –THERMTRIP#

The Topology 1B OD signal THERMTRIP# should adhere to the following routing and layout recommendations. Table 6 lists the recommended routing requirements for the THERMTRIP# signals of the processor. The routing guidelines allow the signal to be routed as either micro-strip or strip-lines using 53 ± 15% characteristic trace impedance. The pull-up voltage for termination resistor Rtt is VCCP.

THERMTRIP# can be implemented in a number of ways to meet design goals. It can be routed to the ICH4-M or any optional system receiver. Intel recommends that the THERMTRIP# signal of the processor be routed to the THRMTRIP# signal of the ICH4-M. The ICH4-M's THRMTRIP# signal is a new signal to the I/O controller hub architecture that allows the ICH4-M to quickly put the whole system into an S5 state whenever the catastrophic thermal trip point has been reached.

**Figure 10. Routing Illustration for Topology 1B**

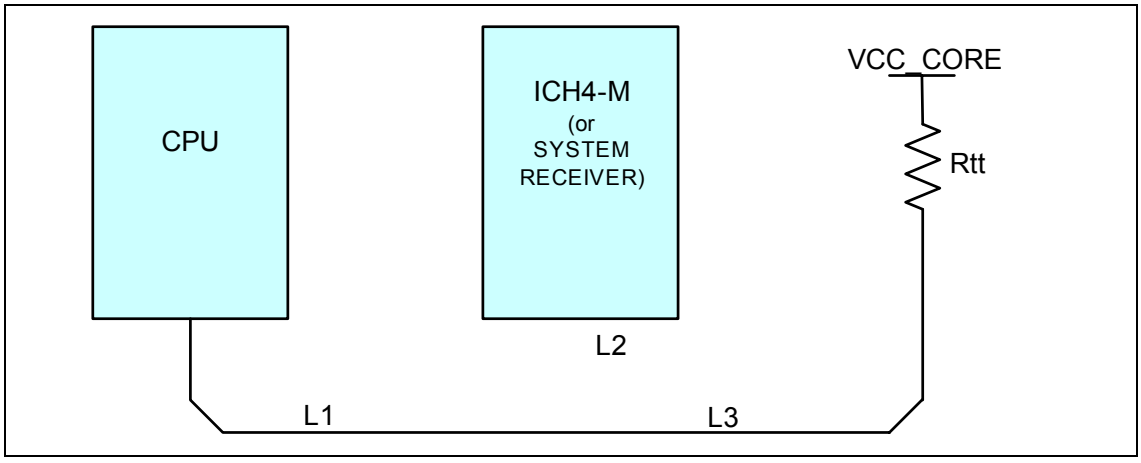



**Table 6. Layout Recommendations for Topology 1B**

| L1 | L2 | L3 | R1 | Rtt | Transmission Line Type |
|---|---|---|---|---|---|
| 0.5" – 12.0" | 0" – 3.0" | 0" – 3.0" | 56 ± 5% | 56 ± 5% | Micro-strip |
| 0.5" – 12.0" | 0" – 3.0" | 0" – 3.0" | 56 ± 5% | 56 ± 5% | Strip-line |

### 4.3.7.1.3. Topology 1C: Open Drain (OD) Signals Driven by the Processor –PROCHOT#

The Topology 1C OD signal PROCHOT#, should adhere to the following routing and layout recommendations. Table 7 lists the recommended routing requirements for the PROCHOT# signal. The routing guidelines allow the signal to be routed as either a micro-strip or strip-line using 55 ± 15% characteristic trace impedance. Figure 11 shows the recommended implementation for providing voltage translation between the processor's PROCHOT# signal and a system receiver that utilizes a 3.3-V interface voltage (shown as VCCP).

Series resistor Rs is a component of the voltage translation logic and serves as a driver isolation resistor. Rs is shown separated by distance L3 from the first bipolar junction transistor (BJT), Q1, to emphasize the placement of Rs with respect to Q1. The placement of Rs a distance L3 before the Q1 BJT is a specific implementation of the generalized voltage translator circuit shown in Figure 11. Rs should be placed at the beginning of the T-split from the PROCHOT# signal. The pull-up voltage for termination resistor Rtt is VCCP.

Intel recommends that PROCHOT# be routed using the voltage translation logic shown in Figure 11.

**Figure 11. Routing Illustration for Topology 1C**

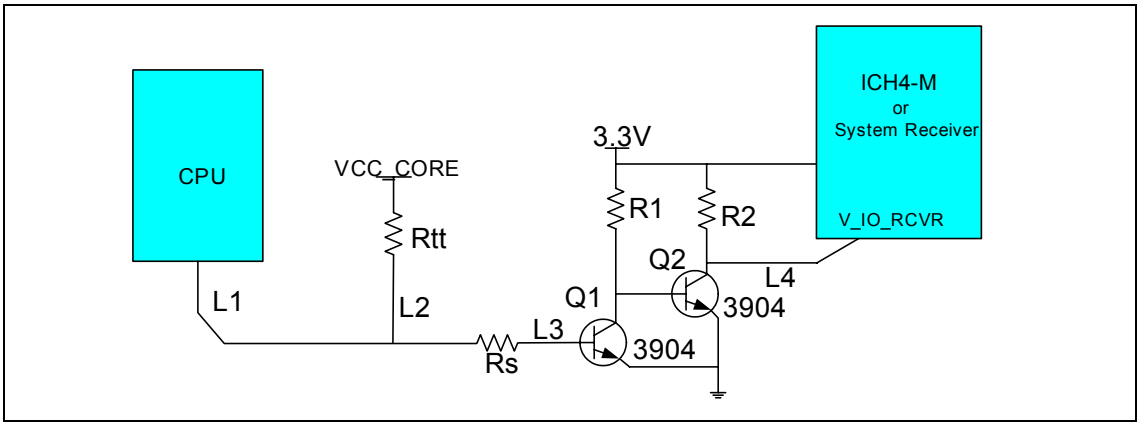



**Table 7. Layout Recommendations for Topology 1C**

| L1 | L2 | L3 | L4 | Rs | R1 | R2 | Rtt | Transmission Line Type |
|---|---|---|---|---|---|---|---|---|
| 0.5 – 12.0" | 0 - 3.0" | 0 – 3.0" | 0.5 – 12.0" | ± 5% | 1.3 k ± 5% | 330 ± 5% | 56 ± 5% | Micro-strip |
| 0.5 – 12.0" | 0 - 3.0" | 0 – 3.0" | 0.5 – 12.0" | ± 5% | 1.3 k ± 5% | 330 ± 5% | 56 ± 5% | Strip-line |

#### 4.3.7.1.4. Topology 2A: Open Drain (OD) Signals Driven by ICH4-M – PWRGOOD

The Topology 2A OD signal PWRGOOD should adhere to the following routing and layout recommendations.

Table 8 lists the recommended routing requirements for the PWRGOOD signal of the Mobile Intel Pentium 4 processor. The routing guidelines allow the signal to be routed as either micro-strip or strip-lines using 53 ± 15% characteristic trace impedance. The pull-up voltage for termination resistor Rtt is VCC_CORE.

***Note:*** The Intel ICH4-M's CPUPWRGD signal should be routed point-to-point to the Mobile Intel Pentium 4 processor's PWRGOOD signal. The routing from the Mobile Intel Pentium 4 processor's PWRGOOD pin should fork out to both the termination resistor, Rtt, and the ICH4-M. Segments L1 and L2 from Figure 17 should not T-split from a trace from the Mobile Intel Pentium 4 processor pin.

**Figure 12. Routing Illustration for Topology 2A**

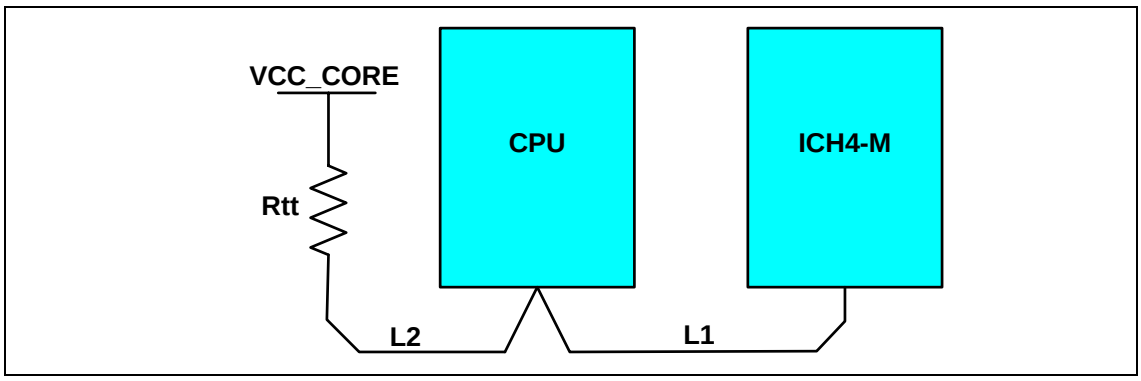



**Table 8. Layout Recommendations for Topology 2A**

| L1 | L2 | Rtt | Transmission Line Type |
|---|---|---|---|
| 0.5" – 12.0" | 0" – 3.0" | 300 ± 5% | Micro-strip |
| 0.5" – 12.0" | 0" – 3.0" | 300 ± 5% | Strip-line |

#### 4.3.7.1.5. Topology 2B: CMOS Signals Driven by ICH4-M – DPSLP#

The Topology 2B CMOS DPSLP# signal should adhere to the following routing and layout recommendations illustrated in Figure 13. As listed in Table 9, the L1 and L2 segments of the DPSLP# signal topology can be routed as either micro-strip or strip-lines using 53 ± 15% characteristic trace impedance. Note that the Intel ICH4-M's DPSLP# signal should be routed point-to-point with the daisy chain topology shown. The routing of DPSLP# at the CPU should fork out to both the ICH4-M and the GMCH. Segments L1 and L2 from Table 9 should not T-split from a trace from the Mobile Intel Pentium 4 processor pin.

**Figure 13. Routing Illustration for Topology 2B**

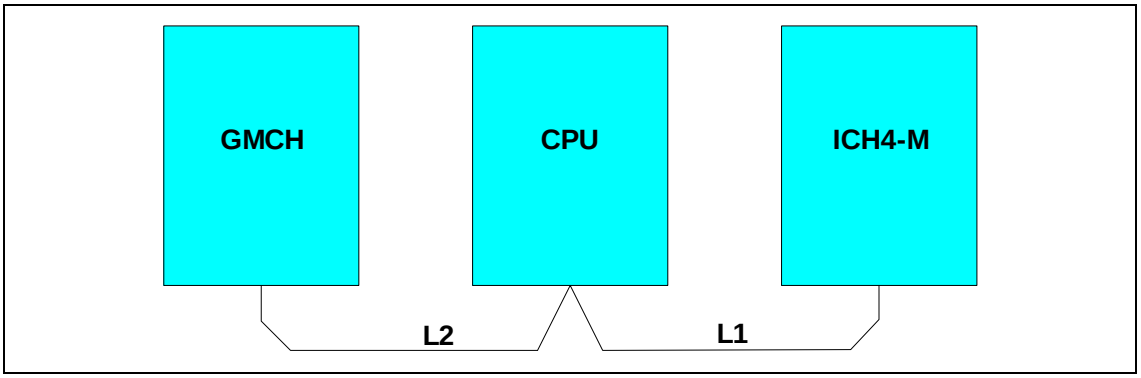



**Table 9. Layout Recommendations for Topology 2B**

| L1 | L2 | Transmission Line Type |
|---|---|---|
| 0.5" – 12.0" | 0.5" – 6.5" | Micro-strip |
| 0.5" – 12.0" | 0.5" – 6.5" | Strip-line |

#### 4.3.7.1.6. Topology 2C: CMOS Signals Driven by ICH4-M – A20M#, IGNNE#, LINT0/INTR, LINT1/NMI, SLP#, SMI#, and STPCLK#

The Topology 2C CMOS A20M#, IGNNE#, LINT0/INTR, LINT1/NMI, SLP#, SMI#, and STPCLK# signals should implement a point-to-point connection between the ICH4-M and the Mobile Intel Pentium 4 processor. The routing guidelines allow both signals to be routed as either micro-strip or strip-lines using 53 ± 15% characteristic trace impedance. No additional motherboard components are necessary for this topology.

**Figure 14. Routing Illustration for Topology 2C**

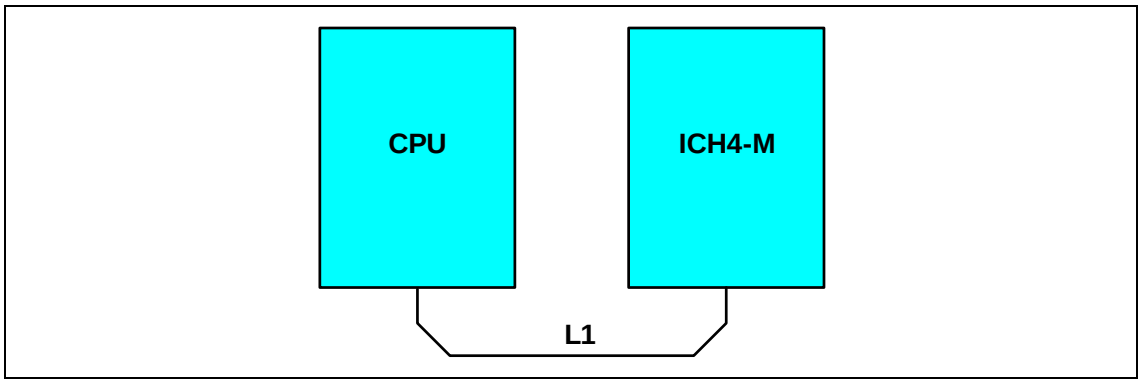



**Table 10. Layout Recommendations for Topology 2C**

| L1 | Transmission Line Type |
|---|---|
| 0.5” – 12.0” | Micro-strip |
| 0.5” – 12.0” | Strip-line |

### 4.3.7.1.7. Topology 3: CMOS Signals Driven by ICH4-M to CPU and FWH – INIT#

The signal INIT# should adhere to the following routing and layout recommendations. Table 11 lists the recommended routing requirements for the INIT# signal of the ICH4-M. The routing guidelines allow both signals to be routed as either micro-strip or strip-lines using 53 ± 15% characteristic trace impedance.

Figure 15 shows the recommended implementation for providing voltage translation between the ICH4-M's INIT# voltage signaling level and any firmware hub (FWH) that utilizes a 3.3-V interface voltage (shown as a supply V_IO_FWH). See Section 4.3.7.2 for more details on the voltage translator circuit. For convenience, the entire topology and required transistors and resistors for the voltage translator is shown in Figure 15.

Series resistor Rs is a component of the voltage translator logic circuit and serves as a driver isolation resistor. Rs is shown separated by distance L3 from the first bipolar junction transistor (BJT), Q1, to emphasize the placement of Rs with respect to Q1. The placement of Rs a distance of L3 before the Q1 BJT is a specific implementation of the generalized voltage translator circuit shown in Figure 16. The routing recommendations of transmission line L3 in Figure 15 is listed in Table 11 and Rs should be placed at the beginning of the T-split of the trace from the ICH4-M's INIT# pin.

**Figure 15. Routing Illustration for Topology 3**

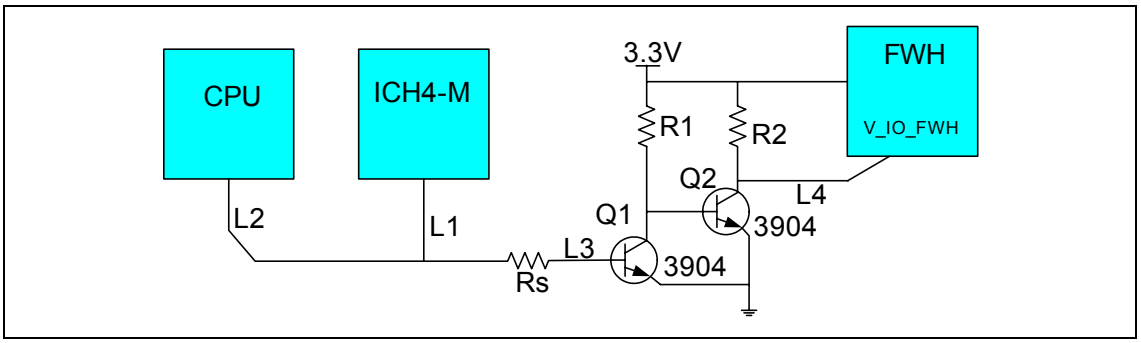



**Table 11. Layout Recommendations for Topology 3**

| L1 + L2 | L3 | L4 | Rs | R1 | R2 | Transmission Line Type |
|---|---|---|---|---|---|---|
| 0.5" – 12.0" | 0" – 3.0" | 0.5" – 6.0" | 300 ± 5% | 1.3 k ± 5% | 330 ± 5% | Micro-strip |
| 0.5" – 12.0" | 0" – 3.0" | 0.5" – 6.0" | 300 ± 5% | 1.3 k ± 5% | 330 ± 5% | Strip-line |

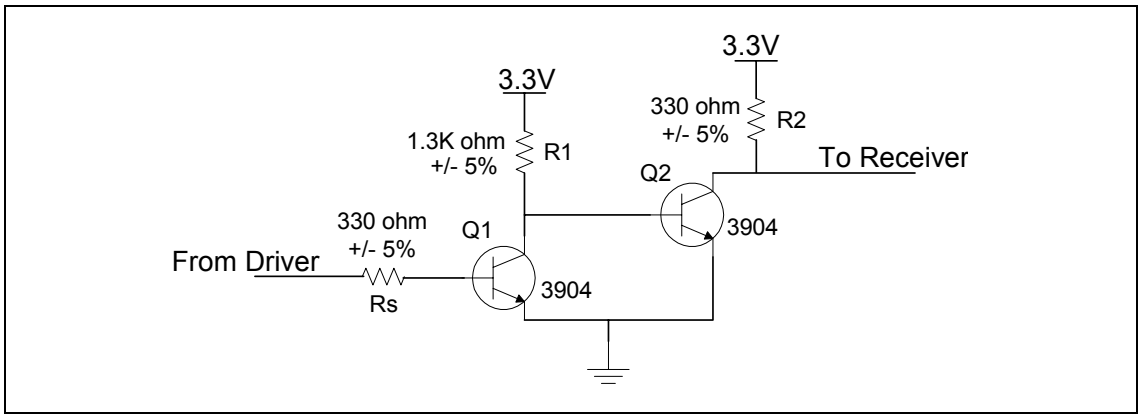
### 4.3.7.2. Voltage Translation Circuit

A voltage translation circuit or component is required on any signals where the voltage signaling level between two components connected by a transmission line may cause unpredictable signal quality. The recommended voltage translation circuit for the platform is shown in Figure 16. For the INIT# signal (Section 4.3.7.1.7) a specialized version of this voltage translator circuit is used where the driver isolation resistor, Rs, is place at the beginning of a transmission line that connects to the first bipolar junction transistor, Q1. Though the circuit shown in Figure 16 was developed to work with signals that require translation from VCC_CORE to a 3.3-V voltage level, the same topology and component values, in general, can be adapted for use with other signals as well provided the interface voltage of the receiver is also 3.3 V. Any component value changes or component placement requirements for other signals must be simulated in order to guarantee good signal quality and acceptable performance from the circuit.

In addition to providing voltage translation between driver and receiver devices, the recommended circuit also provides filtering for noise and electrical glitches. A larger driver isolation resistor, Rs, can be used on the collector of Q1, however, it will result in a slower response time to the output falling edge. In the case of the INIT# signal, resistors with values as close as possible to those listed in Figure 16 should be used without exception.

With the low VCC_CORE signaling level of the processor system bus, the voltage translation circuit provides ample isolation of any transients or signal reflections at the input of transistor Q1 from reaching the output of transistor Q2. Based on simulation results, the voltage translation circuit can effectively isolate transients as large as 200 mV and that last as long as 60 ns.

**Figure 16. Voltage Translation Circuit for 3.3-V Receivers**




## 4.3.8. AGTL+ I/O Buffer Compensation

The Mobile Intel Pentium 4 processor has two pins, COMP[1:0], and the 852GME / 852PM chipset GMCH has two pins, HXRCOMP and HYRCOMP, that require compensation resistors to adjust the AGTL+ I/O buffer characteristics to specific board and operating environment characteristics. Also, the GMCH requires two special reference voltage generation circuits to pins HXSWING and HYSWING for the same purpose described above. Refer to the *Mobile Intel® Pentium® 4 Processor Datasheet, Mobile Intel® Pentium® 4 Processor supporting Hyper-Threading Technology on 90-nm process technology Datasheet* and *Intel® 852GME Chipset GMCH and Intel® 852PM Chipset MCH Datasheet* for details on resistive compensation.

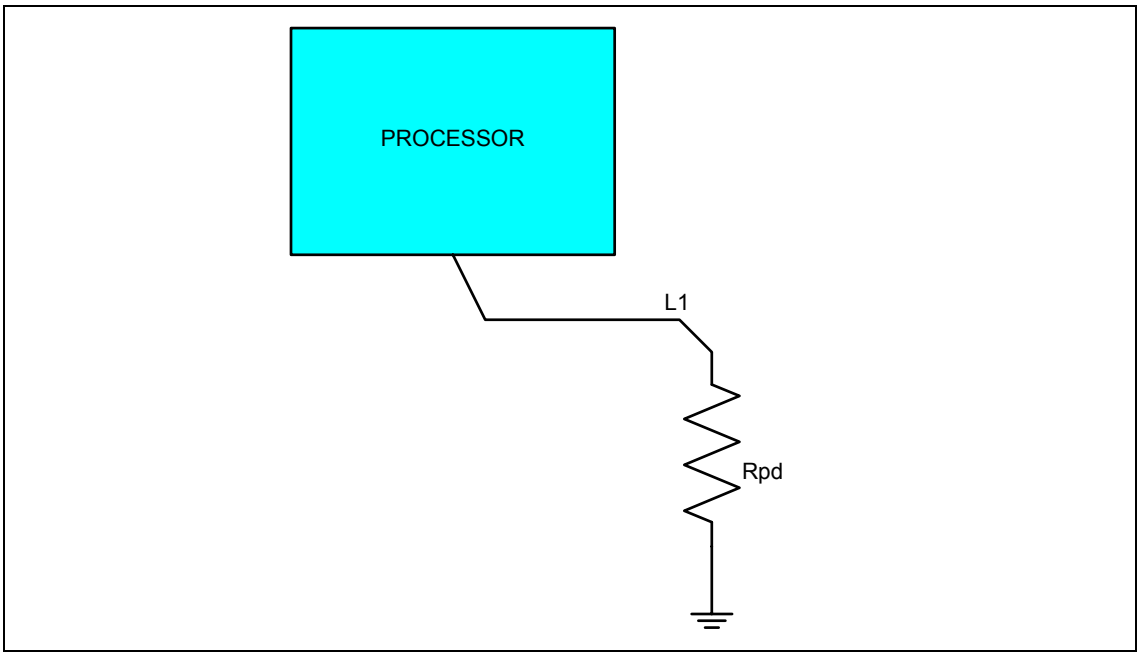
#### 4.3.8.1. Mobile Intel Pentium 4 Processor AGTL+ I/O Buffer Compensation

The COMP[1:0] signals adhere to the following routing recommendation. Table 12 illustrates the recommendation topology.

**Table 12. Layout Recommendation for COMP[1:0]**

| Trace width | Trace Spacing | L1 | Rpd |
|---|---|---|---|
| 15 mil | 25 mils | 0.5 inches Maximum | 61.9 ± 1% |

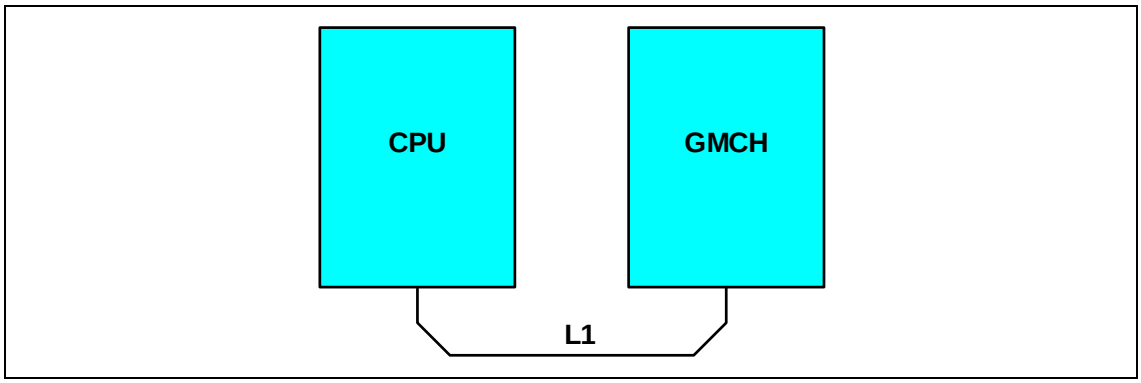
**Figure 17. Routing Recommendation for COMP[1:0]**




## 4.3.9. Processor RESET# Signal

The RESET# signal is a common clock signal driven by the GMCH CPURESET# pin. In a production system where no ITP700FLEX debug port is implemented, a simple point-to-point connection between the CPURESET# pin of the GMCH and the processor's RESET# pin is recommended (see Figure 18).On-die termination of the AGTL+ buffers on both the processor and the GMCH provide proper signal quality for this connection. Length L1 of this interconnect should be limited to minimum of 1 inch and maximum of 6.5 inches.

**Figure 18. Processor RESET# Signal Routing Topology with NO ITP700FLEX Connector**




For a system that implements an ITP700FLEX debug port, a more elaborate topology is required in order to guarantee proper signal quality at both the processor signal pad and the ITP700FLEX input receiver. In this case the topology illustrated in Figure 19 should be implemented. The CPURESET# signal from the GMCH should fork out (do not route one trace from GMCH pin and then T-split) towards the processor's RESET# pin as well as towards the Rtt and Rs resistive termination network placed next to the ITP700FLEX debug port connector. Rtt (54.9 + 1%) pulls-up to the VCCP voltage and is placed at the end of the L2 line that is limited to a 12-inch maximum length. Rs (22.6 ± 1%) should be placed right next to Rtt to minimize the routing between them in the vicinity of the ITP700FLEX connector to limit the L3 length to less than 0.5 inches. ITP700FLEX operation requires the matching of L2 + L3 - L1 length to the length of the BPM[4:0]# signals length within ± 50 ps.

Currently 1% tolerance resistors are recommended for Rs and Rtt. The use of 5% tolerant resistors for these resistors, and whether it could provide adequate signal quality performance, is under investigation.

**Figure 19. Processor RESET# Signal Routing Topology with ITP700FLEX Connector**

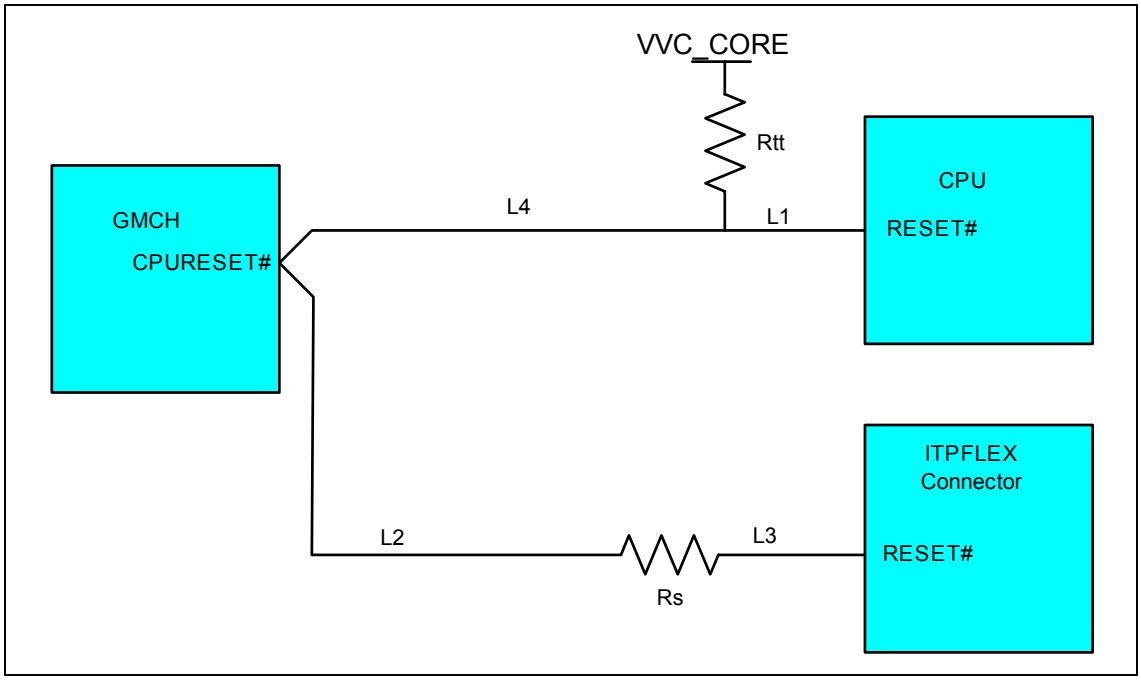


**Table 13. Processor RESET# Signal Routing Guidelines with ITP700FLEX Connector**

| L1 | L1+L4 | L2 + L3 | L3 | Rs | Rtt |
|---|---|---|---|---|---|
| 0.1” – 0.5” | 1.0” – 6.0” | 12.0” max | 0.5” max | Rs = 150 ± 1% | Rtt = 51 ± 1% |

## 4.4. Host Vrefs

The AGTL+ VREF provides a reference voltage for all of the FSB signals on the CP. It is required that a voltage divider yields **0.63 *VCC_AVG** where VCC_AVG is the average voltage of VCC_CPU and GMCH_VTT. The output is then routed to the CPU’s GTLREF.

## 4.5. ITP Debug Port

Please refer to the *ITP700 Debug Port Design Guide*, which can be found on http://developer.intel.com/design/Xeon/guides/249679.htm.

### 4.5.1. Logic Analyzer Interface (LAI)

Intel is working with two logic analyzer vendors to provide logic analyzer interfaces (LAIs) for use in debugging the Mobile Intel Pentium 4 processor system. Tektronix* and Agilent* should be contacted to get specific information about their logic analyzer interfaces. The following information is general in nature. Specific information must be obtained from the logic analyzer vendor.

Due to the complexity of the Mobile Intel Pentium 4 processor system, the LAI is critical in providing the ability to probe and capture system bus signals. There are two sets of considerations to keep in mind when designing Mobile Intel Pentium 4 processor that can make use of an LAI: mechanical and electrical.

#### 4.5.1.1. Mechanical Considerations

The LAI is installed between the processor socket and the Mobile Intel Pentium 4 processor. The LAI pins plug into the socket, while the Mobile Intel Pentium 4 processor plugs into a socket on the LAI. Cabling that is part of the LAI egresses the system to allow an electrical connection between the Mobile Intel Pentium 4 processor and a logic analyzer. The maximum volume occupied by the LAI, known as the keepout volume, as well as the cable egress restrictions, should be obtained from the logic analyzer vendor. System designers must make sure that the keepout volume remains unobstructed inside the system. Note that it is possible that the keepout volume reserved for the LAI may include space normally occupied by the Mobile Intel Pentium 4 processor heat sink. If this is the case, the logic analyzer vendor will provide a cooling solution as part of the LAI.

#### 4.5.1.2. Electrical Considerations

The LAI will also affect the electrical performance of the system bus; therefore, it is critical to obtain electrical load models from each of the logic analyzers to be able to run system level simulations to prove that their tool will work in the system. Contact the logic analyzer vendor for electrical specifications and load models for the LAI solution they provide.

## 4.6. Mobile Intel Pentium 4 Processor and 852GME/852GMV/852PMChipset FSB Signal Package Lengths

Table 14 lists the package trace lengths of the Mobile Intel Pentium 4 processor and the 852GME/852GMV/852PMGMCH for the source synchronous data and address signals. All the signals within the same group are routed to the same length as listed below with ± 0.1-mil accuracy. As a result of this package trace length matching, no motherboard trace length compensation is needed for these signals. Refer to Section 4.1 for further details. The Mobile Intel Pentium 4 processor and 852GME GMCH package traces are routed as micro-strip lines with a nominal characteristic impedance of 53 ± 15%.

**Table 14. Mobile Intel Pentium 4 Processor and 852GME Chipset Package Lengths**

| Processor lengths | | | GMCH Lengths | | |
|---|---|---|---|---|---|
| **Signal** | **Processor Ball** | **Length (inches)** | **Signal** | **GMCH ball** | **Length (mils)** |
| **Address Group 0** | | | | | |
| ADSTB[0]# | L5 | 0.210 | HADSTB[0]# | T26 | 419 |
| A[3]# | K2 | 0.368 | HA[3]# | P23 | 468 |
| A[4]# | K4 | 0.265 | HA[4]# | T25 | 353 |
| A[5]# | L6 | 0.155 | HA[5]# | T28 | 551 |
| A[6]# | K1 | 0.415 | HA[6]# | R27 | 523 |
| A[7]# | L3 | 0.304 | HA[7]# | U23 | 274 |
| A[8]# | M6 | 0.144 | HA[8]# | U24 | 333 |
| A[9]# | L2 | 0.372 | HA[9]# | R24 | 327 |
| A[10]# | M3 | 0.327 | HA[10]# | U28 | 560 |
| A[11]# | M4 | 0.246 | HA[11]# | V28 | 566 |
| A[12]# | N1 | 0.394 | HA[12]# | U27 | 522 |
| A[13]# | M1 | 0.408 | HA[13]# | T27 | 501 |
| A[14]# | N2 | 0.349 | HA[14]# | V27 | 562 |
| A[15]# | N4 | 0.241 | HA[15]# | U25 | 375 |
| A[16]# | N5 | 0.198 | HA[16]# | V26 | 491 |
| REQ[0]# | J1 | 0.427 | HREQ[0]# | R28 | 569 |
| REQ[1]# | K5 | 0.207 | HREQ[1]# | P25 | 378 |
| REQ[2]# | J4 | 0.270 | HREQ[2]# | R23 | 247 |
| REQ[3]# | J3 | 0.337 | HREQ[3]# | R25 | 383 |
| REQ[4]# | H3 | 0.356 | HREQ[4]# | T23 | 276 |
| **Address Group 1** | | | | | |
| ADSTB[1]# | R5 | 0.214 | HADSTB[1]# | AA26 | 504 |

| Processor lengths | | | GMCH Lengths | | |
|---|---|---|---|---|---|
| A[17]# | T1 | 0.470 | HA[17]# | Y24 | 457 |
| A[18]# | R2 | 0.404 | HA[18]# | V25 | 389 |
| A[19]# | P3 | 0.303 | HA[19]# | V23 | 284 |
| A[20]# | P4 | 0.246 | HA[20]# | W25 | 414 |
| A[21]# | R3 | 0.334 | HA[21]# | Y25 | 429 |
| A[22]# | T2 | 0.388 | HA[22]# | AA27 | 545 |
| A[23]# | U1 | 0.458 | HA[23]# | W24 | 382 |
| A[24]# | P6 | 0.156 | HA[24]# | W23 | 353 |
| A[25]# | U3 | 0.379 | HA[25]# | W27 | 536 |
| A[26]# | T4 | 0.281 | HA[26]# | Y27 | 556 |
| A[27]# | V2 | 0.417 | HA[27]# | AA28 | 631 |
| A[28]# | R6 | 0.166 | HA[28]# | W28 | 579 |
| A[29]# | W1 | 0.493 | HA[29]# | AB27 | 558 |
| A[30]# | T5 | 0.217 | HA[30]# | Y26 | 484 |
| A[31]# | U4 | 0.285 | HA[31]# | AB28 | 617 |
| Data Group 0 | | | | | |
| DSTBN[0]# | E22 | 0.338 | HDSTBN[0]# | J28 | 763 |
| DSTBP[0]# | F21 | 0.326 | HDSTBP[0]# | K27 | 662 |
| D[0]# | B21 | 0.414 | HD[0]# | K22 | 329 |
| D[1]# | B22 | 0.475 | HD[1]# | H27 | 620 |
| D[2]# | A23 | 0.538 | HD[2]# | K25 | 438 |
| D[3]# | A25 | 0.608 | HD[3]# | L24 | 387 |
| D[4]# | C21 | 0.386 | HD[4]# | J27 | 600 |
| D[5]# | D22 | 0.386 | HD[5]# | G28 | 693 |
| D[6]# | B24 | 0.535 | HD[6]# | L27 | 518 |
| D[7]# | C23 | 0.464 | HD[7]# | L23 | 329 |
| D[8]# | C24 | 0.515 | HD[8]# | L25 | 458 |
| D[9]# | B25 | 0.590 | HD[9]# | J24 | 438 |
| D[10]# | G22 | 0.274 | HD[10]# | H25 | 504 |
| D[11]# | H21 | 0.203 | HD[11]# | K23 | 319 |
| D[12]# | C26 | 0.589 | HD[12]# | G27 | 620 |
| D[13]# | D23 | 0.462 | HD[13]# | K26 | 494 |
| D[14]# | J21 | 0.183 | HD[14]# | J23 | 393 |
| D[15]# | D25 | 0.550 | HD[15]# | H26 | 554 |
| DBI[0]# | E21 | 0.309 | DINV[0]# | J25 | 514 |

| Processor lengths | | | GMCH Lengths | | |
|---|---|---|---|---|---|
| **Data Group 1** | | | | | |
| DSTBN[1]# | K22 | 0.301 | HDSTBN[1]# | C27 | 788 |
| DSTBP[1]# | J23 | 0.306 | HDSTBP[1]# | D26 | 736 |
| D[16]# | H22 | 0.272 | HD[16]# | F25 | 593 |
| D[17]# | E24 | 0.480 | HD[17]# | F26 | 634 |
| D[18]# | G23 | 0.358 | HD[18]# | B27 | 834 |
| D[19]# | F23 | 0.418 | HD[19]# | H23 | 412 |
| D[20]# | F24 | 0.443 | HD[20]# | E27 | 714 |
| D[21]# | E25 | 0.508 | HD[21]# | G25 | 522 |
| D[22]# | F26 | 0.513 | HD[22]# | F28 | 731 |
| D[23]# | D26 | 0.597 | HD[23]# | D27 | 766 |
| D[24]# | L21 | 0.176 | HD[24]# | G24 | 493 |
| D[25]# | G26 | 0.524 | HD[25]# | C28 | 837 |
| D[26]# | H24 | 0.412 | HD[26]# | B26 | 815 |
| D[27]# | M21 | 0.171 | HD[27]# | G22 | 453 |
| D[28]# | L22 | 0.245 | HD[28]# | C26 | 768 |
| D[29]# | J24 | 0.401 | HD[29]# | E26 | 691 |
| D[30]# | K23 | 0.313 | HD[30]# | G23 | 464 |
| D[31]# | H25 | 0.473 | HD[31]# | B28 | 914 |
| DBI[1]# | G25 | 0.458 | DINV[1]# | E25 | 628 |
| **Data Group 2** | | | | | |
| DSTBN[2]# | K22 | 0.252 | HDSTBN[2]# | E22 | 538 |
| DSTBP[2]# | J23 | 0.266 | HDSTBP[2]# | E21 | 502 |
| D[32]# | M23 | 0.300 | HD[32]# | B21 | 664 |
| D[33]# | N22 | 0.226 | HD[33]# | G21 | 501 |
| D[34]# | P21 | 0.178 | HD[34]# | C24 | 683 |
| D[35]# | M24 | 0.371 | HD[35]# | C23 | 675 |
| D[36]# | N23 | 0.271 | HD[36]# | D22 | 633 |
| D[37]# | M26 | 0.454 | HD[37]# | C25 | 747 |
| D[38]# | N26 | 0.437 | HD[38]# | E24 | 619 |
| D[39]# | N25 | 0.383 | HD[39]# | D24 | 655 |
| D[40]# | R21 | 0.165 | HD[40]# | G20 | 358 |
| D[41]# | P24 | 0.343 | HD[41]# | E23 | 608 |
| D[42]# | R25 | 0.381 | HD[42]# | B22 | 828 |
| D[43]# | R24 | 0.329 | HD[43]# | B23 | 726 |

| Processor lengths | | | GMCH Lengths | | |
|---|---|---|---|---|---|
| D[44]# | T26 | 0.420 | HD[44]# | F23 | 563 |
| D[45]# | T25 | 0.380 | HD[45]# | F21 | 460 |
| D[46]# | T22 | 0.221 | HD[46]# | C20 | 647 |
| D[47]# | T23 | 0.279 | HD[47]# | C21 | 654 |
| DBI[2]# | P26 | 0.441 | DINV[2]# | B25 | 784 |
| **Data Group 3** | | | | | |
| DSTBN[3]# | W22 | 0.298 | HDSTBN[3]# | D18 | 505 |
| DSTBP[3]# | W23 | 0.300 | HDSTBP[3]# | E18 | 463 |
| D[48]# | U26 | 0.419 | HD[48]# | G18 | 372 |
| D[49]# | U24 | 0.324 | HD[49]# | E19 | 511 |
| D[50]# | U23 | 0.270 | HD[50]# | E20 | 548 |
| D[51]# | V25 | 0.384 | HD[51]# | G17 | 326 |
| D[52]# | U21 | 0.167 | HD[52]# | D20 | 575 |
| D[53]# | V22 | 0.252 | HD[53]# | F19 | 469 |
| D[54]# | V24 | 0.341 | HD[54]# | C19 | 598 |
| D[55]# | W26 | 0.447 | HD[55]# | C17 | 541 |
| D[56]# | Y26 | 0.454 | HD[56]# | F17 | 372 |
| D[57]# | W25 | 0.426 | HD[57]# | B19 | 649 |
| D[58]# | Y23 | 0.336 | HD[58]# | G16 | 347 |
| D[59]# | Y24 | 0.386 | HD[59]# | E16 | 490 |
| D[60]# | Y21 | 0.222 | HD[60]# | C16 | 522 |
| D[61]# | AA25 | 0.426 | HD[61]# | E17 | 431 |
| D[62]# | AA22 | 0.268 | HD[62]# | D16 | 509 |
| D[63]# | AA24 | 0.394 | HD[63]# | C18 | 579 |
| DBI[3]# | V21 | 0.202 | DINV[3]# | G19 | 431 |

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# 5. Platform Power Requirements

Please contact your Intel field representative for more information on the electrical requirements for the DC-to-DC voltage regulator for the Mobile Intel Pentium 4 processor and Intel Celeron processor.

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# 6. System Memory Design Guidelines (DDR-SDRAM)

The Intel 852GME/852GMV/852PMGMCH/MCH Double Data Rate (DDR) SDRAM system memory interface consists of SSTL-2 compatible signals. These SSTL-2 compatible signals have been divided into several signal groups: Data, Control, Command, CPC, Clock, and Feedback signals. Table 15 summarizes the different signal groupings. Refer to the *Intel® 852GME Chipset GMCH and Intel® 852PM Chipset MCH Datasheet* for details on the signals listed.

**Table 15. GMCH/MCH Chipset Memory Signal Groups**

| Group | Signal Name | Description |
|---|---|---|
| Clocks | SCK[5:0] | DDR-SDRAM Differential Clocks - (3 per SO-DIMM) |
| | SCK#[5:0] | DDR-SDRAM Inverted Differential Clocks - (3 per SO-DIMM) |
| Data | SDQ[63:0] | Data Bus |
| | SDQ[71:64] | Check Bits for ECC Function |
| | SDQS[8:0] | Data Strobes |
| | SDM[8:0] | Data Mask |
| Control | SCKE[3:0] | Clock Enable - (One per Device Row) |
| | SCS#[3:0] | Chip Select - (One per Device Row) |
| Command | SMA[12:6,3,0] | Memory Address Bus |
| | SBA[1:0] | Bank Select |
| | SRAS# | Row Address Select |
| | SCAS# | Column Address Select |
| | SWE# | Write Enable |
| CPC | SMA[5,4,2,1] | Command per Clock (SO-DIMM0) |
| | SMAB[5,4,2,1] | Command per Clock (SO-DIMM1) |
| Feedback | RCVENOUT# | Receive Enable Output (no external connection) |
| | RCVENIN# | Receive Enable Input (no external connection) |

## 6.1. Length Matching and Length Formulas

The routing guidelines presented in the following subsections define the recommended routing topologies, trace width and spacing geometries, and absolute minimum and maximum routed lengths for each signal group, all of which are recommended to achieve optimal SI and timing. In addition to the absolute length limits provided in the individual guideline tables, more restrictive length matching formulas are also provided that further restrict the minimum to maximum length range of each signal group with respect to clock, within the overall boundaries defined in the guideline tables, as required to guarantee adequate timing margins. These secondary constraints are referred to as length matching constraints and the formulas used are referred to as length matching formulas.

All signal groups except the clocks and feedback signals are length matched per slot to the DDR clocks, with the clocks themselves being length tuned to a fixed length across each SO-DIMM slot. The amount of minimum to maximum length variance allowed for each group around the clock reference length varies from signal group to signal group depending on the amount of timing variance which can be tolerated. A simple summary of the length matching formulas for each signal group is provided in the tables below.

**Table 16. Intel 852GME/852GMV/852PMChipset GMCH/MCH DDR 333 Length Matching Formulas**

| Signal Group | Minimum Length | Maximum Length |
|---|---|---|
| Control to Clock | Clock –2.0” | Clock - 0.5” |
| Command to Clock | Clock – 2.0” | Clock + 2.0” |
| CPC to Clock | Clock – 2.0” | Clock - 1.0” |
| Strobe to Clock | Clock – 2.0” | Clock + 0.5” |
| Data to Strobe | Strobe – 25 mils | Strobe + 25 mils |

**NOTES:**
1. All length matching formulas are based on GMCH/MCH die-pad to SO-DIMM connector pin total length.
2. Backward compatible and supports DDR200 and DDR266
3. Package length tables are provided for all signals in order to facilitate this pad to pin matching. Note that the clock length used for length matching may vary by SO-DIMM slot, based on SO-DIMM spacing. Length formulas should be applied to each SO-DIMM slot independently. An offset of up to 1.0 inch between clock groups is allowed under the guidelines. The full geometry and routing guidelines along with the exact length matching formulas and associated diagrams are provided in the individual signal group guidelines sections to follow.

## 6.2. Package Length Compensation

As mentioned in Section 6.1, all length matching is done GMCH/MCH die-pad to SO-DIMM pin. The reason for this is to compensate for the package length variation across each signal group. The GMCH/MCH does not equalize package lengths internally as some previous GMCH/MCH components have, and therefore, the GMCH/MCH requires length matching.

Package length compensation should not be confused with length matching as discussed in the previous section. Length matching refers to constraints on the min and max length bounds of a signal group based on clock length, whereas package length compensation refers to the process of compensating for package length variance across a signal group. There is of course some overlap in that both affect the target length of an individual signal. It is recommended that the initial route be completed based on the

length matching formulas in conjunction with nominal package lengths and that package length compensation be performed as secondary operation.

## 6.3. Topologies and Routing Guidelines

The GMCH/MCH DDR SDRAM system memory interface implements the low swing, high-speed, terminated SSTL_2 topology. This section contains information on the recommended interconnect topologies and routing guidelines for each of the signal groups that comprise the DDR interface. When implemented as defined, these guidelines provide a robust DDR solution on a GMCH/MCH chipset based design.

### 6.3.1. Clock Signals – SCK[5:0], SCK#[5:0]

The clock signal group includes the differential clock pairs SCK/SCK#[5:0]. The GMCH/MCH generates and drives these differential clock signals required by the DDR interface; therefore, no external clock driver is required for the DDR interface. The GMCH/MCH only supports unbuffered DDR SO-DIMMs; three differential clock pairs are routed to each SO-DIMM connector. Table 17 summarizes the clock signal mapping.

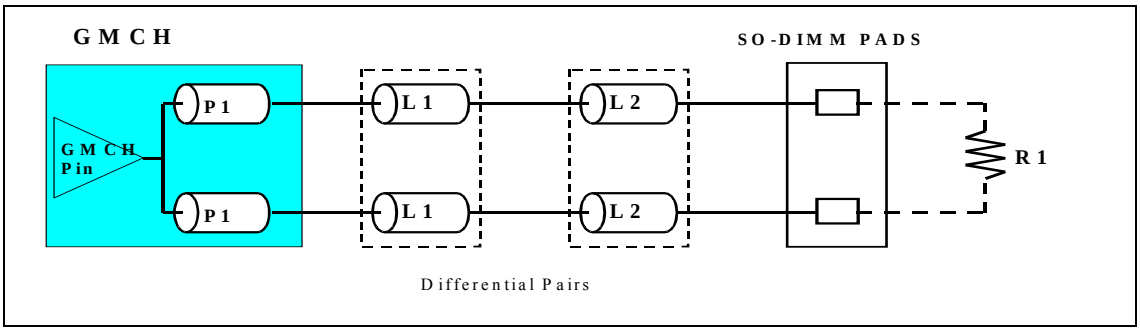
**Table 17. Clock Signal Mapping**

| Signal | Relative To |
|---|---|
| SCK/SCK#[2:0] | SO-DIMM0 |
| SCK/SCK#[5:3] | SO-DIMM1 |

#### 6.3.1.1. Clock Topology Diagram

The GMCH/MCH provides six differential clock output pairs, or three clock pairs per SO-DIMM socket. The motherboard clock routing topology is shown below for reference. Refer to the routing guidelines in Figure 20 for detailed length and spacing rules for each segment. The clock signals should be routed as closely coupled differential pairs over the entire length. Spacing to other DDR signals should not be less than 20 mils. Isolation spacing to non-DDR signals should be 25 mils.

**Figure 20. Memory Clock Routing Topology SCK/SCK#[5:0]**



### 6.3.1.2. Memory Clock Routing Guidelines

**Table 18. Clock Signal Group Routing Guidelines**

| Parameter | Definition |
|---|---|
| Signal Group | SCK[5:0] and SCK#[5:0] |
| Topology | Differential Pair Point to Point |
| Reference Plane | Ground Referenced |
| Single Ended Trace Impedance ( Zo ) (**see note on trace width** below) | 42 +/-15% (for reference only) |
| Differential Mode Impedance (Zdiff) (**see note on trace width** below) | 70 +/- 15% (for reference only) |
| Nominal Trace Width (**see note on trace width** and exceptions for breakout region below) | Inner Layers: 7 mils<br>Outer Layers: 8 mils (pin escapes only) |
| Nominal Pair Spacing (edge to edge) (see exceptions for breakout region below) | Inner Layers: 4 mils<br>Outer Layers: 5 mils (pin escapes only) |
| Minimum Pair to Pair Spacing (see exceptions for breakout region below) | 20 mils |
| Minimum Serpentine Spacing | 20 mils |
| Minimum Spacing to Other DDR Signals (see exceptions for breakout region below) | 20 mils |
| Minimum Isolation Spacing to non-DDR Signals | 25 mils |
| Maximum Via Count | 2 (per side) |
| Package Length Range – P1 | 1000 mils +/- 350 mils (Refer to Table 19 for exact lengths.) |
| Trace Length Limits – L1 | Max = 300 mils (breakout segment) |
| Total MB Length Limits – L1 + L2 | Min = 0.5”<br>Max = 5.0” |
| Total Length – P1 + L1 + L2 | Total length target is determined by placement (see Figure 20)<br>Total length for SO-DIMM0 group = X0 (see Figure 21)<br>Total length for SO-DIMM1 group = X1 (see Figure 21) |
| SCK to SCK# Length Matching | Match total length to +/- 10 mils (see Section 6.3.1.3) |
| Clock to Clock Length Matching (Total Length) | Match all SO-DIMM0 clocks to X0 +/- 25 mils (see Figure 21)<br>Match all SO-DIMM1 clocks to X1 +/- 25 mils (see Figure 21) |
| **Breakout Exceptions**<br>(Reduced geometries for GMCH/MCH breakout region) | Inner Layers: 4 mil trace, 4 mil pair space allowed<br>Outer Layers: 5 mil trace, 5 mil pair space allowed<br>Pair to pair spacing of 5 mils allowed<br>Spacing to other DDR signals of 5 mils allowed<br>Maximum breakout length is 0.3” |

**NOTES:**

1. Pad to pin length tuning is utilized on clocks in order to achieve minimal variance. Package lengths range between approximately 600 mils and 1400 mils. Exact package lengths for each clock signal are provided at the end of this section. Overall target length should be established based on placement and routing flow. The resulting motherboard segment lengths must fall within the ranges specified.
2. The DDR clocks should be routed on internal layers, except for pin escapes. It is recommended that pin escape vias be located directly adjacent to the ball pads on all clocks. Surface layer routing should be minimized.

3. Clock differential impedance is controlled indirectly through the single ended impedance specification for the board. Clock signal integrity and edge rates are improved when clock trace widths are widened from the standard 55 Ω single ended trace width. As the table indicates, a trace width of approximately 3 mils wider than standard width was found to be optimal (i.e. inner layers: 4 mils std + 3 mils = 7 mils). The nominal single ended impedance of the widened clock traces is in the range of 42 Ω, and the nominal differential impedance is in the range of 70 Ω. However, impedance control is implemented through geometry control; these values are for reference only.
4. Exceptions to the trace width and spacing geometries are allowed in the breakout region in order to fan-out the interconnect pattern. Reduced spacing should be avoided as much as possible.

#### 6.3.1.3. Clock Length Matching Requirements

The GMCH/MCH chipset provides three differential clock pair for each SO-DIMM. A differential clock pair is made up of a SCK signal and its complement signal SCK#. Refer to Section 6.1 for more details on length matching requirements.

The differential pairs for one SO-DIMM are:

SCK[0] / SCK#[0]
SCK[1] / SCK#[1]
SCK[2] / SCK#[2]

The differential pairs for the second SO-DIMM are:

SCK[3] / SCK#[3]
SCK[4] / SCK#[4]
SCK[5] / SCK#[5]

The two sets of differential clocks must be length tuned on the motherboard such that any pair to pair package length variation is tuned out. The three pairs associated with SO-DIMM0 are tuned to a fixed overall length, including package, and the three pairs associated with SO-DIMM1 are tuned to a fixed overall length.

The two traces associated with each clock pair are length matched within the package; however some additional compensation may be required on the motherboard in order to achieve the ± 10 mil length tolerance within the pair.

Between clock pairs the package length varies substantially. Therefore, the motherboard length of each clock pair must be length adjusted to tune out package variance. The total length including package should be matched to within ± 25 mils of each other, as shown in Figure 21. This may result in a clock length variance of as much as 700 mils on the motherboard.

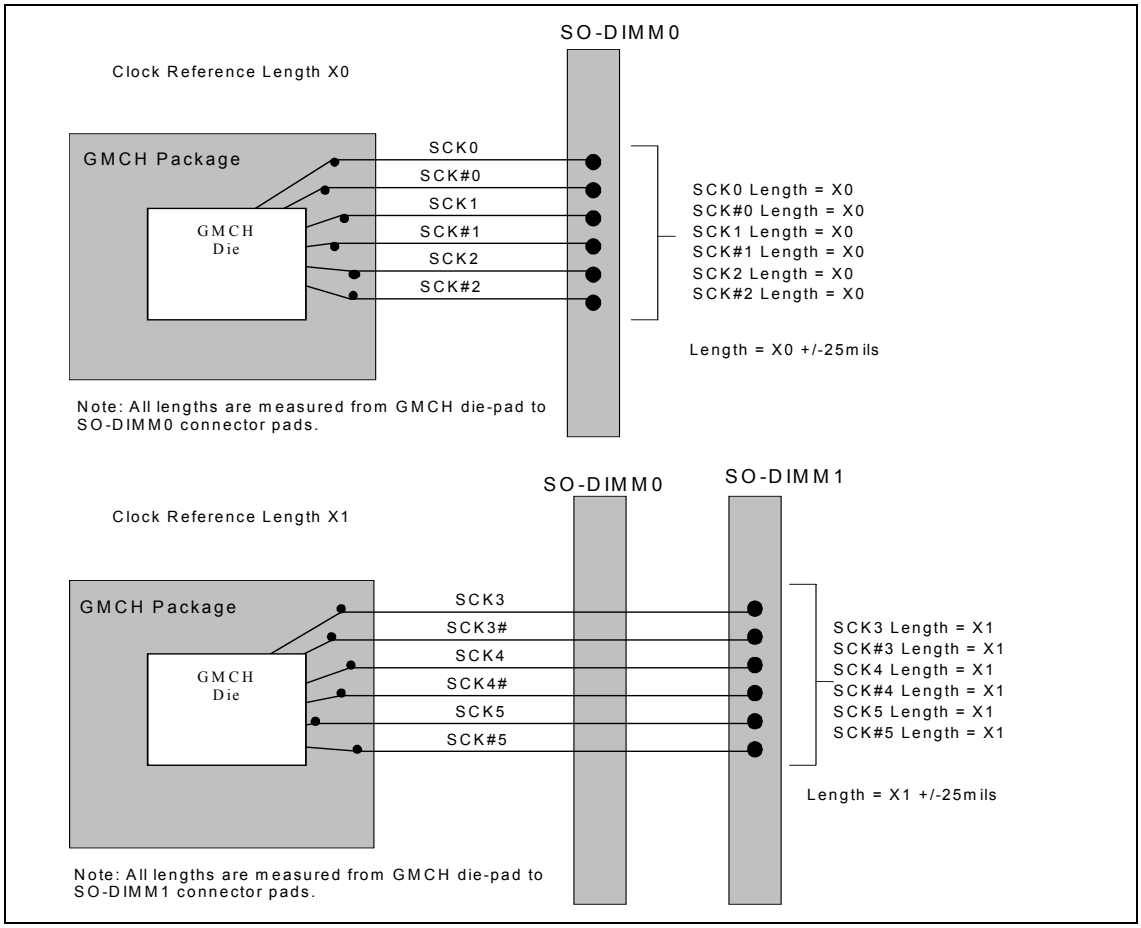
The first step in determining the routing lengths for clocks and all other clock relative signal groups is to establish the target length for each SO-DIMM clock group. These target lengths are shown as X0 and X1, in Figure 21. These are the lengths to which all clocks within the corresponding group will be matched and the reference length values used to calculate the length ranges for the other signal groups.

### 6.3.1.4. Clock Reference Lengths

The clock reference length for each SO-DIMM clock group is determined by first determining the longest total clock length required to complete the clock routing. A table of clock package lengths is provided in Table 19 to assist in this calculation. Once the longest total length is determined for each clock group, this becomes a lower bound for the associated clock reference length. At this point it is helpful to have completed a test route of the SDQ/SDQS bus such that final clock reference lengths can be defined with consideration of the impact on SDQ/SDQS bus routability. Some iteration may be required.

Once the reference lengths X0 and X1 are defined then the next step is to tune each clock pairs' motherboard trace segment lengths as required such that the overall length of each clock equals the associated clock reference length plus or minus the 25 mil tolerance. Again, the reference length for the two sets of clocks should be offset by the nominal routing length between SO-DIMM connectors.

**Figure 21. Memory Clock Trace Length Matching Diagram**



### 6.3.1.5. Clock Package Length Table

The package length data in the table below should be used to tune the motherboard length of each SCK/SCK# clock pair between the GMCH/MCH and the associated SO-DIMM socket. It is recommended that die-pad to SO-DIMM pin length be tuned to within ± 25 mils in order to optimize timing margins on the interface.

**Table 19. Memory Clock Package Lengths**

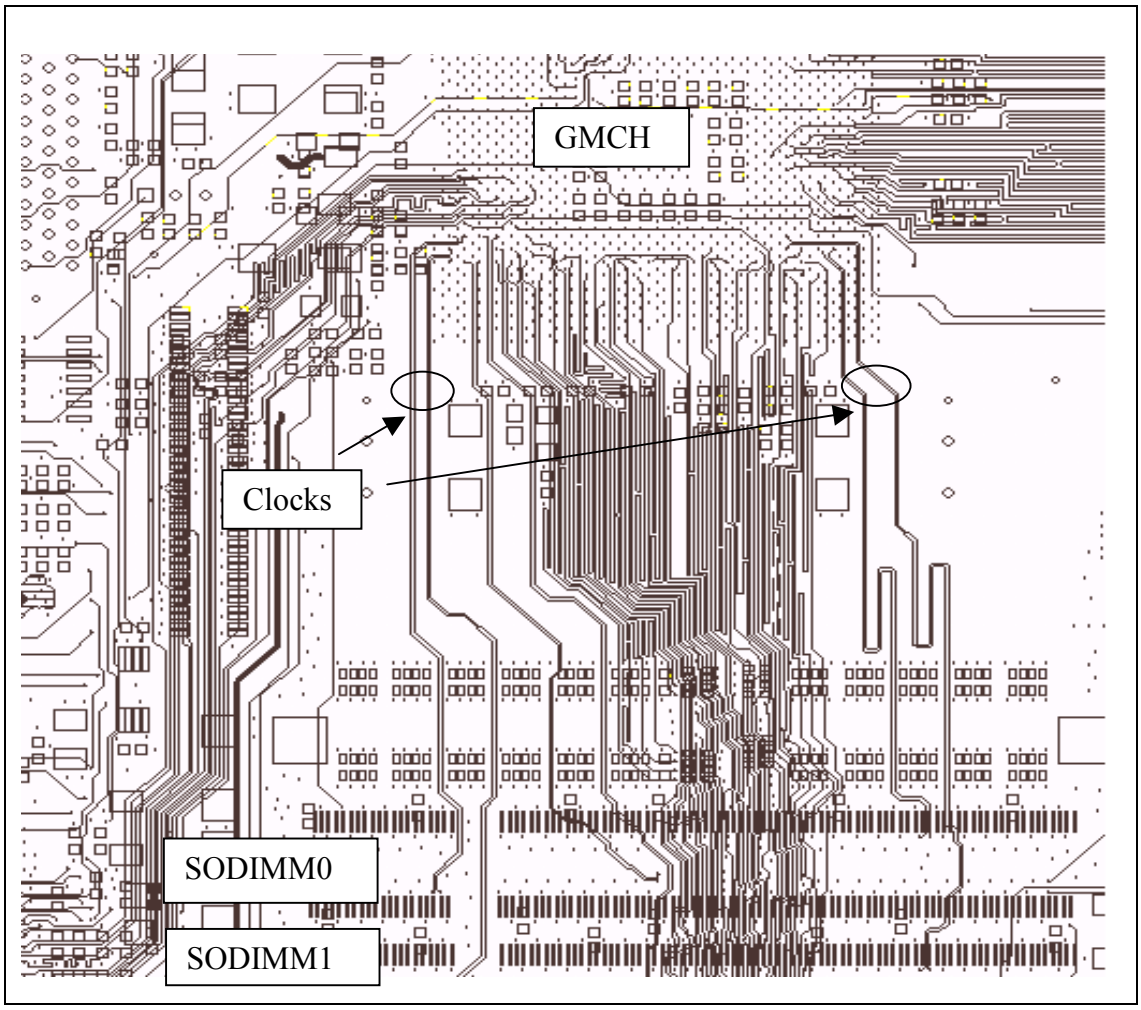
| Signal | Pin Number | Package Length (mils) |
|---|---|---|
| SCK_0 | AB2 | 1177 |
| SCK#_0 | AA2 | 1169 |
| SCK_1 | AC26 | 840 |
| SCK#_1 | AB25 | 838 |
| SCK_2 | AC3 | 1129 |
| SCK#_2 | AD4 | 1107 |
| SCK_3 | AC2 | 1299 |
| SCK#_3 | AD2 | 1305 |
| SCK_4 | AB23 | 643 |
| SCK#_4 | AB24 | 656 |
| SCK_5 | AA3 | 1128 |
| SCK#_5 | AB4 | 1146 |

Package length compensation can be performed on each individual clock output thereby matching total length on SCK/SCK# exactly, or alternatively the average package length can be used for both outputs of a pair and length tuning done with respect to the motherboard portion only.

### 6.3.1.6. Clock Routing Example

Figure 22 is an example of a board routing for the clock signal group.

**Figure 22. Clock Signal Routing Example**




## 6.3.2. Data Signals – SDQ[71:0], SDM[8:0], SDQS[8:0]

The GMCH/MCH data signals are source synchronous signals that include a 72-bit wide data bus, which includes 8 check bits for Error Checking and Correction (ECC), a set of 9 Data Mask bits, and a set of 9 data strobe signals. There is an associated data strobe and data mask bit for each of the 8-bit, data byte groups, making for a total of nine, 10-bit byte lanes. This section summarizes the SDQ/SDM to SDQS routing guidelines and length matching recommendations.

The data signals include SDQ[71:0], SDM[8:0], and SDQS[8:0]. The data signals should transition from an external layer to an internal signal layer under the GMCH/MCH. Keep to the same internal layer until transitioning back to an external layer at the series resistor. After the series resistor, the signal should transition from the external layer to the same internal layer and route to SO-DIMM0. At SO-DIMM0,

the signal should transition to an external layer and connect to the appropriate pad of the connector. After the SO-DIMM0 transition, continue to route the signal on the same internal layer to SO-DIMM1. Transition back out to an external layer and connect to the appropriate pad of SO-DIMM1. Connection to the termination resistor should be via the same internal layer with a transition back to the external layer near the resistor. External trace lengths should be minimized.

To facilitate routing, swapping of the byte lanes is allowed for SDQ[63:0] only. Bit swapping within the byte lane is also allowed for SDQ[63:0] only. The check bits, SDQ[71:64], cannot be byte lane swapped with another SDQ byte lane. Also, bit swapping within the SDQ[71:64] byte lane is not allowed. It is suggested that the parallel termination be placed on both sides of SO-DIMM1 to simplify routing and minimize trace lengths. All internal and external signals should be ground referenced to keep the path of the return current continuous.

Resistor packs are acceptable for the series (Rs) and parallel (Rt) data and strobe termination resistors, but data and strobe signals can't be placed within the same R pack as the command or control signals. The table and diagrams below depict the recommended topology and layout routing guidelines for the DDR-SDRAM data signals.

Intel recommends that the full data bus SDQ[71:0], mask bus SDM[8:0], and strobe signals SDQS[8:0] be routed on the same internal signal layer. It is required that the SDQ byte group and the associated SDM and SDQS signals within a byte lane be routed on the same internal layer.

The total length of SDQ, SDM, and SDQS traces between the GMCH/MCH and the SO-DIMMs must be within the range defined in the overall guidelines, and is also constrained by a length range boundary based on SCK/SCK# clock length, and a SDQ/SDM to SDQS length matching requirement within each byte lane. Note also that all length matching must be done inclusive of package length. A table of SDQ, SDM, and SDQS package lengths is provided at the end of this Section to facilitate this process.

There are two levels of matching implemented on the data bus signals.

The first is the length range constraint on the SDQS signals based on clock reference length.

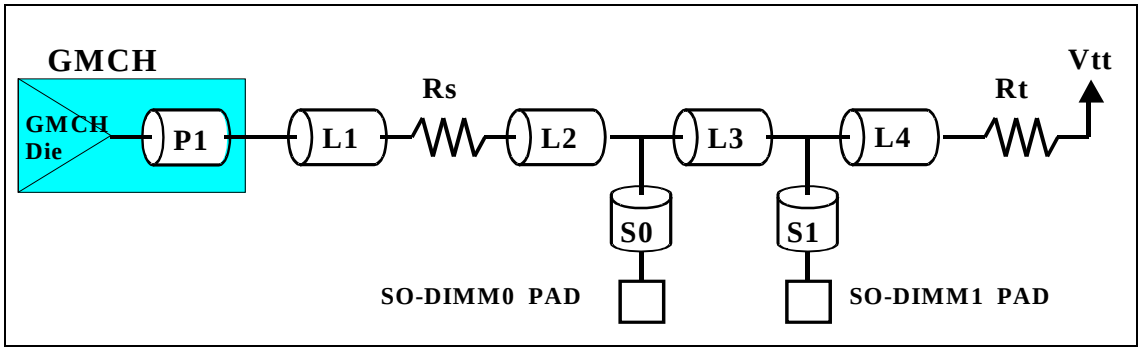
The second is SDQ/SDM to SDQS length matching within a byte lane.

The length of the SDQS signal for each byte lane must fall within a range determined by the clock reference length, as defined in the SDQS to SCK/SCK length matching section. The actual length of SDQS for each byte lane may fall anywhere within this range based on placement and routing flow.

Once the SDQS length for a byte lane is established, the SDQ and SDM signals within the byte lane must be length matched to each other, inclusive of package length, as described in the SDQ to SDQS length matching Section 6.3.2.3.

### 6.3.2.1. Data Bus Topology

**Figure 23. Data Signal Routing Topology**




The data signals should be routed using a 2 to 1 trace spacing to trace width ratio for signals within the DDR group, except clocks and strobes. There should be a minimum of 20 mils of spacing to non-DDR related signals. Data signals should be routed on inner layers with minimized external trace lengths.

**Table 20. Intel 852GME Chipset GMCH/MCH Memory Data Signal Group Routing Guidelines**

| Parameter | Definition |
|---|---|
| Signal Group | SDQ[71:0], SDQS[8:0], SDM[8:0] |
| Motherboard Topology | Daisy Chain with Parallel Termination |
| Reference Plane | Ground Referenced |
| Characteristic Trace Impedance (Zo) | 55 +/- 15% |
| Nominal Trace Width | Inner layers: 4 mils<br>Outer layers: 5 mils |
| Minimum Spacing to Trace Width Ratio | SDQ/SDM: 2 to 1 (e.g. 8 mil space to 4 mil trace)<br>SDQS: 3 to 1 (e.g. 12 mil space to 4 mil trace) |
| Minimum Isolation Spacing to non-DDR Signals | 20 mils |
| Package Length P1 | 700 mils +/- 300 mils (See Table 22 for details) |
| Trace Length L1 – GMCH/MCH Signal Ball to Series Termination Resistor Pad | Min = 0.5”<br>Max = 3.75” |
| Trace Length L2 – Series Termination Resistor Pad to First SO-DIMM Via | Max = 0.75” |
| Stub Length S0, S1 – Stub from Via to SO-DIMM Pad | Max = 0.25” |
| Total Length L1 + L2 + S0 – Total Length from GMCH/MCH to First SO-DIMM Pad | Min = 0.5”<br>Max = 4.0” |
| Total Length L1 + L2 + L3 + S1 – Total Length from GMCH/MCH to Second SO-DIMM Pad | Min = 0.75”<br>Max = 4.5” |
| Total Length S0 + L3 + S1– Total SO-DIMM pad to SO-DIMM pad spacing | Min = 0.25”<br>Max = 1.0” |

| Parameter | Definition |
|---|---|
| Trace Length L4 – Last SO-DIMM Via to Parallel Termination Resistor Pad | Max = 1.0” |
| Series Termination Resistor (Rs) | 10 ± 5% |
| Parallel Termination Resistor (Rt) | 56 ± 5% |
| Length Matching Requirements | SDQS to SCK/SCK# See length matching Section 6.3.2.2<br>SDQ/SDM to SDQS, to +/- 25mils, within each byte lane |

**NOTES:**
1. Power distribution vias from Rt to Vtt are not included in this count.
2. The overall minimum and maximum length to the SO-DIMM must comply with clock length matching requirements.
3. It is possible to route using 4 vias if trace segments L2 and L4 are routed on the same external layer as the associated SO-DIMM, for example if L2 is on the same layer as SO-DIMM0.

### 6.3.2.2. SDQS to Clock Length Matching Requirements

The first step in length matching is to determine the SDQS length range based on the SCK/SCK# reference length defined previously. The total length of the SDQS strobe signals, including package length, between the GMCH/MCH die-pad and the SO-DIMMs must fall within the range defined in the formulas below. See the clock Section for the definition of the clock reference length. Refer to Figure 23 for the definition of the various trace segments. The length tuning requirements are also depicted in Figure 24. Refer to Section 6.1 for more details on length matching and length formula requirements.

**Length range formula for SO-DIMM0:**

$X_0$ = SCK/SCK#[2:0] total reference length, including package length

$Y_0$ = SDQS[8:0] total length = GMCH/MCH package + L1 + L2 + S0, as shown in Figure 24,

where: ( $X_0$ – 2.0” ) $Y_0$ ( $X_0$ + 0.5” ) for DDR 200/266/333

**Length range formula for SO-DIMM1,**

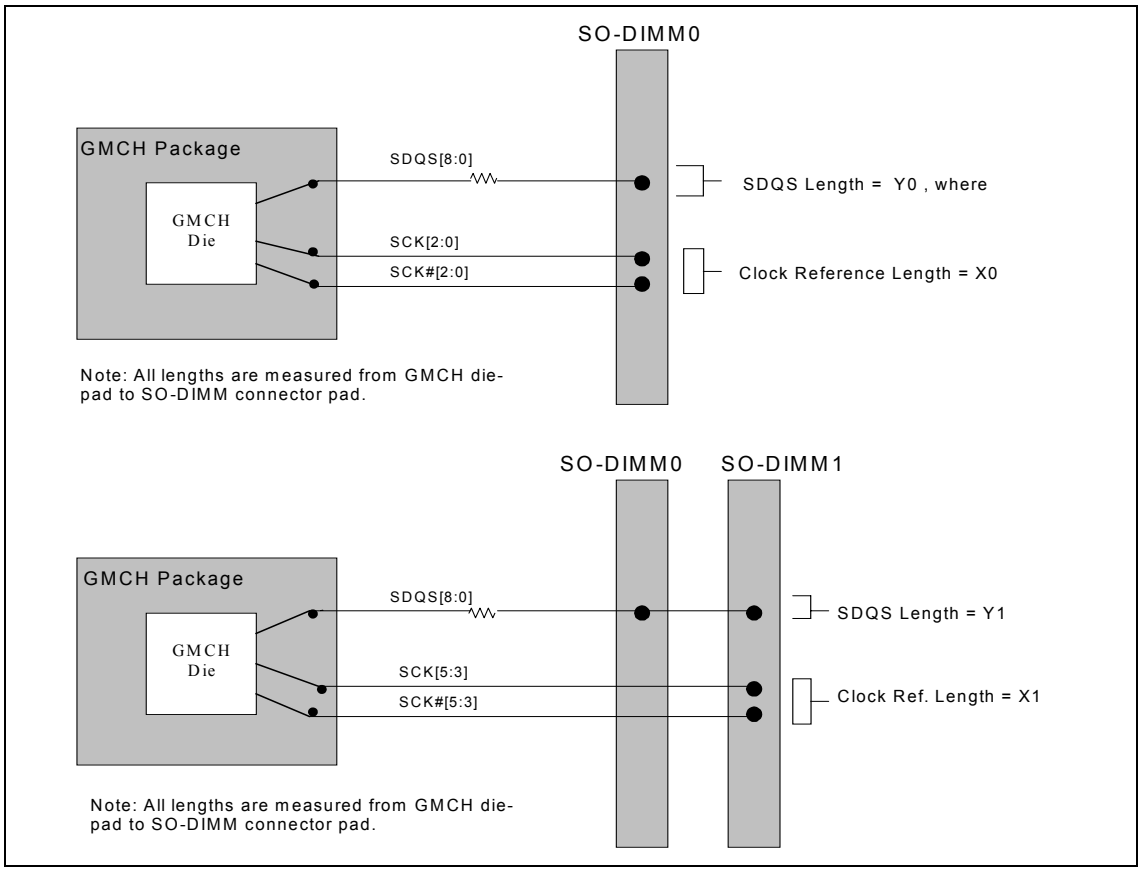
$X_1$ = SCK/SCK#[5:3] total reference length, including package length

$Y_1$ = SDQS[8:0] total length = GMCH/MCH package + L1 + L2 + L3 + S1, as shown Figure 24,

where: ( $X_0$ – 2.0” ) $Y_0$ ( $X_0$ + 0.5” ) for DDR 200/266/333

Length matching is only performed from the GMCH/MCH to the SO-DIMMs, and does not involve the length of L4, which can vary over its entire range. Intel recommends that routing segment length L3 between SO-DIMM0 to SO-DIMM1 be held fairly constant and equal to the offset between clock reference lengths X0 and X1. This will produce the most straightforward length-matching scenario. Note that a nominal SDQS package length of 750 mils can be used to estimate MB lengths prior to performing package length compensation. Refer to Section 6.2 for more details on package length compensation.

**Figure 24. SDQS to Clock Trace Length Matching Diagram**



### 6.3.2.3. Data to Strobe Length Matching Requirements

The data bit signals, SDQ[71:0] are grouped by byte lanes and associated with a data mask signal SDM[8:0], and a data strobe, SDQS[8:0].

The data and mask signals must be length matched to their associated strobe within ± 25 mils, including package.

For SO-DIMM0 this length matching includes the motherboard trace length to the pads of the SO-DIMM0 connector (L1 + L2 + S0) plus package length.

For SO-DIMM1, the motherboard trace length to the pads of the SO-DIMM1 connector (L1 + L2 + L3 + S1) plus package length.

Refer to Section 6.2 for more details on package length compensation.

**Length range formula for SDQ and SDM,**

**X** = SDQS total length, including package length, as defined previously

**Y** = SDQ, SDM total length, including package length, within same byte lane as show in Figure 25,

where: ( X – 25 mils ) Y ( X + 25 mils )

Length matching is not required from the SO-DIMM1 to the parallel termination resistors. Figure 25 on the following page depicts the length matching requirements between the SDQ, SDM, and SDQS signals within a byte lane. Byte lane mapping is defined in Table 21 below.

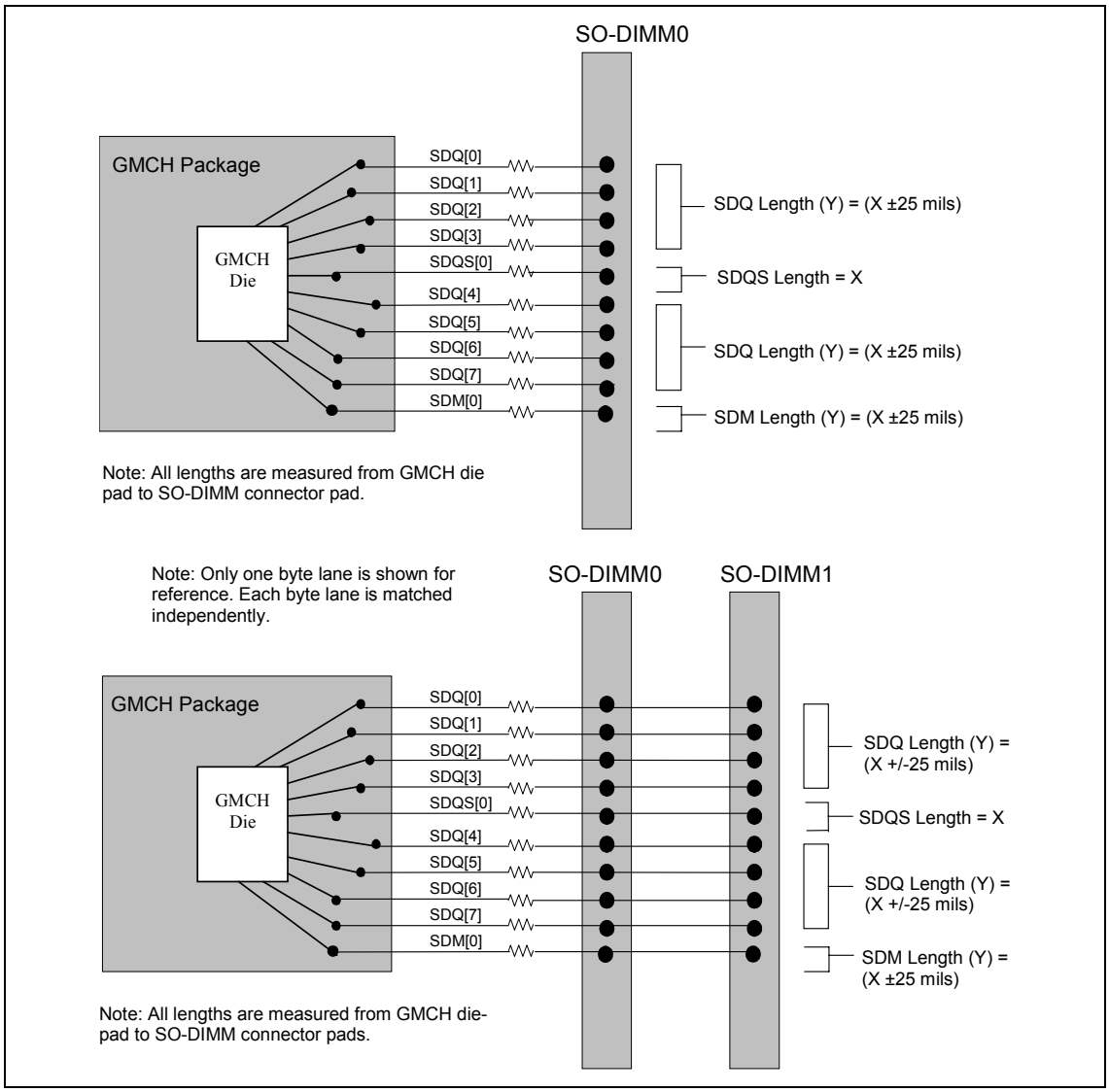
### 6.3.2.4. SDQ to SDQS Mapping

Table 21 below defines the mapping between the nine byte lanes, nine mask bits, and the nine SDQS signals, as required to do the required length matching.

**Table 21. SDQ/SDM to SDQS Mapping**

| Signal | Mask | Relative To |
|---|---|---|
| SDQ[7:0] | SDM[0] | SDQS[0] |
| SDQ[15:8] | SDM[1] | SDQS[1] |
| SDQ[23:16] | SDM[2] | SDQS[2] |
| SDQ[31:24] | SDM[3] | SDQS[3] |
| SDQ[39:32] | SDM[4] | SDQS[4] |
| SDQ[56:40] | SDM[5] | SDQS[5] |
| SDQ[55:48] | SDM[6] | SDQS[6] |
| SDQ[63:56] | SDM[7] | SDQS[7] |
| SDQ[71:64] | SDM[8] | SDQS[8] |

**Figure 25. SDQ/SDM to SDQS Trace Length Matching Diagram**



### 6.3.2.5. SDQ/SDQS Signal Package Lengths

The package length data in Table 22 below should be used to tune the length of each SDQ, SDM, and SDQS motherboard trace as required to achieve the overall length matching requirements defined in the prior sections.

**Table 22. Memory SDQ/SDM/SDQS Package Lengths**

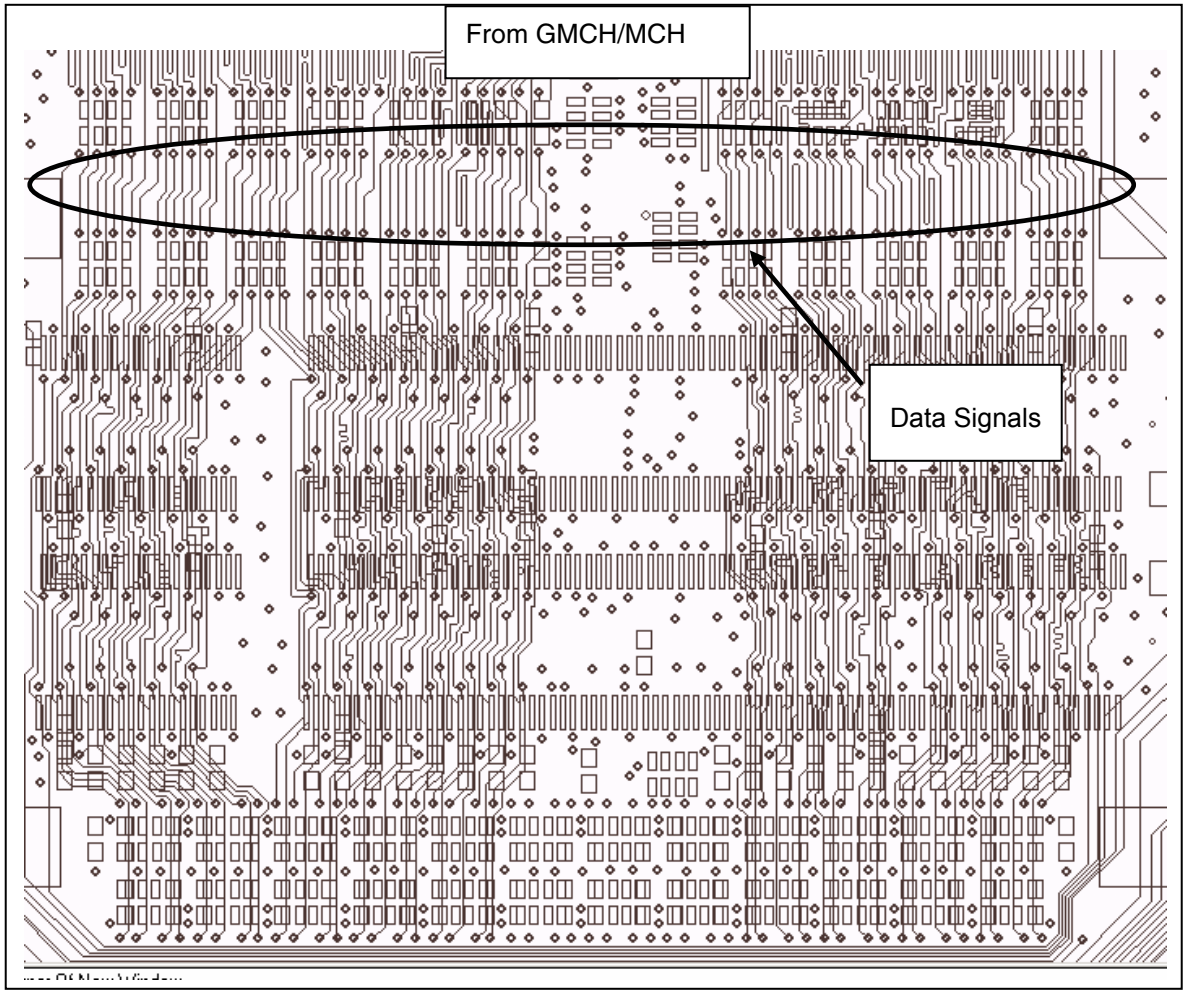
| Signal | Pin Number | Pkg Length (mils) | Signal | Pin Number | Pkg Length (mils) | Signal | Pin Number | Pkg Length (mils) |
|---|---|---|---|---|---|---|---|---|
| SDQ_00 | AF2 | 785 | SDQ_24 | AH10 | 648 | SDQ_48 | AE23 | 592 |
| SDQ_01 | AE3 | 751 | SDQ_25 | AH11 | 622 | SDQ_49 | AH23 | 752 |
| SDQ_02 | AF4 | 690 | SDQ_26 | AG13 | 572 | SDQ_50 | AE24 | 666 |
| SDQ_03 | AH2 | 903 | SDQ_27 | AF14 | 655 | SDQ_51 | AH25 | 817 |
| SDQ_04 | AD3 | 682 | SDQ_28 | AG11 | 599 | SDQ_52 | AG23 | 639 |
| SDQ_05 | AE2 | 739 | SDQ_29 | AD12 | 460 | SDQ_53 | AF23 | 667 |
| SDQ_06 | AG4 | 741 | SDQ_30 | AF13 | 536 | SDQ_54 | AF25 | 707 |
| SDQ_07 | AH3 | 845 | SDQ_31 | AH13 | 642 | SDQ_55 | AG25 | 783 |
| SDQ_08 | AD6 | 607 | SDQ_32 | AH16 | 766 | SDQ_56 | AH26 | 834 |
| SDQ_09 | AG5 | 756 | SDQ_33 | AG17 | 558 | SDQ_57 | AE26 | 701 |
| SDQ_10 | AG7 | 685 | SDQ_34 | AF19 | 510 | SDQ_58 | AG28 | 808 |
| SDQ_11 | AE8 | 558 | SDQ_35 | AE20 | 579 | SDQ_59 | AF28 | 756 |
| SDQ_12 | AF5 | 734 | SDQ_36 | AD18 | 408 | SDQ_60 | AG26 | 782 |
| SDQ_13 | AH4 | 825 | SDQ_37 | AE18 | 458 | SDQ_61 | AF26 | 748 |
| SDQ_14 | AF7 | 644 | SDQ_38 | AH18 | 658 | SDQ_62 | AE27 | 673 |
| SDQ_15 | AH6 | 912 | SDQ_39 | AG19 | 596 | SDQ_63 | AD27 | 608 |
| SDQ_16 | AF8 | 622 | SDQ_40 | AH20 | 677 | SDQ_64 | AG14 | 566 |
| SDQ_17 | AG8 | 624 | SDQ_41 | AG20 | 730 | SDQ_65 | AE14 | 477 |
| SDQ_18 | AH9 | 676 | SDQ_42 | AF22 | 562 | SDQ_66 | AE17 | 571 |
| SDQ_19 | AG10 | 634 | SDQ_43 | AH22 | 702 | SDQ_67 | AG16 | 530 |
| SDQ_20 | AH7 | 710 | SDQ_44 | AF20 | 563 | SDQ_68 | AH14 | 701 |
| SDQ_21 | AD9 | 508 | SDQ_45 | AH19 | 644 | SDQ_69 | AE15 | 421 |
| SDQ_22 | AF10 | 569 | SDQ_46 | AH21 | 716 | SDQ_70 | AF16 | 491 |
| SDQ_23 | AE11 | 469 | SDQ_47 | AG22 | 783 | SDQ_71 | AF17 | 530 |
| SDM_0 | AE5 | 838 | SDQS_0 | AG2 | 925 | | | |
| SDM_1 | AE6 | 693 | SDQS_1 | AH5 | 838 | | | |
| SDM_2 | AE9 | 538 | SDQS_2 | AH8 | 756 | | | |
| SDM_3 | AH12 | 606 | SDQS_3 | AE12 | 466 | | | |
| SDM_4 | AD19 | 492 | SDQS_4 | AH17 | 678 | | | |

| Signal | Pin Number | Pkg Length (mils) | Signal | Pin Number | Pkg Length (mils) | Signal | Pin Number | Pkg Length (mils) |
|---|---|---|---|---|---|---|---|---|
| SDM_5 | AD21 | 470 | SDQS_5 | AE21 | 487 | | | |
| SDM_6 | AD24 | 557 | SDQS_6 | AH24 | 770 | | | |
| SDM_7 | AH28 | 917 | SDQS_7 | AH27 | 858 | | | |
| SDM_8 | AH15 | 685 | SDQS_8 | AD15 | 418 | | | |

### 6.3.2.6. Memory Data Routing Example

Figure 26 is an example of a board routing for the Data signal group. The majority of the Data signal route is on an internal layer, both external layers can be used for parallel termination R-pack placement.

**Figure 26. Data Signals Group Routing Example**



## 6.3.3. Control Signals – SCKE[3:0], SCS#[3:0]

The GMCH/MCH control signals, SCKE[3:0] and SCS#[3:0], are clocked into the DDR SDRAM devices using clock signals SCK/SCK#[5:0]. The GMCH/MCH drives the control and clock signals together, with the clocks crossing in the valid control window. The GMCH/MCH provides one chip select (CS) and one clock enable (CKE) signal per SO-DIMM physical device row. Two chip select and two clock enable signals will be routed to each SO-DIMM. Refer to Table 23 for the CKE and CS# signal to SO-DIMM mapping.

**Table 23. Control Signal to SO-DIMM Mapping**

| Signal | Relative To | SO-DIMM Pin |
|---|---|---|
| SCS#[0] | SO-DIMM0 | AD23 |
| SCS#[1] | SO-DIMM0 | AD26 |
| SCS#[2] | SO-DIMM1 | AC22 |
| SCS#[3] | SO-DIMM1 | AC25 |
| SCKE[0] | SO-DIMM0 | AC7 |
| SCKE[1] | SO-DIMM0 | AB7 |
| SCKE[2] | SO-DIMM1 | AC9 |
| SCKE[3] | SO-DIMM1 | AC10 |

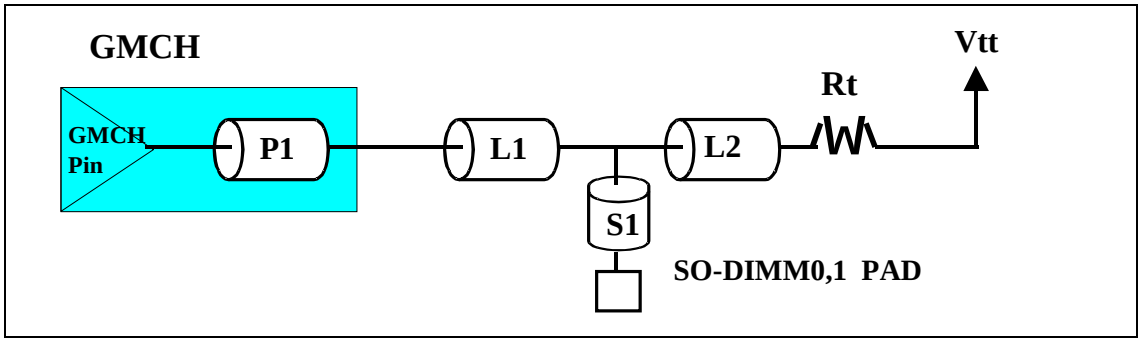
The control signal routing should transition from an external layer to an internal signal layer under the GMCH/MCH, keep to the same internal layer until transitioning back out to an external layer to connect to the appropriate pad of the SO-DIMM connector and the parallel termination resistor. If the layout requires additional routing before the termination resistor, return to the same internal layer and transition back out to an external layer immediately prior to parallel termination resistor.

External trace lengths should be minimized. Intel suggests that the parallel termination be placed on both sides of the board to simplify routing and minimize trace lengths. All internal and external signals should be ground reference to keep the path of return current continuous. Intel suggests that all control signals be routed on the same internal layer.

Resistor packs are acceptable for the parallel (Rt) control termination resistors, but control signals can not be placed within the same R pack as the data or command signals. Figure 27 and Table 24 below depict the recommended topology and layout routing guidelines for the DDR-SDRAM control signals.

### 6.3.3.1. Control Signal Topology

**Figure 27. Control Signal Routing Topology**




The control signals should be routed using 2 to 1 trace spacing to trace width ratio for signals within the DDR group, except clocks and strobes. There should be a minimum of 20-mils of spacing to non-DDR related signals. Control signals should be routed on inner layers with minimized external trace lengths.

### 6.3.3.2. Control Signal Routing Guidelines

**Table 24. Control Signal Routing Guidelines**

| Parameter | Routing Guidelines |
|---|---|
| Signal Group | SCKE[3:0], SCS#[3:0] |
| Motherboard Topology | Point-to-Point with Parallel Termination |
| Reference Plane | Ground Referenced |
| Characteristic Trace Impedance (Zo) | 55 ±15% |
| Nominal Trace Width | Inner layers: 4 mils<br>Outer layers: 5 mils |
| Minimum Spacing to Trace Width Ratio | 2 to 1 (e.g. 8 mil space to 4 mil trace) |
| Minimum Isolation Spacing to non-DDR Signals | 20 mils |
| Package Length P1 | 500 mils ± 250 mils (Refer to Table 25 for details) |
| Stub Length S1 – Stub from Via to SO-DIMM Pad | Max = 0.25” |
| Trace Length L1+S1 – Total length from GMCH/MCH Signal Ball to SO-DIMM Pad | Min = 0.5 inches<br>Max = 5.5 inches for DDR 266<br>Max = 4.5 inches for DDR 333 |
| Trace Length L2 – SO-DIMM via to Parallel Termination Resistor Pad | Max = 2.0 inches |
| Parallel Termination Resistor (Rt) | 56 ± 5% |
| Maximum Recommended Motherboard Via Count Per Signal | 3 |
| Length Matching Requirements | CTRL to SCK/SCK# [5:0] See length matching Section 6.3.3.3 and Figure 28. |

**NOTES:**
1. Recommended resistor values and trace lengths may change in a later revision of the design guide.

2. Power distribution vias from Rt to Vtt are not included in this count.
3. It is possible to route using two vias if one via is shared that connects to the SO-DIMM pad and parallel termination resistor.
4. The overall maximum and minimum length to the SO-DIMM must comply with clock length matching requirements.

### 6.3.3.3. Control to Clock Length Matching Requirements

The length of the control signals, between the GMCH/MCH die pad and the SO-DIMM must fall within the range defined below, with respect to the associated clock reference length. Refer to Figure 27 for a definition of the various trace segments that make up this path. The length of trace from the SO-DIMM to the termination resistor need not be length matched. The length matching requirements are also depicted in Figure 28. Refer to Section 6.1 for more details on length matching requirements.

**Length range formula for SO-DIMM0:**

$X_0$ = SCK/SCK#[2:0] total reference length, including package length.

$Y_0$ = SCS#[1:0] & SCKE[1:0] total length = GMCH/MCH package length + L1 + S1, as shown in Figure 28

where: ( $X_0$ – 2.0” ) $Y_0$ ( $X_0$ - 0.5” ) for DDR 200/266/33

**Length range formula for SO-DIMM1:**

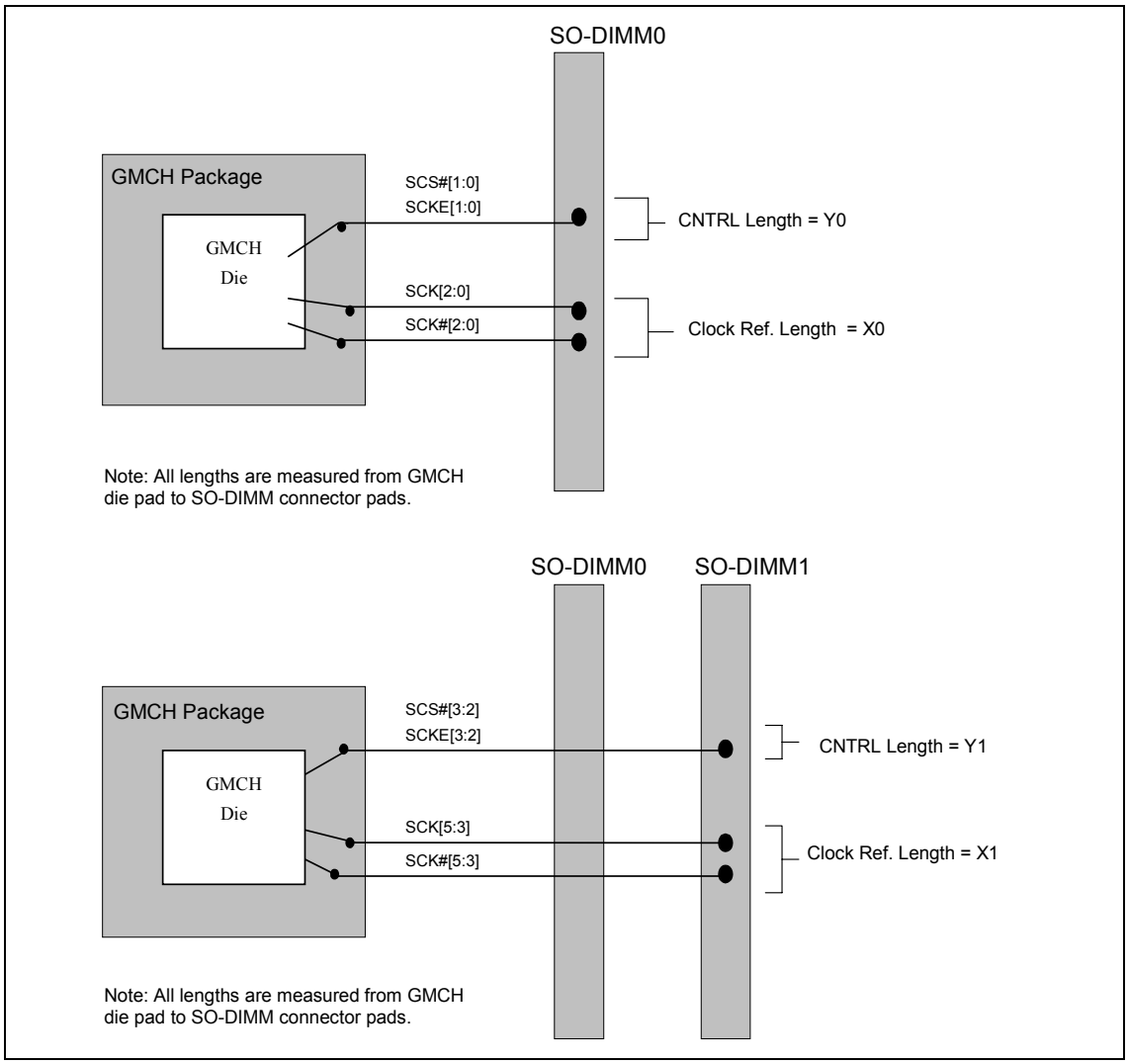
$X_1$ = SCK/SCK#[5:3] total reference length, including package length.

$Y_1$ = SCS#[3:2] & SCKE[3:2] total length = GMCH/MCH package length + L1 + S1, as shown in Figure 28,

where: ( $X_1$ – 2.0” ) $Y_1$ ( $X_1$ - 0.5” ) for DDR 200/266/33

No length matching is required from the SO-DIMM to the termination resistor. Figure 28 on the following page depicts the length matching requirements between the control signals and clock. A nominal CS/CKE package length of 500 mils can be used to estimate baseline MB lengths. Refer to Section 6.2 for more details on package length compensation.

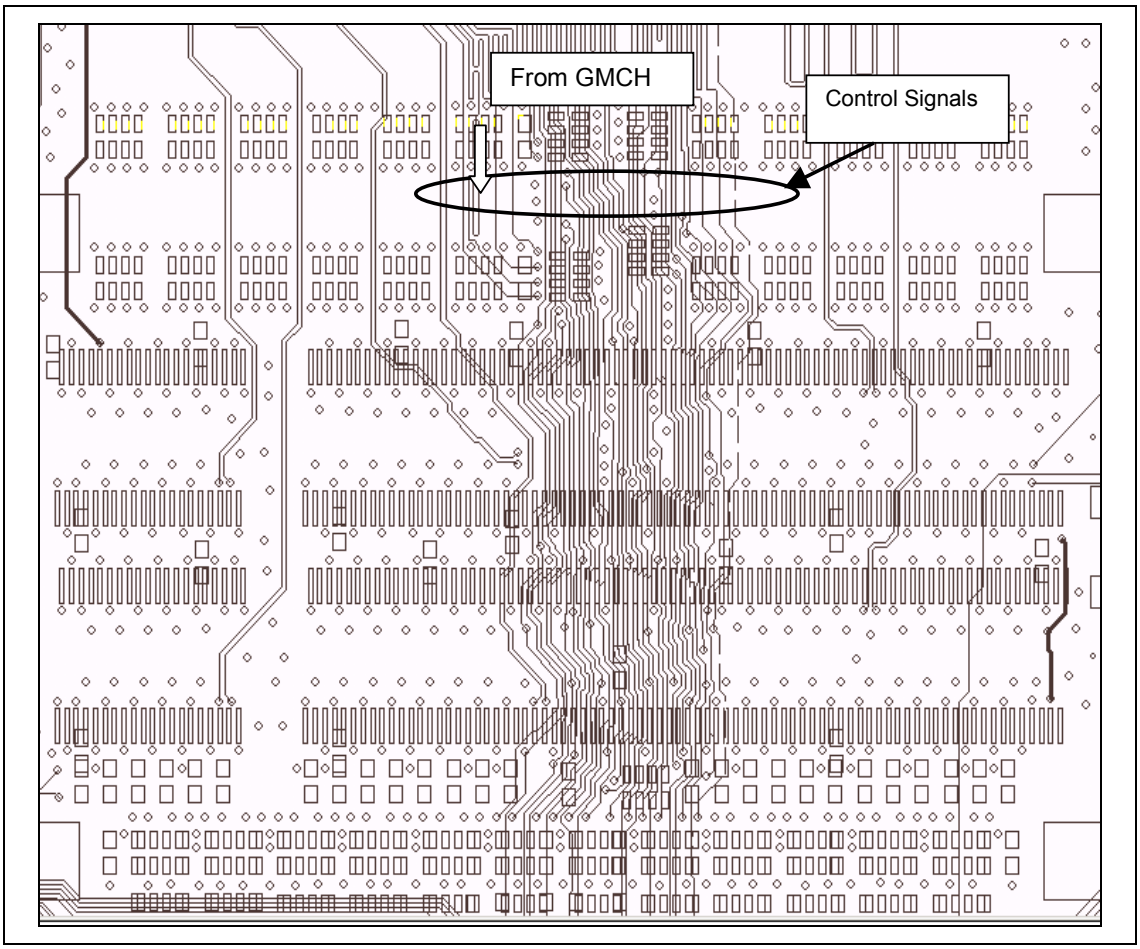
**Figure 28. Control Signal to Clock Trace Length Matching Diagram**



### 6.3.3.4. Memory Control Routing Example

Figure 29 is an example of a board routing for the Control signal group.

**Figure 29. Control Signals Group Routing Example**



#### 6.3.3.5. Control Group Package Length Table

The package length data in Table 25 below should be used to match the overall length of each command signal to its associated clock reference length. Note that due to the relatively small variance in package length and adequate timing margins it is acceptable to use a fixed 500-mil nominal package length for all control signals, thereby reducing the complexity of the motherboard length calculations.

**Table 25. Control Group Package Lengths**

| Signal | Pin Number | Package Length (mils) | Signal | Pin Number | Package Length (mils) |
|---|---|---|---|---|---|
| SCS#[0] | AD23 | 502 | SCKE[0] | AC7 | 443 |
| SCS#[1] | AD26 | 659 | SCKE[1] | AB7 | 389 |
| SCS#[2] | AC22 | 544 | SCKE[2] | AC9 | 386 |
| SCS#[3] | AC25 | 612 | SCKE[3] | AC10 | 376 |

### 6.3.4. Command Signals – SMA[12:6,3,0], SBA[1:0], SRAS#, SCAS#, SWE#

The GMCH/MCH chipset command signals, SMA[12:0], SBA[1:0], SRAS#, SCAS#, and SWE# clocked into the DDR SDRAMs using the clock signals SCK/SCK#[5:0]. The GMCH/MCH drives the command and clock signals together, with the clocks crossing in the valid command window. There are three supported topologies for the command signal group. Topology 1 is a daisy chain topology. Topology 2 implements a T routing topology. Both topologies allow series resistors to be placed between the two SO-DIMMs to dampen the SO-DIMM to SO-DIMM resonance. Topology 2 is the topology that best allows for placement of the SO-DIMMs back to back in the butterfly configuration, thus minimizing the SO-DIMM footprint area. Topology 3 allows the series resistors to be physically placed after the farthest SO-DIMM, when there is no room between the two connectors. Note that series resistors are essential in all of the three topologies.

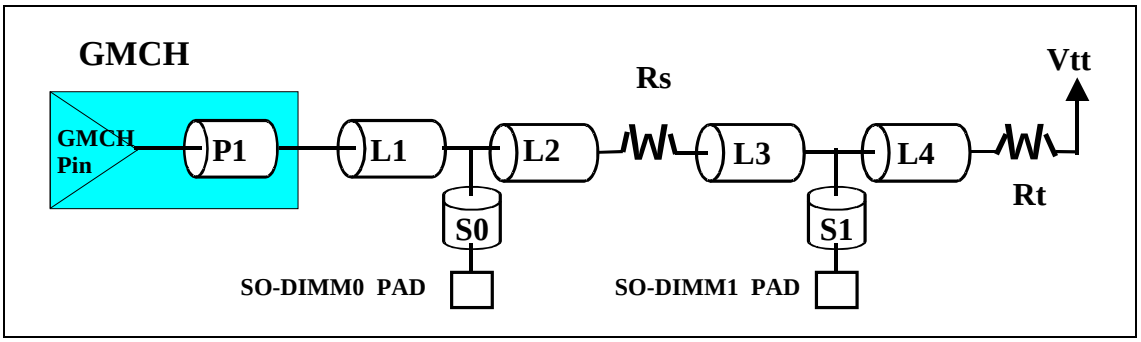
### 6.3.4.1. Command Topology 1

The command signal routing should transition from an external layer to an internal signal layer under the GMCH/MCH. Keep to the same internal layer until transitioning back to an external layer immediately prior to connecting the SO-DIMM0 connector pad. At the via transition for SO-DIMM0, continue the signal route on the same internal layer to the series termination resistor (Rs), collocated to SO-DIMM1. At this resistor the signal should transition to an external layer immediately prior to the pad of Rs. After the series resistor, Rs, continue the signal route on the external layer landing on the appropriate connector pad of SO-DIMM1. After SO-DIMM1, transition to the same internal layer or stay on the external layer and route the signal to Rt.

Intel suggests that the parallel termination (Rt) be placed on both sides of the board to simplify routing and minimize trace lengths. All internal and external signals should be ground referenced to keep the path of the return current continuous.

Resistor packs are acceptable for the series and parallel command termination resistors but command signals can not be placed within the same R-packs as data, strobe, or control signals. Figure 30 and Table 26 below depict the recommended topology and layout routing guidelines for the DDR-SDRAM command signals routing to SO-DIMM0 and SO-DIMM1.

**Figure 30. Command Routing for Topology 1**




The command signals should be routed using a 2 to 1 trace spacing to trace width ratio for signals within the DDR group, except clocks and strobes. There should be a minimum of 20 mils spacing to non-DDR related signals. Command signals should be routed on inner layers with minimized external traces.

### 6.3.4.2. Command Topology 1 Routing Guidelines

**Table 26. Command Topology 1 Routing Guidelines**

| Parameter | Routing Guidelines |
|---|---|
| Signal Group | SMA[12:6,3,0], SBA[1:0], SRAS#, SCAS#, SWE# |
| Motherboard Topology | Daisy Chain with Parallel Termination |
| Reference Plane | Ground Referenced |
| Characteristic Trace Impedance (Zo) | 55 ± 15% |
| Nominal Trace Width | Inner layers: 4 mils<br>Outer layers: 5 mils |
| Minimum Spacing to Trace Width Ratio | 2 to 1 (e.g. 8 mil space to 4 mil trace) |
| Minimum Isolation Spacing to non-DDR Signals | 20 mils |
| Package Length P1 | 500 mils +/- 250 mils<br>(See Table 29 for exact package lengths.) |
| Stub Lengths S0, S1 | Max = 0.25” |
| Trace Length L1 + S0 – GMCH/MCH Command Signal Ball to First SO-DIMM Pad | Min = 0.5 inch<br>Max = 4.0 inches |
| Total Length L1 + L2 + L3 + S1 – Total Length from GMCH/MCH Ball to Second SO-DIMM Pad | Min = 1.0”<br>Max = 7.0” |
| Total Length S0 + L2 + L3 + S1– Total SO-DIMM pad to SO-DIMM pad spacing | Max = 3.0” |
| Trace Length L4 – Second SO-DIMM Via to Parallel Resistor Pad | Max = 1.5 inches |
| Series Termination Resistor (Rs) | 10 ± 5% |
| Parallel Termination Resistor (Rt) | 56 ± 5% |
| Maximum Recommended Motherboard Via Count Per Signal | 6 |
| Length Matching Requirements | CMD to SCK/SCK# [5:0]<br>See length matching Section 6.3.4.3 and Figure 31 for details. |

**NOTES:**
1. Recommended resistor values and trace lengths may change in a later revision of the design guide.
2. Power distribution vias from Rt to Vtt are not included in this count.
3. The overall maximum and minimum length to the SO-DIMM must comply with clock length matching requirements.
4. It is possible to route using four vias if one via is shared that connects to the SO-DIMM1 pad and parallel termination resistor.

### 6.3.4.3. Command Topology 1 Length Matching Requirements

The routing length of the command signals, between the GMCH/MCH die pad and the SO-DIMM must be within the range defined below, with respect to the associated clock reference length. Refer to Figure 30 for a definition of the various motherboard trace segments. The length of trace from the SO-DIMM to the termination resistor need not be length matched. The length matching requirements are also depicted in Figure 31. Refer to Section 6.1 for more details on length matching requirements.

**Length range formula for SO-DIMM0:**

X0 = SCK/SCK#[2:0] total reference length, including package length.

Y0 = CMD signal total length = GMCH/MCH package + L1 + S0, as shown in Figure 31,

where: $( X_0 – 2.0” ) \quad Y_0 \quad ( X_0 + 2.0” )$ for DDR 200/266/333

**Length range formula for SO-DIMM1:**

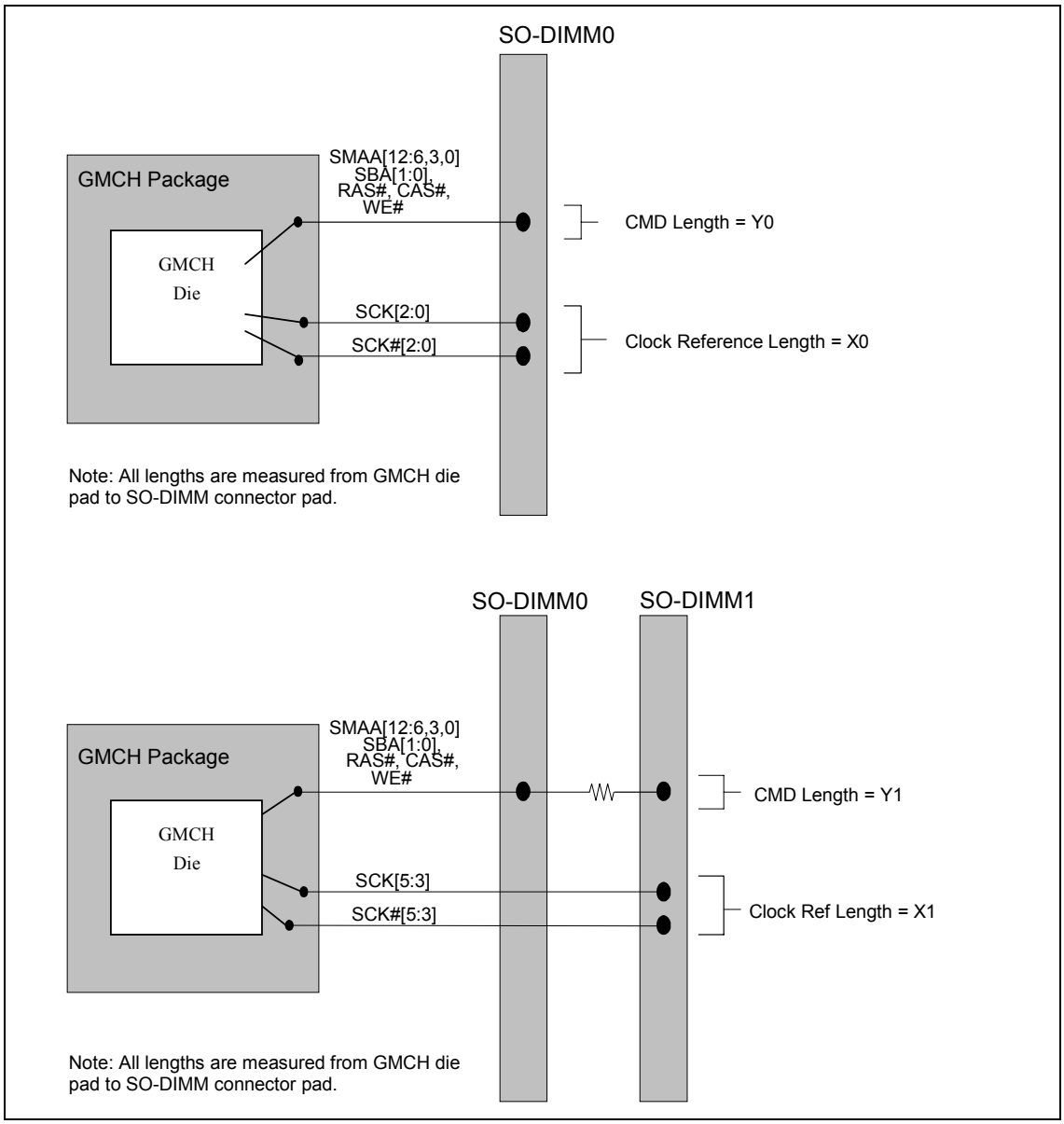
X1 = SCK/SCK#[5:3] total reference length, including package length.

Y1 = CMD signal total length = GMCH/MCH package + L1 + L2 + L3 + S1, as shown in Figure 31,

where: $( X_1 – 2.0” ) \quad Y_1 \quad ( X_1 + 2.0” )$ for DDR 200/266/333

No length matching is required from SO-DIMM1 to the termination resistor. Figure 31 on the following page depicts the length matching requirements between the command signals and clock. A nominal CMD package length of 500 mils can be used to estimate baseline MB lengths. Refer to Section 6.2 for more details on package length compensation.

**Figure 31. Topology 1 Command Signal to Clock Trace Length Matching Diagram**



### 6.3.4.4. Command Topology 2

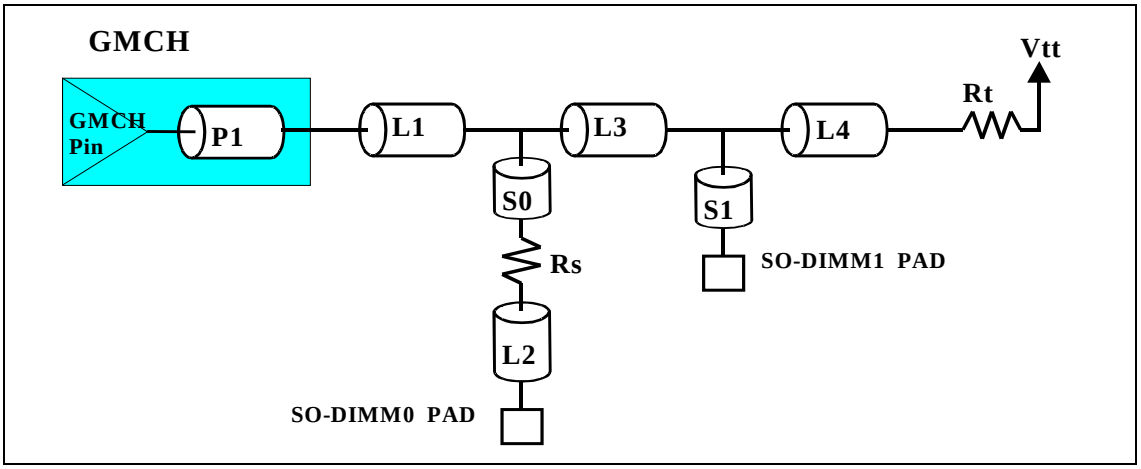
The command signal routing should transition from an external layer to an internal signal layer under the GMCH/MCH. Keep to the same internal layer until transitioning back to an external layer at the series resistor Rs. At this point there is a T in the topology. One leg of the T will route through Rs and either transition back to the same internal layer or stay external and landing on the appropriate connector pad of SO-DIMM0. If it was necessary to return to the internal layer the signal should return to the external layer immediately prior to landing on the appropriate connector pad of SO-DIMM0. The other leg of the T will continue on the same internal layer and return to the external layer immediately prior to landing on the appropriate connector pad of SO-DIMM1. If possible, stay on the external layer and connect to the parallel termination resistor or if the parallel termination resistor is on the opposite side of the board from the SO-DIMM1 connector then share the via and route to the parallel termination resistor. If sharing the via or using the opposite side of the board is not possible, continue on the same internal layer and route to the external layer immediately prior to the termination resistor.

External trace lengths should be minimized. It is suggested that the parallel termination be placed on both sides of the board to simplify routing and minimize trace lengths. All internal and external signals should be ground referenced to keep the path of the return current continuous. It is recommended that command signal group be routed on same internal layer.

It is suggested that the parallel termination (Rt) be placed on both sides of the board to simplify routing and minimize trace lengths. All internal and external signals should be ground referenced to keep the path of the return current continuous.

Resistor packs are acceptable for the series and parallel command termination resistors but command signals can not be placed within the same R-packs as data, strobe or control signals. Figure 32 and Table 27 below depict the recommended topology and layout routing guidelines for the DDR-SDRAM command signals routing to SO-DIMM0 and SO-DIMM1.

**Figure 32. Command Routing Topology 2**




The command signals should be routed using a 2 to 1 trace spacing to trace width ratio for signals within the DDR group, except clocks and strobes. There should be a minimum of 20 mils of spacing to non-DDR related signals. Command signals should be routed on inner layers with minimized external trace lengths.

### 6.3.4.5. Command Topology 2 Routing Guidelines

**Table 27. Command Topology 2 Routing Guidelines**

| Parameter | Routing Guidelines |
|---|---|
| Signal Group | SMA[12:6,3,0], SBA[1:0], SRAS#, SCAS#, SWE# |
| Motherboard Topology | Branched T with Parallel Termination |
| Reference Plane | Ground Referenced |
| Characteristic Trace Impedance (Zo) | 55 ± 15% |
| Nominal Trace Width | Inner layers: 4 mils<br>Outer layers: 5 mils |
| Minimum Spacing to Trace Width Ratio | 2 to 1 (e.g. 8 mil space to 4 mil trace) |
| Minimum Isolation Spacing to non-DDR Signals | 20 mils |
| Package Length P1 | 500 mils ± 250 mils<br>(See Table 29 for exact package length.) |
| Stub Length S0, S1 | Max = 0.25” |
| Trace Length L2 – Series Resistor Pad to First SO-DIMM Pad | Max = 1.0 inches |
| Total Length L1+ S0 + L2 – Total length from GMCH/MCH ball to First SO-DIMM pad | Min = 0.5”<br>Max = 5.0” |
| Total Length L1+ L3 + S1 – Total length from GMCH/MCH ball to Second SO-DIMM pad | Min = 1.0”<br>Max = 7.0” |
| Total Length S0 + L2 + L3 + S1– Total SO-DIMM pad to SO-DIMM pad spacing | Max = 3.0” |
| Trace Length L4 – Second SO-DIMM Via to Parallel Resistor Pad | Max = 1.5” |
| Series Termination Resistor (Rs) | 10 ± 5% |
| Parallel Termination Resistor (Rt) | 56 ± 5% |
| Maximum Recommended Motherboard Via Count Per Signal | 6 |
| Length Matching Requirements | CMD to SCK/SCK# [5:0]<br>See length matching Section 6.3.4.6 and Figure 33 for details. |

**NOTES:**
1. Recommended resistor values and trace lengths may change in a later revision of the design guide.
2. Power distribution vias from Rt to Vtt are not included in this count.
3. The overall maximum and minimum length to the SO-DIMM must comply with clock length matching requirements.
4. It is possible to route using three vias if one via is shared that connects to the SO-DIMM0 pad and series termination resistor, if a via is shared that connects L1 to series termination and if one via is shared that connects to the SO-DIMM1 pad and parallel termination resistor.

### 6.3.4.6. Command Topology 2 Length Matching Requirements

The routed length of the command signals, between the GMCH/MCH package ball and the SO-DIMM must be within the range defined below, with respect to the associated clock reference length. Refer to Figure 32 for a definition of the various motherboard trace segments. The length of trace from the SO-DIMM to the termination resistor need not be length matched. The length matching requirements are also depicted in Figure 33. Refer to Section 6.1 for more details on length matching requirements.

**Length range formula for SO-DIMM0**

$\mathbf{X_0}$ = SCK/SCK#[2:0] total reference length, including package length.

$\mathbf{Y_0}$ = CMD signal total length = GMCH/MCH package + L1 + L2 + S0, as shown in Figure 33,

where: ( $X_0$ – 2.0” ) $Y_0$ ( $X_0$ + 2.0” ) for DDR 200/266/333

**Length range formula for SO-DIMM1**

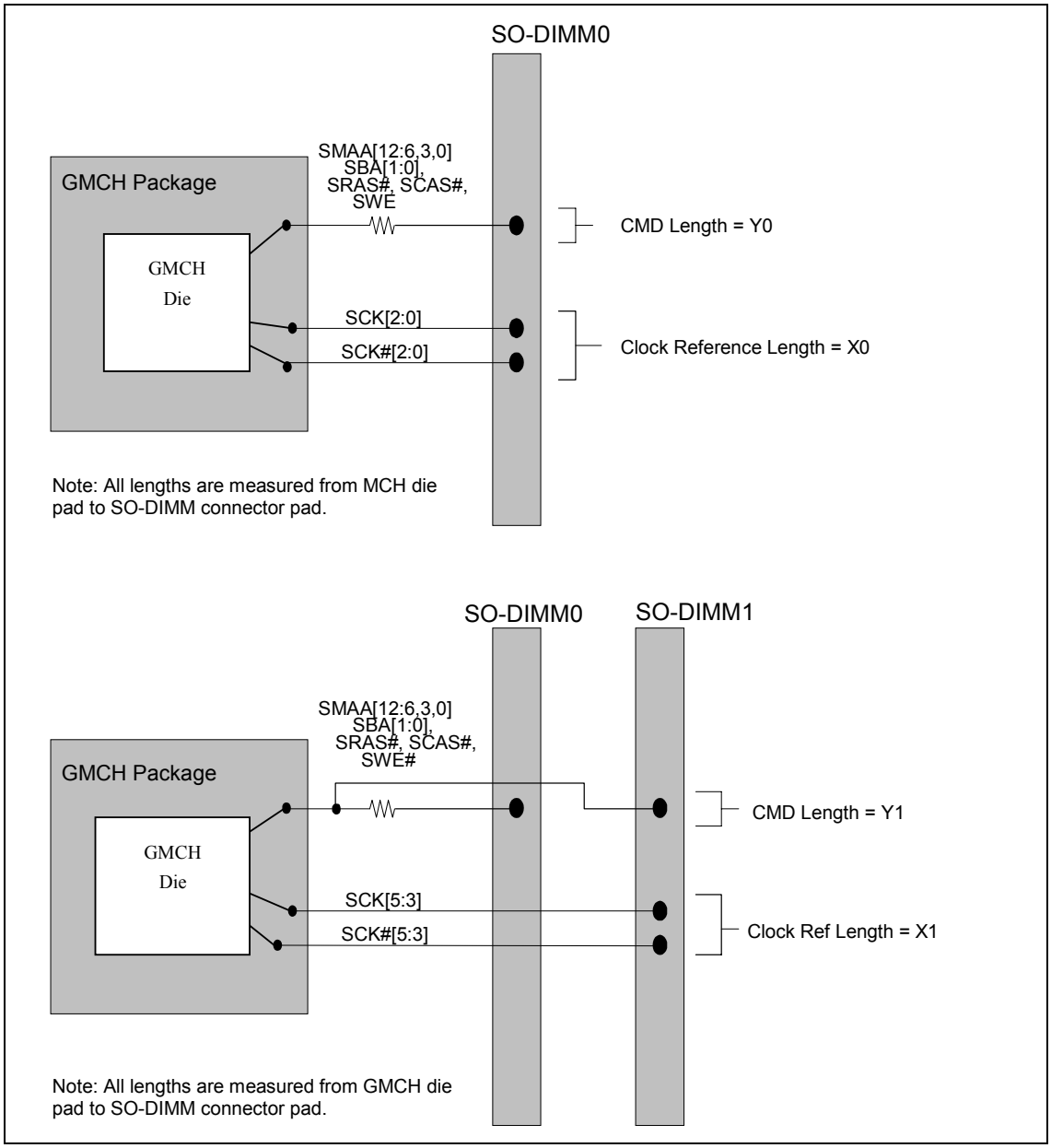
$\mathbf{X_2}$ = SCK/SCK#[5:3] total reference length, including package length.

$\mathbf{Y_2}$ = CMD signal total length = GMCH/MCH package length + L1 + L3 + S1, as shown in Figure 33,

where: ( $X_1$ – 2.0” ) $Y_1$ ( $X_1$ + 2.0” ) for DDR 200/266/333

No length matching is required from SO-DIMM1 to the termination resistor. Figure 33 on the following page depicts the length matching requirements between the command signals and clock. A nominal CMD package length of 500 mils can be used to estimate baseline MB lengths. Refer to Section 6.2 for more details on package length compensation.

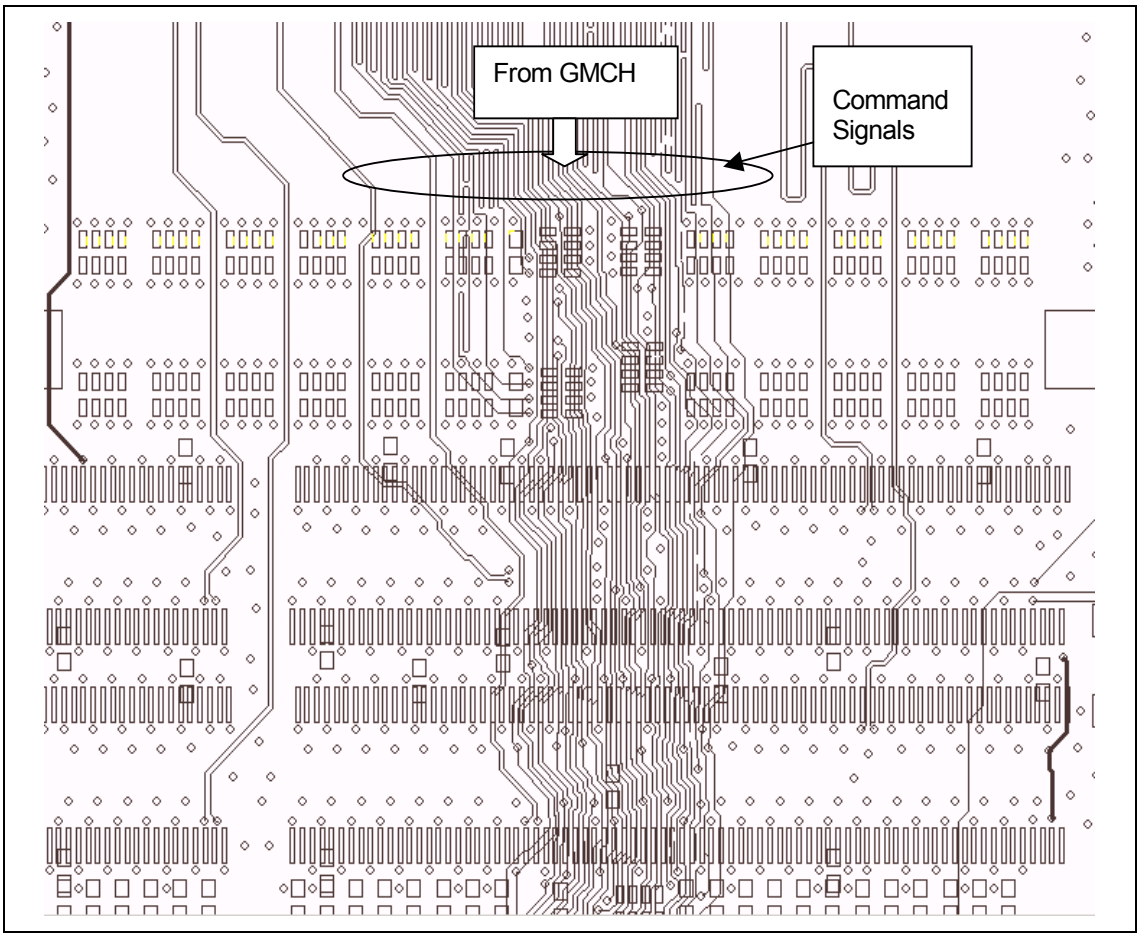
**Figure 33. Topology 2 Command Signal to Clock Trace Length Matching Diagram**



### 6.3.4.7. Command Topology 2 Routing Example

Figure 34 is an example of a board routing for the Command signal group.

**Figure 34. Example of Command Signal Group**



### 6.3.4.8. Command Topology 3

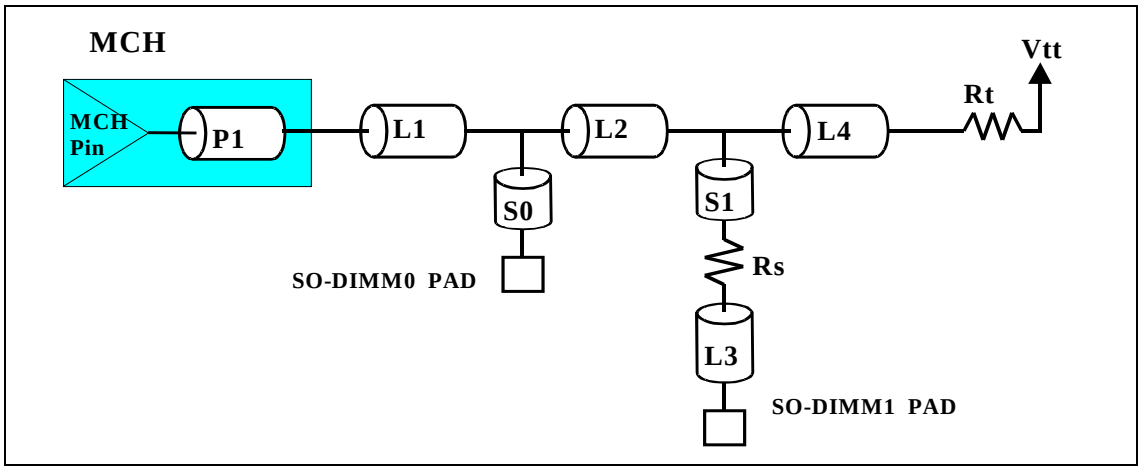
This topology is recommended when the SO-DIMMS are too close together for the series resistor to be placed between connectors. In this topology the series resistors are placed behind the second SO-DIMM.

External trace lengths should be minimized. It is suggested that the parallel termination be placed on both sides of the board to simplify routing and minimize trace lengths. All internal and external signals should be ground referenced to keep the path of the return current continuous. Intel recommends that the command signal group be routed on same internal layer.

Intel suggests that the parallel termination (Rt) be placed on both sides of the board to simplify routing and minimize trace lengths. All internal and external signals should be ground referenced to keep the path of the return current continuous.

Resistor packs are acceptable for the series and parallel command termination resistors but command signals can not be placed within the same R-packs as data, strobe or control signals. The diagrams and tables below depict the recommended topology and layout routing guidelines for the DDR-SDRAM command signals routing to SO-DIMM0 and SO-DIMM1.

**Figure 35. Command Routing Topology 3**




The command signals should be routed using a 2 to 1 trace spacing to trace width ratio for signals within the DDR group, except clocks and strobes. There should be a minimum of 20 mils of spacing to non-DDR related signals. Command signals should be routed on inner layers with minimized external trace lengths.

### 6.3.4.9. Command Topology 3 Routing Guidelines

**Table 28. Command Topology 3 Routing Guidelines**

| Parameter | Routing Guidelines |
|---|---|
| Signal Group | SMA[12:6,3,0], SBA[1:0], SRAS#, SCAS#, SWE# |
| Motherboard Topology | Branched T with Parallel Termination |
| Reference Plane | Ground Referenced |
| Characteristic Trace Impedance (Zo) | 55 ± 15% |
| Nominal Trace Width | Inner layers: 4 mils<br>Outer layers: 5 mils |
| Minimum Spacing to Trace Width Ratio | 2 to 1 (e.g. 8 mil space to 4 mil trace) |
| Minimum Isolation Spacing to non-DDR Signals | 20 mils |
| Package Length P1 | 500 mils ± 250 mils<br>(See Table 29 for exact package lengths.) |
| Stub Length S0, S1 | Max = 0.25” |
| Total Length L1+ S0 – Total length from GMCH/MCH ball to First SO-DIMM pad | Min = 0.5”<br>Max = 4.0” |
| Trace Length L3 – Series Resistor Pad to Second SO-DIMM Pad | Max = 1.0” |
| Total Length L1+L2 + L3 + S1 – Total length from GMCH/MCH ball to Second SO-DIMM pad | Min = 1.0”<br>Max = 7.0” |
| Total Length S0 + L2 + L3 + S1– Total SO-DIMM pad to SO-DIMM pad spacing | Max = 3.0” |
| Trace Length L4 – Second SO-DIMM Via to Parallel Resistor Pad | Max = 1.5” |
| Series Termination Resistor (Rs) | 10 ± 5% |
| Parallel Termination Resistor (Rt) | 56 ± 5% |
| Maximum Recommended Motherboard Via Count Per Signal | 6 |
| Length Matching Requirements | CMD to SCK/SCK# [5:0]<br>See length matching Section 6.3.4.10 and Figure 36 for details. |

**NOTES:**
1. Recommended resistor values and trace lengths may change in a later revision of the design guide.
2. Power distribution vias from Rt to Vtt are not included in this count.
3. The overall maximum and minimum length to the SO-DIMM must comply with clock length matching requirements.
4. It is possible to route using three vias if one via is shared that connects to the SO-DIMM0 pad and series termination resistor, if a via is shared that connects L1 to series termination and if one via is shared that connects to the SO-DIMM1 pad and parallel termination resistor.

### 6.3.4.10. Command Topology 3 Length Matching Requirements

The routed length of the command signals, between the GMCH/MCH package ball and the SO-DIMM must be within the range defined below, with respect to the associated clock reference length. Refer to Figure 32 for a definition of the various motherboard trace segments. The length of trace from the SO-DIMM to the termination resistor need not be length matched. The length matching requirements are also depicted in Figure 33. Refer to Section 6.1 for more details on length matching requirements.

**Length range formula for SO-DIMM0:**

$\mathbf{X_0}$ = SCK/SCK#[2:0] total reference length, including package length.

$\mathbf{Y_0}$ = CMD signal total length = GMCH/MCH package + L1 + S0, as shown in Figure 36,

where: ( $X_0$ – 2.0” ) $Y_0$ ( $X_0$ + 2.0” ) for DDR 200/266/333

**Length range formula for SO-DIMM1:**

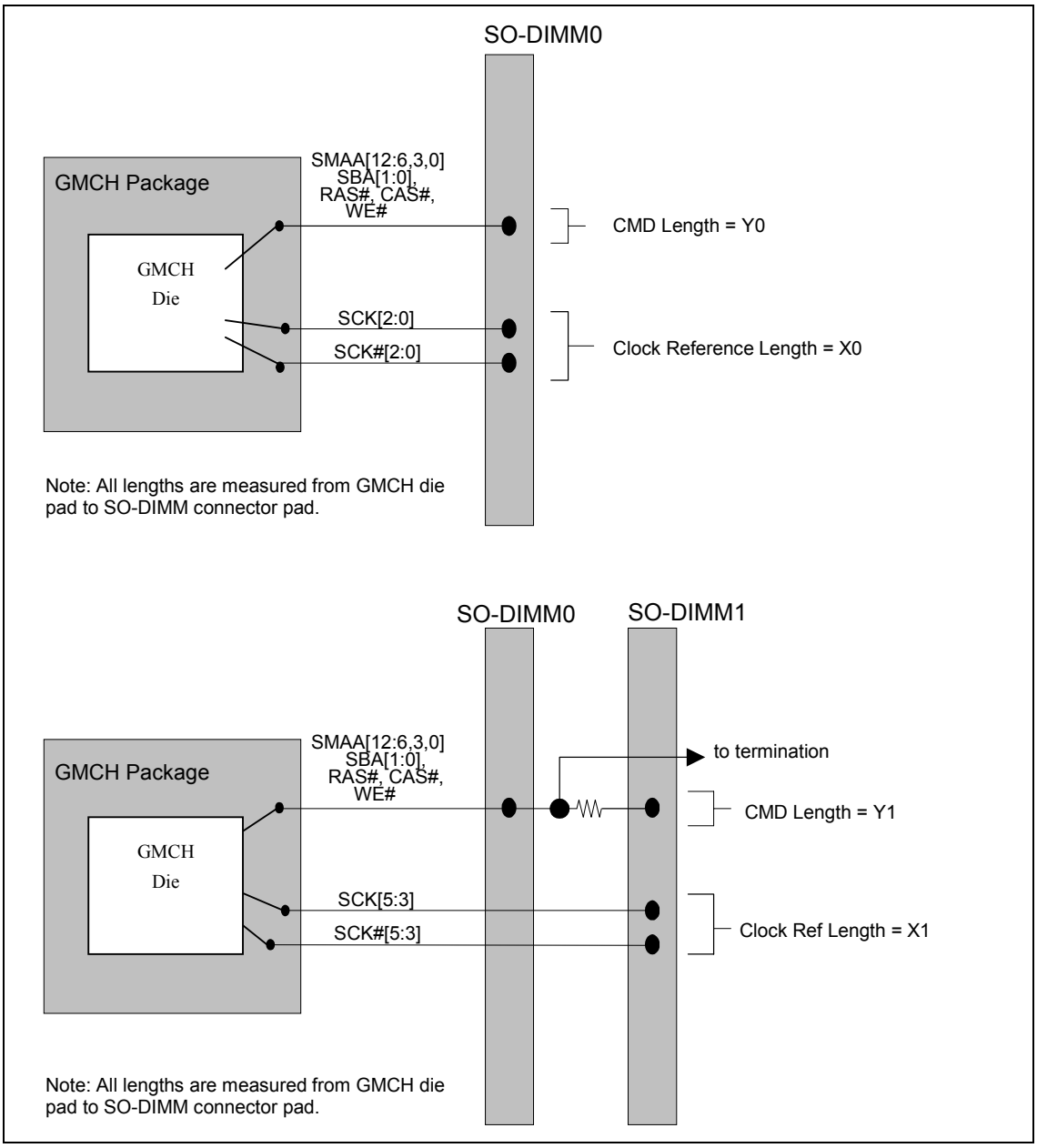
$\mathbf{X_2}$ = SCK/SCK#[5:3] total reference length, including package length.

$\mathbf{Y_2}$ = CMD signal total length = GMCH/MCH package length + L1 + L2 +L3 + S1, as shown in Figure 36,

where: ( $X_1$ – 2.0” ) $Y_1$ ( $X_1$ + 2.0” ) for DDR 200/266/333

No length matching is required from SO-DIMM1 to the termination resistor. Figure 33 on the following page depicts the length matching requirements between the command signals and clock. A nominal CMD package length of 500 mils can be used to estimate baseline MB lengths. Refer to Section 6.2 for more details on package length compensation.

**Figure 36. Topology 3 Command Signal to Clock Trace Length Matching Diagram**



### 6.3.4.11. Command Group Package Length Table

The package length data in Table 29 below should be used to match the overall length of each command signal to its associated clock reference length.

**Table 29. Command Group Package Lengths**

| Signal | Pin Number | Pkg Length (mils) |
|---|---|---|
| SMA[0] | AC18 | 420 |
| SMA[3] | AD17 | 472 |
| SMA[6] | AD8 | 591 |
| SMA[7] | AD7 | 596 |
| SMA[8] | AC6 | 630 |
| SMA[9] | AC5 | 681 |
| SMA[10] | AC19 | 377 |
| SMA[11] | AD5 | 683 |
| SMA[12] | AB5 | 609 |
| SBA[0] | AD22 | 592 |
| SBA[1] | AD20 | 435 |
| SCAS# | AC24 | 562 |
| SRAS# | AC21 | 499 |
| SWE# | AD25 | 751 |

## 6.3.5. CPC Signals – SMA[5,4,2,1], SMAB[5,4,2,1]

The GMCH/MCH chipset CPC (clock-per-command) signals, SMA[5,4,2,1] and SMAB[5,4,2,1]are "clocked" into the DDR SDRAM devices using clock signals SCK/SCK#[5:0]. The GMCH/MCH drives the CPC and clock signals together, with the clocks crossing in the valid command window. The GMCH/MCH provides one set of CPC signals per SO-DIMM slot.

Refer to Table 23 for the CKE and CS# signal to SO-DIMM mapping.

**Table 30. CPC Signal to SO-DIMM Mapping**

| Signal | Relative To | SO-DIMM Pin |
|---|---|---|
| SMA[1] | SO-DIMM0 | AD14 |
| SMA[2] | SO-DIMM0 | AD13 |
| SMA[4] | SO-DIMM0 | AD11 |
| SMA[5] | SO-DIMM0 | AC13 |
| | | |
| SMAB[1] | SO-DIMM1 | AD16 |
| SMAB[2] | SO-DIMM1 | AC12 |
| SMAB[4] | SO-DIMM1 | AF11 |
| SMAB[5] | SO-DIMM1 | AD10 |

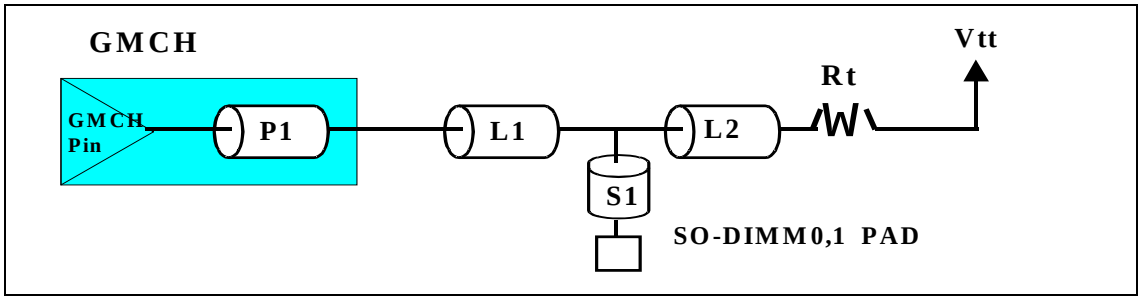
The CPC signal routing should transition from an external layer to an internal signal layer under the GMCH/MCH. Keep to the same internal layer until transitioning back out to an external layer to connect to the appropriate pad of the SO-DIMM connector and the parallel termination resistor. If the layout requires additional routing before the termination resistor, return to the same internal layer and transition back out to an external layer immediately prior to parallel termination resistor.

External trace lengths should be minimized. Intel suggests that the parallel termination be placed on both sides of the board to simplify routing and minimize trace lengths. All internal and external signals should be ground reference to keep the path of return current continuous. Intel suggests that all CPC signals be routed on the same internal layer.

Resistor packs are acceptable for the parallel (Rt) CPC termination resistors. Figure 37 and Table 31 below depict the recommended topology and layout routing guidelines for the DDR-SDRAM CPC signals.

### 6.3.5.1. CPC Signal Topology

**Figure 37. Command per Clock Signal Routing Topology**




The CPC signals should be routed using 2 to 1 trace space to width ratio for signals within the DDR group, except clocks and strobes. There should be a minimum of 20-mils of spacing to non-DDR related signals. CPC signals should be routed on inner layers with minimized external trace lengths.

### 6.3.5.2. CPC Signal Routing Guidelines

**Table 31. CPC Signal Routing Guidelines**

| Parameter | Routing Guidelines |
|---|---|
| Signal Group | SMA[5,4,2,1], SMAB[5,4,2,1] |
| Motherboard Topology | Point-to-Point with Parallel Termination |
| Reference Plane | Ground Referenced |
| Characteristic Trace Impedance (Zo) | 55 ±15% |
| Nominal Trace Width | Inner layers: 4 mils<br>Outer layers: 5 mils |
| Minimum Spacing to Trace Width Ratio | 2 to 1 (e.g. 8 mil space to 4 mil trace) |
| Minimum Isolation Spacing to non-DDR Signals | 20 mils |
| Package Length P1 | 500 mils ± 250 mils<br>(See Table 32 for exact package lengths.) |
| Stub Length S1 | Max = 0.25” |
| Trace Length L1 – GMCH/MCH Control Signal Ball to SO-DIMM Pad | Min = 0.5 inches<br>Max = 5.5 inches for DDR266<br>Max = 4.5 inches for DDR333 |
| Trace Length L2 – SO-DIMM Via to Parallel Termination Resistor Pad | Max = 2.0 inches |
| Parallel Termination Resistor (Rt) | 56 ± 5% |
| Maximum Recommended Motherboard Via Count Per Signal | 3 |

| | |
|---|---|
| Length Matching Requirements | CPC to SCK/SCK# [5:0]<br>See length matching Section 6.3.5.3 for details. |

**NOTES:**
1. Recommended resistor values and trace lengths may change in a later revision of the design guide.
2. Power distribution vias from Rt to Vtt are not included in this count.
3. It is possible to route using two vias if one via is shared that connects to the SO-DIMM pad and parallel termination resistor.
4. The overall maximum and minimum length to the SO-DIMM must comply with clock length matching requirements.

### 6.3.5.3. CPC to Clock Length Matching Requirements

The total length of the CPC signals, between the GMCH/MCH die pad and the SO-DIMM must fall within the range defined below, with respect to the associated clock reference length. Refer to Figure 37 for a definition of the various trace segments. The length the trace from the SO-DIMM to the termination resistor need not be length matched. Refer to Section 6.1 for more details on length matching requirements. A table of CPC signal package length is provided in Section 6.3.5.4.

**Length range formula for SO-DIMM0:**

$\mathbf{X_0}$ = SCK/SCK#[2:0] total reference length, including package length.

$\mathbf{Y_0}$ = SMA[5,4,2,1] total length = GMCH/MCH package + L1 + S1, as shown in,

where: ( $X_0$ – 2.0” ) $Y_0$ ( $X_0$ - 1.0” ) for DDR 200/266/333

**Length range formula for SO-DIMM1:**

$\mathbf{X_1}$ = SCK/SCK#[5:3] total reference length, including package length.

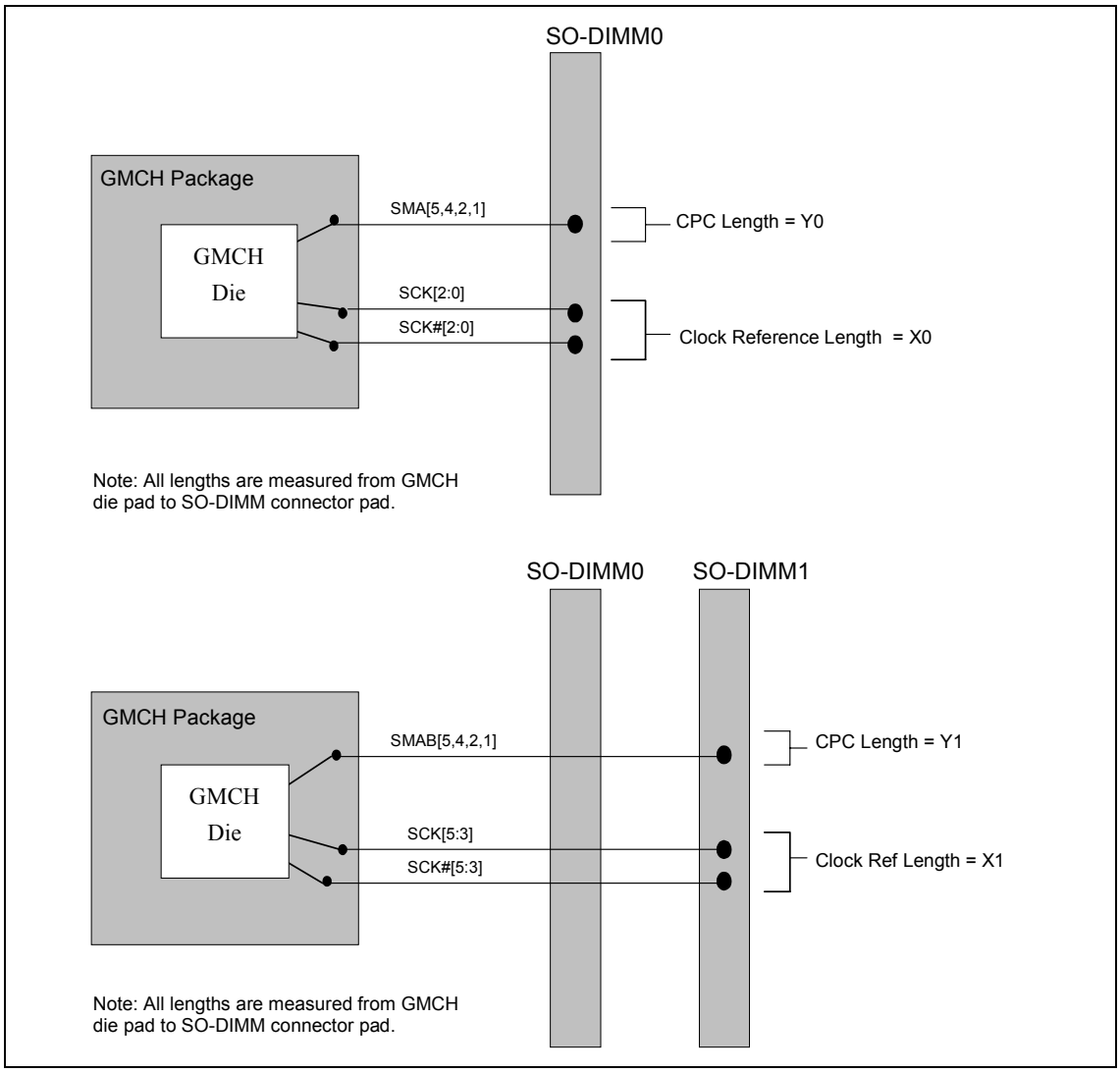
$\mathbf{Y_1}$ = SMAB[5,4,2,1] total length = GMCH/MCH package + L1 + S1, as shown in,

where: ( $X_1$ – 2.0” ) $Y_1$ ( $X_1$ - 1.0” ) for DDR 200/266/333

No length matching is required from SO-DIMM1 to the termination resistor.

on the following page depicts the length matching requirements between the CPC signals and clock. A nominal CPC package length of 500 mils can be used to estimate baseline MB lengths. Refer to Section 6.2 for more details on package length compensation.

**Figure 38. CPC Signals to Clock Length Matching Diagram**




### 6.3.5.4. CPC Group Package Length Table

The package length data in the table below should be used to match the overall length of each CPC signal to its associated clock reference length.

**Table 32. CPC Group Package Lengths**

| Signal | Pin Number | Pkg Length (mils) | Signal | Pin Number | Pkg Length (mils) |
|---|---|---|---|---|---|
| SMA[1] | AD14 | 398 | SMAB[1] | AD16 | 427 |
| SMA[2] | AD13 | 443 | SMAB[2] | AC12 | 395 |
| SMA[4] | AD11 | 430 | SMAB[4] | AF11 | 716 |
| SMA[5] | AC13 | 346 | SMAB[5] | AD10 | 631 |

### 6.3.6. Feedback – RCVENOUT#, RCVENIN#

The Intel 852GME/852GMV/852PMchipset GMCH/MCH provides a feedback signal called “receive enable” (RCVEN#), which is used to measure timing for the read data.

The RCVENOUT# signal is shunted directly to RCVENIN# inside the package in order to reduce timing variance. With this change it is no longer necessary to provide an external connection. However, it is recommended that both signals be transitioned to the bottom side with vias located adjacent to the package ball in order to facilitate probing.

## 6.4. Routing Updates for “High-Density” Memory Device Support

Simulation results show that the current DDR layout and routing guidelines for the Intel 852GME/852GMV/852PMchipset-based platforms can support “high-density” SO-DIMM memory modules. Please contact your Intel field representative for command signal group related BIOS settings for supporting high-density SO-DIMM modules.

## 6.5. ECC Disable Guidelines

The GMCH/MCH can be configured to operate in an ECC data integrity mode that allows multiple bit error detection and single bit error correction. This option to support ECC DDR memory modules is dependent on design objectives. By default, ECC functionality is disabled on the platform.

### 6.5.1. GMCH/MCH ECC Functionality Disable

If non-ECC memory modules are to be the only supported memory type on the platform, then the eight DDR check bits signals, associated strobe, data mask bit, and differential clock pairs associated with the ECC device for each SO-DIMM can be left as no connects on the GMCH/MCH. For the GMCH/MCH, this includes SDQ[71:64], SDQS8, SDM8 and the two differential clock pairs that are not routed to the SO-DIMMs.

The 852GME/852GMV/852PMchipset GMCH/MCH provides the capability to enable and disable the CS/CKE control and SCK signals to unpopulated SO-DIMMs to save power. Although DDR SO-DIMM connectors may provide motherboard lands for three clock pairs, non-ECC SO-DIMMs only require two pairs.

The GMCH/MCH provides some flexibility on how the SCK clock pairs, control signals, and CPC signals are assigned to the SO-DIMMs, provided that BIOS initialization of memory matches the hardware configuration. Two examples are listed below. Please contact your Intel field representative for memory reference code for more details.

| *Example 1* | | *Example 2* | |
|---|---|---|---|
| **SO-DIMM0** | **SO-DIMM1** | **SO-DIMM0** | **SO-DIMM1** |
| SCK0,1,2 | SCK3,4,5 | SCK0,1,2 | SCK3,4,5 |
| SMAA[1,2,4,5] | SMAB[1,2,4,5] | SMAB[1,2,4,5] | SMAA[1,2,4,5] |
| SCKE0,1; SCS#0,1 | SCKE2,3; SCS#2,3 | SCKE0,1; SCS#0,1 | SCKE2,3; SCS#2,3 |

On platforms where ECC memory is supported, it is important that all relevant SDQ, SDQS, and SCK signals to the SO-DIMMs be disabled when the system is populated with only non-ECC or a combination of ECC and non-ECC memory.

Please contact your Intel field representative for information on memory initialization and register programming.

### 6.5.2. DDR Memory ECC Functionality Disable

It is imperative that systems that do not support ECC memory ensure the SCK clock pairs that are normally sent to ECC SO-DIMMs be disabled. If the SCK clock pairs associated with the check bit signals were left floating in a non-ECC memory only system and ECC memory was used in one or more of the SO-DIMM slots, this could cause the ECC device on the SO-DIMM to be enabled. If SDQ[71:64] is disabled/tri-stated or not routed, then these floating inputs can cause the ECC device to draw current and potentially compromise the ECC device.

In *JEDEC PC2100 DDR SDRAM Unbuffered SO-DIMM Reference Design Specification, Rev 1.0*, it is noted that pin 89 and pin 91 (CK2 and CK2#) of the SO-DIMM connector are reserved for x72 modules or registered modules. By default, 852GME/852GMV/852PMdoes not drive SCK2, SCK2#, SCK5, SCK5#. Therefore, it is important to make sure that the memory modules are not expected to use all clock pairs.

## 6.6. System Memory Compensation

See Section 12.5.4 for details.

## 6.7. SMVREF Generation

See Section 12.5.3.1 for details.

## 6.8. DDR Power Delivery

See Section 12.5.4 for details.

## 6.9. External Thermal Sensor Based Throttling (ETS#)

The GMCH/MCH's ETS# input pin is an active low input that can be used with an external thermal sensor to monitor the temperature of the DDR SO-DIMMs for a possible thermal condition. Assertion of ETS# will result in the limiting of DRAM bandwidth on the DDR memory interface to reduce the temperature in the vicinity of the system memory.

By default, the functionality and input buffer associated with ETS# are disabled. Also, the GMCH/MCH can be programmed to send an SERR, SCI, or SMI message to the ICH4-M upon the assertion of this signal. External thermal sensors that are suitable for the purpose described above would need to have a small form factor and be able to accurately monitor the ambient temperature in the vicinity of the DDR system memory.

### 6.9.1. ETS# Usage Model

The thermal sensors targeted for this application with the GMCH/MCH's ETS# are planned to be capable of measuring the ambient temperature only and should be able to assert ETS# if the preprogrammed thermal limits/conditions are met or exceeded. Because many variables within a mobile system can affect the temperature measured at any given point, the expected usage and effectiveness of ETS# is also very focused. Factors such as thermal sensor placement, airflow within a mobile chassis, adjacent components, thermal sensor sensitivity, and thermal sensor response time, allow ETS# to be effectively used for controlling skin temperatures. However, due to the location of the thermal sensor, ETS# should not be used for measuring or controlling the Tj or Tcase parameters of DDR-SDRAM devices since it cannot respond quickly enough to dynamic changes in DRAM power.

### 6.9.2. ETS# Design Guidelines

ETS#, as implemented in the GMCH/MCH, is an active low signal and does **not** have an integrated pull-up to maintain a logic 1. As a result of this, an external 8.2-k to 10-k pull-up resistor should be provided near the ETS# pin, connected to 3.3 V. Ideally, the thermal sensor should implement an open drain type output buffer to drive ETS#. A system is expected to have one thermal sensor per SO-DIMM connector on the motherboard.

### 6.9.3. Thermal Sensor Routing and Placement Guidelines

Routing guidelines and other special, motherboard design considerations will vary with the vendor and type of thermal sensor chosen for this ETS# application. As a result, vendor specific design guidelines should also be followed closely to ensure proper operation of this feature. As a general rule, system designers should follow good design practices in ensuring good signal integrity on this signal as well as achieving adequate isolation from adjacent signals. Also, any thermal design considerations (e.g. proper ground flood placement underneath the external thermal sensor; proper isolation of the differential signal routing for thermal diode applications, etc.) for the external thermal sensor itself should also be met.

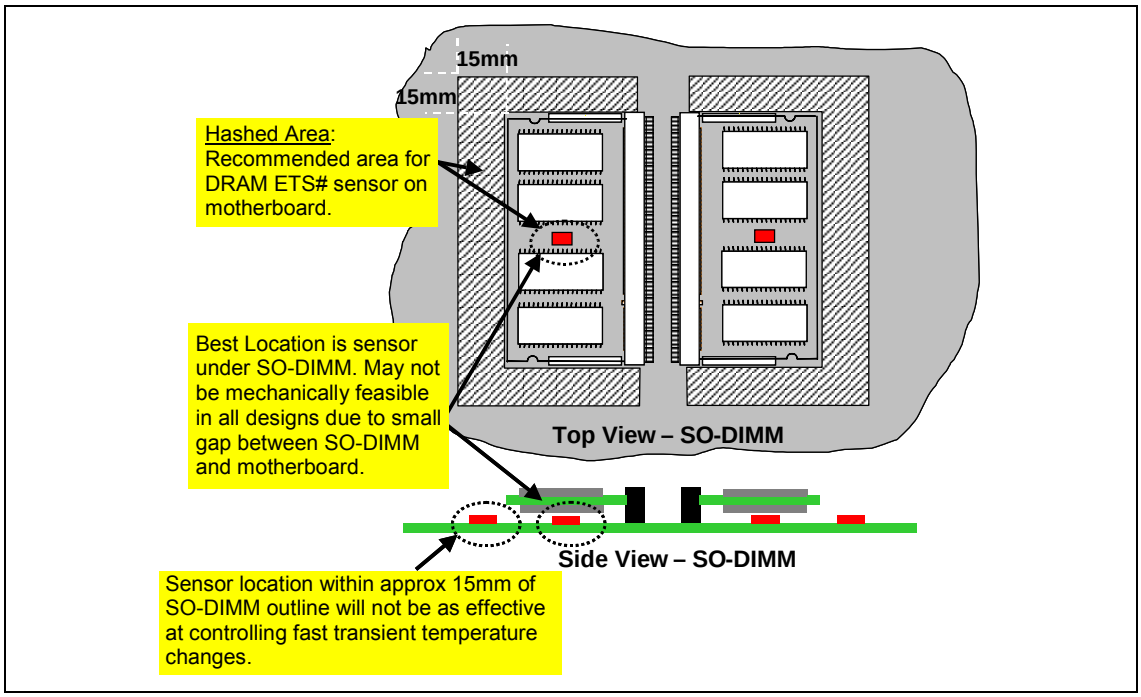
The many factors that can affect the accuracy of ambient temperature measurements by thermal sensors make the placement of them a very critical and especially challenging task. Ideally, one thermal sensor should be placed near each SO-DIMM in a system. The thermal sensor should be located in an area

where the effects of airflow and effects of conduction from adjacent components are minimized. This allows for the best correlation of thermal sensor temperature to chassis or notebook surface temperature. See Figure 39 for details.

Assuming airflow is negligible within a system, the optimal placement of the thermal sensor is on the surface of the motherboard directly beneath the shadow of an SO-DIMM module centered longitudinally and laterally in relation to the outline of the SO-DIMM. The thermal sensor should have a form factor small enough to allow it to fit beneath double-sided memory modules (i.e. modules with memory devices on both sides of a module). If placement within the outline of an SO-DIMM is not possible, then the next best option is to locate it within approximately 15 mm (0.6 inches) of the outline/SO-DIMM shadow. Again, this assumes negligible effects from airflow.

Please refer to the *Intel® 852GM Chipset Mobile Thermal Design Guide* for more details.

**Figure 39. DDR Memory Thermal Sensor Placement**



# 7. Integrated Graphics Display Port

***Note:*** This section of this document applies to Intel 852GME GMCH chipsets.

The GMCH contains four display ports: an analog CRT port, a dedicated LVDS port, and two 12-bit Digital Video Out (DVO) ports. Section 7.1 will discuss the CRT and RAMDAC routing requirements. Section 7.2 will discuss the dedicated LVDS port. Section 7.3 will discuss the DVOB and DVOC design guideline. Section 7.4 provides recommendations for a flexible modular design guideline for DVOB and DVOC muxed interfaces. Section 7.5 provides recommendations for the GPIO signal group.

## 7.1. Analog RGB/CRT Guidelines

### 7.1.1. RAMDAC/Display Interface

The GMCH integrated graphics/chipset design interfaces to an analog display via a RAMDAC. The RAMDAC is a subsection of the graphics controller display engine and consists of three identical 8-bit digital-to-analog converter (DAC) channels, one for the display's red, green, and blue electron guns.

Each RGB output is doubly terminated with a 75- resistance: One 75- resistance is connected from the DAC output to the board ground, and the other termination resistance exists within the display. The equivalent DC resistance at the output of each DAC is 37.5 . The current output from each DAC flows into this equivalent resistive load to produce a video voltage, without the need for external buffering. There is also a pi-filter on each channel that is used to reduce high-frequency noise and to reduce EMI. In order to maximize the performance, the filter impedance, cable impedance, and load impedance should be matched.

Since the DAC operates at pixel frequencies up to 350 MHz, special attention should be paid to signal integrity and EMI. RGB routing, component placement, component selection, cable and load impedance (monitor) all play a large role in the analog display's quality and robustness. This holds true for all resolutions, but especially for those at 1600x1200 resolutions or higher.

### 7.1.2. Reference Resistor (REFSET)

A reference resistor, Rset, is used to set the reference current for the DAC. This resistor is an external resistor with a 1% tolerance that is placed on the circuit board. A reference resistor can be selected from a range between 124 to 137 (1%). Based on board design, DAC RGB outputs may be measured when the display is completely white. If the RGB voltage value is between 665 mV to 770 mV, then the video level is within VESA specification and the resistor value that was chosen will be optimal for board design.

A reference voltage is generated on the GMCH from a bandgap voltage reference circuit. The bandgap reference voltage level is approximately 1.2 V and this voltage is divided by four to generate the reference voltage. The VESA video standard defines the LSB current for each DAC channel. The RAMDAC reference current is designed on-die to be equal to 32 LSB. Therefore, the external reference resistor value is defined as:

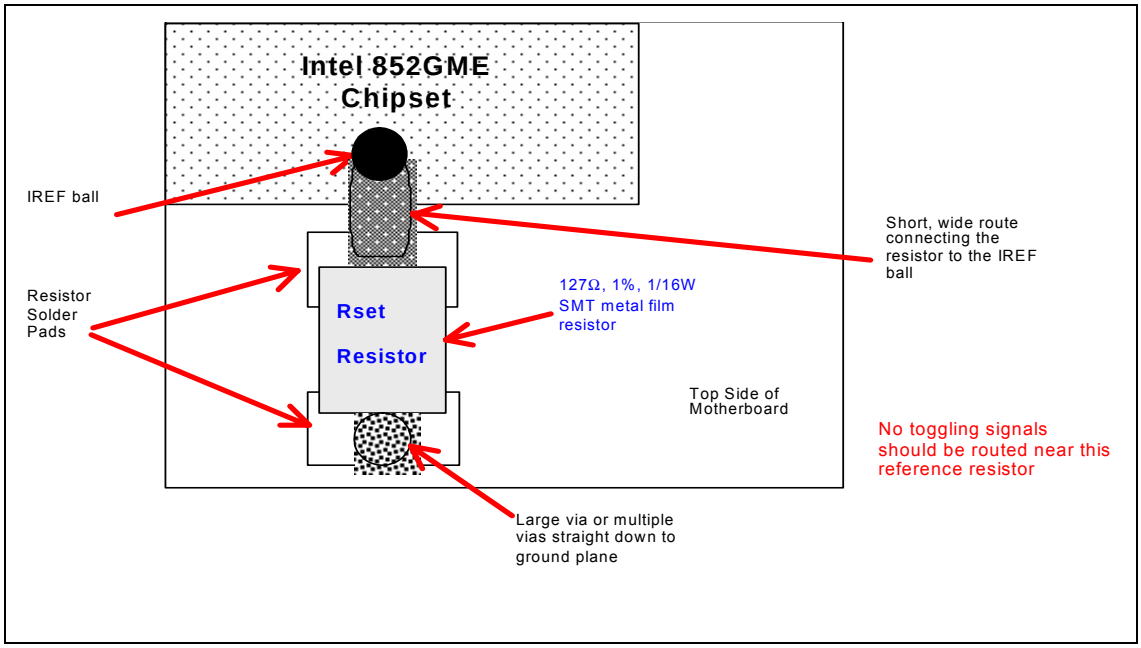
**Equation 2.**

$$Rset = \frac{Vreference}{Ireference} = \frac{(Vbg / 4)}{32 * (73.2uA)}$$

A 127- 1% precision resistor value is the recommend value to use. See Figure 40 for the recommended Rset placement.

***Note:*** When using 852GME platform with external graphics only, Rset resistor is not needed.

**Figure 40. Rset Placement**




## 7.1.3. RAMDAC Board Design Guidelines

Care should be taken when routing the analog RAMDAC signals. This is especially true to successfully support high display resolution where pixel frequency can be as high as 350 MHz. Intel recommends that each analog R, G, B signal be routed single-endedly. The analog RGB signals should be routed with an impedance of 37.5 . Intel recommends that these be routed on an inner routing layer and that it be shielded with VSS planes, if possible. Spacing between DAC channels and to other signals should be maximized; 20-mil spacing is recommended. The RGB signals require pi filters that should be placed near the VGA connector. It consists of two 3.3-pF caps with a 75 Ω ferrite bead at 100 MHz between them. The RGB signals should have a 75-Ω, 1% terminating pull-down resistor. The complement signals (R#, G#, and B#) should be grounded to the ground plane.

***Note:*** When using 852GME/852GMV/852PMwith external graphics only, the RGB 75-Ω termination resistors are not needed.

Intel recommends that the pi filter and terminating resistors be placed as close as possible to the VGA connector. After the 75- termination resistor, the RGB signals routing to the pi-filters and the VGA

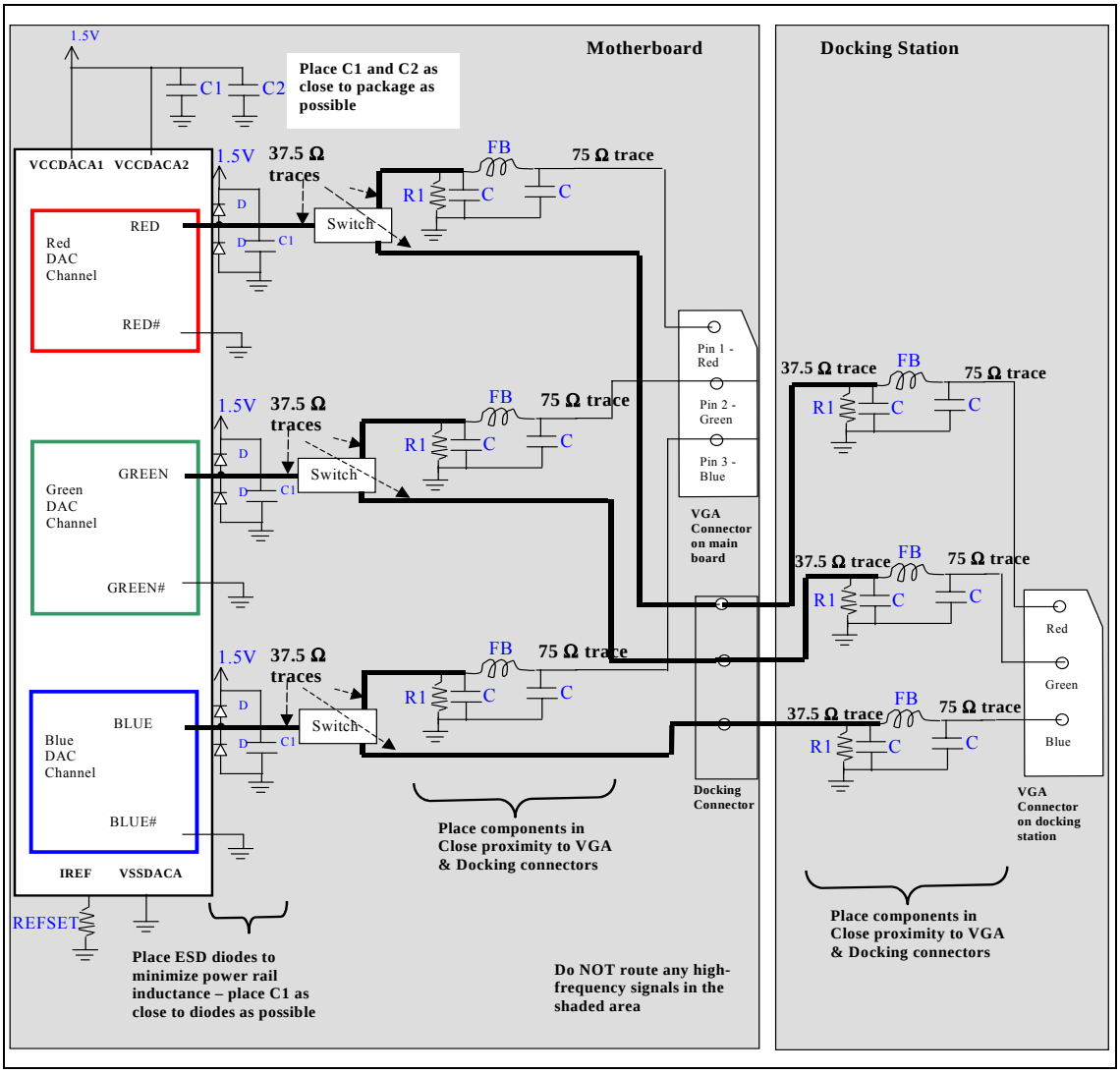
connector *should ideally be routed with 75- impedance (~ 5 mil traces), or as close to 75- impedance as possible.*

The RGB signals also require protection diodes between 1.5 V and ground. These diodes should have low C ratings (~5 pF max) and small leakage current (~ 10 A at 120˚C) and should be properly decoupled with a 0.1- F cap. These diodes and decoupling should be placed to minimize power rail inductance. The choice between diodes (or diode packs) should comprehend the recommended electrical characteristics in addition to cost.

The RGB signals should be length matched as closely as possible (from the GMCH to the VGA connector) and should not exceed 200 mils of mismatch.

## 7.1.4. RAMDAC Routing Guidelines

**Figure 41. GMCH DAC Routing Guidelines with Docking Connector**



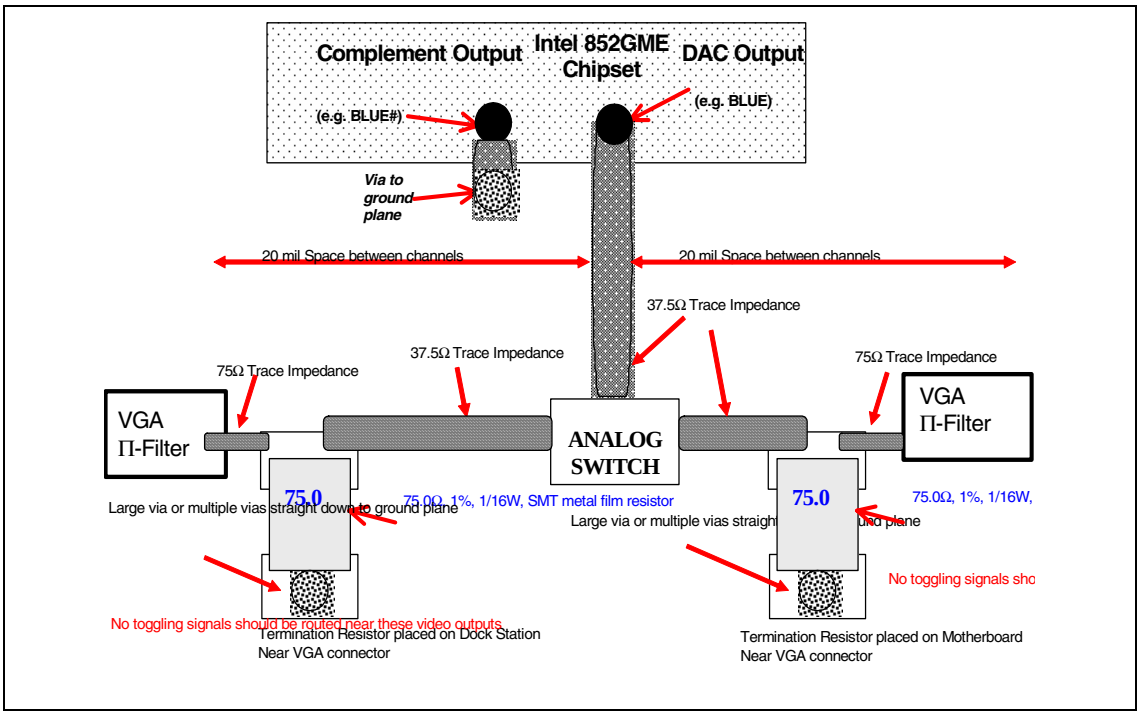
The DAC channel (red, green, blue) outputs should be routed as single-ended shielded routes to an analog switch to support a docking station. An analog switch should be used in order to provide the proper termination that is required for high-performance video signal integrity. See Table 33. The analog switch should exhibit a low "on" resistance (< 8 ) and low parasitic capacitance (<10 pF). The output routing from the analog switch should be routed as single-ended, 37.5-Ω impedance to the 75- termination resistors that are located near the VGA connector on the motherboard and the VGA connector on the docking station. The single-ended routing after these 75- termination resistors to the pi-filter and then to the VGA connector should be ideally 75- . The recommended routing of the termination resistors is shown in Table 33.

### Table 33. Recommended GMCH DAC Components

| Recommended DAC Board Components | | | | |
|---|---|---|---|---|
| **Component** | **Value** | **Tolerance** | **Power** | **Type** |
| R1 | 75.0 | 1% | 1/16 W | SMT, Metal Film |
| Refset[1] | 127.0 | 1% | 1/16 W | SMT, Metal Film |
| C1 | 0.1 µF | 20% | ----- | SMT, Ceramic |
| C2 | 0.01 µF | 20% | ----- | SMT, Ceramic |
| C | 3.3 pF | 10% | ----- | SMT, Ceramic |
| D | PAC DN006 | ------- | 350 mW | California Micro Devices – ESD diodes for VGA, SOIC package Or equivalent diode array |
| FB | 75 @ 100 MHz | -------- | ------- | MuRata* BLM11B750S |
| Analog Switch | ------- | ------- | Rated for a continuous channel current of 100 mA (min) | Ron < 8 , Con < 10pF Texas Instruments SN74CB3Q3306 |

**NOTE:** Not needed when using 852PM platform or 852GME platform with external graphics.

**Figure 42. DAC R, G, B Routing and Resistor Layout Example**




**NOTE:** The routing to the docking connector is not shown in this figure; however, this routing scheme applies to the docking connector as well.

## 7.1.5. DAC Power Requirements

The DAC requires a 1.5-V supply through its two VCCADAC balls. The two may share a set of capacitors, 0.1 F and 0.01 F, but this connection should have low inductance. Separate analog power or ground planes are not required for the DAC.

However, since the DAC is an analog circuit, it is particularly sensitive to AC noise seen on its power rail. Designs should provide as clean and quiet a supply as possible to the VCCA_DAC. Additional filtering and/or separate voltage rail may be needed to do so. On the Intel CRB, there is a placeholder for a LC filter in case there is noise present in the VCCA power rail.

Video DAC Power Supply DC Specification: 1.50 V ± 5%
Video DAC Power Supply AC Specification:
+/- 0.3% from 0.10 Hz to 10 MHz
+/- 0.95% from 10 MHz to max pixel clock frequency
Absolute minimum voltage at the VCCA package ball = 1.40 V

Please refer to the *Intel® 852GME Chipset GMCH and Intel® 852PM Chipset MCH Datasheet* for AC/CD specification.

### 7.1.6. HSYNC and VSYNC Design Considerations

HSYNC and VSYNC signals are connected to the analog display attached to the VGA connector. These are 3.3-V outputs from the GMCH. Some monitors have been found to drive HSYNC and VSYNC signals during reset. Because these signals are used as straps on the 852GME, the GMCH can enter an illegal state under these conditions. In order to prevent these signals from being driven to the GMCH during reset, system designers must ensure the GMCH is isolated from any monitor driving HSYNC or VSYNC while PCI_RST# is active. Appropriate logic is required between the GMCH and the VGA connector (both the on-board VGA connector and the VGA connector at the docking station) to accomplish this.

Intel's recommended option is to use an analog switch (i.e. discrete FET, Q-buffer) to switch these signals between the on-board VGA connector and the docking connector. In this case, footprints for a series resistor and an optional capacitor are needed on each of these signals to meet the VESA electrical specifications for video signals. Resistor and capacitor values of 39 Ω and 33 pF respectively are used on the CRB. These values were calculated based on the GMCH buffer strength and board routing. Customers are recommended to perform a signal integrity check specific to their board topology to determine the appropriate resistor and capacitor values for their platforms.

An alternative option is to use a unidirectional buffer on each of these signals. For each of the HSYNC and VSYNC signals, a footprint for a series resistor must be placed between the GMCH and the unidirectional buffer to prevent excessive overshoot and undershoot at the input of the buffer. Consideration should also be taken in designing the filter circuit on the output of these buffers to ensure that the VESA electrical specifications for video signals are met at both the on-board VGA connector as well as on the docking station. Customers are strongly encouraged to perform complete signal integrity validation at the input of the buffer and at the VGA connectors.

### 7.1.7. DDC and I2C Design Considerations

DDCADATA and DDCACLK are 3.3-V IO buffers connecting the GMCH to the monitor. If higher signaling voltage (5 V) is required by the monitor, level shifting devices may be used. Pull-up resistors of 2.2-k (or of the appropriate value derived from simulation) are required on each of these signals.

## 7.2. LVDS Transmitter Interface

The Intel LVDS (Low Voltage Differential Signaling) transmitter serializer converts up to 24 bits of parallel digital RGB data, (8 bits per RGB), along with up to 4 bits for control (SHFCLK, HSYNC, VSYNC, DE) into 2, 4 channel serial bit streams, for output by the LVDS transmitter.

The transmitter is fully differential and utilizes a current mode drive with a high impedance output. The drive current develops a differential swing in the range of 250 mV to 450 mV across a 100- termination load.

The parallel digital data is serially converted to a 7-bit serial bit stream that is transmitted over the 8 channel LVDS interface at 7x the input clock. The differential output clock channel transmits the output clock at the input clock frequency. While the differential output channels transmit the data at the 7x clock rate (1 bit time is 7x the input clock). The 7x serializer will synchronize and regenerate and input clock from 35 MHz to 112 MHz. Typical operation is at 65 MHz (15.4 ns), therefore, at a 7x clock rate,

1 bit time would be 2.2 ns. With data cycle times as small as 2.2 ns, propagation delay mismatch is critical, such that intra-channel skew (skew between the inverting and non-inverting output) must be kept minimal.

LIBG pin is a current reference on the LVDS interface. A 1.5-k pull down is required unless 855GME platform is being used with external graphics only option.

The following differential signal groups comprise the LVDS Interface. The topology rules for each group are defined in subsequent sections.

**Table 34. Signal Group and Signal Pair Names**

| Channel | Signal Group | Signal Pair Names |
|---|---|---|
| Channel A | Clocks | ICLKAM, ICLKAP |
| | Data Bus | IYAM[3:0], IYAP[3:0] |
| Channel B | Clocks | ICLKBM, ICLKBP |
| | Data Bus | IYBM[3:0], IYBP[3:0] |

## 7.2.1. LVDS Length Matching Constraints

The routing guidelines presented in the following subsections define the recommended routing topologies, trace width and spacing geometries, and absolute minimum and maximum routed lengths for each signal group. These recommendations are provided to achieve optimal SI and timing. In addition to the absolute length limits provided, more restrictive length matching requirements are also provided. The additional requirements further restrict the minimum to maximum length range of each signal group with respect to clock strobe, as required to guarantee adequate timing margins.

## 7.2.2. LVDS Package Length Compensation

As mentioned in Section 7.2.1, all length matching is done from GMCH die-pad to LVDS connector pin. The reason for this is to compensate for the package length variation across each signal group in order to minimize timing variance. The GMCH does not equalize package lengths internally as some previous GMCH components have, and therefore, the GMCH requires a length matching process. See Table 36 for the GMCH LVDS package lengths information.

Package length compensation should not be confused with length matching as discussed in the previous section. Length matching refers to constraints on the minimum and maximum length bounds of a signal group based on clock length, whereas package length compensation refers to the process of compensating for package length variance across a signal group. There is of course some overlap in that both affect the target length of an individual signal. Intel recommends that the initial route be completed based on the length matching formulas in conjunction with nominal package lengths and that package length compensation be performed as secondary operation.

## 7.2.3. LVDS Routing Guidelines

Each LVDS channel is required to be length matched to within ± 20 mils of the LVDS clock strobe signals. The two complementary signals in each clock strobe pair, as well as in each data pair, are also required to be length matched to within ± 20 mils of each other. See Table 35 for summary of LVDS signal group routing guidelines.

**Table 35. LVDS Signal Group Routing Guidelines**

| Parameter | Definition |
|---|---|
| Signal Group | LVDS |
| Topology | Differential Pair Point to Point |
| Reference Plane | Ground Referenced |
| Differential Mode Impedance (Zdiff) | 100 ± 15% |
| Nominal Trace Width | 4 mils |
| Nominal Pair Spacing (edge to edge) | 7 mils |
| Minimum Pair to Pair Spacing<br>(see exceptions for breakout region below) | 20 mils |
| Minimum Serpentine Spacing | 20 mils |
| Minimum Spacing to Other LVDS Signals<br>(see exceptions for breakout region below) | 20 mils |
| Minimum Isolation Spacing to non-LVDS Signals | 20 mils |
| Maximum Via Count | 2 (per line) |
| Package Length Range | 550 mils ± 150mils<br>(See LVDS package length Table 36 for exact lengths) |
| Total Length | Max 10” |
| Data to Clock Length Matching | Match all segments to within ± 20 mils of associated clock pair |
| Clock to Clock# Length Matching (Total Length) | Match clocks to ± 20 mils |
| Data to Data# Length Matching (Total Length) | Match data to ± 20 mils |
| **Breakout Exceptions**<br>(Reduced geometries for GMCH breakout region) | Breakout section should be as shorter as possible. Try to maintain trace width as 4 mils, spacing 7 mils, while the spacing between pairs can be 10-20 mils. |

The traces associated with the LVDS transmitter timing domain signals are differential traces terminated across 100 ± 15 % and should be routed as:

Strip-line only.

Isolate all other signals from the LVDS signals to prevent coupling from other sources onto the LVDS lines.

Use controlled impedance traces that match the differential impedance of your transmission medium (i.e. cable) and termination resistor

Run the differential pair trace lines as close together as possible as soon as they leave the IC, not greater than 10 mils. This will help eliminate reflections and ensure noise is coupled as common mode. Plus, noise induced on the differential lines is much more likely to appear as common mode, which is rejected by the receiver.

The LVDS transmitter timing domain signals have a maximum trace length of 10.0 inches. This maximum applies to all of the LVDS Transmitter signals.

Traces must be ground referenced and must not switch layers between the GMCH and connector.

When choosing cables, it is important to remember:

Use controlled impedance media. The differential impedance of cable LVDS uses should be 100 ± 15%. Cables should not introduce major impedance discontinuities that cause signal reflection.

Balanced cables (twisted pair) are usually better than unbalanced cables (ribbon cable, multi-conductor) for noise reduction and signal quality.

Cable length must be less than 16 inches.

**Table 36. LVDS Package Lengths**

| Signal Group | GMCH Signal Name | Package Trace Length (mils) | Signal Group | GMCH Signal Name | Package Trace Length (mils) |
|---|---|---|---|---|---|
| CHANNEL A | ICLKAP | 503.7 | CHANNEL B | ICLKAP | 502.0 |
| | ICLKAM | 498.8 | | ICLKAM | 499.1 |
| | IYAP0 | 399.6 | | IYBP0 | 359.8 |
| | IYAM0 | 385.4 | | IYBM0 | 353.7 |
| | IYAP1 | 487.5 | | IYBP1 | 524.7 |
| | IYAM1 | 466.2 | | IYBM1 | 516.6 |
| | IYAP2 | 572.6 | | IYBP2 | 623.3 |
| | IYAM2 | 566.2 | | IYBM2 | 604.2 |
| | IYAP3 | 643.2 | | IYBP3 | 441.8 |
| | IYAM3 | 637.8 | | IYBM3 | 441.7 |

# 7.3. Digital Video Out Port

The 852GME GMCH digital video out (DVO) port interface supports a wide variety of third party DVO compliant devices (e.g. TV encoder, TMDS transmitter or integrated TV encoder and TMDS transmitter).The 852GME has two dedicated DVO's (DVOB and DVOC). Intel's DVO port is a 1.5-V only interface that can support transactions up to 165 MHz. Some of the DVO port command signals may require voltage translation circuit depending on the third party device.

## 7.3.1. DVO Interface Signal Groups

### 7.3.1.1. DVOB Interface Signals

**Input Signals**

DVOBFLDSTL

**Output Data Signals**

DVOBHSYNC

DVOBVSYNC

DVOBBLANK#

DVOBD[11:0]

**Output Strobe Signals**

DVOBCLK (DVOBCLK[0])

DVOBCLK# (DVOBCLK[1])

### 7.3.1.2. DVOC Interface Signals

**Input Signals**

DVOCFLDSTL

**Output Data Signals**

DVOCHSYNC

DVOCVSYNC

DVOCBLANK#

DVOCD[11:0]

**Output Strobe Signals**

DVOCCLK (DVOCCLK[0])

DVOCCLK# (DVOCCLK[1])

#### 7.3.1.3. Common Signals for Both DVO Ports

**Input Signals**

DVOBCCLKINT

DVOBCINTR#

ADDID[7:0]

DVODETECT

**Voltage References, PLL Power Signals**

DVORCOMP

GVREF

## 7.3.2. DVOB and DVOC port Interface Routing Guidelines

For 852GME platforms, guidelines will apply for both interfaces.

### 7.3.2.1. Length Mismatch Requirements

The routing guidelines presented in the following subsections define the recommended routing topologies, trace width and spacing geometries, and absolute minimum and maximum routed lengths for each signal group, which are recommended to achieve optimal SI and timing. In addition to the absolute length limits provided in the individual guideline tables, more restrictive length matching requirements are also provided which further restrict the minimum to maximum length range of each signal group with respect to clock strobe, within the overall boundaries defined in the guideline tables, as required to guarantee adequate timing margins. These secondary constraints are referred to as length matching constraints. The amount of minimum to maximum length variance allowed for each group around the clock strobe reference length varies from signal group to signal group depending on the amount of timing variation, which can be tolerated. Refer to Table 37 for DVO length matching requirements.

**Table 37. DVO Interface Trace Length Mismatch Requirements**

| Data Group | Signal Matching to Strobe Clock | DVO Clock Strobes Associated With the Group | Clock Strobe Matching | Notes |
|---|---|---|---|---|
| DVOBD [11:0] | ± 100 mils | DVOBCLK[1:0] | ± 10 mils | 1,2 |
| DVOCD [11:0] | ± 100 mils | DVOCCLK[1:0] | ± 10 mils | 1,2 |

**NOTE:** Data signals of the same group should be trace length matched to the clock within ±100 mil including package lengths.

***All length matching formulas are based on GMCH die-pad to DVO device pin total length.*** Package length table are provided for all signals in order to facilitate this pad to pin matching.

### 7.3.2.2. Package Length Compensation

As mentioned in Section 7.3.2.1, all length matching is done from the GMCH die-pad to the DVO connector pin. The reason for this is to compensate for the package length variation across each signal group in order to minimize timing variance. The GMCH does not equalize package lengths internally as some previous GMCH components have, and therefore, the GMCH requires a length matching process. See Table 39 for the DVOB package lengths information and see Table 40 for DVOC package lengths information.

Package length compensation should not be confused with length matching as discussed in the previous section. Length matching refers to constraints on the minimum and maximum length bounds of a signal group based on clock length, whereas package length compensation refers to the process of adjusting out package length variance across a signal group. There is of course some overlap in that both affect the target length of an individual signal. Intel recommends that the initial route be completed based on the length matching formulas in conjunction with nominal package lengths and that package length compensation be performed as secondary operation.

### 7.3.2.3. DVOB and DVOC Routing Guidelines

Table 38 provides the DVOB and DVOC routing guideline summary.

**Table 38. DVOB and DVOC Routing Guideline Summary**

| Parameter | Definition |
|---|---|
| Signal Group | DVOBD [11:0], DVCBD [11:0] |
| Motherboard Topology | Point to point |
| Reference Plane | Ground Referenced |
| Characteristic Trace Impedance (Zo) | 55 ± 15% |
| Nominal Trace Width | Inner layers: 4 mils |
| Minimum Spacing to Trace Width Ratio | 2 to 1 (e.g. 8 mil space to 4 mil trace) |
| Minimum Isolation Spacing to non-DVO Signals | 20 mils |
| Minimum Spacing to Other DVO Signals | 12 mils (see exceptions for breakout region below) |
| Minimum Spacing of DVOBCLK [1:0] or DVOCCLK [1:0] to any other signals | 12 mils |
| Package Length Range – P1 | See Table 39 and Table 40 for package lengths. |
| Total Length – | Max 6” |
| Data to Clock Strobe Length Matching Requirements | + 100 mils (See Table 37 for length matching requirements) |
| CLK0 to CLK1 Length Matching Requirements | + 10 mils (See Table 37 for length matching requirements.) |

The routing guideline recommendations in this section apply for both interfaces. Refer to Table 39 for GMCH DVOB package lengths and Table 40 for GMCH DVOC package lengths. The DVO interface signals are routed point to point as follows:

All signals should be routed as striplines (inner layers).

All signals in a signal group should be routed on the same layer. Routing studies have shown that these guidelines can be met. The trace length and trace spacing requirements ***must*** not be violated by any signal.

Route the DVOBCLK[1:0] or DVOCCLK[1:0] signal pairs 4 mils wide and 8 mils apart with a max trace length of 6in. This signal pair should be a minimum of 12 mils from any adjacent signals.

In order to break out of the 852GME GMCH, the DVOB and/or DVOC data signals can be routed with a trace width of 4 mils and a trace spacing of 7 mils. The signals should be separated to a trace width of 4 mils and a trace spacing of 8 mils within 0.3 inches of the GMCH component.

**Table 39. DVOB Interface Package Lengths**

| Signal | Pin Number | Package Length (mils) |
|---|---|---|
| DVOBBLANK# | L2 | 583 |
| DVOBCCLKINT | M3 | 520 |
| DVOBCINTR# | G2 | 712 |
| DVOBCLK | P3 | 475 |
| DVOBCLK# | P4 | 439 |
| DVOBD[0] | R3 | 489 |
| DVOBD[1] | R5 | 439 |
| DVOBD[2] | R6 | 343 |
| DVOBD[3] | R4 | 415 |
| DVOBD[4] | P6 | 409 |
| DVOBD[5] | P5 | 387 |
| DVOBD[6] | N5 | 466 |
| DVOBD[7] | P2 | 553 |
| DVOBD[8] | N2 | 568 |
| DVOBD[9] | N3 | 504 |
| DVOBD[10] | M1 | 611 |
| DVOBD[11] | M5 | 510 |
| DVOBFLDSTL | M2 | 566 |
| DVOBHSYNC | T6 | 339 |

**Table 40. DVOC Interface Package Lengths**

| Signal | Pin Number | Package Length (mils) |
|---|---|---|
| DVOCBLANK# | L3 | 541 |
| DVOCCLK | J3 | 601 |
| DVOCCLK# | J2 | 675 |
| DVOCD[0] | K5 | 489 |
| DVOCD[1] | K1 | 692 |
| DVOCD[2] | K3 | 622 |
| DVOCD[3] | K2 | 685 |
| DVOCD[4] | J6 | 536 |
| DVOCD[5] | J5 | 518 |
| DVOCD[6] | H2 | 720 |
| DVOCD[7] | H1 | 771 |
| DVOCD[8] | H3 | 649 |
| DVOCD[9] | H4 | 625 |
| DVOCD[10] | H6 | 521 |
| DVOCD[11] | G3 | 762 |
| DVOCFLDSTL | H5 | 566 |
| DVOCHSYNC | K6 | 491 |
| DVOCVSYNC | L5 | 440 |

#### 7.3.2.4. DVOB and DVOC Port Termination

The DVO interface does not require external termination.

## 7.3.3. DVOB and DVOC Assumptions, Definitions, and Specifications

The source synchronous solution space consists of all designs in which the flight time mismatch between a strobe and its associated data is less than the total allowable skew:

$$\mathbf{T}_{skew} = \mathbf{T}_{\mathbf{flight}data} - \mathbf{T}_{\mathbf{flight}strobe}$$

Where $\mathbf{T}_{\mathbf{flight}data}$ and $\mathbf{T}_{\mathbf{flight}strobe}$ are the driver-pad-to-receiver-pin flight times of the data and the strobe respectively.

The DVO physical interface is a point-to-point topology using 1.5-V signaling. The DVO uses a 165-MHz clock.

The flight time skew simulations simulate all parameters that could cause a skew between two signals, including motherboard and add-in card line lengths, effective capacitance in the buffer models, crosstalk on each of the different interconnect combinations, data pattern dependencies, and ISI induced skews.

## 7.3.4. DVOB and DVOC Simulation Method

A model for simulation purposes is shown in Figure 43. The DVO component is a third party-chip.

**Figure 43. DVOB and DVOC Simulations Model**

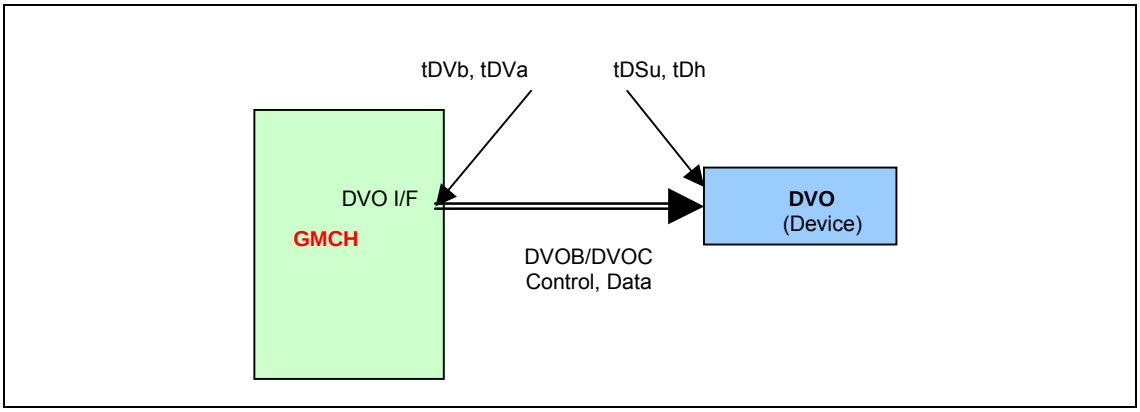
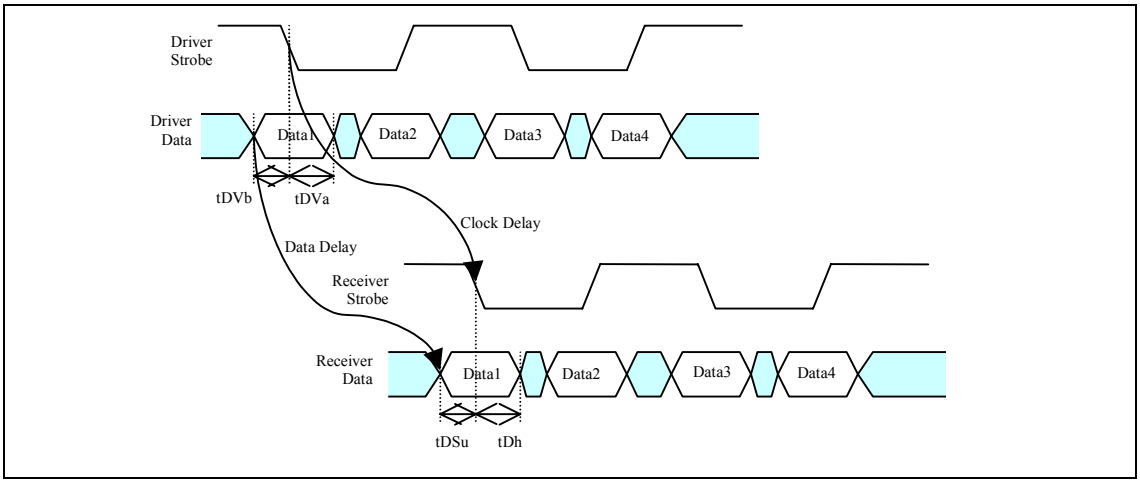



**Figure 44. Driver-Receiver Waveforms Relationship Specification**




The setup margin and the hold margin for a particular design depends on the values of the data valid times and the data setup and hold times on both the driver and the receiver sides. However, note that available margins are not absolute values. Any skew due to routing and loading differences, any coupling differences in the parallel traces, and any effects of SSO (ISI, ground bounce, etc.) should be accounted for in the timing budget as they will reduce the total available margin for the design.

**Table 41. Allowable Interconnect Skew Calculation**

| Component | Skew Element | Symbol | Setup | Hold | Units |
|---|---|---|---|---|---|
| Driver | Data Valid before Strobe | tDVb | 570 | | ps |
| | Data Valid after Strobe | tDVa | | 770 | ps |
| Interconnect | Allowable Skew | | TBD | TBD | ps |
| Receiver | Data Setup to Strobe | tDSu | TBD | | ps |
| | Data Hold from Strobe | tDh | | TBD | ps |

**NOTE:** All numbers in this table are from the 852GME GMCH specification documents that are applicable for this interface. For third party receiver devices, please refer to appropriate third party vendor specifications.

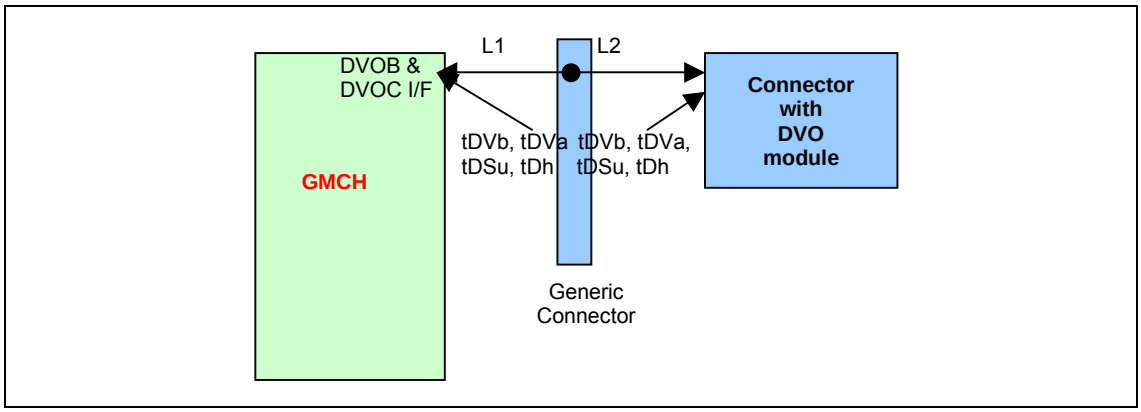
# 7.4. DVOB and DVOC port Flexible (Modular) Design

The GMCH supports flexible design interfaces described in this section.

## 7.4.1. DVOB and DVOC Module Design

The 852GME GMCH supports a DVO module design connected to the GMCH through a generic connector. Simulation method is the same as in Section 7.3.4. Lengths L1 and L2 are determined by simulation as L1= 4 inches and L2= 2 inches. Refer to Figure 46 for the generic connector parasitic model.

**Figure 45. DVO Enabled Simulation Model**




All signals should be routed as striplines (inner layers).All signals in a signal group should be routed on the same layer. Routing studies have shown that these guidelines can be met. The trace length and trace spacing requirements ***must*** not be violated by any signal. Trace length mismatch for all signals within a signal group should be as close to ± 100 mils with respect to the strobe clocks as possible to provide optimal timing margin.

Table 42 shows DVO enabled routing guideline summary.

**Table 42. DVO Enabled Routing Guideline Summary**

| Signal | Maximum Length | Trace Width | Trace Spacing | Length Mismatch | Notes |
|---|---|---|---|---|---|
| DVO Timing Domain | L1=4 in<br>L2=2 in | 4 mils | 8 mils | ± 100 mils | |

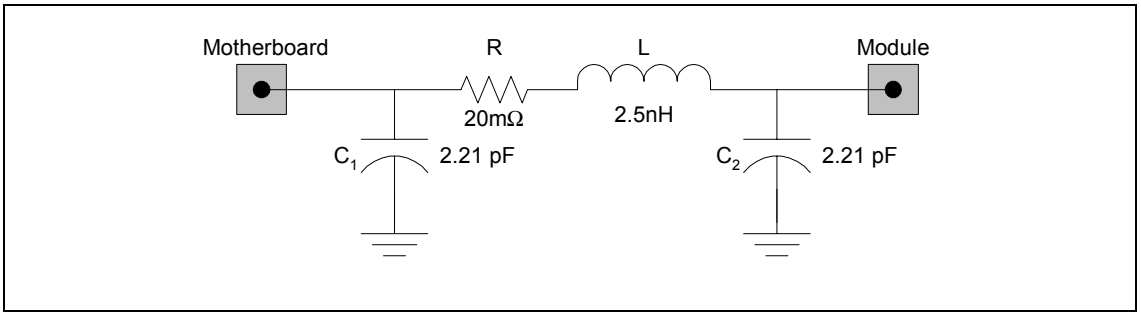
For DVO module case, the simulation model is the same as Figure 45 and the routing guideline is the same as in

Table 42; each strobe pair must be separated from other signals by at least 12 mils. For multiplexed design, more conservative length mismatch (± 0.1 inches) is adopted.

#### 7.4.1.1. Generic Connector Model

Figure 46 shows the generic connector model used in simulation for flexible DVO implementation. This is only for reference. Actual connector may have different parasitic values. Designs using this approach need to be simulated first.

**Figure 46. Generic Module Connector Parasitic Model**




## 7.5. DVO GMBUS and DDC Interface Considerations

The GMCH DVOB and/or DVOC port controls the video front-end devices via the GMBUS (I2C) interface. DDCADATA and DDCACLK should be connected to the CRT connector. The GMBUS should be connected to the DVO device, as required by the specifications for those devices. The protocol and bus may be used to configure registers in the TV encoder, TMDS transmitter, or any other external DVI device. The GMCH also has an option to utilize the DDCPCLK and DDCPDATA to collect EDID (Extended Display Identification) from a digital display panel.

Pull-ups (or pull-ups with the appropriate value derived from simulating the signal) typically ranging from 2.2 k to 10 k are required on each of these signals.

The following GMCH signal groups list the five possible GMBUS pairs.

**Table 43. GMBUS Pair Mapping and Options**

| Pair # | Signal Name | Buffer Type | Description | Notes |
|---|---|---|---|---|
| 0 | DDCADATA | 3.3 V | DDC for Analog monitor (CRT) connection. | This can not be shared with other DDC or I2C pairs due to legacy monitor issues. |
| | DDCACLK | | | |
| 1 | LCLKCTRLA | 3.3 V | For control of SSC clock generator devices down on motherboard. | If SSC is not supported then can be used for DVOB or DVOC GMBUS. |
| | LCLKCTRLB | | | |
| 2 | DDCPDATA | 3.3 V | DDC for Digital Display connection via the integrated LVDS display port for support for EDID panel. | If EDID panels are not supported. Can optionally use as GMBUS for DVOB or DVOC. |
| | DDCPCLK | | | |
| 3 | MDVIDATA | 1.5 V | GMBUS control of DVI devices (TMDS or TV encoder) | Can optionally use as GMBUS for DVOB or DVOC. |
| | MDVICLK | | | |
| 4 | MI2CDATA | 1.5 V | GMBUS control of DVI devices (TMDS or TV encoder) | Can optionally use as GMBUS for DVOB or DVOC. |
| | MI2CCLK | | | |
| 5 | MDDCDATA | 1.5 V | DDC for Digital Display connection via TMDS device | Can optionally use as GMBUS for DVOB or DVOC. |
| | MDDCCLK | | | |

**NOTE:** All GMBUS pairs can be optionally programmed to support any interface and is programmed through the BMP utility.

If any of GMBUS pairs (expect DDCADATA/DDCCLK for CRT) are not used, 2.2 k – 100 k pull-up (or pull-ups with the appropriate value derived from simulating the signal), resistors are required except for LCLKCTRLA/LCLKCTRLB GMBUS pair. This will prevent the GMCH DVOB interface from confusing noise on these lines for false cycles.

## 7.5.1. Leaving the GMCH DVOB or DVOC Port Unconnected

If the motherboard does not implement any of the possible video devices with the DVO port, please follow the guidelines recommended on the motherboard. DVO Output signals may be left unconnected if they are not used.

Pull-down resistors are required for the following signals if not used:

DVOBFLDSTL

DVOCFLDSTL

DVOBCCLKINT

Pull-up resistors are required for the following signals if not used:

DVOBCINTR#

## 7.6. Miscellaneous Input Signals and Voltage Reference

ADDID[7]: Pulldown to ground with a 1-k resistor when using the DVOB or DVOC port. This is a VBIOS strapping option to load the TPV AIM module for DVOB and DVOC port. Pulldown not required if DVOB or DVOC is not enabled.

ADDID[6:0]: Leave unconnected (NC).

DVODETECT: Leave unconnected (NC) when using the DVOB or DOVC port.

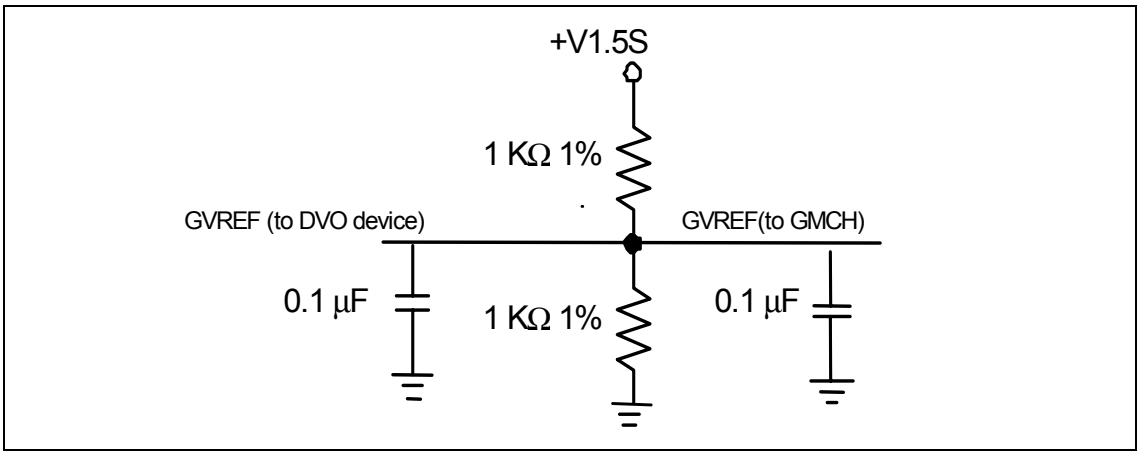
AGPBUSY#: Connect directly to ICH4-M. A 10-k, pullup resistor is required, unless using 852PM platform or 852GME platform with external graphics

DVORCOMP is used to calibrate the DVOB buffers. It should be connected to ground via a 40.2- resistor using a routing guideline of 10-mil trace and 20-mil spacing.

DPMS: connects to 1.5 V version of the ICH4-M's SUSCLK or a clock that runs during S1.

GVREF: Reference voltage for the DVOB and DVOC input buffers. Refer to the figure below for proper signal conditioning.

**Figure 47. GVREF Reference Voltage**



# 8. AGP Port Design Guidelines

For detailed AGP interface functionality (e.g., protocols, rules, signaling mechanisms), refer to the latest *AGP Interface Specification*, Revision 2.0, which can be obtained from http://www.agpforum.org.

## 8.1. AGP Interface

The852GME/852GMV/852PMAGP buffers operate in only one mode: 1.5-V drive, not 3.3-V safe. This mode is compliant with the AGP 2.0 Specification.

AGP 4X, 2X and 1X must operate at 1.5 V. The AGP interface supports up to 4X AGP signaling. AGP semantic cycles to DRAM are not snooped on the host bus.

The MCH/GMCH supports PIPE# or SBA [7:0] AGP address mechanisms, but not both simultaneously. Either the PIPE# or the SBA [7:0] mechanism must be selected during system initialization.

The AGP interface is clocked from a 66-MHz clock. The AGP interface is asynchronous to the host bus, system memory, and internal graphics device. When AGP interface has been enabled, the internal graphics will be disabled using GMCH strapping option. The AGP interface is synchronous to the hub interface with a clock ratio of 1:1 (66 MHz : 66 MHz).

The GMCH multiplexes the AGP signal interface with two DVO ports. These DVO ports are capable of supporting a variety of digital display devices such as TMDS transmitters and TV-Out encoders. It is possible to use the DVO ports in dual-channel mode to support higher resolutions and refresh rates (single channel mode is limited to a 165-MHz pixel clock rate).

### 8.1.1. AGP 2.0

The AGP Interface Specification, Revision 2.0, enhances the functionality of the original AGP Interface Specification, Revision 1.0, by allowing 4X data transfers (i.e., 4 data samples per clock), and 1.5-volt operation. The 4X operation of the AGP interface provides for "quad-pumping" of the AGP AD (address/data) and SBA (side-band addressing) buses. That is, data is sampled four times during each 66-MHz AGP clock. This means that each data cycle is ¼ of a 15-ns (66-MHz) clock or 3.75 ns. It is important to understand that 3.75 ns is the data cycle time, not the clock cycle time. During 2X operation, data is sampled twice during a 66-MHz clock cycle.

Therefore, the data cycle time is 7.5 ns. To allow for these high-speed data transfers, the 2X mode of AGP operation uses source-synchronous data strobing. During 4X operation, the AGP interface uses differential source-synchronous strobing.

With data cycle times as small as 3.75 ns and setup/hold times of 1 ns, propagation delay mismatch is critical. In addition to reducing propagation delay mismatch, it is important to minimize noise. Noise on the data lines will cause the settling time to be long. If the mismatch between a data line and the associated strobe is too great, or if there is noise on the interface, incorrect data will be sampled. The low-voltage operation on AGP (1.5 V) requires even more noise immunity.

## 8.1.2. AGP Interface Signal Groups

The signals on the AGP interface are broken into three groups: 1X timing domain signals, 2X/4X timing domain signals, and miscellaneous signals. Each group has different routing requirements.

In addition, within the 2X/4X timing domain signals, there are three sets of signals. All signals in the 2X/4X timing domain must meet minimum and maximum trace length requirements, as well as trace width and spacing requirements. Because of the multiplexed AGP/DVO interface, there are trace length matching requirements within each set of 2X/4X signals, as well as between sets of 2X/4X signals. The signal groups are listed in following table.

**Table 44. AGP 2.0 Signal Groups**

| 1X Signals | 2X signals | 4X Signals |
|---|---|---|
| CLK (3.3 V)<br>GRBF#<br>GWBF#<br>GST_[2:0]<br>GPIPE#<br>GREQ#<br>GGNT#<br>GPAR<br>GFRAME#<br>GIRDY#<br>GTRDY#<br>GSTOP#<br>GDEVSEL#<br>GAD_[31:0]<br>GC/BE_[3:0]#<br>GADSTB_[1:0] | 2X signals include all 1X signals and:<br>GADSTB_[1:0]<br>GSBSTB<br>GAD_[31:0] signals and associated GC/BE_[3:0]# signals are running at 2X mode. | 4X signals include all 1X signals and:<br>GADSTB_[1:0]<br>GADSTB_[1:0]#<br>GSBSTB<br>GSBSTB#<br>GAD_[31:0] signals and associated GC/BE_[3:0]# signals are running at 4X mode. |

**Table 45. AGP 2.0 Data/Strobe Associations**

| Data | Associated Strobe in 1X | Associated Strobe in 2X | Associated Strobes in 4X |
|---|---|---|---|
| AD[15:0] and C/BE[1:0]# | Strobes are not used in 1X mode. All data is sampled on rising clock edges. | AD_STB0 | AD_STB0, AD_STB0# |
| AD[31:16] and C/BE[3:2]# | Strobes are not used in 1X mode. All data is sampled on rising clock edges. | AD_STB1 | AD_STB1, AD_STB1# |
| SBA[7:0] | Strobes are not used in 1X mode. All data is sampled on rising clock edges. | SB_STB | SB_STB, SB_STB# |

The routing guidelines for each group of signals (1X timing domain signals, 2X/4X timing domain signals, and miscellaneous signals) will be addressed separately.

# 8.2. AGP Routing Guidelines

## 8.2.1. 1x Timing Domain Routing Guidelines

### 8.2.1.1. Trace Length Requirements for AGP 1X

This section contains information on the 1X timing domain routing guidelines. The AGP 1X timing domain signals (refer to Table 46) have a maximum trace length of 10 inches. The target impedance is 55- ± 15%. This maximum applies to ALL of the signals listed as 1X timing domain signals in Table 46. In addition to this maximum trace length requirement (refer to Table 46 and Table 47) these signals must meet the trace spacing and trace length mismatch requirements in Sections 8.2.1.2 and 8.2.1.3.

**Table 46. Layout Routing Guidelines for AGP 1X Signals**

| 1X signals | Max. Length (inches) | Width (mils) | Space (mils) |
|---|---|---|---|
| CLK_AGP_SLT | 10 | 4 | 4 |
| AGP_PIPE# | 10 | 4 | 4 |
| AGP_RBF# | 10 | 4 | 4 |
| AGP_WBF# | 10 | 4 | 4 |
| AGP_ST[2:0] | 10 | 4 | 4 |
| AGP_FRAME# | 10 | 4 | 4 |
| AGP_IRDY# | 10 | 4 | 4 |
| AGP_TRDY# | 10 | 4 | 4 |
| AGP_STOP# | 10 | 4 | 4 |
| AGP_DEVSEL# | 10 | 4 | 4 |
| AGP_REQ# | 10 | 4 | 4 |
| AGP_GNT# | 10 | 4 | 4 |
| AGP_PAR | 10 | 4 | 4 |

#### 8.2.1.2. Trace Spacing Requirements

AGP 1X timing domain signals (refer to Table 46) can be routed with 4-mil minimum trace separation.

#### 8.2.1.3. Trace Length Mismatch

There are no trace length mismatch requirements for 1X timing domain signals. These signals must meet minimum and maximum trace length requirements.

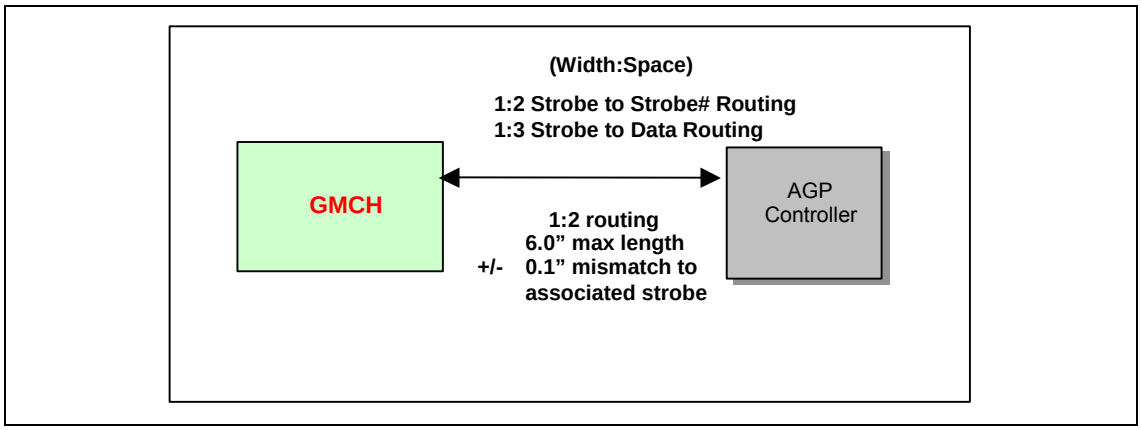
### 8.2.2. 2x/4x Timing Domain Routing Guidelines

#### 8.2.2.1. Trace Length Requirements for AGP 2X/4X

These trace length guidelines apply to ALL of the signals listed as 2X/4X timing domain signals in Table 47. In addition to these maximum trace length requirements, these signals must meet the trace spacing and trace length mismatch requirements in Sections 8.2.2.2 and 8.2.2.3.

The maximum line length and mismatch requirements are dependent on the routing rules used on the motherboard. These routing rules were created to give design freedom by making tradeoffs between signal coupling (trace spacing) and line lengths. These routing rules are divided by trace spacing. In 1:2 spacing, the distance between the traces is two times the width of traces.

**Figure 48. AGP Layout Guidelines**




For 2X/4X lines in AGP interface, the max length is 6.0 inches (pin to pin) and 1:2 trace spacing is required. 2X signals must be matched to their associated strobe within 0.1 inch. 4X signals must be matched to both of their associated strobes within 0.1 inch. Reduce line length mismatch to ensure added margin.

### 8.2.2.2. Trace Spacing Requirements

AGP 2X/4X timing domain signals (refer to Table 47) must be routed as documented in Table 47. They should be routed using 4-mil traces. Additionally, the signals can be routed with 5-mil spacing when breaking out of the GMCH/MCH. The routing must widen to the requirement in Table 48 within 0.3 inches of the GMCH/MCH package.

Since the strobe signals (AD_STB0, AD_STB0#, AD_STB1, AD_STB1#, SB_STB, and SB_STB#) act as clocks on the source synchronous AGP interface, special care should be taken when routing these signals. Because each strobe pair is truly a differential pair, the pair should be routed together (e.g. AD_STB0 and AD_STB0# should be routed next to each other). The two strobes in a strobe pair should be routed on 4-mil traces with 8 mils of space (1:2) between them. This pair should be separated from the rest of the AGP signals (and all other signals) by at least 15 mils (1:3). The strobe pair must be length matched to less than ± 0.1 inches (that is, a strobe and its compliment must be the same length within ± 0.1 inches).

**Table 47. Layout Routing Guidelines for AGP 2X/4X Signals**

| Signal | Maximum Length (inch) | Trace Space (mils) (4 mil traces) | Length Mismatch (inch) | Relative To | Notes |
|---|---|---|---|---|---|
| 2X/4X Timing Domain Set#1 | 6 | 8 | ± 0.1 | AGP_ADSTB0 and AGP_ADSTB0# | AGP_ADSTB0, AGP_ADSTB0# must be the same length (±10 mils) |
| 2X/4X Timing Domain Set#2 | 6 | 8 | ± 0.1 | AGP_ADSTB1 and AGP_ADSTB1# | AGP_ADSTB1, AGP_ADSTB1# must be the same length (±10 mils) |
| 2X/4X Timing Domain Set#3 | 6 | 8 | ± 0.1 | AGP_SBSTB and AGP_SBSTB # | AGP_SBSTB, AGP_SBSTB# must be the same length (±10 mils) |

### 8.2.2.3. Trace Length Mismatch Requirements

**Table 48. AGP 2.0 Data Lengths Relative to Strobe Length**

| Max Trace Length | Trace Spacing | Strobe Length | Min Trace Length | Max Trace Length |
|---|---|---|---|---|
| < 6 in | 1:2 | X | X – 0.1 in | X + 0.1 in |

The trace length minimum and maximum (relative to strobe length) should be applied to each set of 2X/4X timing domain signals **independently**. If AD_STB0 is 5 inches and ADSTB0# is 5.01 inches, then AD[15:0] and C/BE[1:0] must be between 4.91 inches and 5.1 inches. However, AD_STB1 and ADSTB1# can be 3.5 inches and 3.51 inches (and therefore AD[31:16] and C/BE#[3:2] must be between 3.41 inches and 3.6 inches). In addition, all 2X/4X timing domain signals must meet the maximum trace length requirements.

All signals should be routed as strip lines (inner layers).

All signals in a signal group should be routed on the same layer. Routing studies have shown that these guidelines can be met. The trace length and trace spacing requirements ***must*** not be violated by any signal. Trace length mismatch for all signals within a signal group should be as close to 0 inches as possible to provide optimal timing margin.

The strobe pair must be length matched to less than ± 0.01 inches (that is, a strobe and its compliment must be the same length within ± 0.01 inches).

Table 49 shows the AGP 2.0 routing summary.

**Table 49. AGP 2.0 Routing Guideline Summary**

| Signal | Maximum Length | Trace Spacing (4 mil traces) | Length Mismatch | Relative To | Notes |
|---|---|---|---|---|---|
| 1X Timing Domain | 10 in | 4 mils | No Requirement | N/A | None |
| 2X/4X Timing Domain Set#1 | 6 in | 8 mils | ± 0.1 in | AD_STB0 and AD_STB0# | AD_STB0, AD_STB0# must be the same length |
| 2X/4X Timing Domain Set#2 | 6 in | 8 mils | ± 0.1 in | AD_STB1 and AD_STB1# | AD_STB1, AD_STB1# must be the same length |
| 2X/4X Timing Domain Set#3 | 6 in | 8 mils | ± 0.1 in | SB_STB and SB_STB# | SB_STB, SB_STB# must be the same length |

## 8.2.3. AGP Clock Skew

The maximum total AGP clock skew, between the GMCH/MCH and the graphics component, is 1 ns for all data transfer modes. This 1 ns includes skew and jitter, which originates on the motherboard, add-in module (if used), and clock synthesizer. Clock skew must be evaluated not only at a single threshold voltage, but also at all points on the clock edge that falls in the switching range. The 1 ns skew budget is divided such that the motherboard is allotted 0.9 ns of clock skew (the motherboard designer shall determine how the 0.9 ns is allocated between the board and the synthesizer).

## 8.2.4. AGP Signal Noise Decoupling Guidelines

The main focus of these guidelines is to minimize signal integrity problems on the AGP interface of the Intel chipset GMCH/MCH. The following guidelines are not intended to replace thorough system validation on Intel chipset-based products.

A minimum of six 0.01-µF capacitors are required and must be as close as possible to the MCH-M. These should be placed within 70 mils of the outer row of balls on the GMCH/MCH for VDDQ decoupling. Ideally, this should be as close as possible.

The designer should evenly distribute placement of decoupling capacitors in the AGP interface signal field.

Intel recommends that the designer use a low-ESL ceramic capacitor, such as with a 0603 body-type X7R dielectric.

In order to add the decoupling capacitors within 70 mils of the GMCH/MCH and/or close to the vias, the trace spacing may be reduced as the traces go around each capacitor. The narrowing of space between traces should be minimal and for as short a distance as possible (1.0 inch max.).

In addition to the minimum decoupling capacitors, the designer should place bypass capacitors at vias that transition the AGP signal from one reference signal plane to another. One extra 0.01 uF capacitor per 10 vias is required. The capacitor should be placed as close as possible to the center of the via field.

## 8.2.5. AGP Interface Package Lengths

**Table 50. AGP Interface Package Lengths**

| Signal | Pin Number | Package Length (mils) |
|---|---|---|
| GAD0 | T6 | 339 |
| GAD1 | T5 | 362 |
| GAD2 | R5 | 440 |
| GAD3 | R3 | 489 |
| GAD4 | R4 | 415 |
| GAD5 | R6 | 343 |
| GAD6 | P5 | 387 |
| GAD7 | P6 | 409 |
| GAD8 | N5 | 466 |
| GAD9 | N3 | 504 |
| GAD10 | N2 | 568 |
| GAD11 | M5 | 510 |
| GAD12 | M1 | 611 |
| GAD13 | M3 | 520 |
| GAD14 | M2 | 566 |
| GAD15 | T7 | 296 |
| GAD16 | L5 | 440 |
| GAD17 | K6 | 491 |
| GAD18 | L3 | 541 |
| GAD19 | K5 | 489 |
| GAD20 | K1 | 692 |
| GAD21 | K3 | 622 |
| GAD22 | K2 | 685 |
| GAD23 | J6 | 536 |
| GAD24 | H1 | 772 |
| GAD25 | H2 | 720 |
| GAD26 | H4 | 625 |
| GAD27 | H3 | 649 |
| GAD28 | G3 | 762 |
| GAD29 | H6 | 521 |
| GAD30 | G2 | 712 |
| GAD31 | H5 | 566 |

| Signal | Pin Number | Package Length (mils) |
|---|---|---|
| GADSTB_0 | P3 | 475 |
| GADSTBB_0 | P4 | 439 |
| GADSTB_1 | J3 | 601 |
| GADSTBB_1 | J2 | 675 |
| GSBA_0 | E5 | 686 |
| GSBA_1 | F5 | 617 |
| GSBA_2 | E3 | 738 |
| GSBA_3 | E2 | 865 |
| GSBA_4 | G5 | 668 |
| GSBA_5 | F4 | 688 |
| GSBA_6 | G6 | 518 |
| GSBA_7 | F6 | 613 |
| GSBSTB | F2 | 799 |
| GSBSTBB | F3 | 761 |
| GPIPEB | D5 | 644 |
| GCBEB_0 | P2 | 553 |
| GCBEB_1 | L2 | 583 |
| GCBEB_2 | L4 | 515 |
| GCBEB_3 | J5 | 518 |
| GST_0 | C4 | 750 |
| GST_1 | C3 | 797 |
| GST_2 | C2 | 856 |
| GRBFB | D3 | 962 |
| GWBFB | D2 | 947 |
| GFRAMEB | M6 | 486 |
| GIRDYB | K7 | 751 |
| GTRDYB | N7 | 350 |
| GSTOPB | P7 | 423 |
| GDEVSELB | N6 | 399 |
| GREQB | B3 | 762 |
| GGNTB | B2 | 849 |
| GPAR | L7 | 623 |

## 8.2.6. AGP Routing Ground Reference

Intel strongly recommends that at least the following critical signals be referenced to ground from the MCH and GMCH to an AGP controller connector using a minimum number of vias on each net:

AD_STB0

AD_STB0#

AD_STB1

AD_STB1#

SB_STB

SB_STB#

G_TRDY#

G_IRDY#

G_GNT#

ST[2:0].

## 8.2.7. Pull-ups

The AGP 2.0 Specification requires AGP control signals to have pull-up resistors to VDDQ to ensure they contain stable values when no agent is actively driving the bus. Also, the AD_STB[1:0]# and ST_STB# strobes require pull-down resistors to GND. The Intel 852GME/852GMV/852PMchipset MCH/GMCH has integrated many of these pull-up/pull-down resistors on the AGP interface and a few other signals not required by the AGP 2.0 Specification. Pull-ups are allowed on any signal except AD_STB[1:0]# and SB_STB#.

The Intel chipset GMCH has no support for the PERR# and SERR# pins of an AGP graphics controller that supports PERR# and SERR#. Pull-ups to a 1.5-V source are required down on the motherboard in such cases.

### Table 51. AGP Pull-Up/Pull-Down Requirements and Straps

| Signal | AGP 2.0 Signal Pull-Up/ Pull-Down Requirements | MCH-M Integrated Pull-Up/ Pull-Down | Notes |
|---|---|---|---|
| DEVSEL# | | Pull-Up | |
| FRAME# | | Pull-Up | |
| GNT# | | Pull-Up | |
| INTA# | Pull-Up | | 3, 5 |
| INTB# | Pull-Up | | 3, 5 |
| IRDY# | | Pull-Up | |
| PERR# | Pull-Up | | 2 |
| PIPE# | | Pull-Up | |
| RBF# | | Pull-Up | |
| REQ# | | Pull-Up | 1 |
| SERR# | Pull-Up | | 2 |
| ST[2:0] | | Pull-Down | 4 |
| STOP# | Pull-Up | Pull-Up | |
| TRDY# | | Pull-Up | |
| WBF# | | Pull-Up | |
| AD_STB[1:0] | | Pull-Up | |
| AD_STB[1:0]# | | Pull-Down | |
| SB_STB | | Pull-Up | |
| SB_STB# | | Pull-Down | |
| SBA[7:0] | | Pull-Up | 1 |

**NOTES:**

1. The Intel chipset GMCH has integrated pull-ups to ensure that these signals do not float when there is no add-in card in the connector.
2. The Intel chipset MCH-M does not implement the PERR# and SERR# signals. Pull-ups on the motherboard are required for AGP graphics controllers that implement these signals.
3. The Intel chipset MCH does not implement interrupt signals. AGP graphics controller's INTA# and INTB# signals must but routed to the system PCI interrupt request handler where the pull-up requirement should be met as well. For 852GME/PM /ICH4-M chipset-based systems, they can be routed to the ICH4-M's PIRQ signals that are open drain and require pull-ups on the motherboard.
4. ST[1:0] provide the strapping options for 100-MHz FSB operation and DDR memory, respectively.
5. INTA# and INTB# should be pulled to 3.3 V, not VDDQ.
6. The pull-up/pull-down resistor value requirements are shown in Table 52.

### Table 52. AGP 2.0 Pull-up Resistor Values

| Rmin | Rmax |
|---|---|
| 4 k | 16 k |

The recommended AGP pull-up/pull-down resistor value is 8.2 k .

## 8.2.8. AGP VDDQ and VCC

AGP specifies two separate power planes: VCC and VDDQ. VCC is the core power for the graphics controller and VDDQ is the interface voltage.

## 8.2.9. VREF Generation for AGP 2.0 (2X and 4X)

### 8.2.9.1. 1.5-V AGP Interface (2X/4X)

The voltage divider networks consist of AC and DC elements. The reference voltage that should be supplied to the Vref pins of the GMCH/MCH and the graphics controller is ½ * VDDQ. Two, 1-k ± 1% resistors can be used to divide VDDQ down to the necessary voltage level.

The Vref divider network should be placed as close to the AGP interface as is practical to get the benefit of the common mode power supply effects. However, the trace spacing around the Vref signals must be a minimum of 25 mils to reduce crosstalk and maintain signal integrity.

## 8.2.10. AGP Compensation

The 852GME chipset MCH-M AGP interface supports resistive buffer compensation. For PCBs with characteristic impedance of 55 , tie the GRCOMP pin to a 40.2 ± 1% pull-down resistor (to ground) via a 10-mil wide, very short ( 0.5 inches) trace.

**AGP Link:**
http://www.intel.com/technology/agp/info.htm

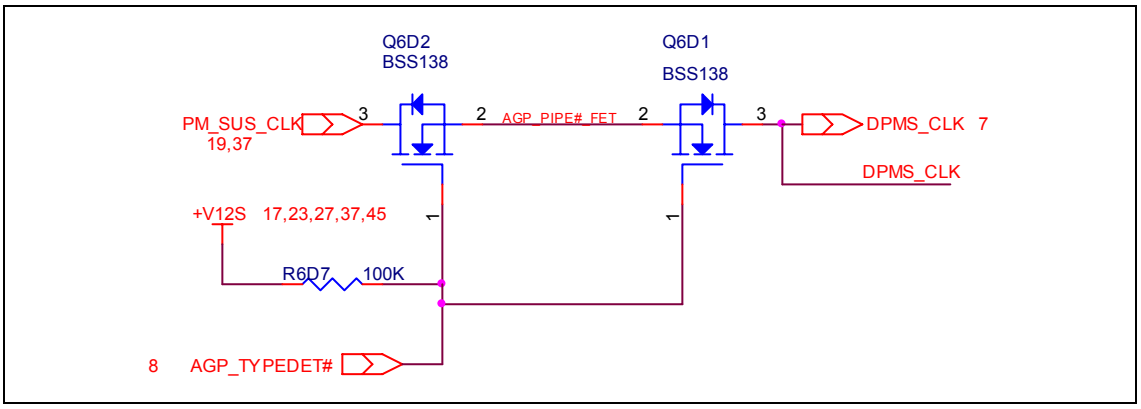
**AGP StressTool Link:**
http://www.intel.com/technology/agp/downloads/agp_stress.htm

## 8.2.11. PM_SUS_CLK/AGP_PIPE# Design Consideration

The following design consideration provides the option to support both AGP and DVO devices with one ADD Connector. Refer to Figure 49 and customer reference schematics for more detail.

The GMCH expects either the PM_SUS_CLK signal from the ADD connector when there is a no AGP device or the AGP_PIPE# signal when there is an AGP device. The AGP_TYPEDET# signal is driven high when no AGP card is detected, allowing DPMS_CLK to be driven by PM_SUS_CLK. In the case where an AGP card is detected, AGP_TYPE# signal goes high which allows DMPS_CLK to be driven by AGP_PIPE#.

**Figure 49. DPMS Circuit**

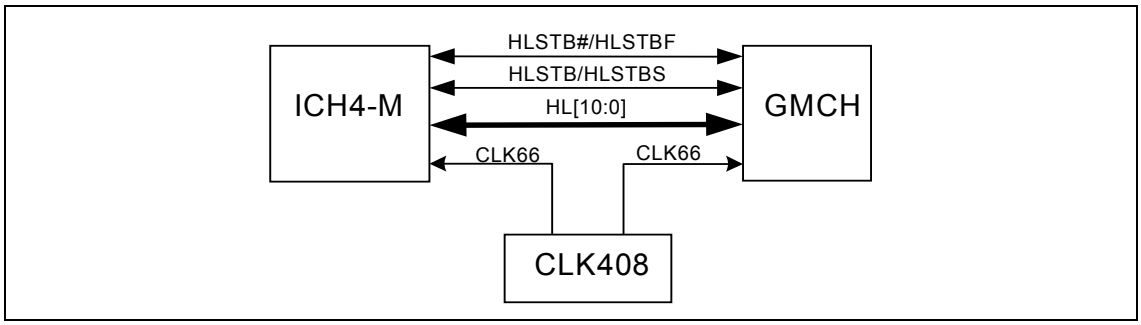


# 9. Hub Interface

The GMCH and ICH4-M pin-map assignments have been optimized to simplify the hub interface routing between these devices. Intel recommends that the hub interface signals be routed directly from the GMCH to the ICH4-M with all signals referenced to VSS. Layer transitions should be kept to a minimum. If a layer change is required, use only two vias per net and keep all data signals and associated strobe signals on the same layer.

The hub interface signals are broken into two groups: data signals (HL) and strobe signals (HLSTB). For the 11-bit hub interface, HL[10:0] are associated with the data signals while HLSTB and HLSTB# are associated with the strobe signals.

**Figure 50. Hub Interface Routing Example**




## 9.1. Hub Interface Compensation

This section documents the routing guidelines for the 11-bit hub interface using enhanced (parallel) termination. This hub interface connects the ICH4-M to the GMCH. The ICH4-M should strap its HLRCOMP pin to $V_{CC}$=1.5 V, as summarized in Table 53. The 852GME chipset GMCH should strap its HLRCOMP pin to $V_{CC}$=1.5V as summarized in Table 53.

The trace impedance must equal 55 ± 15%

**Table 53. Hub Interface RCOMP Resistor Values**

| Component | Trace Impedance | HLCOMP Resistor Value | HLCOMP Resistor Tied to |
|---|---|---|---|
| ICH4-M | 55 ± 15% | 48.7 ± 1% | Vcc1_5 |
| 852GME/852PM | 55 ± 15% | 37.4 ± 1% | Vcc1_5 |

## 9.2. Hub Interface Data HL[10:0] and Strobe Signals

The hub interface HL[10:0] data signals should be routed on the same layer as hub interface Strobe signals.

### 9.2.1. HL[10:0] and Strobe Signals Internal Layer Routing

Traces should be routed 4 mils wide with 8 mils trace spacing (4 on 8) and 20 mils spacing from other signals. In order to break out of the GMCH and ICH4-M packages, the HL[10:0] signals can be routed 4 on 7. The signal must be separated to 4 on 8 within 300 mils from the package.

The minimum HL[10:0] on board signal trace length is 1.5 inches, while the maximum is 6 inches. The HL[10:0] signals must be matched within ± 100 mils of the HLSTB differential pair. There is no explicit matching requirement between the individual HL[10:0] signals.

The hub interface strobe signals HLSTB and HLSTB# should be routed as a differential pair, 4 mils wide with 8 mils trace spacing (4 on 8). The maximum length for strobe signals is 6 inches. Each strobe signal must be the same length and each HL[10:0] signal must be matched to within ± 100 mils of the strobe signals. All length matching should be done from GMCH die to the ICH4-M die. Refer to the package length Table 54 and Table 55.

**Table 54. Hub Interface Signals Internal Layer Routing Summary**

| Signal | Min length (inch) | Max length (inch) | Width (mils) | Space (mils) | Mismatch length (mils) | Relative To | Space with other signals (mils) | Notes |
|---|---|---|---|---|---|---|---|---|
| HL[10:0] | 1.5” | 6” | 4 | 8 | ± 100 | Differential HLSTB pair | 20 | |
| HLSTB<br>HLSTB# | 1.5” | 6” | 4 | 8 | ± 100 | Data lines | 20 | HLSTB and HLSTB# must be ± 10 mils of each other |

### Table 55. Hub Interface Package Lengths for ICH4-M

| Signal | Pin Number | Package Length (mils) |
|---|---|---|
| HUB_PD0 | L19 | 551 |
| HUB_PD1 | L20 | 562 |
| HUB_PD2 | M19 | 552 |
| HUB_PD3 | M21 | 567 |
| HUB_PD4 | P19 | 599 |
| HUB_PD5 | R19 | 627 |
| HUB_PD6 | T20 | 623 |
| HUB_PD7 | R20 | 593 |
| HUB_PD8 | P23 | 668 |
| HUB_PD9 | L22 | 559 |
| HUB_PD10 | N22 | 682 |
| HUB_PD11 | K21 | 560 |
| HUB_CLK | T21 | 605 |
| HUB_PSTRB | P21 | 541 |
| HUB_PSTRB# | N20 | 565 |

### Table 56. Hub Interface Package Lengths for GMCH

| Signal | Pin Number | Package Length (mils) |
|---|---|---|
| HL[0] | U7 | 281 |
| HL[1] | U4 | 408 |
| HL[2] | U3 | 476 |
| HL[3] | V3 | 484 |
| HL[4] | W2 | 551 |
| HL[5] | W6 | 355 |
| HL[6] | V6 | 328 |
| HL[7] | W7 | 343 |
| HL[8] | T3 | 499 |
| HL[9] | V5 | 399 |
| HL[10] | V4 | 457 |
| GCLKIN | Y3 | 539 |
| HLSTB | W3 | 504 |
| HLSTB# | V2 | 548 |

### 9.2.2. Terminating HL[11]

The HL[11] signal exists on the ICH4-M but not the GMCH and is not used on the platform. HL[11] must be pulled down to ground via a 56- resistor.

## 9.3. Hub VREF/VSWING Generation/Distribution

The hub interface reference voltage (VREF) is used on both the GMCH (HLVREF) and the ICH4-M (HIREF). The hub interface also has a reference voltage (VSWING) for the GMCH (PSWING) and the ICH4-M (HI_VSWING), to control voltage swing and impedance strength of the hub interface buffers. The VREF voltage requirements must be set appropriately for proper operation. See Table 57 for the VREF and VSWING voltage specifications. Sections 9.3.1 to 9.3.4 provide details on the different options for VREF and VSWING voltage divider circuitry requirements.

**Table 57. Hub Interface VREF/VSWING Reference Voltage Specifications**

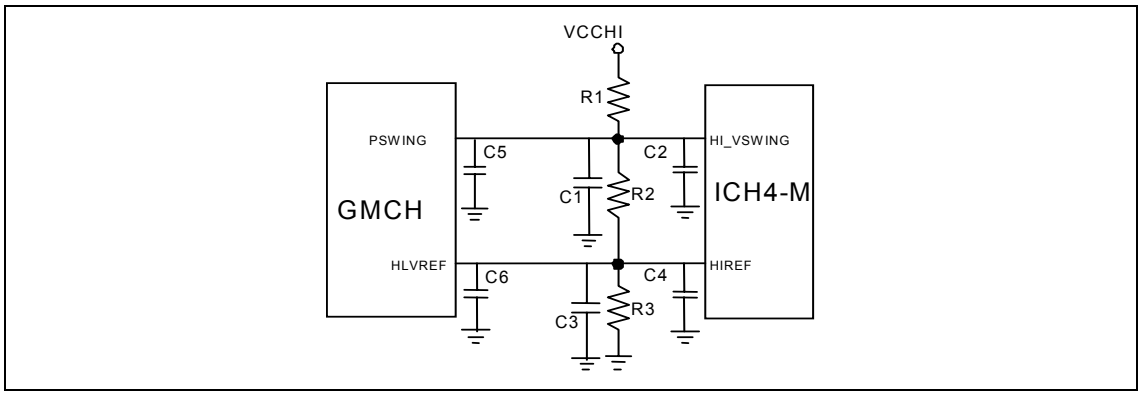
| VREF | VSWING | NOTES |
|---|---|---|
| HIREF (ICH4-M)<br>HLVREF (GMCH) | HI_VSWING (ICH4-M)<br>PSWING (GMCH) | |
| 350 mV +/- 8% | 800 mV +/- 8% | See Sections 9.3.1 to 9.3.4for recommendations for the VREF/VSWING voltage generation circuitry. See Table 60 for recommended resistor values. |

### 9.3.1. Single Generation Voltage Reference Divider Circuit

The GMCH and ICH4-M may share the same single voltage divider circuit. This option provides one voltage divider circuit to generate both VREF and VSWING reference voltage. The reference voltage for both VREF and VSWING must meet the voltage specification in Table 57.

If the voltage specifications are not met, then an individual, locally generated, voltage divider circuit is required. The maximum trace length from the GMCH to ICH4-M is 4 inches or less. The voltage divider circuit should be place midway between the GMCH and ICH4-M. Normal precautions should be taken to minimize crosstalk to other signals (< 10-15 mV). If the trace length exceeds 4 inches, then the locally generated voltage reference divider should be used. See Section 9.3.2 for the more details.

**Figure 51. Single VREF/VSWING Voltage Generation Circuit for Hub Interface**




The resistor values, R1, R2, and R3 must be rated at 1% tolerance. See Table 59 for recommended resistor values. The selected resistor values ensure that the reference voltage tolerance is maintained over the input leakage specification. Two, 0.1-µF capacitors (C1 and C3) should be placed close to the divider. In addition, the 0.01-µF bypass capacitor (C2, C4, C5, and C6) should be placed within 0.25 inches of HLVREF/VREF pin (for C4 and C6) and HI_VSWING pin (for C2 and C5).

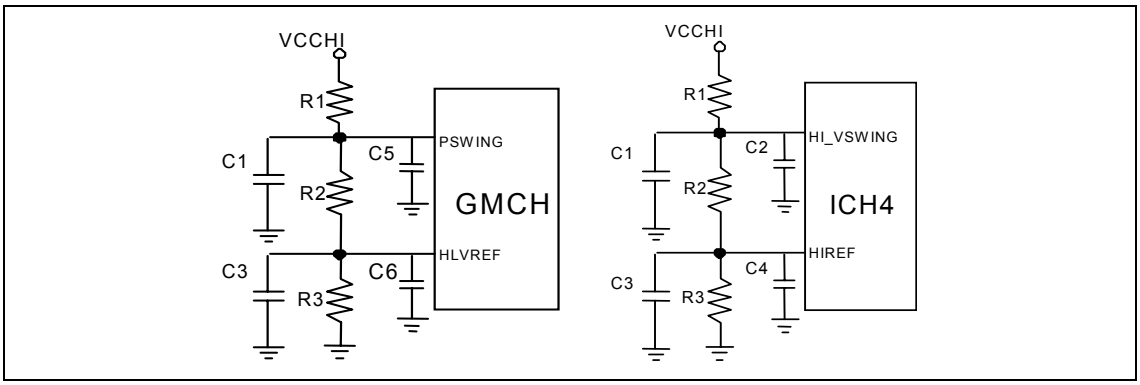
**Table 58. Recommended Resistor Values for Single VREF/VSWING Divider Circuit**

| | Recommended Resistor Values | | | | | | VCCHI |
|---|---|---|---|---|---|---|---|
| Option 1 | R1 = 80.6 | 1% | R2 = 51.1 | 1% | R3 = 40.2 | 1% | 1.5 V |
| Option 2 | R1 = 255 | 1% | R2 = 162 | 1% | R3 = 127 | 1% | 1.5 V |
| Option 3 | R1 = 226 | 1% | R2 = 147 | 1% | R3 = 113 | 1% | 1.5 V |
| | C1 and C3 = 0.1 µF (near divider)<br>C2, C4, C5, C6 = 0.01 µF (near component) | | | | | | |

## 9.3.2. Locally Generated Voltage Reference Divider Circuit

This section describes the option to generate the voltage references separately for GMCH and ICH4-M, to be used if the routing distance between GMCH and ICH4-M is greater than 4 inches. One voltage divider circuit is used to generate both HIVREF and HI_VSWING voltage references for ICH4-M. Another voltage divider circuit is used for GMCH. The reference voltage for both HIVREF and HI_VSWING must meet the voltage specification in Table 59. The resistor values R1, R2, and R3 must be rated at 1% tolerance (see Table 59). Normal care needs to be taken to minimize crosstalk to other signals (< 10-15 mV). If the voltage specifications are not met then individually generated voltage divider circuit for HIVREF and HI_VSWING is required.

**Figure 52. ICH4-M and GMCH Locally Generated Reference Voltage Divider Circuit**




## 9.3.3. Single GMCH and ICH4-M Voltage Generation / Separate Divider Circuit for VSWING/VREF

This section describes the option to use one voltage divider circuit for VREF, shared by both ICH4-M and GMCH, while using another voltage divider circuit for VSWING. This allows for tuning the two reference voltages independently. The reference voltage for both HIVREF and HI_VSWING must meet the voltage specification in Table 59. Normal care needs to be taken to minimize crosstalk to other signals (< 10-15 mV).

**Figure 53. Shared GMCH and ICH4-M Reference Voltage with Separate Voltage Divider Circuit for VSWING and VREF**

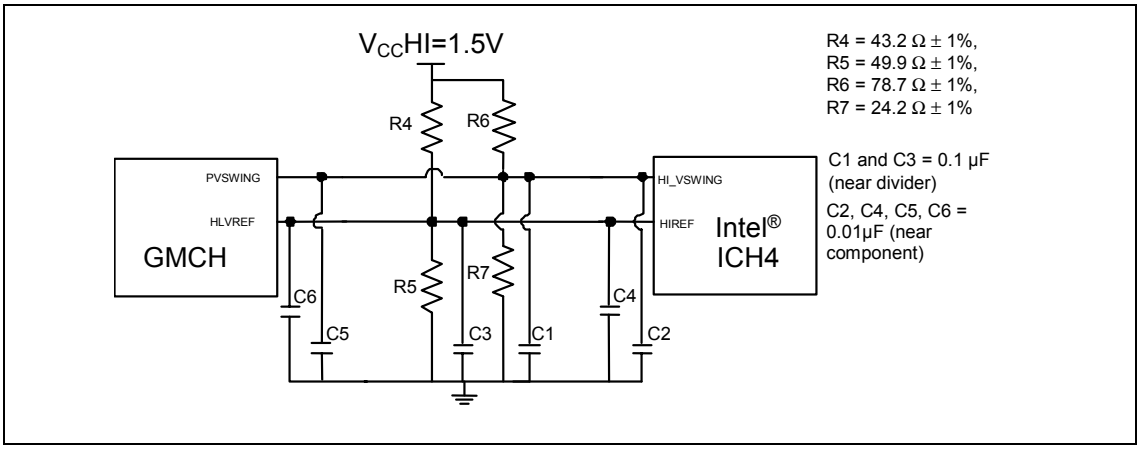



**Table 59. Recommended Resistor Values for Separate HIVREF and HI_VSWING Divider Circuits**

| Signal | Recommended Resistor Values | VCCHI | Capacitor value |
|---|---|---|---|
| HIVREF (350 mV) | R4 = 43.2 1%<br>R5 = 49.9 1%, | VCCHI=1.5 V | C3 = 0.1 µF (near divider)<br>C2, C5 = 0.01 µF (near component) |
| HI_VSWING (800 mV) | R6 = 78.7 1%<br>R7 = 24.2 1%, | VCCHI=1.5 V | C1 = 0.1 µF (near divider)<br>C4, C6 = 0.01 µF (near component) |

## 9.3.4. Separate GMCH and ICH4-M Voltage Generation / Separate Divider Circuits for VREF and VSWING

This option allows for tuning the voltage references HIVREF and HI_VSWING individually, for both ICH4-M and GMCH. The reference voltage for both HIVREF and HI_VSWING must meet the voltage specification in Table 60. Normal care needs to be taken to minimize crosstalk to other signals (< 10-15 mV).

**Figure 54. Individual HIVREF and HI_VSWING Voltage Reference Divider Circuits for ICH4-M and GMCH**

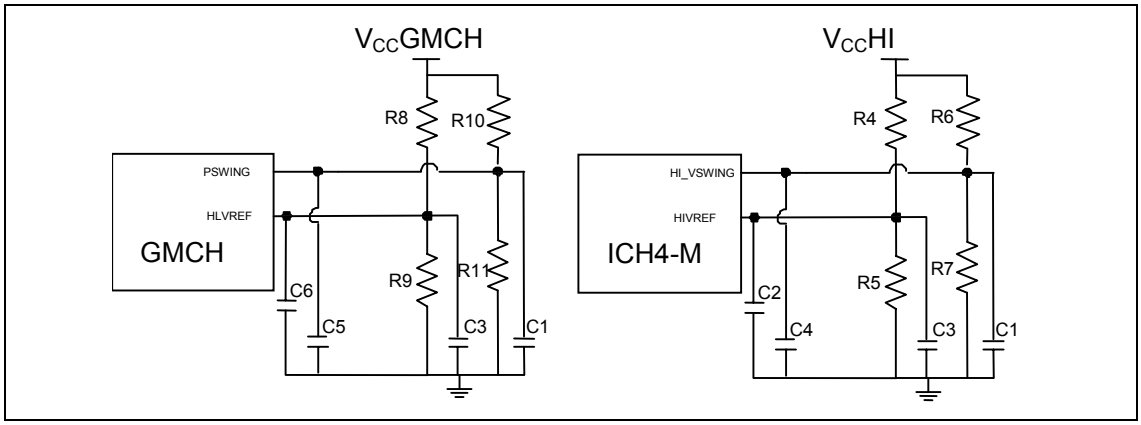



**Table 60. Recommended Resistor Values for HIVREF and HI_VSWING Divider Circuits for ICH4-M**

| Chipset Component | Signal | Recommended Resistor Values | VCCHI | Capacitor value |
|---|---|---|---|---|
| ICH4-M | HIVREF (350mV) | R4 = 487 1%<br>R5 = 150 1%, | VCCHI=1.5 V | C3 = 0.1 µF (near divider)<br>C2 = 0.01 µF (near component) |
| | HI_VSWING (800mV) | R6 = 130 1%<br>R7 = 150 1%, | VCCHI=1.5 V | C1 = 0.1 µF (near divider)<br>C4 = 0.01 µF (near component) |
| 852GME/PM | HLVREF (350mV) | R8 = 243 1%<br>R9 = 100 1% | VCCGMCH=1.5 V | C3 = 0.1 µF (near divider)<br>C6 = 0.01 µF (near component) |
| | PSWING (800mV) | R10 = 49.9 1%<br>R11 = 100 1% | VCCGMCH=1.5 V | C1 = 0.1 µF (near divider)<br>C5 = 0.01 µF (near component) |

# 9.4. Hub Interface Decoupling Guidelines

To improve I/O power delivery, use two 0.1-µF capacitors per each component (i.e. the ICH4-M and GMCH). These capacitors should be placed within 50 mils from each package, adjacent to the rows that contain the hub interface. If the layout allows, wide metal fingers running on the $V_{SS}$ side of the board should connect the $V_{CC}$HI side of the capacitors to the $V_{CC}$HI power pins. Similarly, if layout allows, metal fingers running on the $V_{CC}$HI side of the board should connect the groundside of the capacitors to the $V_{SS}$ power pins.

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# 10. I/O Subsystem

## 10.1. IDE Interface

This section contains guidelines for connecting and routing the Intel 82801DBM ICH4-M IDE interface. The ICH4-M has two independent IDE channels. This section provides guidelines for IDE connector cabling and motherboard design, including component and resistor placement, and signal termination for both IDE channels. The ICH4-M has integrated the series resistors that have been typically required on the IDE data signals (PDD[15:0] and SDD[15:0]) running to the two ATA connectors. While it is not anticipated that additional series termination resistors will be required, OEMs should verify motherboard signal integrity through simulation. Additional external, 0- resistors can be incorporated into the design to address possible noise issues on the motherboard. The additional resistor layout increases flexibility by offering stuffing options at a later date.

The IDE interface can be routed with 5-mil traces on 7-mil spaces, and must be less than 8 inches long (from ICH4-M to IDE connector). Additionally, the maximum length difference between the shortest data signal and the longest strobe signal of a channel is 0.5 inches.

### 10.1.1. Cabling

Length of cable: Each IDE cable must be equal to or less than 18 inches.

Capacitance: Less than 35 pF.

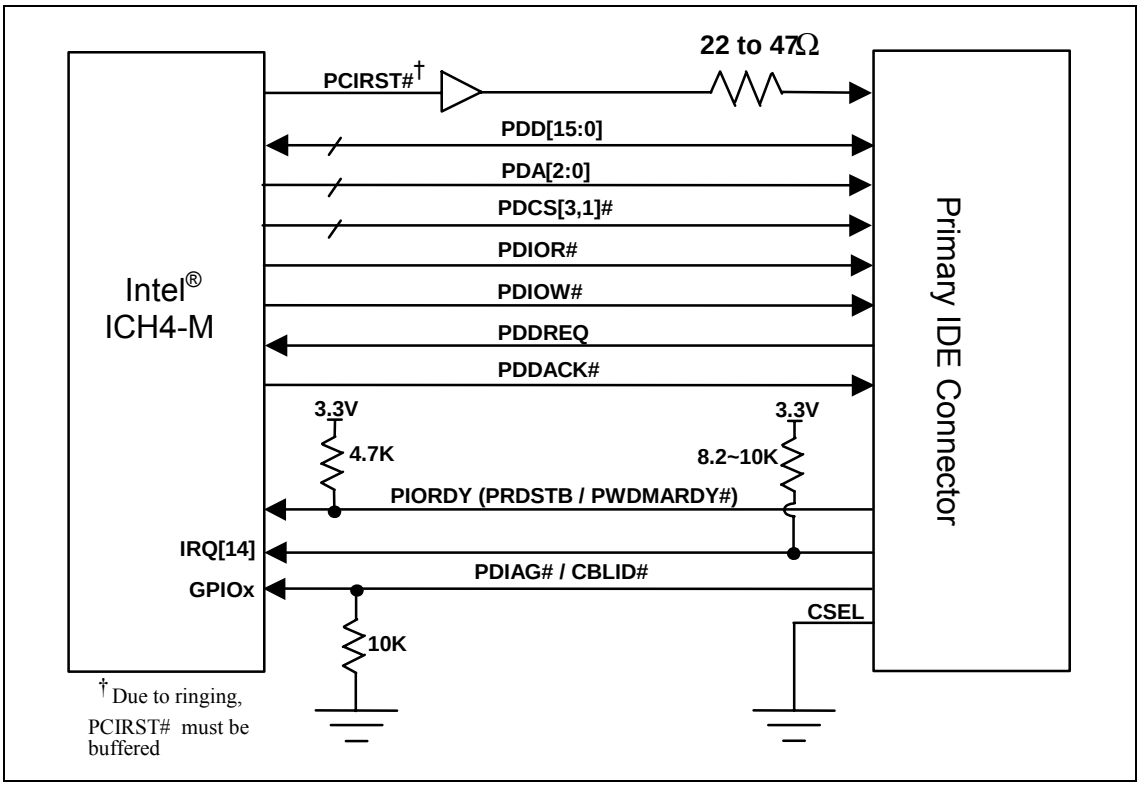
Placement: A maximum of 6 inches between drive connectors on the cable. If a single drive is placed on the cable it should be placed at the end of the cable. If a second drive is placed on the same cable, it should be placed on the next closest connector to the end of the cable (6 inches away from the end of the cable).

Grounding: Provide a direct low impedance chassis path between the motherboard ground and hard disk drives.

ICH4-M Placement: The ICH4-M must be placed equal to or less than 8 inches from the ATA connector(s).

## 10.1.2. Primary IDE Connector Requirements

**Figure 55. Connection Requirements for Primary IDE Connector**




The following are connection requirements for Primary IDE Connector:

22 - 47 series resistors are required on RESET#. The correct value should be determined for each unique motherboard design, based on signal quality.

An 8.2 k - 10 k pull-up resistor is required on IRQ14 to VCC3_3.

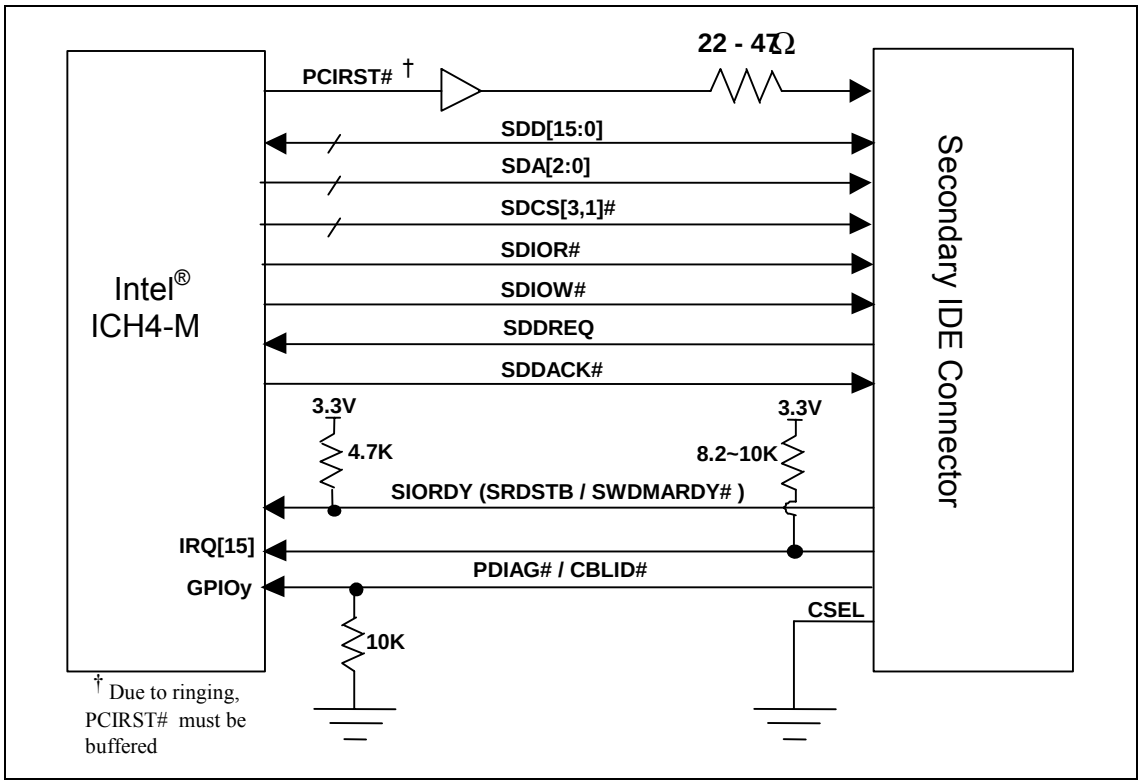
A 4.7-k pull-up resistor to VCC3_3 is required on PIORDY and SIORDY.

Series resistors can be placed on the control and data lines to improve signal quality. The resistors are placed as close to the connector as possible. Values are determined for each unique motherboard design.

The 10-k resistor to ground on the PDIAG#/CBLID# signal is required on the Primary Connector. This change is to prevent the GPI pin from floating if a device is not present on the IDE interface.

## 10.1.3. Secondary IDE Connector Requirements

**Figure 56. Connection Requirements for Secondary IDE Connector**




The following are connection requirements for Secondary IDE Connector:

22 - 47 series resistors are required on RESET#. The correct value should be determined for each unique motherboard design, based on signal quality.

An 8.2 k - 10 k pull-up resistor is required on IRQ15 to VCC3_3.

A 4.7-k pull-up resistor to VCC3_3 is required on PIORDY and SIORDY.

Series resistors can be placed on the control and data lines to improve signal quality. The resistors are placed as close to the connector as possible. Values are determined for each unique motherboard design.

The 10-k resistor to ground on the PDIAG#/CBLID# signal is required on the Secondary Connector. This change is to prevent the GPI pin from floating if a device is not present on the IDE interface.

## 10.1.4. Mobile IDE Swap Bay Support

Systems that require the support for an IDE "hot" swap drive bay can be designed to utilize the ICH4-M's IDE interface disable feature to achieve this functionality. To support a mobile "hot" swap bay, the ICH4-M allows the IDE output signals to be tri-stated or driven low and input buffers to be turned off. This requires certain hardware and software requirements to be met for proper operation.

From a hardware perspective, the equivalent of two spare control signals (e.g. GPIO's) and a FET are needed to properly utilize the IDE tri-state feature. An IDE drive must have a reset signal (i.e. first additional control signal) driving its reset pin and a power supply that is isolated from the rest of the IDE interface. To isolate the power supplied to the IDE drive bay, a second additional control signal is needed to control the enabling/disabling of a FET that supplies a separate plane flood powering the IDE drive and its interface.

**Although actual hardware implementations may vary, the isolated reset signal and power plane are strict requirements. S**ystems that connect the IDE swap bay drive to the same power plane and reset signals of the ICH4-M should not use this IDE tri-state feature. Many IDE drives use the control and address lines as straps that are used to enter test modes. If the IDE drive is powered up along with the ICH4-M while the IDE interface is tri-stated rather than being driven to the default state, then the IDE drive could potentially enter a test mode. To avoid such a situation, the aforementioned hardware requirements or equivalent solution should be implemented.

### 10.1.4.1. ICH4-M IDE Interface Tri-State Feature

The new IDE interface tri-state capabilities of the ICH4-M also include a number of configuration bits that must be programmed accordingly for proper system performance. The names of the critical registers, their location, and brief description are listed below.

1. B0:D31:F0 Offset D5h (BACK_CNTL – Backed Up Control register) bits [7:6] need to be set to 1 in order to enable the tri-stating of the primary and secondary IDE pins when the interfaces are put into reset. By default both bits are set to 1.
2. B0:D31:F0 Offset D0-D3h (GEN_CNTL – General Control register) bit [3] should be set to 1 in order to lock the state of bits [7:6] at B0:D31:F0 Offset D5h. This prevents any inadvertent reprogramming of the IDE interface pins to a non-tri-state mode during reset by a rogue software program. By default this bit is set to 0 and BIOS should set this bit to 1. This is a write once bit only and requires a PCIRST# to reset to 0. Thus, this bit also needs to be set to 1 after resume from S3-S5.
3. B0:D31:F1 Offset 54h (IDE_CONFIG – IDE I/O Configuration register) bits [19:18] (SEC_SIG_MODE) and bits [17:16] (PRIM_SIG_MODE) control the reset states of the secondary and primary IDE channels, respectively. The values in SEC_SIG_MODE and PRIM_SIG_MODE are tied to the values set by the BACK_CNTRL register bits [7:6], respectively. When bits [7:6] are set to 1, the PRIM_SIG_MODE and SEC_SIG_MODE will be set to 01 for tri-state when the either IDE channel is put in reset.
4. B0:D31:F1 Offset 40-41h (Primary) and 42-23h (Secondary) bit [5] and bit [1] (IDE_TIM – IDE Timing register) are the IORDY Sample Point Enable bits for drive 1 and 0 of the primary and secondary IDE channels, respectively. By default, these bits are set to 0 and during normal power up, should be set to 1 by the BIOS to enable IORDY assertion from the IDE device when an access is requested.

### 10.1.4.2. S5/G3 to S0 Boot Up Procedures for IDE Swap Bay

The procedures listed below summarize the steps that must be followed during power up of an IDE swap bay drive:

1. ICH4-M powers up, IDE interface is tri-stated, disk drive is not powered up. IDE drive is recognized as being on a separate power plane and its reset is different from the ICH4-M.
2. BIOS powers on the IDE drive. e.g. GPIO is used to switch on a FET on the board.
3. Once the IDE drive and interface is powered up, the ICH4-M exits from tri-state mode and begins to actively drive the interface.
4. Once ready, the BIOS can de-assert the reset signal to the IDE drive, e.g. GPIO routed to the IDE drive's reset pin.

### 10.1.4.3. Power Down Procedures for Mobile Swap Bay

The procedures listed below summarize the steps that must be followed in order to remove an IDE device from the mobile swap bay:

1. User indicates to the system that removal of IDE device from the mobile swap bay should begin. Once the system recognizes that all outstanding IDE accesses have completed, the reset signal to the swap device should be asserted.
2. The IDE channel (primary or secondary) that the device resides on should then be set to drive low mode rather than the default tri-state mode. This requires setting the IDE_CONFIG register (B0:D31:F0 Offset 54h) bits [19:18] or [17:16] to 10 (10b). This will cause all IDE outputs to the IDE drive to drive low rather than the default tri-state (which is useful during boot up to prevent any IDE drives from entering a test mode).
3. The IORDY Sample Point Enable bit of the IDE_TIM register for the appropriate IDE device should then be set to 0 to disable IORDY sampling by the ICH4-M. This ensures that zeros will always be returned if the OS attempts to access the IDE device being swapped.
4. Power to the isolated power plane of the IDE device can then be removed and the system can indicate to the user that the mobile swap bay can be removed and the IDE device replaced.

### 10.1.4.4. Power Up Procedures After Device "Hot" Swap Completed

The procedures listed below summarize the steps that must be followed after a new IDE device has been added to the mobile swap bay and the swap bay must be powered back up:

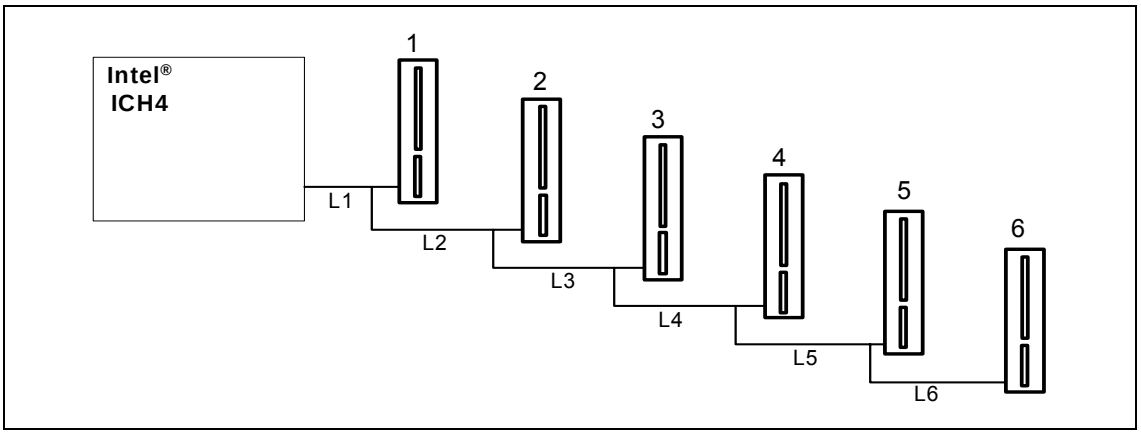
1. Once the IDE swap bay is replaced into the system, the power plane to the device should be enabled once again.
2. The IORDY Sample Point Enable bit of the IDE_TIM register for the appropriate IDE device should then be set to 1 to enable IORDY sampling by the ICH4-M. This allows the OS to access the IDE device once again and waits for the assertion of IORDY in response to an access request.
3. Once the system IDE interface is configured for normal operation once again, the reset signal to the swap device should be de-asserted to allow the drive to initialize.

## 10.2. PCI

The Intel 82801DBM ICH4-M provides a PCI Bus interface that is compliant with the *PCI Local Bus Specification Revision 2.2*. The implementation is optimized for high performance data streaming when the ICH4-M is acting as either the target or the initiator in the PCI bus.

The ICH4-M supports six PCI Bus masters (excluding the ICH4-M), by providing six REQ#/GNT# pairs. In addition, the ICH4-M supports two PC/PCI REQ#/GNT# pairs, one of which is multiplexed with a PCI REQ#/GNT# pair.

**Figure 57. PCI Bus Layout Example**



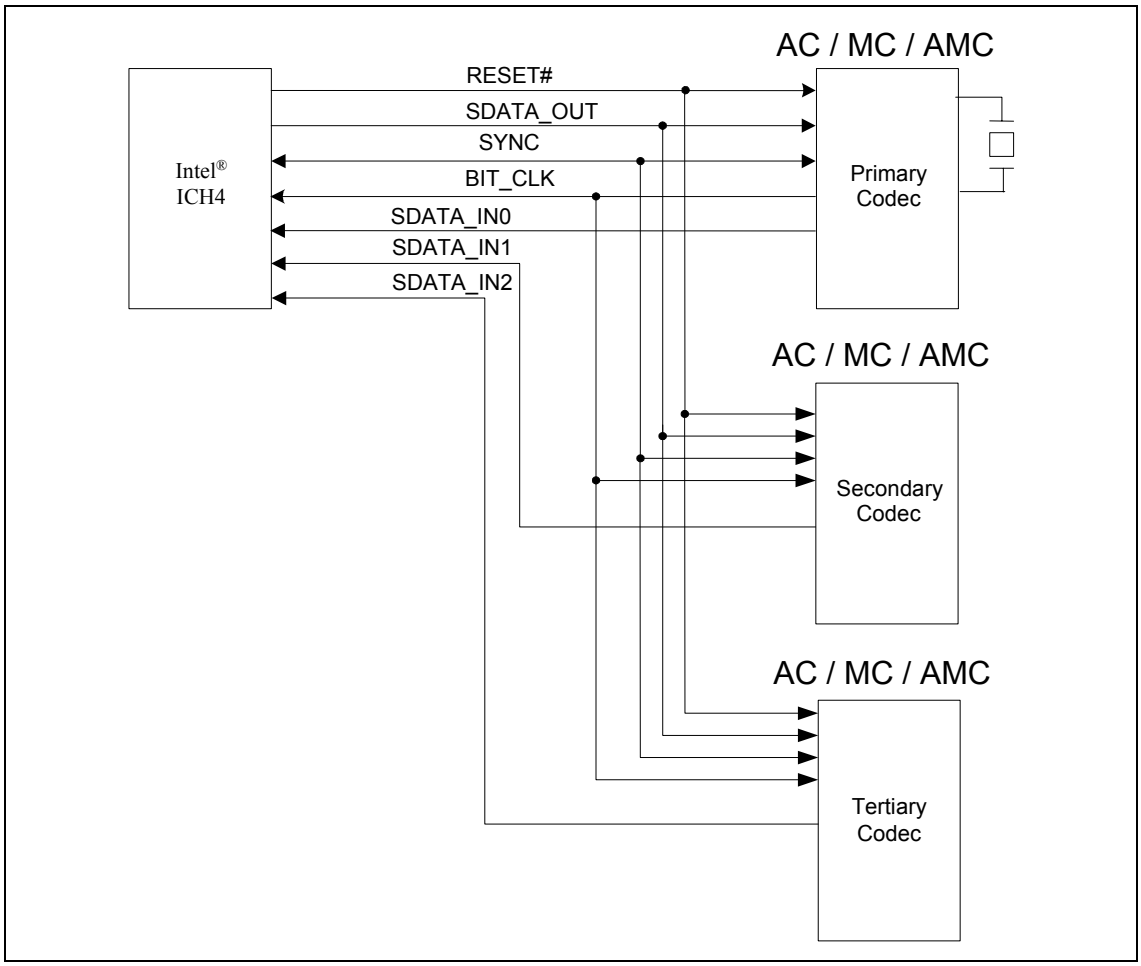

## 10.3. AC'97

The Intel 82801DBM ICH4-M implements an AC'97 2.1, 2.2, and 2.3 compliant digital controller. Please contact your codec IHV (Independent Hardware Vendor) for information on 2.2 compliant products. The AC'97 2.2 specification is on the Intel website:

http://developer.intel.com/ial/scalableplatforms/audio/index.htm - 97spec/

The AC-link is a bi-directional, serial PCM digital stream. It handles multiple input and output data streams, as well as control register accesses, employing a time division multiplexed (TDM) scheme. The AC-link architecture provides for data transfer through individual frames transmitted in a serial fashion. Each frame is divided into 12 outgoing and 12 incoming data streams, or slots. The architecture of the ICH4-M AC-link allows a maximum of three codecs to be connected. Figure 58 shows a three-codec topology of the AC-link for the ICH4-M.

**Figure 58. Intel 82801DBM ICH4-M AC'97 – Codec Connection**




**NOTE:** If a modem codec is configured as the primary AC-link Codec, there should not be any Audio Codecs residing on the AC-link. The primary codec may be connected to AC_SDIN0 as documented in the Intel ICH4-M Datasheet.

Clocking is provided from the primary codec on the link via AC_BIT_CLK, and is derived from a 24.576-MHz crystal or oscillator. Refer to the primary codec vendor for crystal or oscillator requirements. AC_BIT_CLK is a 12.288-MHz clock driven by the primary codec to the digital controller (ICH4-M) and to any other codec present. That clock is used as the time base for latching and driving data. **Clocking AC_BIT_CLK directly off the CK-408 clock chip's 14.31818-MHz output is not supported.**

The ICH4-M supports wake-on-ring from S1M-S5 via the AC'97 link. The codec asserts AC_SDIN to wake the system. To provide wake capability and/or caller ID, standby power must be provided to the modem codec.

The ICH4-M has weak pull-down/pull-ups that are always enabled. This will keep the link from floating when the AC-link is off or there are no codecs present.

If the Shut-off bit is not set, it implies that there is a codec on the link. Therefore, AC_BIT_CLK and AC_SDOUT will be driven by the codec and the ICH4-M respectively. However, AC_SDIN0,

AC_SDIN1, and AC_SDIN2 may not be driven. If the link is enabled, the assumption can be made that there is at least one codec.

**Figure 59. Intel 82801DBM ICH4-M AC'97 – AC_BIT_CLK Topology**

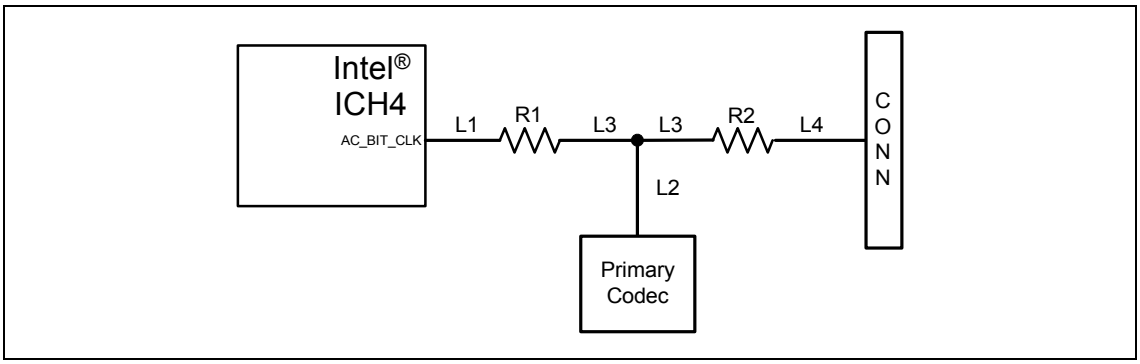


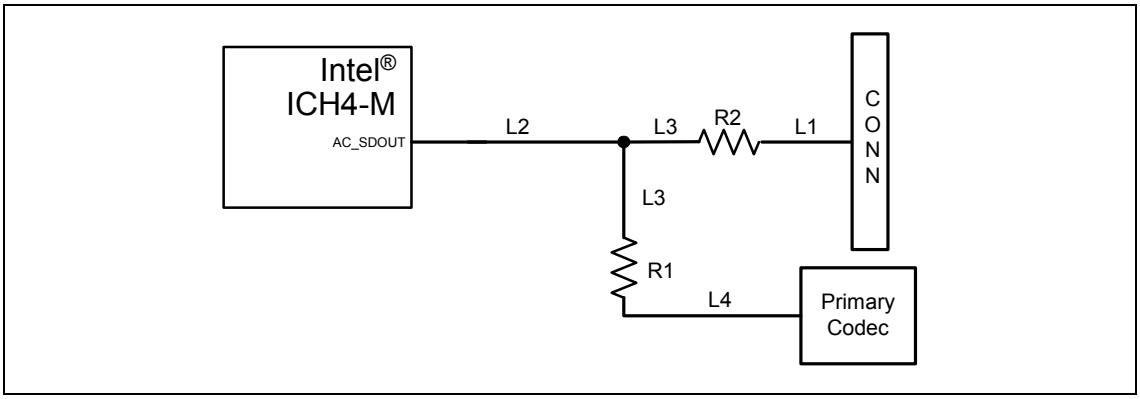

**Table 61. AC'97 AC_BIT_CLK Routing Summary**

| AC'97 Routing Requirements | Maximum Trace Length (inches) | Series Termination Resistance | AC_BIT_CLK Signal Length Matching |
|---|---|---|---|
| 5 on 5 | L1 = (1 to 8) – L3<br>L2 = 0.1 to 6<br>L3 = 0.1 to 0.4<br>L4 = (1 to 6) – L3 | R1 = 33 - 47<br>R2 = Option 0 resistor for debugging purposes | N/A |

**NOTES:**

1. Simulations were performed using Analog Device's* Codec (AD1885) and the Cirrus Logic's* Codec (CS4205b). Results showed that if the AD1885 codec was used a 33- resistor was best for R1 and if the CS4205b codec was used a 47- resistor for R1 was best.
2. Bench data shows that a 47- resistor for R1 is best for the Sigmatel* 9750 codec.

**Figure 60. Intel 82801DBM AC'97 – AC_SDOUT/AC_SYNC Topology**

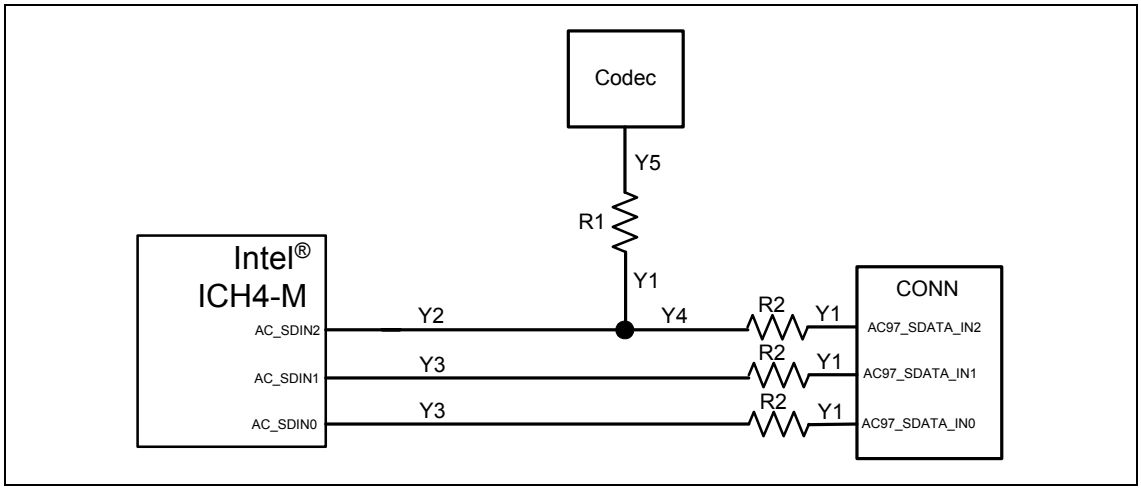


### Table 62. AC'97 AC_SDOUT/AC_SYNC Routing Summary

| AC'97 Routing Requirements | Maximum Trace Length (inches) | Series Termination Resistance | AC_SDOUT/AC_SYNC Signal Length Matching |
|---|---|---|---|
| 5 on 5 | L1 = (1 to 6) – L3<br>L2 = 1 to 8<br>L3 = 0.1 to 0.4<br>L4 = (0.1 to 6) – L3 | R1 = 33 - 47<br>R2 = R1 if the connector card that will be used with the platform does not have a series termination on the card. Otherwise R2 = 0 | N/A |

**NOTES:**
1. Simulations were performed using Analog Device's* Codec (AD1885) and the Cirrus Logic's* Codec (CS4205b). Results showed that if the AD1885 codec was used a 33- resistor was best for R1 and if the CS4205b codec was used a 47- resistor for R1 was best.
2. Bench data shows that a 47- resistor for R1 is best for the Sigmatel* 9750 codec.

### Figure 61. Intel 82801DBM AC'97 – AC_SDIN Topology




### Table 63. AC'97 AC_SDIN Routing Summary

| AC'97 Routing Requirements | Maximum Trace Length (inches) | Series Termination Resistance | AC_SDIN Signal Length Matching |
|---|---|---|---|
| 5 on 5 | Y1 = 0.1 to 0.4<br>Y2 = (1 to 8) – Y1<br>Y3 = (1 to 14) – Y1<br>Y4 = (1 to 6) – Y1<br>Y5 = (0.1 to 6) – Y1 | R1 = 33 - 47<br>R2 = R1 if the connector card that will be used with the platform does not have a series termination on the card. Otherwise R2 = 0 | N/A |

**NOTES:**
1. Simulations were performed using Analog Device's Codec (AD1885) and the Cirrus Logic's Codec (CS4205b). Results showed that if the AD1885 codec was used a 33- resistor was best for R1 and if the CS4205b codec was used a 47- resistor for R1 was best.

2. Bench data shows that a 47- resistor for R1 is best for the Sigmatel 9750 codec.

## 10.3.1. AC'97 Routing

To ensure the maximum performance of the codec, proper component placement and routing techniques are required. These techniques include properly isolating the codec, associated audio circuitry, analog power supplies, and analog ground plane, from the rest of the motherboard. This includes plane splits and proper routing of signals not associated with the audio section. Contact your vendor for device-specific recommendations.

The basic recommendations are as follows:

Special consideration must be given for the ground return paths for the analog signals.

Digital signals routed in the vicinity of the analog audio signals must not cross the power plane split lines. Analog and digital signals should be located as far as possible from each other.

Partition the board with all analog components grouped together in one area and all digital components in another.

Separate analog and digital ground planes should be provided, with the digital components over the digital ground plane, and the analog components, including the analog power regulators, over the analog ground plane. The split between planes must be a minimum of 0.05 inches wide.

Keep digital signal traces, especially the clock, as far as possible from the analog input and voltage reference pins.

Do not completely isolate the analog/audio ground plane from the rest of the board ground plane. There should be a single point (0.25 inches to 0.5 inches wide) where the analog/isolated ground plane connects to the main ground plane. The split between planes must be a minimum of 0.05 inches wide.

Any signals entering or leaving the analog area must cross the ground split in the area where the analog ground is attached to the main motherboard ground. That is, no signal should cross the split/gap between the ground planes, which would cause a ground loop, thereby greatly increasing EMI emissions and degrading the analog and digital signal quality.

Analog power and signal traces should be routed over the analog ground plane.

Digital power and signal traces should be routed over the digital ground plane.

Bypassing and decoupling capacitors should be close to the IC pins, or positioned for the shortest connections to pins, with wide traces to reduce impedance.

All resistors in the signal path or on the voltage reference should be metal film. Carbon resistors can be used for DC voltages and the power supply path, where the voltage coefficient, temperature coefficient, and noise are not factors.

Regions between analog signal traces should be filled with copper, which should be electrically attached to the analog ground plane. Regions between digital signal traces should be filled with copper, which should be electrically attached to the digital ground plane.

Locate the crystal or oscillator close to the codec.

## 10.3.2. Motherboard Implementation

The following design considerations are provided for the implementation of an ICH4-M platform using AC'97. These design guidelines have been developed to ensure maximum flexibility for board designers, while reducing the risk of board-related issues. These recommendations are not the only implementation or a complete checklist, but they are based on the ICH4-M platform.

Active components such as FET switches, buffers or logic states should not be implemented on the AC-link signals, except for AC_RST#. Doing so would potentially interfere with timing margins and signal integrity.

The ICH4-M supports wake-on-ring from S1M-S5 states via the AC'97 link. The codec asserts AC_SDIN to wake the system. To provide wake capability and/or caller ID, standby power must be provided to the modem codec. If no codec is attached to the link, internal pull-downs will prevent the inputs from floating, so external resistors are not required.

PC_BEEP should be routed through the audio codec. Care should be taken to avoid the introduction of a pop when powering the mixer up or down.

#### 10.3.2.1. Valid Codec Configurations

**Table 64. Supported Codec Configurations**

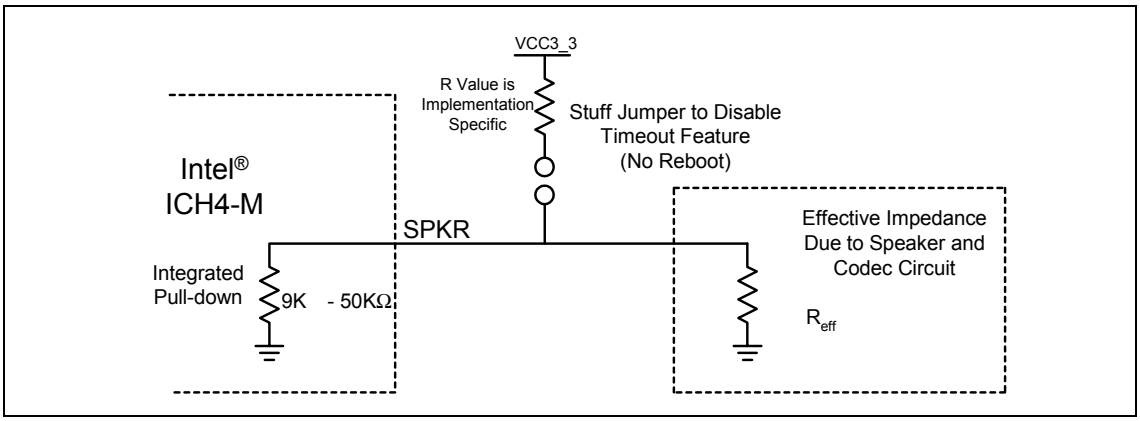
| Option | Primary Codec | Secondary Codec | Tertiary Codec | Notes |
|---|---|---|---|---|
| 1 | Audio | Audio | Audio | 1 |
| 2 | Audio | Audio | Modem | 1 |
| 3 | Audio | Audio | Audio/Modem | 1 |
| 4 | Audio | Modem | Audio | 1 |
| 5 | Audio | Audio/Modem | Audio | 1 |
| 6 | Audio/Modem | Audio | Audio | 1 |

**NOTES:**
1. For power management reasons, codec power management registers are in audio space. As a result, if there is an audio codec in the system it must be Primary.
2. There cannot be two modems in a system since there is only one set of modem DMA channels.
3. The ICH4-M supports a codec on any of the AC_SDIN lines, however the modem codec ID must be either 00 or 01.

### 10.3.3. SPKR Pin Configuration

SPKR is used as both the output signal to the system speaker and as a functional strap. The strap function enables or disables the "TCO Timer Reboot function" based on the state of the SPKR pin on the rising edge of PWROK. When enabled, the ICH4-M sends an SMI# to the processor upon a TCO timer timeout. The status of this strap is readable via the NO_REBOOT bit (bit 1, D31: F0, Offset D4h). The SPKR signal has a weak integrated pull-down resistor (the resistor is only enabled during boot/reset). Therefore, its default state is a logical zero or set to reboot. To disable the feature, a jumper can be populated to pull the signal line high (see Figure 62). The value of the pull-up must be such that the voltage divider output caused by the pull-up, the effective pull-down ($R_{eff}$), and the ICH4-M's integrated pull-down resistor will be read as logic high (0.5 * VCC3_3 to VCC3_3 + 0.5 V).

Figure 62. Example Speaker Circuit




# 10.4. USB 2.0 Guidelines and Recommendations

## 10.4.1. Layout Guidelines

### 10.4.1.1. General Routing and Placement

Use the following general routing and placement guidelines when laying out a new design. These guidelines will help to minimize signal quality and EMI problems. The USB 2.0 validation efforts focused on a four-layer motherboard where the first layer is a signal layer, the second plane is power, the third plane is ground and the fourth is a signal layer. This results in the placement of most of the routing on the fourth plane (closest to the ground plane), allowing a higher component density on the first plane.

1. Place the ICH4-M and major components on the un-routed board first. With minimum trace lengths, route high-speed clock, periodic signals, and USB 2.0 differential pairs first. Maintain maximum possible distance between high-speed clocks/periodic signals to USB 2.0 differential pairs and any connector leaving the PCB (i.e. I/O connectors, control and signal headers, or power connectors).
2. USB 2.0 signals should be ***ground referenced*** (on recommended stack-up this would be the bottom signal layer).
3. Route USB 2.0 signals using a minimum of vias and corners. This reduces reflections and impedance changes.
4. When it becomes necessary to turn 90°, use two 45° turns or an arc instead of making a single 90° turn. This reduces reflections on the signal by minimizing impedance discontinuities. (As shown in Figure 62).
5. Do not route USB 2.0 traces under crystals, oscillators, clock synthesizers, magnetic devices or ICs that use and/or duplicate clocks.
6. Stubs on high-speed USB signals should be avoided, as stubs will cause signal reflections and affect signal quality. If a stub is unavoidable in the design, the sum of all stubs for a particular signal line should not exceed 200 mils.
7. Route all traces over continuous planes (VCC or GND), with no interruptions. Avoid crossing over anti-etch if at all possible. Crossing over anti-etch (plane splits) increases inductance and radiation levels by forcing a greater loop area. Likewise, avoid changing layers with USB 2.0

traces as much as practical. It is preferable to change layers to avoid crossing a plane split. Refer to 10.4.2.

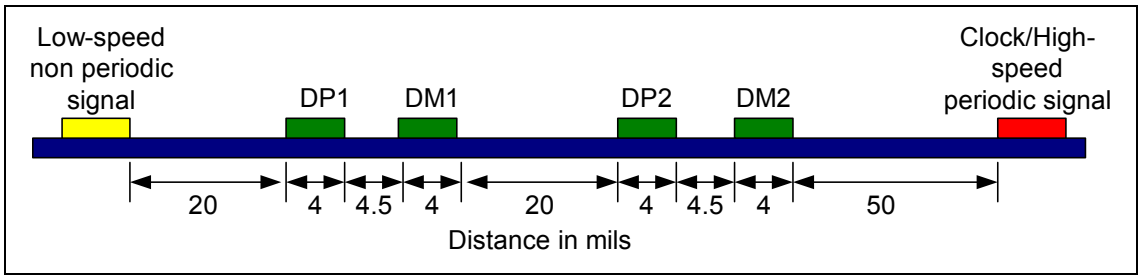
8. Separate signal traces into similar categories and route similar signal traces together (such as routing differential pairs together).
9. Keep USB 2.0 USB signals clear of the core logic set. High current transients are produced during internal state transitions and can be very difficult to filter out.
10. Follow the 20*h thumb rule by keeping traces at least 20*(height above the plane) away from the edge of the plane (VCC or GND, depending on the plane the trace is over). For the suggested stack-up the height above the plane is 4.5 mils. This calculates to a 90-mil spacing requirement from the edge of the plane. This helps prevent the coupling of the signal onto adjacent wires and also helps prevent free radiation of the signal from the edge of the PCB.

### 10.4.1.2. USB 2.0 Trace Separation

The separation guidelines are as follows:

1. Maintain parallelism between USB differential signals with the trace spacing needed to achieve 90- differential impedance. Deviations will normally occur due to package breakout and routing to connector pins. Just ensure the amount and length of the deviations is kept to the minimum possible.
2. Use an impedance calculator to determine the trace width and spacing required for the specific board stack-up being used. 4-mil traces with 4.5-mil spacing results in approximately 90- differential trace impedance.
3. Minimize the length of high-speed clock and periodic signal traces that run parallel to high speed USB signal lines, to minimize crosstalk. Based on EMI testing experience, the minimum suggested spacing to clock signals is 50 mils.
4. Based on simulation data, use 20-mil minimum spacing between high-speed USB signal pairs and other signal traces for optimal signal quality. This helps to prevent crosstalk.

**Figure 63. Recommended USB Trace Spacing**




### 10.4.1.3. USBRBIAS Connection

The USBRBIAS pin and the USBRBIAS# pin can be shorted and routed 5 on 5 to one end of a 22.6 ±1% resistor to ground. Place the resistor within 500 mils of the ICH4-M and avoid routing next to clock pins.

**Figure 64. USBRBIAS Connection**

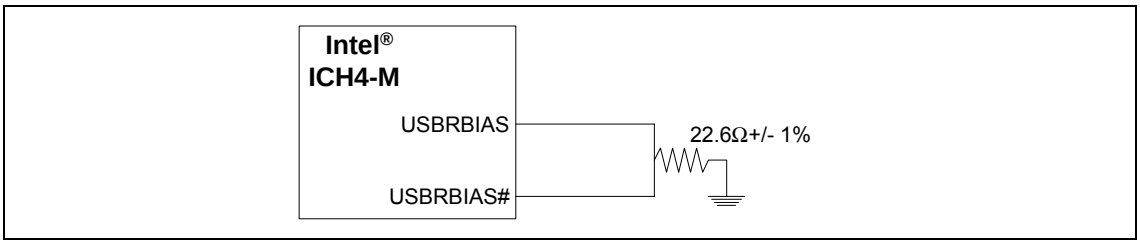



**Table 65. USBRBIAS/USBRBIAS# Routing Summary**

| USBRBIAS/ USBRBIAS# Routing Requirements | Maximum Trace Length | Signal Length Matching | Signal Referencing |
|---|---|---|---|
| 5 on 5 | 500 mils | N/A | N/A |

### 10.4.1.4. USB 2.0 Termination

A common-mode choke should be used to terminate the USB 2.0 bus. Place the common-mode choke as close as possible to the connector pins. See Section 10.4.4 for details.

### 10.4.1.5. USB 2.0 Trace Length Pair Matching

USB 2.0 signal pair traces should be trace length matched. Max trace length mismatch between USB 2.0 signal pair should be no greater that 150 mils.

### 10.4.1.6. USB 2.0 Trace Length Guidelines

**Table 66. USB 2.0 Trace Length Guidelines (With Common-mode Choke)**

| Configuration | Signal Referencing | Signal Matching | Motherboard Trace Length | Card Trace Length | Maximum Total Length |
|---|---|---|---|---|---|
| Back Panel | Ground | The max mismatch between data pairs should not be greater than 150 mils | 17 inches | N/A | 17 inches |

**NOTES:**
1. These lengths are based upon simulation results and may be updated in the future.
2. All lengths are based upon using a common-mode choke (see Section 10.4.4.1 for details on common-mode choke).

## 10.4.2. Plane Splits, Voids, and Cut-Outs (Anti-Etch)

The following guidelines apply to the use of plane splits voids and cutouts.

### 10.4.2.1. VCC Plane Splits, Voids, and Cut-Outs (Anti-Etch)

Use the following guidelines for the $V_{CC}$ plane.

1. Traces should not cross anti-etch, for it greatly increases the return path for those signal traces. This applies to USB 2.0 signals, high-speed clocks, and signal traces as well as slower signal traces that might be coupling to them. USB signaling is not purely differential in all speeds (i.e. the full-speed single ended zero is common mode).
2. Avoid routing of USB 2.0 signals 25 mils of any anti-etch to avoid coupling to the next split or radiating from the edge of the PCB.

When breaking signals out from packages it is sometimes very difficult to avoid crossing plane splits or changing signal layers, particularly in today's motherboard environment that uses several different voltage planes. Changing signal layers is preferable to crossing plane splits if a choice has to be made between one or the other.

If crossing a plane split is completely unavoidable, proper placement of stitching caps can minimize the adverse effects on EMI and signal quality performance caused by crossing the split. Stitching capacitors are small-valued capacitors (1 F or lower in value) that bridge voltage plane splits close to where high speed signals or clocks cross the plane split. The capacitor ends should tie to each plane separated by the split. They are also used to bridge, or bypass, power and ground planes close to where a high-speed signal changes layers. As an example of bridging plane splits, a plane split that separates $V_{CC}5$ and $V_{CC}3_3$ planes should have a stitching cap placed near any high-speed signal crossing. One side of the cap should tie to $V_{CC}5$ and the other side should tie to $V_{CC}3_3$. Stitching caps provide a high frequency current return path across plane splits. They minimize the impedance discontinuity and current loop area that crossing a plane split creates.

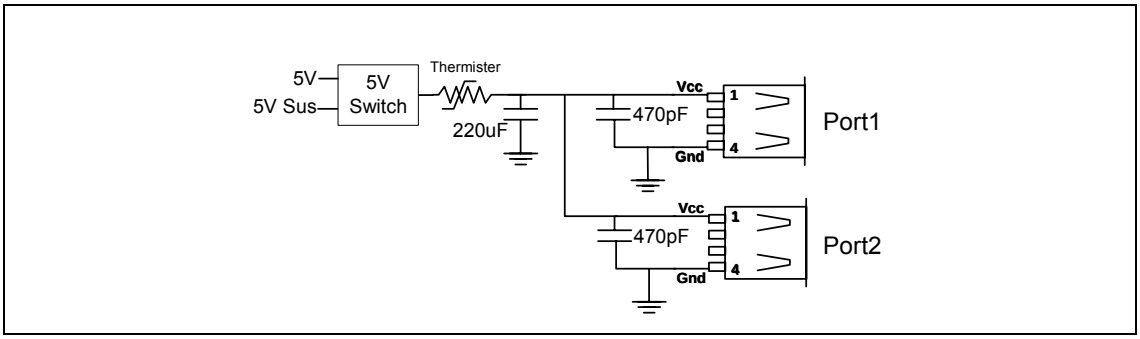
### 10.4.2.2. GND Plane Splits, Voids, and Cut-Outs (Anti-Etch)

Avoid anti-etch on the GND plane.

## 10.4.3. USB Power Line Layout Topology

The following is a suggested topology for power distribution of Vbus to USB ports. Circuits of this type provide two types of protection during dynamic attach and detach situations on the bus: inrush current limiting (droop) and dynamic detach fly-back protection. These two different situations require both bulk capacitance (droop) and filtering capacitance (for dynamic detach fly-back voltage filtering). It is important to minimize the inductance and resistance between the coupling capacitors and the USB ports. That is, capacitors should be placed as close as possible to the port and the power carrying traces should be as wide as possible, preferably, a plane. A good rule is to make the power carrying traces wide enough that the system fuse will blow on an over current event. If the system fuse is rated at 1 amp, then the power carrying traces should be wide enough to carry at least 1.5 amps.

Figure 65. Good Downstream Power Connection



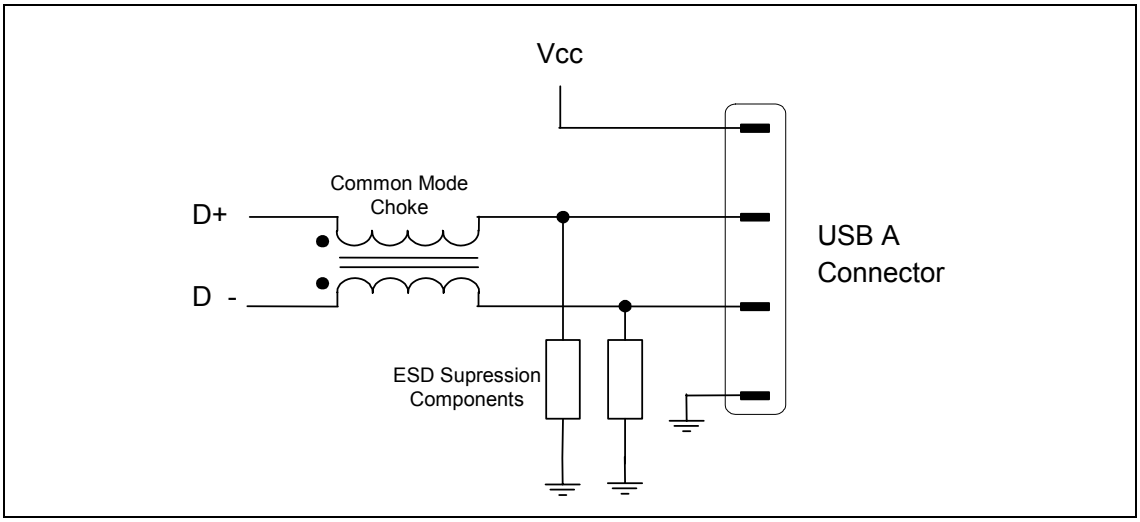

## 10.4.4. EMI Considerations

The following guidelines apply to the selection and placement of common-mode chokes and ESD protection devices.

### 10.4.4.1. Common Mode Chokes

Testing has shown that common-mode chokes can provide required noise attenuation. A design should include a common-mode choke footprint to provide a stuffing option **in the event** the choke is needed to pass EMI testing. Figure 66 shows the schematic of a typical common-mode choke and ESD suppression components. The choke should be placed as close as possible to the USB connector signal pins.

Figure 66. Common Mode Choke Schematic




Common mode chokes distort full-speed and high-speed signal quality. As the common mode impedance increases, the distortion will increase, so you should test the effects of the common mode choke on full speed and high-speed signal quality. Common mode chokes with a target impedance of 80 to 90 at 100 MHz generally provide adequate noise attenuation.

Finding a common mode choke that meets the designer's needs is a two-step process:

1. A part must be chosen with the impedance value that provides the required noise attenuation. This is a function of the electrical and mechanical characteristics of the part chosen and the frequency and strength of the noise present on the USB traces that you are trying to suppress.
2. Once you have a part that gives passing EMI results the second step is to test the effect this part has on signal quality. Higher impedance common-mode chokes generally have a greater damaging effect on signal quality, so care must be used when increasing the impedance without doing thorough testing. Thorough testing means that the signal quality must be checked for low-speed, full-speed and high-speed USB operation.

### 10.4.5. ESD

Classic USB (1.0/1.1) provided ESD suppression using in line ferrites and capacitors that formed a low pass filter. This technique doesn't work for USB 2.0 due to the much higher signal rate of high-speed data. A device that has been tested successfully is based on spark gap technology. Proper placement of any ESD protection device is on the data lines between the common-mode choke and the USB connector data pins as shown in Figure 66. Other types of low-capacitance ESD protection devices may work as well but were not investigated. As with the common mode choke solution, it is recommended to include footprints for some type of ESD protection device as a stuffing option in case it is needed to pass ESD testing.

### 10.4.6. USB Selective Suspend

The USB Specification states maximum current consumption on the "USB bus" is 500 mA for normal operation, 2.5 mA for suspend power when remote wakeup is to be supported and 500 µA otherwise. However, some Bluetooth* devices may require more current in suspend state than specified in the USB specification. Therefore, the system designers should ensure that, on their particular system implementation, there is enough current supplied to the Bluetooth device during suspend state in order for selective suspend to function properly.

## 10.5. I/O APIC (I/O Advanced Programmable Interrupt Controller)

The Intel ICH4-M is designed to be backwards compatible with a number of the legacy interrupt handling mechanisms as well as to be compliant with the latest I/O (x) APIC architecture. In addition to implementing two, 8259 interrupt controllers (PIC), the ICH4-M also incorporates an Advanced Programmable Interrupt Controller (APIC) that is implemented via the 3-wire serial APIC bus that connects all I/O and local APICs. Advancement in the interrupt delivery and control architecture of the ICH4-M is represented by support for the I/O (x) APIC specification where PCI devices deliver interrupts as write cycles that are written directly to a register representing the desired interrupt. These are ultimately delivered via the serial APIC bus or FSB. Furthermore, on 852GME/852GMV/852PMbased systems, the ICH4-M has the option to let the integrated I/O APIC behave as an I/O (x) APIC. This allows the ICH4-M to deliver interrupts in a parallel manner rather than just a serial one and is accomplished by I/O APIC writing to a region of memory that is snooped by the processor and thereby processor knows what interrupt goes active.

On 852GME/852GMV/852PMbased platforms, the serial I/O APIC bus interface of the ICH4-M should be disabled. I/O (x) APIC is supported on the platform and the servicing of interrupts is accomplished via a BFSB interrupt delivery mechanism.

The serial I/O APIC bus interface of the ICH4-M should be disabled as follows.

1. Tie APICCLK directly to ground.
2. Tie APICD0, APICD1 to ground through a 10-k resistor. (Separate pull-downs are required if using XOR chain testing)

The processors discussed in this document do not have pins dedicated for a serial I/O APIC bus interface and thus, no hardware change is necessary. However, it is strongly encouraged to enable I/O APIC support in the BIOS and operating system on 852GME/852GMV/852PMbased systems rather than the legacy 8259 interrupt controller due to the performance benefits and efficiencies that the I/O (x) APIC architecture enjoys over the older PIC architecture.

## 10.6. SMBus 2.0/SMLink Interface

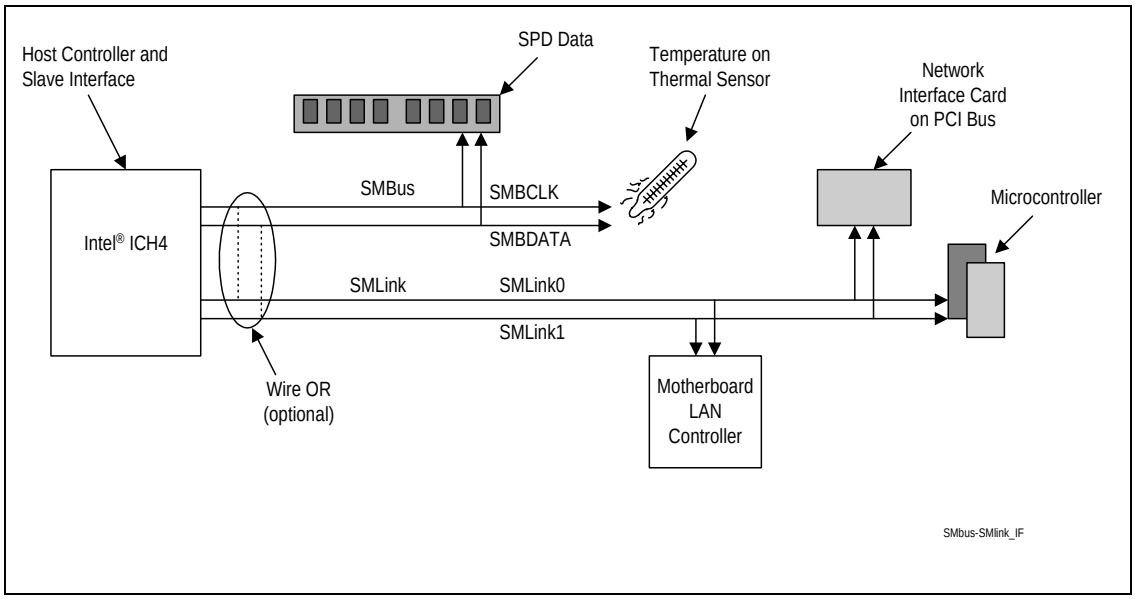
The SMBus interface on the ICH4-M uses two signals SMBCLK and SMBDATA to send and receive data from components residing on the bus. These signals are used exclusively by the SMBus host controller. The SMBus host controller resides inside the ICH4-M.

The ICH4-M incorporates an SMLink interface supporting Alert-on-LAN*, Alert-on-LAN2*, and a slave functionality. It uses two signals SMLINK[1:0]. SMLINK[0] corresponds to a SMBus clock signal and SMLINK[1] corresponds to a SMBus data signal. These signals are part of the SMB slave interface.

For Alert-on-LAN functionality, the ICH4-M transmits heartbeat and event messages over the interface. When using the Intel 82562EM Platform LAN Connect component, the ICH4-M's integrated LAN controller will claim the SMLink heartbeat and event messages and send them out over the network. An external, Alert-on-LAN2*enabled LAN controller (i.e. Intel 82562EM 10/100 Mbps platform LAN connect) will connect to the SMLink signals to receive heartbeat and event messages, as well as access the ICH4-M SMBus slave interface. The slave interface function allows an external micro-controller to perform various functions. For example, the slave write interface can reset or wake a system, generate SMI# or interrupts, and send a message. The slave read interface can read the system power state, read the watchdog timer status, and read system status bits.

Both the SMBus host controller and the SMBus slave interface obey the SMBus 1.0 protocol, so the two interfaces can be externally wire-OR'ed together to allow an external management ASIC (such as Intel 82562EM 10/100 Mbps platform LAN connect) to access targets on the SMBus as well as the ICH4-M slave interface. Additionally, the ICH4-M supports slave functionality, including the Host Notify protocol, on the SMLink pins. Therefore, in order to be fully compliant with the SMBus 2.0 specification (which requires the Host Notify cycle), the SMLink and SMBus signals **must** be tied together externally. This is done by connecting SMLink[0] to SMBCLK and SMLink[1] to SMBDATA.

**Figure 67. SMBUS 2.0/SMLink Protocol**




Intel does not support external access of the ICH4-M's Integrated LAN controller via the SMLink interface. Also, Intel does not support access of the ICH4-M's SMBus slave interface by the ICH4-M's SMBus host controller. Refer to *the Intel® 82801DBM I/O Controller Hub 4 Mobile (ICH4-M) Datasheet* for full functionality descriptions of the SMLink and SMBus interface.

## 10.6.1. SMBus Architecture and Design Considerations

### 10.6.1.1. SMBus Design Considerations

SMBus design solutions will vary for all platforms. The total bus capacitance and device capabilities must be considered when designing SMBus segments. Routing SMBus to the PCI slots makes the design process even more challenging since they add so much capacitance to the bus. This extra capacitance has a large affect on the bus time constant which in turn affects the bus rise and fall times.

Primary considerations in the design process are:

1. Device class (High/Low power). Most designs use primarily high power devices.
2. Are there devices that must run in S3?
3. Amount of $V_{CC_SUSPEND}$ current available, i.e. minimizing load of $V_{CC_SUSPEND}$.

### 10.6.1.2. General Design Issues/Notes

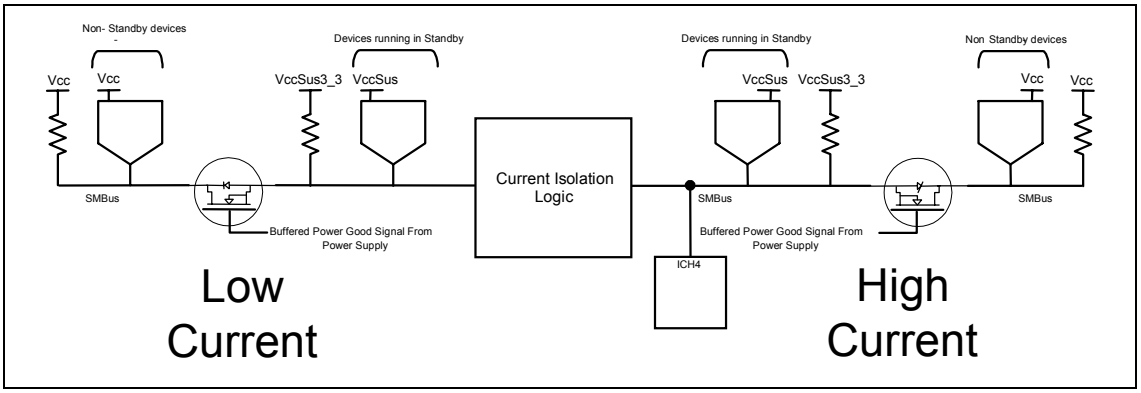
Regardless of the architecture used, there are some general considerations.

1. The pull-up resistor size for the SMBus data and clock signals is dependent on the bus load (this includes all device leakage currents). Generally the SMBus device that can sink the least amount of current is the limiting agent on how small the resistor can be. The pull-up resistor cannot be made so large that the bus time constant (Resistance X capacitance) does not meet the SMBus rise and fall time specification.
2. The maximum bus capacitance that a physical segment can reach is 400 pF.
3. The Intel ICH4-M does not run SMBus cycles while in S3.
4. SMBus devices that can operate in S3 must be powered by the $V_{CC_SUSPEND}$ supply.

### 10.6.1.3. High Power/Low Power Mixed Architecture

This design allows for current isolation of high and low current devices while also allowing SMBus devices to communicate during the S3 state. $V_{CC_SUSPEND}$ leakage is minimized by keeping non-essential devices on the core supply. This is accomplished by the use of a "FET" to isolate the devices powered by the core and suspend supplies. See Figure 68.

**Figure 68. High Power/Low Power Mixed $V_{CC_SUSPEND}$/$V_{CC_CORE}$ Architecture**




Added Considerations for Mixed Architecture

1. The bus switch must be powered by $V_{CC_SUSPEND}$.
2. Devices that are powered by the $V_{CC_SUSPEND}$ well must not drive into other devices that are powered off. This is accomplished with the "bus switch."
3. The bus bridge can be a device like the Phillips PCA9515.

### 10.6.1.4. Calculating the Physical Segment Pull-Up Resistor

The following tables are provided as a reference for calculating the value of the pull-up resistor that may be used for a physical bus segment. If any physical bus segment exceeds 400 pF, then a bus bridge device like the Phillips* PCA9515 must be used to separate the physical segment into two segments that individually have a bus capacitance less than 400 pF.

### Table 67. Bus Capacitance Reference Chart

| Device | # of Devices/ Trace Length | Capacitance Includes | Cap (pF) |
|---|---|---|---|
| ICH4-M | 1 | Pin Capacitance | 12 |
| CK408 | 1 | Pin Capacitance | 10 |
| SO-DIMMS | 2 | Pin Capacitance (10 pF) + 1 inch worth of trace capacitance (2 pF/inch) per SO-DIMM and 2 pF connector capacitance per SO-DIMM | 28 |
| | 3 | | 42 |
| PCI Slots | 2 | Each PCI add-in card is allowed up to 40 pF + 3 pF per each connector | 86 |
| | 3 | | 129 |
| | 4 | | 172 |
| | 5 | | 215 |
| | 6 | | 258 |
| Bus Trace Length in inches | ≥24 | 2 pF per inch of trace length | 48 |
| | ≥36 | | 72 |
| | ≥48 | | 96 |

### Table 68. Bus Capacitance/Pull-Up Resistor Relationship

| Physical Bus Segment Capacitance | Pull-Up Range (For Vcc = 3.3 V |
|---|---|
| 0 to 100 pF | 8.2 k to 1.2 k |
| 100 to 200 pF | 4.7 k to 1.2 k |
| 200 to 300 pF | 3.3 k to 1.2 k |
| 300 to 400 pF | 2.2 k to 1.2 k |

# 10.7. FWH

The following provides general guidelines for compatibility and design recommendations for supporting the FWH device. The majority of the changes will be incorporated in the BIOS. Refer to the *FWH BIOS Specification* or equivalent.

## 10.7.1. FWH Decoupling

Refer to Section 12.7.6 for more details.

## 10.7.2. In Circuit FWH Programming

All cycles destined for the FWH will appear on PCI. The ICH4-M hub interface to PCI bridge will put all CPU boot cycles out on PCI (before sending them out on the FWH interface). If the ICH4-M is set for subtractive decode, these boot cycles can be accepted by a positive decode agent on the PCI bus. This enables the ability to boot from a PCI card that positively decodes these memory cycles. In order to boot from a PCI card, it is necessary to keep the ICH4-M in subtractive decode mode. If a PCI boot card is inserted and the ICH4-M is programmed for positive decode, there will be two devices positively decoding the same cycle.

## 10.7.3. FWH INIT# Voltage Compatibility

The FWH INIT# signal trip points need to be considered because they are NOT consistent among different FWH manufacturers. The INIT# signal is active low. Therefore, the inactive state of the ICH4-M INIT# signal needs to be at a value slightly higher than the $V_{IH}$ min FWH INIT# pin specification. The inactive state of this signal is typically governed by the formula V_CPU_IO(min) – noise margin. Therefore, if the V_CPU_IO(min) of the processor is 1.60 V, the noise margin is 200 mV and the $V_{IH}$ min spec of the FWH INIT# input signal is 1.35 V, there would be no compatibility issue because 1.6 V – 0.2 V = 1.40 V which is greater than the 1.35 V minimum of the FWH. If the $V_{IH}$ min of the FWH was 1.45 V, then there would be an incompatibility and logic translation would need to be used. The examples above do not take into account any noise that may be encountered on the INIT# signal. Care must be taken to ensure that the $V_{IH}$ min specification is met with ample noise margin. In applications where it is necessary to use translation logic, refer to Section 4.3.7.2.

The solution assumes that level translation is necessary. The figure in Section 4.3.7.1.7 implements a solution for the ICH4-M FWH signal INIT#. Trace lengths and resistor values can be found in Table 5.

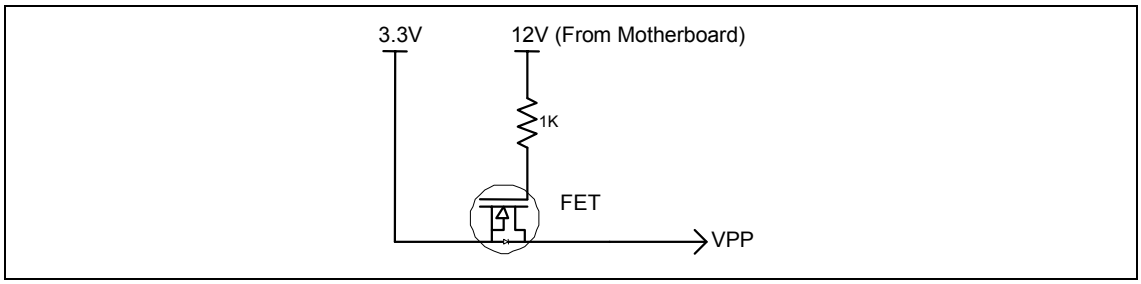
The voltage translator circuitry is shown in Figure 16. Intel strongly recommended that any system that implements a FWH should have its INIT# input connected to the ICH4-M.

## 10.7.4. FWH $V_{PP}$ Design Guidelines

The $V_{PP}$ pin on the FWH is used for programming the flash cells. The FWH supports $V_{PP}$ of 3.3 V or 12 V. If $V_{PP}$ is 12 V, the flash cells will program about 50% faster than at 3.3 V. However, the FWH only supports 12-V $V_{PP}$ for 80 hours (3.3 V on Vpp does not affect the life of the device). The 12-V $V_{PP}$ would be useful in a programmer environment, which is typically an event that occurs very infrequently (much less than 80 hours). The $V_{PP}$ pin MUST be tied to 3.3 V on the motherboard.

In some instances, it is desirable to program the FWH during assembly with the device soldered down on the board. In order to decrease programming time it becomes necessary to apply 12 V to the $V_{PP}$ pin. The following circuit will allow testers to put 12 V on the $V_{PP}$ pin while keeping this voltage separated from the 3.3-V plane to which the rest of the power pins are connected. This circuit also allows the board to operate with 3.3 V on this pin during normal operation.

**Figure 69. FWH VPP Isolation Circuitry**




## 10.7.5. FWH INIT# Assertion/Deassertion Timings

Due to the large routing solution space and necessity of a voltage translator in the design of a FWH on 852GME/852GMV/852PMand ICH4-M based platforms, the following timing requirements must be met to ensure proper system operation.

For INIT# assertion timings, a conservative analysis of the worst case signal propagation times shows that no timing concerns exist because the ICH4-M asserts INIT# for 16 PCI clocks (485 ns) before deasserting. This provides adequate time for INIT# to propagate to both the processor and FWH.

For the INIT# deassertion event, the critical timing is the minimum period of time before the processor is ready to begin fetching code from the FWH after the INIT# based reset begins. This minimum period is conservatively set at 1 CPU clock (10 ns). This also represents the maximum allowed propagation time for the INIT# signal from the ICH4-M to the FWH.

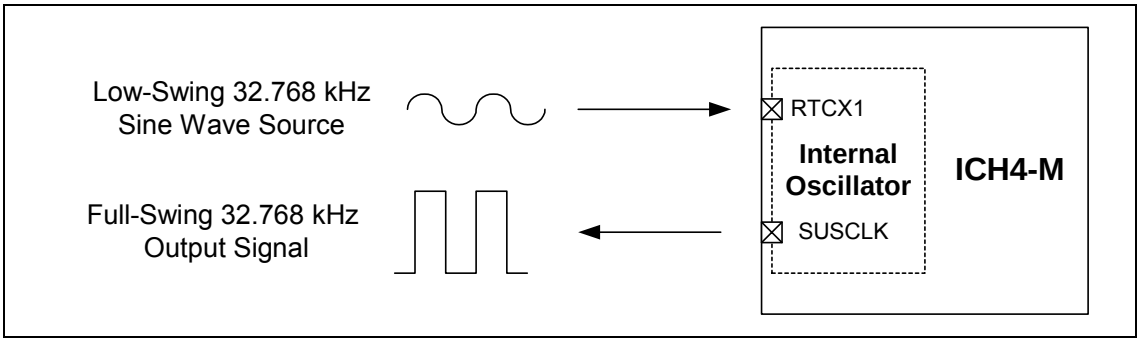
Systems that use alternative devices (i.e. not a FWH) to store the firmware may or may not require the use of INIT#. If INIT# is not used, an analysis should be done to ensure there is no negative impact to system operation. If INIT# is implemented on such a device, voltage translation may be necessary, and the assertion/deassertion timings noted above still apply.

## 10.8. RTC

The Intel 82801DBM ICH4-M contains a real time clock (RTC) with 256 bytes of battery backed SRAM. The internal RTC module provides two key functions: keeping date and time and storing system data in its RAM when the system is powered down.

The ICH4-M uses a crystal circuit to generate a low-swing 32-kHz input sine wave. This input is amplified and driven back to the crystal circuit via the RTCX2 signal. Internal to the ICH4-M, the RTCX1 signal is amplified to drive internal logic as well as generate a free running full swing clock output for system use. This output ball of the ICH4-M is called SUSCLK. This is illustrated in Figure 70.

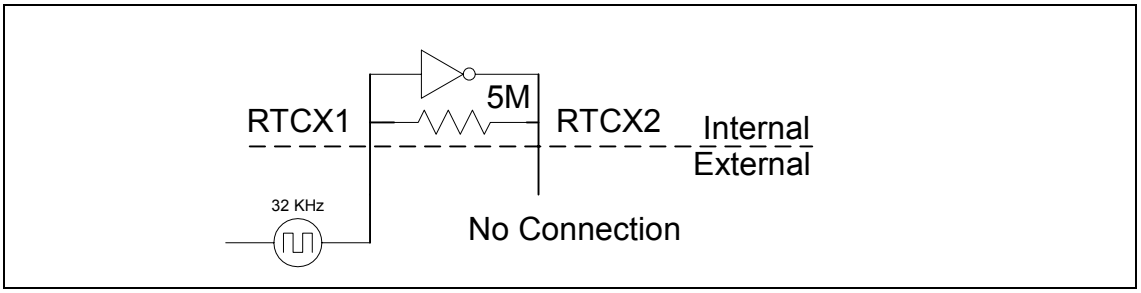
**Figure 70. RTCX1 and SUSCLK Relationship in ICH4-M**




For further information on the RTC, please consult Application Note AP-728 *ICH Family Real Time Clock (RTC) Accuracy and Considerations Under Test Conditions*. This application note is valid for the ICH4-M.

Even if the ICH4-M internal RTC is not used, it is still necessary to supply a clock input to RTCX1 of the ICH4-M because other signals are gated off that clock in suspend modes. However, in this case the frequency accuracy (32.768 kHz) of the clock inputs is not critical; a cheap crystal can be used or a single clock input can be driven into RTCX1with RTCX2 left as no connect; Figure 71 illustrates the connection. **This is not a validated feature on the ICH4-M. Please note that the peak-to-peak swing on RTCX1 cannot exceed 1.0 V.**

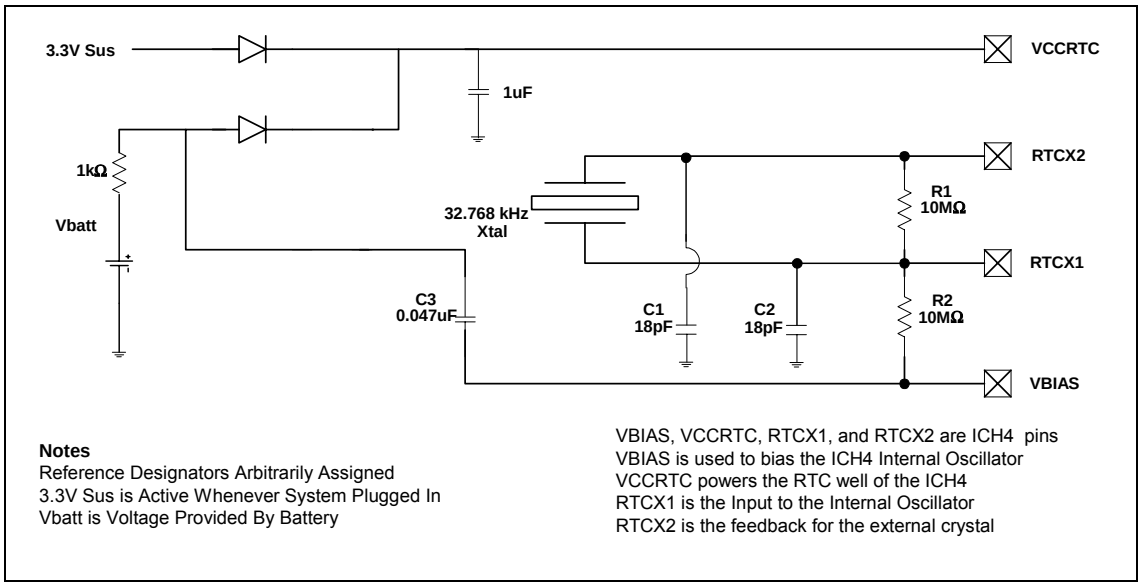
**Figure 71. External Circuitry for the ICH4-M Where the Internal RTC is Not Used**



## 10.8.1. RTC Crystal

The Intel 82801DBM ICH4-M RTC module requires an external oscillating source of 32.768 kHz connected on the RTCX1 and RTCX2 balls. Figure 72 documents the external circuitry that comprises the oscillator of the ICH4-M RTC.

**Figure 72. External Circuitry for the ICH4-M RTC**




**NOTES:**

1. The exact capacitor value needs to be based on what the crystal maker recommends. (Typical values for C1 and C2 are 18 pF, based on crystal load of 12.5 pF.)
2. $V_{CCRTC}$: Power for RTC Well
3. RTCX2: Crystal Input 2 – Connected to the 32.7 68 kHz crystal.
4. RTCX1: Crystal Input 1 – Connected to the 32.7 68 kHz crystal.
5. $V_{BIAS}$: RTC BIAS Voltage – This ball is used to provide a reference voltage and this DC voltage sets a current, which is mirrored throughout the oscillator and buffer circuitry.
6. $V_{SS}$: Ground

**Table 69. RTC Routing Summary**

| RTC Routing Requirements | Maximum Trace Length To Crystal | Signal Length Matching | R1, R2, C1, and C2 tolerances | Signal Referencing |
|---|---|---|---|---|
| 5 mil trace width (results in ~2 pF per inch) | 1 inch | NA | R1 = R2 = 10 M ± 5%<br>C1 = C2 = (NPO class)<br>See Section 10.9.2 for calculating a specific capacitance value for C1 and C2 | Ground |

## 10.8.2. External Capacitors

To maintain the RTC accuracy, the external capacitor $C_3$ needs to be 0.047 µF and capacitor values $C_1$ and $C_2$ should be chosen to provide the manufacturer's specified load capacitance ($C_{load}$) for the crystal when combined with the parasitic capacitance of the trace, socket (if used), and package. The following equation can be used to choose the external capacitance values.

**Equation 3.**

$$C_{load} = [(C_1 + C_{in1} + C_{trace1})*(C_2 + C_{in2} + C_{trace2})]/[(C_1 + C_{in1} + C_{trace1} + C_2 + C_{in2} + C_{trace2})] + C_{parasitic}$$

Where:

$C_{load}$ = Crystal's load capacitance. This value can be obtained from Crystal's specification.

$C_{in1}$, $C_{in2}$ = input capacitances at RTCX1, RTCX2 balls of the ICH4-M. These values can be obtained in the ICH4-M's data sheet.

$C_{trace1}$, $C_{trace2}$ = Trace length capacitances measured from Crystal terminals to RTCX1, RTCX2 balls. These values depend on the characteristics of board material, the width of signal traces and the length of the traces. A typical value, based on a 5 mil wide trace and a ½ ounce copper pour, is approximately equal to :

$$C_{trace} = \text{trace length} * 2 \text{ pF/inch}$$

$C_{parasitic}$ = Crystal's parasitic capacitance. This capacitance is created by the existence of 2 electrode plates and the dielectric constant of the crystal blank inside the Crystal part. Refer to the crystal's specification to obtain this value.

Ideally, $C_1$, $C_2$ can be chosen such that $C_1 = C_2$. Using the equation of $C_{load}$ above, the value of $C_1$, $C_2$ can be calculated to give the best accuracy (closest to 32.768 kHz) of the RTC circuit at room temperature. However, $C_2$ can be chosen such that $C_2 > C_1$. Then $C_1$ can be trimmed to obtain the 32.768 kHz.

In certain conditions, both $C_1$, $C_2$ values can be shifted away from the **theoretical values** (calculated values from the above equation) to obtain the closest oscillation frequency to 32.768 kHz. When $C_1$, $C_2$ values are smaller then the theoretical values, the RTC oscillation frequency will be higher.

The following example illustrates the use of the practical values $C_1$, $C_2$ in the case that theoretical values cannot guarantee the accuracy of the RTC in low temperature condition:

**Example:**

According to a required 12-pF load capacitance of a typical crystal that is used with the ICH4-M, the calculated values of $C_1 = C_2$ is 10 pF at room temperature (25°C) to yield a 32.768-kHz oscillation.

At 0°C the frequency stability of crystal gives – 23 ppm (assumed that the circuit has 0 ppm at 25°C). This makes the RTC circuit oscillate at 32.767246 kHz instead of 32.768 kHz.

If the values of $C_1$, $C_2$ are chosen to be 6.8 pF instead of 10 pF, the RTC will oscillate at a higher frequency at room temperature (+23 ppm) but this configuration of $C_1$ / $C_2$ makes the circuit oscillate closer to 32.768 kHz at 0°C. The 6.8-pF value of C1 and 2 is the **practical value**.

Note that the temperature dependency of crystal frequency is a parabolic relationship (ppm / degree square). The effect of changing the crystal's frequency when operating at 0°C (25°C below room temperature) is the same when operating at 50°C (25°C above room temperature).

## 10.8.3. RTC Layout Considerations

Since the RTC circuit is very sensitive and requires high accuracy oscillation, reasonable care must be taken during layout and routing of the RTC circuit. Some recommendations are:

1. Reduce trace capacitance by minimizing the RTC trace length. The ICH4-M requires a trace length less than 1 inch on each branch (from crystal's terminal to RTCXn ball). Routing the RTC circuit should be kept simple to simplify the trace length measurement and increase accuracy on calculating trace capacitances. Trace capacitance depends on the trace width and dielectric constant of the board's material. On FR-4, a 5-mil trace has approximately 2 pF per inch.
2. Trace signal coupling must be limited as much as possible by avoiding the routing of adjacent PCI signals close to RTCX1 & RTCX2, and VBIAS.
3. Ground guard plane is highly recommended.
4. The oscillator $V_{CC}$ should be clean; use a filter, such as an RC low-pass, or a ferrite inductor.

## 10.8.4. RTC External Battery Connections

The RTC requires an external battery connection to maintain its functionality and its RAM while the ICH4-M is not powered by the system.

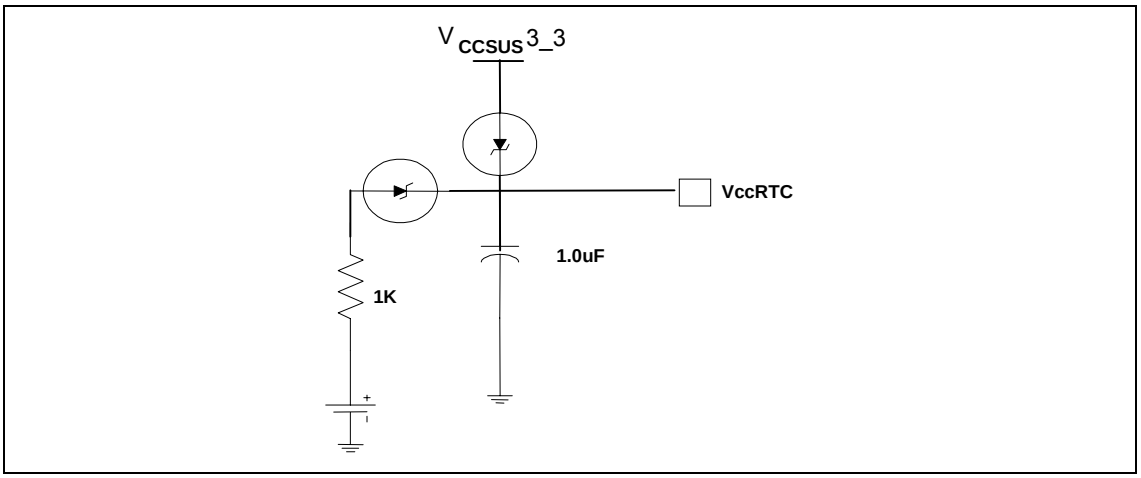
Example batteries are Duracell* 2032, 2025, or 2016 (or equivalent), which can give many years of operation. Batteries are rated by storage capacity. The battery life can be calculated by dividing the capacity by the average current required. For example, if the battery storage capacity is 170 mAh (assumed usable) and the average current required is 5 µA, the battery life will be at least:

*170,000 µAh / 5 µA = 34,000 h = 3.9 years*

The voltage of the battery can affect the RTC accuracy. In general, when the battery voltage decays, the RTC accuracy also decreases. High accuracy can be obtained when the RTC voltage is in the range of 3.0 V to 3.3 V.

The battery must be connected to the ICH4-M via a Schottky diode circuit for isolation. The Schottky diode circuit allows the ICH4-M RTC-well to be powered by the battery when the system power is not available, but by the system power when it is available. To do this, the diodes are set to be reverse biased when the system power is not available. Figure 73 is an example of a diode circuit that is used.

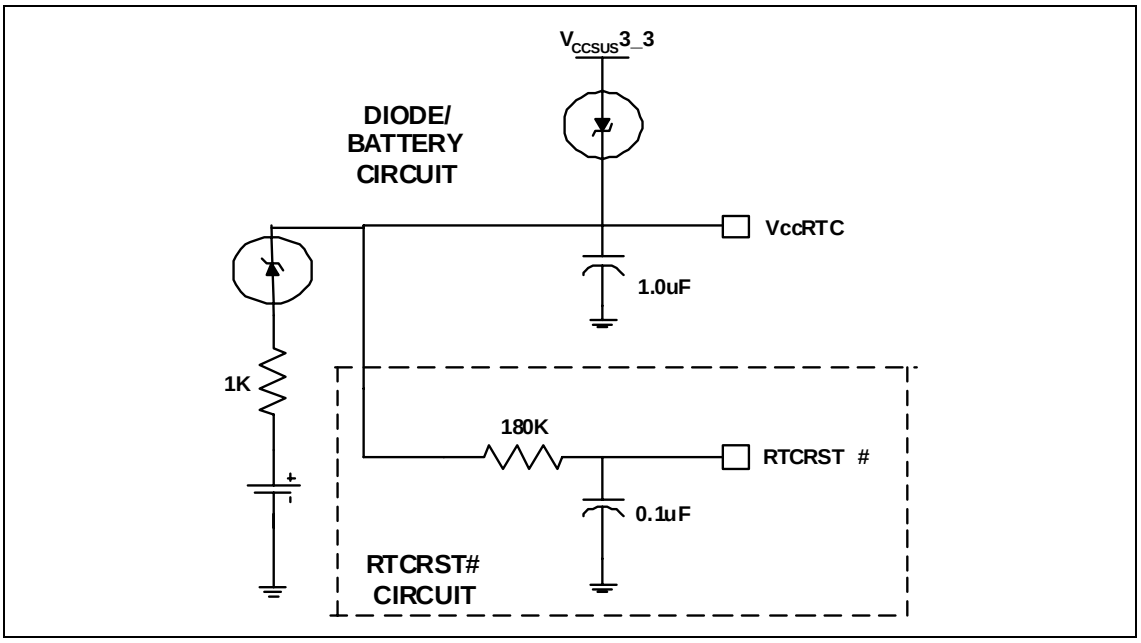
**Figure 73. Diode Circuit to Connect RTC External Battery**




A standby power supply should be used in a mobile system to provide continuous power to the RTC when available, which will significantly increase the RTC battery life and thereby the RTC accuracy.

## 10.8.5. RTC External RTCRST# Circuit

**Figure 74. RTCRST# External Circuit for the ICH4-M RTC**




The ICH4-M RTC requires some additional external circuitry. The RTCRST# signal is used to reset the RTC well. The external capacitor and the external resistor between RTCRST# and the RTC battery (VBAT) were selected to create an RC time delay, such that RTCRST# will go high some time after the battery voltage is valid. The RC time delay should be in the range of 18 ms - 25 ms. Any resistor and capacitor combination that yields the proper time constant is acceptable. When RTCRST# is asserted, bit 2 (RTC_PWR_STS) in the GEN_PMCON_3 (General PM Configuration 3) register is set to 1, and

remains set until software clears it. As a result, when the system boots, the BIOS knows that the RTC battery has been removed.

This RTCRST# circuit is combined with the diode circuit (shown in Figure 73) whose purpose is to allow the RTC well to be powered by the battery when the system power is not available. Figure 74 is an example of this circuitry that is used in conjunction with the external diode circuit.

### 10.8.6. $V_{BIAS}$ DC Voltage and Noise Measurements

VBIAS is a DC voltage level that is necessary for biasing the RTC oscillator circuit. This DC voltage level is filtered out from the RTC oscillation signal by the RC network of R2 and C3 (see Figure 72). Therefore, it is a self-adjusting voltage. Board designers should not manually bias the voltage level on VBIAS. Checking VBIAS level is used for testing purposes only to determine the right bias condition of the RTC circuit.

VBIAS should be at least 200 mV DC. The RC network of R2 and C3 will filter out most of AC signal noise that exists on this ball. However, the noise on this ball should be kept minimal in order to guarantee the stability of the RTC oscillation.

Probing VBIAS requires the same technique as probing the RTCX1, RTCX2 signals (using Op-Amp). See Application Note AP-728 for further details on measuring techniques.

***Note:*** VBIAS is very sensitive to environmental conditions.

### 10.8.7. SUSCLK

SUSCLK is a square waveform signal output from the RTC oscillation circuit. Depending on the quality of the oscillation signal on RTCX1 (largest voltage swing), SUSCLK duty cycle can be between 30-70%. If the SUSCLK duty cycle is beyond 30-70% range, it indicates a poor oscillation signal on RTCX1 and RTCX2.

SUSCLK can be probed directly using normal probe (50- input impedance probe) and it is an appropriated signal to check the RTC frequency to determine the accuracy of the ICH4-M's RTC clock (see Application Note AP-728 for further details).

### 10.8.8. RTC-Well Input Strap Requirements

All RTC-well inputs (RSMRST#, RTCRST#, INTRUDER#) must be either pulled up to $V_{CC}$RTC or pulled-down to ground while in the G3 state. RTCRST# when configured as shown in Figure 74 meets this requirement. RSMRST# should have a weak external pull-down to ground and INTRUDER# should have a weak external pull-up to $V_{CC}$RTC. This will prevent these nodes from floating in G3, and correspondingly will prevent $I_{CC}$RTC leakage that can cause excessive coin-cell drain. The PWROK input signal should also be configured with an external weak pull-down.

## 10.9. Internal LAN Layout Guidelines

The Intel 82801DBM ICH4-M provides several options for LAN capability. The platform supports several components depending upon the target market. Available LAN components include the Intel

82540EP Gigabit Ethernet Controller, Intel® 82551QM Fast Ethernet Controller, Intel® 82562ET, and Intel® 82562EM Platform LAN Connect components.

**Table 70. LAN Component Connections/Features**

| LAN Component | Interface to ICH4-M | Connection | Features |
|---|---|---|---|
| Intel® 82540EP (196 BGA) | PCI | Gigabit Ethernet (1000BASE-T) with Alert Standard Format (ASF) alerting | Gigabit Ethernet, ASF 1.0 alerting, PCI 2.2 compatible |
| Intel® 82551QM (196 BGA) | PCI | Performance 10/100 Ethernet with ASF alerting | Ethernet 10/100 connection, ASF 1.0 alerting, PCI 2.2 compatible |
| Intel® 82562EM (48 Pin SSOP) | LCI | Advanced 10/100 Ethernet | Ethernet 10/100 connection, Alert on LAN* (AoL) |
| Intel® 82562ET (48 Pin SSOP) | LCI | Basic 10/100 Ethernet | Ethernet 10/100 connection |

**NOTE:** Design guidelines are provided for each required interface and connection.

## 10.9.1. Footprint Compatibility

The Intel 82540EP Gigabit Ethernet Controller and the Intel 82551QM Fast Ethernet Controller are all manufactured in a footprint compatible 15 mm x 15 mm (1-mm pitch), 196-ball grid array package. Many of the critical signal pin locations on the 82540EM and the 82551QM are identical, allowing designers to create a single design that accommodates any one of these parts. Because the usage of some pins on the 82540EM differs from the usage on the 82551QM, the parts are not referred to as “pin compatible.” The term “footprint compatible” refers to the fact that the parts share the same package size, same number and pattern of pins, and layout of signals. This allows for flexible, cost effective, and multipurpose design.

Design guidelines are provided for each required interface and connection. Refer to the following figures and the subsequent table for the corresponding section of this design guide.

**Figure 75. Intel 82801DBM ICH4-M/Platform LAN Connect Section**

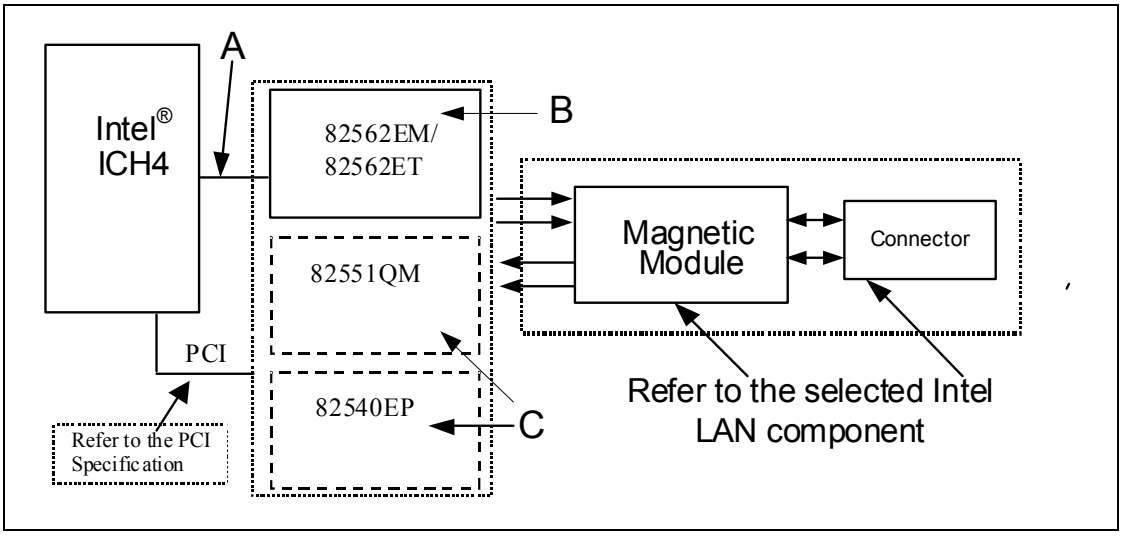


**Table 71. LAN Design Guide Section Reference**

| Layout Section | Figure 75 Reference | Design Guide Section |
|---|---|---|
| Intel ICH4-M – LAN Connect Interface (LCI) | A | Reference Section 10.9.2 |
| Intel 82562ET / Intel 82562EM | B | Reference Section 10.9.2 |
| Intel 82551QM / Intel 82540EP | C | Reference Section 10.9.5 |

## 10.9.2. Intel® 82801DBM ICH4-M – LAN Connect Interface Guidelines

This section contains guidelines on how to implement a Platform LAN Connect device on a system motherboard. It should not be treated as a specification and the system designer must ensure that the system meets the specified timings. Special care must be given to matching the LAN_CLK traces to those of the other signals. The following signal lines are used on this interface:

LAN_CLK

LAN_RSTSYNC

LAN_RXD[2:0]

LAN_TXD[2:0]

This interface supports Intel 82562ET and Intel 82562EM components. Signal lines LAN_CLK, LAN_RSTSYNC, LAN_RXD[0], and LAN_TXD[0] are shared by all components. The AC characteristics for this interface are found in the *Intel® 82801DBM I/O Controller Hub 4 Mobile (ICH4-M) Specification Update.*

### 10.9.2.1. Bus Topologies

The Platform LAN Connect Interface can be configured in several topologies:

Direct point-to-point connection between the ICH4-M and the LAN component

LOM Implementation

#### 10.9.2.1.1. LOM (LAN On Motherboard) Point-To-Point Interconnect

The following are guidelines for a single solution motherboard. Either Intel 82562EM or Intel 82562ET is uniquely installed.

**Figure 76. Single Solution Interconnect**

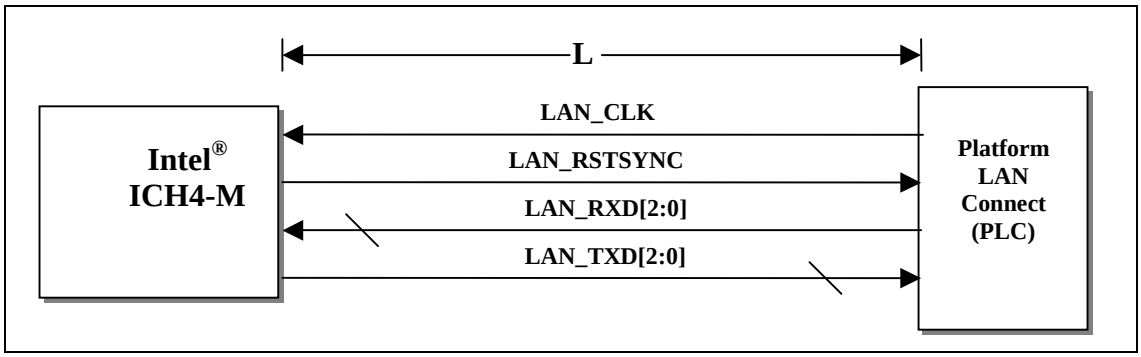


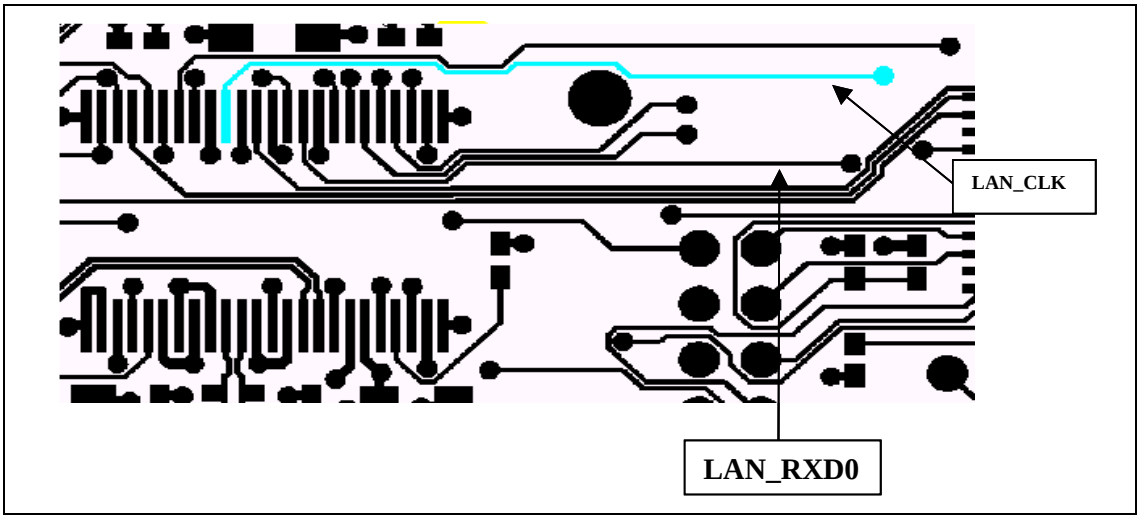
**Table 72. LAN LOM Routing Summary**

| Trace Impedance | LAN Routing Requirements | Maximum Trace Length | Signal Referencing | LAN Signal Length Matching |
|---|---|---|---|---|
| 55 ± 15% | 5 on 10 | 4.5 to 12 inches | Ground | Data signals must be equal to or no more than 0.5 inches (500 mils) shorter than the LAN clock trace. |

### 10.9.2.2. Signal Routing and Layout

Platform LAN Connect Interface signals must be carefully routed on the motherboard to meet the timing and signal quality requirements of this interface specification. The following are some general guidelines that should be followed. Intel recommends that the board designer simulate the board routing to verify that the specifications are met for flight times and skews due to trace mismatch and crosstalk. On the motherboard the length of each data trace is either equal in length to the LAN_CLK trace or up to 0.5 inches shorter than the LAN_CLK trace. (LAN_CLK should always be the longest motherboard trace in each group.)

**Figure 77. LAN_CLK Routing Example**




### 10.9.2.3. Crosstalk Consideration

Noise due to crosstalk must be carefully controlled to a minimum. Crosstalk is the key cause of timing skews and is the largest part of the $t_{RMATCH}$ skew parameter. $t_{RMATCH}$ is the sum of the trace length mismatch between LAN_CLK and the LAN data signals. To meet this requirement on the board, the length of each data trace is either equal to or up to 0.5 inches shorter than the LAN_CLK trace. Maintaining at least 100 mils of spacing should minimize noise due to crosstalk from non-PLC signals.

### 10.9.2.4. Impedances

The motherboard impedances should be controlled to minimize the impact of any mismatch between the motherboard. An impedance of 55 ± 15% is strongly recommended; otherwise, signal integrity requirements may be violated.

#### 10.9.2.5. Line Termination

Line termination mechanisms are not specified for the LAN connect interface. Slew rate controlled output buffers achieve acceptable signal integrity by controlling signal reflection, over/undershoot, and ringback. A 0- to 33- series resistor can be installed at the driver side of the interface should the developer have concerns about over/undershoot.

***Note:*** The receiver must allow for any drive strength and board impedance characteristic within the specified ranges.

#### 10.9.2.6. Terminating Unused LAN Connect Interface Signals

The LAN connect interface on the ICH4-M can be left as a no-connect if it is not used.

### 10.9.3. Intel 82562ET / Intel 82562EM Guidelines

For correct LAN performance, designers must follow the general guidelines outlined in Section 10.9.6. Additional guidelines for implementing an Intel 82562ET or Intel 82562EM Platform LAN Connect component are provided below.

#### 10.9.3.1. Guidelines for Intel 82562ET / Intel 82562EM Component Placement

Component placement can affect signal quality, emissions, and temperature of a board design. This section will provide guidelines for component placement. Careful component placement can:

Decrease potential problems directly related to electromagnetic interference (EMI), which could cause failure to meet FCC and IEEE test specifications.

Simplify the task of routing traces. To some extent, component orientation will affect the complexity of trace routing. The overall objective is to minimize turns and crossovers between traces.

Minimizing the amount of space needed for the Ethernet LAN interface is important because all other interfaces will compete for physical space on a motherboard near the connector edge. As with most subsystems, the Ethernet LAN circuits need to be as close as possible to the connector. Thus, it is imperative that all designs be optimized to fit in a very small space.

#### 10.9.3.2. Crystals and Oscillators

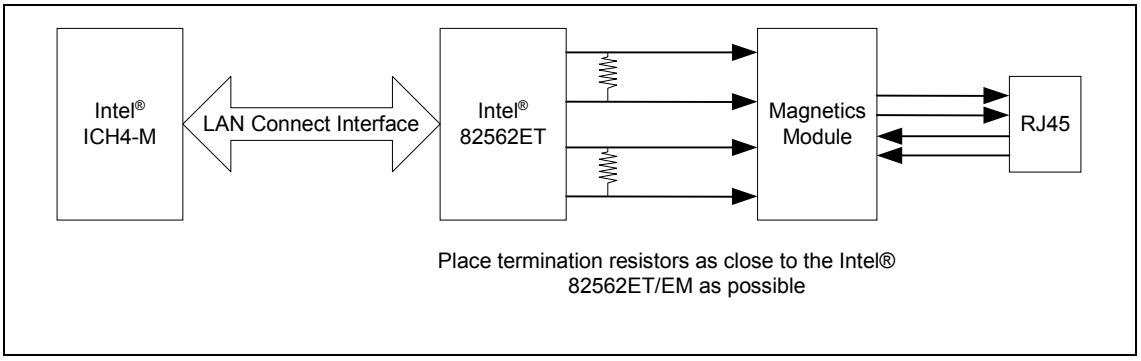
To minimize the effects of EMI, clock sources should not be placed near I/O ports or board edges. Radiation from these devices may be coupled onto the I/O ports or out of the system chassis. Crystals should also be kept away from the ethernet magnetics module to prevent interference of communication. The retaining straps of the crystal (if they should exist) should be grounded to prevent the possibility radiation from the crystal case and the crystal should lay flat against the PC board to provide better coupling of the electromagnetic fields to the board.

For a noise free and stable operation, place the crystal and associated discrete components as close as possible to the Intel 82562ET/EM, keeping the trace length as short as possible and do not route any noisy signals in this area.

### 10.9.3.3. Intel 82562ET / Intel 82562EM Termination Resistors

The 100 ± 1% resistor used to terminate the differential transmit pairs (TDP/TDN) and the 121 ± 1% receive differential pairs (RDP/RDN) should be placed as close to the Platform LAN connect component (Intel 82562ET or Intel 82562EM) as possible. This is due to the fact these resistors are terminating the entire impedance that is seen at the termination source (i.e. Intel 82562ET), including the wire impedance reflected through the transformer.

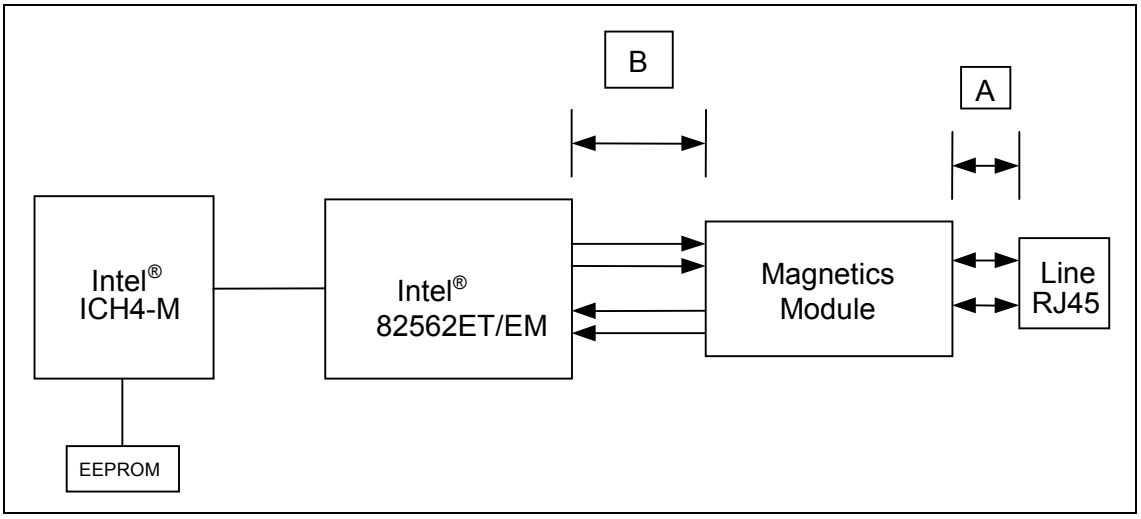
**Figure 78. Intel 82562ET / Intel 82562EM Termination**




### 10.9.3.4. Critical Dimensions

There are two dimensions to consider during layout. Distance A from the line RJ-45 connector to the magnetics module and distance B from the Intel 82562ET or Intel 82562EM to the magnetics module. The combined total distances A and B must not exceed 4 inches (preferably, less than 2 inches). See Figure 79.

**Figure 79. Critical Dimensions for Component Placement**



| Distance | Priority | Guideline |
|---|---|---|
| A | 1 | < 1 inch |
| B | 2 | < 1 inch |

#### 10.9.3.4.1. Distance from Magnetics Module to RJ-45 (Distance A)

The distance A in Figure 79 above should be given the highest priority in board layout. The distance between the magnetics module and the RJ-45 connector should be kept to less than one inch of separation. The following trace characteristics are important and should be observed:

Differential Impedance: The differential impedance should be 100 . The single ended trace impedance will be approximately 50 ; however, the differential impedance can also be affected by the spacing between the traces.

Trace Symmetry: Differential pairs (such as TDP and TDN) should be routed with consistent separation and with exactly the same lengths and physical dimensions (for example, width).

***Caution:*** Asymmetric and unequal length traces in the differential pairs contribute to common mode noise. This can degrade the receive circuit's performance and contribute to radiated emissions from the transmit circuit. If the Intel 82562ET must be placed further than a couple of inches from the RJ-45 connector, distance B can be sacrificed. Keeping the total distance between the Intel 82562ET and RJ-45 will as short as possible should be a priority.

***Note:*** Measured trace impedance for layout designs targeting 100 often result in lower actual impedance. OEMs should verify actual trace impedance and adjust their layout accordingly. If the actual impedance is consistently low, a target of 105 to 110 should compensate for second order effects.

#### 10.9.3.4.2. Distance from Intel 82562ET / 82562ET to Magnetics Module (Distance B)

Distance B should also be designed to be less than one inch between devices. The high-speed nature of the signals propagating through these traces requires that the distance between these components be closely observed. In general, any section of traces that is intended for use with high-speed signals should observe proper termination practices. Proper termination of signals can reduce reflections caused by impedance mismatches between device and traces. The reflections of a signal may have a high frequency component that may contribute more EMI than the original signal itself. For this reason, these traces should be designed to a 100- differential value. These traces should also be symmetric and equal length within each differential pair.

### 10.9.3.5. Reducing Circuit Inductance

The following guidelines show how to reduce circuit inductance in both back planes and motherboards. Traces should be routed over a continuous ground plane with no interruptions. If there are vacant areas on a ground or power plane, the signal conductors should not cross the vacant area. This increases inductance and associated radiated noise levels. Noisy logic grounds should be separated from analog signal grounds to reduce coupling. Noisy logic grounds can sometimes affect sensitive DC subsystems such as analog to digital conversion, operational amplifiers, etc. All ground vias should be connected to every ground plane; and similarly, every power via, to all power planes at equal potential. This helps reduce circuit inductance. Another recommendation is to physically locate grounds to minimize the loop area between a signal path and its return path. Rise and fall times should be as slow as possible because

signals with fast rise and fall times contain many high frequency harmonics that can radiate significantly. The most sensitive signal returns closest to the chassis ground should be connected together. This will result in a smaller loop area and reduce the likelihood of crosstalk. The effect of different configurations on the amount of crosstalk can be studied using electronics modeling software.

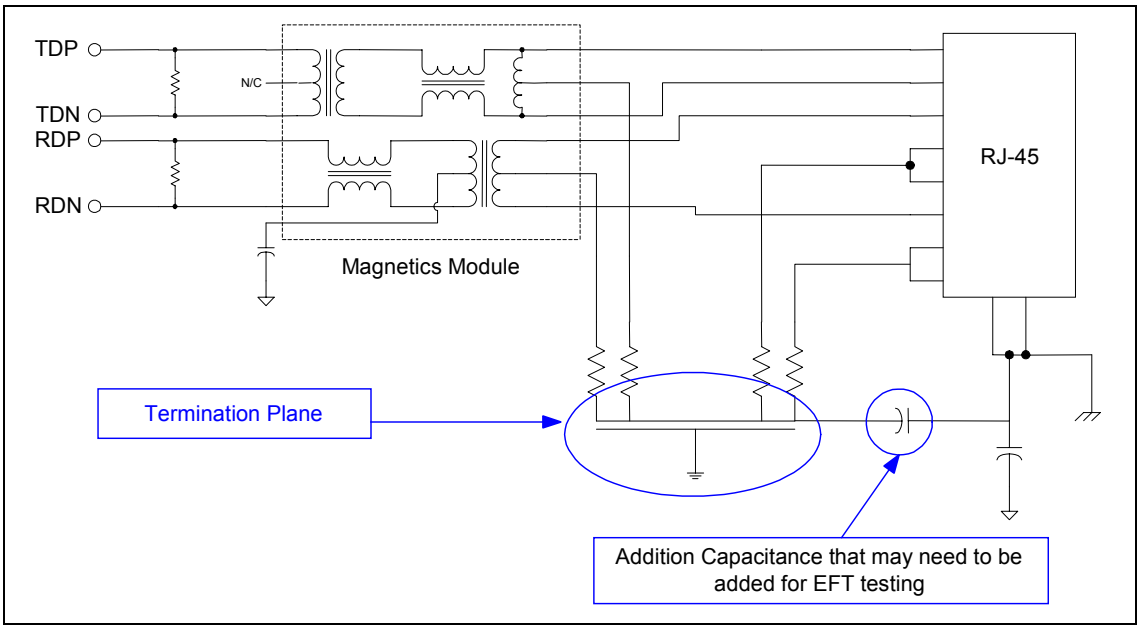
#### 10.9.3.5.1. Terminating Unused Connections

In Ethernet designs, it is common practice to terminate unused connections on the RJ-45 connector and the magnetics module to ground. Depending on overall shielding and grounding design, this may be done to the chassis ground, signal ground, or a termination plane. Care must be taken when using various grounding methods to insure that emission requirements are met. The method most often implemented is called the "Bob Smith" Termination. In this method, a floating termination plane is cut out of a power plane layer. This floating plane acts as a plate of a capacitor with an adjacent ground plane. The signals can be routed through 75- resistors to the plane. Stray energy on unused pins is then carried to the plane.

#### 10.9.3.5.2. Termination Plane Capacitance

Intel recommends that the termination plane capacitance equal a minimum value of 1500 pF. This helps reduce the amount of crosstalk on the differential pairs (TDP/TDN and RDP/RDN) from the unused pairs of the RJ-45. Pads may be placed for an additional capacitance to chassis ground, which may be required if the termination plane capacitance is not large enough to pass EFT (Electrical Fast Transient) testing. If a discrete capacitor is used, to meet the EFT requirements it should be rated for at least 1000 Vac.

**Figure 80. Termination Plane**

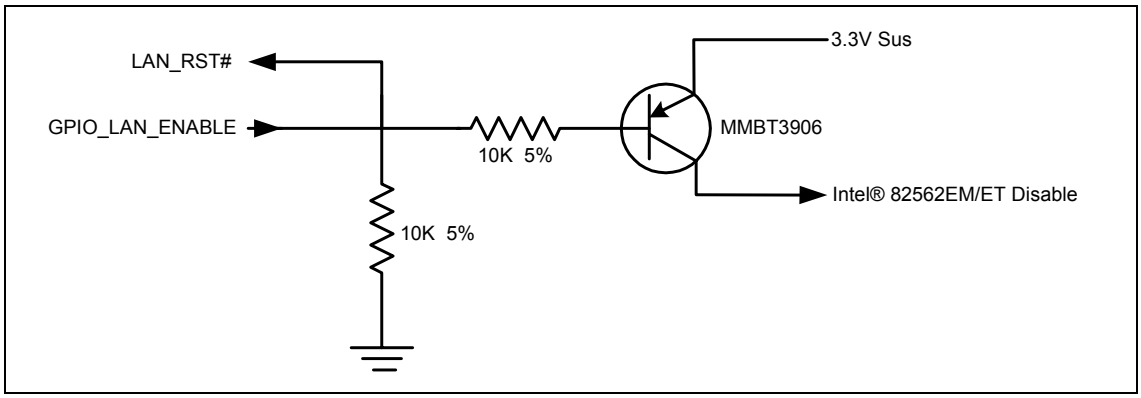


## 10.9.4. Intel 82562ET/EM Disable Guidelines

To disable the Intel 82562ET/EM, the device must be isolated (disabled) prior to reset (RSM_PWROK) asserting. Using a GPIO, such as GPO28 to be LAN_Enable (enabled high), LAN will default to enabled on initial power-up and after an AC power loss. This circuit shown below will allow this behavior. The BIOS controlling the GPIO can disable the LAN micro-controller.

***Note:*** LAN_RST# needs to be held low for 10ms after power is stable. It is assumed that RSMRST# logic will provide this delay. Because GPIO28 will default to high during power up, an AND gate has been implemented to ensure the required delay for LAN_RST# is met.

**Figure 81. Intel 82562ET/EM Disable and Power Down Circuitry**




There are four pins that can put the Intel 82562ET/EM controller in different operating states: Test_En, Isol_Tck, Isol_Ti, and Isol_Tex. Table 73 describes the operational/disable features for this design.

The four control signals shown in the below table should be configured as follows: Test_En should be pulled-down thru a 100- resistor. The remaining three control signals should each be connected through 100- series resistors to the common node “Intel 82562ET/EM _Disable” of the disable circuit.

**Table 73. Intel 82562ET/EM Control Signals**

| Test_En | Isol_Tck | Isol_Ti | Isol_Tex | State |
|---|---|---|---|---|
| 0 | 0 | 0 | 0 | Enabled |
| 0 | 1 | 1 | 1 | Disabled w/ Clock (low power) |
| 1 | 1 | 1 | 1 | Disabled w/out Clock (lowest power) |

In addition, if the LAN Connect Interface of the ICH4-M is not used, the VccLAN1_5 and the VccLAN3_3 are still required to be powered during normal operating states. It is acceptable to power the VccLAN1_5 and VccLAN3_3 power pins by the same voltage source that supplies power to the Vcc1_5 and Vcc3_3 power pins. Also, the LAN_RST# pin of the ICH4-M should be pulled-down to GND with a 10-k resistor to keep the interface disabled.

## 10.9.5. Design and Layout Consideration for Intel 82540EP / 82551QM

For specific design and layout considerations for the Intel 82540EP Gigabit Ethernet Controller and the Intel 82551QM Faster Ethernet Controller, please refer to the following documents:

*82551QM / 82540EM Interchangeable LOM Design Application Note (AP 432) (Reference #10565)*

*82540EP Gigabit Ethernet Controller Networking Silicon Product Preview Datasheet*

*82540EP Gigabit Ethernet Controller Specification Update*

*82540EP/82541EI & 82562EZ(EX) Dual Footprint Design Guide Application Note (AP-444) (Reference# 12504)*

## 10.9.6. General Intel 82562ET/82562EM/82551QM/82540EP Differential Pair Trace Routing Considerations

Trace routing considerations are important to minimize the effects of crosstalk and propagation delays on sections of the board where high-speed signals exist. Signal traces should be kept as short as possible to decrease interference from other signals, including those propagated through power and ground planes.

Observe the following suggestions to help optimize board performance.

***Note:*** Some suggestions are specific to a 4.3-mil stack-up.

Maintain constant symmetry and spacing between the traces within a differential pair.

Keep the signal trace lengths of a differential pair equal to each other.

Keep the total length of each differential pair under 4 inches. (Many customer designs with differential traces longer than 5 inches have had one or more of the following issues: IEEE phy conformance failures, excessive EMI (Electro Magnetic Interference), and/or degraded receive BER (Bit Error Rate).)

Do not route the transmit differential traces closer than 100 mils to the receive differential traces.

Do not route any other signal traces both parallel to the differential traces, and closer than 100 mils to the differential traces (300 mils is recommended).

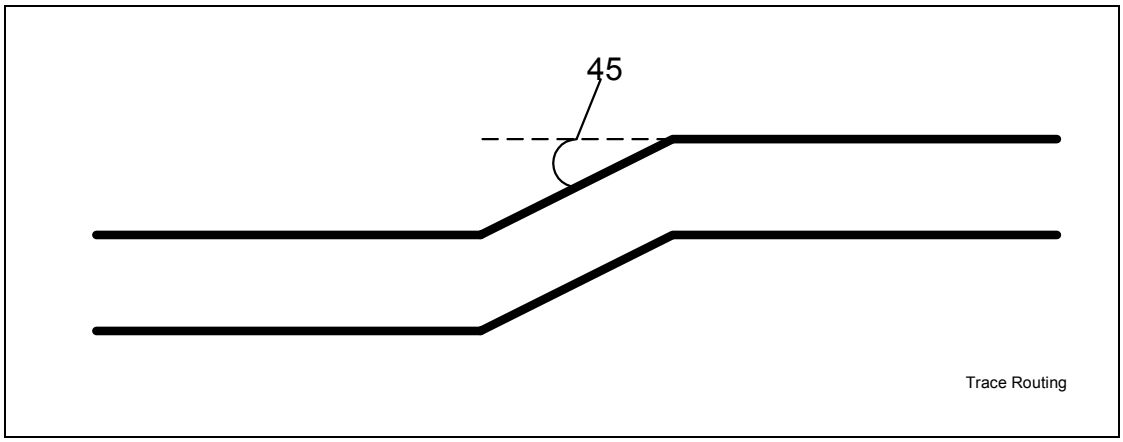
Keep maximum separation between differential pairs to 7 mils.

For high-speed signals, the number of corners and vias should be kept to a minimum. If a 90° bend is required, it is recommended to use two 45° bends instead. Refer to Figure 82.

Traces should be routed away from board edges by a distance greater than the trace height above the ground plane. This allows the field around the trace to couple more easily to the ground plane rather than to adjacent wires or boards.

Do not route traces and vias under crystals or oscillators. This will prevent coupling to or from the clock. And as a general rule, place traces from clocks and drives at a minimum distance from apertures by a distance that is greater than the largest aperture dimension.

**Figure 82. Trace Routing**




### 10.9.6.1.1. Trace Geometry and Length

The key factors in controlling trace EMI radiation are the trace length and the ratio of trace-width to trace-height above the ground plane. To minimize trace inductance, high-speed signals and signal layers that are close to a ground or power plane should be as short and wide as practical. Ideally, this trace width to height above the ground plane ratio is between 1:1 and 3:1. To maintain trace impedance, the width of the trace should be modified when changing from one board layer to another if the two layers are not equidistant from the power or ground plane. Differential trace impedances should be controlled to be approximately 100 . It is necessary to compensate for trace-to-trace edge coupling, which can lower the differential impedance by up to 10 , when the traces within a pair are closer than 30 mils (edge to edge).

Traces between decoupling and I/O filter capacitors should be as short and wide as practical. Long and thin traces are more inductive and reduce the intended effect of decoupling capacitors. Also, for similar reasons traces to I/O signals and signal terminations should be as short as possible. Vias to the decoupling capacitors should be sufficiently large in diameter to decrease series inductance. Additionally, the PLC should not be closer than one inch to the connector/magnetics/edge of the board.

### 10.9.6.1.2. Signal Isolation

Some rules to follow for signal isolation:

Separate and group signals by function on separate layers if possible. Maintain a gap of 100 mils between all differential pairs (Ethernet) and other nets, but group associated differential pairs together.

***Note:*** Over the length of the trace run, each differential pair should be at least 0.3 inches away from any parallel signal traces.

Physically group together all components associated with one clock trace to reduce trace length and radiation.

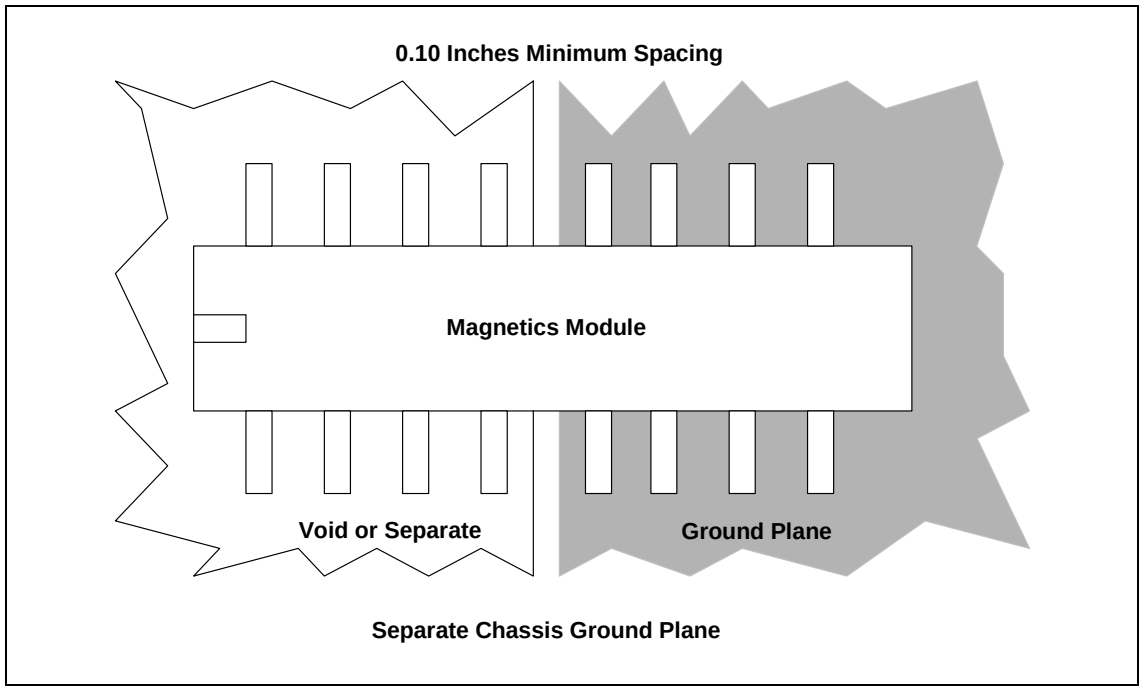
Isolate I/O signals from high speed signals to minimize crosstalk, which can increase EMI emission and susceptibility to EMI from other signals.

Avoid routing high-speed LAN traces near other high-frequency signals associated with a video controller, cache controller, CPU, or other similar devices.

#### 10.9.6.1.3. Magnetics Module General Power and Ground Plane Considerations

To properly implement the common mode choke functionality of the magnetics module the chassis or output ground (secondary side of transformer) should be separated from the digital or input ground (primary side) by a physical separation of 100 mils minimum

**Figure 83. Ground Plane Separation**




Good grounding requires minimizing inductance levels in the interconnections and keeping ground returns short, signal loop areas small, and power inputs bypassed to signal return, will significantly reduce EMI radiation.

Some rules to follow that will help reduce circuit inductance in both back planes and motherboards.

Route traces over a continuous plane with no interruptions (don't route over a split plane). If there are vacant areas on a ground or power plane, avoid routing signals over the vacant area. This will increase inductance and EMI radiation levels.

Separate noisy digital grounds from analog grounds to reduce coupling. Noisy digital grounds may affect sensitive DC subsystems.

All ground vias should be connected to every ground plane; and every power via should be connected to all power planes at equal potential. This helps reduce circuit inductance.

Physically locate grounds between a signal path and its return. This will minimize the loop area.

Avoid fast rise/fall times as much as possible. Signals with fast rise and fall times contain many high frequency harmonics, which can radiate EMI.

The ground plane beneath the filter/transformer module should be split. The RJ-45 connector side of the transformer module should have chassis ground beneath it. By splitting ground planes beneath transformer, noise coupling between the primary and secondary sides of the transformer and between the adjacent coils in the transformer is minimized. There should not be a power plane under the magnetics module.

### 10.9.6.2. Common Physical Layout Issues

A list of common physical layer design and layout mistakes in LAN on motherboard designs is provide below:

1. Unequal length of the two traces within a differential pair. Inequalities create common-mode noise and will distort the transmit or receive waveforms.
2. Lack of symmetry between the two traces within a differential pair. (Each component and/or via that one trace encounters, the other trace must encounter the same component or a via at the same distance from the PLC.) Asymmetry can create common-mode noise and distort the waveforms.
3. Excessive distance between the PLC and the magnetics or between the magnetics and the RJ-45 connector. Beyond a total distance of about 4 inches, it can become extremely difficult to design a spec-compliant LAN product. Long traces on FR4 (fiberglass epoxy substrate) will attenuate the analog signals. In addition, any impedance mismatch in the traces will be aggravated if they are longer (see #9 below). The magnetics should be as close to the connector as possible (≤ one inch).
4. Routing any other trace parallel to and close to one of the differential traces. Crosstalk getting onto the receive channel will cause degraded long cable BER. Crosstalk getting onto the transmit channel can cause excessive emissions (failing FCC) and can cause poor transmit BER on long cables. At a minimum, other signals should be kept 0.3 inches from the differential traces.
5. Routing the transmit differential traces next to the receive differential traces. The transmit trace that is closest to one of the receive traces will put more crosstalk onto the closest receive trace and can greatly degrade the receiver's BER over long cables. After exiting the PLC, the transmit traces should be kept 0.3 inches or more away from the nearest receive trace. The only possible exceptions are in the vicinities where the traces enter or exit the magnetics, the RJ-45, and the PLC.
6. Use of an inferior magnetics module. The magnetics modules that we use have been fully tested for IEEE PLC conformance, long cable BER, and for emissions and immunity. (Inferior magnetics modules often have less common-mode rejection and/or no auto transformer in the transmit channel.)
7. Use of an 82555 or 82558 physical layer schematic in a PLC design. The transmit terminations and decoupling are different. There are also differences in the receive circuit. Please follow the appropriate reference schematic or application note.
8. Not using (or incorrectly using) the termination circuits for the unused pins at the RJ-45 and for the wire-side center-taps of the magnetics modules. These unused RJ pins and wire-side center-taps must be correctly referenced to chassis ground via the proper value resistor and a capacitance or termplane. If these are not terminated properly, there can be emissions (FCC) problems, IEEE conformance issues, and long cable noise (BER) problems. The application notes have schematics that illustrate the proper termination for these unused RJ pins and the magnetics center-taps.
9. Incorrect differential trace impedances. It is important to have approximately 100- impedance between the two traces within a differential pair. This becomes even more important as the differential traces become longer. It is very common to see designs that have differential trace impedances between 75 and 85 , even when designed for 100 . (To calculate differential impedance, many impedance calculators only multiply the single-ended impedance by two. This does not take into account edge-to-edge capacitive coupling between the two traces. When the

two traces within a differential pair are kept close† to each other, the edge coupling can lower the effective differential impedance by 5 - 20 . A 10- - 15- drop in impedance is common.) Short traces will have fewer problems if the differential impedance is a little off.

10. Use of capacitor that is too large between the transmit traces and/or too much capacitance from the magnetic's transmit center-tap (on the Intel 82562ET side of the magnetics) to ground. Using capacitors more than a few pF in either of these locations can slow the 100 Mbps rise and fall time so much that they fail the IEEE rise time and fall time specs. This will also cause return loss to fail at higher frequencies and will degrade the transmit BER performance. Caution should be exercised if a cap is put in either of these locations. If a cap is used, it should almost certainly be less than 22 pF. (6 pF to 12 pF values have been used on past designs with reasonably good success.) These caps are not necessary, unless there is some overshoot in 100 Mbps mode.

***Note:*** It is important to keep the two traces within a differential pair close† to each other. Keeping them close (close should be considered to be less than 0.030 inches between the two traces within a differential pair. 0.007 inch trace-to-trace spacing is recommended) helps to make them more immune to crosstalk and other sources of common-mode noise. This also means lower emissions (i.e. FCC compliance) from the transmit traces and better receive BER for the receive traces.

# 10.10. Power Management Interface

## 10.10.1. SYS_RESET# Usage Model

The System Reset signal (SYS_RESET#) of the ICH4-M can be connected directly to a reset button or any other equivalent driver in the system where the desired effect is to immediately put the system into reset. If an ITP700FLEX debug port is implemented on the system, Intel recommends that the DBR# signal of the ITP interface be connected to SYS_RESET# as well. If SYS_RESET# is implemented, a weak pull-up resistor pulled-up to the 3.3-V standby rail (VccSUS3_3) should also be implemented to ensure that no potential floating inputs to SYS_RESET# cause a system reset. The ICH4-M will debounce signals on this pin (16 ms) and allow the SMBus to go idle before resetting the system. This delay to allow all outstanding SMBus cycles to complete first and to prevent a slave device on the SMBus from “hanging” by resetting in the middle of an SMBus cycle.

## 10.10.2. PWRBTN# Usage Model

The Power Button signal (PWRBTN#) of the ICH4-M can be connected directly to a power button or any other equivalent driver (e.g. power management controller) where the desired effect is to indicate a system request to go to a sleep state (if in a normal operating mode) or to cause a wake event (if in a sleep state already). This signal is internally pulled-up in the ICH4-M to the 3.3-V standby rail (VccSUS3_3) through a weak pull-up resistor (20 k nominal). The ICH4-M has 16 ms of internal debounce logic on this pin.

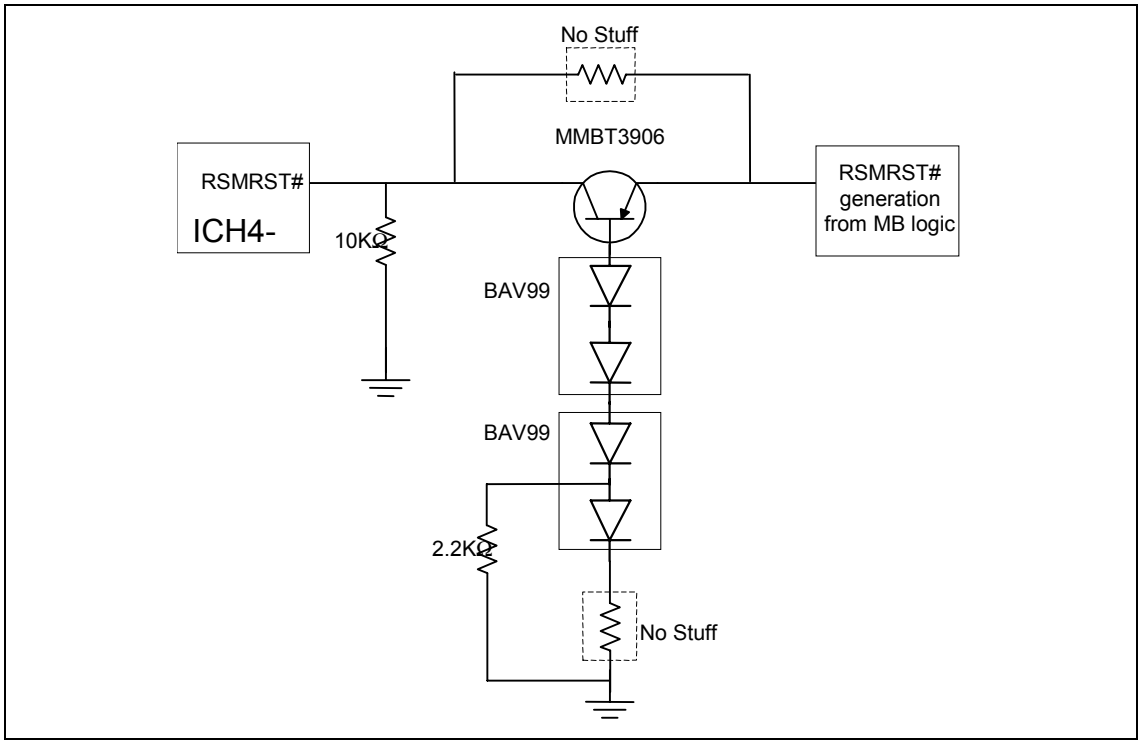
## 10.10.3. Power Well Isolation Control Strap Requirements

The RSMRST# signal of the ICH4-M must transition from 20% signal level to 80% signal level and vice-versa in 50 µs. Slower transitions may result in excessive droop on the VCCRTC node during Sx-to-G3 power state transitions (removal of AC power). Droop on this node can potentially cause the

CMOS to be cleared or corrupted, the RTC to loose time after several AC power cycles, or the intruder bit might assert erroneously.

The circuit shown in Figure 84 can be implemented to control well isolation between the VccSUS3_3 and RTC power-wells in the event that RSMRST# is not being actively asserted during the discharge of the standby rail or does not meet the above rise/fall time.

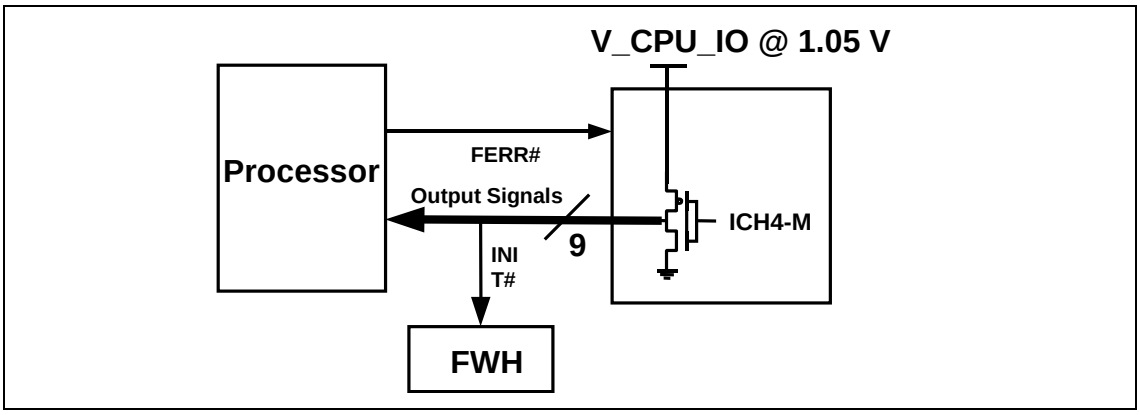
**Figure 84. RTC Power Well Isolation Control**




## 10.11. CPU CMOS Considerations

The Intel 82801DBM ICH4-M has been designed to be voltage compatible with the CMOS signals of the Mobile Intel Pentium 4 processor and Intel Celeron processor. For these processor-based systems, the ICH4-M's V_CPU_IO rail uses the same 1.05-V voltage as the $V_{CCP}$ rails for the processor. It is important to verify that the voltage requirements of all CPU and ICH4-M signals are compatible with the FWH as well. See Section 10.7.3 for FWH details. Figure 85 shows a typical interface between the ICH4-M, CPU, and FWH. See Section 4.3.7.1.6 for recommended topologies and routing guidelines.

**Figure 85. ICH4-M CPU CMOS Signals with CPU and FWH**



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# 11. Platform Clock Routing Guidelines

## 11.1. System Clock Groups

The system clocks are considered a subsystem in themselves. At the center of this subsystem is the Clock Synthesizer/Driver component. Several vendors offer suitable products, as defined in the Intel CK408 Synthesizer/Driver Specification. This device provides the set of clocks required to implement a platform level motherboard solution. Table 74 below provides a breakdown of the various individual clocks.

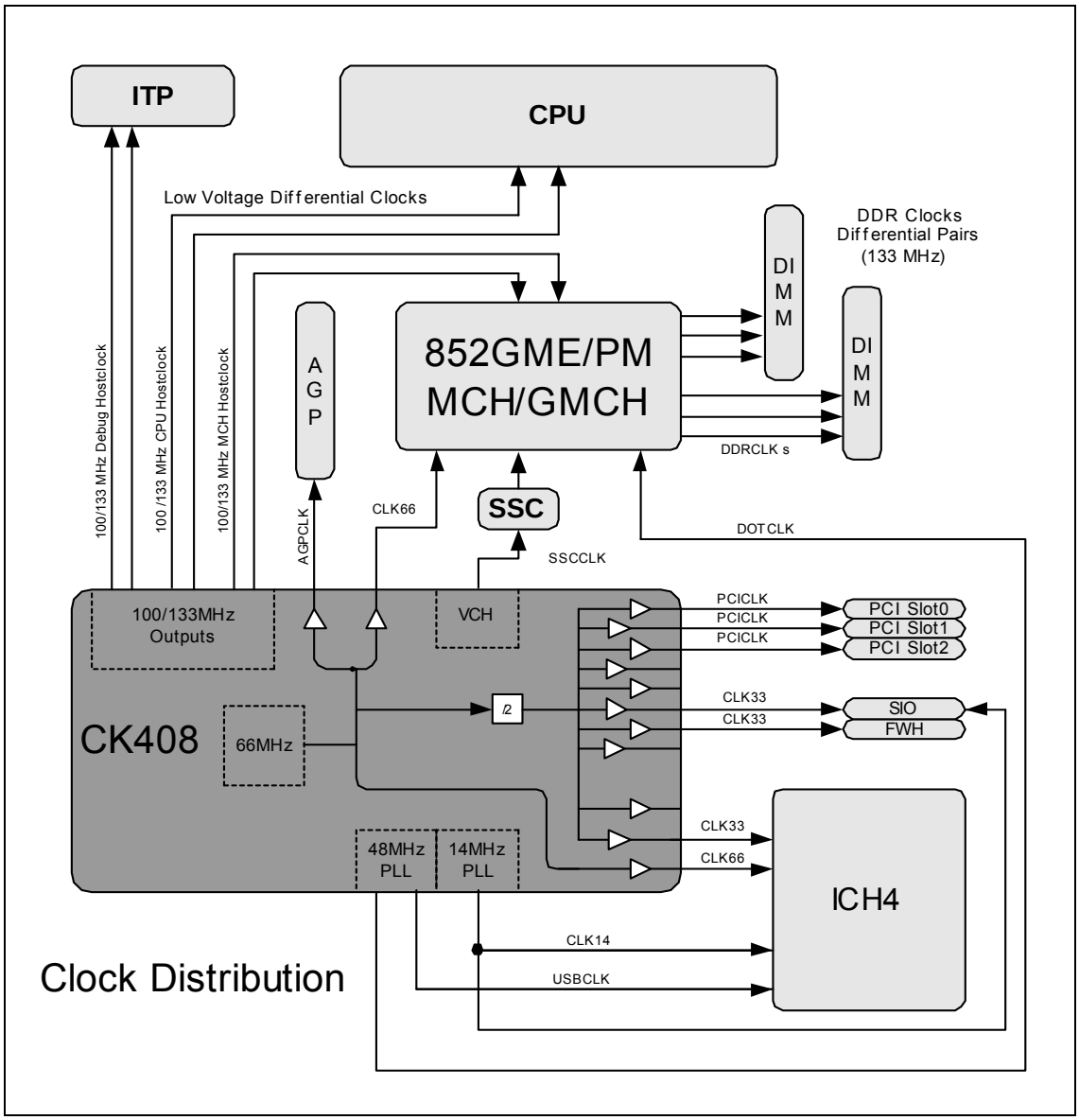
***Note:*** When used in 852GME /852PM platforms, the CK408 is configured in the unbuffered mode and a host clock swing of 710 mV.

**Table 74. Individual Clock Breakdown**

| Clock Group | Frequency | Driver/Pin | Receiver/s | Comments |
|---|---|---|---|---|
| HOST_CLK | 100/133 MHz | CK408<br>CPU[2:0] | CPU<br>MCH<br>Debug Port | Length matched<br>Differential signaling |
| CLK66 | 66 MHz | CK408<br>3V66[5:0] | MCH<br>ICH4-M | Length matched |
| AGPCLK | 66 MHz | CK408<br>3V66[5:0] | AGP Connector<br>AGP Controller | Length matched to CLK66 *<br>* CLK66 length minus 4.0” |
| CLK33 | 33 MHz | CK408<br>PCIF[2:0] | ICH4-M | Length matched to CLK66<br>Synchronous but not edge aligned with CLK66<br>Phase delay of 1.5 ns to 3.5 ns |
| | 33 MHz | CK408<br>PCI[6:0] | SIO<br>FWH | |
| PCICLK<br>(Expansion) | 33 MHz | CK408<br>PCI[6:0] | PCI Conn #1<br>PCI Conn #2<br>PCI Conn #3 | Length matched to CLK33 *<br>* CLK33 length minus 2.5” |
| CLK14 | 14 MHz | CK408<br>REF0 | ICH4<br>SIO | Independent clock |
| DOTCLK | 48 MHz | CK408<br>48MHz | MCH | Independent clock |
| SSCCLK | 48/66 MHz | CK408<br>VCH | MCH | Independent clock |
| USBCLK | 48 MHz | CK408<br>48 MHz | ICH4-M | Independent clock |

Figure 86 depicts the system clock subsystem including the clock generator, major platform components, and all the related clock interconnects.

**Figure 86. Clock Distribution Diagram**



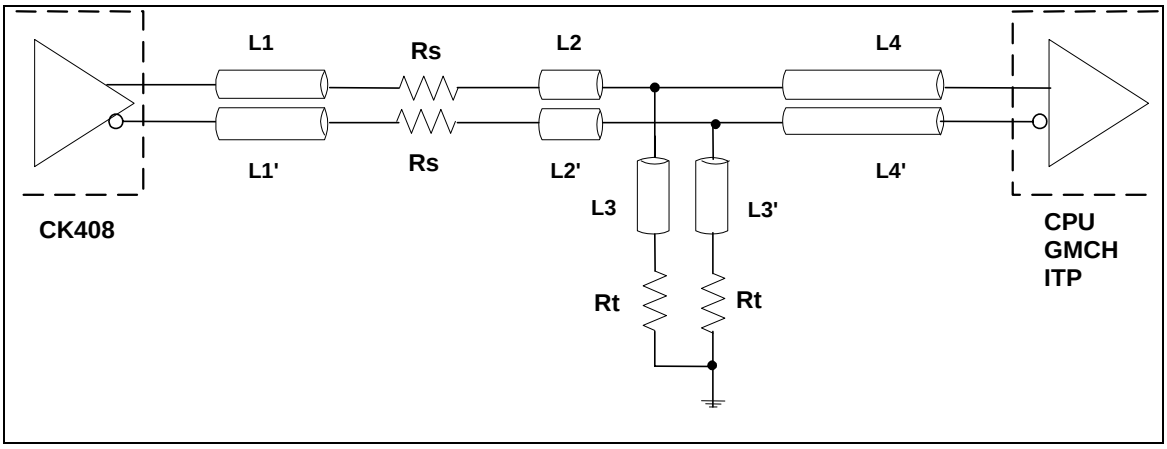
## 11.2. Clock Group Topologies and Routing Constraints

The topology diagrams and routing constraint tables provided on the following pages define the recommended topology and routing rules for each of the platform level clocks. These topologies and rules have been simulated and verified to produce the required waveform integrity and timing characteristics for reliable platform operation.

### 11.2.1. Host Clock Group

The host clocks are routed point to point as closely coupled differential pairs on the motherboard, with dedicated buffers for each of the three loads. These clocks utilize a Source Shunt Termination scheme as shown Figure 87.

**Figure 87. Source Shunt Termination Topology**




The clock driver differential bus output structure is a “Current Mode Current Steering” output that develops a clock signal by alternately steering a programmable constant current to the external termination resistors Rt. The resulting amplitude is determined by multiplying IOUT by the value of Rt. The current IOUT is programmable by a resistor and an internal multiplication factor so the amplitude of the clock signal can be adjusted for different values of Rt to match impedances or to accommodate future load requirements.

The recommended termination for the differential bus clock is a “Source Shunt termination.” Parallel Rt resistors perform a dual function, converting the current output of the clock driver to a voltage and matching the driver output impedance to the transmission line. The series resistors Rs provide isolation from the clock driver’s output parasitics, which would otherwise appear in parallel with the termination resistor Rt.

The recommended value for Rt is a 49.9 ohm ± 1% resistor. The tight tolerance is required to minimize crossing voltage variance. The recommended value for Rs is 33 ± 5%. Simulations have shown that Rs values above 33 provide no benefit to signal integrity but only degrade the edge rate.

The MULT0 pin (CK408 pin #43) should be pulled-up through a 10 k to VCC – setting the multiplication factor to 6. The IREF pin (CK408 pin #42) should be tied to ground through a 475 ± 1 % resistor – making the IREF 2.32 mA.

### Table 75. Host Clock Group Routing Constraints

| Parameter | Definition |
|---|---|
| Class Name | HOST_CLK |
| Class Type | Individual Differential Pairs |
| Topology | Differential Source Shunt Terminated |
| Reference Plane | Ground Referenced (contiguous over length) |
| Single Ended Trace Impedance ( Zo ) | 55 ohms ± 15% |
| Differential Mode Impedance (Zdiff) | 100 ohms ± 15% |
| Nominal Inner Layer Trace Width | 4.0 mils |
| Nominal Inner Layer Pair Spacing (edge to edge)<br>(except as allowed below) | 4.0 mils |
| Nominal Outer Layer Trace Width | 5.0 mils (pin escapes only) |
| Nominal Outer Layer Pair Spacing (edge to edge)<br>(except as allowed below) | 5.0 mils |
| Minimum Spacing to Other Signals | 25 mils |
| Serpentine Spacing | 25 mils |
| Maximum Via Count | 5 (per side) |
| Series Termination Resistor Value | 33 ohms ± 5% |
| Shunt Termination Resistor Value | 49.9 ohms ± 1% |
| Trace Length Limits – L1 & L1’ | Up to 500mils |
| Trace Length Limits – L2 & L2’ | Up to 200 mils |
| Trace Length Limits – L3 & L3’ | Up to 500 mils |
| Trace Length Limits – L4 & L4’ | 2.0” to 8.0” |
| Total Length Range– L1 + L2 + L4 | 2.0” to 8.5” |
| Length Matching Required | Yes (Pin to Pad) |
| Clk to Clk# Length Matching | ± 10 mils (per segment)<br>± 10 mils (overall) |
| Clock to Clock Length Matching | CPU HCLK = ITP HCLK = (MCH HCLK – 0.25”)<br>Tolerance = ± 20 mils |
| Breakout Region Exceptions | No breakout exceptions allowed |

**NOTES:**
1. Differential pairs should be routed as a closely coupled side-by-side pair on a single layer over their entire length.
2. To minimize skew, Intel recommends that all clocks be routed on a single layer. If clock pairs are to be routed on multiple layers, the routed length on each layer should be equalized across all clock pairs.

3. As specified in the table above, the nominal length of the clock pair terminating at the 852GME GMCH should be routed 0.25 inches shorter than the other two clock pairs. This is to compensate for a difference in package length between the CPU and the GMCH.
4. A trace length offset (depends on CK408 vendor clock skew) between CLK66 going to the GMCH (GCLKIN) and HCLK going to the GMCH (BCLK) is recommended in order to prevent the CLK66 rising edge from occurring within the +/- 350ps keepout area on either side of the HCLK edge.

#### 11.2.1.1. Host Clock Group General Routing Guidelines

The general guidelines are as follows:

When routing the 100-MHz differential clocks, do not split up the two halves of a differential clock pair between layers and route to all agents on the same physical routing layer referenced to ground.

If a layer transition is required, make sure that the skew induced by the vias used to transition between routing layers is compensated in the traces to other agents.

Do not place vias between adjacent complementary clock traces and avoid differential vias. Vias placed in one half of a differential pair must be matched by a via in the other half. Differential vias can be placed within length L1, between clock driver and Rs, if needed to shorten length L1.

#### 11.2.1.2. Clock to Clock Length Matching and Compensation

The HCLK pairs to the CPU and GMCH should be matched as close as possible in total length from CK408 pin to the die-pad of the receiving device. In addition, the L1/L1' segments of all three clock pairs should be length matched to within ± 10 mils. Pair to pair overall length matching requires knowledge of the package lengths of various CPUs, and the GMCH, as well as the effective length of the CPU socket/interposer if used. This information is provided in table below and Table 76.

Once routing lengths are defined for the CPU and GMCH, match the motherboard length of the ITP clock pair to the motherboard length of the CPU clock pair.

| Parameter | Length |
|---|---|
| Mobile Intel Pentium 4 processor, Intel Celeron processor package Length | 485 mils |
| Intel 852GME/852GMV/852PMChipset GMCH package length | 1142 mils |
| CPU Socket Equivalent Length | 157 mils |

#### 11.2.1.3. EMI Constraints

Clocks are a significant contributor to EMI and should be treated with care. The following recommendations can aid in EMI reduction:

Maintain uniform spacing between the two halves of differential clocks.

Route clocks on physical layer adjacent to the VSS reference plane only.

## 11.2.2. CLK66 Clock Group

The 66-MHz clocks are series terminated and routed point to point on the motherboard, with dedicated buffers for each of the loads. These clocks are all length tuned to match each other and the CLK33 clocks.

**Figure 88. CLK66 Clock Group Topology**

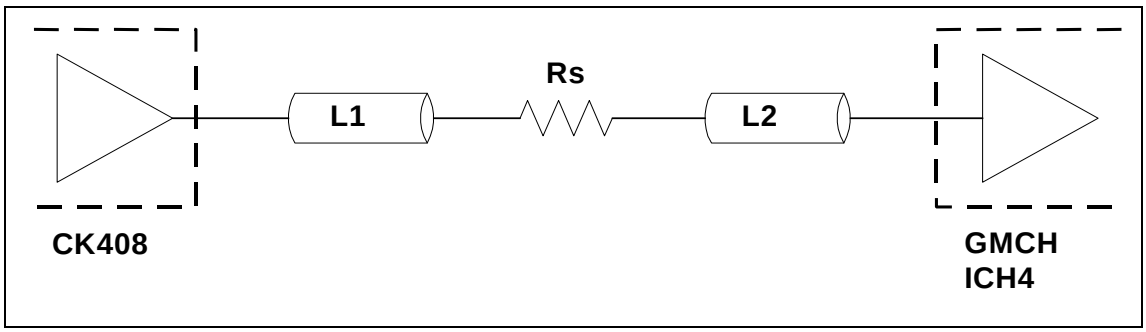



**Table 76. CLK66 Clock Group Routing Constraints**

| Parameter | Definition |
|---|---|
| Class Name | CLK66 |
| Class Type | Individual Nets |
| Topology | Series Terminated Point to Point |
| Reference Plane | Ground Referenced |
| Single Ended Trace Impedance ( Zo ) | 55 ohms ± 15% |
| Nominal Inner Layer Trace Width | 4.0 mils |
| Nominal Outer Layer Trace Width | 5.0 mils (pin escapes only) |
| Minimum Spacing (see exceptions below) | 20 mils |
| Serpentine Spacing | 20 mils |
| Maximum Via Count | 4 (per side) |
| Series Termination Resistor Value | 33 ohms ± 5 % |
| Trace Length Limits – L1 | Up to 500 mils (breakout segment) |
| Trace Length Limits – L2 | 4.0” to 8.5” |
| Total Length Range – L1 + L2 | 4.0” to 9.0” |
| Length Matching Required | Yes (Pin to Pin) |
| Clock to Clock Length Matching | ± 100 mils CLK66 to CLK66 |
| Breakout Region Exceptions. (Reduced spacing for GMCH & ICH breakout region) | 5 mil trace with 5 mil space on outers<br>4 mil trace with 4 mil space in inners<br>Maximum breakout length is 0.3” |

**NOTES:**

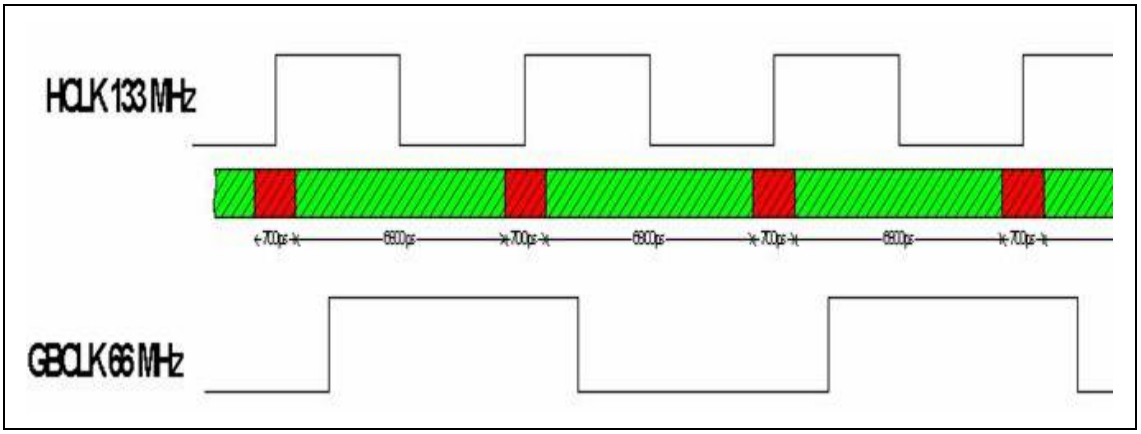
1. The overall length of CLK66 is considered the reference length for all other clocks, except USBCLK and CLK14. The length of this clock should be set within the range and then used as the basis for defining the length of all other length matched clocks.

2. A trace length offset (depends on CK408 vendor clock skew) between CLK66 going to the GMCH (GCLKIN) and HCLK going to the GMCH (BCLK) is recommended in order to prevent the CLK66 rising edge from occurring within the +/- 350 ps keepout area on either side of the HCLK edge

## 11.2.3. Host Clock to CLK66 Routing Recommendations

The rising edge of the HCLK (BCLK) input must either lead or lag the rising edge of CLK66 (GCLKIN) by more than 350 ps at the input balls of the GMCH as measured at the 50% point of each rising edge. Refer to the following figure for details:

**Figure 89. BCLK to GCLKIN Timing Requirement**




When assessing whether a system design meets the required BCLK/GCLKIN phase relationship, the following factors should be taken into account:

Selected clock synthesizer chip's worst case (minimum) phase relationship between CLK66 (GCLKIN) and HCLKx (BCLK) rising edges. This includes the following clock timing parameters:

Min phase offset. Since the CK408 spec does not specify the phase offset between CLK66 and CPUx, the actual worst case (min) offset must be determined by consulting with the selected clock synthesizer chip's vendor.

Cycle-to-cycle jitter on each clock output. Max jitter is specified by the CK408 clock spec, but may be less than the max specified for any particular CK408 compatible clock synthesizer chip.

Trace length difference between BCLK and GCLKIN routing.

Board manufacturing variations affecting signal delay across clock traces.

All relevant variables should be evaluated over the system's full specified operating temperature range.

## 11.2.4. CLK33 Clock Group

The 33-MHz clocks are series terminated and routed point to point on the motherboard with dedicated buffers for each of the loads. These clocks are length tuned to match the CLK66 clocks; however, they are out of phase due to an internal phase delay in the CK408.

**Figure 90. CLK33 Group Topology**

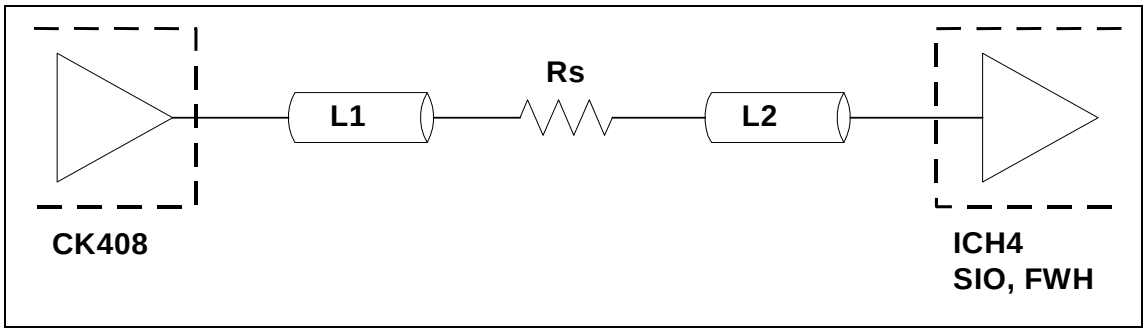



**Table 77. CLK33 Clock Group Routing Constraints**

| Parameter | Definition |
|---|---|
| Class Name | CLK33 |
| Class Type | Individual Nets |
| Topology | Series Terminated Point to Point |
| Reference Plane | Ground Referenced |
| Single Ended Trace Impedance ( Zo ) | 55 ohms ± 15% |
| Nominal Inner Layer Trace Width | 4.0 mils |
| Nominal Outer Layer Trace Width | 5.0 mils (pin escapes only) |
| Minimum Spacing (see exceptions below) | 20 mils |
| Serpentine Spacing | 20 mils |
| Maximum Via Count | 4 |
| Series Termination Resistor Value | 33 ohms ± 5 % |
| Trace Length Limits – L1 | Up to 500mils |
| Trace Length Limits – L2 | 4.0” to 8.5” |
| Total Length Range – L1 + L2 | CLK66 Length |
| Length Matching Required | Yes (Pin to Pin) |
| Clock to Clock Matching | ± 100 mils<br>CLK33 to CLK33 to CLK66 |
| Breakout Region Exceptions | 5 mil trace with 5 mil space on outers<br>4 mil trace with 4 mil space in inners<br>Maximum breakout length is 0.3” |

## 11.2.5. PCI Clock Group

The PCI clocks are series terminated and routed point to point as on the motherboard between the CK408 and the PCI connectors with dedicated buffers for of the three slots. These clocks are synchronous to the CLK33 clocks and are length tuned to compensate for the segment on the PCI daughtercard.

**Figure 91. PCI Clock Group Topology**

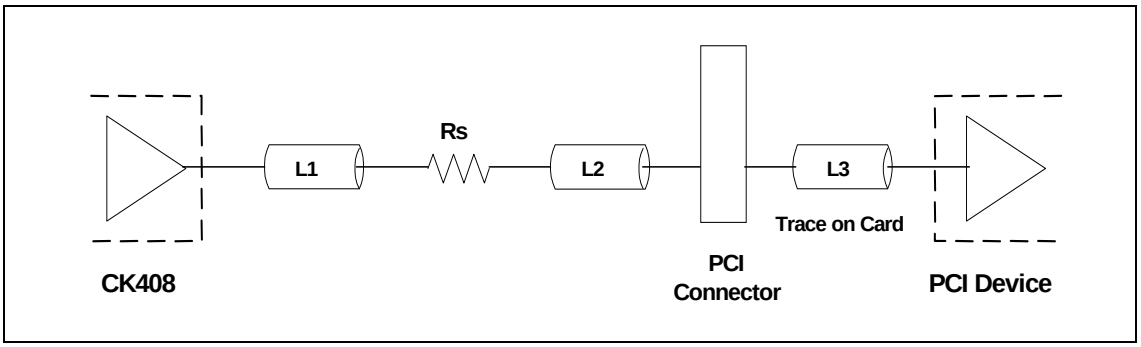



**Table 78. PCICLK Clock Group Routing Constraints**

| Parameter | Definition |
|---|---|
| Class Name | PCICLK |
| Class Type | Individual Nets |
| Topology | Series Terminated Point to Point |
| Reference Plane | Ground Referenced |
| Single Ended Trace Impedance ( Zo ) | 55 ohms ± 15% |
| Nominal Inner Layer Trace Width | 4.0 mils |
| Nominal Outer Layer Trace Width | 5.0 mils (pin escapes only) |
| Minimum Spacing (see exceptions below) | 20 mils |
| Serpentine Spacing | 20 mils |
| Maximum Via Count | 4 |
| Series Termination Resistor Value | 33 ohms ± 5 % |
| Trace Length Limits – L1 | Up to 500 mils (breakout segment) |
| Trace Length Limits – L2 | 1.5” to 8.0” |
| Trace Length Limits – L3 | 2.5” (as per PCI specification) |
| Total Length Range – L1 + L2 + L3 | CLK33 – 2.5” (for nominal matching) |
| Length Matching Required | Yes (Pin to Pin) |
| Clock to Clock Length Matching | ± 2.0” PCICLK to PCICLK to (CLK33 – 2.5”) |
| Breakout Region Exceptions | 5 mil trace with 5 mil space on outers<br>4 mil trace with 4 mil space in inners<br>Maximum breakout length is 0.3” |

## 11.2.6. CLK14 Clock Group

The 14-MHz clocks are series terminated and routed point to point on the motherboard. A single clock output is shared between the two loads. These clocks are length tuned to each other but are not synchronous with any other clocks.

**Figure 92. CLK14 Clock Group Topology**

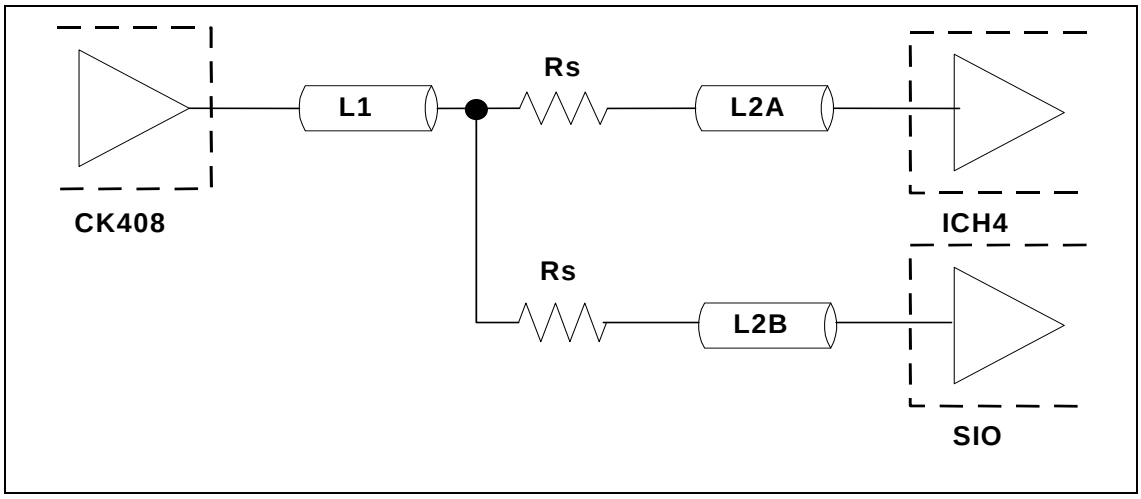



**Table 79. CLK14 Clock Group Routing Constraints**

| Parameter | Definition |
|---|---|
| Class Name | CLK14 |
| Class Type | Individual Nets |
| Topology | Dual Series Terminated Point to Point |
| Reference Plane | Ground Referenced |
| Single Ended Trace Impedance ( Zo ) | 55 ohms ± 15% |
| Nominal Inner Layer Trace Width | 4.0 mils |
| Nominal Outer Layer Trace Width | 5.0 mils (pin escapes only) |
| Minimum Spacing (see exceptions below) | 20 mils |
| Serpentine Spacing | 20 mils |
| Maximum Via Count | 4 (per driver/receiver path) |
| Series Termination Resistor Value | 33 ohms ± 5 % |
| Trace Length Limits – L1 | Up to 500 mils |
| Trace Length Limits – L2A, L2B | 2.0” to 8.5” |
| Total Length Range – L1 + L2A & L1 + L2B | 2.0” to 9.0” |
| Length Matching Required | Yes (Pin to Pin) |
| Clock to Clock Length Matching | ± 500 mils<br>CLK14A to CLK14B |
| Breakout Region Exceptions | 5 mil trace with 5 mil space on outers<br>4 mil trace with 4 mil space in inners<br>Maximum breakout length is 0.3” |

## 11.2.7. DOTCLK Clock Group

The 48-MHz DOTCLK is series terminated and routed point to point on the motherboard. This clock operates independently and is not length tuned to any other clock.

**Figure 93. DOTCLK Clock Topology**

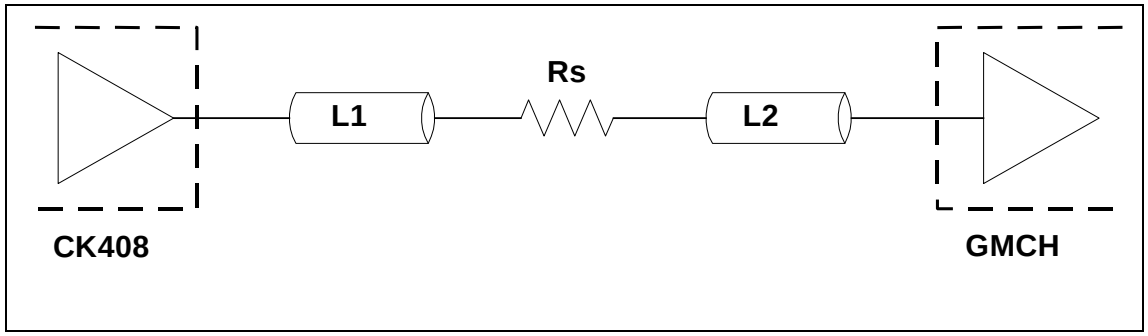



**Table 80. DOTCLK Clock Routing Constraints**

| Parameter | Definition |
|---|---|
| Class Name | DOTCLK |
| Class Type | Individual Net |
| Topology | Series Terminated Point to Point |
| Reference Plane | Ground Referenced |
| Single Ended Trace Impedance ( Zo ) | 55 ohms ± 15% |
| Nominal Inner Layer Trace Width | 4.0 mils |
| Nominal Outer Layer Trace Width | 5.0 mils (pin escapes only) |
| Minimum Spacing (see exceptions below) | 25 mils |
| Maximum Via Count | 4 |
| Series Termination Resistor Value | 33 ohms ± 5 % |
| Trace Length Limits – L1 | Up to 500 mils |
| Trace Length Limits – L2 | 2.0” to 8.0” |
| Total Length Range – L1 + L2 | 2.0” to 8.5” |
| Length Matching Required | No |
| Breakout Exceptions | 5 mil trace with 5 mil space on outers<br>4 mil trace with 4 mil space in inners<br>Maximum breakout length is 0.3” |

**NOTES:**

1. The DOTCLK is used internally by the GMCH to generate the pixel clock and must exhibit very low jitter. Care should be taken to avoid routing through noisy areas and spacing rules should be observed. Guard traces may be employed if necessary with ground stake vias on no less than 0.5-inch intervals.
2. If external graphics is only supported on the platform then dotclock does not need to be connected to GMCH.

## 11.2.8. SSCCLK Clock Group

The 48/66 MHz SSCCLK operates independently and is not length tuned to any other clock. This clock employs a spread-spectrum device in its path to reduce EMI. The overall clock path is divided into two segments as shown below with each segment series terminated and routed point to point.

**Figure 94. SSCCLK Clock Topology**

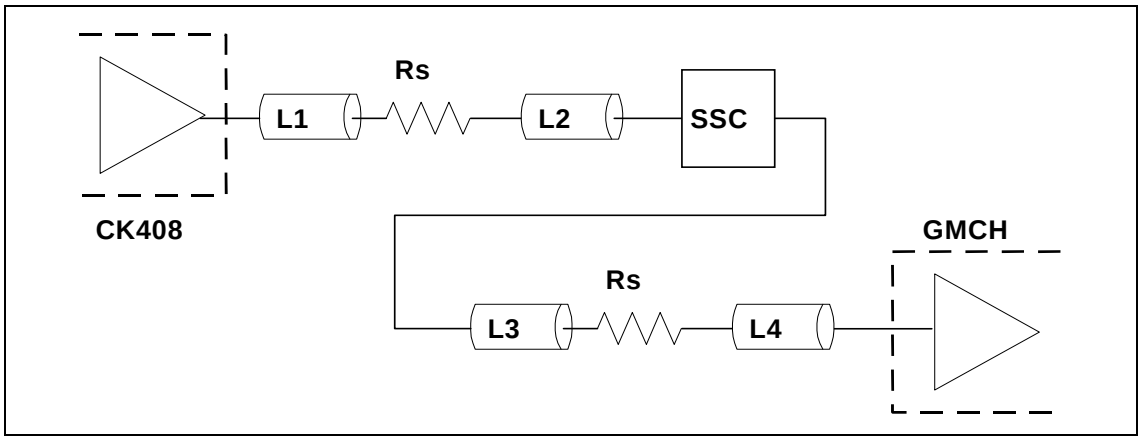



**Table 81. SSCCLK Clock Routing Constraints**

| Parameter | Definition |
|---|---|
| Class Name | SSCCLK |
| Class Type | Individual Net |
| Topology | Series Terminated Point to Point |
| Reference Plane | Ground Referenced |
| Single Ended Trace Impedance ( Zo ) | 55 ohms ± 15% |
| Nominal Inner Layer Trace Width | 4.0 mils |
| Nominal Outer Layer Trace Width | 5.0 mils (pin escapes only) |
| Minimum Spacing (see exceptions below) | 20 mils |
| Maximum Via Count | 4 (per driver/receiver path) |
| Series Termination Resistor Value | 33 ohms ± 5 % |
| Trace Length Limits – L1 | Up to 500 mils |
| Trace Length Limits – L2 | 1.0” to 4.0” |
| Trace Length Limits – L3 | Up to 500 mils |
| Trace Length Limits – L4 | 1.0” to 7.0” |
| Total Length Range – L1 + L2 + L3 + L4 | 3.0” to 8.5” |
| Length Matching Required | No |
| Breakout Exceptions | 5 mil trace with 5 mil space on outers<br>4 mil trace with 4 mil space in inners<br>Maximum breakout length is 0.3” |

**NOTE:** If external graphics is only supported on the platform then dotclock does not need to be connected to GMCH.

## 11.2.9. USBCLK Clock Group

The 48-MHz USBCLK is series terminated and routed point to point on the motherboard. This clock operates independently and is not length tuned to any other clock.

**Figure 95. USBCLK Clock Topology**

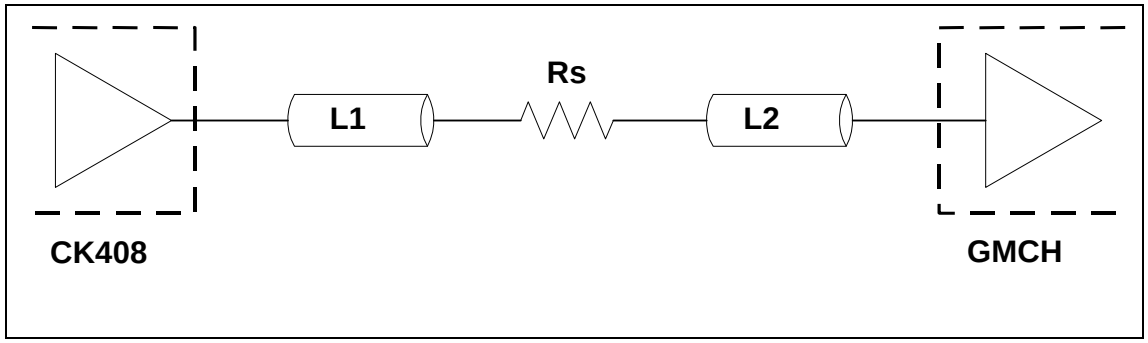



**Table 82. USBCLK Clock Routing Constraints**

| Parameter | Definition |
|---|---|
| Class Name | USBCLK |
| Class Type | Individual Net |
| Topology | Series Terminated Point to Point |
| Reference Plane | Ground Referenced |
| Single Ended Trace Impedance ( Zo ) | 55 ohms ± 15% |
| Nominal Inner Layer Trace Width | 4.0 mils |
| Nominal Outer Layer Trace Width | 5.0 mils (pin escapes only) |
| Minimum Spacing (see exceptions below) | 20 mils |
| Maximum Via Count | 4 |
| Series Termination Resistor Value | 33 ohms ± 5 % |
| Trace Length Limits – L1 | Up to 500 mils |
| Trace Length Limits – L2 | 3.0” to 12.0” |
| Total Length Range – L1 + L2 | 3.0” to 12.5” |
| Length Matching Required | No |
| Breakout Exceptions | 5 mil trace with 5 mil space on outers<br>4 mil trace with 4 mil space in inners<br>Maximum breakout length is 0.3” |

# 11.3. CK-408 Clock Power Supply Decoupling

See Section 12.7.8 for details.

## 11.4. CK-408 PWRDWN# Signal Connections

The PWRDWN# input of the CK-408 clock chip is **required** to be driven by **both** the SLP_S1# and SLP_S3# signals from the ICH4-M, i.e. the PWRDWN# pin of the CK-408 should be driven by the output of the logical AND of the SLP_S1# and SLP_S3# signals. This configuration best allows CPU[2:0] to be tri-stated during S1-M or lower (numerically higher) states.

For systems that do not support S1M but do support the S3 state, the PWRDWN# input of the CK-408 clock chip should be connected to the SLP_S3# output of the ICH4-M. It is **not** recommended that PWRDWN# be pulled-up to the CK-408's 3.3-V power supply if the S3 state is the second highest, power consuming state supported by the platform (i.e. S1M and S2 not supported). The advantage of using SLP_S3# rather than the 3.3-V supply to qualify PWRDWN# is that it reduces the likelihood of the CK-408 clocks driving into unpowered components and potentially damaging the clock input buffers. Also SLP_S3# can help reduce power consumption because it will be asserted before the 3.3-V supply will be shut off, thus minimizing the amount of time that the clocks will be left toggling.

# 12. Platform Power Delivery Guidelines

## 12.1. Definitions

S0 / Full-On operation. During Full-On operation, all components on the motherboard are powered and the system is fully functional.

S1-M / Power-On-Suspend (POS, Mobile). In the mobile implementation of the Power-On-Suspend state, the outputs of the clock chip stopped in order to save power. All components remain powered but may or may not be in a low power state.

S3 / Suspend-To-RAM (STR). In the STR state, the system state is stored in main memory and all unnecessary system logic is turned off. Only main memory and logic required to wake the system remain powered.

S4 / Suspend-To-Disk (STD). In the STD state, the system state is stored in non-volatile secondary storage (e.g. a hard disk) and all unnecessary system logic is turned off. Only logic required to wake the system remain powered. Standby power rails may or may not be powered depending on system design and the presence of AC or battery power.

S5 / Soft-Off. The Soft-Off state corresponds to the G2 state. Restart is only possible with the power button.

Full-Power operation. During Full-Power operation, all components remain powered. Full-power operation includes both Full-On and the S1M (CPU Stop-Grant state).

Suspend operation. During suspend operation, power is removed from some components on the motherboard. 852GME chipset-based systems can be designed to support a number of suspend states such as Power-On-Suspend (S1M), Suspend-to-RAM (S3), Suspend-to-Disk (S4), and Soft-Off (S5).

Core power rail. A power rail that is only on during full-power operation. These power rails are on when the PSON signal is asserted to the ATX power supply.

Standby power rail. A power rail that in on during suspend operation (these rails are also on during full-power operation). These rails are on at all times (when the power supply is plugged into AC power). The only standby power rail that is distributed directly from the ATX power supply is: 5 $V_{SB}$ (5 V Standby). There are other standby rails that are created with voltage regulators on the motherboard.

Derived power rail. A derived power rail is any power rail that is generated from another power rail using an on-board voltage regulator. For example, 3.3 $V_{SB}$ is usually derived (on the motherboard) from 5 $V_{SB}$ using a voltage regulator.

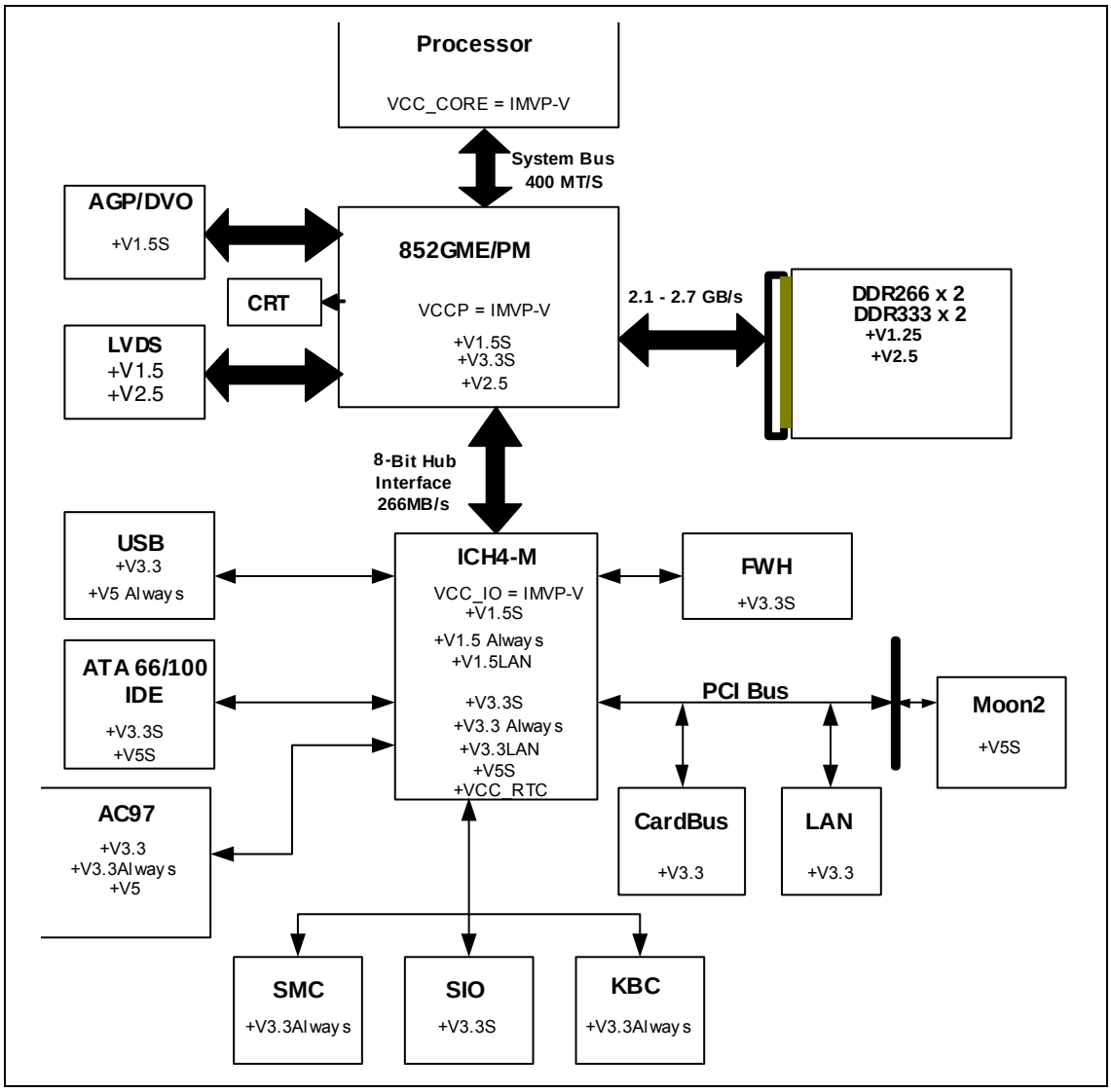
Dual power rail. A dual power rail is derived from different rails at different times (depending on the power state of the system). Usually, a dual power rail is derived from a standby supply during suspend operation and derived from a core supply during full-power operation. Note that the voltage on a dual power rail may be misleading.

## 12.2. Platform Power Requirements

Figure 96 below shows the power delivery architecture for an example 852GME/852GMV/852PMchipset platform. This power delivery architecture supports the "Instantly Available PC Design Guidelines" via the S3 system state. To ensure that enough power is available during S3, a thorough power budget should be completed. The power requirements should include each device's power requirements, both in *suspend* and in *Full-On*. The power requirements should be compared against the power budget supplied by the power supply. Due to the requirements of main memory and PCI 3.3 Vaux (and possibly other devices in the system), it is necessary to create a *dual* power rail.

The solutions given in this document are only examples. There are many power distribution methods that achieve similar results. It is critical, when deviating from these examples, to consider the effect of the change.

**Figure 96. Platform Power Delivery Architectural Block Diagram**



# 12.3. Voltage Supply

## 12.3.1. Power Management States

**Table 83. Power Management States**

| Signal | SLP_S1# | SLP_S3# | SLP_S4# | SLP_S5# | +V*ALW | +V* | +V*S | Clocks |
|---|---|---|---|---|---|---|---|---|
| FULL ON | HIGH | HIGH | HIGH | HIGH | ON | ON | ON | ON |
| S1M (POS) | LOW | HIGH | HIGH | HIGH | ON | ON | ON | LOW |
| S3 (STR) | LOW | LOW | HIGH | HIGH | ON | ON/OFF | OFF | OFF |
| S4 (STD) | LOW | LOW | LOW | HIGH | ON | ON/OFF | OFF | OFF |
| S5 (Soft Off) | LOW | LOW | LOW | LOW | ON | ON/OFF | OFF | OFF |

## 12.3.2. Power Supply Rail Descriptions

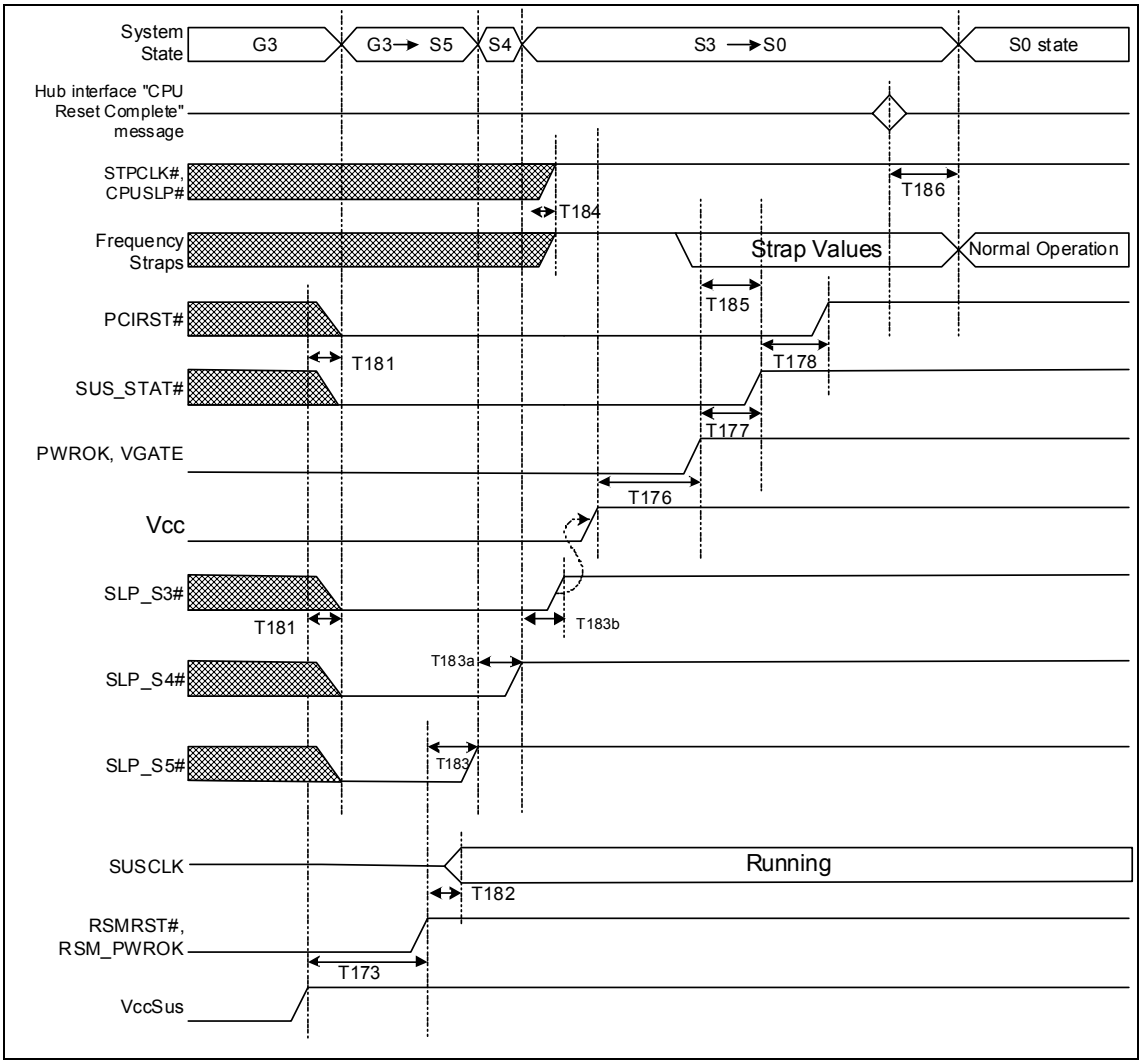
**Table 84. Power Supply Rail Descriptions**

| Signal Names | Voltage (V) | Current (A) | Tolerance | Enable | Description |
|---|---|---|---|---|---|
| +V1_25 | 1.25 | 0.01 | ± 3.2% | SLP_S4# - HIGH | DDR Termination |
| +V1_5 | 1.5 | 0.03 | ± 5% | SLP_S4# - HIGH | LAN logic |
| +V1_5S | 1.5 | 1.35 | ± 5% | SLP_S3# - HIGH | GMCH DVO-Core, DLVDS, DAC, ALVD, ICH4-M core, VCCHL |
| +V1_5ALWAYS | 1.5 | 0.1 | ± 5% | +V3ALWAYS | ICH4-M Resume |
| +V2_5 | 2.5 | 8.12 | ± 5% | SLP_S4# - HIGH | GMCH DDR I/O, LVDS<br>DDR SO-DIMM |
| +V3ALWAYS | 3.3 | 0.4 | ± 5% | +VDC_ON | ICH4-M Resume, SMC/KBC, AC'97 |
| +V3 | 3.3 | 0.9 | ± 5% | SLP_S5# - HIGH | ICH4-M resume I/O & LAN I/O, Cardbus, AC'97, RS232 |
| +V3S | 3.3 | 7.0 | ± 5% | SLP_S3# - HIGH | ICH4-M I/O, CK-408, FWH, SIO, AC'97, IDE |
| +V5 | 5 | 9.0 | ± 5% | SLP_S5# - HIGH | USB, AC'97, HDD, DVD, CD-ROM, +V2_5, +V1_25 |
| +V5S | 5 | 1.0 | ± 5% | SLP_S3# - HIGH | ICH4-M, MSE/KBD, FDD, IDE |
| +V5ALWAYS | 5 | 3.0 | ± 5% | +VDC | USB Supply |
| +V12S | 12 | 0.2 | ± 5% | SLP_S3# - HIGH | Cardbus |
| +VCC_CORE | IMVP-V | TBD | IMVP-V | +VCC_VID -HIGH | See IMVP-V Design Guide for detail |
| +VCCP | IMVP-V | TBD | IMVP-V | +VCC_VID | See IMVP-V Design Guide for detail |
| +VCC_VID | 1.2 | TBD | IMVP-V | VR_ON | See IMVP-V Design Guide for detail |

## 12.4. 852GME/852GMV/852PMGMCH/ICH4-M Platform Power-Up Sequence

Figure 97 describes the power-on timing sequence for a GMCH / ICH4-M-based platform.

**Figure 97. GMCH / ICH4-M Platform Power-Up Sequence**



### Table 85. Timing Sequence Parameters for Figure 97

| Symbol | Description | Min | Max | Units | Notes | Fig |
|---|---|---|---|---|---|---|
| T173 | VccSus supplies active to RSMRST# inactive | 5 | - | ms | | Figure 97 |
| T175b | VccLAN supplies active to LAN_RST# active | 10 | - | ms | | Figure 97 |
| T176 | Vcc supplies active to PWROK, VGATE active | 10 | - | ms | | Figure 97 |
| T177 | PWROK and VGATE active and SYS_RESET# inactive to SUS_STAT# inactive | 32 | 38 | RTCCLK | | Figure 97 |
| T178 | SUS_STAT# inactive to PCIRST# inactive | 1 | 3 | RTCCLK | | Figure 97 |
| T181 | VccSus active to SLP_S5#, SUS_STAT# and PCIRST# active | | 50 | ns | | Figure 97 |
| T182/T183 | RSMRST# inactive to SUSCLK running, SLP_S5# inactive | | 110 | ms | 1 | Figure 97 |
| T183a | SLP_S5# inactive to SLP_S4# inactive | 1 | 2 | RTCCLK | | Figure 97 |
| T183b | SLP_S4# inactive to SLP_S3# inactive | 1 | 2 | RTCCLK | | Figure 97 |
| T184 | Vcc active to STPCLK#, CPUSLP#, STP_CPU#, STP_PCI#, SLP_S1#, C3_STAT# inactive, and CPU Frequency Strap signals high | | 50 | ns | | Figure 97 |
| T185 | PWROK and VGATE active and SYS_RESET# inactive to SUS_STAT# inactive and CPU Frequency Straps latched to strap values | 32 | 38 | RTCCLK | 2 | Figure 97 |
| T186 | CPU Reset Complete to Frequency Straps signals unlatched from strap values | 7 | 9 | CLK66 | 3 | Figure 97 |

**NOTES:**
1. If there is no RTC battery in the system, so VccRTC and the VccSus supplies come up together, the delay from RTCRST# and the RSMRST# inactive to SUSCLK toggling may be as much as 1000 ms.
2. These transitions are clocked off the internal RTC. 1 RTC clock is approximately 32 µs.
3. This transition is clocked off the 66-MHz CLK66. 1 CLK66 is approximately 15 ns.

**Figure 98. Power On Sequencing Timing Diagram (VR Circuitry)**

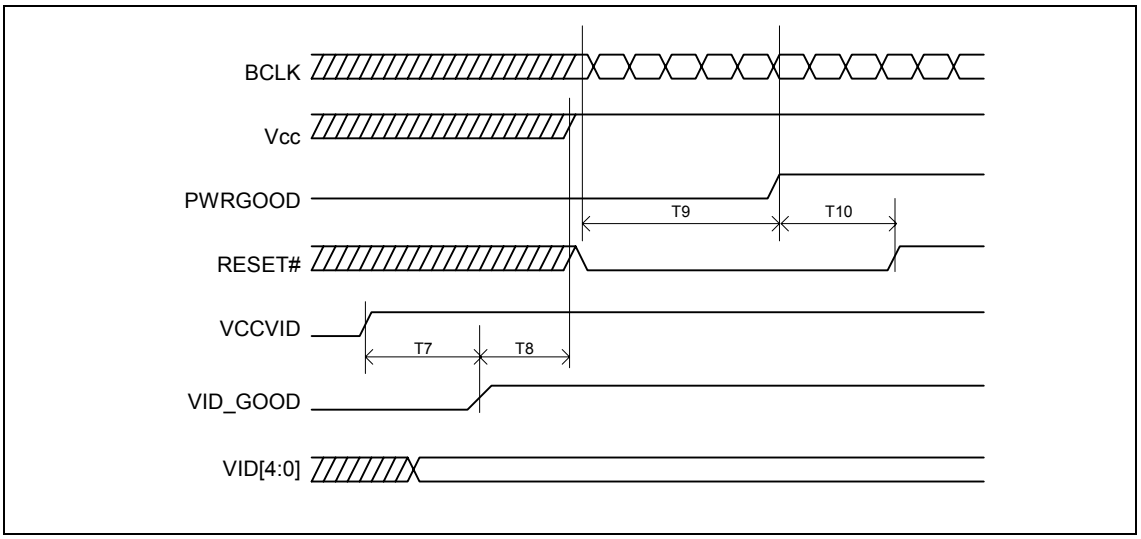



**Table 86. Timing Sequence Parameters for Figure 98**

| Sym | Description | Min | Max | Units | Notes | Fig |
|---|---|---|---|---|---|---|
| T7 | VCCVID > 1V to VID_GOOD high | 1 | | us | | Figure 98 |
| T8 | VID_GOOD to Vcc valid maximum time | | 50 | ms | | Figure 98 |
| T9 | PWRGOOD inactive pulse width | 10 | | BCLKS | | Figure 98 |
| T10 | PWRGOOD to RESET# deassertion time | 1 | | ms | | Figure 98 |

## 12.4.1. ICH4-M Power Sequencing Requirements

### 12.4.1.1. 3.3 V/1.5 V Power Sequencing

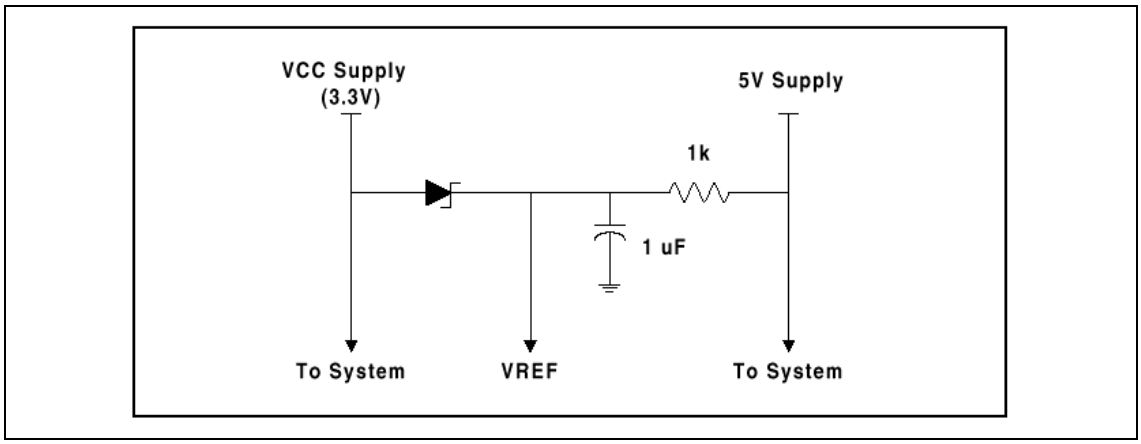
No power sequencing requirements exist for the associated 3.3 V/1.5 V rails of the Intel ICH4-M. It is generally good design practice to power up the core before or at the same time as the other rails.

### 12.4.1.2. $V_{5REF}$/ 3.3 V Sequencing

$V_{5REF}$ is the reference voltage for 5-V tolerance on inputs to the Intel ICH4-M. $V_{5REF}$ must be powered up before $V_{CC3_3}$, or after $V_{CC3_3}$ within 0.7 V. Also, $V_{5REF}$ must power down after $V_{CC3_3}$, or before $V_{CC3_3}$ within 0.7 V. It must also power down after or simultaneous to $V_{CC3_3}$. These rules must be followed in order to ensure the safety of the Intel ICH4-M. If the rule is violated, internal diodes will attempt to draw power sufficient to damage the diodes from the $V_{CC3_3}$ rail. Figure 99 shows a sample implementation of how to satisfy the $V_{5REF}$/ 3.3 V sequencing rule.

This rule also applies to the stand-by rails, but in most platforms, the $V_{CCSUS3_3}$ rail is derived from the $V_{CCSUS5}$ and therefore, the $V_{CCSUS3_3}$ rail will always come up after the $V_{CCSUS5}$ rail. As a result, $V_{5REF_SUS}$ will always be powered up before $V_{CCSUS3_3}$. In platforms that do not derive the $V_{CCSUS3_3}$ rail from the $V_{CCSUS5}$ rail, this rule must be comprehended in the platform design.

**Figure 99. Example $V_{5REF}$ / 3.3 V Sequencing Circuitry**




### 12.4.1.3. $V_{5REF_SUS}$ Design Guidelines

In order to meet reliability and testing requirements for the USB interface, the following design recommendations for the $V_{5REF_SUS}$ pins of the ICH4-M should be followed. Changes to the USB specification regarding continuous short conditions must be addressed. The USB 1.1 specification requires host controllers to withstand a continuous short between the USB 5-V connector supply to a USB signal at the connector for an unspecified duration of time. Also, the USB 2.0 specification requires a host controller to withstand a short between the USB 5-V connector supply to a USB signal at the connector for 24 hours. The recommendation is to provide a 5V_ALWAYS (active S0-S5) supply to the $V_{5REF_SUS}$ pins if available (see Figure 100). If such a supply rail is not readily available on the platform, then an alternative implementation using a 3.3V_ALWAYS (active S0-S5) and a VCC5 (active S0-S1M) or VCCSUS5 (active S0-S3) rail can be used instead (see Figure 101).

**Figure 100. V5REF_SUS with 5V_ALWAYS Connection Option (Recommended)**

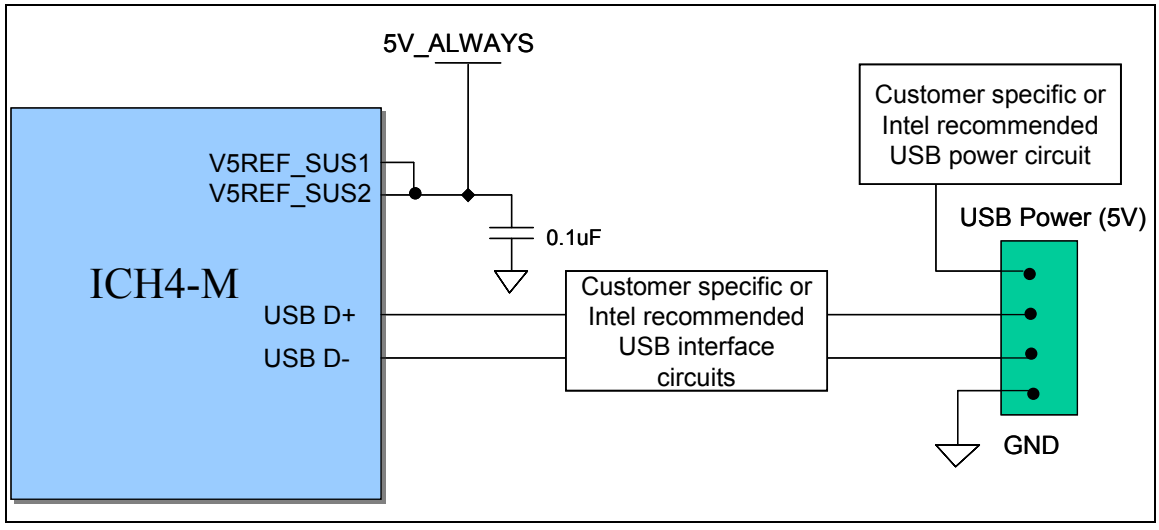
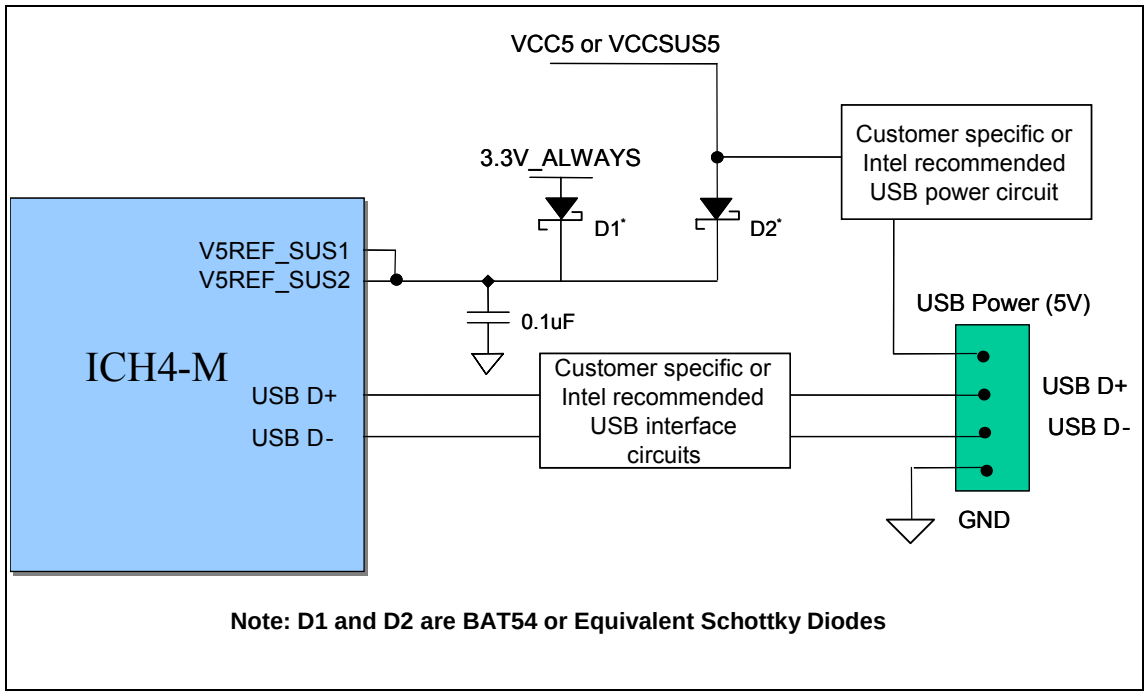


Figure 101. V5REF_SUS with 3.3V_ALWAYS and VCC5 or VCC5_SUS Connection Option




**Note: D1 and D2 are BAT54 or Equivalent Schottky Diodes**

## 12.4.2. GMCH Power Sequencing Requirements

No GMCH power sequencing requirements exist for the 852GME / 852PM GMCH platform. All GMCH power rails should be stable before deasserting reset, but the power rails can be brought up in any order desired. Good design practice would have all GMCH power rails come up as close in time as possible, with the core voltage coming up first.

The ICH4-M's CPUPWRGOOD output represents the logical AND of its PWROK and VGATE inputs. When VGATE is asserted, it indicates that core power and the PCICLK are stable and PCIRST# will be de-asserted a minimum of 1 ms later. It is the responsibility of the system designers to ensure that the power and timing requirements for the processor and GMCH are met.

## 12.4.3. DDR Power Sequencing Requirements

No DDR-SDRAM power sequencing requirements are specified during power up or power down if the following criteria are met:

VDD and VDDQ are driven from a single power converter output.

VTT is limited to 1.44 V (reflecting VDDQ(max)/2 + 50 mV VREF variation + 40 mV VTT variation)

VREF tracks VDDQ/2

A minimum resistance of 42 (22 series resistor + 22 parallel resistor ± 5% tolerance) limits the input current from the VTT supply into any pin.

If the above criteria can not be met by the system design, then Table 87 below must be adhered to during power up.

**Table 87. DDR Power-Up Initialization Sequence**

| Voltage Description | Sequencing | Voltage Relationship to Avoid Latch-up |
|---|---|---|
| VDDQ | After or with VDD | < VDD + 0.3 V |
| VTT | After or with VDDQ | < VDDQ + 0.3 V |
| VREF | After or with VDDQ | < VDQ + 0.3 V |

### 12.4.4. PWR ICH4-M SYS_RESET# Signal

The Intel ICH4-M has a new signal called ICH4-M SYSRST#. This signal is an input to the ICH4-M and provides a way to activate a system reset. In previous designs with ICH3-M, system reset logic was often tied into PWROK, forcing an asynchronous reset. For a cleaner design, Intel recommends that system reset logic such as a debug port reset signal and/or a reset button, if used, be connected to this signal. SYS_RESET# provides an intelligent way to reset the system since it will wait up to 25 ms ± 2 ms for SMBus traffic to idle before initiating a system reset. Not only will some combinational logic that may have been needed for PWROK be unnecessary—reset button debounce circuitry is also not needed as the ICH4-M has this built-in. SYS_RESET# is in the resume I/O well of the ICH4-M and so circuitry connected to this signal must also be on the resume, or always on, rail.

## 12.5. DDR Power Delivery Design Guidelines

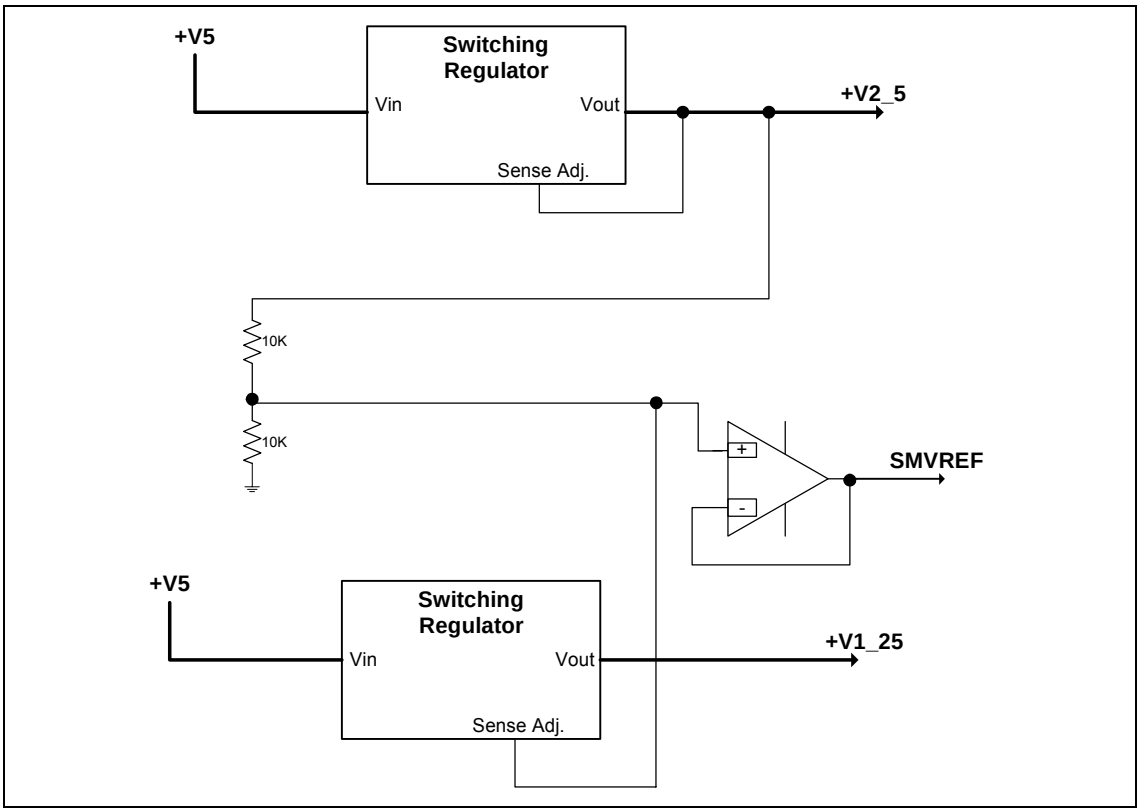
The main focus of these GMCH guidelines is to minimize signal integrity problems and improve the power delivery to of the GMCH system memory interface and the DDR SO-DIMMs. This document is not the original source for these specifications. Refer to the following documents for the latest details on voltage and current requirements found in this design guide.

*JEDEC Standard, JESD79, Double Data Rate (DDR) SDRAM Specification*

*Intel DDR 20 JEDEC Spec Addendum Rev 0.9* or later

*Intel® 852GME Chipset GMCH and Intel® 852PM Chipset MCH Datasheet*

**Figure 102. DDR Power Delivery Block Diagram**




## 12.5.1. DDR Interface Decoupling Guidelines

The following decoupling recommendations for the DDR system memory interface are subject to change.

### 12.5.1.1. GMCH VCCSM Decoupling Guidelines

Every GMCH ground and VCCSM power ball in the system memory interface should have its own via. For the VCCSM pins of the GMCH, a minimum of eleven, 0603 form factor, 0.1- , high frequency capacitors is required and must be placed within 150 mils of the GMCH package. The eleven capacitors should be evenly distributed along the GMCH DDR system memory interface and must be placed perpendicular to the GMCH with the power (2.5 V) side of the capacitors facing the GMCH. The trace from the power end of the capacitor should be as wide as possible and it must connect to a 2.5-V power ball on the outer row of balls on the GMCH. Each capacitor should have their 2.5-V via placed directly over and connected to a separate 2.5-V copper finger, and they should be as close to the capacitor pad as possible, within 25 mils. The ground end of the capacitors must connect to the ground flood and to the ground plane through a via. This via should be as close to the capacitor pad as possible, within 25 mils, and with as thick a trace as possible.

#### 12.5.1.2. DDR SO-DIMM System Memory Decoupling Guidelines

Discontinuities in the DDR signal return paths will occur when the signals transition between the motherboard and the SO-DIMMs. To account for this ground to 2.5-V discontinuity, a minimum of nine 0603 0.1-µF high frequency bypass capacitors is required between the SO-DIMMs to help minimize any anticipated return path discontinuities that will be created. The bypass capacitors should be connected to 2.5 V and ground. The ground trace should connect to a via that transitions to the ground plane. The ground via should be placed as close to the ground pad as possible. The 2.5-V trace should connect to a via that transitions to the 2.5-V copper flood and it should connect to the closet 2.5-V SO-DIMM pin on either the first o second SO-DIMM connector, with a wide trace. The capacitors 2.5-V traces should be distributed as evenly as possible amongst the two SO-DIMMs. Finally, the 2.5-V via should be placed as close to the 2.5-V pad as possible.

## 12.5.2. 2.5-V Power Delivery Guidelines

The 2.5-V power for the GMCH system memory interface and the DDR SO-DIMMs is delivered around the DDR command, control, and clock signals. Special attention must be paid to the 2.5-V copper flooding to ensure proper GMCH and SO-DIMM power delivery. This 2.5-V flood must extend from the GMCH 2.5-V power vias all the way to the 2.5-V DDR voltage regulator and its bulk capacitors, located at the end of the DDR channel beyond the second SO-DIMM connector. The 2.5-V DDR voltage regulator must connect to the 2.5-V flood with a minimum of six vias, and the SO-DIMM connector 2.5-V pins as well as the GMCH 2.5-V power vias must connect to the 2.5-V copper flood. The copper flooding to the GMCH should include at least seven fingers to allow for the routing of the DDR signals and for optimal GMCH power delivery. The copper fingers must be kept as wide as possible in order to keep the loop inductance path from the 2.5-V voltage regulator to the GMCH at a minimum. In the areas where the copper flooding necks down around the GMCH make sure to keep these neck down lengths as short as possible. The 2.5-V copper flooding under the SO-DIMM connectors must encompass all the SO-DIMM 2.5-V pins and must be sold except for the small areas where the clocks are routed within the SO-DIMM pin field where they connect to their specified SO-DIMM pins.

Additionally, a small 2.5-V copper flood shape should be placed under the GMCH to encompass and increase the copper flooding to the back row of the 2.5-V GMCH pins. This flood must not be placed under any of the DDR signals. In order to maximize the copper flooding, these signals should be kept as short as possible in order to reduce the amount of serpentining needed in this area on the bottom layer. Also, a minimum of 12-mil isolation spacing should be maintained between the copper flooding and the DDR signals. Finally, the six, GMCH, 2.5-V, high-frequency decoupling capacitors located on the top signal layer should have their 2.5-V via placed directly over and connected to a separate 2.5-V copper finger.

## 12.5.3. DDR Reference Voltage

Table 88, Table 89, and Table 90 group the voltage and current specifications together for the memory, GMCH, and termination voltage respectively. There are three voltages specified for a DDR VR system. Although there are only two unique voltage regulators for 2.5 V and 1.25-V nominal, each specific power rail described here has a unique specification.

For convenience, tolerances are given in both % and volts though validation should be done using the spec exactly as it is written. If this states a tolerance in terms of volts (e.g. VREF says ± 0.025 V), then that specific voltage tolerance should be used, not a percentage of the measured value. Likewise,

percentages should be used where stated. If not stated, then either way is fine. Voltage specs are defined as either “Absolute” or “Relative.” These are described in Table 88.

***Note:*** VREF to SO_DIMM and GMCH should stay on during S3 state on all 852 chipset families.

**Table 88. Absolute vs. Relative Voltage Specification**

| Type of Specification | Description |
|---|---|
| Absolute Specification | This is a standard specification most commonly used. This means that the voltage limits are based on a fixed nominal voltage and have a symmetric ± tolerance added to determine the acceptable voltage range. For example, a VDD spec does not depend on any other voltage levels. It is simply 2.5 V ± 8%. |
| Relative Specification | This is a specification whose nominal value is not fixed but is relative to or is a function of another voltage. This means that the other voltage must be measured to know what the nominal value is and then the symmetrical ± tolerance added to that measured value. For example, a VREF spec depends on the actual value of VDD to determine VDD/2 and then tolerance ± 0.050 V from this calculated value. |

In the following three tables, only the 2.5-V supply is a fixed, absolute specification, whereas all of the 1.25-V nominal supplies are relative to the 2.5-V supply directly or another 1.25-V supply, which is then relative to the 2.5-V supply. Due to these 1.25-V relative specifications, it is important that the 1.25-V supply can track the variations in the 2.5-V supply and respond according to the 2.5-V variations. This can be implemented as shown in the block diagram in Figure 102 where the 2.5-V output is divided in half and used to generate the 1.25-V reference into the 1.25-V, VR controller design. In this manner, the 1.25-V VR will respond proportionally to variations in the 2.5-V supply, improving the voltage margin of the relative supply requirements and overall memory system stability.

As of publication of this document, all specifications were current. However, it is realized that the current specifications are considered to be higher than actually expected and will be reduced in future specifications.

**Table 89. DDR-SDRAM SO-DIMM Voltage and Current Requirements**

| Parameter | Symbol | Unit | Definition | Minimum | Nominal | Maximum |
|---|---|---|---|---|---|---|
| Core Supply Voltage, Static | Vdd | Volts, V | Vdd | 2.3 | 2.5 | 2.7 |
| I/O Supply Voltage, Static | VddQ | Volts, V | VddQ | 2.3 | 2.5 | 2.7 |
| Core Supply Current, Static | Idd | Amperes, A | | | | 5.0 |
| I/O Supply Current, Static | IddQ | Amperes, A | | | | 0.920 |
| Absolute I/O Reference Supply Voltage, Static | VREF | Volts, V | Vdd/2 ± 0.05 V | Vdd/2 – 0.05 | Vdd/2 | Vdd/2 + 0.05 |
| I/O Reference Supply Current, Static | Iref | Amperes, A | | | | < 0.001 |

**Table 90. Intel GMCH System Memory Voltage and Current Requirements**

| Parameter | Symbol | Unit | Definition | Minimum | Nominal | Maximum |
|---|---|---|---|---|---|---|
| GMCH DDR Supply Voltage (I/O), Static | VCCSM | Volts, V | VCCSM | 2.375 | 2.5 | 2.625 |
| GMCH DDR Supply Current, Static | Ivccsm | Amperes, A | | | | 2.8 |
| Intel GMCH Reference Supply Voltage, Static | SMVREF | Volts, V | VCCSM/2 ± 2% | VCCSM/2 – 2% | VCCSM/2 | VCCSM/2 + 2% |
| Intel GMCH Reference Supply Current, Static | Isdref | Amperes, A | | | | 0.01 |
| SMRCOMP Termination Supply Voltage, Static | Vtt | Volts, V | SMVref ± 0.04 V | SMVref – 0.04 | SMVref | SMVref + 0.04 |
| SMRCOMP Termination Supply Current, Static | Ittrc | Amperes, A | | | | 0.025 |

**Table 91. Termination Voltage and Current Requirements**

| Parameter | Symbol | Unit | Minimum | Nominal | Maximum |
|---|---|---|---|---|---|
| Termination Supply Voltage, Static | Vtt | Volts, V | SMVref – 0.04V | SMVref | SMVref + 0.04V |
| Termination Supply Current, Static | Itt | Amperes, A | | | 2.4 |

### 12.5.3.1. SMVREF Layout and Routing Recommendations

There is one SMVREF pin on the 852GME / 852PM GMCH that is used to set the reference voltage level for the DDR system memory signals (SMVREF_0). The reference voltage must be supplied to the SMVREF pin. The voltage level that needs to be supplied to this pin must be equal to VCCSM/2. Note in Figure 102 that although SMVREF is generated from the 2.5-V supply, a buffer is used as well. A buffer has also been used to provide this reference to the system for the GMCH and memory. This is the "VREF" signals to the DDR memory devices and the "SMVREF" signals (SMVREF_0) to the GMCH. The reference design utilizes this buffer to provide the necessary current to these devices, which a simple voltage divider is not capable of providing. The reference voltage supplied to SMVREF has the tightest tolerance in the memory system of ± 2%. A simple resistor divider is not a voltage regulator and is most definitely not a current source. Any current drawn across the resistor divider used to generate this 1.25-V reference will cause a voltage drop across the top resistor, which distorts or biases this reference to a lower voltage. The clarification below summarizes SMVREF.

### Table 92. GMCH System Memory I/O SMVREF Calculation

| Name | VCCSM[1] | SMVREF |
|---|---|---|
| PURPOSE | GMCH DDR SUPPLY VOLTAGE (I/O), STATIC | GMCH REFERENCE SUPPLY VOLTAGE, STATIC |
| | VCCSM | SMVREF = (VCCSM ± 5%) / 2 |
| VOLTAGE Nominal (V) | 2.500 "± 5%" | 1.250 "± 2%" |
| | | |
| TOLERANCE (±V) | 0.125 | 0.025 |
| Vmax(V) | 2.625 | 1.275 |
| Vmin(V) | 2.375 | 1.225 |
| | Ivccsm (max) | Isdref (max) |
| Imax (A) | 1.400 | 0.010 |

**NOTE:** GMCH VREF REQUIREMENTS: the GMCH core is called "VCCSM" =+2.5 V ± 5%. SMVREF is ("VCCSM"± 5%)/2 ± 2%. Whether the 2.5 V is 5% high or low, the voltage needs to be divided by 2 with a 2% accuracy. Therefore, use 1% resistors or better.

As shown in Table 92, the max current required by the GMCH for the SMVREF input is 0.010 A. This is too big of a load for a resistor divider. Some sample calculations are shown in Table 93; it is impossible to maintain regulation within 2% using a resistive divider without using a resistor so small that the 2.5-V current requirement becomes prohibitive. Hence, a buffer is required due to the 10-mA current requirement of the GMCH SMVREF.

### Table 93. Effects of Varying Resistor Values in the Divider Circuit

| Rdivider ( ) | Leakage (A) | Rtop Vdroop (V) | I(2.5) total = 2.5 V/2R (A) |
|---|---|---|---|
| 1 | 0.01 | 0.01 | 1.25 |
| 10 | 0.01 | 0.1 | 0.125 |
| 100 | 0.01 | 1 | 0.0125 |
| 1000 | 0.01 | 10 | 0.00125 |
| *10000* | *0.01* | *100* | 0.000125 |
| 100000 | 0.01 | 1000 | 1.25E-05 |
| 1000000 | 0.01 | 10000 | 1.25E-06 |

**NOTES:**

1. Rdivider: This is the resistor value selected to form the divider. Assumes both top and values are equal as required for divide by 2.
2. Leakage: This is the amount of leakage current which needs to sourced from the 2.5-V supply, across the divider's top resistor (Rtop) and out to the GMCH SMVREF input or the DDR VREF input. This current does not go across the bottom resistor.
3. Rtop Vdroop: This is the resulting voltage droop across Rtop as a result of the leakage current.
4. I(2.5) total = 2.5 V/2R. This is the total current through divider. This is calculated to consider the amount of current & power used as a DC current through the divider.
5. The implementation of a buffer is also required by the DDR. The same VREF may be used for both GMCH and the DDR as well.

### 12.5.3.2. DDR VREF Requirements

Making the same calculations for the DDR loading, the max VREF load is 1 mA; therefore, a divider is STILL NOT feasible as the load of 1 mA causes unacceptable drop across even a small Rs, which wastes power.

**Table 94. DDR VREF Calculation**

| Name | Vdd | Vref |
|---|---|---|
| Purpose | Core Supply Voltage, Static | I/O Reference Supply Voltage, Static |
| | *Vdd* | *Vref = (Vdd=/-8%) / 2* |
| VOLTAGE Nominal (V) | *2.500* (± 8%) | *1.250* |
| Tolerance (+/-V) | 0.200 | 0.025 |
| Vmax(V) | 2.700 | 1.300 |
| Vmin(V) | 2.300 | 1.200 |
| | Idd | Iref |
| RDDP spec says | *5.000* | *0.001* |

**NOTE:** The DDR core is called "Vdd" =+2.5 V ±8% (=± 0.2 V). VREF is ("Vdd"± 8%)/2 ± 50 mV. Whether the 2.5 V is 8% high or low, ***that voltage*** must be able to be divided by 2, within 50-mV accuracy. Therefore, use 1% resistors or better.

**Table 95. Reference Distortion Due to Load Current**

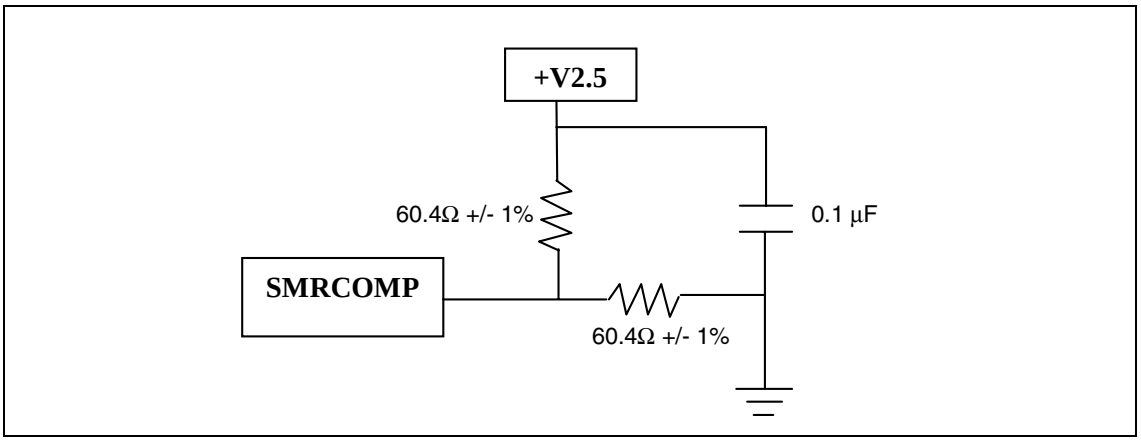
| R( ) | I(A) | Vdroop(V) | I(2.5) total=2.5 V/2R(A) |
|---|---|---|---|
| 1 | 0.001 | 0.001 | 1.25 |
| 10 | 0.001 | 0.01 | 0.125 |
| 100 | 0.001 | 0.1 | 0.0125 |
| 1000 | 0.001 | 1 | 0.00125 |
| *10000* | 0.001 | *10* | 0.000125 |
| 100000 | 0.001 | 100 | 1.25E-05 |
| 1000000 | 0.001 | 1000 | 1.25E-06 |

**NOTE:** As for the GMCH, a calculation can be made for the DDR. This shows that even with the slight load of 1 mA by the DDR, it is still not feasible to use a simple resistor divider. Using the max leakage specs provided and trying to maintain an error of less than 1% (12.5 mV), one needs to decrease the resistor values such that the current just to source the divider becomes unacceptable. A divider alone does not become an acceptable solution until current requirements are in the 100-µA range. Today, it is not possible to guarantee this type of current requirement for these applications. Therefore, the use of a buffer is highly recommended for these reference voltage requirements.

## 12.5.4. DDR SMRCOMP Resistive Compensation

The 852GME / 852PM GMCH requires a system memory compensation resistor, SMRCOMP, to adjust buffer characteristics to specific board and operation environment characteristics. Refer to the *Intel® 852GME Chipset GMCH and Intel® 852PM Chipset MCH Datasheet* and Figure 103 for details on resistive compensation.

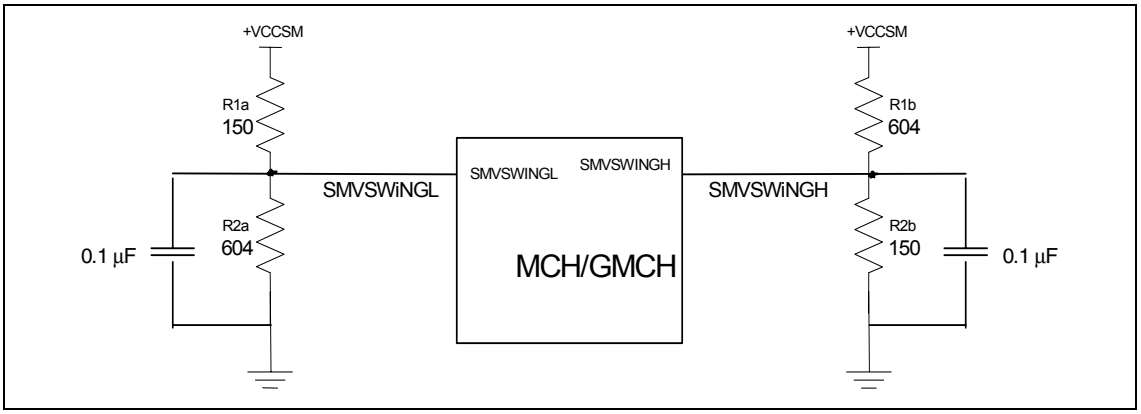
**Figure 103. DDR SMRCOMP Resistive Compensation**




The GMCH's system memory resistive compensation mechanism also requires the generation of reference voltages to the SMVSWINGL and SMVSWINGH pins with a value of 1/3*VCCP. The schematic for SMVSWINGL and SMVSWINGH voltage generation is illustrated in

Figure 104. Two resistive dividers with R1a = R2b = 150 ± 1% and R1b = R2a = 604 ± 1% generate the SMVSWINGL and SMVSWINGH voltages. SMVSWINGL and SMVSWINGH components should be placed within 0.5 inches of their respective pins and connected with a 15-mil wide trace. To avoid coupling with any other signals, maintain a minimum of 25 mils of separation to other signals.

**Figure 104. SMVSWINGL and SMVSWINGH Reference Voltage Generation Circuit**




## 12.5.5. DDR VTT Termination

The recommended topology for DDR-SDRAM Data, Control, and Command signal groups requires that all these signals to be terminated to a 1.25-V source, VTT, at then end of the memory channel opposite the GMCH. A solid 1.25-V termination island should be used to for this purpose. The VTT termination island should be placed on the top signal layer, just beyond the last SO-DIMM connector and must be at least 50-mils wide. The Data and Command signals should be terminated using one resistor per signal. Resistor packs and ± 5% tolerant resistors are acceptable for this application. Only signals from the same DDR signal group can share a resistor pack. See Section 12.5.1 and Section 12.7 for details on high frequency and bulk decoupling requirements.

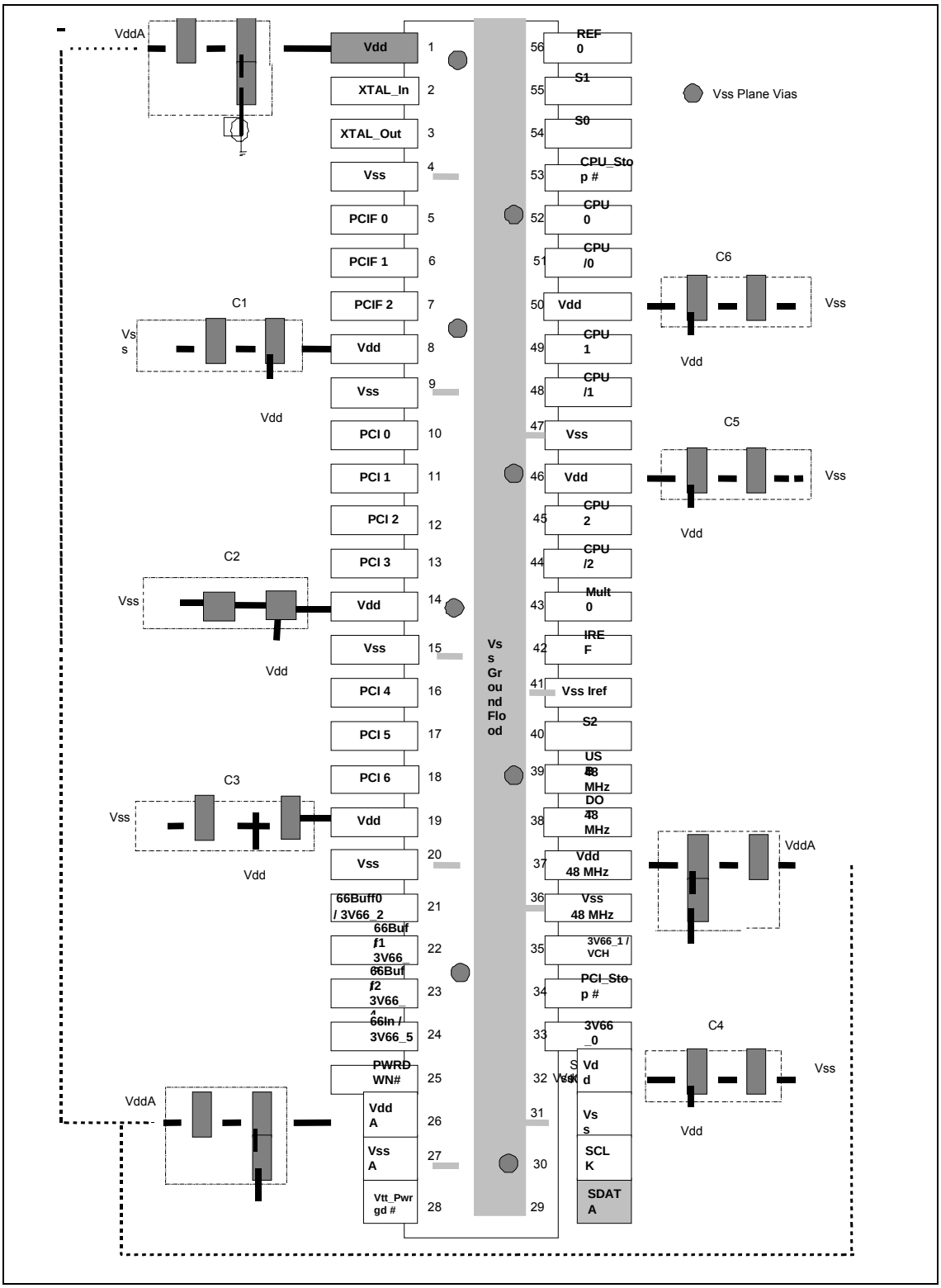
## 12.6. Clock Driver Power Delivery Guidelines

Special care must be taken to provide a quiet VDDA supply to the Ref VDD, VDDA, and the 48-MHz VDD. These VDDA signals are especially sensitive to switching noise induced by the other VDDs on the cock chip. They are also sensitive to switching noise generated elsewhere in the system such as the CPU VRM. The CLC pi-filter should be designed to provide the best reasonable isolation. Intel recommends that a solid ground plane be underneath the clock chip on Layer 2. (Assuming top trace is Layer 1.) Intel also recommends that a ground flood be placed directly under the clock chip to provide a low impedance connection for the VSS pins.

For ALL power connections to planes, decoupling capacitors and vias, the **maximum** trace width allowable and shortest possible lengths should be used to ensure lowest possible inductance. The decoupling capacitors should be connected as shown in the illustration taking care to connect the VDD pins directly to the VDD side of the capacitors. However, the VSS pins should not be connected directly to the VSS side of the capacitors. Instead they should be connected to the ground flood under the part that is via'ed to the ground plane. This is done to avoid VDD glitches propagating out and getting coupled through the decoupling capacitors to the VSS pins. This method has been shown to provide the best clock performance.

The ground flood should be via'ed through to the ground plane with no less than 12-16 vias under the part. It should be well connected. For all power connections, heavy duty and/or dual vias should be used. It is imperative that the standard signal vias and small traces not be used for connecting decoupling capacitors and ground floods to the power and ground planes. VDDA should be generated by using a CLC pi-filter. This VDDA should be connected to the VDD side of the three capacitors that require it using a hefty trace on the top layer. This trace should be routed from the CLC pi-filter using a star topology.

**Figure 105. Decoupling Capacitors Placement and Connectivity**



## 12.7. Decoupling Recommendations

Intel recommends proper design and layout of the system board bulk and high frequency decoupling capacitor solution to meet the transient tolerances for each component. To meet the component transient load steps, it is necessary to properly place bulk and high frequency capacitors close to the component power and ground pins.

### 12.7.1. Processor Decoupling Guidelines

**Table 96. Processor Decoupling Recommendation**

| Signal | Configuration | F | Qty | Notes |
|---|---|---|---|---|
| VCC[VCC_IMVP] | Tie to VCC | 680uF | 9 | |
| VCC[VCC_CORE] | Tie to VCC | 22uF | 14 | |
| VCC[VCC_CORE] | Tie to VCC | 680uF | 9 | Nine X 680uF, 8 m |

***Note:*** Decoupling guidelines are recommendations based on Intel's reference board design. Layout and PCB board design must be considered when deciding on overall decoupling solution.

### 12.7.2. Intel 852GME/852GMV/852PMGMCH Decoupling Guidelines

Bulk decoupling is based on VR solution used on the CRB design. Table 97 below outlines the minimum GMCH decoupling requirements.

**Table 97. GMCH Decoupling Recommendations**

| Pin Name | Configuration | F | Qty | Type | Notes |
|---|---|---|---|---|---|
| VCC | Tie to VCC1_5S | 0.1 µF<br>10 µF<br>150 µF | 4<br>1<br>2 | XR7, 0603, 16 V, 10%<br>XR5, 1206, 6.3 V, 20%<br>SPC, E, 6.3 V, 20% | 1 X 0.1 µF with in 200mils<br>3 X 0.1 µF on bottom side |
| VTTLF | Tie to VCCP | 0.1 µF<br>10 µF<br>150 µF | 2<br>1<br>1 | XR7, 0603, 16 V, 10%<br>XR5, 1206, 6.3 V, 20%<br>SPC, E, 6.3 V, 20% | 2 X 0.1 µF on bottom side |
| VTTHF | Tie to GND | 0.1 µF | 5 | XR7, 0603, 16 V, 10% | |
| VCCHL | Tie to VCC1_5S | 0.1 µF<br>10 µF | 2<br>1 | XR7, 0603, 16 V, 10%<br>XR5, 1206, 6.3 V, 20% | 1 X 0.1 µF with in 200 mils<br>1 X 0.1 µF on bottom side |
| VCCSM | Tie to VCC2_5 | 0.1 µF<br>100 µF | 11<br>2 | XR7, 0603, 16 V, 10%<br>TANT, D, 10 V, 20% | 10 X 0.1 µF with in 200 mils<br>1 X 0.1 µF on bottom side |
| VCCDVO | Tie to VCC1_5S | 0.1 µF<br>10 µF<br>150 µF | 2<br>1<br>1 | XR7, 0603, 16 V, 10%<br>XR5, 1206, 6.3 V, 20%<br>SPC, E, 6.3 V, 20% | 1 X 0.1 µF with in 200 mils<br>1 X 0.1 µF on bottom side |

| Pin Name | Configuration | F | Qty | Type | Notes |
|---|---|---|---|---|---|
| VCCDLVDS[1] | Tie to VCC1_5S | 0.1 µF<br>22 µF<br>47 µF | 1<br>1<br>1 | XR7, 0603, 16 V, 10%<br>TANT, B, 10 V, 20%<br>TANT, D, 10 V, 20% | 1 X 0.1 µF with in 200 mils |
| VCCTXLVDS[1] | Tie to VCCSus2_5 | 0.1 µF<br>22 µf<br>47 µF | 3<br>1<br>1 | XR7, 0603, 16 V, 10%<br>TANT, B, 10 V, 20%<br>TANT, D, 10 V, 20% | 1 X 0.1 µF with in 200 mils<br>2 X 0.1 µF on bottom side |
| VCCGPIO | Tie to Vcc3_3S | 0.1 µF | 1 | XR7, 0603, 16 V, 10% | |
| SMVREF | | 0.1 µF | 1 | XR7, 0603, 16 V, 10% | 1 X 0.1 µF on bottom side |
| SMVSWINGL | | 0.1 µF | 1 | XR7, 0603, 16 V, 10% | |
| SMVSWINGH | | 0.1 µF | 1 | XR7, 0603, 16 V, 10% | |
| HDVREF | | 220 pF<br>1 µF | 3<br>3 | XR7, 0603, 25 V, 10%<br>XR5, 0603, 6.3 V, 20% | |
| HAVREF | | 0.1 µF | 1 | XR7, 0603, 16 V, 10% | |
| HCCREF | | 0.1 µF | 1 | XR7, 0603, 16 V, 10% | |
| HXVSWING | | 0.1 µF | 1 | XR7, 0603, 16 V, 10% | |

**NOTE:** If designing with external graphics decoupling are not required. Still need to connect the power pins.

## 12.7.3. Intel ICH4-M Decoupling Guidelines

The Intel ICH4-M is capable of generating large current swings when switching between logic high and logic low. This condition could cause the component voltage rails to drop below specified limits. To avoid this type of situation, ensure that the appropriate amount of bulk capacitance is added in parallel to the voltage input pins. Intel recommends that the developer use the amount of decoupling capacitors specified in Table 98 to ensure the component maintains stable supply voltages. The capacitors should be placed as close to the package as possible (100 mils nominal). Rotate caps that set over power planes so that the loop inductance is minimized (see Figure 106). The basic theory for minimizing loop inductance is to consider which voltage is on Layer 2 (power or ground) and spin the decoupling cap with the opposite voltage towards the BGA (Ball Grid Array). This greatly minimizes the total loop inductance. Intel recommends that for prototype board designs the designer include pads for extra power plane decoupling caps.

**Figure 106. Minimized Loop Inductance Example**

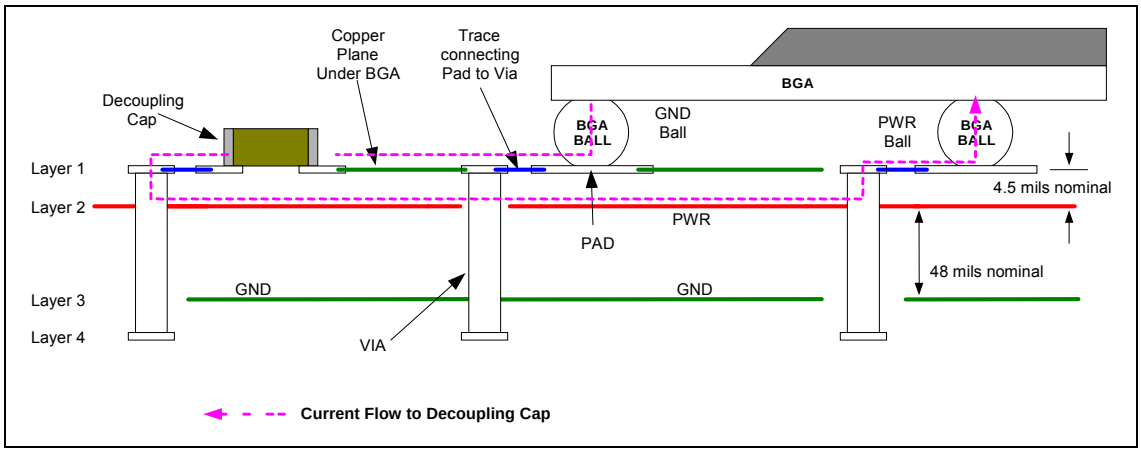



**Table 98. Decoupling Requirements for the Intel ICH4-M**

| Pin | Decoupling Requirements | Decoupling Type (Pin type) | Decoupling Placement |
|---|---|---|---|
| VCC3_3 | (6) 0.1 µF | Decoupling Cap (Vss) | Place near balls: A4, A1, H1, T1, AC10, and AC18 |
| VCCSUS3_3 | (2) 0.1 µF | Decoupling Cap (Vss) | Place near balls: A22 and AC5 |
| VCCLAN3_3 | (2) 0.1 µF | Decoupling Cap (Vss) | Place near balls: E9 and F9 |
| V_CPU_IO | (1) 0.1 µF | Decoupling Cap (Vcc) | Place near ball: AA23 |
| VCC1_5 | (2) 0.1 µF | Decoupling Cap (Vss) | Place near balls: K23 and C23 |
| VCCSUS1_5 | (2) 0.1 µF | Decoupling Cap (Vss) | Place near balls: A16 and AC1 |
| VCCLAN1_5 | (2) 0.1 µF | Decoupling Cap (Vss) | Place near balls: F6 and F7 |
| V5REF | (1) 0.1 µF | Decoupling Cap (Vcc) | Place near ball: E7 |
| V5REF_SUS | (1) 0.1 µF | Decoupling Cap (Vss) | Place near ball: A16 |
| VCCRTC | (1) 0.1 µF | Decoupling Cap (Vcc) | Place near ball: AB5 |
| VCCHI | (2) 0.1 µF | Decoupling Cap (Vss) | Place near balls: T23 and N23 |
| VCCPLL | (1) 0.1 µF<br>(1) 0.01 µF | Decoupling Cap (Vcc) | Place near ball: C22 |

**NOTES:**
1. Capacitors should be placed less than 100 mils from the package.
2. ICH4 -M balls listed in the “Decoupling Placement” guidelines column may not necessarily correlate to a VCC power ball and may include signal balls from different interfaces.

## 12.7.4. DDR VTT High Frequency and Bulk Decoupling

The VTT Island must be decoupled using high-speed bypass capacitors, one 0603, 0.1-µF capacitor per two DDR signals. These decoupling capacitors connect directly to the VTT island and to ground, and must be spread out across the termination island so that all the parallel termination resistors are near high frequency capacitors. The capacitor ground via should be as close to the capacitor pad as possible, within 25 mils with as thick a trace as possible. The ground end of the capacitors must connect to the

ground flood on Layer 2 and to the ground plane on Layer 3 through a via. Finally, the distance from any DDR termination resistor pin to a VTT capacitor pin must not exceed more then 100 mils.

### 12.7.5. Hub Interface Decoupling

See Section 9.4 for details.

### 12.7.6. FWH Decoupling

A 0.1-µF capacitor should be placed between the VCC supply pins and the VSS ground pins to decouple high frequency noise, which may affect the programmability of the device. Additionally, a 4.7-µF capacitor should be placed between the VCC supply pins and the VSS ground pins to decouple low frequency noise. The capacitors should be placed no further than 390 mils from the VCC supply pins.

### 12.7.7. General LAN Decoupling

All VCC pins should be connected to the same power supply.

All VSS pins should be connected to the same ground plane.

Four to six decoupling capacitors, including two 4.7-µF capacitors are recommended

Place decoupling as close as possible to power pins.

### 12.7.8. CK-408 Clock Driver Decoupling

The decoupling caps should be connected taking care to connect the VDD pins directly to the VDD side of the caps. However, the VSS pins should not be connected directly to the VSS side of the caps. Instead, they should be connected to the ground flood under the part that is via'ed to the ground plane. This is done to avoid VDD glitches propagating out and getting coupled through the decoupling caps to the VSS pins. This method has been shown to provide the best clock performance.

The decoupling requirements for a CK-408 compliant clock synthesizer are as follows:

One 10-µF bulk decoupling cap in a 1206 package placed close to the VDD generation circuitry.

Six 0.1-µF high frequency decoupling caps in a 0603 package placed close to the VDD pins on the CK-408.

Three 0.1-µF high frequency decoupling caps in a 0603 package placed close to the VDDA pins on the CK-408.

One 10-µF bulk decoupling cap in a 1206 package placed close to the VDDA generation circuitry

# 12.8. Intel 852GME/852GMV/852PMGMCH Analog Power Delivery

## 12.8.1. Analog Supply Filter Requirements

Table 99 summarizes the eight analog circuits that require filtered supplies on the 852GME / 852PM GMCH. The analog circuits are:

VCCASM

VCCQSM

VCCAHPLL

VCCADPLLA

VCCADPLLB

VCCADAC

VCCAGPLL

VCCALVDS

***Note:*** VCCADAC, VCCAHPLL, VCCAGPLL, and VCCALVDS do not require an RLC filter but do require decoupling capacitors.

**Figure 107. Example Analog Supply Filter**

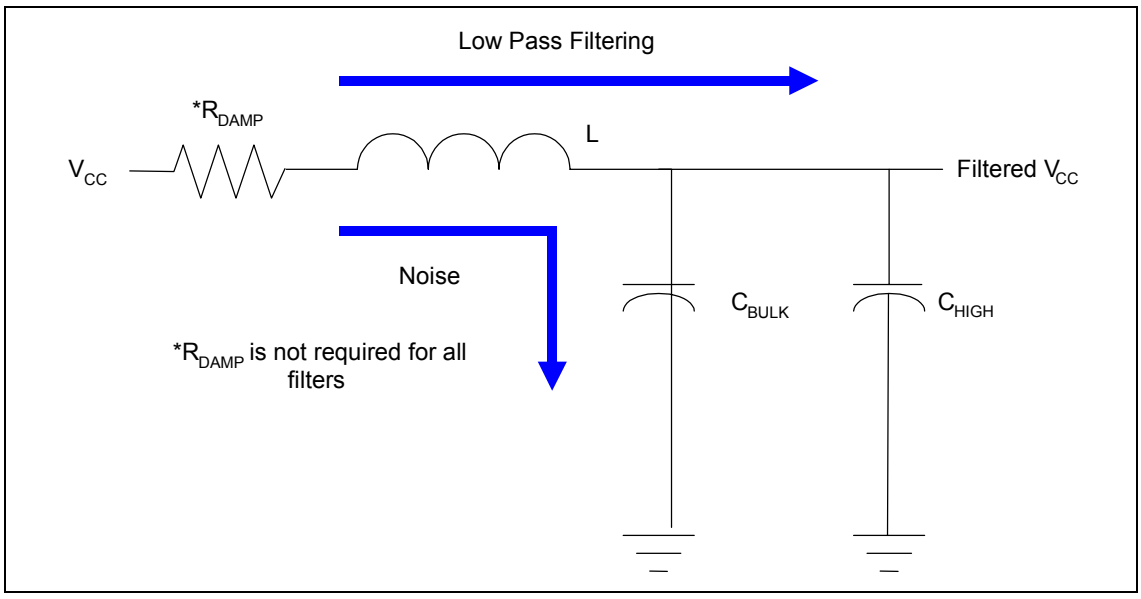


**Table 99. Analog Supply Filter Requirements**

| Required 852GME / 852PM Filters | Rdamp | Rdamp Location | L | Cbulk | Chigh |
|---|---|---|---|---|---|
| IVCCASM | None | N/A | 1210 1 µH DCRmax 0.169 s | 100 µF | 0603 0.1 µF X5R |
| VCCQSM | 1 | In series with capacitor | 0805 0.68 µH DCRmax 0.80 s | 1206 4.7 µF X5R | 0603 0.1 µF X5R |
| VCCAHPLL | None | N/A | None | None | 0603 0.1 µF X5R |
| VCCADPLLA[1] | 1 | In series with inductor | 0805 0.10 µH | 220 µF | 0603 0.1 µF X5R |
| VCCADPLLB | 1 | In series with inductor | 0805 0.10 µH | 220 µF | 0603 0.1 µF X5R |
| VCCADAC[1] | None | N/A | None | None | 0603 0.1 µF X5R 0603 0.01 µF X5R |
| VCCAGPLL | None | N/A | None | None | 0603 0.1 µF X5R |
| VCCALVDS[2] | None | N/A | None | None | 0603 0.1 µF X5R |

**NOTE:** If designing with external graphics decoupling is not required. Still need to connect power pin.

### 12.8.2. Recommended Routing/Component Placement

Recommended routing/component placement is as follows:

Each filter inductor and capacitors should be placed as close to the GMCH as possible.

If possible, route a trace from the VSSADAC and VSSALVDS balls to the capacitor before terminating to ground.

## 12.9. Intel 852GME/852GMV/852PMMaximum Supply Current Numbers

Table 100 shows the preliminary Intel 852GME / 852PM GMCH maximum supply current estimates.

**Table 100. Icc Maximum Sustained Estimates (Icc REV0.3)**

| Platform Component | Performance 133Gfx/400/533 FSB/266DDR 2 SO-DIMMs/4 Rows |
|---|---|
| 1.5 V Core | 1.4 A |
| 1.5 V LVDS (Digital) | 0.07 A |
| 1.5 V DAC & LVDS (Analog) | 0.07 A |
| 1.5 V DVO | 0.09 A |
| 2.5 V LVDS I/O | 0.05 A |
| 1.5 V GTL | TBD |
| 3.3 V GPIO | N/A |
| 1.5 V HUBLink | 0.09 A |
| 1.2 V DDR DLLs | 0.40 A |
| 2.5 V DDR | 2.07 A |

## 12.10. Intel ICH4-M Power Consumption Numbers

Table 101 shows the preliminary Intel ICH4-M power consumption estimates.

**Table 101. Intel ICH4-M Power Consumption Measurements**

| Power Plane | Maximum Power Consumption | | | | |
|---|---|---|---|---|---|
| | S0 | S1-M | S3 | S4/S5 | G3 |
| 1.5 V Core | 500 mA | 85 mA | N/A | N/A | N/A |
| 3.3 V I/O | 480 mA | 0.44 mA | N/A | N/A | N/A |
| 1.5 V LAN | 11.25 mA | 11.25 mA | 0 mA | 0 mA | N/A |
| 3.3 V LAN | 0.6 mA | 0.6 mA | 0 mA | | N/A |
| 1.5 V SUS | 79 mA | 46 mA | 8 mA | 8 mA | N/A |
| 3.3 V SUS | 166 mA | 0.7 mA | 0.06 mA | 0.06 mA | N/A |
| $V_{CCRTC}$ | N/A | N/A | N/A | N/A | 5 µA |
| $V_{_CPU_IO}$ | 2.5 mA | 2.5 mA | N/A | N/A | N/A |
| Vcc HI (HI 1.5 – 1.5V) | 99 mA | 99 mA | N/A | N/A | N/A |
| V5REF | 10 µA | 10 µA | N/A | N/A | N/A |
| V5REF_SUS | 10 µA | 10 µA | 10 µA | 10 µA | 10 µA |

**NOTES:**
1. 3.3-V SUS and 1.5-V SUS assume 6 high-speed ports populated.
2. Vcc HI power consumption is dependent on the Hub Interface being used

## 12.11. Thermal Design Power

The thermal design power is the estimated maximum possible expected power generated in a component by a realistic application. It is based on extrapolations in both hardware and software technology over the life of the product. It does not represent the expected power generated by a power virus. The thermal design power numbers for the 852GME/ 52PM GMCH and Intel ICH4-M are listed below.

**Table 102. Intel 852GME/852GMV/852PMGMCH Component Thermal Design Power**

| 852GME/852GMV/852PMGMCH - Thermal Design Power Consumption Dissipation (estimated) | |
|---|---|
| 852GME/852GMV/852PMGMCH | 3.8 W (maximum) |

**Table 103. Intel ICH4-M Component Thermal Design Power**

| Intel ICH4 - Thermal Design Power Consumption Dissipation (estimated) | |
|---|---|
| Intel ICH4-M | 2.2 W (maximum) |

# 13. Test Signals

The Mobile Intel Pentium 4 processor and 852GME/852GMV/852PMGMCH may have signals listed as "RSVD", "NC", or other name whose functionality is Intel reserved. The following section contains recommendations on how these Intel reserved signals on the processor or GMCH should be handled.

## 13.1. Mobile Intel Pentium 4 Processor Reserved Signals

The Mobile Intel Pentium 4 processor has NC and TESTHI signals that are Intel reserved in the pin-map. For connection recommendations on the TESTHI signals, refer to the latest *Mobile Intel® Pentium® 4 Processor Datasheet* or *Mobile Intel® Pentium® 4 Processor supporting Hyper-Threading Technology on 90-nm process technology*. All NC signals must remain unconnected.

## 13.2. Intel 852GME / 852PM GMCH RSVD Signals

The Intel 852GME / 852PM GMCH has a total of 32 RSVD and 12 NC signals that are Intel reserved in the pin-map. The recommendation is to provide test points for all RSVD signals. All NC signals should be left as no connects. The location of the Intel reserved signals in the GMCH pin-map is listed in Table 104.

**Table 104. GMCH "Intel Reserved" Signal Pin-Map Locations**

| Signal Name | Ball Name |
|---|---|
| NC | AJ29 |
| NC | AH29 |
| NC | B29 |
| NC | A29 |
| NC | AJ28 |
| NC | A28 |
| NC | AA9 |
| NC | AJ4 |
| NC | AJ2 |
| NC | A2 |
| NC | AH1 |
| NC | B1 |
| RSVD | AA22 |
| RSVD | L3 |
| RSVD | J3 |
| RSVD | J2 |
| RSVD | K5 |
| RSVD | K1 |
| RSVD | H6 |
| RSVD | G3 |
| RSVD | K3 |
| RSVD | K2 |
| RSVD | J6 |

| Signal Name | Ball Name |
|---|---|
| RSVD | J5 |
| RSVD | H2 |
| RSVD | H1 |
| RSVD | H3 |
| RSVD | H4 |
| RSVD | H5 |
| RSVD | K6 |
| RSVD | L5 |
| RSVD | F12 |
| RSVD | D12 |
| RSVD | B12 |
| RSVD | AA5 |
| RSVD | L4 |
| RSVD | F3 |
| RSVD | D3 |
| RSVD | B3 |
| RSVD | F2 |
| RSVD | D2 |
| RSVD | C2 |
| RSVD | B2 |
| RSVD | D7 |

# 14. Platform Design Checklist

This checklist provides design recommendation and guidelines for Intel 852GME/PM chipset platform for use with the Mobile Intel Pentium 4 processor and Intel Celeron processor. This checklist highlights design considerations that should be reviewed prior to manufacturing a motherboard that implements the 852GME/PM chipset. The items contained in this checklist address important connections to these devices and critical supporting circuitry. This is not a complete list, and it does not guarantee that a design will function properly.

***Note:*** Unless otherwise specified the default tolerance on resistors is ± 5%.

***Note:*** The (S) reference after power rails such as VCC3_3 (S) indicates a switched rail - one that is powered off during S3-S5. This work is ongoing, and the recommendations and considerations herein are subject to change.

## 14.1. General Information

The following section should be filled out by the OEM or Intel field representative.

| | |
|---|---|
| Processor | |
| Processor Min Frequency targeted for this platform | |
| Processor Max Frequency targeted for this platform | |
| Voltage Regulator Solution | Part#/Vendor:<br>Target ICC(max): |
| Target Thermal Envelope (Watts) | |
| Battery Life | Target: |
| Form Factor | |
| Panel Vendor and Size | Part#/Vendor: |
| Backlight Inverter | Part#/Vendor: |
| DVO Device | Part#/Vendor: |
| LOM or mini-PCI LAN? | |
| Wireless Solution? | |
| Target FCS (First Customer Ship) Date | |

## 14.2. Customer Implementation of Voltage Rails

Fill in schematic name of voltage rails and mark boxes of when rails are powered on.

| Name of Rail | On S0-S1 | On S3 | On S4 | On S5 |
|---|---|---|---|---|
| | | | | |
| | | | | |
| | | | | |
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| | | | | |

## 14.3. Design Checklist Implementation

The voltage rail designations in this design checklist are as general as possible. The following table describes the equivalent voltage rails in the Intel CRB schematics.

| Checklist Rail | Intel CRB Rail | On S0-S1 | On S3 | On S4 | On S5 | Notes |
|---|---|---|---|---|---|---|
| Vcc1_25 | +V1.25S [DDR_Vtt] | X | | | | 4 |
| Vcc1_5 | +V1.5S_GMCH_CORE,<br>+V1.5S_GMCH_HUB,<br>+V1.5S_GMCH_DVO/AGP,<br>+V1.5S_GMCH_ALVDS,<br>+V1.5S_GMCH_ADAC,<br>+V1.5S_GMCH_DLVDS,<br>+V1.5S_ICH,<br>+V1.5S_ICHHUB<br>+V1.5S_GMCH_HGPLL,<br>+V1.5S_GMCH_DPLL, | X | | | | |
| VccSus1_5 | +V1.5_ICHLAN | X | X | | | 1,3 |
| V1_5ALWAYS | +V1.5A_ICH | X | X | X | X | |
| VccSus2_5 | +V2.5_GMCH_SM,<br>+V2.5_GMCH_QSM,<br>+V2.5_GMCH_TXLVDS, | X | X | | | |
| Vcc3_3 | +V3.3S_ICH,<br>+V3.3S_GMCH_GPIO,<br>+V3.3S_CLKRC,<br>+V3.3S_SPD,<br>+V3.3S_LVDS, | X | | | | |
| VccSus3_3 | +V3.3_ICHLAN,<br>+V3.3_LAN | X | | | | 1,2,3 |
| V3ALWAYS | +V3.3ALWAYS_ICH | X | X | X | X | |
| Vcc5 | +V5S_DAC | X | | | | |
| VccSus5 | +V5_USB | X | X | | | 1,3 |
| V5ALWAYS | +V5A_ICH | X | X | X | X | |
| Vcc12 | +V12S | X | | | | |
| VccRTC | +V_RTC | X | X | X | X | |
| VCC | +VCC_IMVP | X | | | | |
| VCCIOPLL | +VCC_IMVP | X | | | | |
| VCCA | +VCC_IMVP | X | | | | |

| Checklist Rail | Intel CRB Rail | On S0-S1 | On S3 | On S4 | On S5 | Notes |
|---|---|---|---|---|---|---|
| Vcc1_25 | +V1.25S [DDR_Vtt] | X | | | | 4 |
| VccCORE | +VCC_CORE | X | | | | |

**NOTES:**
1. A rail powered in Sx is dependent on implementation.
2. VccLANx rail is powered on in Sx is dependent on implementation.
3. xALWAYS rail can be the SUS rail depending on implementation.
4. Vcc1_25 is the 1.25 V VTT rail for DDR.

| Pin Name | System Pull-up/Pull-down | Series Termination | Voltage Translation | Notes | ✓ |
|---|---|---|---|---|---|
| A20M# | | | | Point-to-point connection to ICH4-M. | ☐ |
| BR0# | 220 pull-up to VCC | | | Point-to-point connection to GMCH, with resistor placed by GMCH. | ☐ |
| COMP[1:0] | 61.9 ± 1% pull-down to gnd | | | Resistor placed within 0.5" of processor pin. Trace should be at least 25 mils. | ☐ |
| DPSLP# | | | | Point-to-point connection to GMCH. | ☐ |
| FERR# | 56 pull-up to VCC | | | Point-to-point connection to ICH4-M, with resistor placed by ICH4-M. | ☐ |
| GTLREF[3:0] | GTLREF needs to be 63% of VCC<br>51.1 ± 1% pull-up to VCC<br>86.6 ± 1% pull-down to gnd | | | Voltage divider should be placed within 0.5" of processor pin. Place 1-µF cap by the resistor divider, 220 pF by the processor pin. Minimum one GTLREF pin require to be connected as recommended above. | ☐ |
| GHI# | 300 pull-up to VCC | | | Point-to-point connection to ICH4-M. | ☐ |
| IERR# | 56 pull-up to VCC | | | IERR# is a 1.05-V signal. Voltage translation logic may be required if used. | ☐ |
| INIT# | | | R1 = 2 k<br>R2 = 300<br>Rs = 300 | Point-to-point connection to ICH4-M. Voltage transition circuit is required if connecting to FWH. Signal is T-split from the ICH4-M to FWH.<br>See Figure 108. | ☐ |
| IGNNE# | | | | Point-to-point connection to ICH4-M. | ☐ |
| LINT0/INTR | | | | Point-to-point connection to ICH4-M. | ☐ |
| LINT1/NMI | | | | Point-to-point connection to ICH4-M. | ☐ |
| PROCHOT# | 100-k pull up to VCC | | R1 = 1.3 k<br>R2 = 330<br>Rs = 330 | Please refer to CRB schematic for more datials.<br>**If Voltage Translation is Required**: Driver isolation resistor should be placed at the beginning of the T-split to the system receiver. The receiver at the output of the voltage translation circuit can be any receiver that can function properly | ☐ |

| Pin Name | System Pull-up/Pull-down | Series Termination | Voltage Translation | Notes | ✓ |
|---|---|---|---|---|---|
| | | | | with the PROCHOT# signal.<br>See Figure 110. | |
| BOOTSELECT | | | | Connects to CPU VR module. This pin will shift load line depends on Processor. Please refer to IMVP-5 specification for more information. | |
| OPTIMIZED/COMPAT# | | | | Please refer to Processor Datasheet for resistor recommendation. | |
| PWRGOOD | 300 pull-up to VCC | | | Point-to-point connection to ICH4-M, with resistor placed by the processor. | ☐ |
| RESET# | 51 pull-up to VCC<br>If USING ITP700FLEX | 150 from pull-up to ITP700FLEX | | **If ITP700FLEX is Not Used**: Point-to-point connection to GMCH.<br>**If ITP700FLEX is Used**: RESET# connects from processor to GMCH and then forks out to ITP700 FLEX, with pull-up and series damping resistor placed next to ITP. | ☐ |
| SLP# | | | | Point-to-point connection to ICH4-M. | ☐ |
| SMI# | | | | Point-to-point connection to ICH4-M. | ☐ |
| STPCLK# | | | | Point-to-point connection to ICH4-M. | ☐ |
| TESTHI[5:0], TESTHI[10:8] | 56 pull up to VCC | | | | ☐ |
| THERMTRIP# | 56 pull-up to VCC | | | Point-to-point connection to ICH4-M, with resistor placed by ICH4-M. THERMTRIP# is a VCC signal. If connecting to other device, voltage translation logic may be required. | ☐ |
| VCC[85:0] | Connect to VCC | | | | ☐ |
| VCCA, VSSA, VCCIOPLL | Connect to VCC via filter | | | Please refer to Figure 109 | ☐ |
| VCCSENSE, VSSSENSE | Connect to test vias | | | | ☐ |
| VSS[182:0] | Connect to gnd | | | | ☐ |

**NOTE:** Default tolerance for resistors is ± 5% unless otherwise specified.

**Figure 108. Routing Illustration for INIT#**

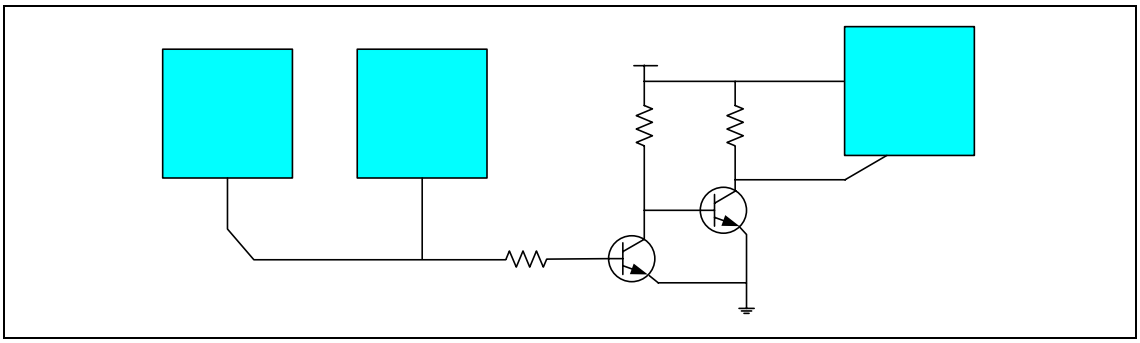


**Figure 109. VCCIOPLL, VCCA and VSSA Power Distribution**

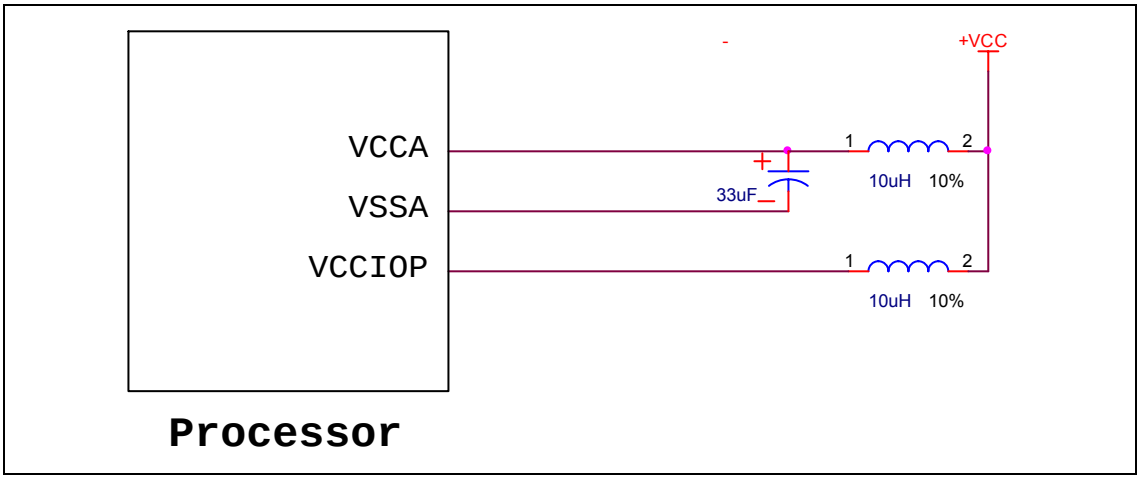
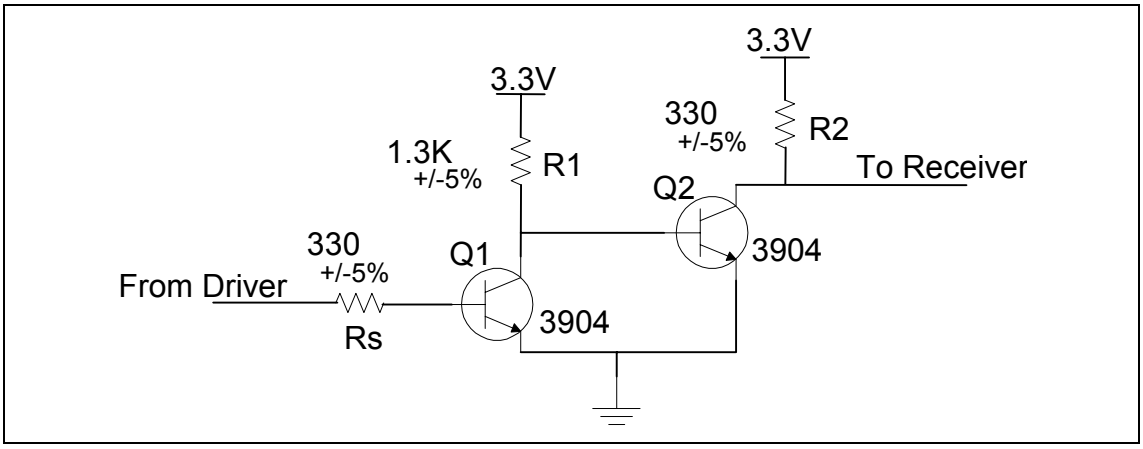



**Figure 110. Voltage Translation Circuit for PROCHOT#**



## 14.4. In Target Probe (ITP)

| Pin Name | System Pull-up / Pull-down | Series Termination Resistor ( | Notes | ✓ |
|---|---|---|---|---|
| BPM[5:0]# | 51 pull-up to VCC | | Connect to processor, with resistors placed by the processor. | ☐ |
| DBR# | 150-240 pull-up to V3ALWAYS | | If using ITP on interporser card, then DBR# should also be connected to DBRESET pin at the processor. | ☐ |
| RESET# | 51 pull-up to VCC<br>If USING ITP700FLEX | 150 from pull-up to ITP700FLEX | See Note 1 | ☐ |
| FBO | | | Connect to TCK pin of processor. | ☐ |
| TCK | 27.4 ± 1% pull-down to gnd | | Connect to processor, with resistor placed by ITP. | |
| TDI | 150 pull-up to VCC | | Connect to processor, with resistor placed by Processor. | ☐ |
| TDO | 75 pull-up to VCC | | Connect to processor, with resistor placed by ITP. If ITP not used, this signal can be left as NC. | ☐ |
| TMS | 39.2 ± 1% pull-up to VCC | | Connect to processor, with resistor placed by ITP. | ☐ |
| TRST# | 680 pull-down to gnd | | Connect to processor. | ☐ |
| VTAP, VTT[1:0] | Connect to VCC | | One 0.1-µF decoupling cap is required. | ☐ |

**NOTE:** The above recommendation is only for ITP700FLEX. If using other ITP, please refer to the appropriate ITP documents.

## 14.5. Decoupling Recommendations

| Signal | Configuration | Value | Qty | Notes | ✓ |
|---|---|---|---|---|---|
| VCC[Vcc_Core] | Connect to VCC | 22 µF | 14 | X5R/X7R, 1206 package. Use for high frequency decoupling. Bulk decoupling will depend on the VR solution. The maximum Equivalent Series Resistance should be equal to or less than 2.5 m | ☐ |
| VCC[Vcc_Core] | Connect to VCC | 9 | 680 µF | Nine X 680 µF, 8 m | |

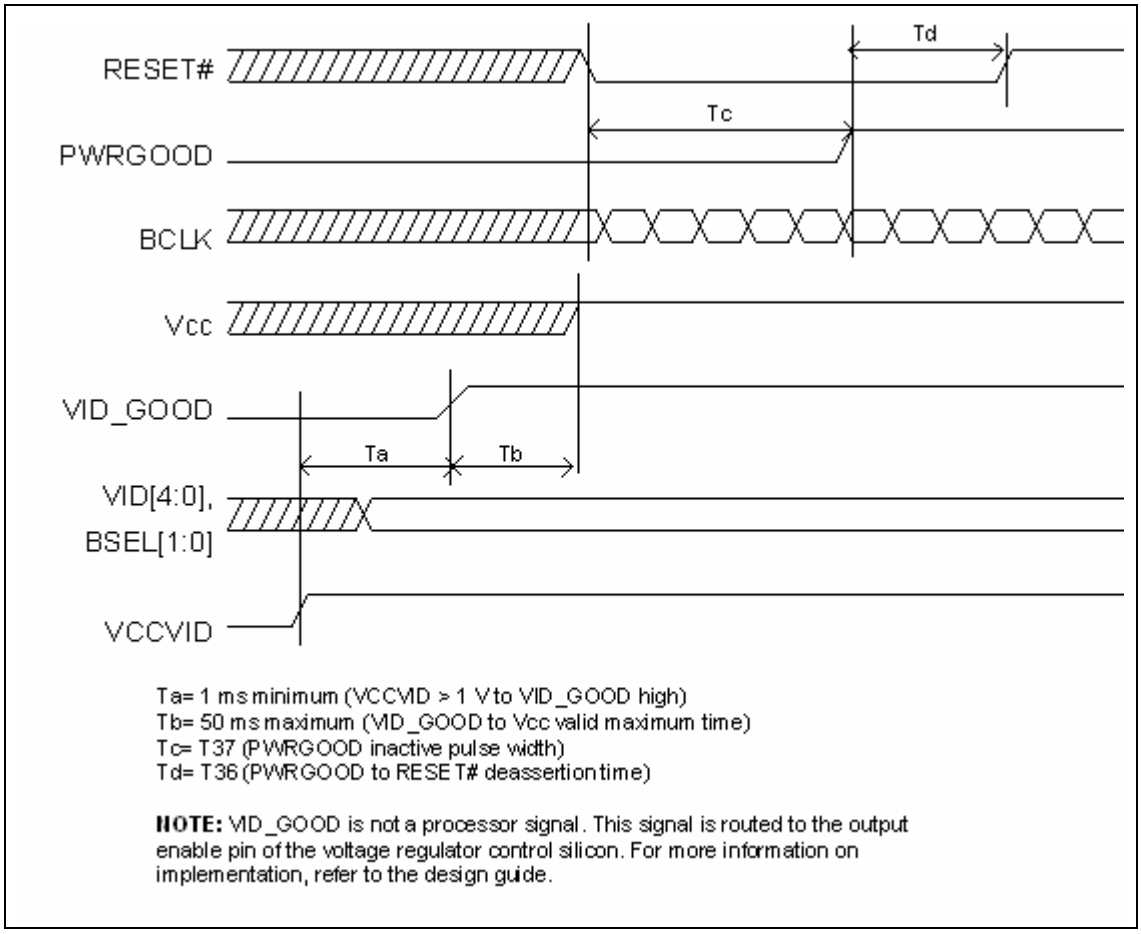
**NOTE:** Decoupling guidelines are recommendations based on our reference board design. Customers will need to take layout & PCB board design into consideration when deciding on overall decoupling solution.

## 14.6. Power-up Sequence

| Sym | Timing Parameters | Min | Max | Unit | Notes | ✓ |
|---|---|---|---|---|---|---|
| Ta | VccVID active to VID_GOOD | 1 | | ms | Please refer to the Processor Datasheet. See Figure 111. | ☐ |
| Tb | VID_GOOD valid to Vcc active | | 50 | ms | Please refer to the Processor Datasheet. See Figure 111. | ☐ |
| Tc | BCLK stable to PWRGOOD active | 10 | | BCLKs | Please refer to the Processor Datasheet. See Figure 111. | ☐ |
| Td | PWRGOOD active to RESET# inactive | 1 | 10 | ms | Please refer to the Processor Datasheet. See Figure 111. | ☐ |

**NOTE:** Please refer to latest processor datasheet.

**Figure 111. Mobile Intel Pentium 4 Processor Power Up Sequence**



# 14.7. CK-408 Clock Checklist

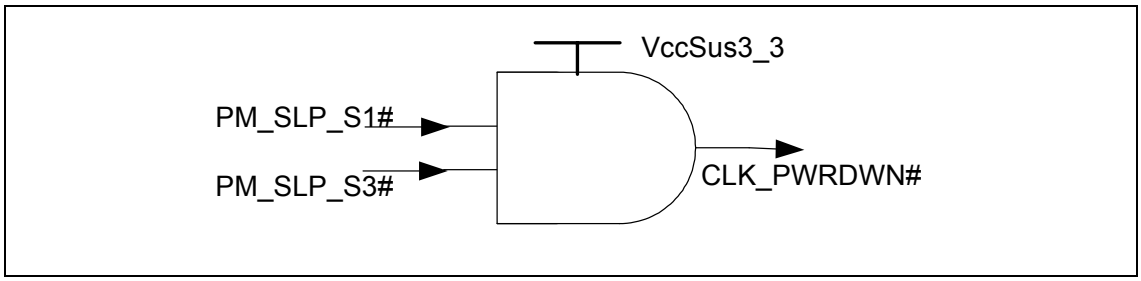
## 14.7.1. Resistor Recommendations

| Pin Name | System Pull-up/Pull-down | Series Resistor | Notes | ✓ |
|---|---|---|---|---|
| 3V66[0]<br>3V66[1] | | 33 | If the signal is used, one 33-ohm series resistor is required. If the signal is NOT used, it should be left as NC (Not Connected) or connected to a test point. | ☐ |
| 66BUF[2:0] | | 33 | Use 66 BUF[1] (pin 22) for GMCH. Use one of the other two signals for ICH4-M. | ☐ |
| CPU[0], CPU[0]#<br>CPU[1], CPU[1]#<br>CPU[2], CPU[2]# | 49.9 ± 1% pull- down to gnd | 33 | Use one pair for the processor and another pair for GMCH. If on-board ITP is implemented, the third pair of clock signals is used for the ITP connector. Otherwise, it can be routed to the dedicated ITP clock pins on the processor socket. | ☐ |
| 48MDOT | | 33 | Connect to GMCH's DREFCLK[1]. | ☐ |
| 3V66/VCH | | 33 | Two possible topologies:<br>1. Use directly for GMCH's DREFSSCLK.<br>2. Use as input to an SSC component and use the SSC component output GMCH's DREFSSCLK[1] | ☐ |
| IREF | 475 ± 1% pull-down to gnd | | | ☐ |
| MULT[0] | 10 k pull-up to Vcc3_3 | | | ☐ |
| PCI[6:0] | | 33 | Connect to various PCI devices. | ☐ |
| PCIF[2],<br>PCIF[1],<br>PCIF[0] | | 33 | Use one clock for ICH4-M. Unused clock pins should be left as NC or connected to a test point. | ☐ |
| PWRDWN# | | AND gate | This signal is needed for supporting S1M. It needs to be driven low by both SLP_S1# and SLP_S3# through an AND gate.<br>See Figure 112 | ☐ |
| REF | | 33 | This is the 14.318-MHz clock reference signal for ICH4-M, SIO and LPC. Each receiver requires one 33-ohm series resistor. | ☐ |
| SEL[2] | 1 k-20 k pull-down to gnd | | | ☐ |
| SEL[1] | 330 k-20 k pull- up to Vcc3_3 | | Connects to proceesor BSEL[0] | ☐ |

| Pin Name | System Pull-up/Pull-down | Series Resistor | Notes | ✓ |
|---|---|---|---|---|
| SEL[0] | 330 k-20 k pull- up to Vcc3_3 | | | ☐ |
| 48MUSB | | 33 | Connect to ICH4-M's 48-MHz clock input. | ☐ |
| XTAL_IN, XTAL_OUT | | | Connect to a 14.318-MHz crystal, placed within 500 mils of CK-408 | ☐ |
| VDD[7:0], VDDA | Connect to Vcc3_3 | | Refer to clock vendor datasheet for decoupling info. | ☐ |
| VSS[5:0], VSSA | Connect to gnd | | | ☐ |
| VSSIREF | Connect to gnd | | | ☐ |

**NOTE:** When using external graphics, may replace series resistor with 100- resistor because signal is not needed.

**Figure 112. Clock Power-down Implementation**



# 14.8. 852GME/852GMV/852PMChecklist

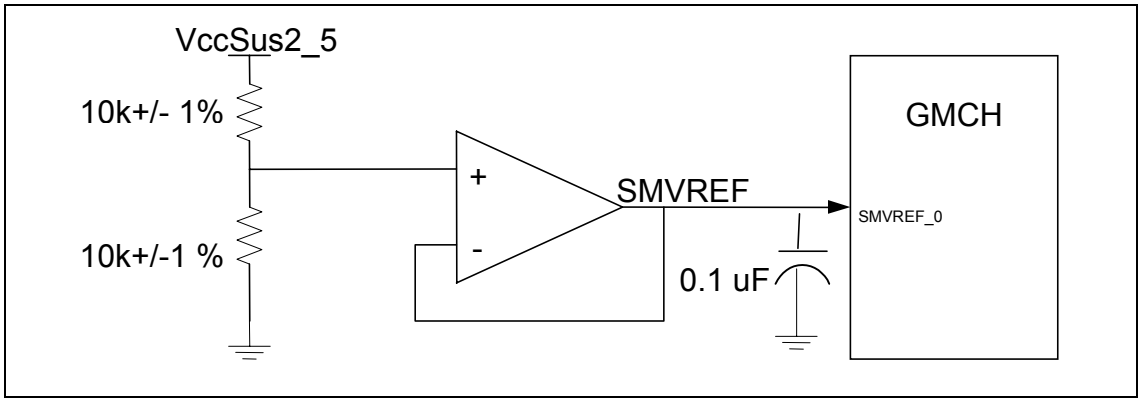
## 14.8.1. System Memory

### 14.8.1.1. GMCH System Memory Interface

| Pin Name | System Pull-up/Pull-down | Series Resistor | Notes | ✓ |
|---|---|---|---|---|
| RCVENIN# | | | This signal should be routed to a via next to ball and left as a NC (No Connect). | ☐ |
| RCVENOUT# | | | This signal should be routed to via next to ball and left as a NC (No Connect). | ☐ |
| SBA[1:0], SCAS#, SRAS#, SWE# | 56 pull-up to Vcc1_25 | 10 | Three topologies available for routing these signals. | ☐ |
| SCKE[3:0], SCS#[3:0] | 56 pull-up to Vcc1_25 | | | ☐ |
| SDQ[63:0], SDM[7:0], SDQS[7:0] | 56 pull-up to Vcc1_25 | 10 | | ☐ |
| SDQ[71:64], SDM8, SDQS8 | 56 pull-up to Vcc1_25 | 10 | For 852GME, if ECC support is not implemented, SDQ[71:64], SDM8, and SDQS8 should be left as NC. For ECC support, these signals connect to SO-DIMMs. | ☐ |
| SMA[12:6,3,0] | 56 pull-up to Vcc1_25 | 10 | Three topologies available for routing these signals. | ☐ |
| SMA[5,4,2,1]<br>SMAB[5,4,2,1] | 56 pull-up to Vcc1_25 | | Use SMA[5,4,2,1] for one SO-DIMM connector; use SMAB[5,4,2,1] for the other SO-DIMM connector. | ☐ |
| SCK0, SCK0#<br>SCK1, SCK1# | | | These clock signals connect to SO-DIMM 0. | ☐ |
| SCK2, SCK2# | | | For M-GM, if ECC supported is not implemented, these clock signals should be left as NC. For ECC support, these signals connect to SO-DIMM 0. | ☐ |
| SCK3, SCK3#<br>SCK4, SCK4# | | | These clock signals connect to SO-DIMM 1. | ☐ |
| SCK5, SCK5# | | | For 852GME, if ECC supported is not implemented, these clock signals should be left as NC. For ECC support, these signals connect to SO-DIMM 1. | ☐ |

| Pin Name | System Pull-up/Pull-down | Series Resistor | Notes | ✓ |
|---|---|---|---|---|
| SMVREF | 10 k 1% pull-up to VccSus2_5<br>10 k 1% pull-down to gnd | | Signal voltage level = VccSus2_5/ 2. Note that a buffer is used to provide the necessary current and reference voltage to SMVREF. Place a 0.1-µF cap by GMCH.<br>See Figure 113.This signal may be optionally connected to Vcc2_5 and powered off in S3. | ☐ |
| SMVSWINGL | 604 1% pull-up to VccSus2_5<br>150 1% pull-down to gnd | | Signal voltage level = 1/5 * VccSus2_5.<br>Need 0.1 µF cap at pin.<br>This signal may be optionally connected to Vcc2_5 and powered off in S3. | ☐ |
| SMVSWINGH | 150 1% pull-up to VccSus2_5<br>604 1% pull-down to gnd | | Signal voltage level = 4/5 * VccSus2_5.<br>Need 0.1 µF cap at pin.<br>This signal may be optionally connected to Vcc2_5 and powered off in S3. | ☐ |
| SMRCOMP | 60.4 1% pull-up to VccSus2_5<br>60.4 1% pull-down to gnd | | Signal voltage level = 1/2 * VccSus2_5.<br>Need 0.1 µF cap by the voltage divider.<br>This signal may be optionally connected to Vcc2_5 and powered off in S3. | ☐ |

**Figure 113. Reference Voltage Level for SMVREF**




### 14.8.1.2. DDR SO-DIMM Interface

| Pin Name | Configuration | Notes | ✓ |
|---|---|---|---|
| VREF[2:1] | | Signal voltage level = VCCSus2_5 / 2. | ☐ |
| VDD[33:1] | Connect to VccSus2_5 | Power must be provided during S3. | ☐ |
| VDDSPD | Connect to Vcc3_3 | | ☐ |
| SA[2:0] | Connect to either VC3_3 or gnd | These lines are used for strapping the SPD address for each SO-DIMM. | ☐ |

| | | | |
|---|---|---|---|
| VSS[31:1] | Connect to gnd | | ☐ |
| RESET(DU) | | Signal can be left as NC (“Not Connected) | ☐ |
| VDDID | | Signal can be left as NC (“Not Connected) | ☐ |
| DU[4:1] | | Signal can be left as NC (“Not Connected) | ☐ |
| GND[1:0] | | Signal can be left as NC (“Not Connected) | ☐ |

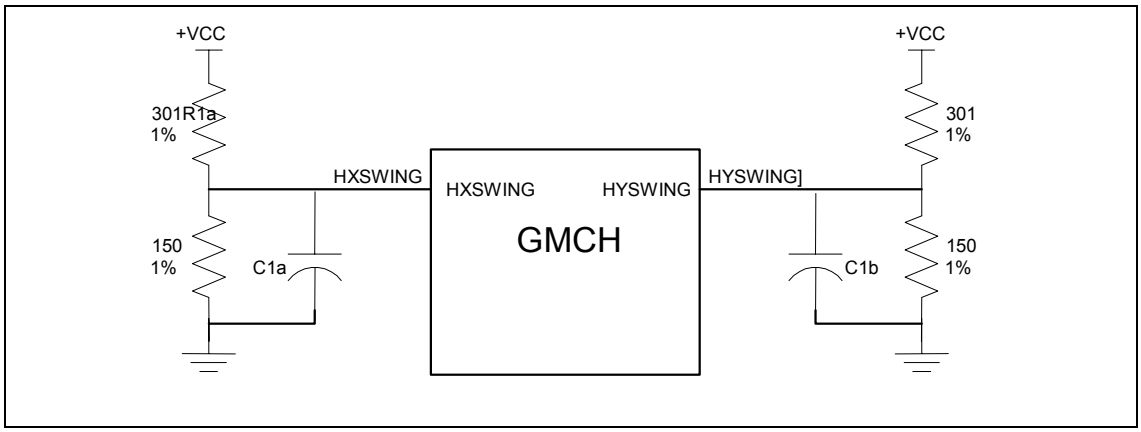
### 14.8.1.3. SO-DIMM Decoupling Recommendation

| Pin Name | F | Qty | Notes | ✓ |
|---|---|---|---|---|
| Vcc1_25 | 0.1 µF<br>0.01 µF | | Place one 0.1 µF cap and one 0.01 µF close to every 4 pull-up resistors terminated to Vcc1_25 (VTT for DDR signal termination). In S3, Vcc1_25 is powered OFF. | ☐ |
| Vcc2_5Sus | 0.1 µF<br>100-150 µF | 9<br>4 | A minimum of 9 high frequency caps are recommeneded to be placed bewteen the SO-DIMMS. A minimum of 4 low frequency caps are required. | ☐ |

## 14.8.2. FSB

| Pin Name | System Pull-up/Pull-down | Notes | ✓ |
|---|---|---|---|
| HXSWING, HYSWING | 301 1% pull-up to VCC<br>150 1% pull-down to gnd | Signal voltage level = 1/3 of VCC. C1a=0.1 µF. C1b=0.1 µF. Trace should be 10-mil wide with 20-mil spacing.<br>See Figure 114. | ☐ |
| HXRCOMP, HYRCOMP | 27.4 1% pull down to gnd | One pulled-down resistor per pin. Trace should be 10-mil wide with 20-mil spacing. | ☐ |
| HDVREF[2:0] | 49.9 1% pull-up to VCC<br>100 1% pull-down to gnd | Signal voltage level = 2/3 of VCC. Need one 0.1 µF cap and one 1 µF cap for voltage divider. | ☐ |
| HAVREF | 49.9 1% pull-up to VCC<br>100 1% pull-down to gnd | Signal voltage level = 2/3 of VCC. Need one 0.1 µF cap and one 1 µF cap for voltage divider. | ☐ |
| HCCVREF | 49.9 1% pull-up to VCC<br>100 1% pull-down to gnd | Signal voltage level = 2/3 of VCC. Need one 0.1 µF cap and one 1 µF cap for voltage divider. | ☐ |

**Figure 114. 852GME HXSWING & HYSWING Reference Voltage Generation Circuit**



## 14.8.3. Hub Interface

| Pin Name | System Pull-up/Pull-down | Notes | ✓ |
|---|---|---|---|
| HLVREF | See Section 14.9.9. | Signal voltage level = 0.35 V ± 8%. | ☐ |
| PSWING | See Section 14.9.9. | Signal voltage level = 0.8 V ± 8%. | ☐ |
| HLZCOMP | 48.7 1% pull-up to VCC | | ☐ |

## 14.8.4. Graphics Interfaces

### 14.8.4.1. LVDS

| Pin Name | System Pull-up/Pull-down | Notes | ✓ |
|---|---|---|---|
| LIBG | 1.5 k 1% pull-down to gnd | | ☐ |
| YAP[3:0]/YAM[3:0]<br>YBP[3:0]/YBM[3:0] | | If any of these LVDS data pairs are unused, they can be left as “no connect.” | ☐ |
| CLKAP/CLKAM<br>CLKBP/CLKBM | | If any of these LVDS clock pairs are not used, they can be left as “no connect.” | ☐ |
| LVREFH, LVREFL, LVBG | | These signals should be left as NC. | ☐ |

### 14.8.4.2. AGP/DVO

| Pin Name | System Pull-up/Pull-down | Notes | ✓ |
|---|---|---|---|
| DVORCOMP | 40.2 1% pull-down to gnd | Trace should be 10-mil wide with 20-mil spacing. | ☐ |
| GVREF | 1 k 1% pull-up to Vcc1_5<br>1 k 1% pull-down to gnd | Signal voltage level = 1/2 of Vcc1_5. Need 0.1 µF cap at pin. | ☐ |
| GAD[28:25]/DVOCD[11:6]<br>GCBE#3/DVOCD5<br>GAD[23:19]/DVO[4:0]<br>GADSTB1/DVOCCLK<br>GADSTB#/DVOCCLK#<br>GAD17/DVOCHSYNC<br>GAD16/DVOCVSYNC<br>GAD18/DVOCBLANK# | | If unused, these signals can be left as NC. | ☐ |
| GAD31/DVOCFLDSTL | 100 k pull-down to gnd | Pull-down resistor required only if signal is unused (10 k-100 k). It is up to DVO device to drive this signal. | ☐ |

| Pin Name | System Pull-up/Pull-down | Notes | ✓ |
|---|---|---|---|
| GAD30/DVOBCINTR# | 100 k pull-up to Vcc1_5 | Pull-up resistor required only if signal is unused (10 k-100 k). It is up to the DVO device to drive this signal. | ☐ |
| GAD13/DVOBCCLKINT | 100 k pull-down to gnd | Pull-down resistor required only if signal is unused (10 k-100 k). It is up to the DVO device to drive this signal. | ☐ |
| GAD3/DVOBD0<br>GAD2/DVOBD1<br>GAD5/DVOBD2<br>GAD4/DVOBD3<br>GAD7/DVOBD4<br>GAD6/DVOBD5<br>GAD8/DVOBD6<br>GCBE#0/DVOBD7<br>GAD10/DVOBD8<br>GAD9/DVOBD9<br>GAD12/DVOBD10<br>GAD11/DVOBD11<br>GADSTB0/DVOBCLK<br>GADSTB#0/DVOBCLK#<br>GAD0/DVOBHSYNC<br>GAD1/DVOBVSYNC<br>GBCE#1/DVOBBLANK# | | If AGP is not used these should left as NC. | ☐ |
| GAD30/DVOBFLDSTL (pin M2) | 100 k pull-down to gnd | For 852GME, pull-down resistor required on this signal (10 k-100 k). If AGP has been used pin doesn't require pull-down. | ☐ |
| GIRDY/MI2CCLK, GDEVSEL/MI2CDATA | 2.2 k pull-up to Vcc1_5 | Pull-up resistor required on each signal even if they are unused (2.2 k-100 k). This signal is 1.5-V tolerant. It may require voltage translation circuit. If AGP has been used pin doesn't require pull-up. | ☐ |
| GTRDY/MDVICLK, GFRAME#/MDVIDATA | 2.2 k pull-up to Vcc1_5 | Pull-up resistor required on each signal even if they are unused (2.2 k-100 k). This signal is 1.5-V tolerant. It may require voltage translation circuit. If AGP has been used pin doesn't require pull-up. | ☐ |
| GSTOP#/MDDCCLK, GAD15/MDDCDATA | 2.2 k pull-up to Vcc1_5 | Pull-up resistor required on each signal even if they are unused (2.2 k-100 k). This signal is 1.5-V tolerant. It may require voltage translation circuit. If AGP has been used pin doesn't require pull-up. | ☐ |
| GSBA[6:0]/ADDID[6:0] | | Leave as NC. | ☐ |
| GSBA7/ADDID7 | 1 k pull-down to gnd if DVO device is onboard | If DVO interface is not used, this signal can be left as "no connect". Otherwise, pull-down is needed. If AGP has been used pin doesn't require pull-down. | ☐ |

| Pin Name | System Pull-up/Pull-down | Notes | ✓ |
|---|---|---|---|
| GPAR/DVODETECT | 1 k pull-up to Vcc1_5 if DVO interface is unused | If DVO interface is used, leave as NC. This signal has internal pull-down. | ☐ |
| GPIPE#/DPMS | | If AGP is not used, connect this signal to 1.5-V version of ICH4-M's SUSCLK or a clock that runs during S1. See Figure 115. | ☐ |
| GST[2:0] | | These AGP signals are also used for strapping purposes. See Section 14.8.5 for details. Isolation circuit is needed for normal operation. See Figure 116. | ☐ |

**Figure 115. DPMS Clock Implementation**

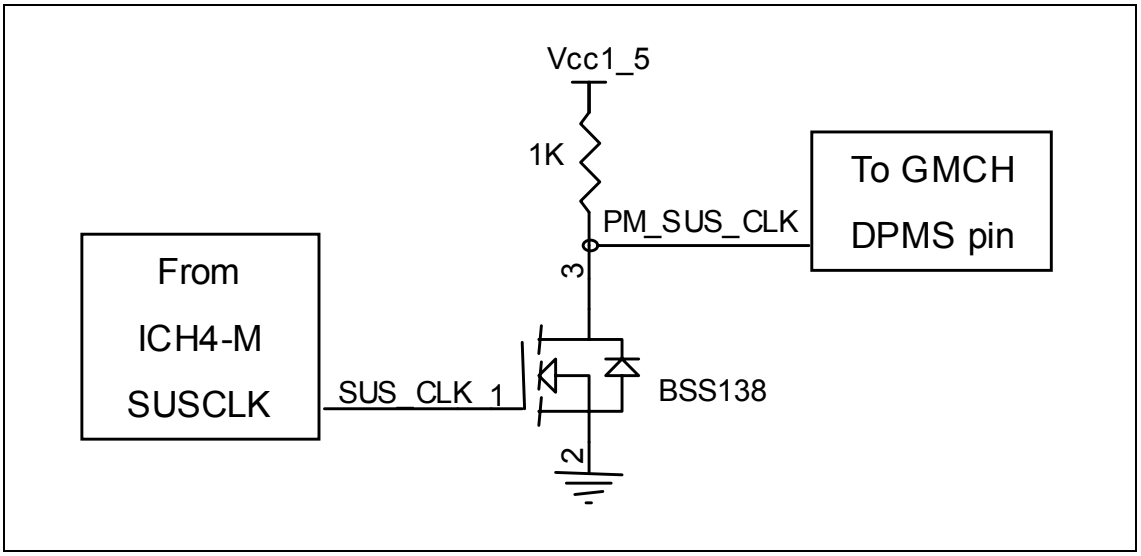
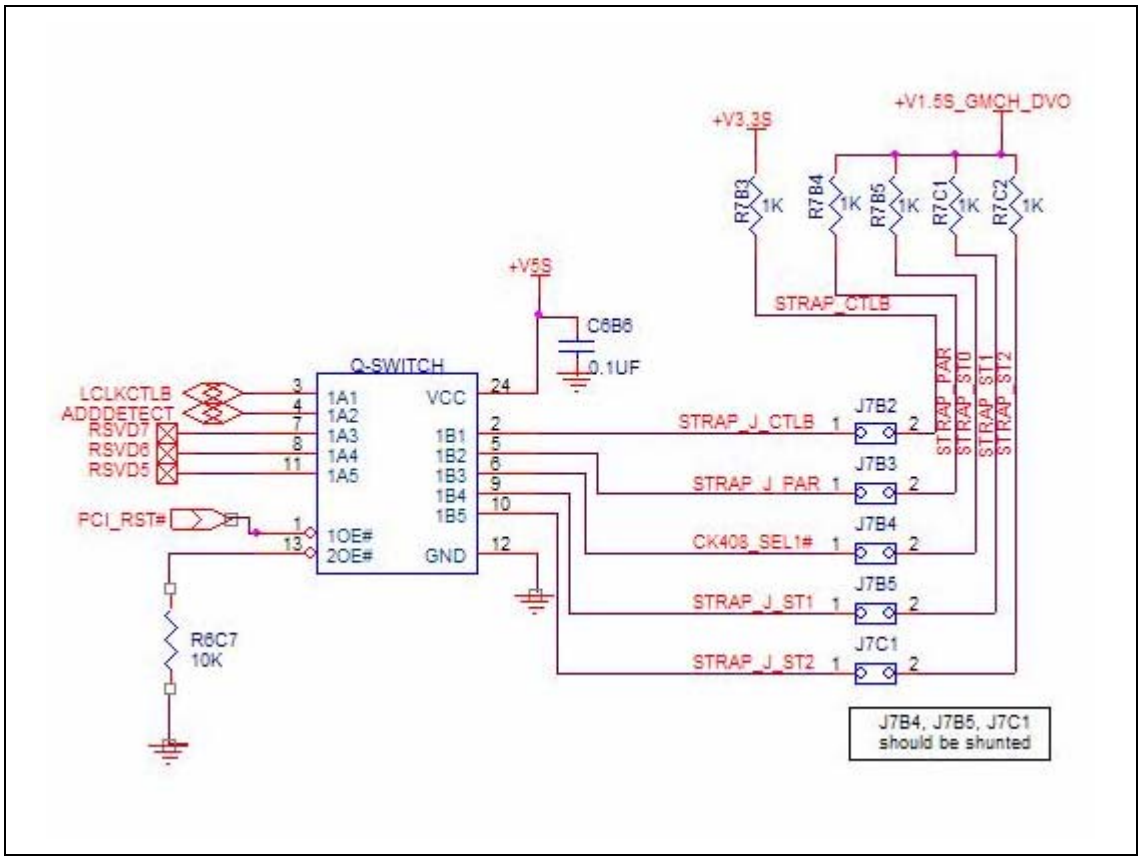


**Figure 116. Q-SWITCH Circuit**



### 14.8.4.3. DAC

| Pin Name | System Pull-up /Pull-down | In Series | Notes | ✓ |
|---|---|---|---|---|
| REFSET | 127 1% pull-down to gnd | | | ☐ |
| RED # | Connect to gnd | | Need to connect to RED's return path | ☐ |
| BLUE # | Connect to gnd | | Need to connect to BLUE's return path | ☐ |
| GREEN# | Connect to gnd | | Need to connect to GREEN's return path | ☐ |
| RED | On GMCH side of ferrite bead:<br>75 1% pull-down to gnd, 3.3 pF cap to gnd, ESD diode protection for Vcc1_5<br>On VGA side of ferrite bead:<br>3.3 pF cap to gnd | Ferrite bead: 75 at 100 MHz | Ferrite bead for EMI suppression between GMCH and VGA connector.<br>See latest Intel Customer Reference Schematics for more details.<br>When using external graphics, the 75 1% pull-down to gnd is not needed. | ☐ |
| BLUE | On GMCH side of ferrite bead:<br>75 1% pull-down to gnd, 3.3 pF cap to gnd, ESD diode protection for Vcc1_5<br>On VGA side of ferrite bead:<br>3.3 pF cap to gnd | Ferrite bead: 75 at 100 MHz | Ferrite bead for EMI suppression between GMCH and VGA connector.<br>See lastest Intel Customer Reference Schematics for more details.<br>When using external graphics, the 75 1% pull-down to gnd is not needed. | ☐ |
| GREEN | On GMCH side of ferrite bead:<br>75 1% pull-down to gnd, 3.3 pF cap to gnd, ESD diode protection for Vcc1_5<br>On VGA side of ferrite bead:<br>3.3 pF cap to gnd | Ferrite bead: 75 at 100 MHz | Ferrite bead for EMI suppression between GMCH and VGA connector.<br>See latest Intel Customer Reference Schematics for more details.<br>When using external graphics, the 75 1% pull-down to gnd is not needed. | ☐ |
| HSYNC | | 39 | Connect to unidirectional buffer to prevent potential electrical overstress and illegal operation of the GMCH.<br>See lastest Intel Customer Reference Schematics for more details. | ☐ |
| VSYNC | | 39 | Connect to unidirectional buffer to prevent potential electrical overstress and illegal operation of the GMCH.<br>See lastest Intel Customer Reference Schematics for more details. | ☐ |

## 14.8.5. Miscellaneous

| Pin Name | System Pull-up/Pull-down | Notes | ✓ |
|---|---|---|---|
| EXTTS | 10 k 1% pull-up to Vcc3_3 | | ☐ |
| DPWR# (pin AA22) | | No Connect | ☐ |
| LCLKCTLB | | | ☐ |
| LCLKCTLA | | Leave as NC if not used. | ☐ |
| GST2, GST1, GST0 | Leave as NC or 1K pull-up to Vcc1_5 | These pins have internal pull-down.<br>Future 852GME/852GMV/852PMdesigns only need GST2 to strap the FSB frequency to 400 MHz or 533 MHz. GST0 and GST1 may be left as NC.<br>Current 852GME/852GMV/852PMdesigns may still use the GST configurations in Table 105. | ☐ |

**Table 105. GST[2:0] Configurations**

| Straps Read Through HPLLCC[2:0] | FSB Frequency | System Memory Frequency | GFX Core Clock - Low | GFX Core Clock - High | Config # |
|---|---|---|---|---|---|
| 000 | 400 MHz | 266 MHz | 133 MHz | 200 MHz | 0 |
| 001 | 400 MHz | 200 MHz | 100 MHz | 200 MHz | 1 |
| 010 | 400 MHz | 200 MHz | 100 MHz | 133 MHz | 2 |
| 011 | 400 MHz | 266 MHz | 133 MHz | 266 MHz | 3 |
| 100 | 533 MHz | 266 MHz | 133 MHz | 200 MHz | 4 |
| 101 | 533 MHz | 266 MHz | 133 MHz | 266 MHz | 5 |
| 110 | 533 MHz | 333 MHz | 166 MHz | 266 MHz | 6 |
| 111 | 400 MHz | 333 MHz | 166 MHz | 250 MHz | 7 |

## 14.8.6. GMCH Decoupling Recommendations

| Pin Name | Configuration | F | Qty | Notes | ✓ |
|---|---|---|---|---|---|
| VCC[17:0] | Connect to Vcc1_5S | 0.1 µF<br>150 µF<br>10 µF | 4<br>2<br>1 | Bulk decoupling is based on VR solutions used on CRB design. | ☐ |
| VTTLF[20:0] | Connect to VCC | 0.1 µF<br>150 µF<br>10 µF | 2<br>1<br>1 | Bulk decoupling is based on VR solutions used on CRB design. | ☐ |
| VTTHF[4:0] | | 0.1 µF | 5 | Connect pins directly to caps. | ☐ |
| VCCHL[7:0] | Connect to Vcc1_5S | 0.1 µF<br>10 µF | 2<br>1 | Bulk decoupling is based on VR solutions used on CRB design. | ☐ |
| VCCSM[36:0] | Connect to VccSus2_5 | 0.1 µF<br>150 µF | 11<br>2 | Bulk decoupling is based on VR solutions used on CRB design. | ☐ |
| VCCQSM[1:0] | Connect to VccSus2_5 with filter network | 0.1 µF<br>4.7 µF+1 | 1<br>1 each | 0.68 uH from power supply to GMCH pins. On GMCH side of inductor: one 0.1 µF to GND, 4.7 µF + 1 to GND | ☐ |
| VCCASM[1:0] | Connect to Vcc1_5S with filter network | 0.1 µF<br>100 µF | 1<br>1 | 1 uH from power supply to GMCH pins, with caps on GMCH side of inductor. | ☐ |
| VCCAGP/VCCDVO[15:0] | Connect to Vcc1_5 | 0.1 µF<br>10 µF<br>150 µF | 2<br>1<br>1 | Bulk decoupling is based on VR solutions used on CRB design. | ☐ |
| VCCADAC[1:0] | Connect to Vcc1_5 | 0.01 µF<br>0.1 µF<br>220 µF (no stuff) | 1<br>1<br>1 | Route VSSADAC to other side of the caps, then to ground.<br>A 0-ohm 0805 resisor is recommended between the caps and Vcc1_5. This and the 220 µF cap footprints are there in case there is noise issue with the VGA supply. | ☐ |
| VCCALVDS | Connect to Vcc1_5 | 0.1 µF<br>0.01 µF | 1<br>1 | Route VSSALVDS to other side of the caps, then to ground. | ☐ |
| VCCDLVDS[3:0] | Connect to Vcc1_5 | 0.1 µF<br>22 µF<br>47 µF | 1<br>1<br>1 | Bulk decoupling is based on VR solutions used on CRB design. | ☐ |
| VCCTXLVDS[3:0] | Connect to VccSus2_5 | 0.1 µF<br>22 µf<br>47 µF | 3<br>1<br>1 | Bulk decoupling is based on VR solutions used on CRB design.<br>This power signal may be optionally connected to Vcc2_5 and powered off in S3. | ☐ |
| VCCGPIO | Connect to Vcc3_3 | 0.1 µF<br>10 µF | 1<br>1 | Bulk decoupling is based on VR solutions used on CRB design. | ☐ |
| VCCAHPLL | Connect to VCC1_5S | 0.1 µF | 1 | | ☐ |
| VCCAGPLL | Connect to VCC1_5S | 0.1 µF | 1 | | ☐ |

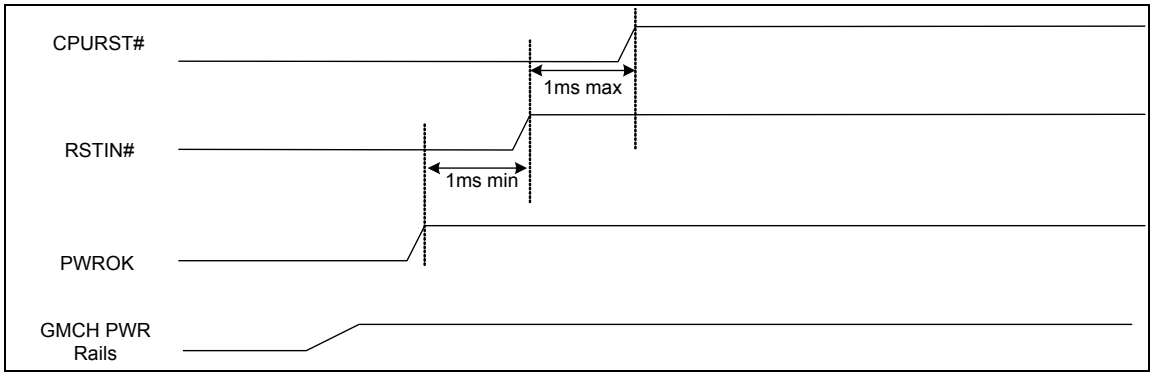
| Pin Name | Configuration | F | Qty | Notes | ✓ |
|---|---|---|---|---|---|
| VCCADPLLA | Connect to VCC1_5S with filter network | 0.1 µF<br>220 µF | 1<br>1 | 0.1 µH from power supply to GMCH pins, with caps on GMCH side of inductor. | ☐ |
| VCCADPLLB | Connect to VCC1_5S with filter network | 0.1 µF<br>220 µF | 1<br>1 | 0.1 µH from power supply to GMCH pins, with caps on GMCH side of inductor. | ☐ |

**NOTE:** Decoupling guidelines are recommendations based on our reference board design. Customers will need to take layout and PCB board design into consideration when deciding on overall decoupling solution.

## 14.8.7. GMCH Power-up Sequence

| Timing Parameters | Min | Max | Unit | Notes | ✓ |
|---|---|---|---|---|---|
| PWROK active to RSTIN# inactive. | 1 | | ms | Please refer to the *Intel® 852GME Chipaer GMCH and Intel® 852PM Chipset MCH Datasheet*. | ☐ |
| RSTIN# inactive to CPURST# inactive. | | 1 | ms | Please refer to *Intel® 852GME Chipaer GMCH and Intel® 852PM Chipset MCH Datasheet*. | ☐ |

**Figure 117. 852GME Power-up Sequence**



## 14.9. ICH4-M Checklist

***Note:*** All inputs to the ICH4-M must not be left floating. Many GPIO signals are fixed inputs that must be pulled up to different sources.

### 14.9.1. PCI Interface and Interrupts

| Pin Name | System Pull-up /Pull-down | Notes | ✓ |
|---|---|---|---|
| PCI_DEVSEL# | 8.2 k pull-up to Vcc3_3 | | ☐ |
| PCI_FRAME# | 8.2 k pull-up to Vcc3_3 | | ☐ |
| PCI_GPIO0 / REQA#<br>PCI_GPIO1 / REQB_L/REQ5# | 8.2 k pull-up to Vcc3_3 | Each signal requires a pull-up resistor. | ☐ |
| PCI_GPIO16 / GNTA# | | GNTA is also used as a strap for “top block swap”. It is sampled on the rising edge of PWROK. By default, this signal is HIGH (strap function DISABLED). It can be enabled by a pull-down to gnd through a 1- k resistor. | ☐ |
| PCI_IRDY# | 8.2 k pull-up to Vcc3_3 | | ☐ |
| PCI_LOCK# | 8.2 k pull-up to Vcc3_3 | | ☐ |
| PCI_PERR# | 8.2 k pull-up to Vcc3_3 | | ☐ |
| PCI_SERR# | 8.2 k pull-up to Vcc3_3 | | ☐ |
| PCI_STOP# | 8.2 k pull-up to Vcc3_3 | | ☐ |
| PCI_TRDY# | 8.2 k pull-up to Vcc3_3 | | ☐ |
| PCI_REQ[4:0]# | 8.2 k pull-up to Vcc3_3 | Each signal requires a pull-up resistor. | ☐ |
| PCI_PME# | | ICH4-M has internal pull-up to VccSus3_3. | ☐ |
| PCI_RST# | 8.2 k k pull-up to Vcc3_3 | | ☐ |
| APICCLK | Pull down to GND (If NOT Used) | | ☐ |
| APICD[1:0] | 10 k pull-down to gnd (If NOT Used) | If XOR chain testing is **NOT** used: Pull down the signals through a shared 10-kohm resistor, if NOT USED.<br>If XOR chain testing is used: Each signal requires a separate 10K pull-down resistor. | ☐ |
| INT_IRQ[15:14] | 8.2 k pull-up to Vcc3_3 | Each signal requires a pull-up resistor. | ☐ |
| INT_PIRQ#[A:D]<br>INT_PIRQE#/GPIO2<br>INT_PIRQF#/GPIO3<br>INT_PIRQG#/GPIO4 | 8.2 k pull-up to Vcc3_3 | External pull up is required for INT_PIRQ#[A:D]. External pull up is required when muxed signal (INT_PIRQ[E:H]#/ GPIO[2:5]) is | ☐ |

| Pin Name | System Pull-up /Pull-down | Notes | ✓ |
|---|---|---|---|
| INT_PIRQH#/GPIO5 | | implemented as PIRQ. | |
| INT_SERIRQ | 8.2 k pull-up to Vcc3_3 | | ☐ |

## 14.9.2. GPIO

***Note:*** Ensure ALL unconnected signals are OUTPUTS ONLY. GPIO[7:0] are 5-V tolerant.

| Recommendations | ✓ |
|---|---|
| **GPIO[7] & [5:0]:**<br>These pins are in the Main Power Well. Pull-ups must use the $V_{CC}3_3$ plane.<br>Unused core well inputs must be pulled up to $V_{CC}3_3$.<br>GPIO[1:0] can be used as REQ[B:A]#.<br>GPIO[1] can be used as PCI REQ[5]#.<br>GPIO[5:2] can be used as PIRQ[H:E]#.<br>These signals are 5 V tolerant.<br>These pins are inputs. | ☐ |
| **GPIO[8] & [13:11]:**<br>These pins are in the Resume Power Well. Pull-ups go to $V_{CC}Sus3_3$ plane.<br>Unused resume well inputs must be pulled up to $V_{CC}Sus3_3$.<br>These are the only GPIs that can be used as ACPI compliant wake events.<br>These signals are not 5V tolerant.<br>GPIO[8] can be used as SMC_EXTSMI#<br>GPIO[11] can be used as SMBALERT#.<br>GPIO[13] can be used as SMC_WAKE_SCI#<br>These pins are inputs | ☐ |
| **GPIO[23:16]:**<br>Fixed as output only. Can be left NC.<br>In Main Power Well ($V_{CC}3_3$).<br>GPIO[17:16] can be used as GNT[B:A]#.<br>GPIO[17] can be used as PCI GNT[5]#.<br>STP_PCI#/GPIO[18] – used in Mobile as STP_PCI# only.<br>SLP_S1#/GPIO[19] - used in Mobile as SLP_S1# only.<br>STP_CPU#/GPIO[20] - used in Mobile as STP_CPU# only.<br>C3_STAT#/GPIO[21] - used in Mobile as C3_STAT# only.<br>CPUPERF#/GPIO[22] - open drain signal. Used in Mobile as CPUPERF# only.<br>SSMUXSEL/GPIO[23] - used in Mobile as SSMUXSEL only. | ☐ |
| **GPIO[28,27,25,24]:**<br>I/O pins. Default as outputs. Can be left as NC.<br>These pins are in the Resume Power Well.<br>CLKRUN#/GPIO[24] (Note: use $V_{CC}3_3$ if signal is required to be pulled-up)<br>GPIO[28, 27, 25] From resume power well ($V_{CC}Sus3_3$). (Note: use $V_{CC}3_3$ if this signal is required to be pulled-up)<br>These signals are NOT 5-V tolerant.<br>GPIO[25] can be used as AUDIO_PWRDN. | ☐ |
| **GPIO[43:32]:**<br>I/O pins. From main power well ($V_{CC}3_3$).<br>Default as outputs when enabled as GPIOs.<br>These signals are **NOT** 5-V tolerant.<br>GPIO[32] can be used as AGP_SUSPEND#.<br>GPIO[33] can be used as KSC_VPPEN#.<br>GPIO[34] can be used as SER_EN.<br>GPIO[35] can be used as FWH_WP#.<br>GPIO[36] can be used as FWH_TBL#.<br>GPIO[40] can be used as IDE_PATADET.<br>GPIO[41] can be used as IDE_SATADET. | ☐ |

## 14.9.3. AGP_BUSY# Design Requirement

| Signal | System Pull-up/Pull-down | Notes | ✓ |
|---|---|---|---|
| AGPBUSY#/GPIO6 | 10 k pull-up to Vcc3_3 | This ICH4-M signal requires a pull-up to the switched 3.3-V rail (powered OFF during S3).<br>This ICH4-M signal must be connected to the AGP_BUSY# output of GMCH.<br>When using external graphics, AGP_BUSY# may be left as NC to the GMCH. | ☐ |

**NOTE:** Please also consult Intel for the latest AGP Busy and Stop signal implementation.

## 14.9.4. (SMBus) System Management Interface

| Pin Name | System Pull-up/Pull-down | Notes | ✓ |
|---|---|---|---|
| SM_INTRUDER# | 100 k pull-up to VccRTC | RTC well input requires pull-up (10 k-100 k) to reduce leakage from coin cell battery in G3. | ☐ |
| SMB_ALERT#/ GPIO[11] | 10 k pull-up to V3ALWAYS | | ☐ |
| SMBCLK, SMBDATA, SMLINK[1:0] | Pull-up to V3ALWAYS | Require external pull-up resistors. Pull up value is determined by bus characteristics. CRB schematics use 10-k pull-up resistors.<br>The SMBus and SMLink signals must be connected together externally in S0 for SMBus 2.0 compliance: SMBCLK connected to SMLink[0] and SMBDATA connected to SMLink[1]. | ☐ |

## 14.9.5. AC ’97 Interface

| Pin Name | System Pull-up/Pull-down | Series Termination Resistor | Notes | ✓ |
|---|---|---|---|---|
| AC_BIT_CLK | None | 33-47 | The internal pull-down resistor is controlled by the AC’97 Global Control Register, ACLINK Shut Off bit:<br>1 = enabled; 0 = disabled<br>When no AC'97 devices are connected to the link, BIOS must set the ACLINK Shut Off bit for the internal keeper resistors to be ENABLED. At that point, pull-ups/pull-downs are NOT needed on ANY of the link signals. | ☐ |
| AC_SDATAIN[2:0] | None | 33-47 | A series termination resistor is required for the PRIMARY CODEC.<br>A series termination resistor is required for the SECONDARY and TERTIARY CODEC if the resistor is not found on CODEC. | ☐ |
| AC_SDATAOUT | None | 33-47 | A series termination resistor is required for the PRIMARY CODEC.<br>One series termination resistor is required for the SECONDARY/ TERTIARY CODEC connector card if the resistor is not found on the connector card. | ☐ |
| AC_SYNC | None | 33-47 | A series termination resistor is required for the PRIMARY CODEC.<br>One series termination resistor is required for the SECONDARY/ TERTIARY CODEC connector card if the resistor is not found on the connector card. | ☐ |

## 14.9.6. ICH4-M Power Management Interface

| Pin Name | System Pull-up/Pull-down | Notes | ✓ |
|---|---|---|---|
| PM_DPRSLPVR | | Signal has integrated pull-down in ICH4-M. | ☐ |
| PM_SLP_S1#/GPIO19<br>PM_SLP_S3#,<br>PM_SLP_S4#,<br>PM_SLP_S5# | | Signals driven by ICH4-M. | ☐ |
| PM_BATLOW# | 10-k pull-up to V3ALWAYS<br>IF NOT USED | Pull up is not required if it is used. However, signal must not float if it is NOT being used | ☐ |
| PM_CLKRUN# | 10-k pull-up to Vcc3_3 | | ☐ |
| PM_PWRBTN# | | Has integrated pull-up of 18 k – 42 k | ☐ |
| PM_PWROK | Weak pull-down to gnd | RTC well input requires pull-down to reduce leakage from coin cell battery in G3. Input must not float in G3.<br>This signal should be connected to power monitoring logic and should go high no sooner than 10 ms after both Vcc3_3 and Vcc1_5 have reached their nominal voltages. CRB uses 100 k pull-down. | ☐ |
| PM_RI# | 10-k pull-up to V3ALWAYS | If this signal is enabled as a wake event, it needs to be powered during a power loss event. If this signal goes low (active), when power returns the RI_STS bit will be set and the system will interpret that as a wake event. | ☐ |
| PM_RSMRST# | Weak pull-down to gnd | RSMRST# is a RTC well input and requires pull-down to reduce leakage from coin cell battery in G3. Input must not float in G3.<br>This signal should be connected to power monitoring logic and should go high no sooner than 10 ms after both Vcc3_3 and Vcc1_5 have reached their nominal voltages. CRB uses 100 K pull-down.<br>Timing Requirement: See LAN_RST#. | ☐ |
| PM_THRM# | 8.2 k Pull-up to Vcc3_3<br>If TEMP SENSOR not sued | External pull-up not required if connecting to temperature sensor. | ☐ |
| PM_SYSRST# | 10 k pull-up to V3ALWAYS if not actively driven. | This signal to ICH4-M should not float. It needs to be at valid level all the time. | ☐ |

## 14.9.7. FWH/LPC Interface

| Pin Name | System Pull-up/Pull-down | Notes | ✓ |
|---|---|---|---|
| LPC_AD[3:0] | | No extra pull-ups required. Connect straight to FWH/LPC. | ☐ |

## 14.9.8. USB Interface

| Pin Name | System Pull-up/Pull-down | Notes | ✓ |
|---|---|---|---|
| USB_OC[5:0]# | 10 k pull-up to V3ALWAYS if not driven | No pull-up is required if signalsl are driven.. Signals must NOT float if they are not being used. | ☐ |
| USBRBIAS, USBRBIAS# | 22.6 ± 1% pull-down to gnd | Connect signals together and pull down through a common resistor, placed within 500 mils of the ICH4-M. Avoid routing next to clock pin. | ☐ |

## 14.9.9. Hub Interface

| Pin Name | System Pull-up/Pull-down | Notes | ✓ |
|---|---|---|---|
| HUB_RCOMP | 48.7 1% pull-up to to Vcc1_5 | Place resistor within 0.5” of ICH4-M pad using a thick trace. | ☐ |
| HUB_VREF, HUB_VSWING | Please refer to Figure 118 and Figure 119 and Figure 120 | HUB_VREF signal voltage level = 0.35 V ± 8%. HUB_VSWING signal voltage level = 0.80 V ± 8%. Three options are available for generating these references. | ☐ |
| HUB_PD11 | 56 pull-down to gnd | | ☐ |

**Figure 118. Separated GMCH and ICH4-M VSWING/VREF Reference Voltage Circuit**

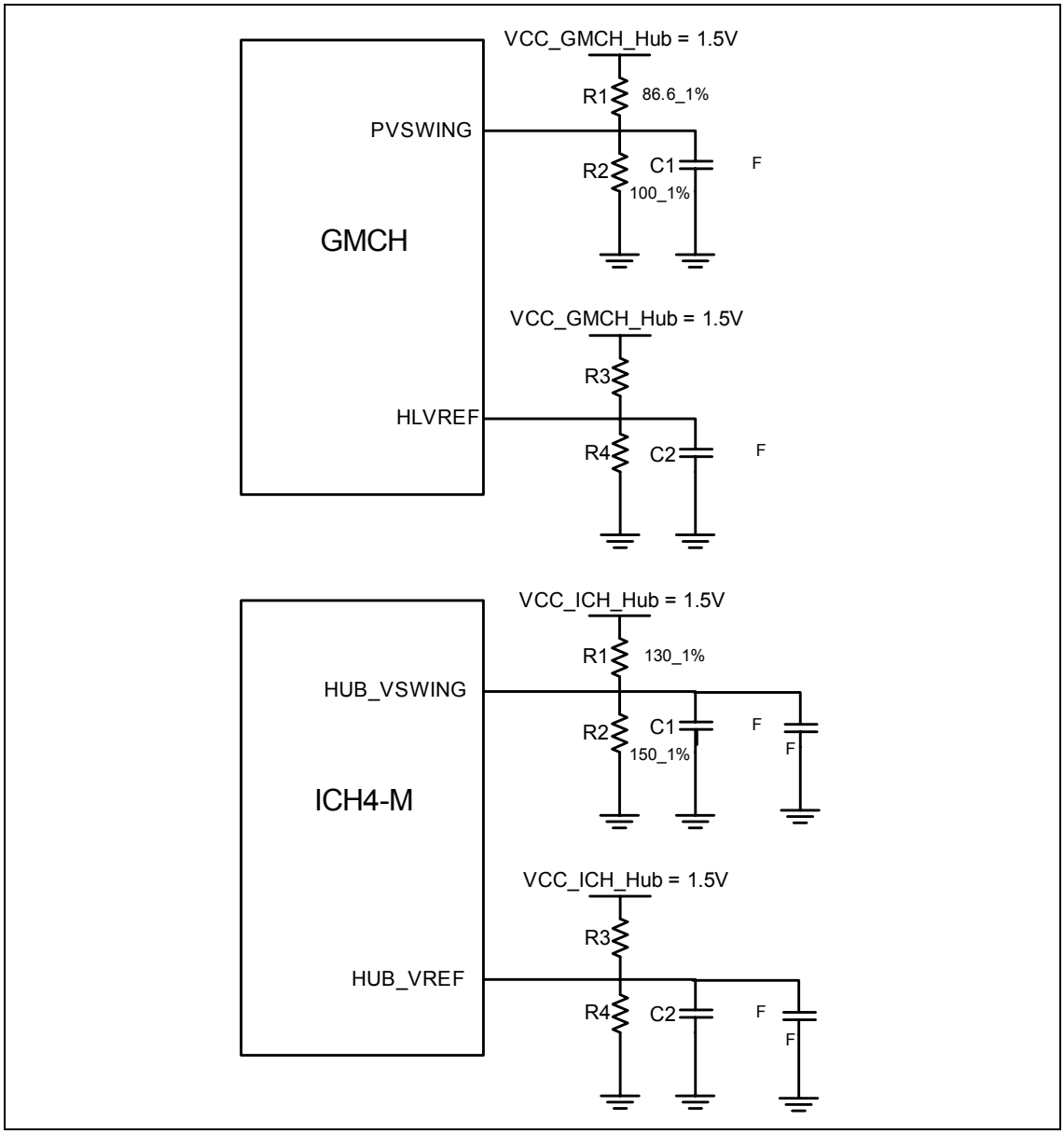


**Figure 119. Single or Locally Generated GMCH & ICH4-M HIVREF/HI_VSWING Circuit**

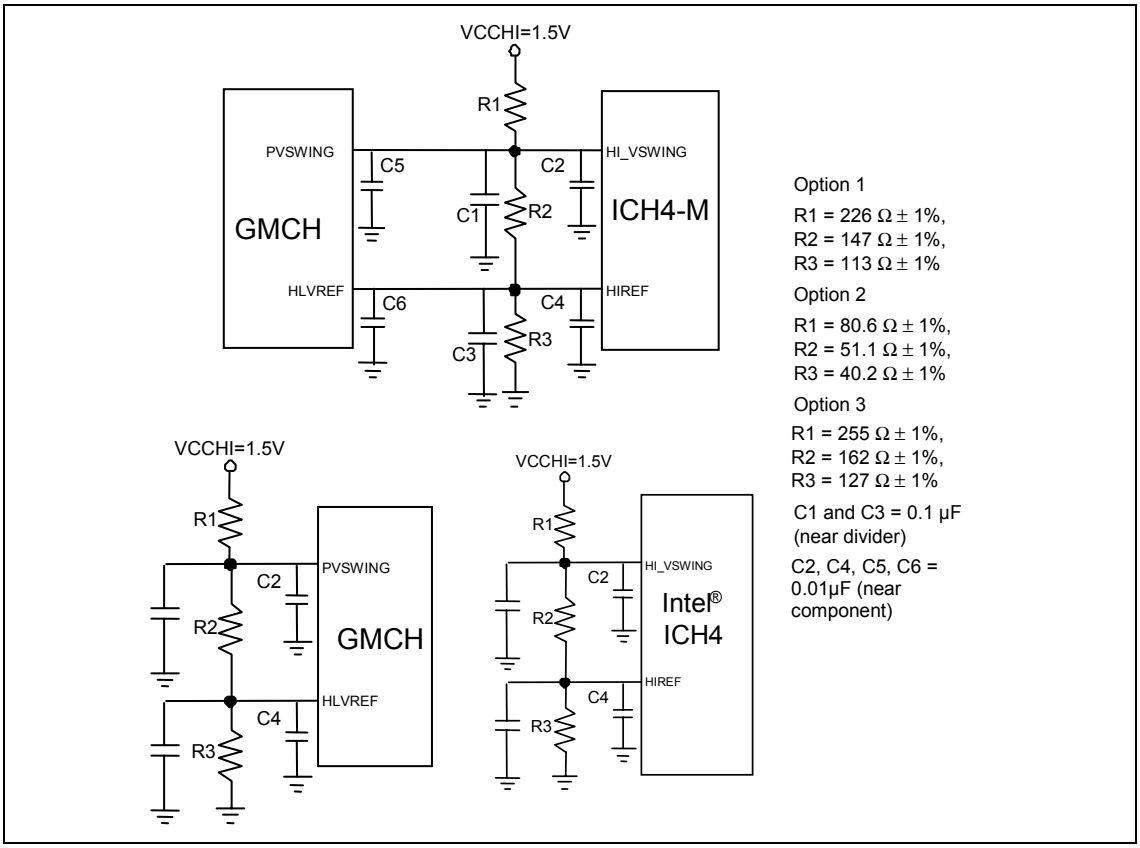
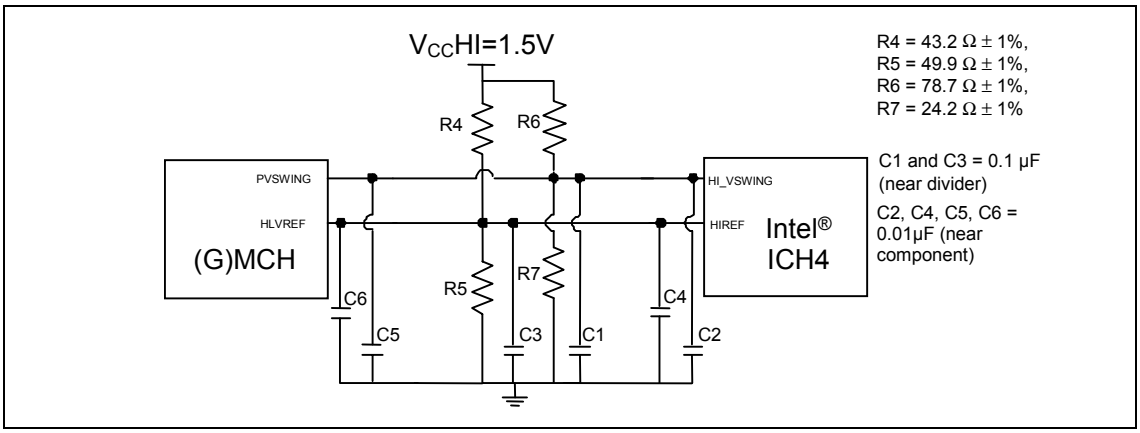



**Figure 120. Single Generated GMCH and ICH4-M VSWING/VREF Reference Voltage/ Local Voltage Divider Circuit for VSWING/VREF**

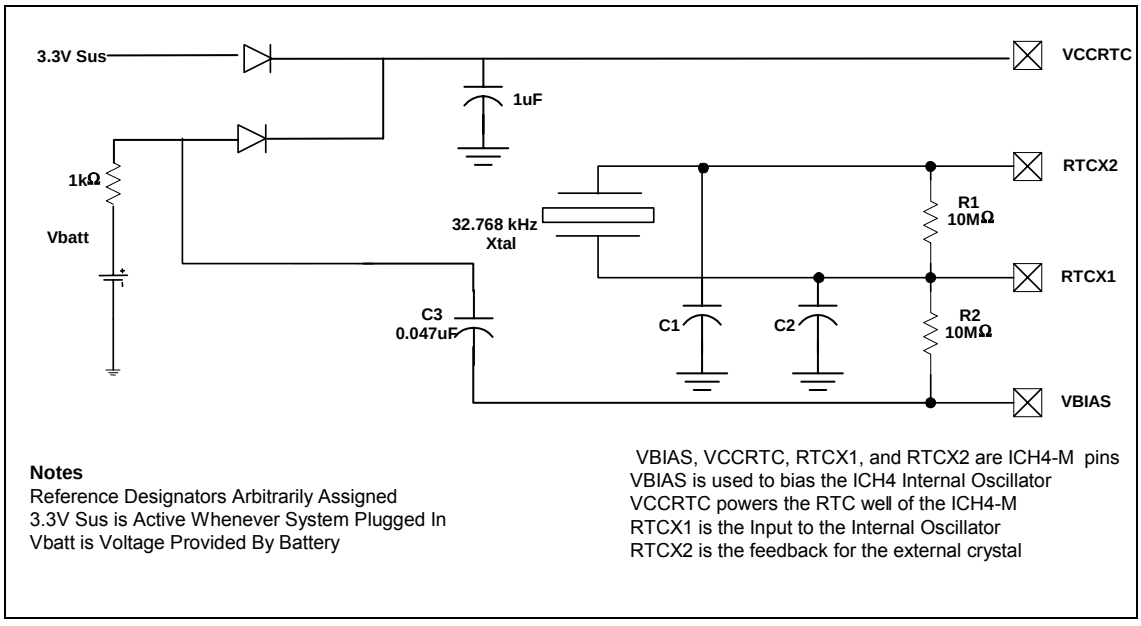


## 14.9.10. RTC Circuitry

| Pin Name | System Pull-up/Pull-down | In Series | Notes | ✓ |
|---|---|---|---|---|
| RTCRST# | 180 k pull-up to VccRTC | | RTCRST# requires 18-25 ms delay. Use a 0.1-µF cap to ground Pull up with 180-k resistor. Any resistor or capacitor combination that yields a time constant is acceptable. | ☐ |
| CLK_RTCX1, CLK_RTCX2 | | | Connect a 32.768-kHZ crystal oscillator across these pins with a 10-M resistor and a decoupling cap at each signal. Values for C1 and C2 are dependent on crystal.<br>See Figure 121. Note 1 | ☐ |
| CLK_VBIAS | | 1 k<br>0.047 µF | Connect to CLK_RTCX1 through a 10-M resistor. Connect to VBATT through a 1 k in series with a 0.047-µF capacitor. Note 2 | ☐ |

**NOTES:**
1. Voltage Swing on RTCX1 pin should not exceed 1.0 V.
2. Recommendation for VBIOS 200 mV-350 mV.

**Figure 121. External Circuitry for the RTC**



## 14.9.11. LAN Interface

| Pin Name | System Pull-up/Pull-down | Notes | ✓ |
|---|---|---|---|
| LAN_JCLK | | Connect to LAN_CLK on the platform LAN Connect Device. If LAN interface is not used, leave the signal unconnected (NC). | ☐ |
| LAN_RST# | 10-k pull-down to gnd<br>If ICH4-M LAN not used | Timing Requirement: Signal should be connected to power monitoring logic, and should go high no sooner than 10 ms after both VccSus3_3 and VccSus1_5 have reached their nominal voltages.<br>**NOTE**: If ICH4-M LAN controller is NOT used, pull LAN_RST# down through a 10-k resistor. | ☐ |
| LAN_RXD[2:0], LAN_TXD[2:0] | | Connect to LAN_RXD on the platform LAN Connect Device.<br>If LAN interface is not used, leave the signal unconnected (NC) | ☐ |
| LAN_RSTYSNC | | Connect to LAN_RSTSYNC on Platform LAN Connect Devce.<br>If LAN interface is not used, leave the signal unconnected (NC). | ☐ |

## 14.9.12. Primary IDE Interface

| Pin Name | System Pull-up/Pull-down | Series Damping | Notes | ✓ |
|---|---|---|---|---|
| IDE_PDD[15:0] | | | These signals have integrated series resistors. | ☐ |
| IDE_PDA[2:0], IDE_PDCS1#, IDE_PDCS3#, IDE_PDDACK#, IDE_PDIOW#, IDE_PDIOR# | | | These signals have integrated series resistors. Pads for series resistors can be implemented should the system designer have signal integrity concerns. | ☐ |
| IDE_PDDREQ | | | These signals have integrated series resistors and pull-down resistors in ICH4-M. | ☐ |
| IDE_PIORDY | 4.7K pull-up to Vcc3_3 | | This signal has integrated series resistor in ICH4-M. | ☐ |
| IDE_PRST# | | 22-47 | The signal must be buffered to provide IDE_RST# for improved signal integrity. | ☐ |

## 14.9.13. Secondary IDE Interface

| Pin Name | System Pull-up/Pull-down | Series Damping | Notes | ✓ |
|---|---|---|---|---|
| IDE_SDD[15:0] | | | These signals have integrated series resistors. | ☐ |
| IDE_SDA[2:0], IDE_SDCS1#, IDE_SDCS3#, IDE_SDDACK#, IDE_SDIOW#, IDE_SDIOR# | | | These signals have integrated series resistors. Pads for series resistors can be implemented should the system designer have signal integrity concerns. | ☐ |
| IDE_SDDREQ | | | These signals have integrated series resistors and pull-down resistors in ICH4-M. | ☐ |
| IDE_SIORDY | 4.7 k pull-up to Vcc3_3 | | This signal has integrated series resistor in ICH4-M. | ☐ |
| IDE_SRST# | | 22-47 | The signal must be buffered to provide IDE_RST# for improved signal integrity.. | ☐ |

## 14.9.14. Miscellaneous Signals

| Pin Name | System Pull-up/Pull-down | Notes | ✓ |
|---|---|---|---|
| SPKR | | SPKR is a strapping option for the TCO Timer Reboot function and is sampled on the rising edge of PWROK. An integrated weak pull-down is enabled only at boot/reset. Status of strap is readable via the NO_REBOOT bit (D31:F0, Offset D4h, bit 1)<br>1 = disabled; 0 = enabled (normal operation)<br>To disable, a jumper can be populated to pull SPKR high. Value of pull-up must be such that the voltage divider output caused by the pull-up, effective impedance of speaker and codec circuit, and internal pull-down will be read as logic high (0.5 * Vcc3_3 to Vcc3_3 + 0.5) | ☐ |

## 14.9.15. ICH4-M Decoupling Recommendations

| Pin Name | Configuration | Value | Q | Notes | ✓ |
|---|---|---|---|---|---|
| VCC1.5 | Connect to Vcc1_5 | 0.1 µF | 2 | Low frequency decoupling is dependent on layout and power supply design. CRB uses one 22 µF and one 100 µF. | ☐ |
| VCC3.3 | Connect to Vcc3_3 | 0.1 µF | 6 | Low frequency decoupling is dependent on layout and power supply design. CRB uses two 22 µF. | ☐ |
| VCCSUS1.5 | Connect to V1_5ALWAYS | 0.1 µF | 2 | Low frequency decoupling is dependent on layout and power supply design. CRB uses one 10 µF. | ☐ |
| VCCSUS3.3 | Connect to V3ALWAYS | 0.1 µF | 2 | Low frequency decoupling is dependent on layout and power supply design. CRB uses one 22 µF. | ☐ |
| VCCLAN1.5 | Connect to VccSus1_5 | 0.1 µF | 2 | Low frequency decoupling is dependent on layout and power supply design. CRB uses one 22 µF. | ☐ |
| VCCLAN3.3 | Connect to VccSus3_3 | 0.1 µF<br>4.7 µF | 2<br>1 | Low frequency decoupling is dependent on layout and power supply design. CRB uses one 22 µF. | ☐ |
| VCC5REF | Connect to Vcc5 through 1 k | 0.1 µF<br>1 µF | 1<br>1 | Caps from VCC5REF to ground. Also connect diode from VCC5REF to Vcc3_3. | ☐ |
| VCC5REFSUS | Connect to V5ALWAYS through 1 k | 0.1 µF<br>1 µF | 1<br>1 | Caps from VCC5REFSUS to ground. Also connect diode from VCC5REFSUS to V3ALWAYS. Please refer to latest Platform RDDP for the implementaion. | ☐ |
| VCC_CPU_IO | Connect to VCC | 0.1 µF<br>1 µF | 1<br>1 | | ☐ |
| VCCLL | Connect to Vcc1_5 | 0.1 µF<br>0.01 µF | 1<br>1 | | ☐ |
| VCCRTC | Connect to VccRTC | 0.1 µF | 1 | | ☐ |
| VCCHI | Connect to Vcc1_5 | 0.1 µF | 2 | Low frequency decoupling is dependent on layout and power supply design. CRB uses one 22 µF. | ☐ |

**NOTE:** All decoupling guidelines are recommendations based on our reference board design. Customers will need to take their layout, and PCB board design into consideration when deciding on their overall decoupling solution. Capacitors should be place less than 100 mils from the package.

## 14.9.16. ICH4-M Power-up Sequence

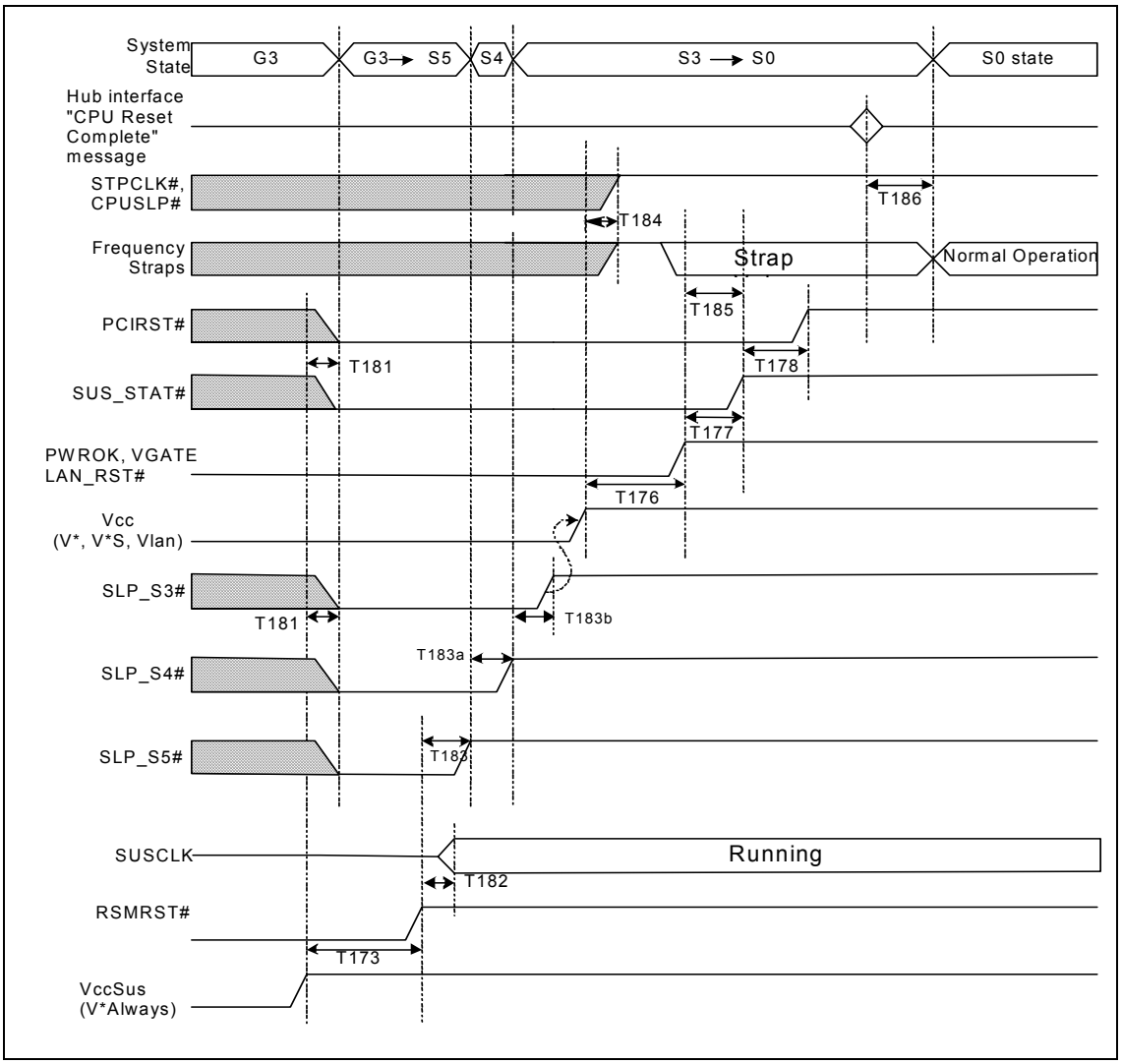
### Table 106. ICH4-M Power-up Timing Specifications

| Sym | Description | Min | Max | Units | Notes | ✓ |
|---|---|---|---|---|---|---|
| T173 | VccSus supplies active to LAN_RST#, RSMRST# inactive | 10 | - | ms | | ☐ |
| T176 | Vcc1.5, Vcc3.3, VccHI supplies active to PWROK, VGATE active | 10 | - | ms | 4 | ☐ |
| T177 | PWROK and VGATE active and SYS_RESET# inactive to SUS_STAT# inactive | 32 | 38 | RTCCLK | 2 | ☐ |
| T178 | SUS_STAT# inactive to PCIRST# inactive | 1 | 3 | RTCCLK | 2 | ☐ |
| T181 | VccSus active to SLP_S5#, SUS_STAT# and PCIRST# active | | 50 | ns | | ☐ |
| T182/T183 | RSMRST# inactive to SUSCLK running, SLP_S5# inactive | | 110 | ms | 1 | ☐ |
| T183a | SLP_S5# inactive to SLP_S4# inactive | 1 | 2 | RTCCLK | 2 | ☐ |
| T183b | SLP_S4# inactive to SLP_S3# inactive | 1 | 2 | RTCCLK | 2 | ☐ |
| T184 | Vcc_CPU_IO active to STPCLK#, CPUSLP# inactive, and CPU Frequency Strap signals high | | 50 | ns | | ☐ |
| T185 | PWROK and VGATE active and SYS_RESET# inactive to SUS_STAT# inactive and CPU Frequency Straps latched to strap values | 32 | 38 | RTCCLK | 2 | ☐ |
| T186 | CPU Reset Complete to Frequency Straps signals unlatched from strap values | 7 | 9 | CLK66 | 3 | ☐ |

**NOTES:**

1. If there is no RTC battery in the system, so VccRTC and the VccSus supplies come up together, the delay from RTCRST# and the RSMRST# inactive to SUSCLK toggling may be as much as 1000 ms.
2. These transitions are clocked off the internal RTC. 1 RTC clock is approximately 32 µs.
3. This transition is clocked off the 66-MHz CLK66. 1 CLK66 is approximately 15 ns.
4. It is not necessary for PWROK to be asserted before or after PM_VGATE is asserted. However, if PWROK is asserted after PM_VGATE, it must be delayed 3-10 ms from PWRGD from the VR (which enables clock). Similarly, if PM_VGATE is asserted after PWROK, it must be delayed 3-10 ms from PWRGD from the VR (which enables clock).
5. Please refer to ICH4-M for latest specifications.

**Figure 122. ICH4 Power-up Sequence Waveforms**



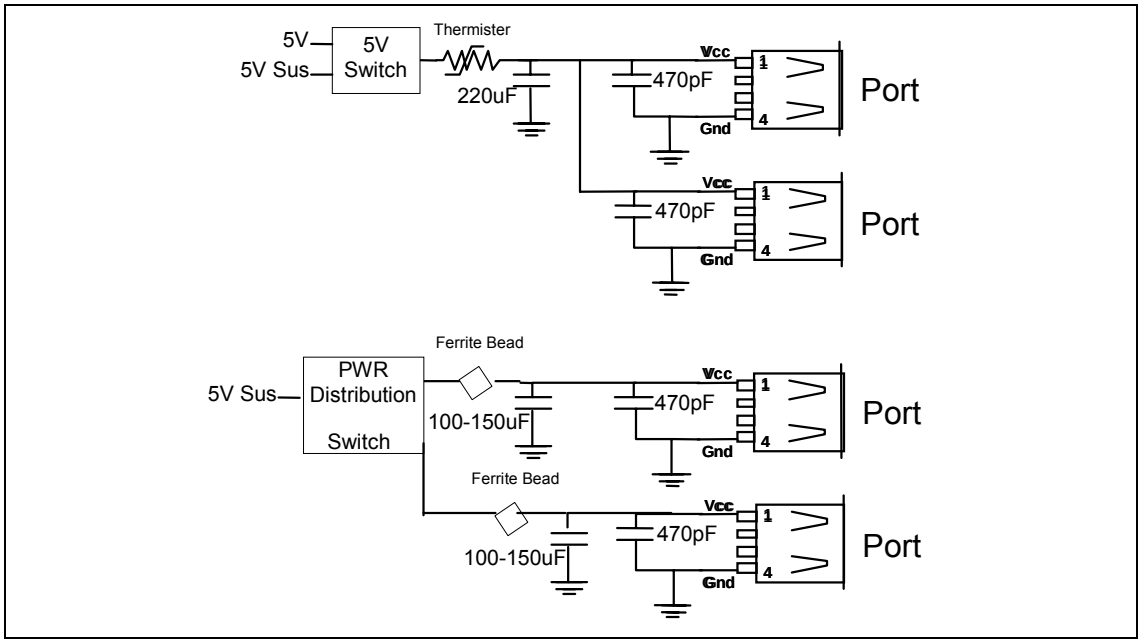

**NOTE:** It is not necessary for PWROK to be asserted before or after PM_VGATE is asserted. However, if PWROK is asserted after PM_VGATE, it must be delayed 3-10 ms from PWRGD from the VR (which enables clock). Similarly, if PM_VGATE is asserted after PWROK, it must be delayed 3-10 ms from PWRGD from the VR (which enables clock).

# 14.10. USB Power Checklist

## 14.10.1. Downstream Power Connection

| Pin Name | Notes | ✓ |
|---|---|---|
| USB_VCC[E:A] | One 220 µF and two 470 pF are recommended for every two power lines. Either a thermister or a power distribution switch (with short circuit and thermal protection) is required.<br>See Figure 123. | ☐ |

**Figure 123. Good Downstream Power Connection**



# 14.11. FWH Checklist

## 14.11.1. Resistor Recommendations

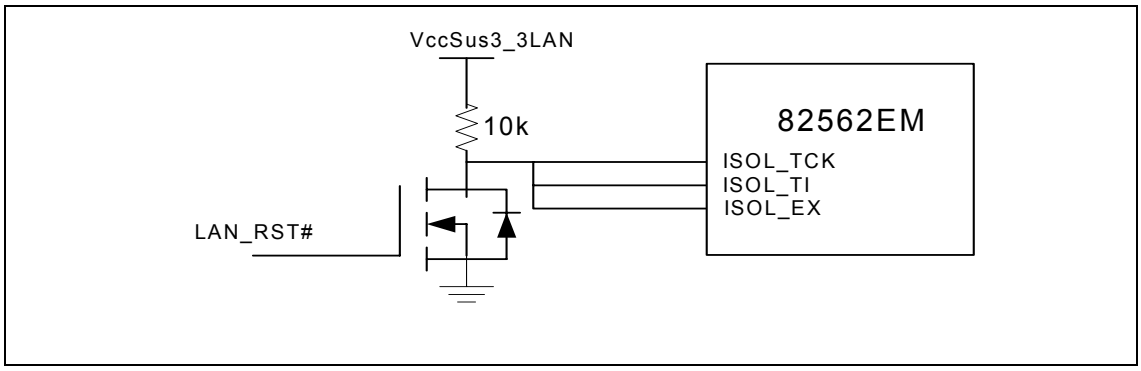
| Pin Name | System Pull-up/Pull-down | Series Damping | Notes | ✓ |
|---|---|---|---|---|
| FGPI[4:0] | 100 pull-down to gnd | | Each signal requires a 100 pull-down resistor. | ☐ |
| IC | 10 k pull-down to gnd | | | ☐ |
| RST# | | 100 | | ☐ |
| ID[3:0] | | | Signals are recommended to be connected to test points. | ☐ |
| RSVD[5:1] | | | Signals are recommended to be connected to test points. | ☐ |
| NC[8:1] | | | The signals should be left as NC (“Not Connected”) | ☐ |

# 14.12. LAN/HomePNA Checklist

## 14.12.1. Resistor Recommendations (for 82562ET / 82562 EM)

| Pin Name | System Pull-up/Pull-down | Term Resistor | Notes | ✓ |
|---|---|---|---|---|
| ISOL_EX, ISOL_TCK, ISOL_TI | 10 k pull-up to VccSus3_3LAN | | If LAN is enabled, all three signals needs to be pulled up to VccSus3_3LAN through a common 10-k pull-up resistor.<br>See Figure 124. | ☐ |
| RBIAS10 | 549 ± 1%pull-down to gnd | | | ☐ |
| RBIAS100 | 619 ± 1%pull-down to gnd | | | ☐ |
| RDP, RDN | | 121 ±1% | Connect 121-ohm resistor between RDP and RDN. | ☐ |
| TDP, TDN | | 100 ± 1% | Connect 100-ohm resistor between TDP and TDN. | ☐ |
| TESTEN | 100 pull-down to gnd | | | ☐ |
| X1, X2 | | | Connect a 25-MHz crystal across these two pins. 22 pF on each pin to ground. | ☐ |
| LAN_RST# | | | On CRB, the power monitoring logic waits for PM_PWROK to go high before deasserting this signal to enable the LAN device. It also keeps this signal high during S3.<br>See Figure 124. | ☐ |

**Figure 124. LAN_RST# Design Recommendation**



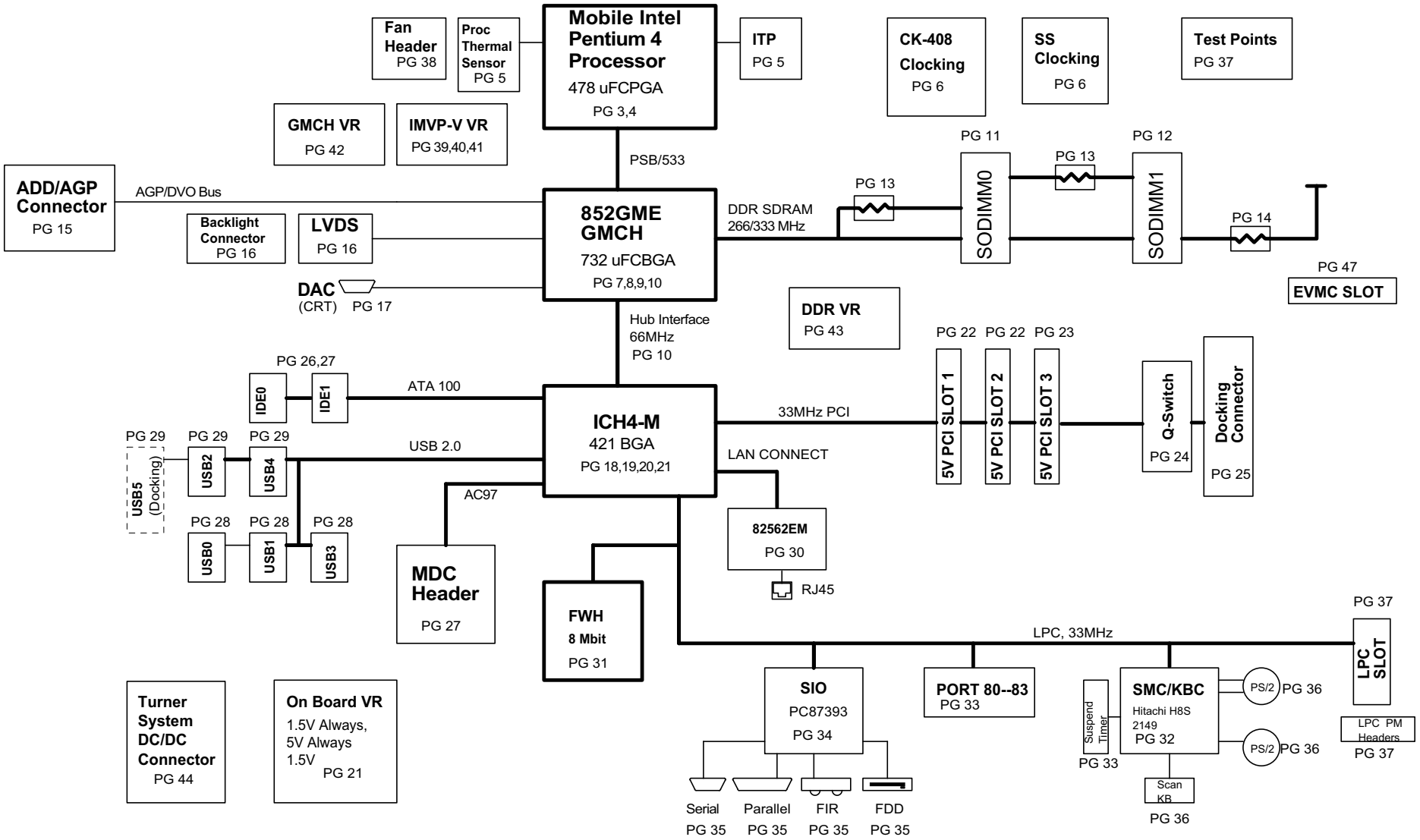

## 14.12.2. Decoupling Recommendations

| Signal Name | Configuration | F | Qty | Notes | ✓ |
|---|---|---|---|---|---|
| VCC[2:1],<br>VCC[2:1],<br>VCCA[2:1],<br>VCCT[4:1] | Connect to<br>VccSus3_3LAN | 0.1 µF<br>4.7 µF | 4<br>2 | | ☐ |
| VCCR[2:1] | Connect to<br>VccSus3_3LAN via filter | 0.1 µF<br>4.7 µF | 1<br>1 | 4.7 uH from power supply to VCCR pins. Caps on VCCR side of the inductor. | ☐ |

# 15. Schematics

Refer to the following pages for schematics.

# Intel® 852GME Platform with the Mobile Intel® Pentium® 4 Processor, Mobile Intel® Pentium® 4 Processor supporting Hyper-Threading Technology on 90-nm process technology, Intel® Celeron® Processor and Intel® Celeron® D Processor Customer Reference Board




| | | | |
|---|---|---|---|
| Title | BLOCK DIAGRAM | | |
| Size A | Project: | Document Number | Rev |
| Date: Friday, May 21, 2004 | | Sheet 1 of 46 | |

# CUSTOMER REFERENCE PLATFORM

## SCHEMATIC ANNOTATIONS AND BOARD INFORMATION

### Voltage Rails

| | |
|---|---|
| +VDC | Primary DC system power supply (10 to 21V) |
| +VCC_IMVP | Core/VTT voltage for processor & VTT for GMCH |
| +VCC_VID | 1.2V for processor PLL and VID circuitry |
| +V1.5S | 1.5V for GMCH core/hub interface |
| +V1.25S | 1.25V DDR Termination voltage |
| +V1.5S | 1.5V switched power rail (off in S3-S5) |
| +V1.5ALWAYS | 1.5V always on power rail |
| +V1.5 | 1.5V power rail (off in S4-S5) |
| +V2.5 | 2.5V power rail for DDR |
| +V3.3ALWAYS | 3.3V always on power rail |
| +V3.3 | 3.3V power rail (off in S4-S5) |
| +V3.3S | 3.3V switched power rail (off in S3-S5) |
| +V5ALWAYS | 5.0V for ICH4M's VCC5REFSUS |
| +V5 | 5.0V power rail (off in S4-S5) |
| +V5S | 5.0V switched power rail (off in S3-S5) |
| +V12S | 12.0V switched power rail (off in S3-S5) |
| -V12S | -12.0V switched power rail for PCI (off in S3-S5) |

### I²C / SMB Addresses

| Device | Address | Hex | Bus |
|---|---|---|---|
| Clock Generator | 1101 001x | D2 | SMB_ICH_S |
| Spread Spectrum Clock | 1101 010x | D4 | SMB_ICH_S |
| SO-DIMM0 | 1010 000x | A0 | SMB_ICH_S |
| SO-DIMM1 | 1010 001x | A2 | SMB_ICH_S |
| Thermal Sensor Header | 1001 000x | 90 | SMB_ICH |
| LVDS Backlight Inverter | ____ ____ | __ | SMB_ICH |
| Dock Connector | ____ ____ | __ | SMB_ICH |
| Smart Battery | 0001 011x | 16 | SMB_SB |
| Smart Battery Charger | 0001 001x | 12 | SMB_SB |
| Smart Selector | 0001 010x | 14 | SMB_SB |
| Bluetooth Header | ____ ____ | __ | SMB_SB |
| LPC Pwr Mngmnt Header | ____ ____ | __ | SMB_SB |
| LPC Pwr Mngmnt Header | ____ ____ | __ | SMB_THRM |
| Thermal Diode | 1001 110x | 9C | SMB_THRM |
| | | | |
| EV Support: | | | |
| DV0-DV3 | 0101 0001 | 51 | SMB_ICH |
| V5-V8 | 0101 0010 | 52 | SMB_ICH |
| PV0-PV3 | 0101 0011 | 53 | SMB_ICH |
| DV4 | 0101 0100 | 54 | SMB_ICH |
| V9-V12 | 0101 0101 | 55 | SMB_ICH |
| I1-I4 | 0101 0110 | 56 | SMB_ICH |
| EP1-EP4 | 0101 0111 | 57 | SMB_ICH |
| PV4 | 0101 0100 | 58 | SMB_ICH |
| V1-V4 | 0101 1001 | 59 | SMB_ICH |

### Default Jumper Settings

| Jumper | Default | Option | Description | Page |
|---|---|---|---|---|
| J7B1 | 1-2 | 1-X | GMCH Strap: PSB Voltage | 08 |
| J7B3 | 1-X | 1-2 | GMCH Strap: DVO/AGP | 08 |
| J7B4 | 1-X | 1-2 | GMCH Strap: Clock Config | 08 |
| J7B5 | 1-2 | 1-X | GMCH Strap: Clock Config | 08 |
| J7B6 | 1-2 | 1-X | GMCH Strap: Clock Config | 08 |
| J6E1 | 2-3 | 1-2 | LVDS EV | 08 |
| J6C2 | 1-2 | 1-X | AGP D3 Hot Support (3.3V) | 15 |
| J7F1 | 1-2 | 2-3 | AGP D3 On Support (1.5V) | 15 |
| J3H1 | 1-2 | 1-X | Docking VGA Enable | 17 |
| J2J3 | 1-X | 1-2 | CMOS Clear | 19 |
| J8J2 | 2-3 | 1-2 | CRB/SV Detect | 19 |
| J9E2 | 1-2 | 2-3 | Moon ISA Support | 23 |
| J9E4 | 1-2 | 2-3 | Moon ISA Support | 23 |
| J9E5 | 2-3 | 1-2 | Moon ISA Support | 23 |
| J9B1 | 1-X | 1-2 | SMC/KBC Hardware Programming | 32 |
| J9A1 | 1-X | 1-2 | KBC 60/64 Decode Disable | 32 |
| J8A2 | 1-2 | 2-3 | SMC/KBC Disable | 32 |
| J8A1 | 1-2 | 1-X | NMI Jumper, SMC Programming | 33 |
| J9H1 | 1-X | 1-2 | Port 80-81/82-83 Select | 33 |
| J9G2 | 1-2 | 2-3 | SIO Disable | 34 |
| J1F1 | 1-X | 1-2 | Manual VID Strap Enable | 39 |
| J1G1 | 1-2 | 2-3 | VID0 Strap | 39 |
| J1G2 | 1-2 | 2-3 | VID1 Strap | 39 |
| J1G3 | 1-2 | 2-3 | VID2 Strap | 39 |
| J1G4 | 1-2 | 2-3 | VID3 Strap | 39 |
| J1H1 | 1-2 | 2-3 | VID4 Strap | 39 |
| J1H2 | 1-2 | 1-X or 2-3 | VID5 Strap | 39 |
| J3G1 | 1-X | 1-2 or 2-3 | DDR EV Support | 43 |
| J3G2 | 1-X | 1-2 or 2-3 | DDR VR Vsense | 43 |

### PCI Devices

| Device | IDSEL # | REQ/GNT # | | Interrupts | PC/PCI |
|---|---|---|---|---|---|
| Slot 1 | AD16 | 1 | 1 | F, G, H, E | A |
| Slot 2 | AD17 | 2 | 2 | G, F, E, H | A |
| Slot 3 | AD18 | 3 | 3 | C, D, B, A (E, F, G, H optional) | A |
| Docking | AD28 | 4 | 4 | D, A, B, C | B |
| LAN | (AD24 internal) | | | (E internal) | |

### LEDs and Switches

| LED | Page | Reference |
|---|---|---|
| Primary IDE | 27 | DS2J2 |
| Secondary IDE | 27 | DS2J1 |
| SMC/KBC Num Lock | 32 | DS8A1 |
| SMC/KBC Scroll Lock | 32 | DS8A2 |
| SMC/KBC Caps Lock | 32 | DS8B1 |
| S0 State | 38 | DS1H1 |
| S1 State | 38 | DS1H3 |
| S3 State | 38 | DS1H2 |
| S4 State | 38 | DS2H2 |
| S5 State | 38 | DS2H1 |
| VID0 | 39 | DS1J4 |
| VID1 | 39 | DS1J3 |
| VID2 | 39 | DS1J2 |
| VID3 | 39 | DS2J4 |
| VID4 | 39 | DS2J3 |
| VID5 | 39 | DS1J1 |

| Switch | Page | Reference |
|---|---|---|
| Virtual Battery On/Off | 32 | SW8A1 |
| Lid | 32 | SW9A1 |
| Power On/Off | 44 | SW8J1 |
| Reset | 44 | SW7J1 |

### Wake Events

RI# (Ring Indicate) from serial port
PME# (Power Management Event) from PCI/mini-PCI slots, ADD slot, LPC slot
I/O from the LAN Interface
LID switch attached to SMC
USB
AC97 wake on ring
SmLink for AOL II
Hot Key from the scan matrix keyboard

### Net Naming Conventions

Suffix
# = Active Low signal

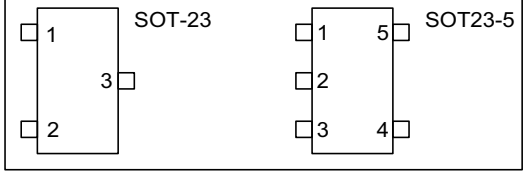
Prefix
H = Host
M = DDR Memory
TP = Test Point (does not connect anywhere else)

### Power States

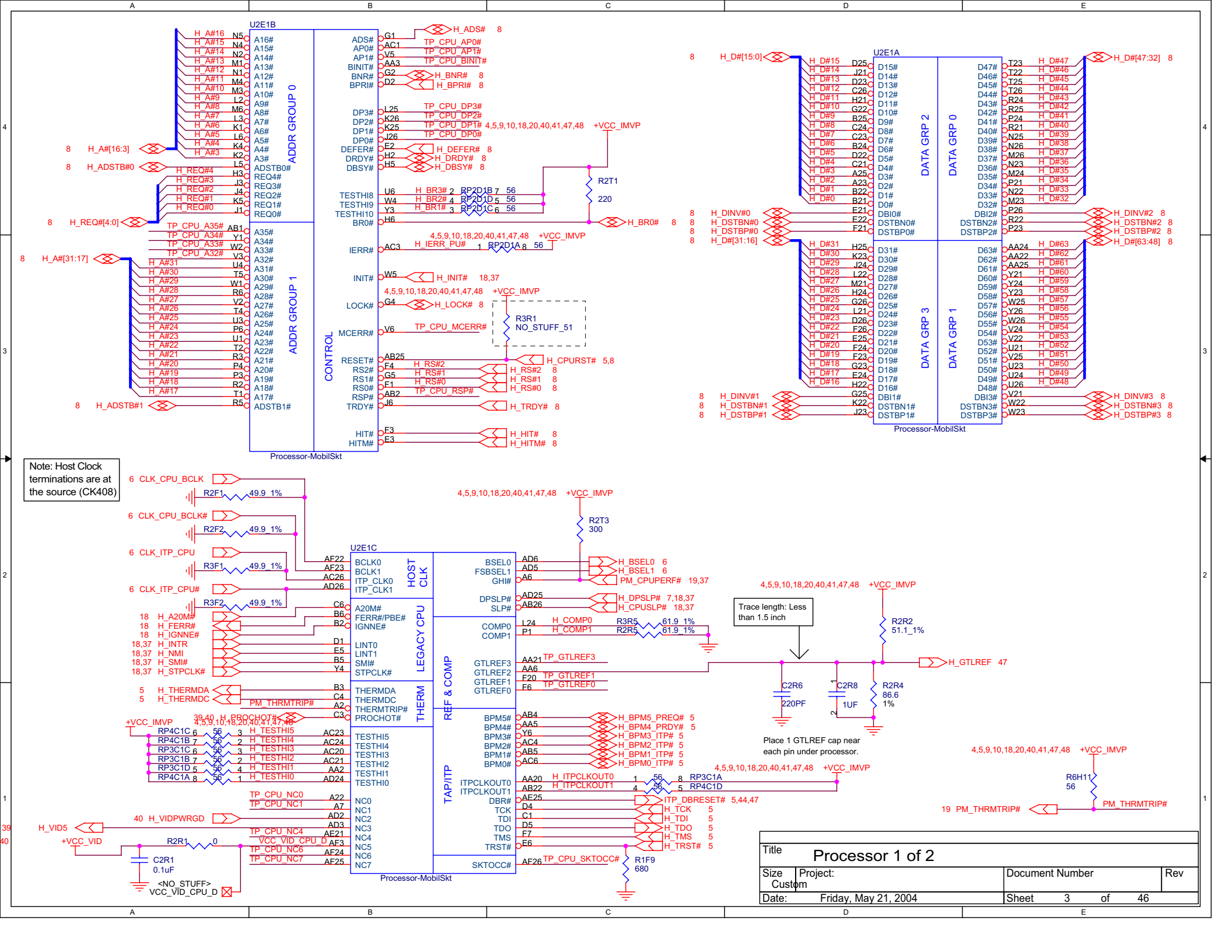
| STATE \ SIGNAL | SLP_S1# | SLP_S3# | SLP_S4# | SLP_S5# | +V*ALWAYS | +V* | +V*S | Clocks |
|---|---|---|---|---|---|---|---|---|
| Full ON | HIGH | HIGH | HIGH | HIGH | ON | ON | ON | ON |
| S1M (Power On Suspend) | LOW | HIGH | HIGH | HIGH | ON | ON | ON | LOW |
| S3 (Suspend to RAM) | LOW | LOW | HIGH | HIGH | ON | ON | OFF | OFF |
| S4 (Suspend To Disk) | LOW | LOW | LOW | HIGH | ON | OFF | OFF | OFF |
| S5 / Soft OFF | LOW | LOW | LOW | LOW | ON | OFF | OFF | OFF |

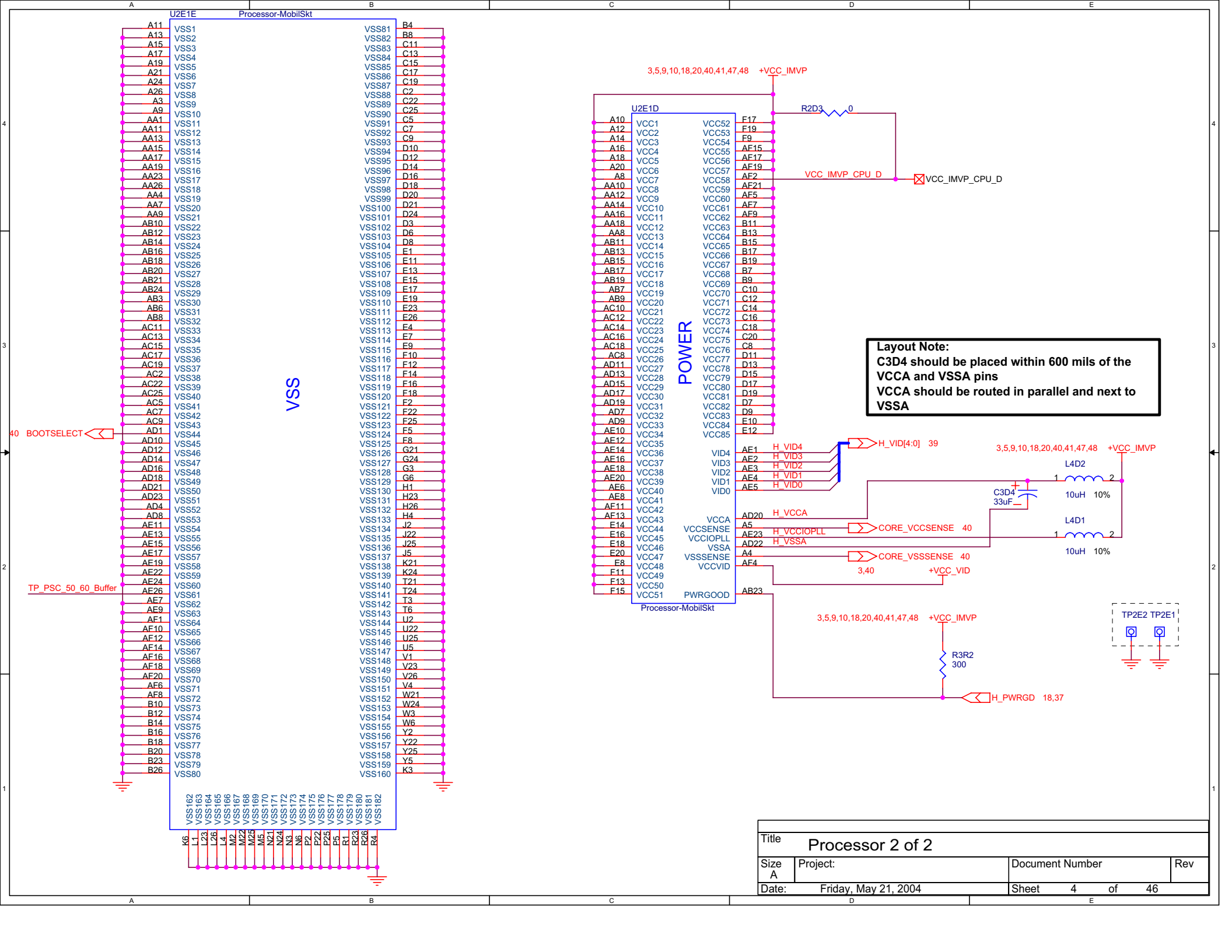
### PCB Footprints

*As seen from top*




| | | | |
|---|---|---|---|
| Title: Notes and Annotations | | | |
| Size: A | Project: | Document Number | Rev |
| Date: Friday, May 21, 2004 | | Sheet 2 of 46 | |


U2E1B
ADDR GROUP 0
ADDR GROUP 1
CONTROL
Processor-MobilSkt
U2E1A
DATA GRP 2
DATA GRP 0
DATA GRP 3
DATA GRP 1
Processor-MobilSkt
U2E1C
HOST CLK
LEGACY CPU
THERM
REF & COMP
TAP/ITP
Processor-MobilSkt
Note: Host Clock terminations are at the source (CK408)
Trace length: Less than 1.5 inch
Place 1 GTLREF cap near each pin under processor.
Title
Processor 1 of 2
Size
Custom
Project:
Document Number
Rev
Date:
Friday, May 21, 2004
Sheet
3
of
46


U2E1E
Processor-MobilSkt
VSS
40 BOOTSELECT
TP_PSC_50_60_Buffer
U2E1D
POWER
Processor-MobilSkt
3,5,9,10,18,20,40,41,47,48 +VCC_IMVP
R2D3 0
VCC_IMVP_CPU_D
VCC_IMVP_CPU_D
H_VID[4:0] 39
H_VID4
H_VID3
H_VID2
H_VID1
H_VID0
H_VCCA
CORE_VCCSENSE 40
H_VCCIOPLL
H_VSSA
CORE_VSSSENSE 40
3,40 +VCC_VID
H_PWRGD 18,37
L4D2
L4D1
10uH 10%
C3D4
33uF
R3R2
300
TP2E2 TP2E1
Layout Note:
C3D4 should be placed within 600 mils of the VCCA and VSSA pins
VCCA should be routed in parallel and next to VSSA
Title
Processor 2 of 2
Size A
Project:
Document Number
Rev
Date: Friday, May 21, 2004
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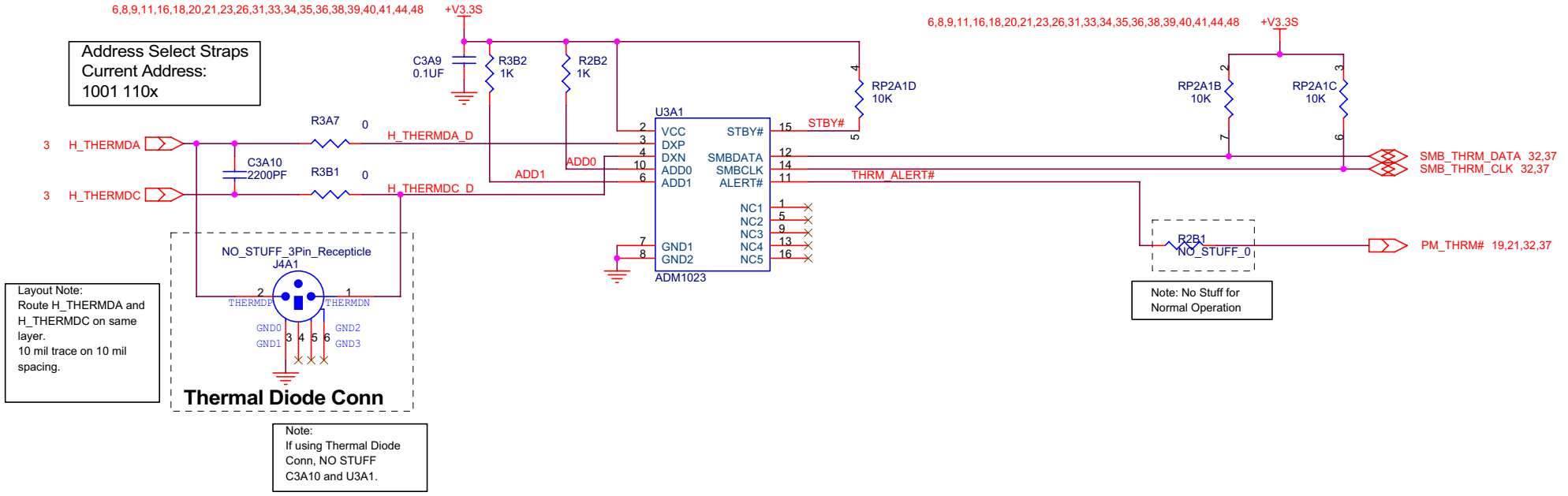
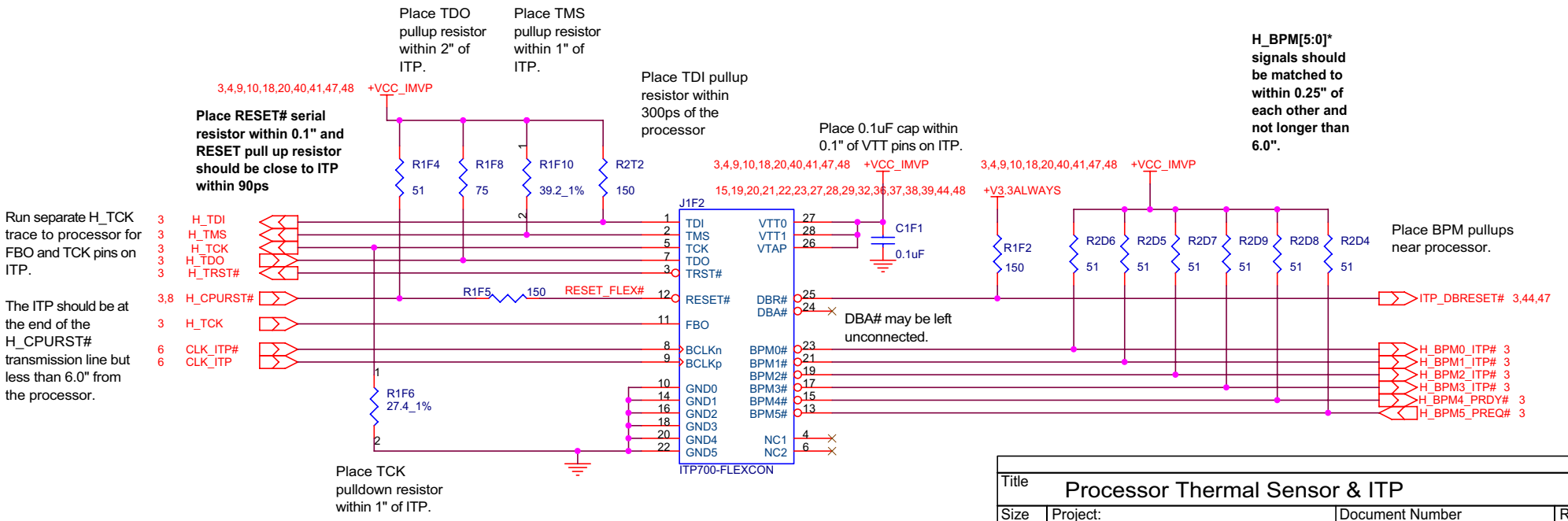
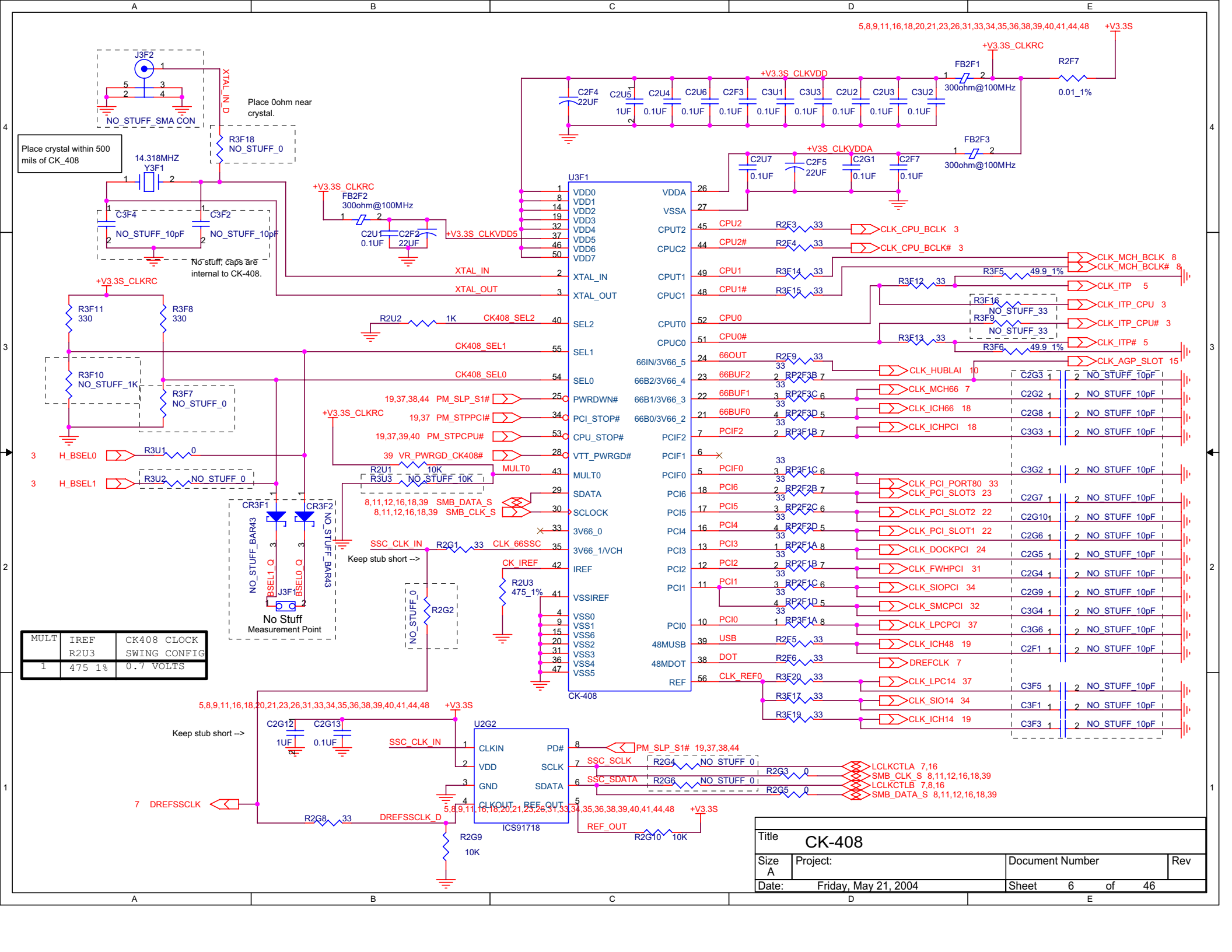
# Processor Thermal Sensor




| | | | |
|---|---|---|---|
| Title | Processor Thermal Sensor & ITP | | |
| Size A | Project: | Document Number | Rev |
| Date: Friday, May 21, 2004 | | Sheet 5 of 46 | |


5,8,9,11,16,18,20,21,23,26,31,33,34,35,36,38,39,40,41,44,48
+V3.3S
+V3.3S_CLKRC
FB2F1
300ohm@100MHz
R2F7
0.01_1%
+V3.3S_CLKVDD
C2F4 22UF
C2U5 1UF
C2U4 0.1UF
C2U6 0.1UF
C2F3 0.1UF
C3U1 0.1UF
C3U3 0.1UF
C2U2 0.1UF
C2U3 0.1UF
C3U2 0.1UF
+V3S_CLKVDDA
FB2F3
300ohm@100MHz
C2U7 0.1UF
C2F5 22UF
C2G1 0.1UF
C2F7 0.1UF
J3F2
NO_STUFF_SMA CON
XTAL_IN_D
Place 0ohm near crystal.
R3F18 NO_STUFF_0
Place crystal within 500 mils of CK_408
14.318MHZ
Y3F1
C3F4 NO_STUFF_10pF
C3F2 NO_STUFF_10pF
No stuff, caps are internal to CK-408.
+V3.3S_CLKRC
FB2F2
300ohm@100MHz
C2U1 0.1UF
C2F2 22UF
+V3.3S_CLKVDD5
U3F1
VDD0
VDD1
VDD2
VDD3
VDD4
VDD5
VDD6
VDD7
VDDA
VSSA
XTAL_IN
XTAL_OUT
SEL2
SEL1
SEL0
PWRDWN#
PCI_STOP#
CPU_STOP#
VTT_PWRGD#
MULT0
SDATA
SCLOCK
3V66_0
3V66_1/VCH
IREF
VSSIREF
VSS0
VSS1
VSS6
VSS2
VSS3
VSS4
VSS5
CPUT2
CPUC2
CPUT1
CPUC1
CPUT0
CPUC0
66IN/3V66_5
66B2/3V66_4
66B1/3V66_3
66B0/3V66_2
PCIF2
PCIF1
PCIF0
PCI6
PCI5
PCI4
PCI3
PCI2
PCI1
PCI0
48MUSB
48MDOT
REF
CK-408
CPU2
CPU2#
CPU1
CPU1#
CPU0
CPU0#
66OUT
66BUF2
66BUF1
66BUF0
PCIF2
PCIF0
PCI6
PCI5
PCI4
PCI3
PCI2
PCI1
PCI0
USB
DOT
CLK_REF0
R2F3 33
R2F4 33
R3F14 33
R3F15 33
R3F5 49.9_1%
R3F12 33
R3F16 NO_STUFF_33
R3F9 NO_STUFF_33
R3F13 33
R3F6 49.9_1%
R2F9 33
R2F3B 7
R2F3C 6
R2F3D 5
R3F1B 7
R3F1C 6
R2F2B 7
R2F2C 6
R2F2D 5
R2F1A 8
R2F1B 7
R2F1C 6
R2F1D 5
R3F1A 8
R2F5 33
R2F6 33
R3F20 33
R3F17 33
R3F19 33
CLK_CPU_BCLK 3
CLK_CPU_BCLK# 3
CLK_MCH_BCLK 8
CLK_MCH_BCLK# 8
CLK_ITP 5
CLK_ITP_CPU 3
CLK_ITP_CPU# 3
CLK_ITP# 5
CLK_AGP_SLOT 15
CLK_HUBLAI 10
CLK_MCH66 7
CLK_ICH66 18
CLK_ICHPCI 18
CLK_PCI_PORT80 33
CLK_PCI_SLOT3 23
CLK_PCI_SLOT2 22
CLK_PCI_SLOT1 22
CLK_DOCKPCI 24
CLK_FWHPCI 31
CLK_SIOPCI 34
CLK_SMCPCI 32
CLK_LPCPCI 37
CLK_ICH48 19
DREFCLK 7
CLK_LPC14 37
CLK_SIO14 34
CLK_ICH14 19
C2G3 C2G2 C2G8 C3G3 C3G2 C2G7 C2G10 C2G6 C2G5 C2G4 C2G9 C3G4 C3G6 C2F1 C3F5 C3F1 C3F3
NO_STUFF_10pF
R3F11 330
R3F8 330
R3F10 NO_STUFF_1K
R3F7 NO_STUFF_0
R2U2 1K CK408_SEL2
CK408_SEL1
CK408_SEL0
19,37,38,44 PM_SLP_S1#
19,37 PM_STPPCI#
19,37,39,40 PM_STPCPU#
39 VR_PWRGD_CK408#
R2U1 10K
R3U3 NO_STUFF_10K
MULT0
8,11,12,16,18,39 SMB_DATA_S
8,11,12,16,18,39 SMB_CLK_S
3 H_BSEL0
R3U1 0
3 H_BSEL1
R3U2 NO_STUFF_0
CR3F1
CR3F2
NO_STUFF_BAR43
BSEL1_Q
BSEL0_Q
J3F1
No Stuff
Measurement Point
SSC_CLK_IN
R2G1 33
CLK_66SSC
Keep stub short -->
CK_IREF
R2U3 475_1%
R2G2
NO_STUFF_0
MULT | IREF R2U3 | CK408 CLOCK SWING CONFIG
1 | 475 1% | 0.7 VOLTS
5,8,9,11,16,18,20,21,23,26,31,33,34,35,36,38,39,40,41,44,48
+V3.3S
Keep stub short -->
C2G12 1UF
C2G13 0.1UF
U2G2
CLKIN
VDD
GND
CLKOUT
PD#
SCLK
SDATA
REF_OUT
ICS91718
SSC_CLK_IN
PM_SLP_S1# 19,37,38,44
SSC_SCLK
SSC_SDATA
R2G4 NO_STUFF_0
R2G6 NO_STUFF_0
R2G3 0
R2G5 0
LCLKCTLA 7,16
SMB_CLK_S 8,11,12,16,18,39
LCLKCTLB 7,8,16
SMB_DATA_S 8,11,12,16,18,39
7 DREFSSCLK
R2G8 33
DREFSSCLK_D
5,8,9,11,16,18,20,21,23,26,31,33,34,35,36,38,39,40,41,44,48
+V3.3S
REF_OUT
R2G10 10K
R2G9 10K
Title CK-408
Size A
Project:
Document Number
Rev
Date: Friday, May 21, 2004
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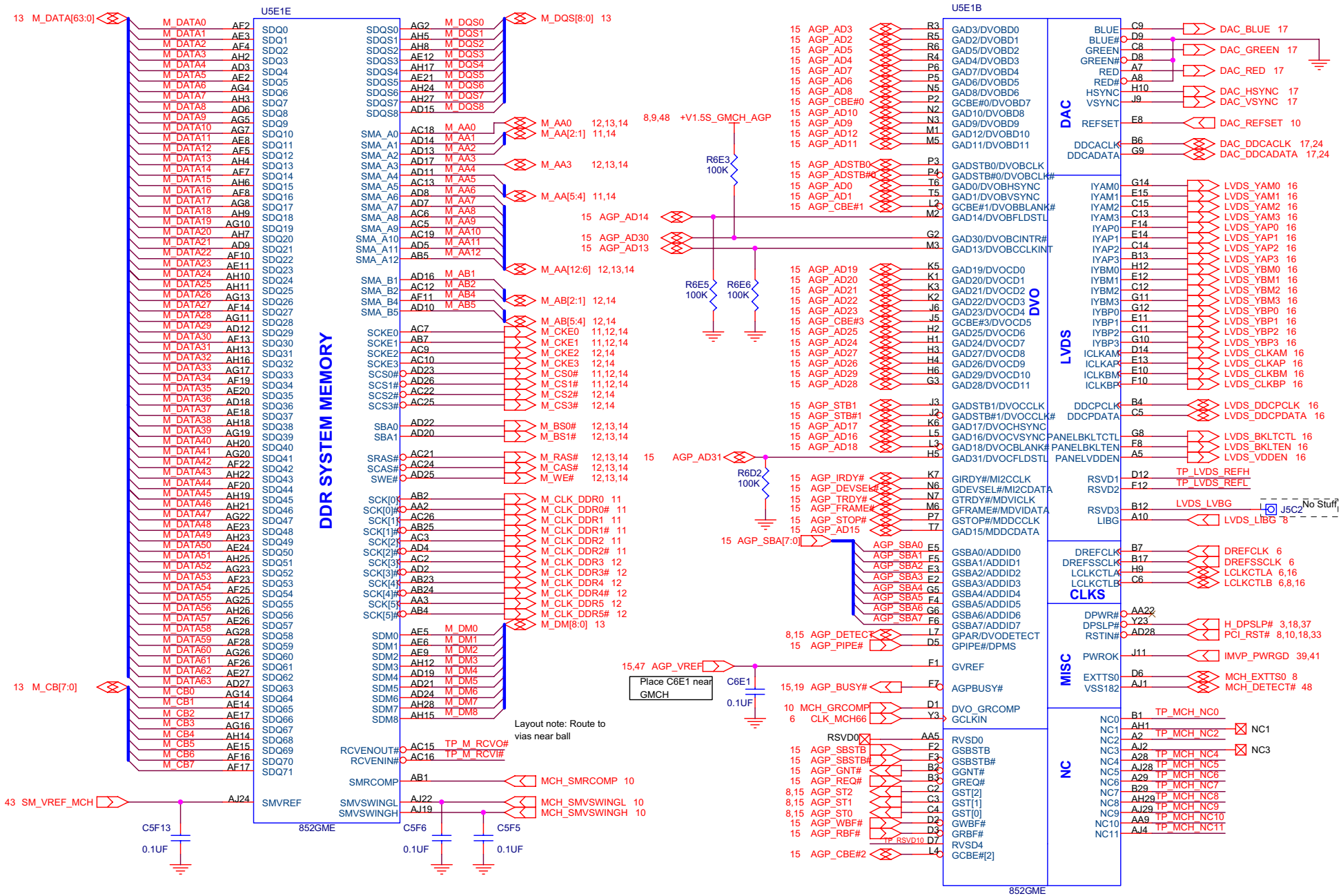
U5E1E
DDR SYSTEM MEMORY
852GME
U5E1B
DAC
LVDS
DVO
CLKS
MISC
NC
852GME
Layout note: Route to vias near ball
Place C6E1 near GMCH
Title
GMCH (1 of 3)
Size A
Project:
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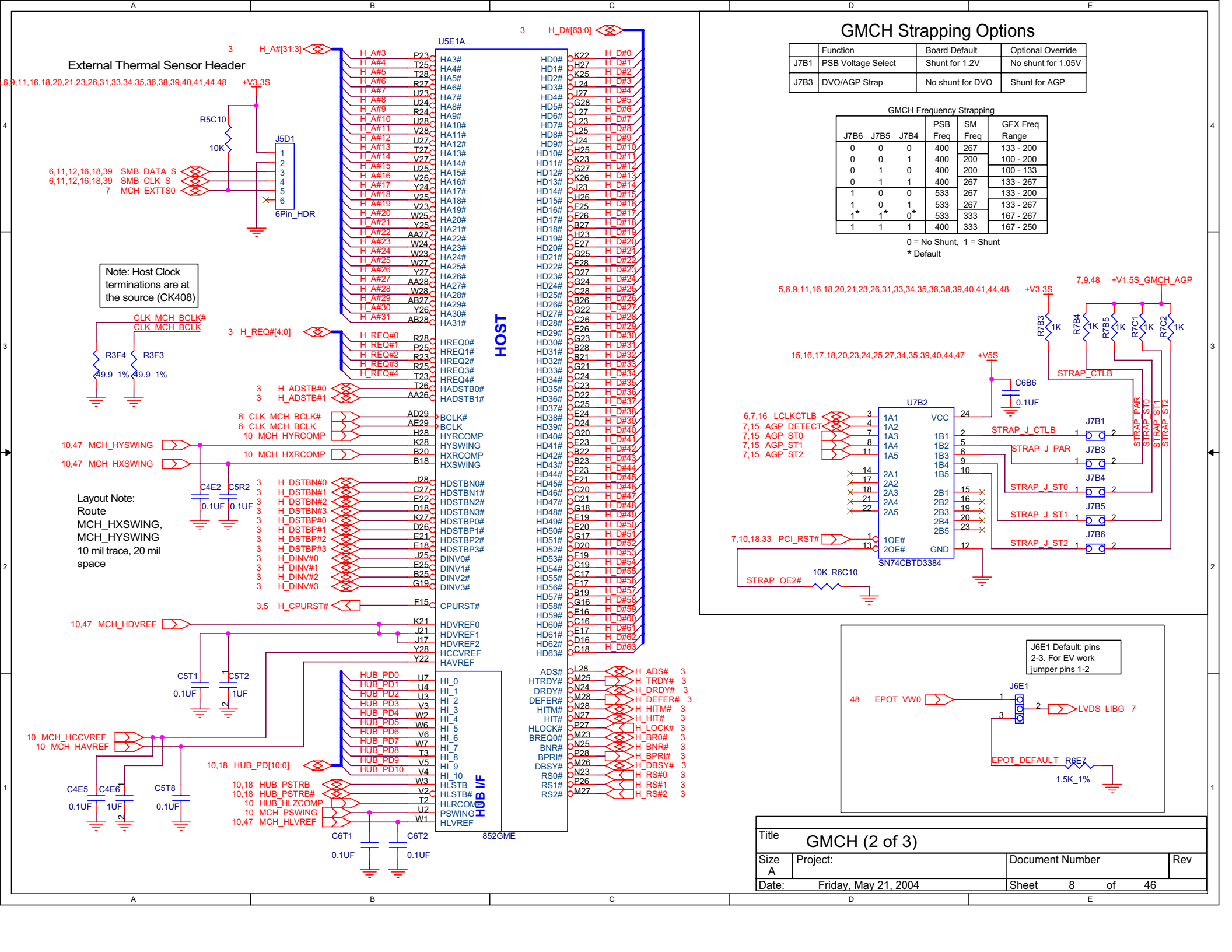
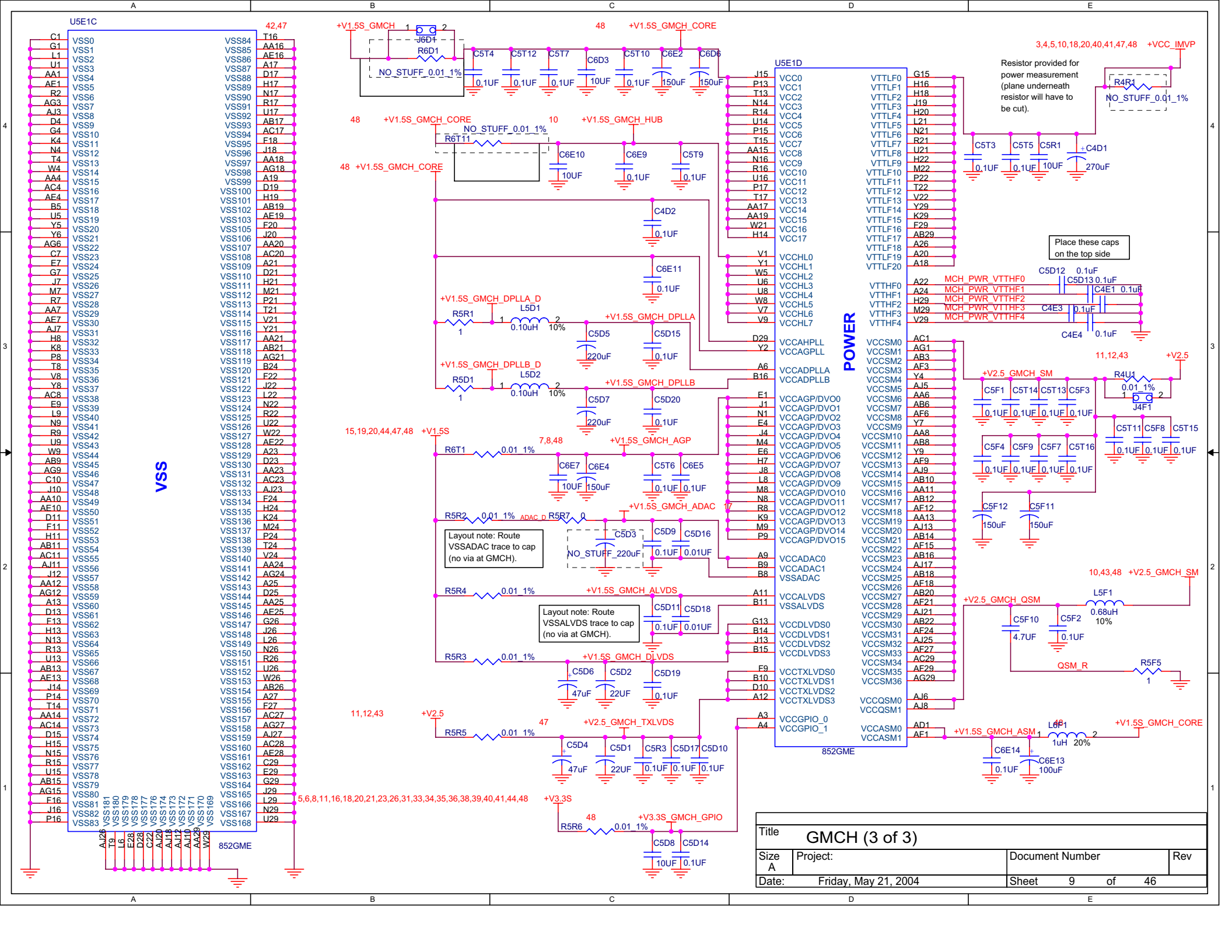



| | Function | Board Default | Optional Override |
|---|---|---|---|
| J7B1 | PSB Voltage Select | Shunt for 1.2V | No shunt for 1.05V |
| J7B3 | DVO/AGP Strap | No shunt for DVO | Shunt for AGP |

| J7B6 | J7B5 | J7B4 | PSB Freq | SM Freq | GFX Freq Range |
|---|---|---|---|---|---|
| 0 | 0 | 0 | 400 | 267 | 133 - 200 |
| 0 | 0 | 1 | 400 | 200 | 100 - 200 |
| 0 | 1 | 0 | 400 | 200 | 100 - 133 |
| 0 | 1 | 1 | 400 | 267 | 133 - 267 |
| 1 | 0 | 0 | 533 | 267 | 133 - 200 |
| 1 | 0 | 1 | 533 | 267 | 133 - 267 |
| 1* | 1* | 0* | 533 | 333 | 167 - 267 |
| 1 | 1 | 1 | 400 | 333 | 167 - 250 |


U5E1C
VSS
852GME
U5E1D
POWER
852GME
Resistor provided for power measurement (plane underneath resistor will have to be cut).
Place these caps on the top side
Layout note: Route VSSADAC trace to cap (no via at GMCH).
Layout note: Route VSSALVDS trace to cap (no via at GMCH).
Title
GMCH (3 of 3)
Size A
Project:
Document Number
Rev
Date: Friday, May 21, 2004
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## GMCH-GT Compensation & Reference Voltages

Host

3,4,5,9,18,20,40,41,47,48 +VCC_IMVP
R5R9 301_1%
8,47 MCH_HXSWING
R5R10 150_1%

3,4,5,9,18,20,40,41,47,48 +VCC_IMVP
R4T1 301_1%
8,47 MCH_HYSWING
R4E2 150_1%

3,4,5,9,18,20,40,41,47,48 +VCC_IMVP
R5T2 49.9_1%
8,47 MCH_HDVREF
R5T1 100_1%

R5D2
8 MCH_HXRCOMP 1 2 27.4_1%

R4E1
8 MCH_HYRCOMP 1 2 27.4_1%

3,4,5,9,18,20,40,41,47,48 +VCC_IMVP
R4T2 49.9_1%
8 MCH_HCCVREF
R4E4 100_1%

3,4,5,9,18,20,40,41,47,48 +VCC_IMVP
R5T4 49.9_1%
8 MCH_HAVREF
R5T5 100_1%

Digital Video Port
7 MCH_GRCOMP
R6D6 40.2_1%

DAC
7 DAC_REFSET
R5R8 127 1%

Hub Interface
9 +V1.5S_GMCH_HUB
R6T2
8 HUB_HLZCOMP
48.7_1%

9 +V1.5S_GMCH_HUB
R6T4 86.6_1%
8 MCH_PSWING
R6T3 100_1%

9 +V1.5S_GMCH_HUB
C6T3 No Stuff
NO_STUFF_470PF
MCH_GTLREF2
R6T6 NO_STUFF_56.2_1%
R6T7 324_1%
8,47 MCH_HLVREF
R6T10 100_1%
C6T4
R6T8 MCH_GTLREF3
NO_STUFF_0 NO_STUFF_0.01UF

## LAI Hub Interface

8,18 HUB_PD[10:0]
8,18 HUB_PSTRB#

J6U1
NO_STUFF_HUBLINK

MCH_HLVREF

HUB_PD0 R6E8 392_1% LAI_HUB_PIN6
HUB_PD2 R6F1 392_1% LAI_HUB_PIN10
HUB_PD4 R6F12 392_1% LAI_HUB_PIN18
R6F10 392_1% LAI_HUB_PIN26
HUB_PD6 R6F16 392_1% LAI_HUB_PIN34
HUB_PD7 R6F21 392_1% LAI_HUB_PIN38

R6F4 392_1% LAI_HUB_PIN7 HUB_PD1
R6F5 392_1% LAI_HUB_PIN11 HUB_PD3
R6F11 392_1% LAI_HUB_PIN19 CLK_HUBLAI 6
R6F13 392_1% LAI_HUB_PIN23 HUB_PSTRB 8,18
R6F17 392_1% LAI_HUB_PIN31 HUB_PD5
LAI_HUB_PIN35 PCI_RST# 7,8,18,33
R6F18 392_1%
R6F22 392_1% LAI_HUB_PIN47 HUB_PD9
R6F25 392_1% LAI_HUB_PIN59 HUB_PD10
R6G1 392_1% LAI_HUB_PIN71 HUB_PD8

## System Memory

9,43,48 +V2.5_GMCH_SM
R5F3 150_1%
7 MCH_SMVSWINGH
R5F1 604 1%

9,43,48 +V2.5_GMCH_SM
R5F4 604 1%
7 MCH_SMVSWINGL
R5F2 150_1%

9,43,48 +V2.5_GMCH_SM
R6T12 60.4_1%
C6T5 0.1UF
7 MCH_SMRCOMP
R6T9 60.4_1%

Layout Note: The following signals should have 10 mil spacing and must be routed 20 mil from any other trace.

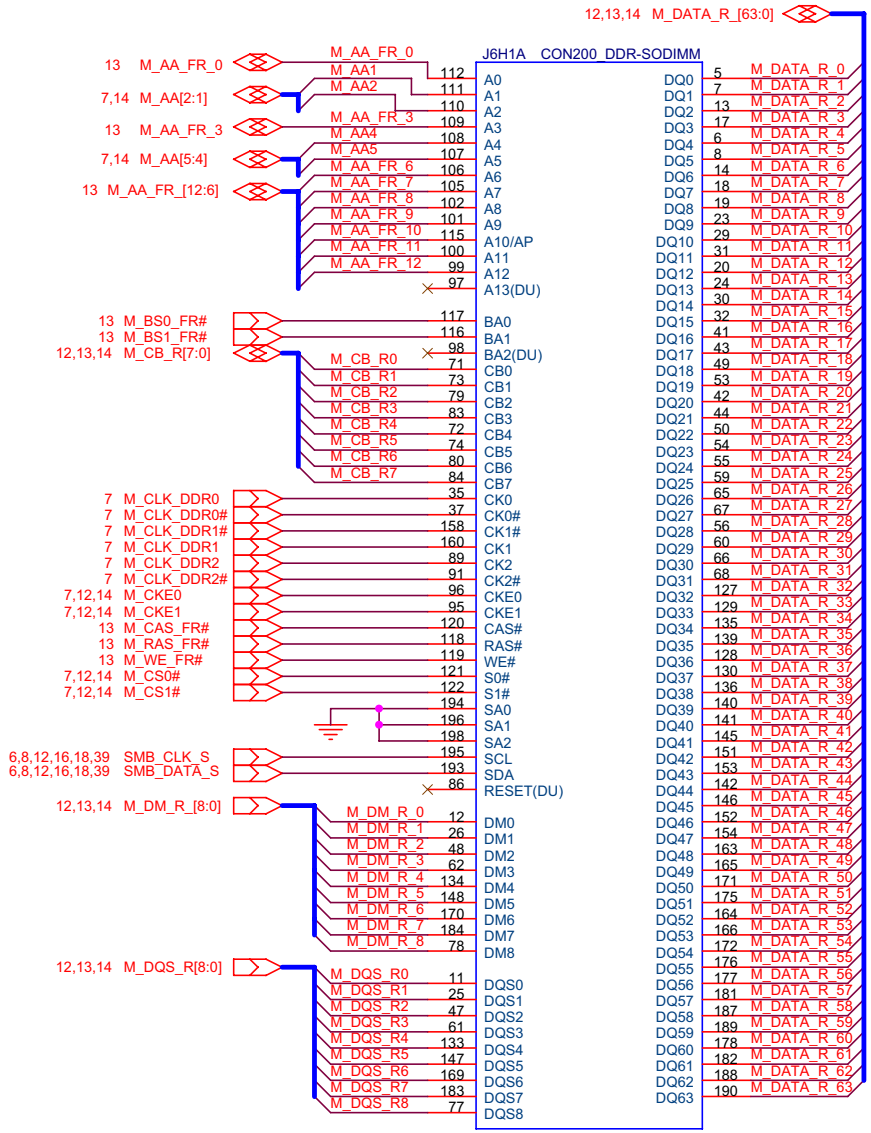
MCH_HXSWING
MCH_HYSWING
MCH_HDVREF
MCH_HXRCOMP
MCH_HYRCOMP
MCH_HCCVREF
MCH_HLVREF
MCH_SMVSWINGL
MCH_SMRCOMP
MCH_SMVSWINGH
HUB_HLZCOMP
MCH_PSWING
DAC_REFSET
MCH_GRCOMP
MCH_HAVREF

Manufacturing Support

J4D1
ANCHOR_CLIP_GHOST
J6D2
ANCHOR_CLIP_GHOST
J4F2
ANCHOR_CLIP_GHOST
J6F1
ANCHOR_CLIP_GHOST

ASSEMBLY_LABEL

| | | | |
|---|---|---|---|
| Title: GMCH Circuitry | | | |
| Size: A | Project: | Document Number | Rev |
| Date: Friday, May 21, 2004 | | Sheet 10 of 46 | |

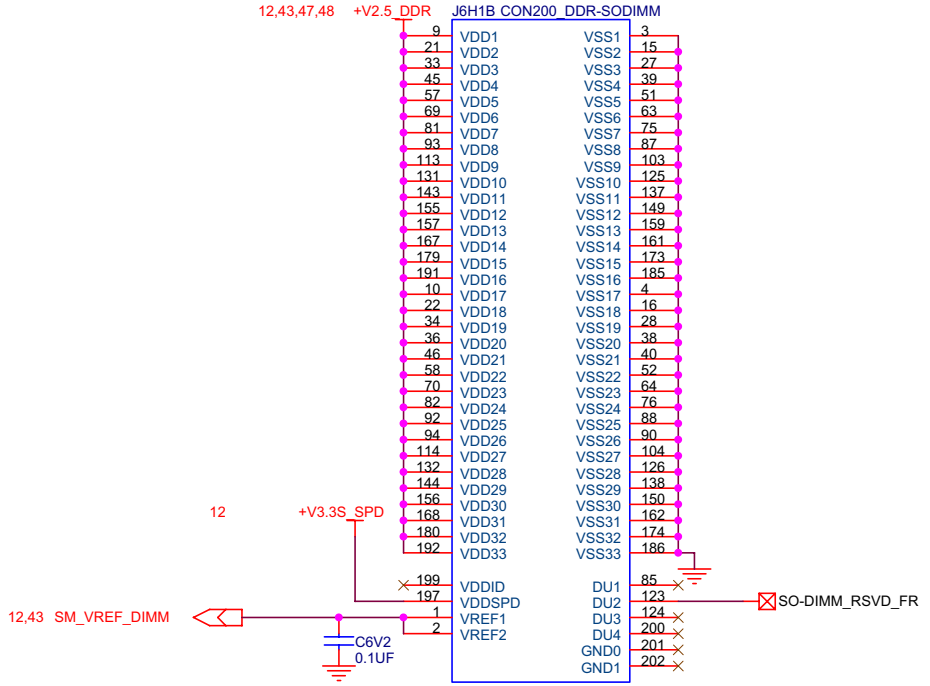


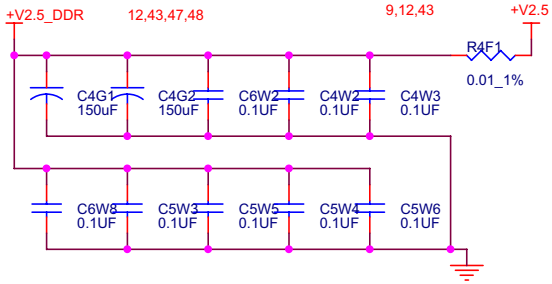

SO-DIMM 0

5,6,8,9,16,18,20,21,23,26,31,33,34,35,36,38,39,40,41,44,48 +V3.3S 12 +V3.3S_SPD

R4W1 0.01_1%

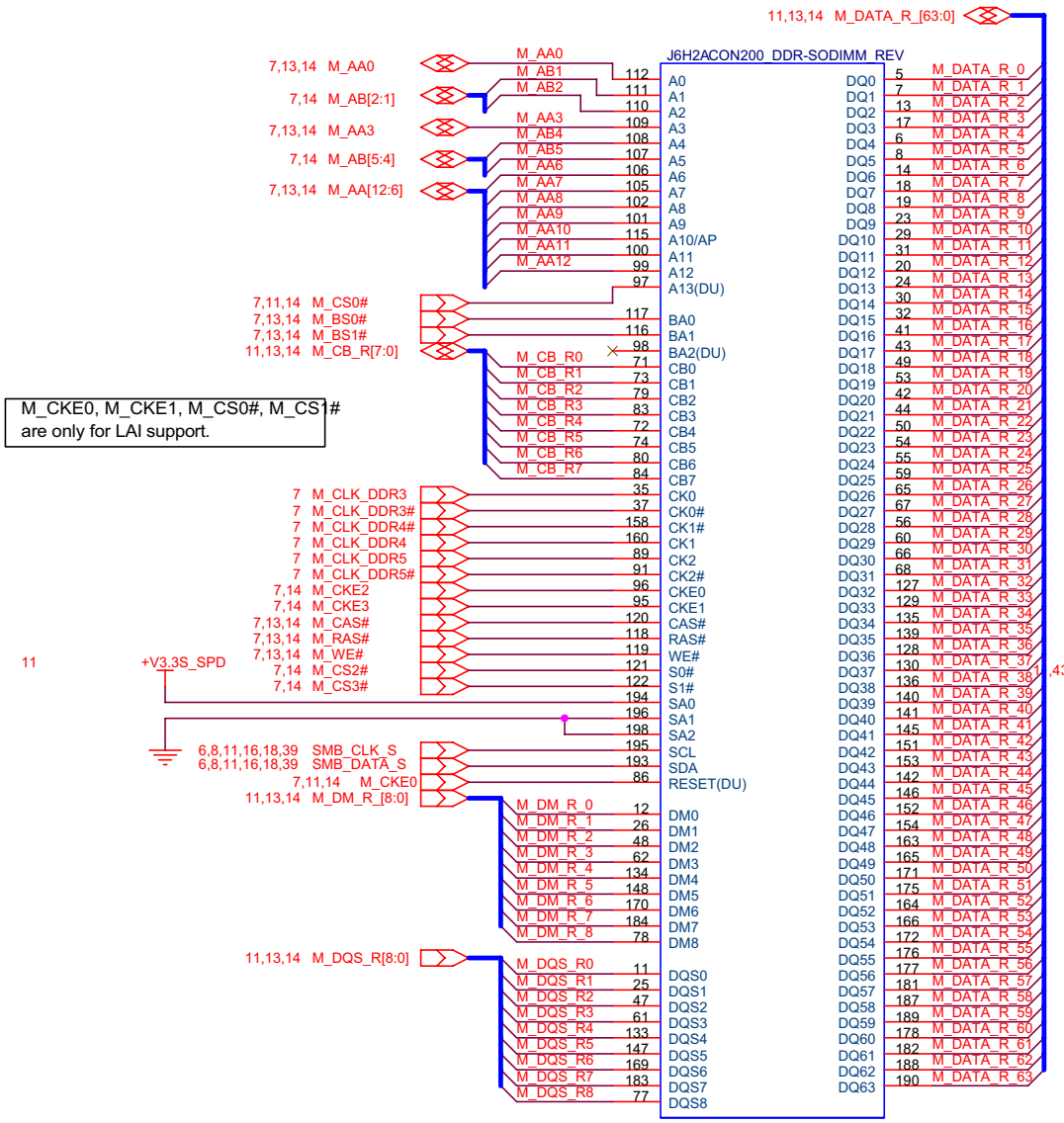
Power plane for Serial Presence Detect logic



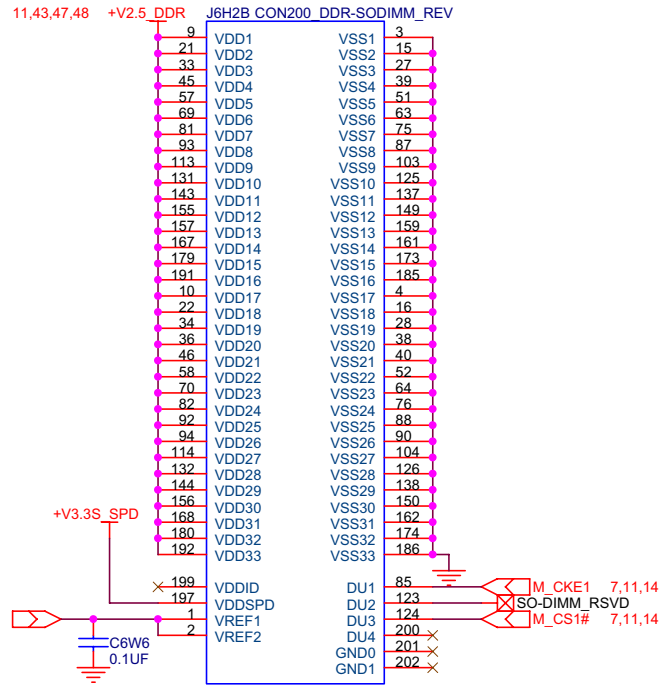

Layout note: Place capacitors between and near DDR connector if possible

| | | | |
|---|---|---|---|
| Title | DDR SO-DIMMs (1 of 2) | | |
| Size A | Project: | Document Number | Rev |
| Date: Friday, May 21, 2004 | | Sheet 11 of 46 | |




# SO-DIMM 1

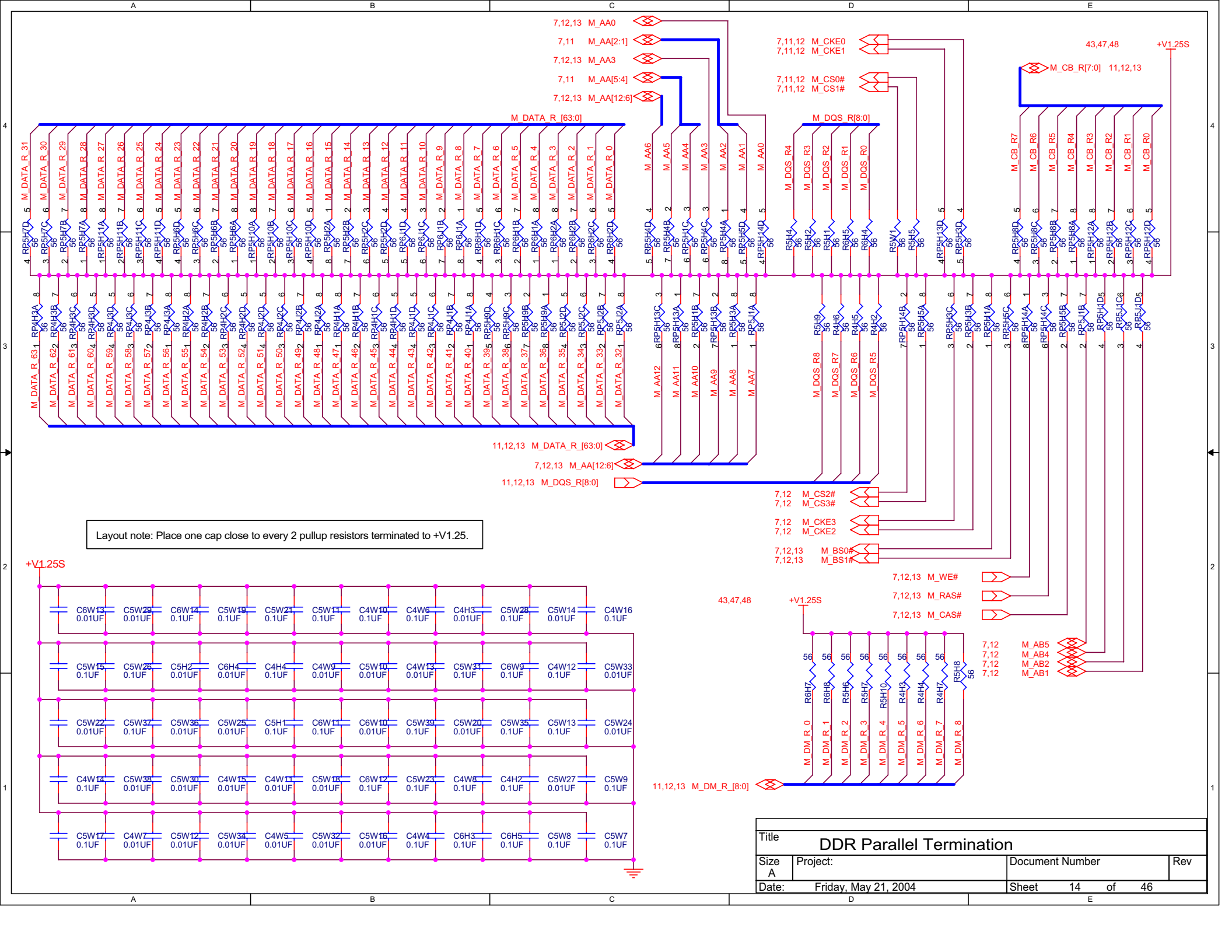
SO-DIMM1 is placed further from GMCH than SO-DIMM0




Layout note: Place capacitors between and near DDR connector if possible

| | | | |
|---|---|---|---|
| Title: DDR SO-DIMMs (2 of 2) | | | |
| Size: A | Project: | Document Number | Rev |
| Date: Friday, May 21, 2004 | | Sheet 12 of 46 | |

| | | | |
|---|---|---|---|
| Title | DDR Series Termination | | |
| Size Custom | Project: | Document Number | Rev |
| Date: Friday, May 21, 2004 | | Sheet 13 of 46 | |


7,12,13 M_AA0
7,11 M_AA[2:1]
7,12,13 M_AA3
7,11 M_AA[5:4]
7,12,13 M_AA[12:6]
M_DATA_R_[63:0]
7,11,12 M_CKE0
7,11,12 M_CKE1
7,11,12 M_CS0#
7,11,12 M_CS1#
M_DQS_R[8:0]
43,47,48 +V1.25S
M_CB_R[7:0] 11,12,13
11,12,13 M_DATA_R_[63:0]
7,12,13 M_AA[12:6]
11,12,13 M_DQS_R[8:0]
7,12 M_CS2#
7,12 M_CS3#
7,12 M_CKE3
7,12 M_CKE2
7,12,13 M_BS0#
7,12,13 M_BS1#
7,12,13 M_WE#
7,12,13 M_RAS#
7,12,13 M_CAS#
43,47,48 +V1.25S
11,12,13 M_DM_R_[8:0]
7,12 M_AB5
7,12 M_AB4
7,12 M_AB2
7,12 M_AB1
+V1.25S
Layout note: Place one cap close to every 2 pullup resistors terminated to +V1.25.
Title
DDR Parallel Termination
Size A
Project:
Document Number
Rev
Date: Friday, May 21, 2004
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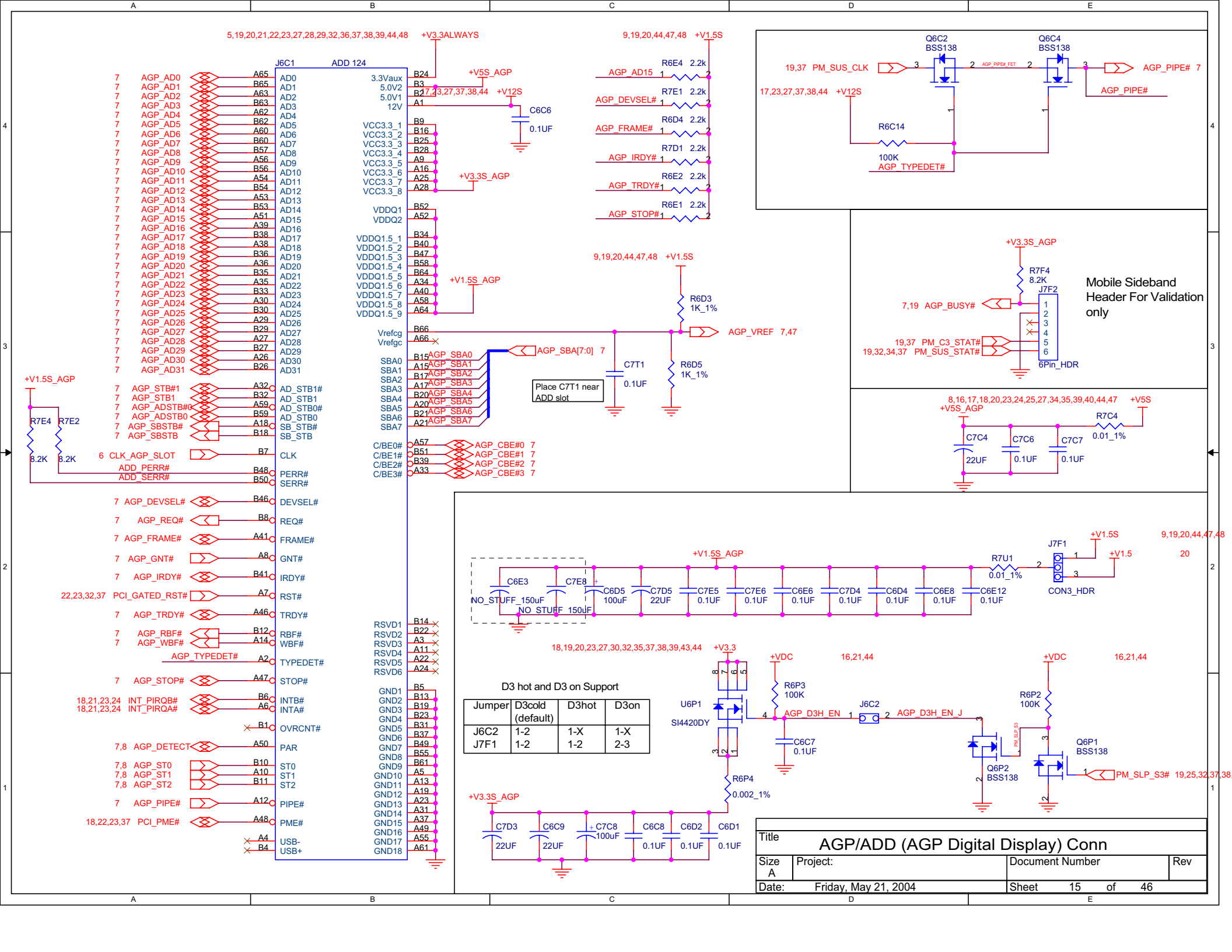
J6C1
ADD 124
AGP_AD0
AGP_AD1
AGP_AD2
AGP_AD3
AGP_AD4
AGP_AD5
AGP_AD6
AGP_AD7
AGP_AD8
AGP_AD9
AGP_AD10
AGP_AD11
AGP_AD12
AGP_AD13
AGP_AD14
AGP_AD15
AGP_AD16
AGP_AD17
AGP_AD18
AGP_AD19
AGP_AD20
AGP_AD21
AGP_AD22
AGP_AD23
AGP_AD24
AGP_AD25
AGP_AD26
AGP_AD27
AGP_AD28
AGP_AD29
AGP_AD30
AGP_AD31
AGP_STB#1
AGP_STB1
AGP_ADSTB#0
AGP_ADSTB0
AGP_SBSTB#
AGP_SBSTB
CLK_AGP_SLOT
ADD_PERR#
ADD_SERR#
AGP_DEVSEL#
AGP_REQ#
AGP_FRAME#
AGP_GNT#
AGP_IRDY#
PCI_GATED_RST#
AGP_TRDY#
AGP_RBF#
AGP_WBF#
AGP_TYPEDET#
AGP_STOP#
INT_PIRQB#
INT_PIRQA#
OVRCNT#
AGP_DETECT
AGP_ST0
AGP_ST1
AGP_ST2
AGP_PIPE#
PCI_PME#
+V1.5S_AGP
R7E4 8.2K
R7E2 8.2K
+V3.3ALWAYS
+V5S_AGP
+V12S
C6C6 0.1UF
+V3.3S_AGP
+V1.5S_AGP
AGP_SBA[7:0]
Place C7T1 near ADD slot
C7T1 0.1UF
R6D5 1K_1%
R6D3 1K_1%
AGP_VREF
R6E4 2.2k AGP_AD15
R7E1 2.2k AGP_DEVSEL#
R6D4 2.2k AGP_FRAME#
R7D1 2.2k AGP_IRDY#
R6E2 2.2k AGP_TRDY#
R6E1 2.2k AGP_STOP#
Q6C2 BSS138
Q6C4 BSS138
19,37 PM_SUS_CLK
AGP_PIPE_FET
AGP_PIPE# 7
R6C14 100K
AGP_TYPEDET#
R7F4 8.2K
J7F2
7,19 AGP_BUSY#
19,37 PM_C3_STAT#
19,32,34,37 PM_SUS_STAT#
6Pin_HDR
Mobile Sideband Header For Validation only
C7C4 22UF
C7C6 0.1UF
C7C7 0.1UF
R7C4 0.01_1%
C6E3 NO_STUFF_150uF
C7E8 NO_STUFF_150uF
C6D5 100uF
C7D5 22UF
C7E5 0.1UF
C7E6 0.1UF
C6E6 0.1UF
C7D4 0.1UF
C6D4 0.1UF
C6E8 0.1UF
C6E12 0.1UF
R7U1 0.01_1%
J7F1
CON3_HDR
D3 hot and D3 on Support
Jumper | D3cold (default) | D3hot | D3on
J6C2 | 1-2 | 1-X | 1-X
J7F1 | 1-2 | 1-2 | 2-3
U6P1 SI4420DY
R6P3 100K
AGP_D3H_EN
J6C2
AGP_D3H_EN_J
C6C7 0.1UF
R6P4 0.002_1%
R6P2 100K
Q6P2 BSS138
Q6P1 BSS138
PM_SLP_S3#
C7D3 22UF
C6C9 22UF
C7C8 100uF
C6C8 0.1UF
C6D2 0.1UF
C6D1 0.1UF
Title
AGP/ADD (AGP Digital Display) Conn
Size A
Project:
Document Number
Rev
Date: Friday, May 21, 2004
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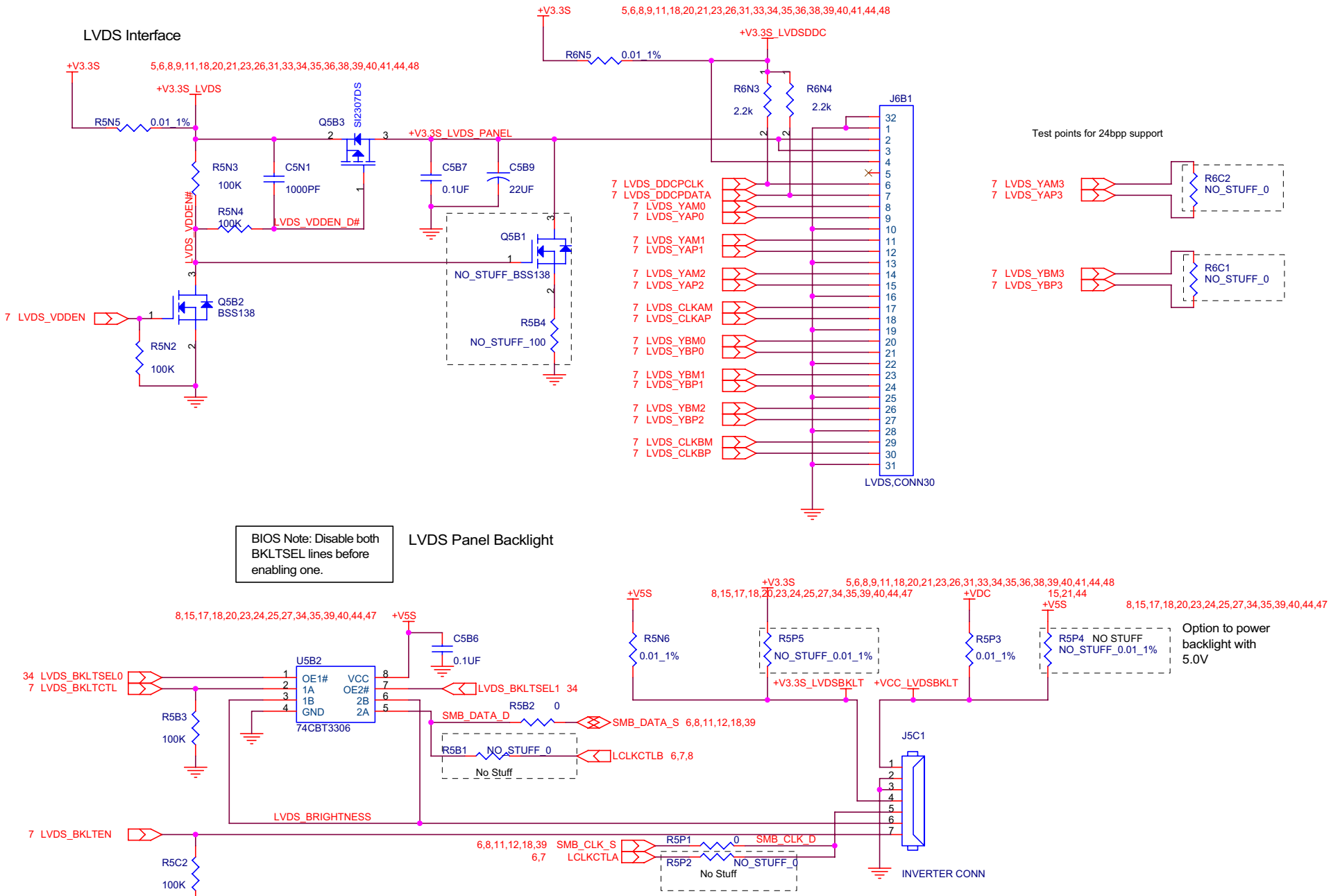
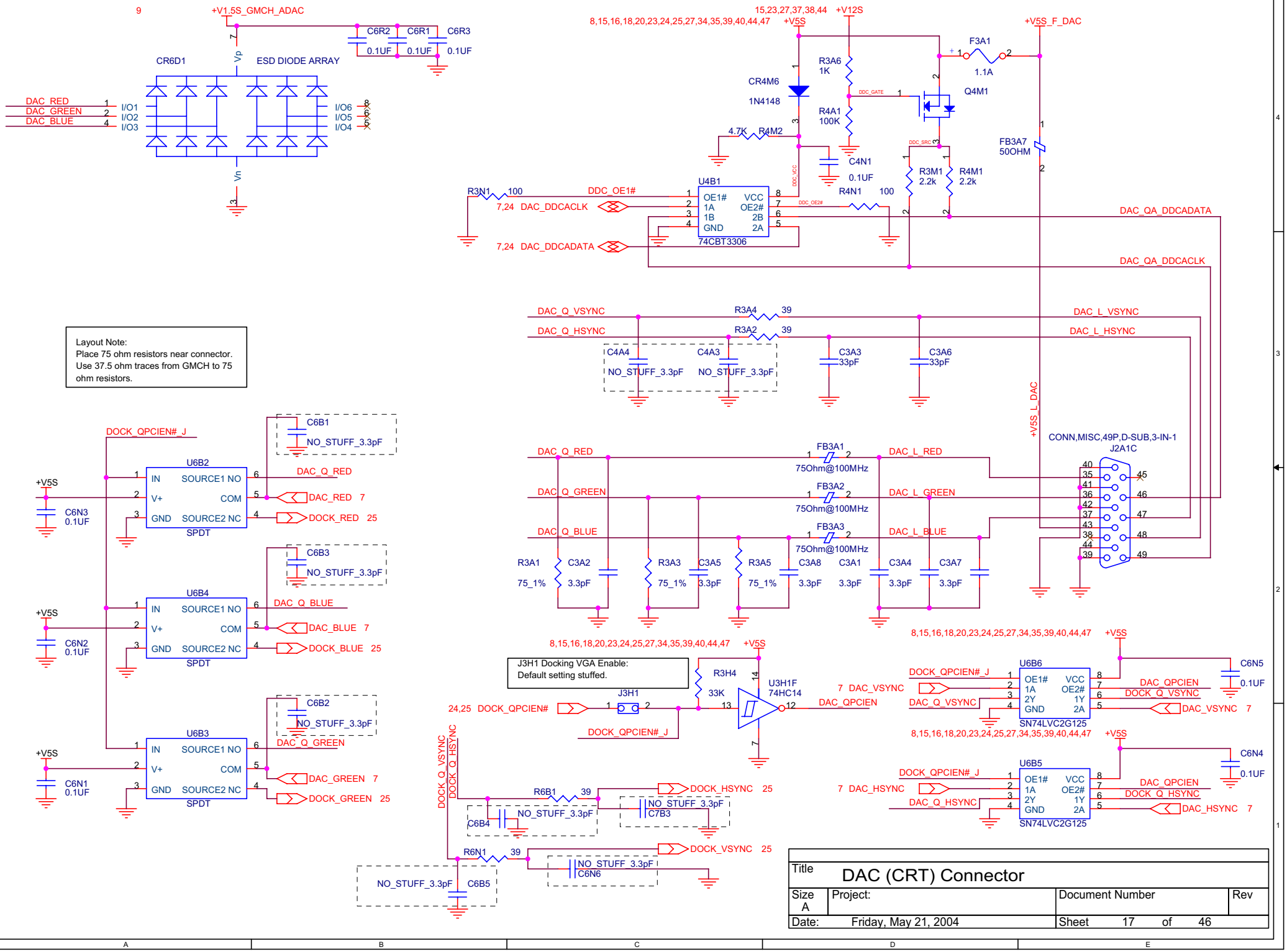
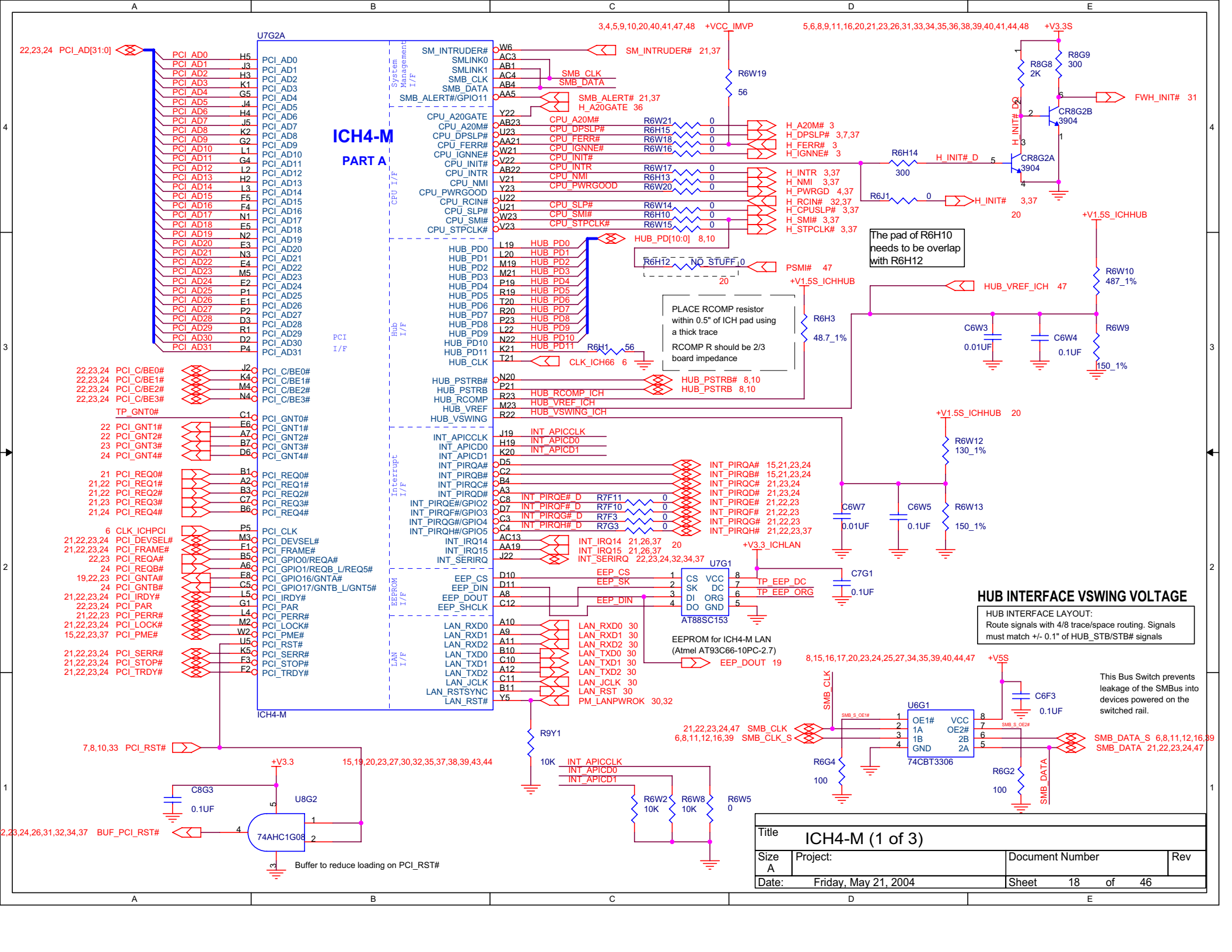



| | | | |
|---|---|---|---|
| Title: LVDS | | | |
| Size: A | Project: | Document Number | Rev |
| Date: Friday, May 21, 2004 | | Sheet 16 of 46 | |




| | | | |
|---|---|---|---|
| Title | DAC (CRT) Connector | | |
| Size A | Project: | Document Number | Rev |
| Date: Friday, May 21, 2004 | | Sheet 17 of 46 | |


U7G2A
ICH4-M
PART A
PCI I/F
System Management I/F
CPU I/F
Hub I/F
Interrupt I/F
EEPROM I/F
LAN I/F
PCI_AD[31:0]
PCI_C/BE0#
PCI_C/BE1#
PCI_C/BE2#
PCI_C/BE3#
TP_GNT0#
PCI_GNT1#
PCI_GNT2#
PCI_GNT3#
PCI_GNT4#
PCI_REQ0#
PCI_REQ1#
PCI_REQ2#
PCI_REQ3#
PCI_REQ4#
CLK_ICHPCI
PCI_DEVSEL#
PCI_FRAME#
PCI_REQA#
PCI_REQB#
PCI_GNTA#
PCI_GNTB#
PCI_IRDY#
PCI_PAR
PCI_PERR#
PCI_LOCK#
PCI_PME#
PCI_RST#
PCI_SERR#
PCI_STOP#
PCI_TRDY#
SM_INTRUDER#
SMLINK0
SMLINK1
SMB_CLK
SMB_DATA
SMB_ALERT#/GPIO11
CPU_A20GATE
CPU_A20M#
CPU_DPSLP#
CPU_FERR#
CPU_IGNNE#
CPU_INIT#
CPU_INTR
CPU_NMI
CPU_PWRGOOD
CPU_RCIN#
CPU_SLP#
CPU_SMI#
CPU_STPCLK#
HUB_PD0
HUB_PD1
HUB_PD2
HUB_PD3
HUB_PD4
HUB_PD5
HUB_PD6
HUB_PD7
HUB_PD8
HUB_PD9
HUB_PD10
HUB_PD11
HUB_CLK
HUB_PSTRB#
HUB_PSTRB
HUB_RCOMP
HUB_VREF
HUB_VSWING
INT_APICCLK
INT_APICD0
INT_APICD1
INT_PIRQA#
INT_PIRQB#
INT_PIRQC#
INT_PIRQD#
INT_PIRQE#/GPIO2
INT_PIRQF#/GPIO3
INT_PIRQG#/GPIO4
INT_PIRQH#/GPIO5
INT_IRQ14
INT_IRQ15
INT_SERIRQ
EEP_CS
EEP_DIN
EEP_DOUT
EEP_SHCLK
LAN_RXD0
LAN_RXD1
LAN_RXD2
LAN_TXD0
LAN_TXD1
LAN_TXD2
LAN_JCLK
LAN_RSTSYNC
LAN_RST#
ICH4-M
+VCC_IMVP
+V3.3S
R6W19
56
R8G8 2K
R8G9 300
CR8G2B 3904
CR8G2A 3904
FWH_INIT# 31
H_INIT#_D
R6H14 300
R6J1 0
H_INIT# 3,37
20
+V1.5S_ICHHUB
The pad of R6H10 needs to be overlap with R6H12
R6H12 NO_STUFF 0
PSMI# 47
HUB_VREF_ICH 47
R6W10 487_1%
R6H3 48.7_1%
R6H1 56
CLK_ICH66 6
C6W3 0.01UF
C6W4 0.1UF
R6W9 150_1%
PLACE RCOMP resistor within 0.5" of ICH pad using a thick trace
RCOMP R should be 2/3 board impedance
R6W12 130_1%
C6W7 0.01UF
C6W5 0.1UF
R6W13 150_1%
+V3.3_ICHLAN
C7G1 0.1UF
U7G1
AT88SC153
TP_EEP_DC
TP_EEP_ORG
EEPROM for ICH4-M LAN
(Atmel AT93C66-10PC-2.7)
EEP_DOUT 19
HUB INTERFACE VSWING VOLTAGE
HUB INTERFACE LAYOUT:
Route signals with 4/8 trace/space routing. Signals must match +/- 0.1" of HUB_STB/STB# signals
+V5S
C6F3 0.1UF
U6G1
74CBT3306
SMB_CLK
SMB_CLK_S
SMB_DATA_S
SMB_DATA
R6G4 100
R6G2 100
This Bus Switch prevents leakage of the SMBus into devices powered on the switched rail.
R9Y1 10K
R6W2 10K
R6W8 10K
R6W5 0
U8G2
74AHC1G08
C8G3 0.1UF
BUF_PCI_RST#
Buffer to reduce loading on PCI_RST#
Title
ICH4-M (1 of 3)
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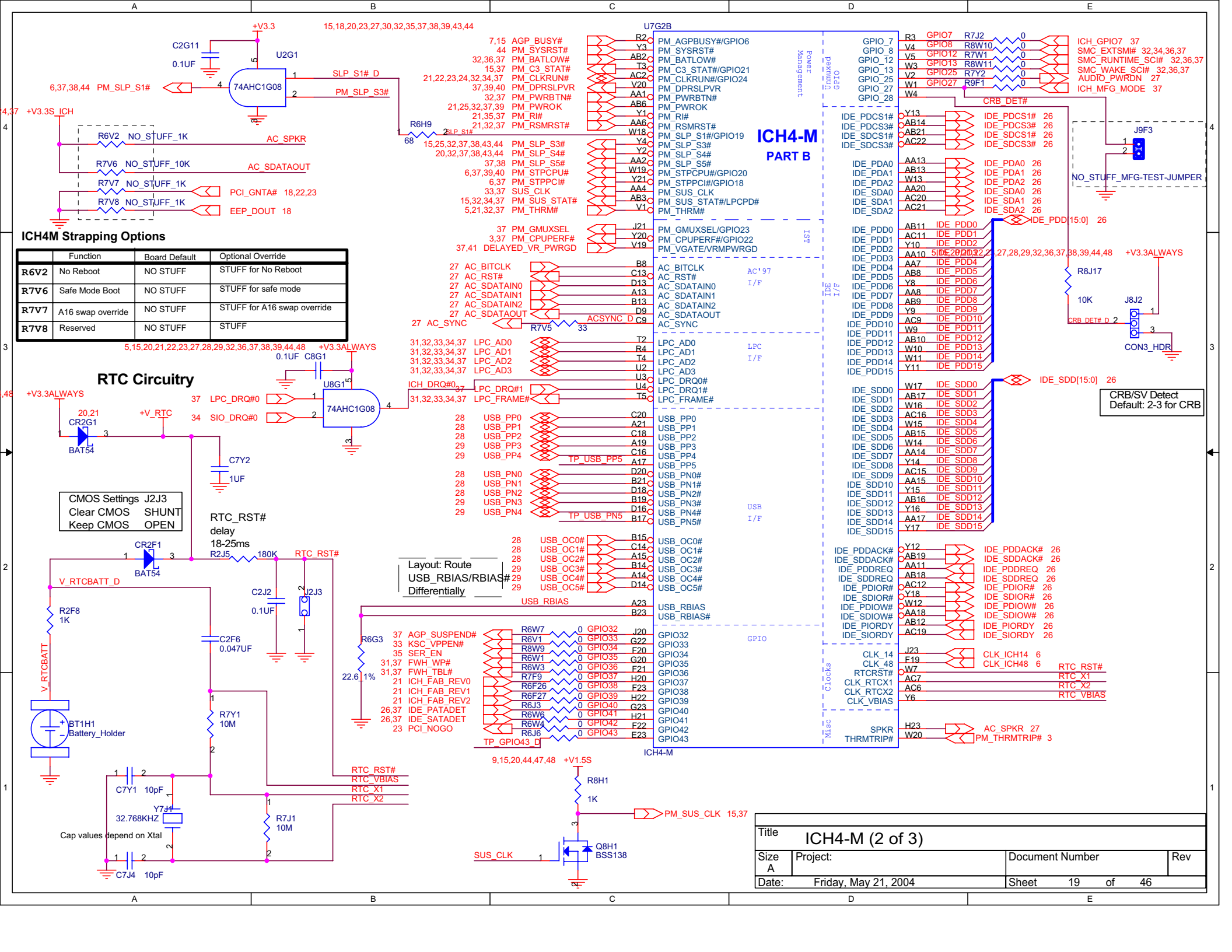
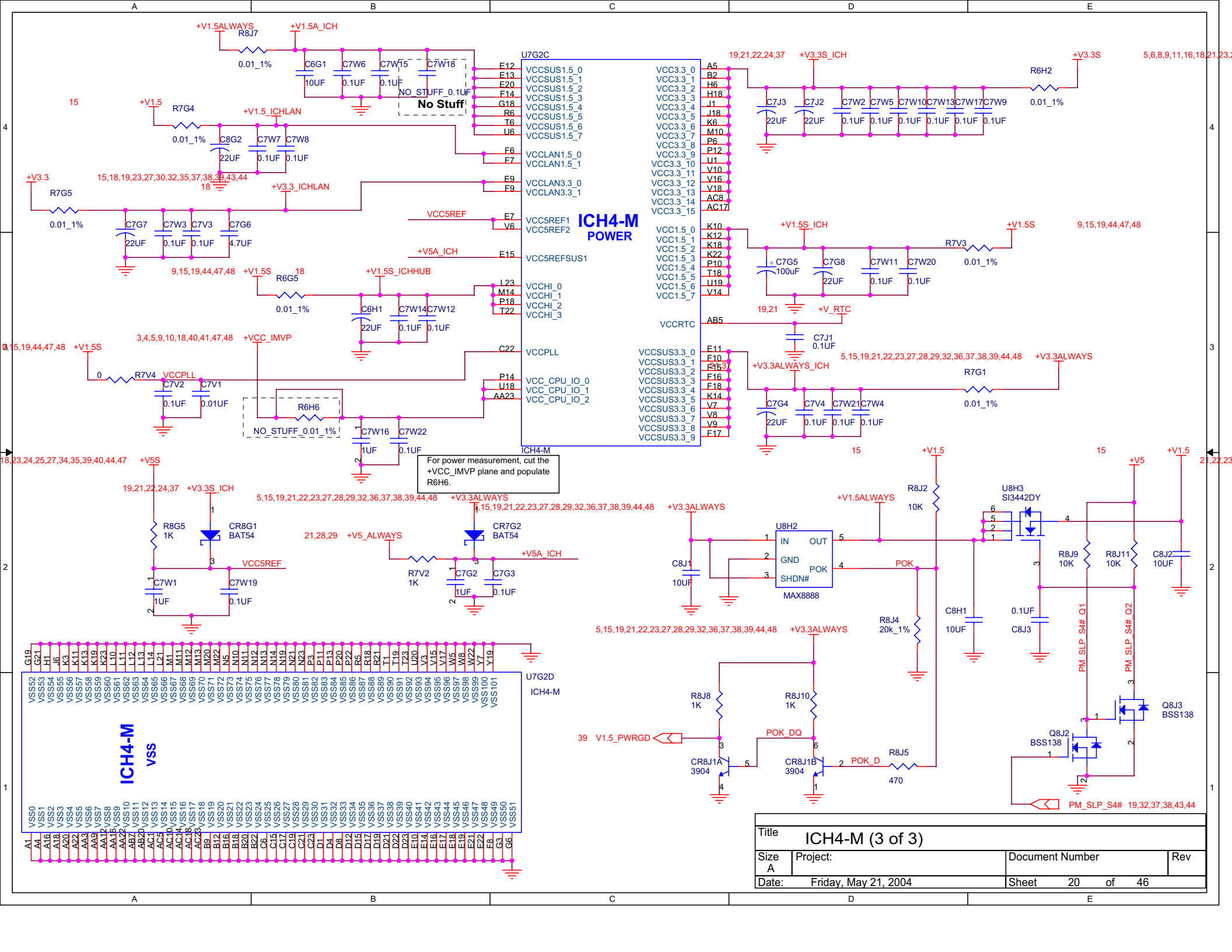



| | Function | Board Default | Optional Override |
|---|---|---|---|
| R6V2 | No Reboot | NO STUFF | STUFF for No Reboot |
| R7V6 | Safe Mode Boot | NO STUFF | STUFF for safe mode |
| R7V7 | A16 swap override | NO STUFF | STUFF for A16 swap override |
| R7V8 | Reserved | NO STUFF | STUFF |


+V1.5ALWAYS
+V1.5A_ICH
R8J7
0.01_1%
C6G1
10UF
C7W6
0.1UF
C7W15
0.1UF
C7W18
NO_STUFF_0.1UF
No Stuff
U7G2C
VCCSUS1.5_0
VCCSUS1.5_1
VCCSUS1.5_2
VCCSUS1.5_3
VCCSUS1.5_4
VCCSUS1.5_5
VCCSUS1.5_6
VCCSUS1.5_7
VCCLAN1.5_0
VCCLAN1.5_1
VCCLAN3.3_0
VCCLAN3.3_1
VCC5REFSUS1
VCCHI_0
VCCHI_1
VCCHI_2
VCCHI_3
VCCPLL
VCC_CPU_IO_0
VCC_CPU_IO_1
VCC_CPU_IO_2
VCC3.3_0
VCC3.3_1
VCC3.3_2
VCC3.3_3
VCC3.3_4
VCC3.3_5
VCC3.3_6
VCC3.3_7
VCC3.3_8
VCC3.3_9
VCC3.3_10
VCC3.3_11
VCC3.3_12
VCC3.3_13
VCC3.3_14
VCC3.3_15
VCC1.5_0
VCC1.5_1
VCC1.5_2
VCC1.5_3
VCC1.5_4
VCC1.5_5
VCC1.5_6
VCC1.5_7
VCCRTC
VCCSUS3.3_0
VCCSUS3.3_1
VCCSUS3.3_2
VCCSUS3.3_3
VCCSUS3.3_4
VCCSUS3.3_5
VCCSUS3.3_6
VCCSUS3.3_7
VCCSUS3.3_8
VCCSUS3.3_9
ICH4-M
POWER
ICH4-M
19,21,22,24,37
+V3.3S_ICH
+V3.3S
R6H2
0.01_1%
C7J3
22UF
C7J2
22UF
C7W2
0.1UF
C7W5
0.1UF
C7W10
0.1UF
C7W13
0.1UF
C7W17
0.1UF
C7W9
0.1UF
15
+V1.5
R7G4
0.01_1%
+V1.5_ICHLAN
C8G2
22UF
C7W7
0.1UF
C7W8
0.1UF
+V3.3
R7G5
0.01_1%
15,18,19,23,27,30,32,35,37,38,39,43,44
18
+V3.3_ICHLAN
C7G7
22UF
C7W3
0.1UF
C7V3
0.1UF
C7G6
4.7UF
VCC5REF
+V5A_ICH
9,15,19,44,47,48
+V1.5S
R6G5
18
0.01_1%
+V1.5S_ICHHUB
C6H1
22UF
C7W14
0.1UF
C7W12
0.1UF
+V1.5S_ICH
+V1.5S
9,15,19,44,47,48
R7V3
0.01_1%
C7G5
100uF
C7G8
22UF
C7W11
0.1UF
C7W20
0.1UF
19,21
+V_RTC
C7J1
0.1UF
3,4,5,9,10,18,40,41,47,48
+VCC_IMVP
3,15,19,44,47,48
+V1.5S
0
R7V4
VCCPLL
C7V2
0.1UF
C7V1
0.01UF
R6H6
NO_STUFF_0.01_1%
C7W16
1UF
C7W22
0.1UF
For power measurement, cut the +VCC_IMVP plane and populate R6H6.
5,15,19,21,22,23,27,28,29,32,36,37,38,39,44,48
+V3.3ALWAYS
+V3.3ALWAYS_ICH
R7G1
0.01_1%
C7G4
22UF
C7V4
0.1UF
C7W21
0.1UF
C7W4
0.1UF
18,23,24,25,27,34,35,39,40,44,47
+V5S
19,21,22,24,37
+V3.3S_ICH
R8G5
1K
CR8G1
BAT54
VCC5REF
C7W1
1UF
C7W19
0.1UF
5,15,19,21,22,23,27,28,29,32,36,37,38,39,44,48
+V3.3ALWAYS
21,28,29
+V5_ALWAYS
R7V2
1K
CR7G2
BAT54
+V5A_ICH
C7G2
1UF
C7G3
0.1UF
+V3.3ALWAYS
C8J1
10UF
U8H2
IN
OUT
GND
POK
SHDN#
MAX8888
+V1.5ALWAYS
R8J2
10K
POK
R8J4
20k_1%
U8H3
SI3442DY
C8H1
10UF
0.1UF
C8J3
R8J9
10K
R8J11
10K
C8J2
10UF
PM_SLP_S4#_Q1
PM_SLP_S4#_Q2
Q8J3
BSS138
Q8J2
BSS138
5,15,19,21,22,23,27,28,29,32,36,37,38,39,44,48
+V3.3ALWAYS
R8J8
1K
R8J10
1K
39
V1.5_PWRGD
POK_DQ
CR8J1A
3904
CR8J1B
3904
POK_D
R8J5
470
PM_SLP_S4#
19,32,37,38,43,44
U7G2D
ICH4-M
VSS
VSS0
VSS1
VSS2
VSS3
VSS4
VSS5
VSS6
VSS7
VSS8
VSS9
VSS10
VSS11
VSS12
VSS13
VSS14
VSS15
VSS16
VSS17
VSS18
VSS19
VSS20
VSS21
VSS22
VSS23
VSS24
VSS25
VSS26
VSS27
VSS28
VSS29
VSS30
VSS31
VSS32
VSS33
VSS34
VSS35
VSS36
VSS37
VSS38
VSS39
VSS40
VSS41
VSS42
VSS43
VSS44
VSS45
VSS46
VSS47
VSS48
VSS49
VSS50
VSS51
VSS52
VSS53
VSS54
VSS55
VSS56
VSS57
VSS58
VSS59
VSS60
VSS61
VSS62
VSS63
VSS64
VSS65
VSS66
VSS67
VSS68
VSS69
VSS70
VSS71
VSS72
VSS73
VSS74
VSS75
VSS76
VSS77
VSS78
VSS79
VSS80
VSS81
VSS82
VSS83
VSS84
VSS85
VSS86
VSS87
VSS88
VSS89
VSS90
VSS91
VSS92
VSS93
VSS94
VSS95
VSS96
VSS97
VSS98
VSS99
VSS100
VSS101
Title
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## ICH4 Pullups

20,37 +V3.3ALWAYS_ICH

19,35,37 PM_RI#
18,37 SMB_ALERT#
RP8H6C 3 6 10K
RP8H7B 2 7 10K

19,20,22,24,37 +V3.3S_ICH

18,22,23,24 PCI_FRAME#
18,22,23,24 PCI_IRDY#
18,22,23,24 PCI_TRDY#
18,22,23,24 PCI_STOP#
18,22,23,24 PCI_SERR#
18,22,23,24 PCI_DEVSEL#
18,22,23 PCI_PERR#
18,22,23,24 PCI_LOCK#
18 PCI_REQ0#
18,22 PCI_REQ1#
18,22 PCI_REQ2#
18,23 PCI_REQ3#
18,24 PCI_REQ4#
18,26,37 INT_IRQ14
18,26,37 INT_IRQ15
15,18,23,24 INT_PIRQA#
15,18,23,24 INT_PIRQB#
18,23,24 INT_PIRQC#
18,23,24 INT_PIRQD#
18,22,23 INT_PIRQE#
18,22,23 INT_PIRQF#
18,22,23 INT_PIRQG#
18,22,23,37 INT_PIRQH#
22,23 PCI_REQ64#
22,23 PCI_ACK64#
19,22,23,24,32,34,37 PM_CLKRUN#

RP8H2D 4 5 8.2K
RP8H3C 3 6 8.2K
RP8H2C 3 6 8.2K
RP8H2B 2 7 8.2K
RP8H2A 1 8 8.2K
RP8H3A 1 8 8.2K
RP8H3D 4 5 8.2K
RP8H3B 2 7 8.2K
RP8H1C 3 6 8.2K
RP8G3C 3 6 8.2K
RP8G2A 1 8 8.2K
RP8H1B 2 7 8.2K
RP8H1D 4 5 8.2K
RP7J1D 4 5 8.2K
RP7J1A 1 8 8.2K
RP8H1A 1 8 8.2K
RP8G3A 1 8 8.2K
RP8G3B 2 7 8.2K
RP8G3D 4 5 8.2K
RP7F2A 1 8 8.2K
RP7F2C 3 6 8.2K
RP7F2B 2 7 8.2K
RP7F2D 4 5 8.2K
RP7E1A 1 8 10K
RP7E1B 2 7 10K
RP8H7D 4 5 10K

19,20 +V_RTC

18,37 SM_INTRUDER# R2J4 100K

5,6,8,9,11,16,18,20,23,26,31,33,34,35,36,38,39,40,41,44,48 +V3.3S

5,19,32,37 PM_THRM# R8H2 8.2K

19,25,32,37,39 PM_PWROK
19,32,37 PM_RSMRST#
R8H4 100K
R8J6 100K

20,37 +V3.3ALWAYS_ICH

18,22,23,24,47 SMB_CLK R8J1 2.2k
18,22,23,24,47 SMB_DATA R8J3 2.2k

## +V5_ALWAYS Generation

+V5 20,22,23,27,36,37,43,44
+V3.3ALWAYS 5,15,19,20,22,23,27,28,29,32,36,37,38,39,44,48
+VDC 15,16,44

R5P7 100K_1%
39 V5A_PWRGD
R5P6 NO_STUFF_680K

Vout=0.8(1+Rtop/Rbot)
Vout=0.8(1+(3.92k/750))= 4.98V
IMAX OUT = 50mV / 10mohms = 5A

Place these caps near U5C3

U5C3 LTC1735-1
COSC, RUN/SS, ITH, SGND, VOSENSE, SENSE-, SENSE+, EXTVCC, PGOOD, TG, BOOST, SW, VIN, INTVCC, BG, PGND

V5A_COSC
RUN_SS
V5A_ITH
V5A_ITH_D
V5A_TG
V5A_BOOST
V5A_SW
V5A_INTVCC
V5A_BG
V5A_BG_D
V5A_SENSE+
V5A_SENSE-
V5A_VOSENSE

C5C16 47pF
C5C14 3300pF
R5C8 37.4k_1%
C5P5 47pF
C5P6 330pF
C5C11 47pF
C5C15 1000PF
C5P1 0.47uF
C5P2 1UF
C5C12 10UF
C5P4 0.1UF

Q5C1A Si4966DY
Q5C1B Si4966DY
CR5C3 MBR0520LT1
CR5C1 B320A
L5C1 4.7uH
R4C16 0.01_1%
R5C7 10_1%
R5C9 10_1%
R5C6 3.92k_1%
R5C5 750_1%

+V5_ALWAYS 20,28,29

## FAB REVISION

19,20,22,24,37 +V3.3S_ICH

R6F20 NO_STUFF_10K
R6F19 10K
R7F8 NO_STUFF_10K
19 ICH_FAB_REV0
19 ICH_FAB_REV1
19 ICH_FAB_REV2
R6F24 10K
R6F23 NO_STUFF_10K
R7F5 10K

### FAB ID Strapping Table

| ICH_FAB_REV 2 | 1 | 0 | BOARD FAB |
|---|---|---|---|
| 0 | 0 | 0 | 1 |
| 0 | 0 | 1 | 2 |
| 0 | 1 | 0 | 3 |
| 0 | 1 | 1 | 4 |
| 1 | 0 | 0 | 5 |
| 1 | 0 | 1 | 6 |
| 1 | 1 | 0 | 7 |
| 1 | 1 | 1 | 8 |

+V5 C5C10 0.1UF
Please place C5C10 near U5C3 Pin 9

20,22,23,27,36,37,43,44 +VDC
C5P3 100pF 10%
C5C3 22UF
Please place C5P3 and C5C3 near U5C3.

15,16,44
+V5_ALWAYS 20,28,29
C4C6 150UF
C4C7 0.1UF
Please place C4C6 and C4P7 near R5C5.

GND_V5A R5P8 0

| | | | |
|---|---|---|---|
| Title | ICH4-M Pullups and Testpoints | | |
| Size A | Project: | Document Number | Rev |
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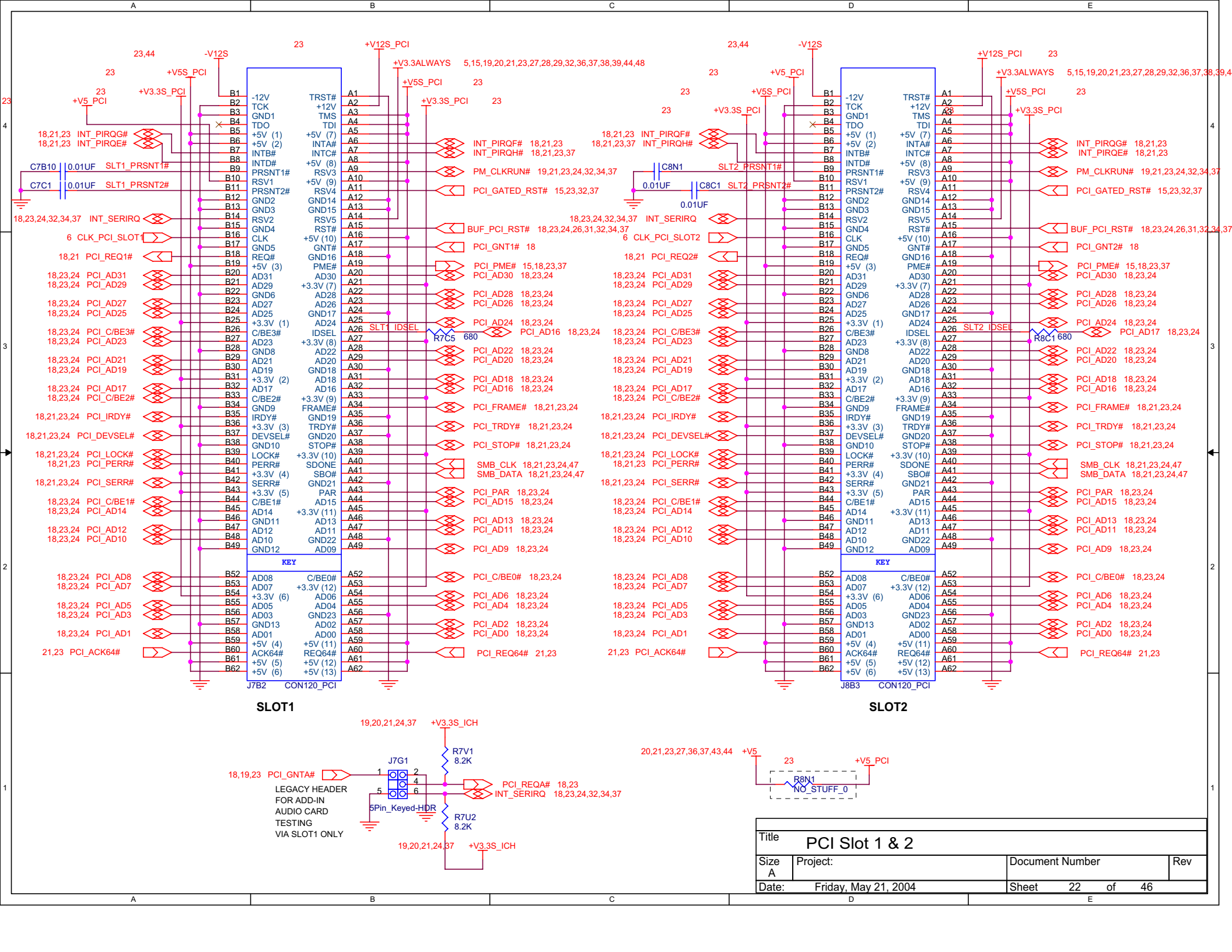
SLOT1
SLOT2
J7B2 CON120_PCI
J8B3 CON120_PCI
KEY
-12V
TCK
GND1
TDO
+5V (1)
+5V (2)
INTB#
INTD#
PRSNT1#
RSV1
PRSNT2#
GND2
GND3
RSV2
GND4
CLK
GND5
REQ#
+5V (3)
AD31
AD29
GND6
AD27
AD25
+3.3V (1)
C/BE3#
AD23
GND8
AD21
AD19
+3.3V (2)
AD17
C/BE2#
GND9
IRDY#
+3.3V (3)
DEVSEL#
GND10
LOCK#
PERR#
+3.3V (4)
SERR#
+3.3V (5)
C/BE1#
AD14
GND11
AD12
AD10
GND12
AD08
AD07
+3.3V (6)
AD05
AD03
GND13
AD01
+5V (4)
ACK64#
+5V (5)
+5V (6)
TRST#
+12V
TMS
TDI
+5V (7)
INTA#
INTC#
+5V (8)
RSV3
+5V (9)
RSV4
GND14
GND15
RSV5
RST#
+5V (10)
GNT#
GND16
PME#
AD30
+3.3V (7)
AD28
AD26
GND17
AD24
IDSEL
+3.3V (8)
AD22
AD20
GND18
AD18
AD16
+3.3V (9)
FRAME#
GND19
TRDY#
GND20
STOP#
+3.3V (10)
SDONE
SBO#
GND21
PAR
AD15
+3.3V (11)
AD13
AD11
GND22
AD09
C/BE0#
+3.3V (12)
AD06
AD04
GND23
AD02
AD00
+5V (11)
REQ64#
+5V (12)
+5V (13)
INT_PIRQG# 18,21,23
INT_PIRQE# 18,21,23
INT_PIRQF# 18,21,23
INT_PIRQH# 18,21,23,37
PM_CLKRUN# 19,21,23,24,32,34,37
PCI_GATED_RST# 15,23,32,37
BUF_PCI_RST# 18,23,24,26,31,32,34,37
PCI_GNT1# 18
PCI_GNT2# 18
PCI_PME# 15,18,23,37
PCI_AD30 18,23,24
PCI_AD28 18,23,24
PCI_AD26 18,23,24
PCI_AD24 18,23,24
PCI_AD16 18,23,24
PCI_AD22 18,23,24
PCI_AD20 18,23,24
PCI_AD18 18,23,24
PCI_FRAME# 18,21,23,24
PCI_TRDY# 18,21,23,24
PCI_STOP# 18,21,23,24
SMB_CLK 18,21,23,24,47
SMB_DATA 18,21,23,24,47
PCI_PAR 18,23,24
PCI_AD15 18,23,24
PCI_AD13 18,23,24
PCI_AD11 18,23,24
PCI_AD9 18,23,24
PCI_C/BE0# 18,23,24
PCI_AD6 18,23,24
PCI_AD4 18,23,24
PCI_AD2 18,23,24
PCI_AD0 18,23,24
PCI_REQ64# 21,23
INT_SERIRQ 18,23,24,32,34,37
CLK_PCI_SLOT1
CLK_PCI_SLOT2
PCI_REQ1#
PCI_REQ2#
PCI_AD31
PCI_AD29
PCI_AD27
PCI_AD25
PCI_C/BE3#
PCI_AD23
PCI_AD21
PCI_AD19
PCI_AD17
PCI_C/BE2#
PCI_IRDY#
PCI_DEVSEL#
PCI_LOCK#
PCI_PERR#
PCI_SERR#
PCI_C/BE1#
PCI_AD14
PCI_AD12
PCI_AD10
PCI_AD8
PCI_AD7
PCI_AD5
PCI_AD3
PCI_AD1
ACK64#
SLT1_PRSNT1#
SLT1_PRSNT2#
SLT1_IDSEL
SLT2_PRSNT1#
SLT2_PRSNT2#
SLT2_IDSEL
C7B10 0.01UF
C7C1 0.01UF
C8N1
C8C1 0.01UF
R7C5 680
R8C1 680
+V12S
-V12S
+V5S_PCI
+V3.3S_PCI
+V5_PCI
+V3.3ALWAYS 5,15,19,20,21,23,27,28,29,32,36,37,38,39,44,48
+V3.3S_ICH
+V5 20,21,23,27,36,37,43,44
R7V1 8.2K
R7U2 8.2K
J7G1
5Pin_Keyed-HDR
18,19,23 PCI_GNTA#
LEGACY HEADER
FOR ADD-IN
AUDIO CARD
TESTING
VIA SLOT1 ONLY
PCI_REQA# 18,23
INT_SERIRQ 18,23,24,32,34,37
R8N1
NO_STUFF_0
Title PCI Slot 1 & 2
Size A
Project:
Document Number
Rev
Date: Friday, May 21, 2004
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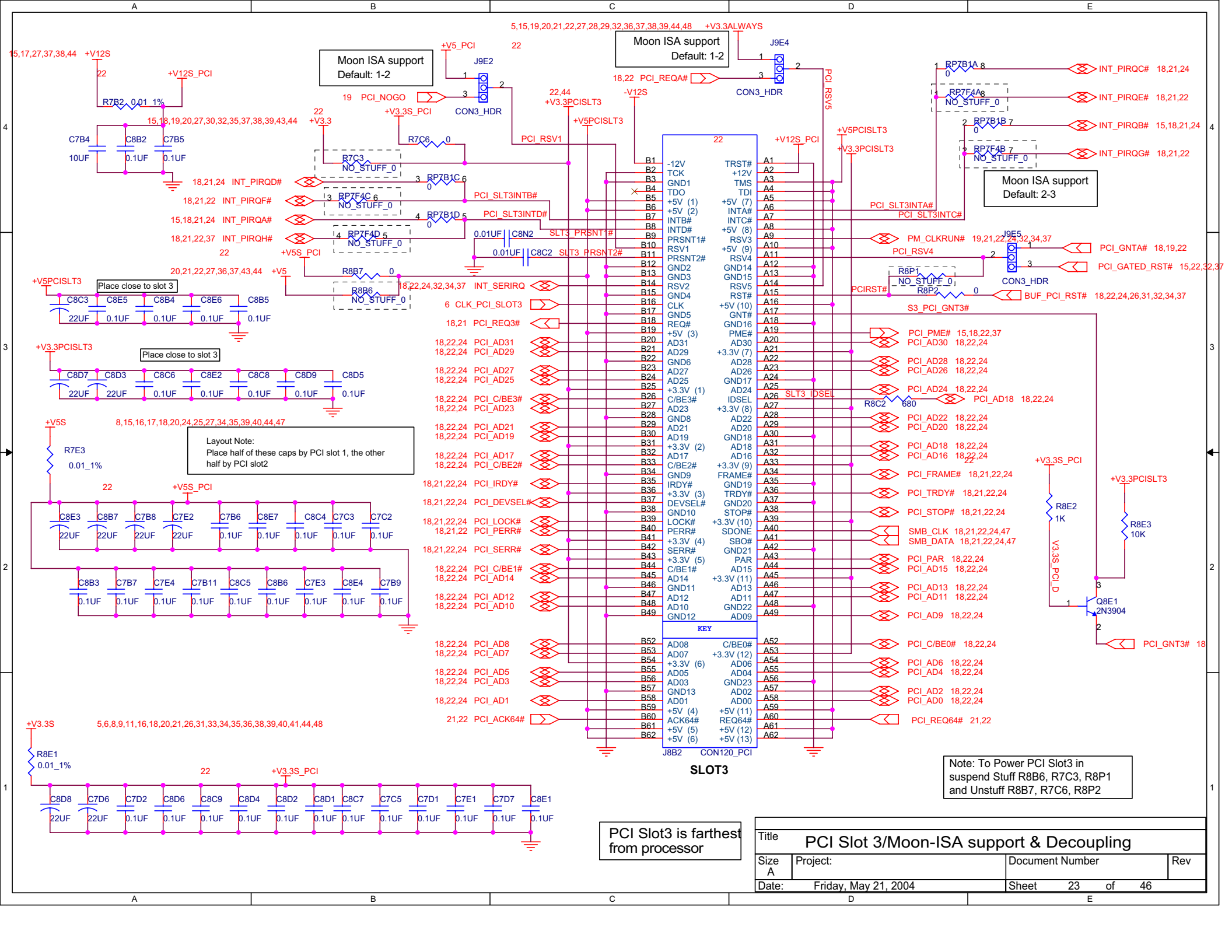
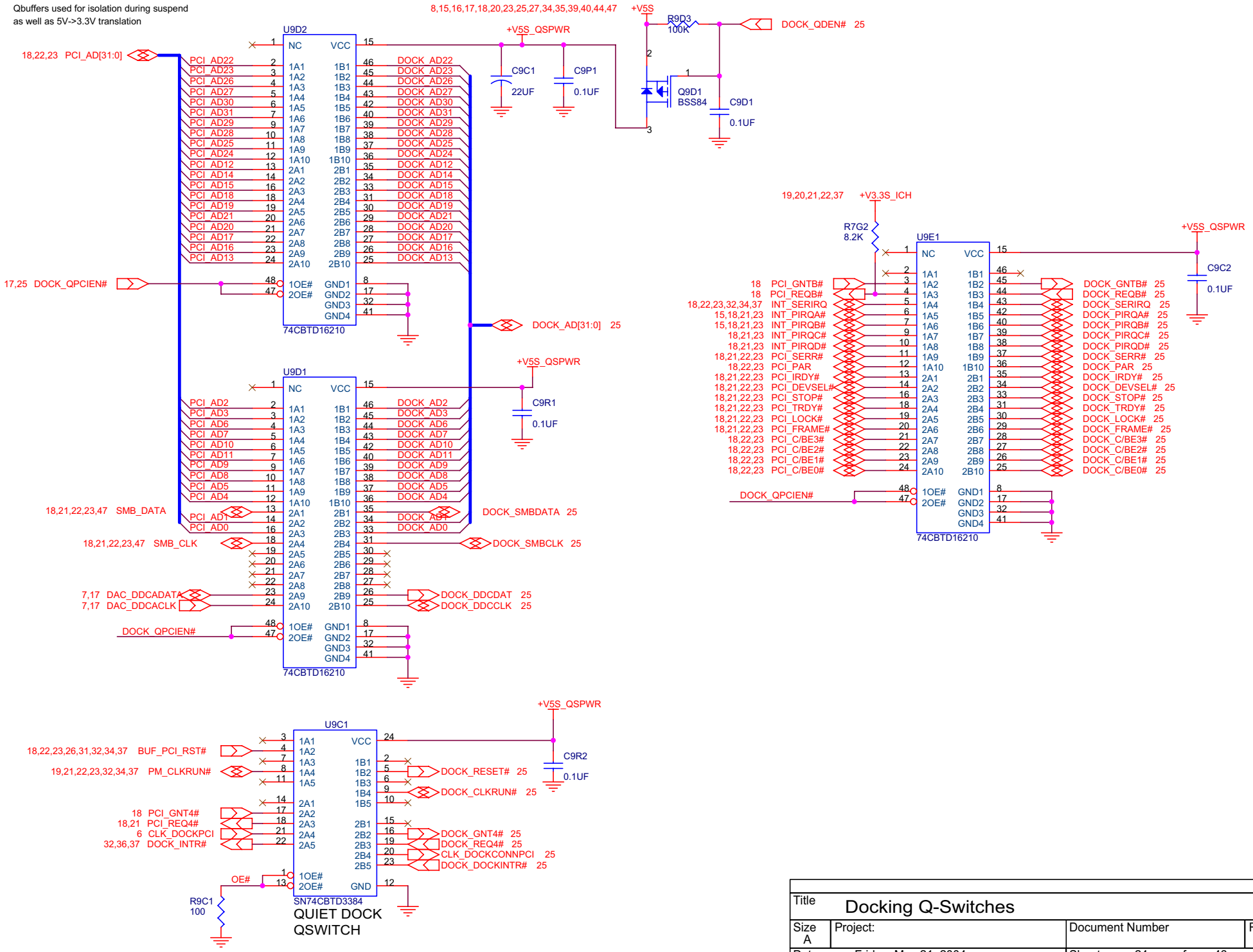
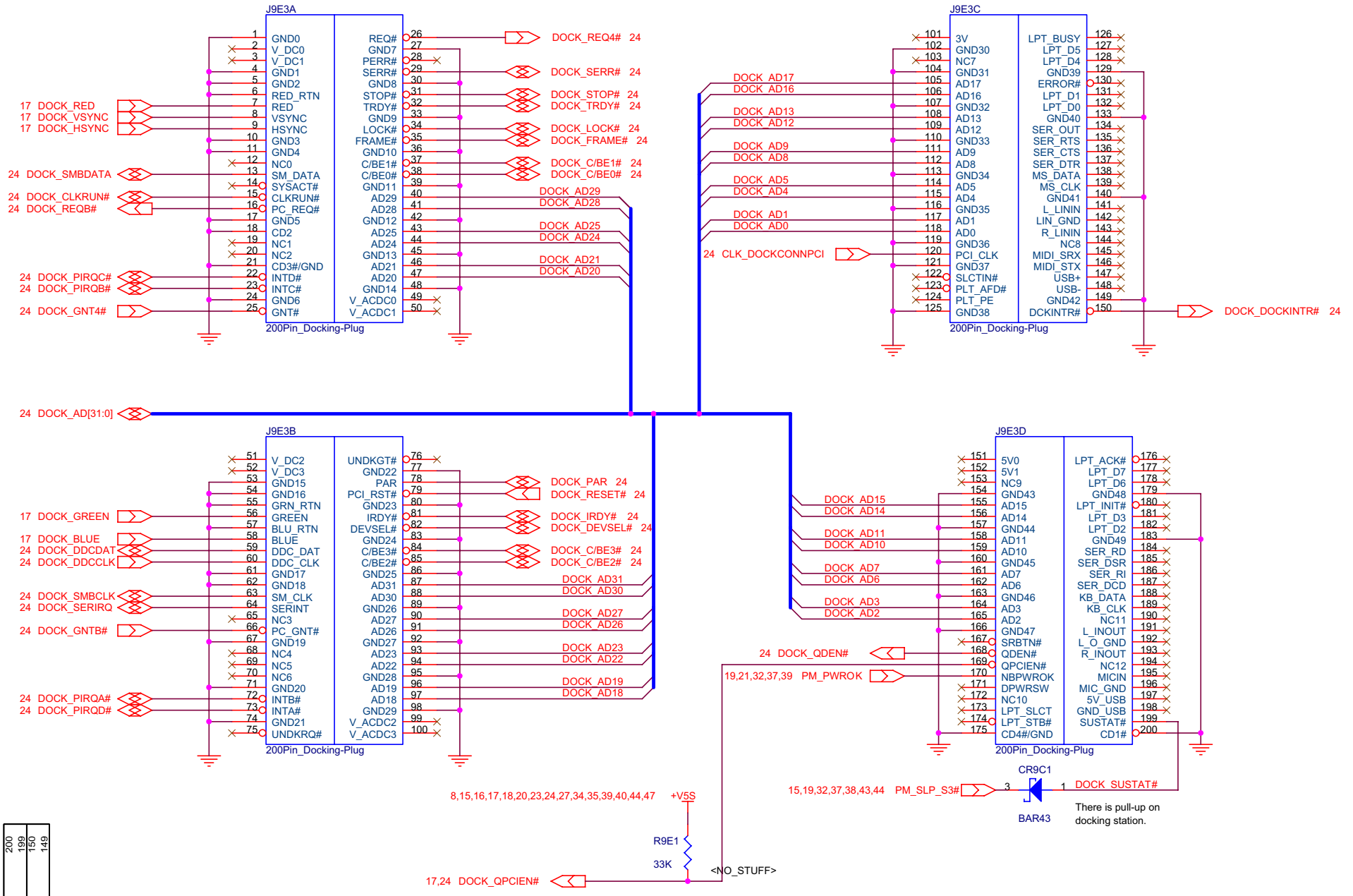

Moon ISA support
Default: 1-2
Moon ISA support
Default: 1-2
Moon ISA support
Default: 2-3
SLOT3
Place close to slot 3
Place close to slot 3
Layout Note:
Place half of these caps by PCI slot 1, the other half by PCI slot2
Note: To Power PCI Slot3 in suspend Stuff R8B6, R7C3, R8P1 and Unstuff R8B7, R7C6, R8P2
PCI Slot3 is farthest from processor
Title
PCI Slot 3/Moon-ISA support & Decoupling
Size A
Project:
Document Number
Rev
Date: Friday, May 21, 2004
Sheet 23 of 46

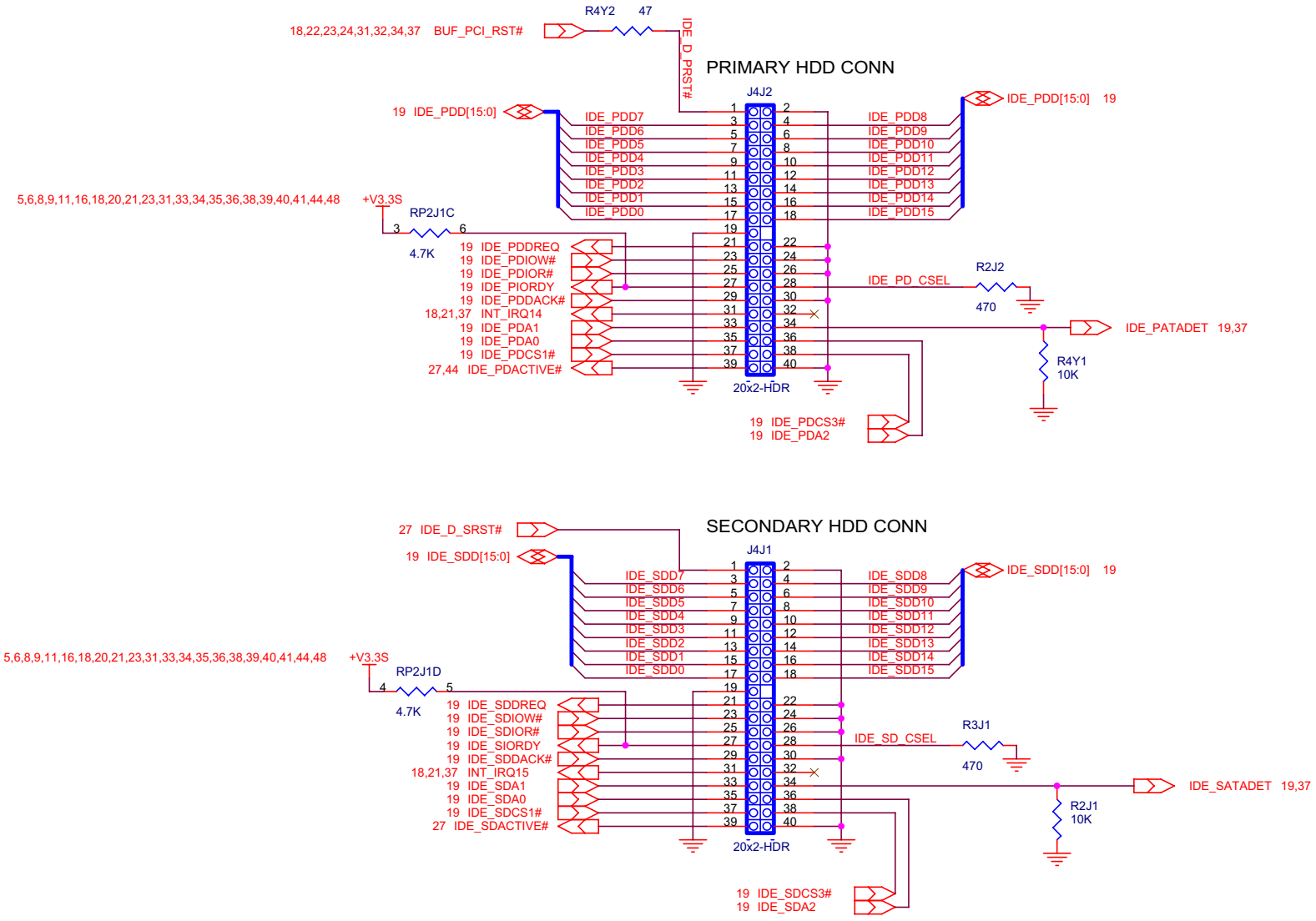
Qbuffers used for isolation during suspend
as well as 5V->3.3V translation



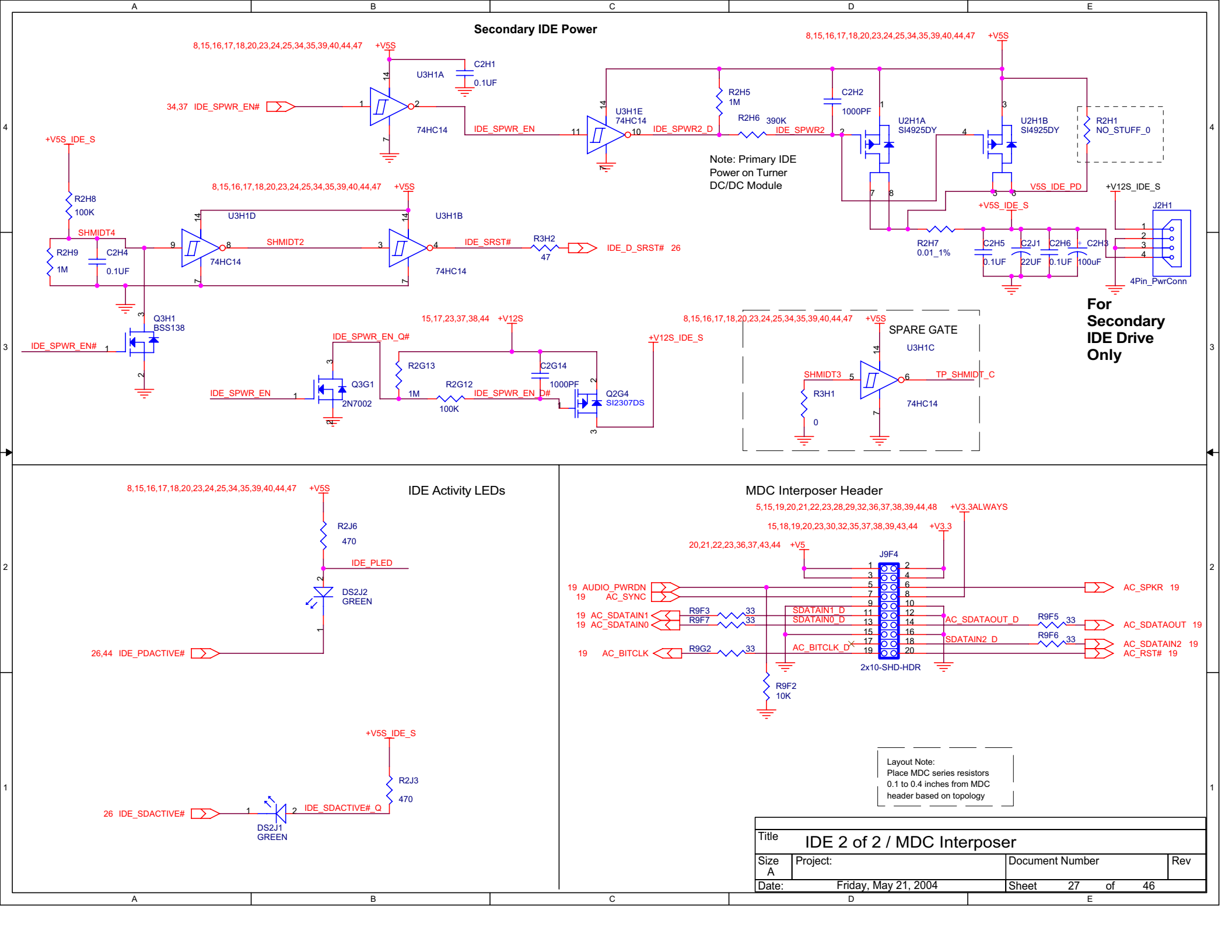

| | | | |
|---|---|---|---|
| Title | Docking Q-Switches | | |
| Size A | Project: | Document Number | Rev |
| Date: Friday, May 21, 2004 | | Sheet 24 of 46 | |




| | | | |
|---|---|---|---|
| Title | Docking Connector | | |
| Size A | Project: | Document Number | Rev |
| Date: Friday, May 21, 2004 | | Sheet 25 of 46 | |




| | | | |
|---|---|---|---|
| Title | IDE 1 of 2 | | |
| Size A | Project: | Document Number | Rev |
| Date: Friday, May 21, 2004 | | Sheet 26 of 46 | |


Secondary IDE Power
8,15,16,17,18,20,23,24,25,34,35,39,40,44,47 +V5S
U3H1A
C2H1
0.1UF
34,37 IDE_SPWR_EN#
74HC14
IDE_SPWR_EN
U3H1E
74HC14
IDE_SPWR2_D
R2H5
1M
R2H6 390K
IDE_SPWR2
C2H2
1000PF
U2H1A
SI4925DY
U2H1B
SI4925DY
R2H1
NO_STUFF_0
V5S_IDE_PD
+V12S_IDE_S
J2H1
4Pin_PwrConn
Note: Primary IDE Power on Turner DC/DC Module
+V5S_IDE_S
R2H8
100K
SHMIDT4
R2H9
1M
C2H4
0.1UF
U3H1D
U3H1B
SHMIDT2
IDE_SRST#
R3H2
47
IDE_D_SRST# 26
R2H7
0.01_1%
C2H5
0.1UF
C2J1
22UF
C2H6
0.1UF
C2H3
100uF
Q3H1
BSS138
IDE_SPWR_EN#
15,17,23,37,38,44 +V12S
IDE_SPWR_EN_Q#
+V12S_IDE_S
R2G13
1M
R2G12
100K
C2G14
1000PF
Q3G1
2N7002
Q2G4
SI2307DS
IDE_SPWR_EN
IDE_SPWR_EN_D#
SPARE GATE
U3H1C
SHMIDT3
R3H1
0
TP_SHMIDT_C
For Secondary IDE Drive Only
IDE Activity LEDs
R2J6
470
IDE_PLED
DS2J2
GREEN
26,44 IDE_PDACTIVE#
+V5S_IDE_S
R2J3
470
26 IDE_SDACTIVE#
IDE_SDACTIVE#_Q
DS2J1
GREEN
MDC Interposer Header
5,15,19,20,21,22,23,28,29,32,36,37,38,39,44,48 +V3.3ALWAYS
15,18,19,20,23,30,32,35,37,38,39,43,44 +V3.3
20,21,22,23,36,37,43,44 +V5
J9F4
2x10-SHD-HDR
19 AUDIO_PWRDN
19 AC_SYNC
AC_SPKR 19
19 AC_SDATAIN1
19 AC_SDATAIN0
R9F3
R9F7
SDATAIN1_D
SDATAIN0_D
AC_SDATAOUT_D
R9F5
AC_SDATAOUT 19
SDATAIN2_D
R9F6
AC_SDATAIN2 19
19 AC_BITCLK
R9G2
AC_BITCLK_D
AC_RST# 19
R9F2
10K
Layout Note:
Place MDC series resistors
0.1 to 0.4 inches from MDC
header based on topology
Title
IDE 2 of 2 / MDC Interposer
Size A
Project:
Document Number
Rev
Date: Friday, May 21, 2004
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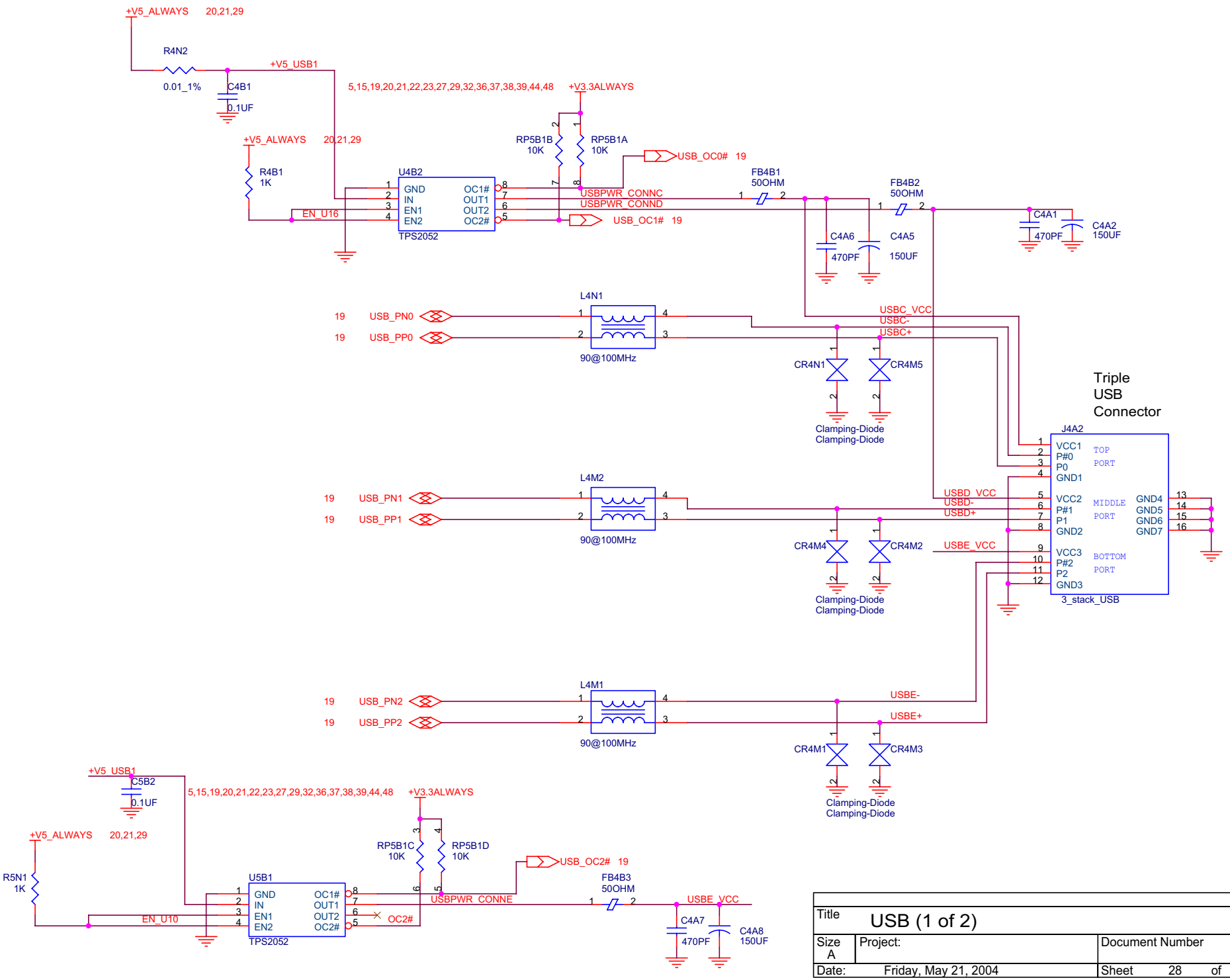
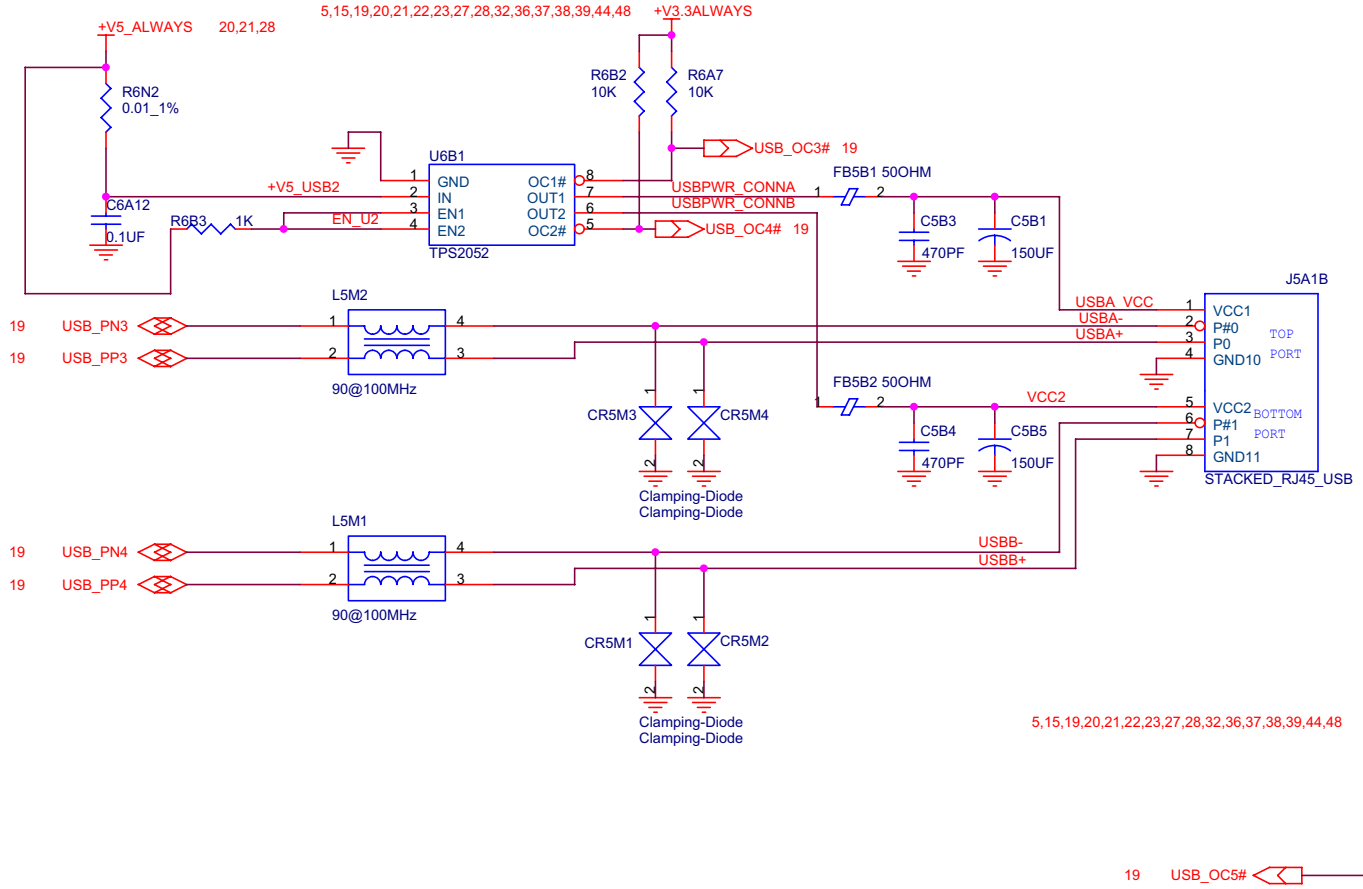
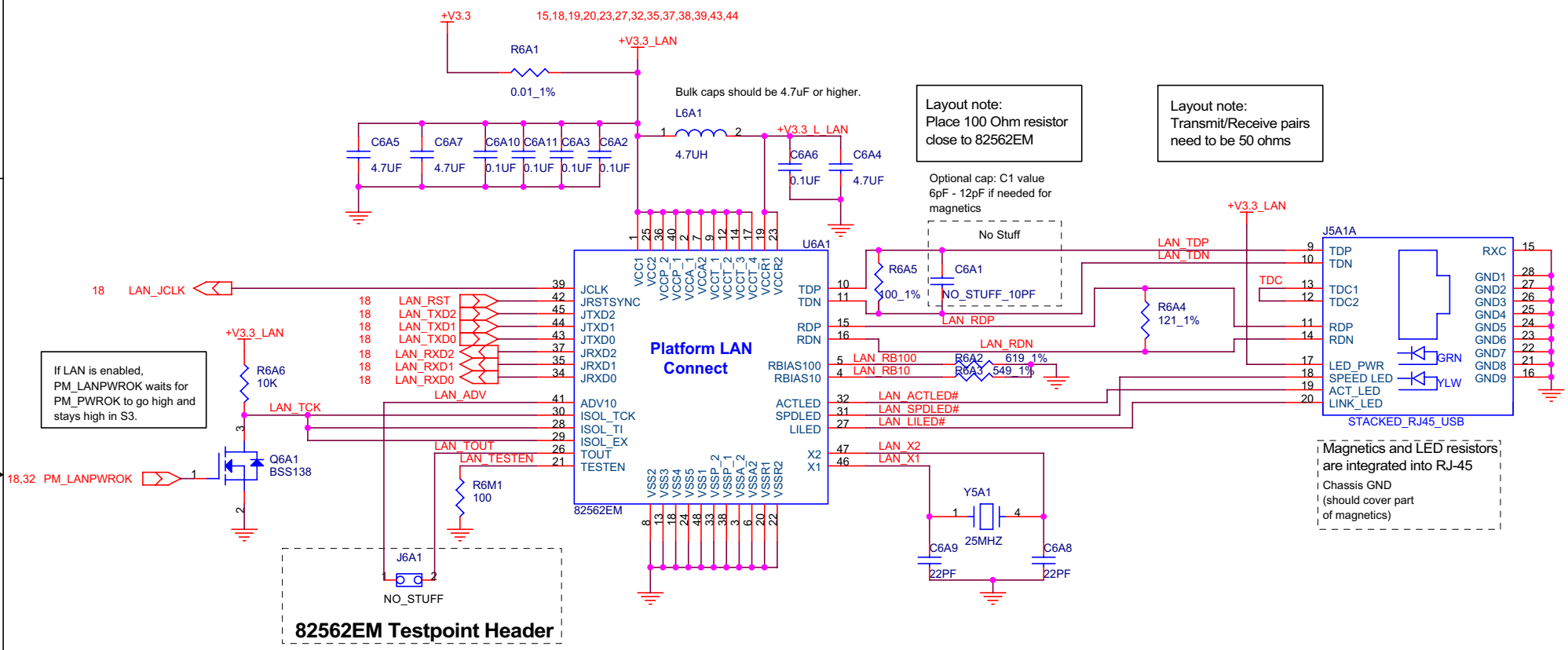


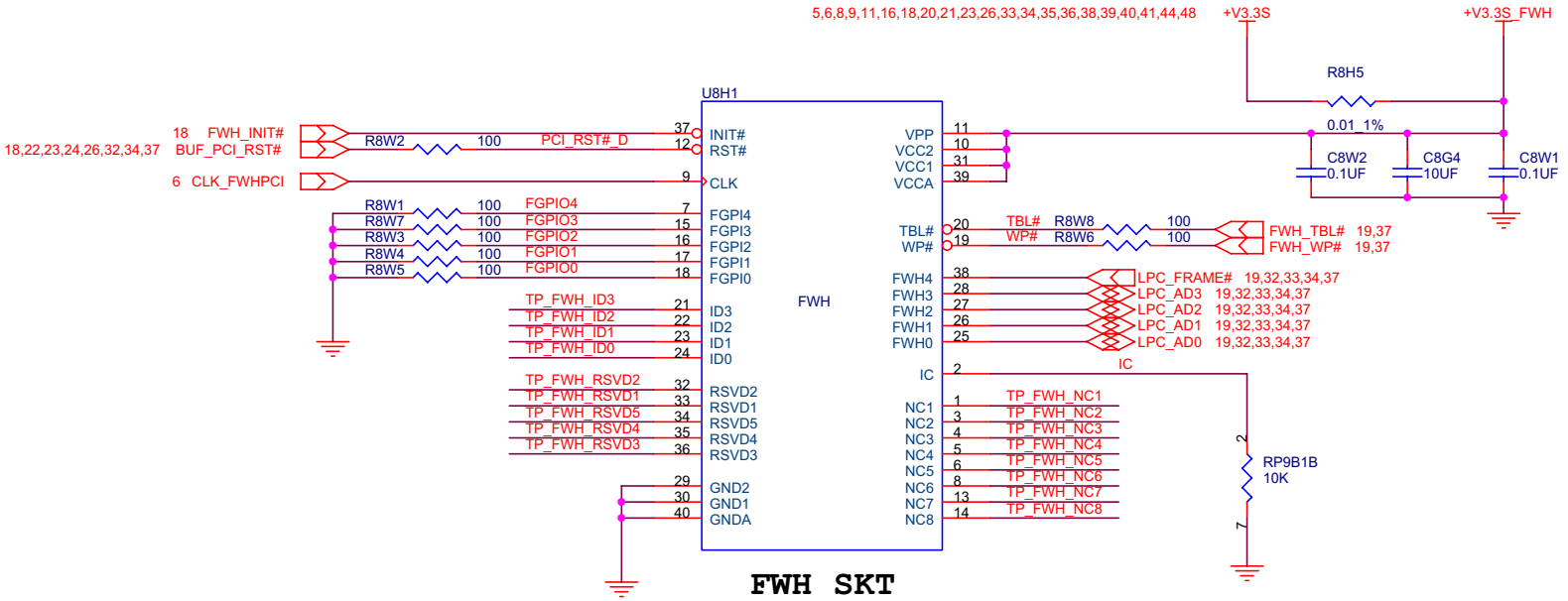

| | | | |
|---|---|---|---|
| Title | USB (1 of 2) | | |
| Size A | Project: | Document Number | Rev |
| Date: Friday, May 21, 2004 | | Sheet 28 of 46 | |




| | | | |
|---|---|---|---|
| Title | USB Connector (2 of 2) | | |
| Size A | Project: | Document Number | Rev |
| Date: Friday, May 21, 2004 | | Sheet 29 of 46 | |



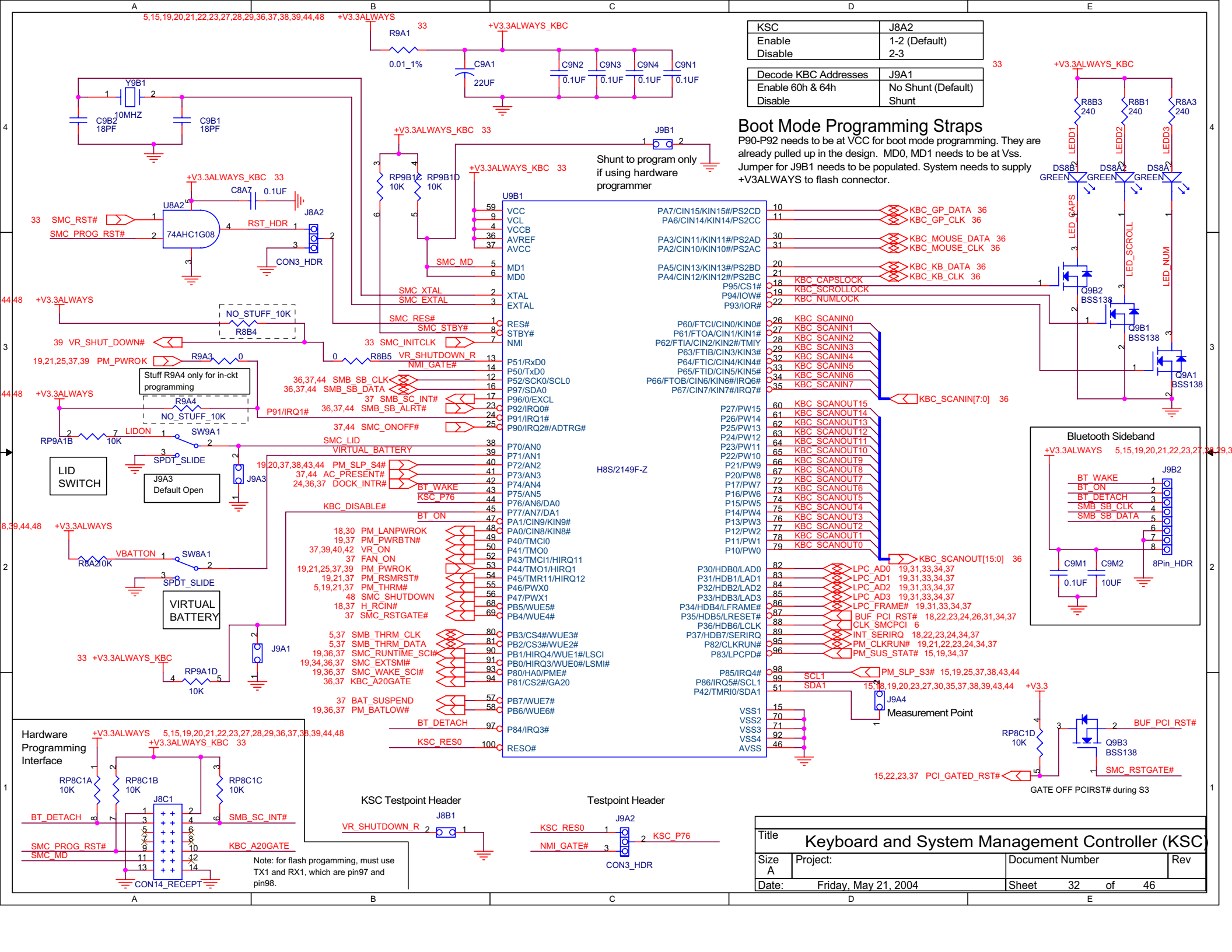

| | | | |
|---|---|---|---|
| Title | LAN Interface (82562EM) | | |
| Size A | Project: | Document Number | Rev |
| Date: Friday, May 21, 2004 | | Sheet 30 of 46 | |



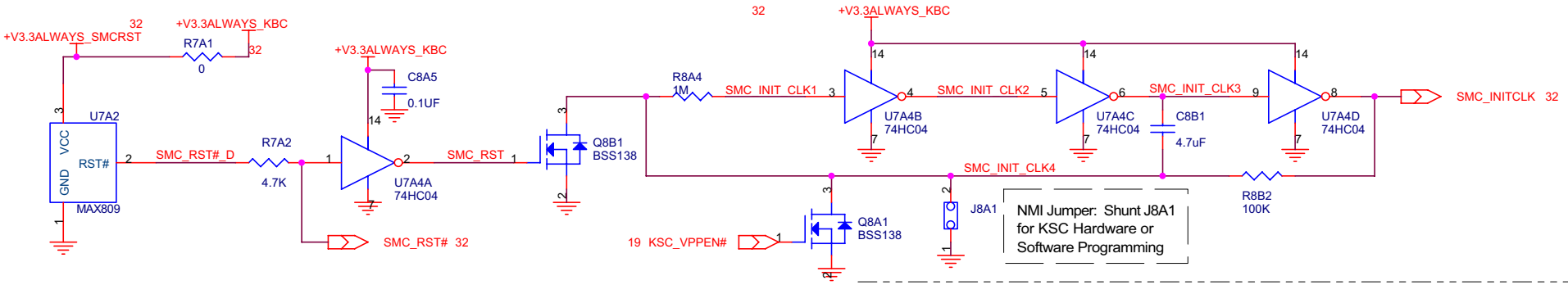

**FWH SKT**

FWH sits in the
FWH_TSOP_Socket,
Not on the board

| | | | |
|---|---|---|---|
| Title: Firmware Hub | | | |
| Size: A | Project: | Document Number | Rev |
| Date: Friday, May 21, 2004 | | Sheet 31 of 46 | |

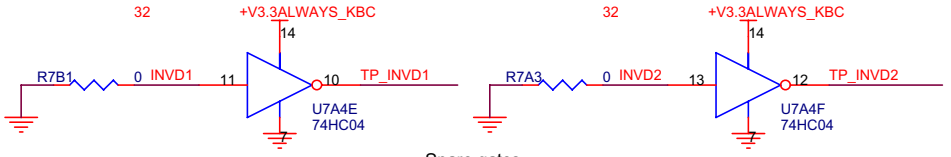

KSC | J8A2
Enable | 1-2 (Default)
Disable | 2-3
Decode KBC Addresses | J9A1
Enable 60h & 64h | No Shunt (Default)
Disable | Shunt
Boot Mode Programming Straps
P90-P92 needs to be at VCC for boot mode programming. They are already pulled up in the design. MD0, MD1 needs to be at Vss. Jumper for J9B1 needs to be populated. System needs to supply +V3ALWAYS to flash connector.
Shunt to program only if using hardware programmer
H8S/2149F-Z
LID SWITCH
VIRTUAL BATTERY
Bluetooth Sideband
Hardware Programming Interface
KSC Testpoint Header
Testpoint Header
Measurement Point
GATE OFF PCIRST# during S3
Note: for flash progamming, must use TX1 and RX1, which are pin97 and pin98.
Title
Keyboard and System Management Controller (KSC)
Size A
Project:
Document Number
Rev
Date: Friday, May 21, 2004
Sheet 32 of 46

# KSC SUSPEND TIMER



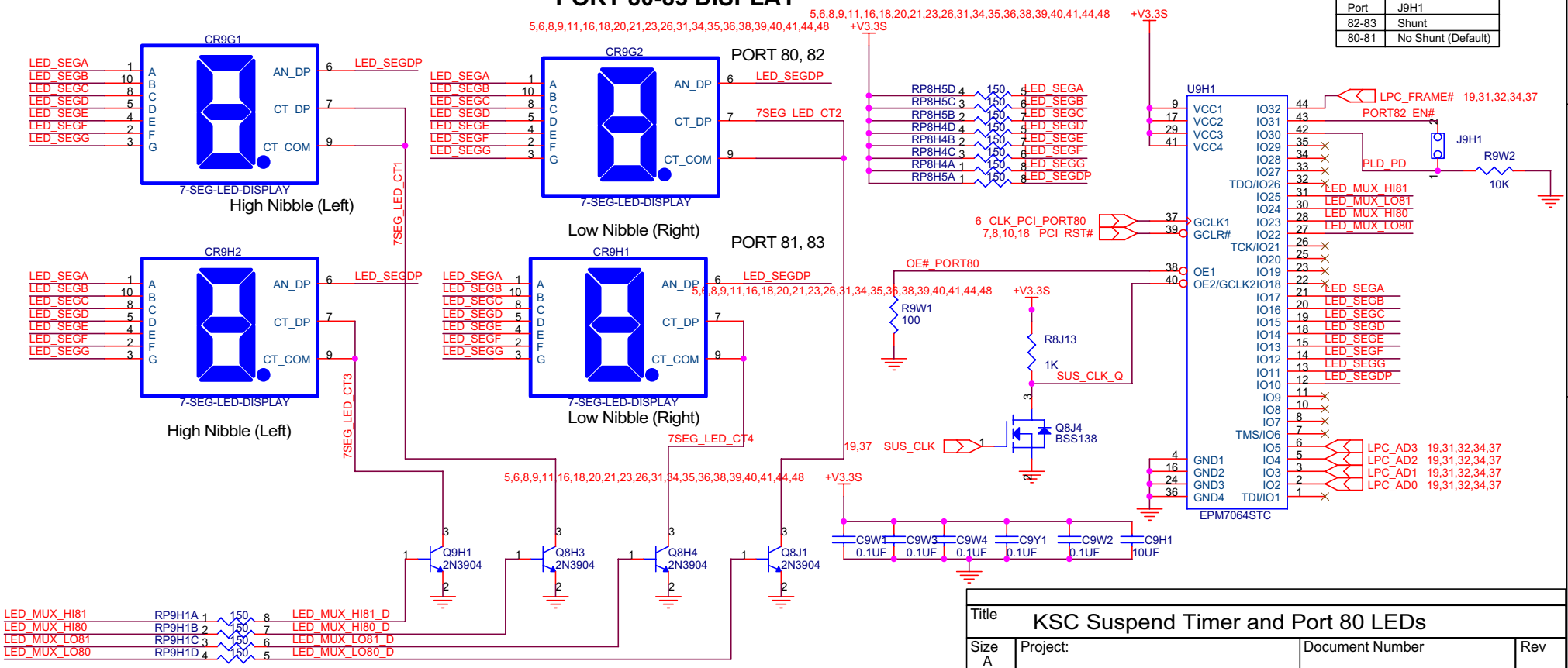

Circuitry provides an interrupt to the KSC every 1s while in suspend (this allows the KSC to complete housekeeping functions while suspended)

| 1Hz Clock | J8A1 |
|---|---|
| Disable | Shunt (Default) |
| Enable | No Shunt |

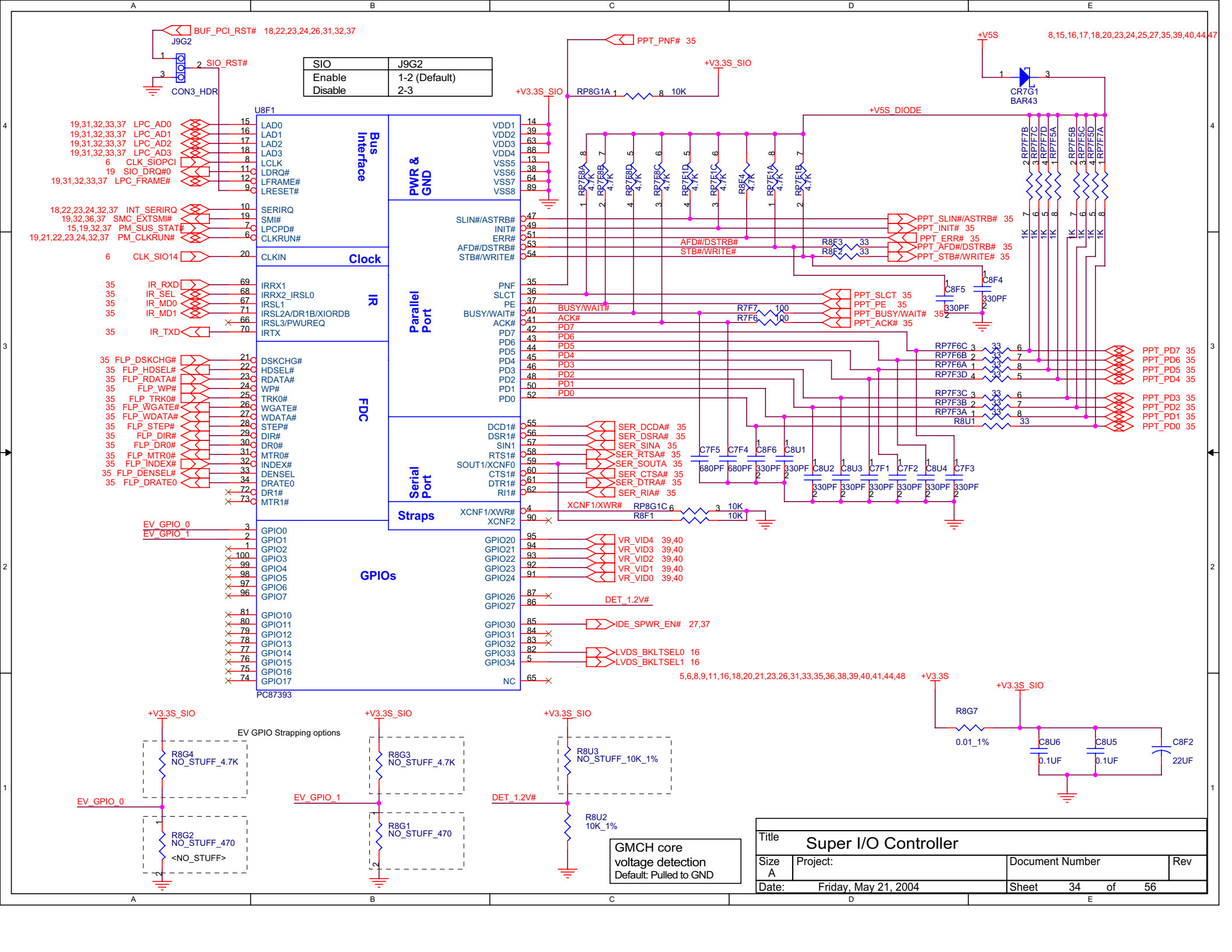



# PORT 80-83 DISPLAY

| Port | J9H1 |
|---|---|
| 82-83 | Shunt |
| 80-81 | No Shunt (Default) |




| Title | KSC Suspend Timer and Port 80 LEDs | | |
|---|---|---|---|
| Size A | Project: | Document Number | Rev |
| Date: Friday, May 21, 2004 | | Sheet 33 of 46 | |


BUF_PCI_RST# 18,22,23,24,26,31,32,37
J9G2
SIO_RST#
CON3_HDR
SIO | J9G2
Enable | 1-2 (Default)
Disable | 2-3
U8F1
PC87393
Bus Interface
PWR & GND
Clock
IR
Parallel Port
FDC
Serial Port
Straps
GPIOs
LAD0
LAD1
LAD2
LAD3
LCLK
LDRQ#
LFRAME#
LRESET#
SERIRQ
SMI#
LPCPD#
CLKRUN#
CLKIN
IRRX1
IRRX2_IRSL0
IRSL1
IRSL2A/DR1B/XIORDB
IRSL3/PWUREQ
IRTX
DSKCHG#
HDSEL#
RDATA#
WP#
TRK0#
WGATE#
WDATA#
STEP#
DIR#
DR0#
MTR0#
INDEX#
DENSEL
DRATE0
DR1#
MTR1#
GPIO0
GPIO1
GPIO2
GPIO3
GPIO4
GPIO5
GPIO6
GPIO7
GPIO10
GPIO11
GPIO12
GPIO13
GPIO14
GPIO15
GPIO16
GPIO17
VDD1
VDD2
VDD3
VDD4
VSS5
VSS6
VSS7
VSS8
SLIN#/ASTRB#
INIT#
ERR#
AFD#/DSTRB#
STB#/WRITE#
PNF
SLCT
PE
BUSY/WAIT#
ACK#
PD7
PD6
PD5
PD4
PD3
PD2
PD1
PD0
DCD1#
DSR1#
SIN1
RTS1#
SOUT1/XCNF0
CTS1#
DTR1#
RI1#
XCNF1/XWR#
XCNF2
GPIO20
GPIO21
GPIO22
GPIO23
GPIO24
GPIO26
GPIO27
GPIO30
GPIO31
GPIO32
GPIO33
GPIO34
NC
PPT_PNF# 35
+V3.3S_SIO
RP8G1A 10K
+V5S
CR7G1 BAR43
+V5S_DIODE
8,15,16,17,18,20,23,24,25,27,35,39,40,44,47
PPT_SLIN#/ASTRB# 35
PPT_INIT# 35
PPT_ERR# 35
PPT_AFD#/DSTRB# 35
PPT_STB#/WRITE# 35
PPT_SLCT 35
PPT_PE 35
PPT_BUSY/WAIT# 35
PPT_ACK# 35
PPT_PD7 35
PPT_PD6 35
PPT_PD5 35
PPT_PD4 35
PPT_PD3 35
PPT_PD2 35
PPT_PD1 35
PPT_PD0 35
SER_DCDA# 35
SER_DSRA# 35
SER_SINA 35
SER_RTSA# 35
SER_SOUTA 35
SER_CTSA# 35
SER_DTRA# 35
SER_RIA# 35
VR_VID4 39,40
VR_VID3 39,40
VR_VID2 39,40
VR_VID1 39,40
VR_VID0 39,40
DET_1.2V#
IDE_SPWR_EN# 27,37
LVDS_BKLTSEL0 16
LVDS_BKLTSEL1 16
5,6,8,9,11,16,18,20,21,23,26,31,33,35,36,38,39,40,41,44,48
+V3.3S
R8G7 0.01_1%
C8U6 0.1UF
C8U5 0.1UF
C8F2 22UF
EV GPIO Strapping options
R8G4 NO_STUFF_4.7K
R8G2 NO_STUFF_470 <NO_STUFF>
R8G3 NO_STUFF_4.7K
R8G1 NO_STUFF_470
R8U3 NO_STUFF_10K_1%
R8U2 10K_1%
GMCH core voltage detection
Default: Pulled to GND
Title: Super I/O Controller
Size: A
Project:
Document Number
Rev
Date: Friday, May 21, 2004
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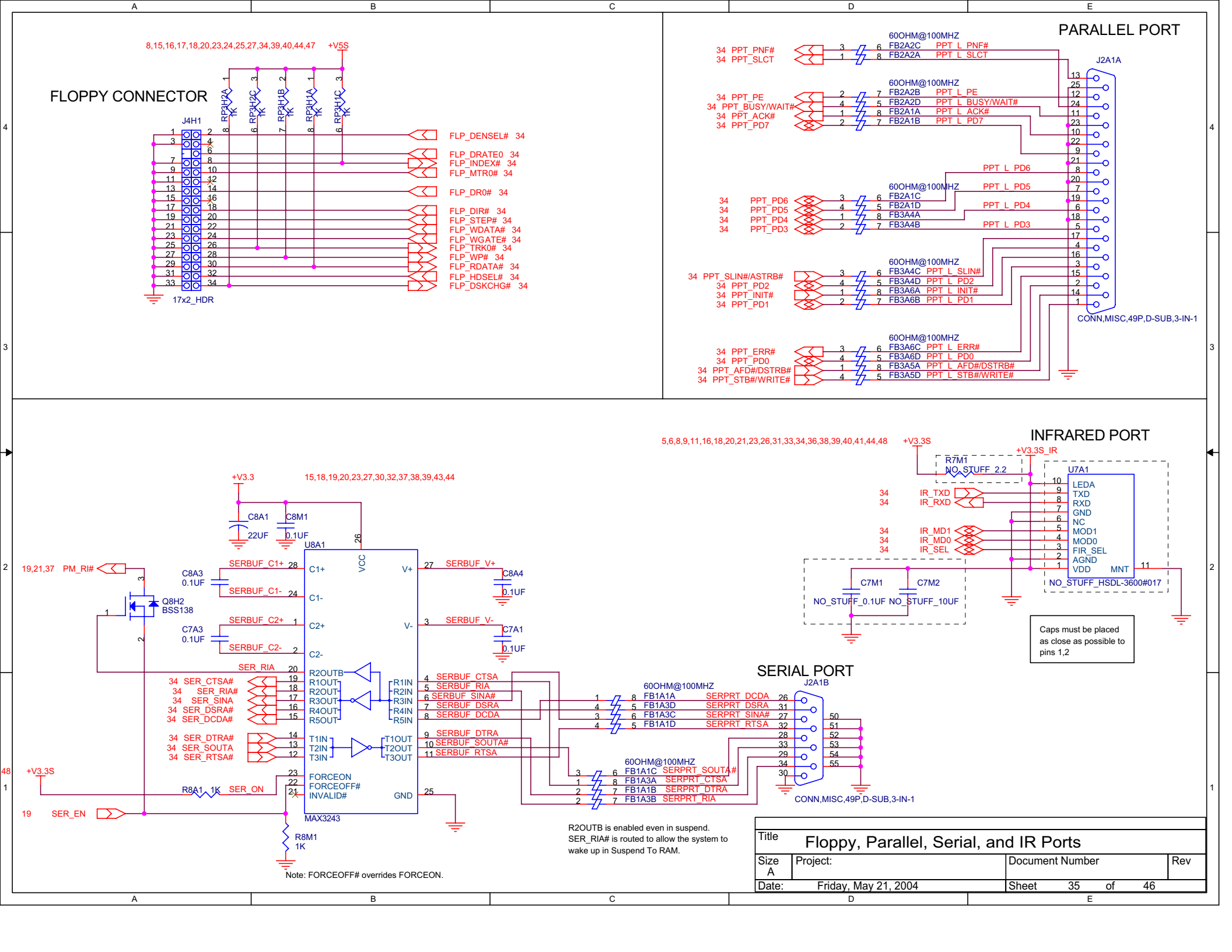
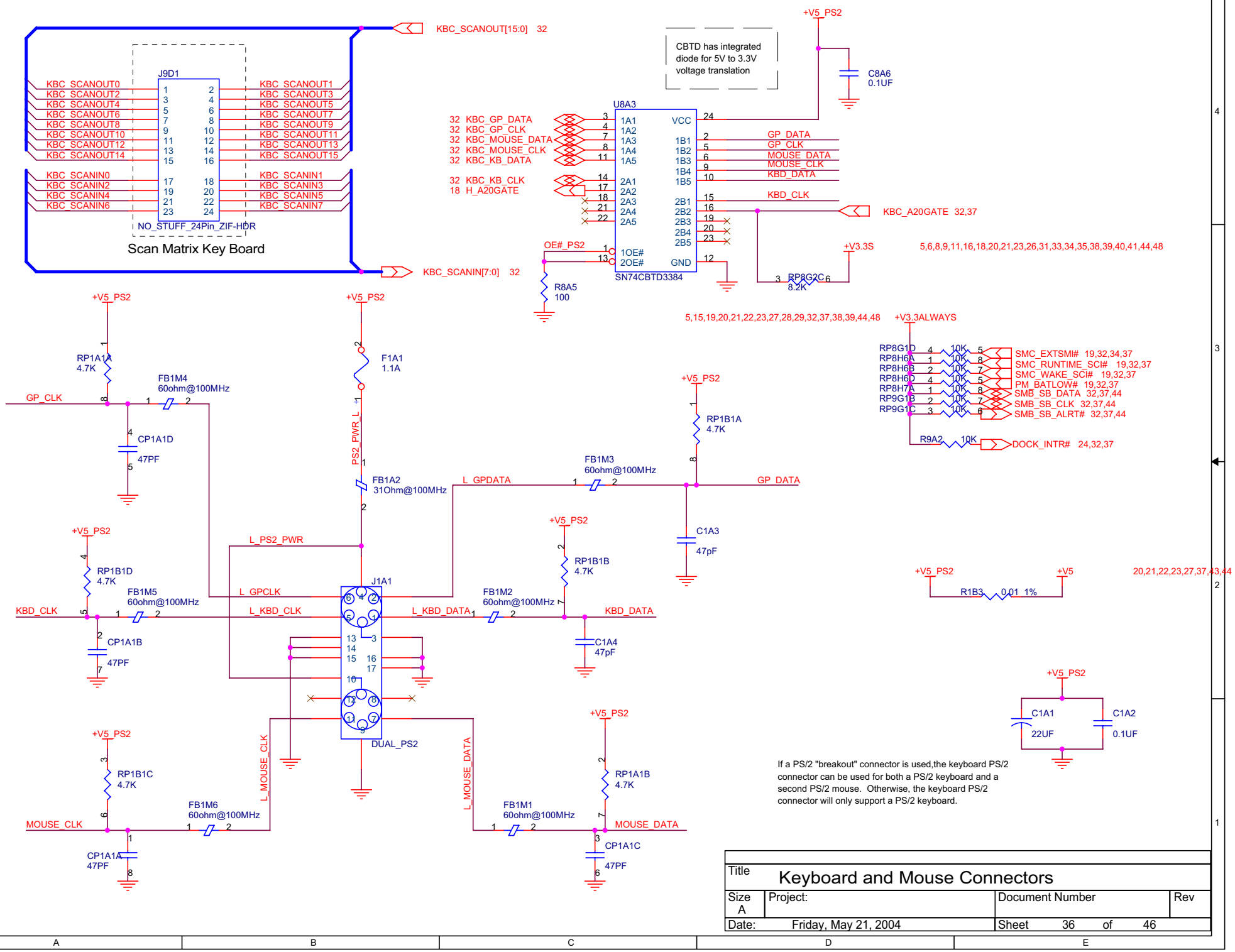
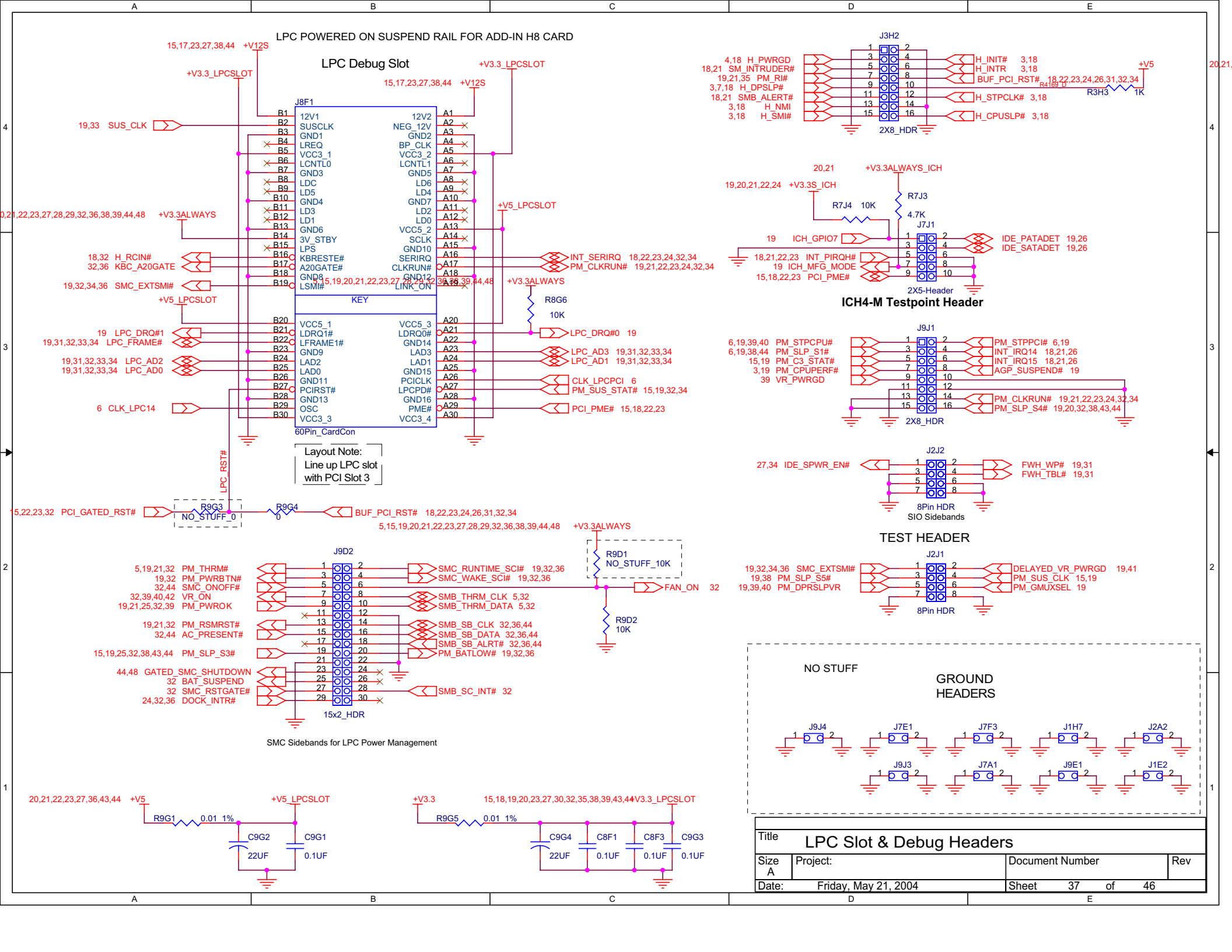
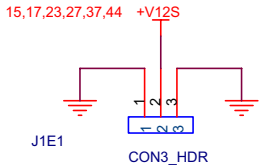

FLOPPY CONNECTOR
8,15,16,17,18,20,23,24,25,27,34,39,40,44,47
+V5S
RP3H2A 1K
RP3H2C 1K
RP3H1B 1K
RP3H1A 1K
RP3H1C 1K
J4H1
17x2_HDR
FLP_DENSEL# 34
FLP_DRATE0 34
FLP_INDEX# 34
FLP_MTR0# 34
FLP_DR0# 34
FLP_DIR# 34
FLP_STEP# 34
FLP_WDATA# 34
FLP_WGATE# 34
FLP_TRK0# 34
FLP_WP# 34
FLP_RDATA# 34
FLP_HDSEL# 34
FLP_DSKCHG# 34
PARALLEL PORT
60OHM@100MHZ
34 PPT_PNF#
34 PPT_SLCT
FB2A2C PPT_L_PNF#
FB2A2A PPT_L_SLCT
34 PPT_PE
34 PPT_BUSY/WAIT#
34 PPT_ACK#
34 PPT_PD7
FB2A2B PPT_L_PE
FB2A2D PPT_L_BUSY/WAIT#
FB2A1A PPT_L_ACK#
FB2A1B PPT_L_PD7
J2A1A
PPT_L_PD6
PPT_L_PD5
PPT_L_PD4
PPT_L_PD3
34 PPT_PD6
34 PPT_PD5
34 PPT_PD4
34 PPT_PD3
FB2A1C
FB2A1D
FB3A4A
FB3A4B
34 PPT_SLIN#/ASTRB#
34 PPT_PD2
34 PPT_INIT#
34 PPT_PD1
FB3A4C PPT_L_SLIN#
FB3A4D PPT_L_PD2
FB3A6A PPT_L_INIT#
FB3A6B PPT_L_PD1
34 PPT_ERR#
34 PPT_PD0
34 PPT_AFD#/DSTRB#
34 PPT_STB#/WRITE#
FB3A6C PPT_L_ERR#
FB3A6D PPT_L_PD0
FB3A5A PPT_L_AFD#/DSTRB#
FB3A5D PPT_L_STB#/WRITE#
CONN,MISC,49P,D-SUB,3-IN-1
INFRARED PORT
5,6,8,9,11,16,18,20,21,23,26,31,33,34,36,38,39,40,41,44,48
+V3.3S
+V3.3S_IR
R7M1
NO_STUFF 2.2
U7A1
LEDA
TXD
RXD
GND
NC
MOD1
MOD0
FIR_SEL
AGND
VDD
MNT
34 IR_TXD
34 IR_RXD
34 IR_MD1
34 IR_MD0
34 IR_SEL
C7M1
C7M2
NO_STUFF_0.1UF
NO_STUFF_10UF
NO_STUFF_HSDL-3600#017
Caps must be placed as close as possible to pins 1,2
+V3.3
15,18,19,20,23,27,30,32,37,38,39,43,44
C8A1 22UF
C8M1 0.1UF
U8A1
MAX3243
VCC
19,21,37 PM_RI#
Q8H2 BSS138
C8A3 0.1UF
C7A3 0.1UF
C8A4 0.1UF
C7A1 0.1UF
SERBUF_C1+
SERBUF_C1-
SERBUF_C2+
SERBUF_C2-
SERBUF_V+
SERBUF_V-
C1+
C1-
C2+
C2-
V+
V-
SER_RIA
34 SER_CTSA#
34 SER_RIA#
34 SER_SINA
34 SER_DSRA#
34 SER_DCDA#
34 SER_DTRA#
34 SER_SOUTA
34 SER_RTSA#
R2OUTB
R1OUT
R2OUT
R3OUT
R4OUT
R5OUT
T1IN
T2IN
T3IN
R1IN
R2IN
R3IN
R4IN
R5IN
T1OUT
T2OUT
T3OUT
SERBUF_CTSA
SERBUF_RIA
SERBUF_SINA#
SERBUF_DSRA
SERBUF_DCDA
SERBUF_DTRA
SERBUF_SOUTA#
SERBUF_RTSA
FORCEON
FORCEOFF#
INVALID#
GND
+V3.3S
R8A1 1K SER_ON
19 SER_EN
R8M1 1K
Note: FORCEOFF# overrides FORCEON.
SERIAL PORT
J2A1B
60OHM@100MHZ
FB1A1A SERPRT_DCDA
FB1A3D SERPRT_DSRA
FB1A3C SERPRT_SINA#
FB1A1D SERPRT_RTSA
FB1A1C SERPRT_SOUTA#
FB1A3A SERPRT_CTSA
FB1A1B SERPRT_DTRA
FB1A3B SERPRT_RIA
CONN,MISC,49P,D-SUB,3-IN-1
R2OUTB is enabled even in suspend.
SER_RIA# is routed to allow the system to wake up in Suspend To RAM.
Title
Floppy, Parallel, Serial, and IR Ports
Size A
Project:
Document Number
Rev
Date: Friday, May 21, 2004
Sheet 35 of 46



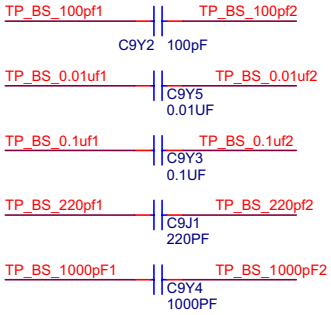

| | | | |
|---|---|---|---|
| Title | Keyboard and Mouse Connectors | | |
| Size A | Project: | Document Number | Rev |
| Date: Friday, May 21, 2004 | | Sheet 36 of 46 | |


LPC POWERED ON SUSPEND RAIL FOR ADD-IN H8 CARD
LPC Debug Slot
J8F1
60Pin_CardCon
KEY
Layout Note:
Line up LPC slot
with PCI Slot 3
J3H2
2X8_HDR
ICH4-M Testpoint Header
J7J1
2X5-Header
J9J1
2X8_HDR
J2J2
8Pin HDR
SIO Sidebands
TEST HEADER
J2J1
8Pin HDR
J9D2
15x2_HDR
SMC Sidebands for LPC Power Management
NO STUFF
GROUND
HEADERS
Title
LPC Slot & Debug Headers
Size
A
Project:
Document Number
Rev
Date:
Friday, May 21, 2004
Sheet
37
of
46

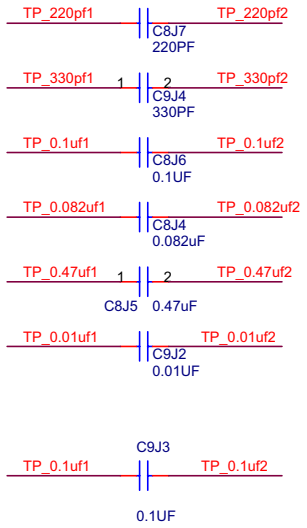
## Processor Fan Header



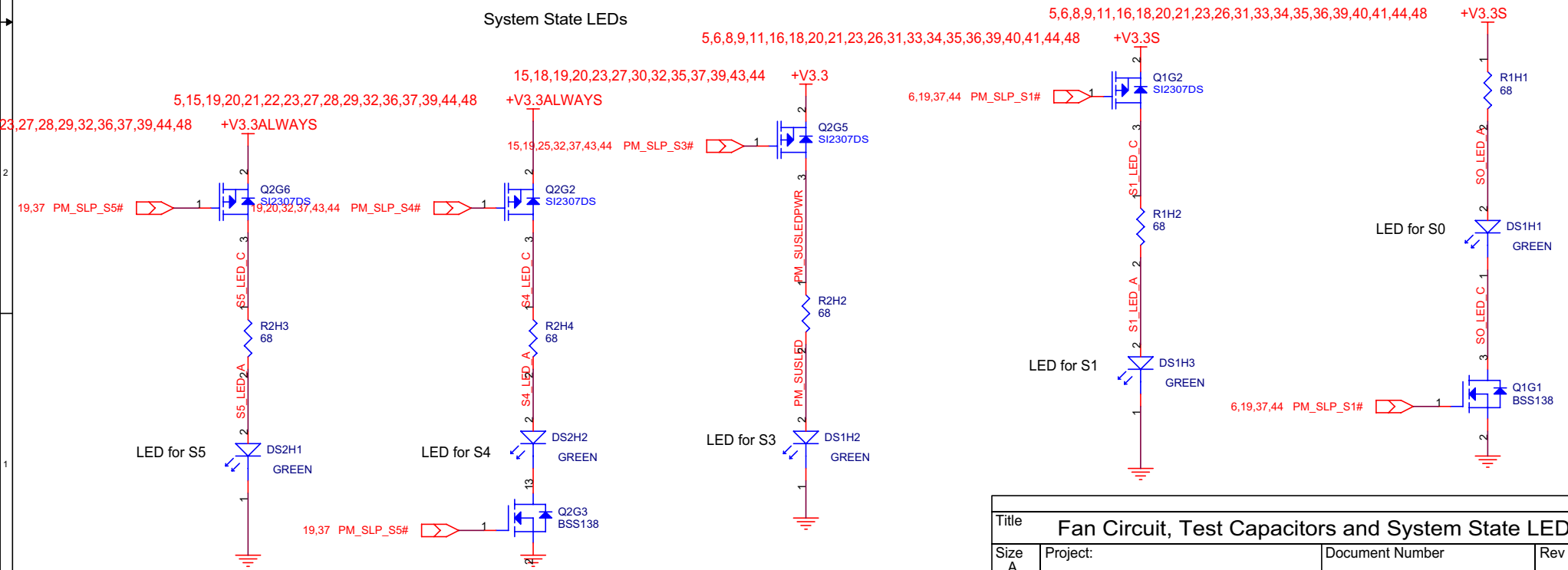

## Test Caps backside



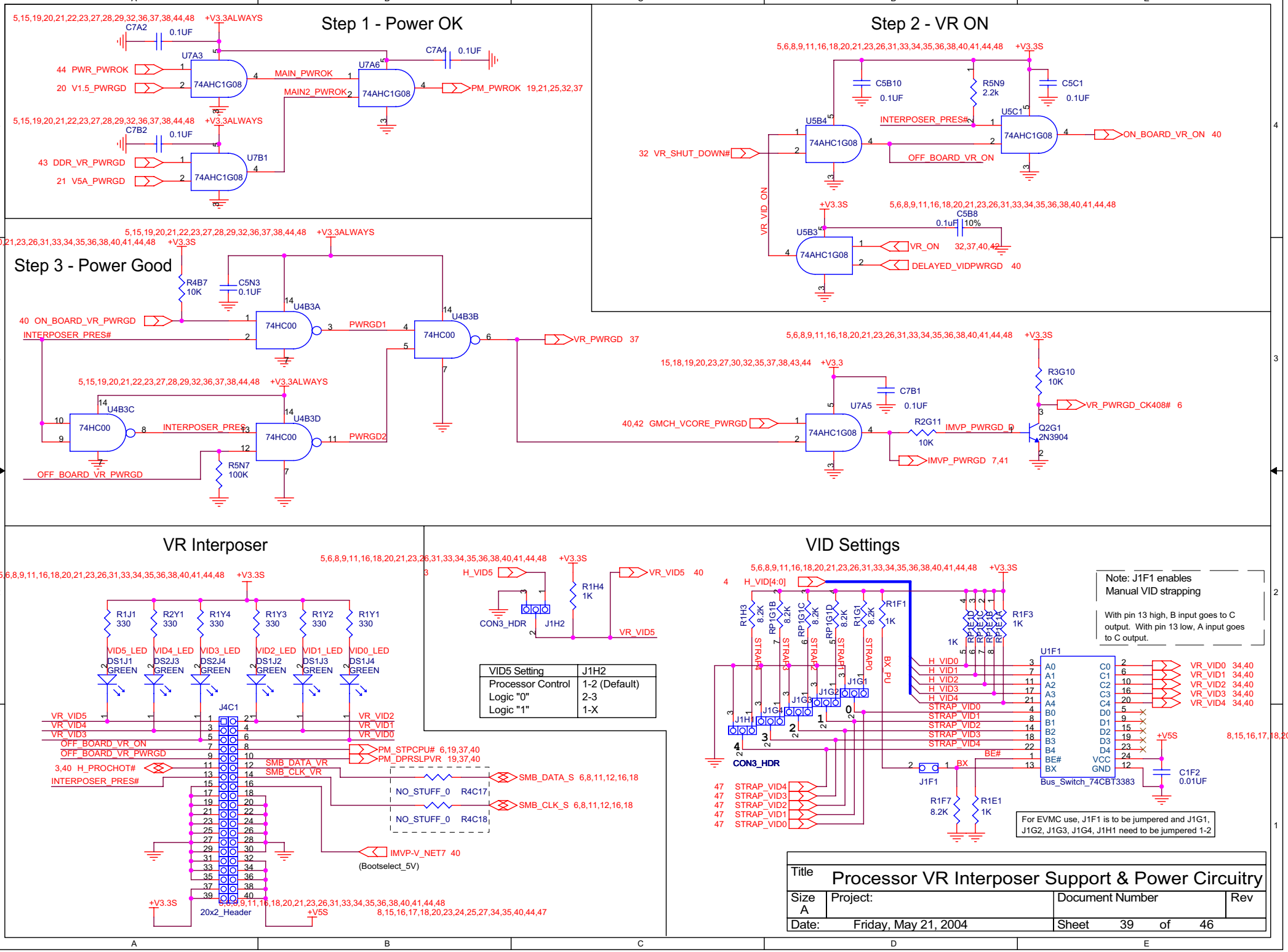

## Test Caps




## System State LEDs




| | | | |
|---|---|---|---|
| Title | Fan Circuit, Test Capacitors and System State LEDs | | |
| Size A | Project: | Document Number | Rev |
| Date: Friday, May 21, 2004 | | Sheet 38 of 46 | |


Step 1 - Power OK
5,15,19,20,21,22,23,27,28,29,32,36,37,38,44,48 +V3.3ALWAYS
C7A2 0.1UF
U7A3
44 PWR_PWROK
20 V1.5_PWRGD
74AHC1G08
MAIN_PWROK
MAIN2_PWROK
U7A6
C7A4 0.1UF
PM_PWROK 19,21,25,32,37
C7B2 0.1UF
U7B1
43 DDR_VR_PWRGD
21 V5A_PWRGD
Step 2 - VR ON
5,6,8,9,11,16,18,20,21,23,26,31,33,34,35,36,38,40,41,44,48 +V3.3S
C5B10 0.1UF
R5N9 2.2k
C5C1 0.1UF
U5B4
U5C1
INTERPOSER_PRES#
32 VR_SHUT_DOWN#
ON_BOARD_VR_ON 40
OFF_BOARD_VR_ON
VR_VID ON
C5B8 0.1uF 10%
U5B3
VR_ON 32,37,40,42
DELAYED_VIDPWRGD 40
Step 3 - Power Good
R4B7 10K
C5N3 0.1UF
U4B3A
U4B3B
74HC00
40 ON_BOARD_VR_PWRGD
PWRGD1
VR_PWRGD 37
U4B3C
U4B3D
PWRGD2
R5N7 100K
OFF_BOARD_VR_PWRGD
15,18,19,20,23,27,30,32,35,37,38,43,44 +V3.3
C7B1 0.1UF
U7A5
40,42 GMCH_VCORE_PWRGD
R2G11 10K
IMVP_PWRGD_D
Q2G1 2N3904
R3G10 10K
VR_PWRGD_CK408# 6
IMVP_PWRGD 7,41
VR Interposer
R1J1 330
R2Y1 330
R1Y4 330
R1Y3 330
R1Y2 330
R1Y1 330
VID5_LED DS1J1 GREEN
VID4_LED DS2J3 GREEN
VID3_LED DS2J4 GREEN
VID2_LED DS1J2 GREEN
VID1_LED DS1J3 GREEN
VID0_LED DS1J4 GREEN
J4C1
VR_VID5
VR_VID4
VR_VID3
OFF_BOARD_VR_ON
OFF_BOARD_VR_PWRGD
3,40 H_PROCHOT#
INTERPOSER_PRES#
VR_VID2
VR_VID1
VR_VID0
PM_STPCPU# 6,19,37,40
PM_DPRSLPVR 19,37,40
SMB_DATA_VR
SMB_CLK_VR
SMB_DATA_S 6,8,11,12,16,18
SMB_CLK_S 6,8,11,12,16,18
NO_STUFF_0 R4C17
NO_STUFF_0 R4C18
IMVP-V_NET7 40
(Bootselect_5V)
20x2_Header
H_VID5
CON3_HDR
J1H2
R1H4 1K
VR_VID5
VID5 Setting | J1H2
Processor Control | 1-2 (Default)
Logic "0" | 2-3
Logic "1" | 1-X
VID Settings
H_VID[4:0]
R1H3 8.2K
RP1G1B 8.2K
RP1G1C 8.2K
RP1G1D 8.2K
R1G1 8.2K
R1F1 1K
R1F3 1K
STRAP4
STRAP3
STRAP2
STRAP1
STRAP0
BX PU
H_VID0
H_VID1
H_VID2
H_VID3
H_VID4
STRAP_VID0
STRAP_VID1
STRAP_VID2
STRAP_VID3
STRAP_VID4
J1G1
J1G2
J1G3
J1G4
J1H1
CON3_HDR
BE#
BX
J1F1
U1F1
Bus_Switch_74CBT3383
VR_VID0 34,40
VR_VID1 34,40
VR_VID2 34,40
VR_VID3 34,40
VR_VID4 34,40
+V5S
C1F2 0.01UF
R1F7 8.2K
R1E1 1K
Note: J1F1 enables Manual VID strapping
With pin 13 high, B input goes to C output. With pin 13 low, A input goes to C output.
For EVMC use, J1F1 is to be jumpered and J1G1, J1G2, J1G3, J1G4, J1H1 need to be jumpered 1-2
Title Processor VR Interposer Support & Power Circuitry
Size A
Project:
Document Number
Rev
Date: Friday, May 21, 2004
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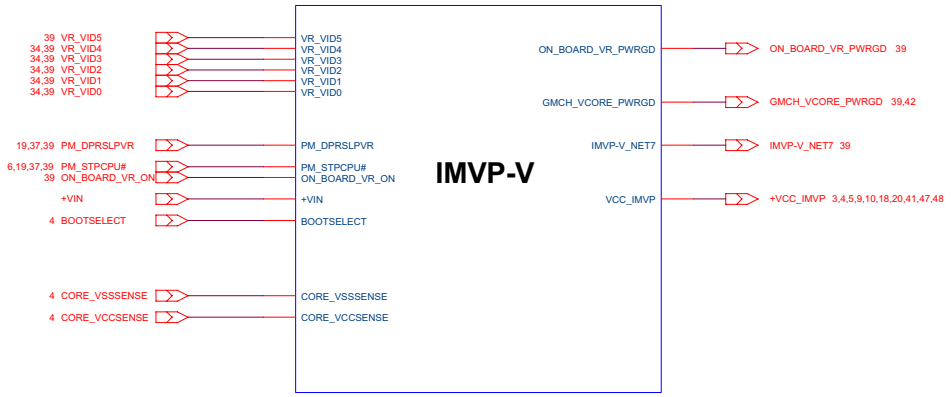
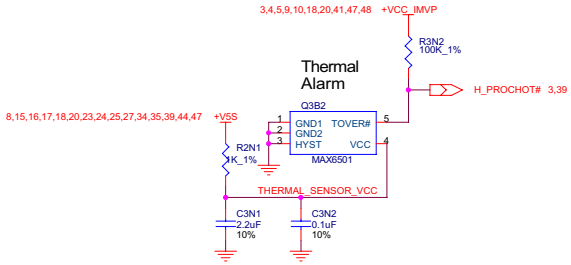



## Temperature Monitor

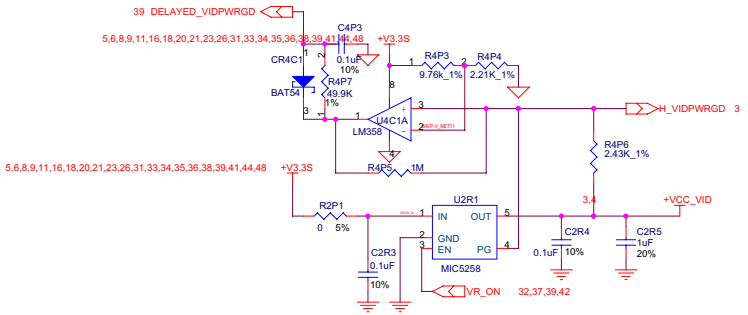



## Mobile Intel Pentium 4 Processor VID table

| Jumper Settings 0 = LOW, 1 = HIGH See page 39 for info. | | | | | | +VCC_IMVP |
|---|---|---|---|---|---|---|
| J1H2 | J1H1 | J1G4 | J1G3 | J1G2 | J1G1 | |
| 0 | 0 | 1 | 0 | 1 | 0 | 0.8375 V |
| 1 | 0 | 1 | 0 | 0 | 1 | 0.8500 V |
| 0 | 0 | 1 | 0 | 0 | 1 | 0.8625 V |
| 1 | 0 | 1 | 0 | 0 | 0 | 0.8750 V |
| 0 | 0 | 1 | 0 | 0 | 0 | 0.8875 V |
| 1 | 0 | 0 | 1 | 1 | 1 | 0.9000V |
| 0 | 0 | 0 | 1 | 1 | 1 | 0.9125 V |
| 1 | 0 | 0 | 1 | 1 | 0 | 0.9250 V |
| 0 | 0 | 0 | 1 | 1 | 0 | 0.9375 V |
| 1 | 0 | 0 | 1 | 0 | 1 | 0.9500 V |
| 0 | 0 | 0 | 1 | 0 | 1 | 0.9625 V |
| 1 | 0 | 0 | 1 | 0 | 0 | 0.9750V |
| 0 | 0 | 0 | 1 | 0 | 0 | 0.9875 V |
| 1 | 0 | 0 | 0 | 1 | 1 | 1.0000 V |
| 0 | 0 | 0 | 0 | 1 | 1 | 1.0125 V |
| 1 | 0 | 0 | 0 | 1 | 0 | 1.0250 V |
| 0 | 0 | 0 | 0 | 1 | 0 | 1.0375 V |
| 1 | 0 | 0 | 0 | 0 | 1 | 1.0500 V |
| 0 | 0 | 0 | 0 | 0 | 1 | 1.0625 V |
| 1 | 0 | 0 | 0 | 0 | 0 | 1.0750 V |
| 0 | 0 | 0 | 0 | 0 | 0 | 1.0875 V |
| 1 | 1 | 1 | 1 | 1 | 1 | OFF |
| 0 | 1 | 1 | 1 | 1 | 1 | OFF |
| 1 | 1 | 1 | 1 | 1 | 0 | 1.1000 V |
| 0 | 1 | 1 | 1 | 1 | 0 | 1.1125V |
| 1 | 1 | 1 | 1 | 0 | 1 | 1.1250V |
| 0 | 1 | 1 | 1 | 0 | 1 | 1.1375V |
| 1 | 1 | 1 | 1 | 0 | 0 | 1.1500V |
| 0 | 1 | 1 | 1 | 0 | 0 | 1.1625V |
| 1 | 1 | 1 | 0 | 1 | 1 | 1.1750V |
| 0 | 1 | 1 | 0 | 1 | 1 | 1.1875V |
| 1 | 1 | 1 | 0 | 1 | 0 | 1.2000V |

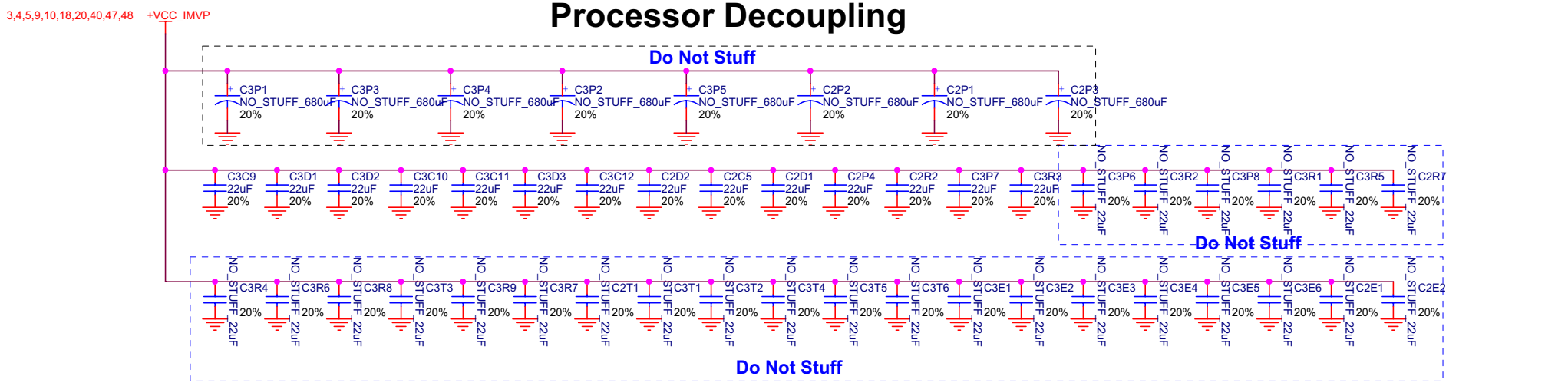
| Jumper Settings 0 = LOW, 1 = HIGH See page 39 for info. | | | | | | +VCC_IMVP |
|---|---|---|---|---|---|---|
| J1H2 | J1H1 | J1G4 | J1G3 | J1G2 | J1G1 | |
| 0 | 1 | 1 | 0 | 1 | 0 | 1.2125 V |
| 1 | 1 | 1 | 0 | 0 | 1 | 1.2250 V |
| 0 | 1 | 1 | 0 | 0 | 1 | 1.2375 V |
| 1 | 1 | 1 | 0 | 0 | 0 | 1.2500 V |
| 0 | 1 | 1 | 0 | 0 | 0 | 1.2625 V |
| 1 | 1 | 0 | 1 | 1 | 1 | 1.2750 V |
| 0 | 1 | 0 | 1 | 1 | 1 | 1.2875 V |
| 1 | 1 | 0 | 1 | 1 | 0 | 1.3000 V |
| 0 | 1 | 0 | 1 | 1 | 0 | 1.3125 V |
| 1 | 1 | 0 | 1 | 0 | 1 | 1.3250 V |
| 0 | 1 | 0 | 1 | 0 | 1 | 1.3375 V |
| 1 | 1 | 0 | 1 | 0 | 0 | 1.3500 V |
| 0 | 1 | 0 | 1 | 0 | 0 | 1.3625 V |
| 1 | 1 | 0 | 0 | 1 | 1 | 1.3750 V |
| 0 | 1 | 0 | 0 | 1 | 1 | 1.3875 V |
| 1 | 1 | 0 | 0 | 1 | 0 | 1.4000 V |
| 0 | 1 | 0 | 0 | 1 | 0 | 1.4125 V |
| 1 | 1 | 0 | 0 | 0 | 1 | 1.4250 V |
| 0 | 1 | 0 | 0 | 0 | 1 | 1.4375 V |
| 1 | 1 | 0 | 0 | 0 | 0 | 1.4500 V |
| 0 | 1 | 0 | 0 | 0 | 0 | 1.4625 V |
| 1 | 0 | 1 | 1 | 1 | 1 | 1.4750 V |
| 0 | 0 | 1 | 1 | 1 | 1 | 1.4875 V |
| 1 | 0 | 1 | 1 | 1 | 0 | 1.5000 V |
| 0 | 0 | 1 | 1 | 1 | 0 | 1.5125 V |
| 1 | 0 | 1 | 1 | 0 | 1 | 1.5250 V |
| 0 | 0 | 1 | 1 | 0 | 1 | 1.5375 V |
| 1 | 0 | 1 | 1 | 0 | 0 | 1.5500 V |
| 0 | 0 | 1 | 1 | 0 | 0 | 1.5625 V |
| 1 | 0 | 1 | 0 | 1 | 1 | 1.5750 V |
| 0 | 0 | 1 | 0 | 1 | 1 | 1.5875 V |
| 1 | 0 | 1 | 0 | 1 | 0 | 1.6000 V |

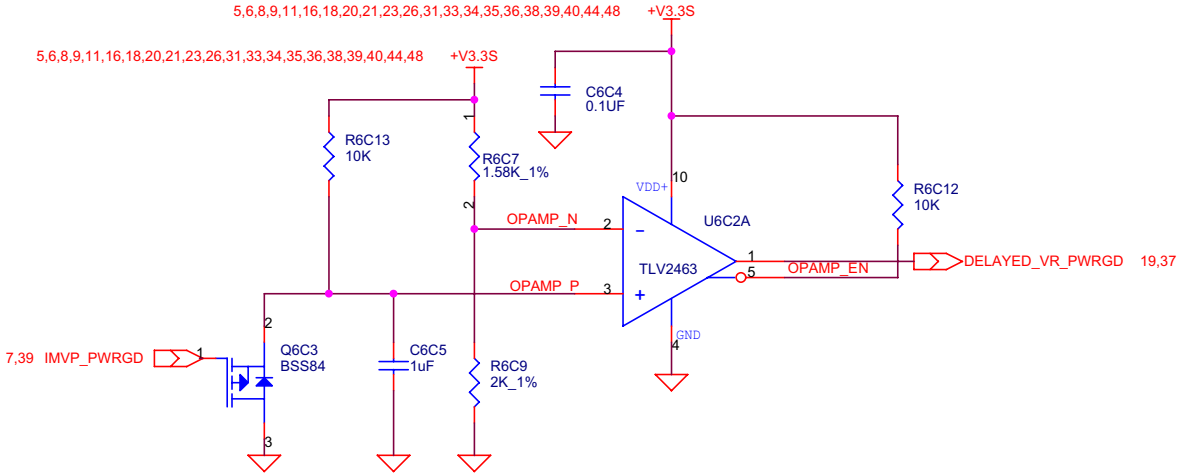
## DELAY POWERGOOD CIRCUIT



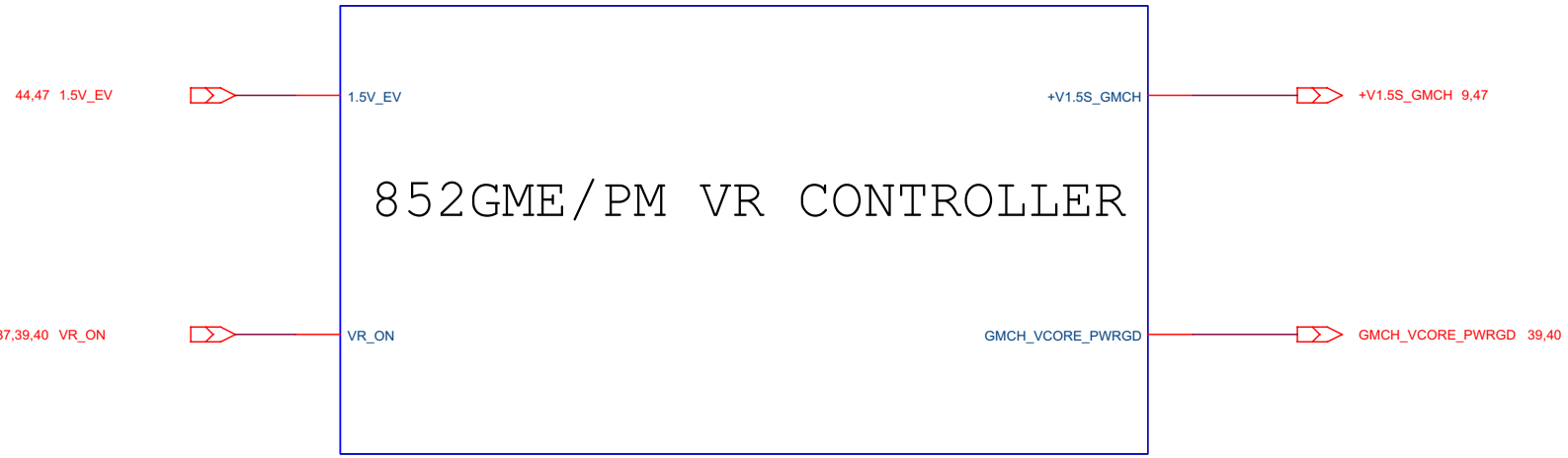

| | | | |
|---|---|---|---|
| Title | Processor Core VR (IMVP-V) | | |
| Size A | Project: | Document Number | Rev |
| Date: | Friday, May 21, 2004 | Sheet 40 of 46 | |

# Processor Decoupling

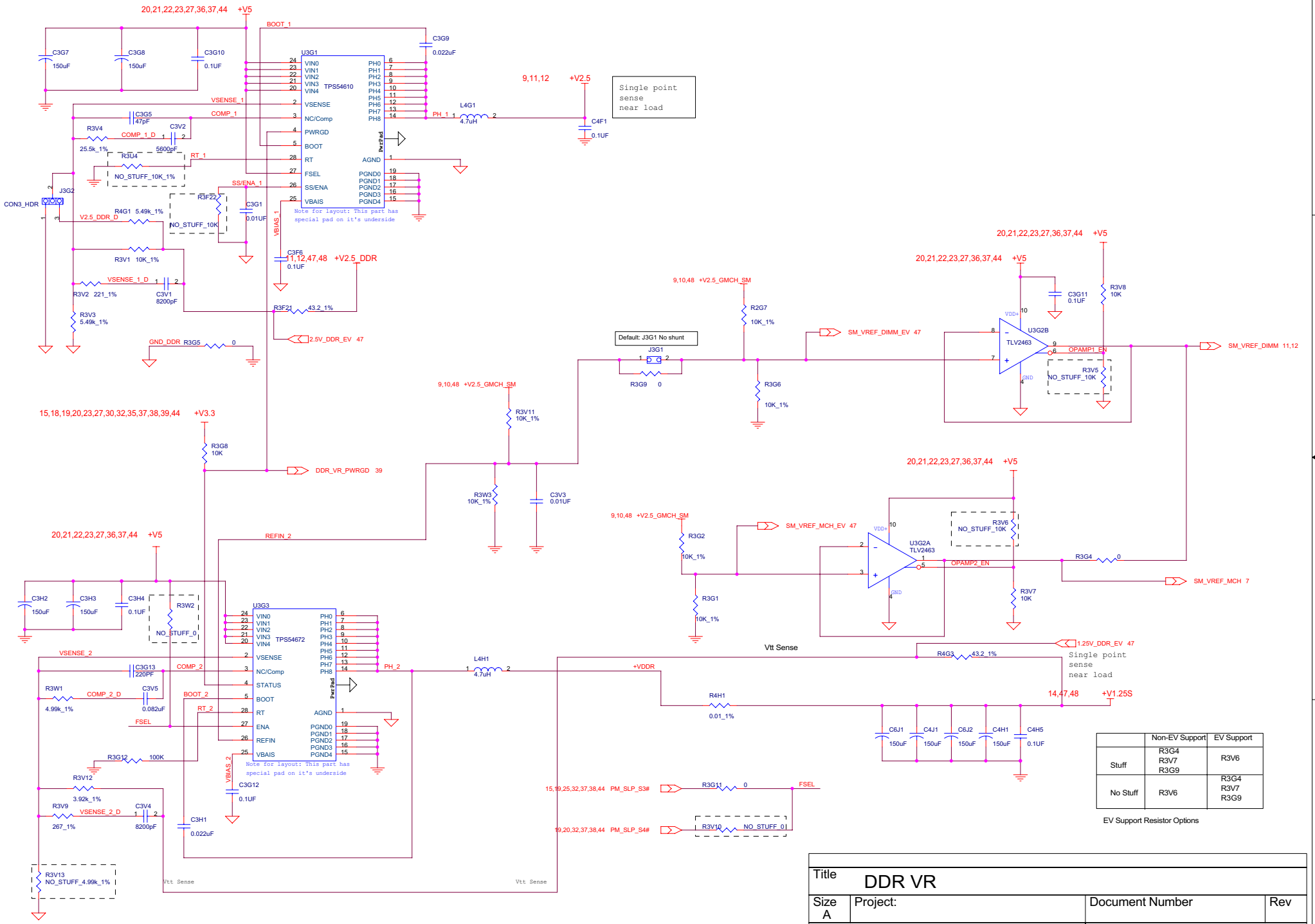



| | | | |
|---|---|---|---|
| Title: Processor Decoupling | | | |
| Size: A | Project: | Document Number | Rev |
| Date: Friday, May 21, 2004 | | Sheet 41 of 46 | |




| | | | |
|---|---|---|---|
| Title | GMCH VR and VCCP | | |
| Size A | Project: | Document Number | Rev |
| Date: Friday, May 21, 2004 | | Sheet 42 of 46 | |



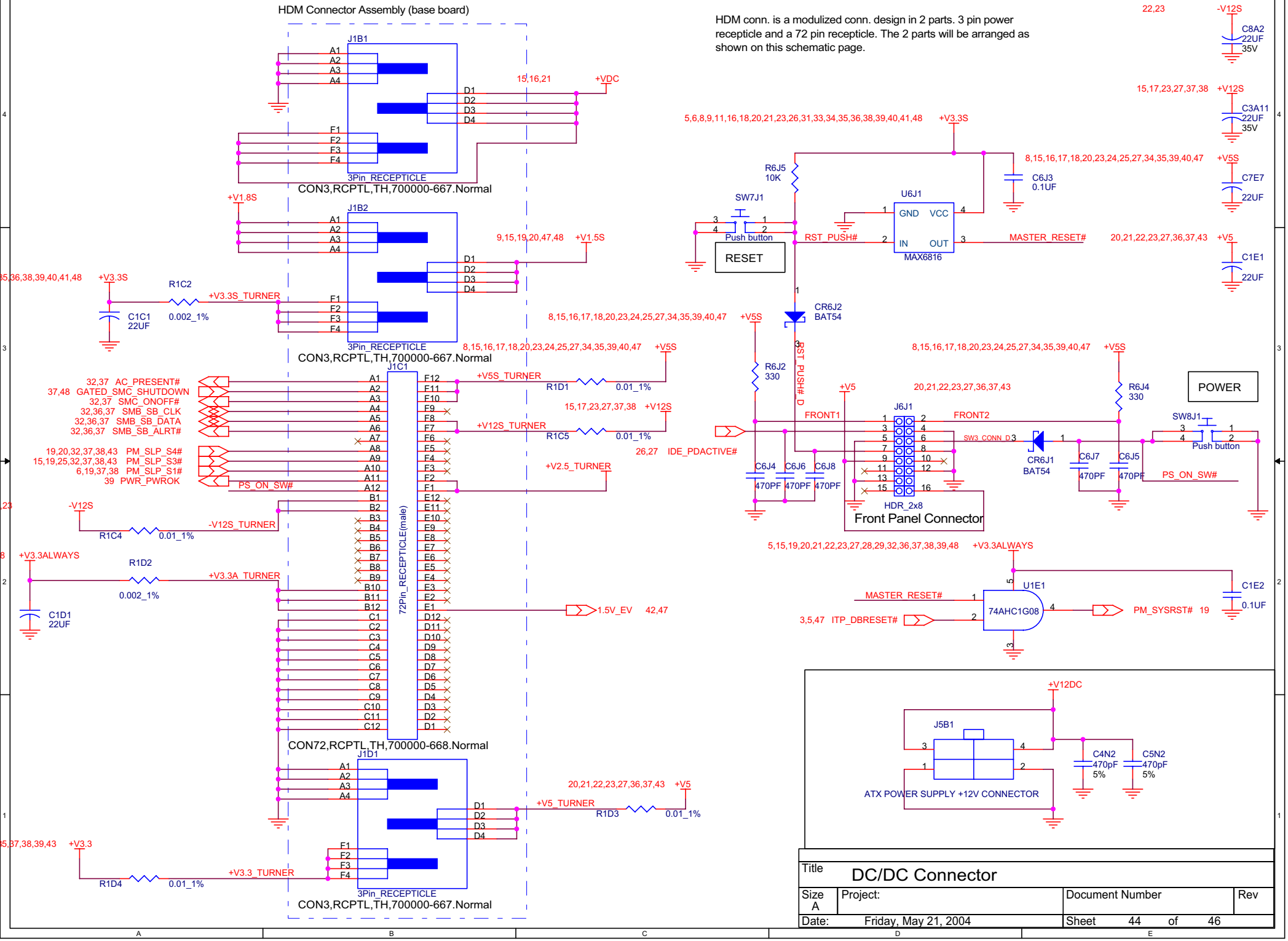

| | Non-EV Support | EV Support |
|---|---|---|
| Stuff | R3G4<br>R3V7<br>R3G9 | R3V6 |
| No Stuff | R3V6 | R3G4<br>R3V7<br>R3G9 |

EV Support Resistor Options

| | | | |
|---|---|---|---|
| Title | DDR VR | | |
| Size A | Project: | Document Number | Rev |
| Date: Friday, May 21, 2004 | | Sheet 43 of 46 | |

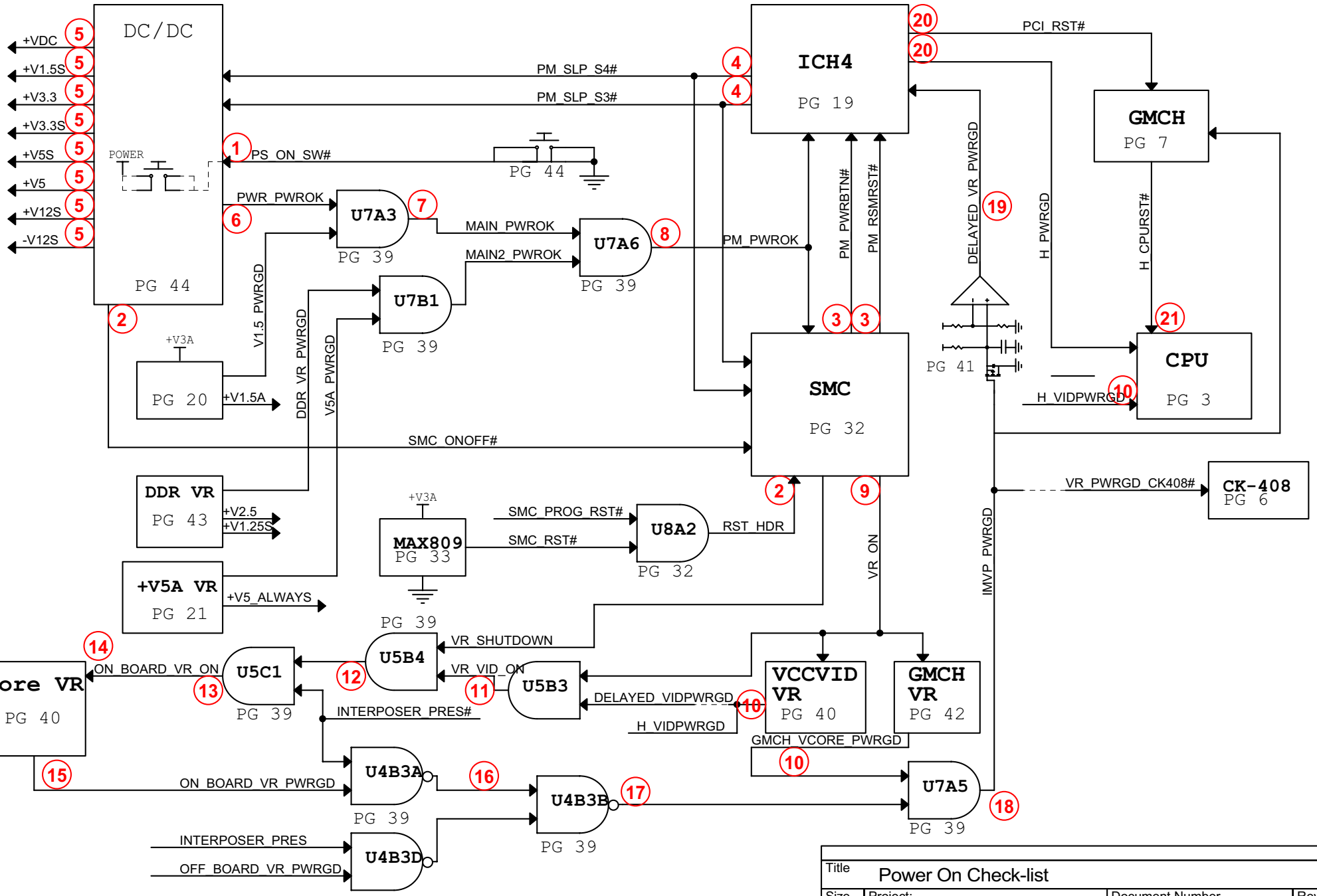
HDM Connector Assembly (base board)

HDM conn. is a modulized conn. design in 2 parts. 3 pin power recepticle and a 72 pin recepticle. The 2 parts will be arranged as shown on this schematic page.



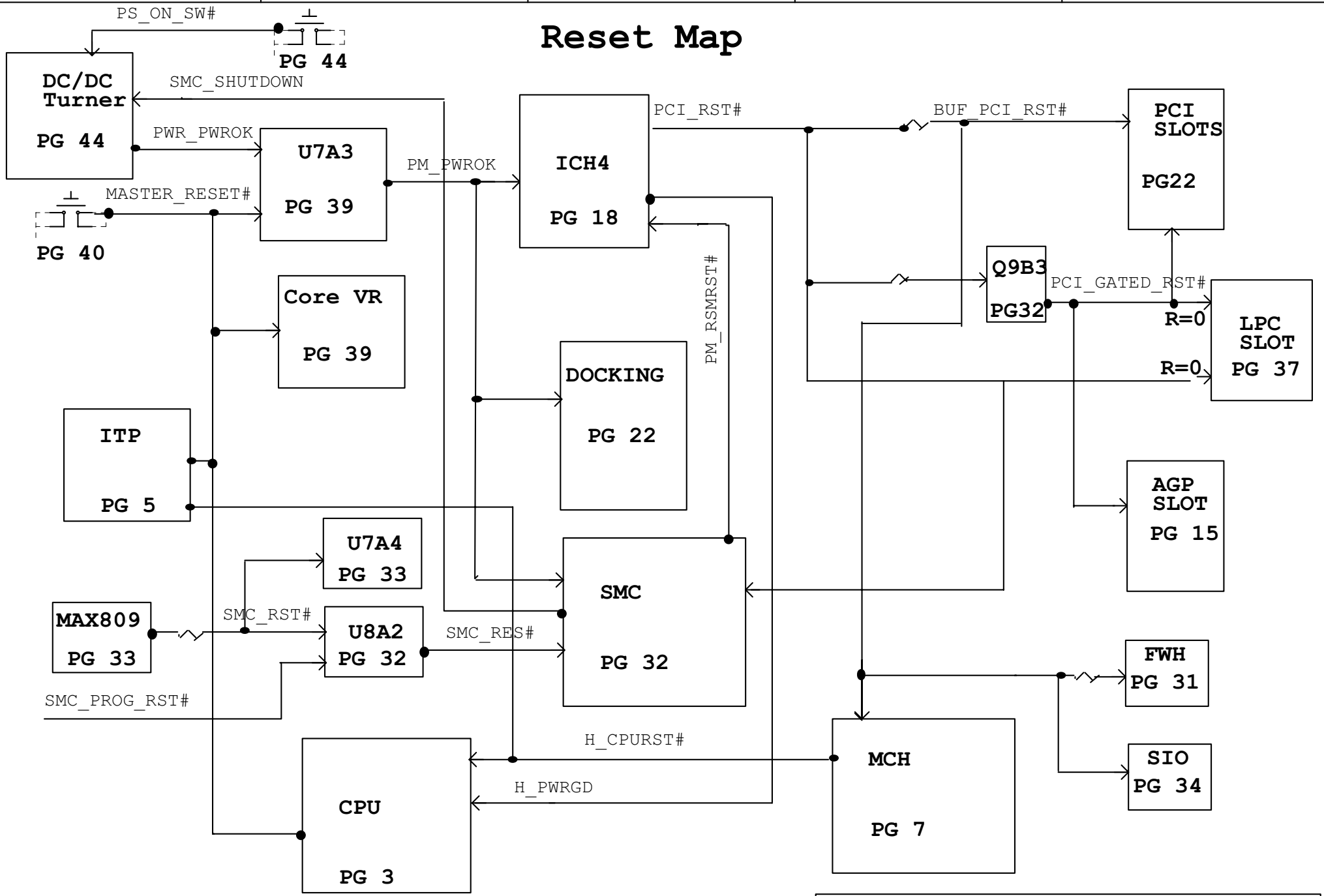

| | | | |
|---|---|---|---|
| Title | DC/DC Connector | | |
| Size A | Project: | Document Number | Rev |
| Date: Friday, May 21, 2004 | | Sheet 44 of 46 | |

# Power On Sequence




| | | | |
|---|---|---|---|
| Title | Power On Check-list | | |
| Size A | Project: | Document Number | Rev |
| Date: Friday, May 21, 2004 | | Sheet 45 of 46 | |

# Reset Map




| | | | |
|---|---|---|---|
| Title: Reset Map | | | |
| Size: A | Project: | Document Number | Rev |
| Date: Friday, May 21, 2004 | | Sheet 46 of 46 | |