



Intel® 852GM Chipset and Intel® 82801DB I/O Controller Hub (ICH4) Embedded Platform

Intel® Celeron® Processor on 0.13 Micron Process in 478-Pin Package, Mobile Intel® Celeron® Processor on 0.13 Micron Process and in Micro-FCPGA Package, and Intel® Celeron® M Processor

Platform Design Guide

December 2005



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Revision History

Date	Revision	Description
December 2005	1.0	Initial public release.

Introduction

1

This design guide provides Intel's design recommendations for the Intel® 852GM chipset-based systems. These design guidelines have been developed to ensure maximum flexibility for board designers while reducing the risk of board-related issues.

The following processors can be combined with the 852GM GMCH chipset:

- Mobile Intel® Celeron® processor
- Intel® Celeron® processor
- Intel® Celeron® M processor

In addition to providing PCB design recommendations such as layout and routing guidelines, this document also addresses other design concerns such as power delivery. The reference schematic checklist included in this document may be used as reference for board designers. While the reference schematic checklist covers specific designs, the core schematics will remain the same for most 852GM chipset family platforms.

1.1 Conventions and Terminology

Table 1. Conventions and Terminology (Sheet 1 of 2)

Terminology	Definition
AC	Audio Codec
ADD	AGP Digital Display
AMC	Audio/Modem Codec
Anti-etch	Any plane-split, void or cutout in a V_{CC} or GND plane is referred to as an anti-etch.
ASF	Alert Standards Format
BER	Bit Error Rate
CMC	Common Mode Choke
CRT	Cathode Ray Tube
DAC	Digital-to-Analog Converter
DVO	Digital Video Out
EMI	Electro Magnetic Interference
ESD	Electrostatic Discharge
FS	Full Speed – Refers to USB 1.1 Full Speed
FSB	Processor to GMCH interface
FWH	Firmware Hub – A non-volatile memory device used to store the system BIOS.
GMCH	Graphics Memory Controller Hub
HS	High Speed – Refers to USB 2.0 High Speed
ICH4	Intel® 82801DB I/O Controller Hub 4 (ICH4): Fourth generation I/O controller hub

Table 1. Conventions and Terminology (Sheet 2 of 2)

Terminology	Definition
LCI	LAN Connect Interface
LOM	LAN on PCB
LPC	Low Pin Count
LS	Low Speed – Refers to USB 1.0 Low Speed.
LVDS	Low Voltage Digital Signaling
MC	Modem Codec
micro FC-BGA	Micro Flip Chip Ball Grid Array
micro FC-PGA	Micro Flip Chip Pin Grid Array
PCB	Printed Circuit Board
PCM	Pulse Code Modulation
PLC	Platform LAN Connect
RTC	Real Time Clock
SMBus	System Management Bus – A two-wire interface through which various system components may communicate.
SPD	Serial Presence Detect
STD	Suspend-To-Disk
STR	Suspend-To-Ram
TCO	Total Cost of Ownership
TDM	Time Division Multiplexed
TDR	Time Domain Reflectometry
TFT	Thin-film Transistor
USB	Universal Serial Bus
VRM	Voltage Regulator Module

1.2 Reference Documents

Table 2 presents reference documents.

Table 2. Reference Documents (Sheet 1 of 2)

Document Title	Document Number or Source
<i>Mobile Intel® Celeron® Processor on 0.13 Micron Process and in Micro-FCPGA Package Datasheet</i>	http://developer.intel.com/design/mobile/datashts/251308.htm
<i>Intel® Celeron® Processor on 0.13 Micron Process in the 478-Pin Package Datasheet</i>	http://developer.intel.com/design/celeron/datashts/251748.htm
<i>Intel® 852GM /852GMV Chipset Graphics and Memory Controller Hub (GMCH) Datasheet</i>	http://developer.intel.com/design/mobile/datashts/252407.htm
<i>Intel® 852GM/852GMV Chipset Graphics and Memory Controller Hub (GMCH) Specification Update</i>	Contact your Intel Representative
<i>Intel Celeron M Processor Datasheet</i>	http://www.intel.com/design/mobile/datashts/300302.htm
<i>Intel Celeron M Processor Specification Update</i>	http://developer.intel.com/design/mobile/specupdt/300303.htm
<i>Ultra Low Voltage Intel Celeron M Processor at 600 MHz Addendum to the Intel Celeron M Processor Datasheet</i>	http://www.intel.com/design/intarch/datashts/301753.htm
<i>ULV Intel Celeron M Processor at 600 MHz for Embedded Applications Thermal Design Guide</i>	http://developer.intel.com/design/intarch/designgd/302288.htm
<i>Intel Celeron M Processor on 90 nm Process Datasheet</i>	http://developer.intel.com/design/mobile/datashts/303110.htm
<i>Intel Celeron M Processor on 90 nm Process for Embedded Applications Thermal Design Guide</i>	http://developer.intel.com/design/intarch/designgd/305994.htm
<i>Intel CK-408 Clock Synthesizer/Driver Specification, Rev 1.0 or later</i>	Contact your Intel Representative
<i>Intel Specification Addendum Rev 1.0 for the JEDEC DDR200 Specification</i>	http://www.intel.com/technology/memory/ddr/specs/ddr200_spec_10.htm
<i>AP-728 Intel ICH Family Real Time Clock (RTC) Accuracy and Considerations under Test Conditions.</i>	http://www.intel.com/design/chipsets/aplnots/292276.htm
<i>Intel® 82801 I/O Controller Hub (ICH4) Datasheet</i>	http://developer.intel.com/design/chipsets/datashts/290744.htm
<i>Intel® 82801 I/O Controller Hub (ICH4) Datasheet Specification Update</i>	http://developer.intel.com/design/chipsets/specupdt/290745.htm
<i>Intel® 82801 I/O Controller Hub (ICH4): Thermal and Mechanical Design Guidelines</i>	http://www.intel.com/design/chipsets/designex/298651.htm
<i>Voltage Regulator Module (VRM) and Enterprise Voltage Regulator-down (EVRC) 10.0</i>	Contact your Intel Representative
<i>ITP700 Debug Port Design Guide</i>	http://www.intel.com/design/xeon/guides/249679.htm
<i>JEDEC Standard, JESD79, Double Data Rate (DDR) SDRAM Specification</i>	http://www.jedec.org/
<i>Intel® Celeron® Processor in the 478-pin package Thermal Design Guide for Embedded Applications</i>	http://developer.intel.com/design/intarch/designgd/273704.htm
<i>FWH BIOS Spec</i>	Contact your Intel Representative

Table 2. Reference Documents (Sheet 2 of 2)

Document Title	Document Number or Source
<i>AC'97 Specification Revision 2.3</i>	http://www.intel.com/design/chipsets/audio/ac97_r23.pdf
<i>Advanced Configuration and Power Interface Specification (ACPI), Revision 3.0</i>	http://www.acpi.info/spec.htm
<i>SMBUS specification, Revision 2.0</i>	http://www.smbus.org/specs
<i>Communication and Networking Riser (CNR) Specification, Revision 1.2</i>	Contact your Intel Representative
<i>Intel ICH Family USB ESD Considerations</i>	Contact your Intel Representative
<i>Intel CK-SSC Spread Spectrum Clock Specification</i>	Contact your Intel Representative

System Overview

2

The Intel® 852GM chipset is a Graphics Memory Controller Hub (GMCH) component for embedded platforms. It provides the processor interface, system memory interface (DDR SDRAM), hub interface, CRT interface, LVDS interface, and a DVO interface. The Intel 852GM GMCH and Intel® 82801DB I/O Controller Hub 4 (ICH4) is optimized for the Intel® Celeron® Processor, Mobile Intel® Celeron® Processor, or the Intel Celeron® M Processor.

The accelerated hub architecture interface (the chipset component interconnect) is designed into the chipset to provide an efficient, high-bandwidth communication channel between the GMCH and the ICH4.

An ACPI-compliant Intel 852GM chipset embedded platform may support the Full-On (S0), Power On Suspend (S1-M), Suspend to RAM (S3), Suspend to Disk (S4), and Soft-Off (S5) power management states. Through the use of an appropriate LAN device, the chipset also supports wake on LAN for remote administration and troubleshooting. The chipset architecture removes the requirement for the ISA expansion bus that was traditionally integrated into the I/O subsystem of PCIs/AGPs. This removes many of the conflicts experienced when installing hardware and drivers into legacy ISA systems. The elimination of ISA provides true plug-and-play for the platform. Traditionally, the ISA interface was used for audio and modem devices. The addition of AC'97 allows the OEM to use software-configurable AC'97 audio and modem coder/decoders (codecs) instead of the traditional ISA devices.

2.1 Terminology

For this document, the following terminology applies.

- *Celeron M processor* refers to both the Intel Celeron M processor and the Ultra Low Voltage Intel Celeron M processor.
- *82852GM* refers to the Intel® 82852GM GMCH.
- *ICH4* refers to Intel 82801DB I/O Controller Hub 4.

2.2 Intel® 852GM Chipset Platform System Features

The Intel 852GM chipset contains two core components: the Intel 852GM GMCH and the Intel ICH4. The GMCH integrates the following:

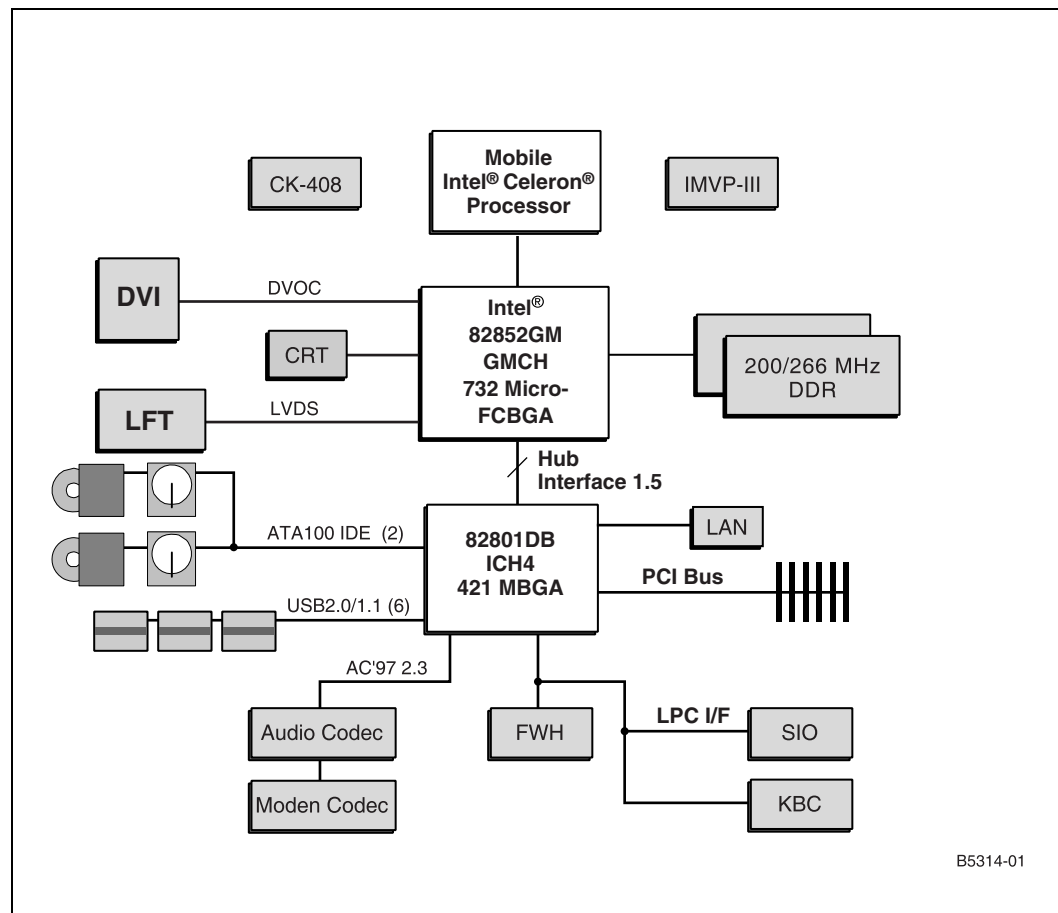
- 400-MHz processor Front Side Bus (FSB) controller
- Graphics controller interface
- Dual Channel 18 bit LVDS interface for TFT panel support
- One Digital Video Out Port (DVO)
- Supports DDR200/266 MHz memory technology
- High-speed Accelerated Hub Architecture interface for communication with the ICH4

The ICH4 integrates the following:

- Ultra ATA 100/66/33 controller
- USB host controller that supports the USB 1.1 and USB 2.0 specification
- LPC interface
- FWH Flash BIOS interface controller
- PCI interface controller
- AC'97 digital controller with Enhanced 20-bit Audio support
- Hub Interface for communication with the GMCH

Figure 1 provides a basic system block diagram of the Intel 852GM chipset with the Mobile Intel Celeron Processor.

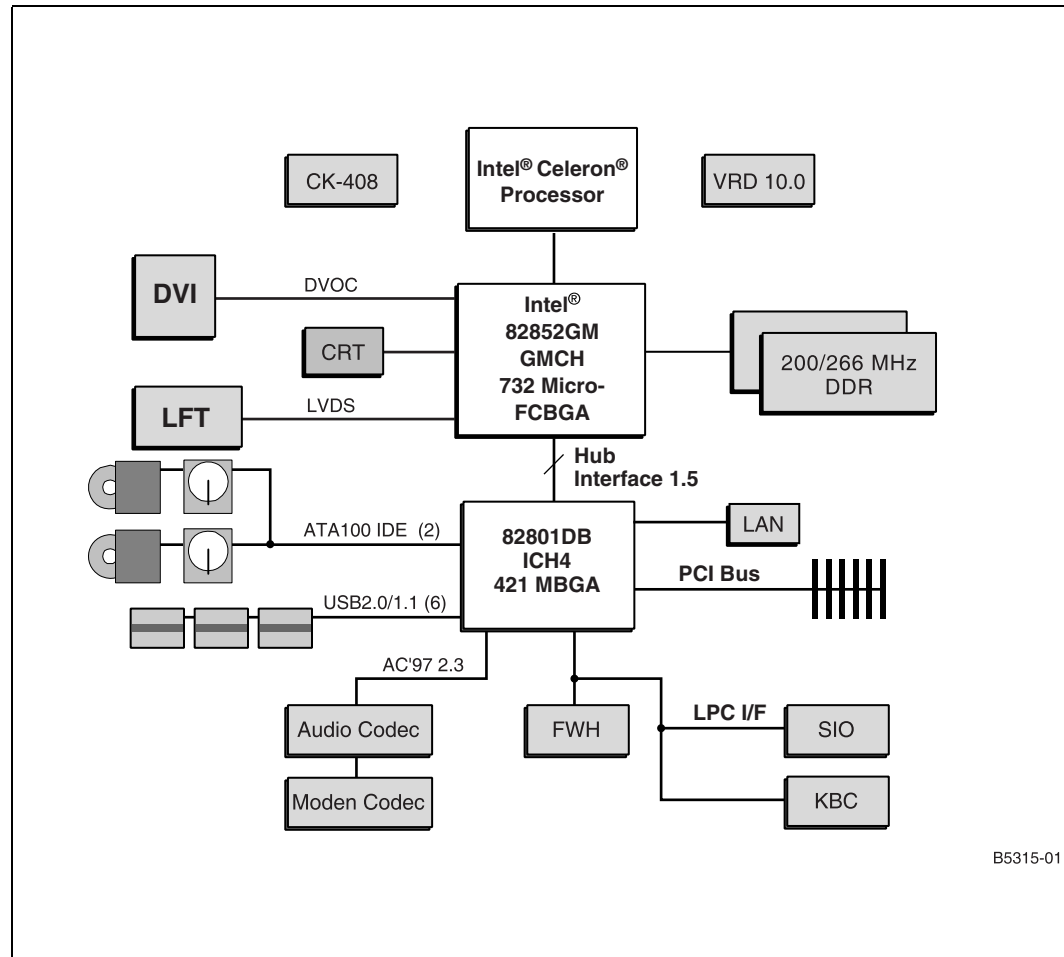
Figure 1. Embedded Intel® 852GM Chipset System Block Diagram with Mobile Intel® Celeron® Processor



Note: When using the Mobile Intel Celeron Processor, IMVP-III voltage regulation design guidelines are required.

Figure 2 provides a basic system block diagram of the Intel 852GM chipset with the Intel Celeron Processor.

Figure 2. Embedded Intel® 852GM Chipset System Block Diagram with Intel® Celeron® Processor

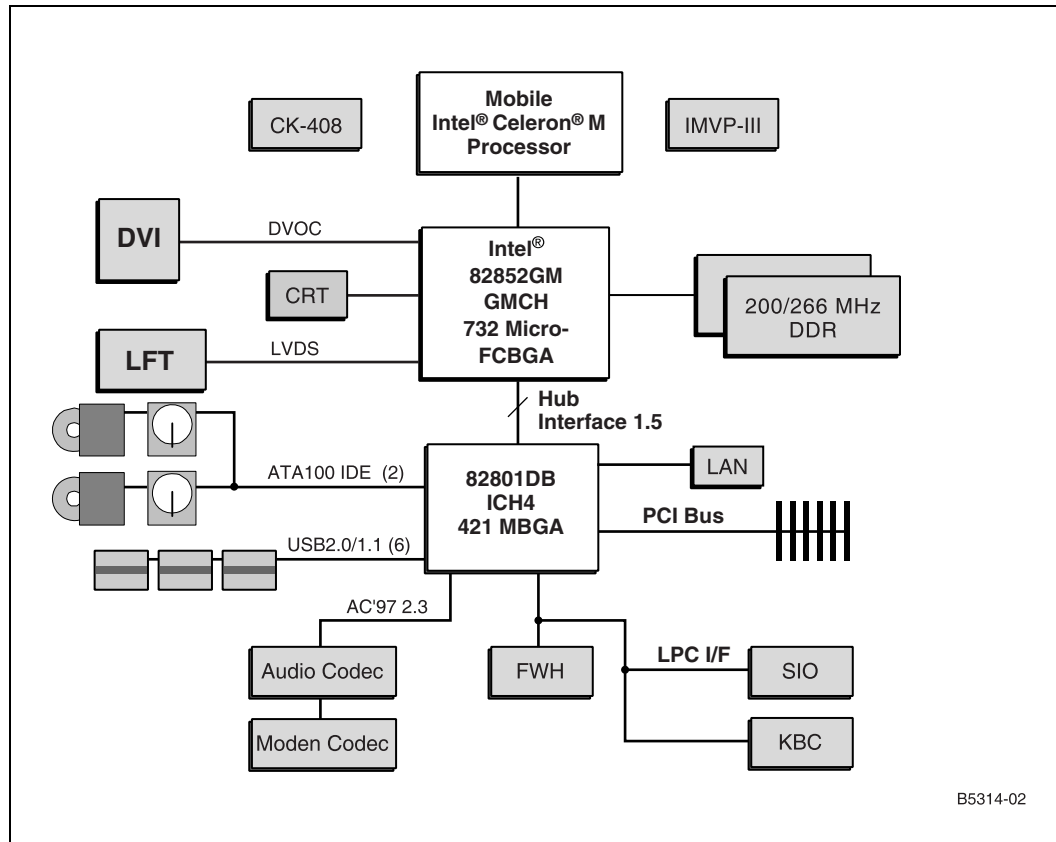


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Note: When using Intel Celeron Processor, VRD 10.0 voltage regulator design guidelines are required.

Figure 3 provides a basic system block diagram of the Intel 852GM chipset with the Intel Celeron M Processor.

Figure 3. Embedded Intel® 852GM Chipset System Block Diagram with Intel® Celeron® M Processor



Note: When using the Intel Celeron M Processor, IMVP-IV voltage regulation design guidelines are required.

2.3 Processor Interface

2.3.1 Mobile Intel® Celeron® Processor

For more details, see the *Mobile Intel Celeron Processor on 0.13 Micron Process and in Micro-FCPGA Package Datasheet*.

2.3.1.1 Architectural Features

- On-die 256-kByte second Level Cache
- Hyper pipelined technology

- 400-MHz Front Side Bus quad-pumped bus running off a 100-MHz system clock making 3.2 GB/sec data transfer rates possible.
- The execution trace cache is a first level cach that stores approximately 12-k decoded micro-operations, which removes the decoder from the main execution path.
- Supports Streaming SIMD Extensions 2 (SSE2)
- Assisted Gunning Transceiver Logic (AGTL+) bus driver technology
- Supports Intel architecture with dynamic execution
- No support for Enhanced Intel SpeedStep Technology, Deeper Sleep operation, or Intel Thermal Monitor 2.

2.3.1.2 Packaging/Power

- 478-pin, micro FCPGA
- 1.30 V (core)
- IMVP-III Voltage Regulator Design Guidelines

2.3.2 Intel Celeron Processor

For more details, see the *Intel Celeron Process on the 0.13 Micron Process in the 478-Pin Package Datasheet*.

2.3.2.1 Architectural Features

- On-die 128-Kbyte second Level Cache
- Hyper pipelined technology
- 400 MHz Front Side Bus quad-pumped bus running off a 100-MHz system clock making 3.2 GB/sec data transfer rates possible.
- The execution trace cache is a first level cach that stores approximately 12-k decoded micro-operations, which removes the decoder from the main execution path.
- Supports Streaming SIMD Extensions 2 (SSE2)
- Assisted Gunning Transceiver Logic (AGTL+) bus driver technology
- Supports Intel architecture with dynamic execution
- No support for Enhanced Intel SpeedStep® Technology, Deeper Sleep operation, or Intel® Thermal Monitor 2.

2.3.2.2 Packaging/Power

- 478-pin, FC-PGA2 package
- 1.475 - 1.525 V (core)
- VRD 10.0 Voltage Regulator Design Guidelines

2.3.3 Intel® Celeron® M Processor 320 on 130 nm process

For more details, see the *Intel Celeron M Processor Datasheet*.

2.3.3.1 Architectural Features

- On-die 512-Kbyte second Level Cache
- On-die primary 32-kB instruction cache and 32-kB write-back data cache
- Supports Streaming SIMD Extensions 2 (SSE2)
- Assisted Gunning Transceiver Logic (AGTL+) bus driver technology
- Hyper pipelined technology
- Supports Intel architecture with dynamic execution
- 400-MHz, source-synchronous front side bus (FSB)
- No support for Enhanced Intel SpeedStep Technology, Deeper Sleep operation, or Intel Thermal Monitor 2.

2.3.3.2 Packaging/Power

- 1.3 GHz operation, available in 478-pin micro FCPGA and 479-ball micro FCBGA packages.
- VCC-CORE for 1.3 GHz: 1.356 V
- TDP for 1.3 GHz = 24.5 W
- IMVP-IV Voltage Regulator Design Guidelines
- VCCA: 1.8 V

2.3.4 Intel® Celeron® M Processor 370 on 90 nm process

For more details, see the *Intel Celeron M Processor on 90 nm process Datasheet*.

2.3.4.1 Architectural Features

- On-die 1-MB second Level Cache
- On-die primary 32-kB instruction cache and 32-kB write-back data cache
- Supports Streaming SIMD Extensions 2 (SSE2)
- Assisted Gunning Transceiver Logic (AGTL+) bus driver technology
- Supports Intel architecture with dynamic execution
- 400-MHz, source-synchronous front side bus (FSB)
- No support for Enhanced Intel SpeedStep Technology, Deeper Sleep operation, or Intel Thermal Monitor 2.

2.3.4.2 Packaging/Power

- 1.5 GHz operation, available in 478-pin micro FCPGA and 479-ball micro FCBGA packages.

- VCCA: 1.8 V and 1.5 V supported only
- TDP = 21 W
- IMVP-IV Voltage Regulator Design Guidelines

2.3.5 Intel Celeron M Processor Ultra Low Voltage 373 on 90 nm process

For more details, see the *Intel Celeron M Processor Datasheet on 90 nm process Datasheet*.

2.3.5.1 Architectural Features

- On-die 512-KB second Level Cache
- On-die primary 32-kB instruction cache and 32-kB write-back data cache
- Supports Streaming SIMD Extensions 2 (SSE2)
- Assisted Gunning Transceiver Logic (AGTL+) bus driver technology
- Supports Intel architecture with dynamic execution
- 400-MHz, source-synchronous front side bus (FSB)
- No support for Enhanced Intel SpeedStep Technology, Deeper Sleep operation, or Intel Thermal Monitor 2.

2.3.5.2 Packaging/Power

- 1.0 GHz operation, available in 479-ball micro FCBGA packages.
- VCCA: 1.8 V and 1.5 V supported only
- TDP = 5.5W
- IMVP-IV Voltage Regulator Design Guidelines

2.3.6 ULV Intel Celeron M Processor at 600 MHz

For more details, see the *Ultra Low Voltage Intel Celeron M Processor at 600 MHz Addendum to the Intel Celeron M Processor Datasheet*.

2.3.6.1 Architectural Features

- On-die 512-Kbyte second Level Cache
- On-die primary 32-kB instruction cache and 32-kB write-back data cache
- Supports Streaming SIMD Extensions 2 (SSE2)
- Assisted Gunning Transceiver Logic (AGTL+) bus driver technology
- Supports Intel architecture with dynamic execution
- 400-MHz, source-synchronous front side bus (FSB)
- No support for Enhanced Intel SpeedStep Technology, Deeper Sleep operation, or Intel Thermal Monitor 2.

2.3.6.2 Packaging/Power

- 600 MHz operation, available in 479-ball micro FCBGA packages.
- VCCA: 1.8 V
- TDP = 7 W
- IMVP-IV Voltage Regulator Design Guidelines

2.4 Intel® 852GM Chipset Graphics Memory Controller Hub (GMCH)

2.4.1 Processor Front Side Bus Support

- AGTL+ bus driver technology (gated AGTL+ receivers for reduced power)
- Supports 32-bit AGTL+ bus addressing (no support for 36-bit address extension)
- Supports Uniprocessor (UP) systems
- 400 MT/s FSB support
- Supports in-order and dynamic deferred transactions

2.4.2 Integrated System Memory DRAM Controller

- Supports up to two double-sided DIMMs (four rows populated) with unbuffered PC1600/PC2100 (Without ECC)
- ECC not support
- Maximum of 1 GB of system memory (using 256 Mb technology devices and two DIMMs) and up to 2 GB of system memory (using high density 512 Mb technology).
- Supports 64-Mb, 128-Mb, 256-Mb, and 512-Mb technologies for x8 and x16 width devices
- Supports 200-MHz and 266-MHz DDR devices
- 64-bit data interface
- Supports up to 16 simultaneous open pages
- Support for DIMM Serial Presence Detect (SPD) scheme via SMBus interface
- STR power management support via self refresh mode using CKE

2.4.3 Integrated Graphics Controller

- Graphics Core Frequency
 - Display/render frequency up to 133 MHz
- 3D Graphics Engine
 - 3D Setup and Render Engine
 - High quality performance Texture Engine

- Analog Display Support
 - 350-MHz integrated 24-bit RAMDAC
 - Hardware color cursor support
 - Accompanying I2C and DDC channels provided through multiplexed interface
 - Hotplug and display support
 - Dual independent pipe for dual independent display
- Digital Video Out Port (DVO) support
 - Single channel DVO Port with 165-MHz dot clock support for a 12-bit interface
 - Compliant with DVI Specification 1.0
- Dedicated LFP (local flat panel) interface
 - Single or dual channel LVDS TFT panel support up to SXGA+ panel resolution with frequency range from 25 MHz to 112 MHz per channel
 - SSC support of 0.5%, 1.0%, and 2.5% center and down spread with external SSC clock
 - Dual Display Twin (Single pipe LVDS+CRT) is not supported if SSC is enabled
 - Supports data format of 18 bpp
 - LCD panel power sequencing compliant with SPWG timing specification
 - Compliant with ANSI/TIA/EIA -644-1995 spec
 - Integrated PWM interface for LCD backlight inverter control
 - Compliant with CPIS Specification 1.5
 - Bi-linear Panel fitting

2.4.4 Packaging/Power

- 732-pin Micro-FCBGA (37.5 mm x 37.5 mm)
- VTTLF, VTTHF (1.05 V);
- VCC, VCCASM, VCCHL, VCCAHPDLL, VCCAGPLL, VCCADPLLA, VCCADPLLB (1.2 V);
- VCCADAC, VCCDVO, VCCDLVDS, VCCALVDS, (1.5 V);
- VCCSM, VCCQSM, VCCTXLVDS (2.5 V);
- VCCGPIO (3.3 V)

2.4.5 Intel® 82801DB I/O Controller Hub 4 (ICH4)

- Upstream accelerated hub architecture interface at 266 Mbytes/s for access to the Intel® 82852GM GMCH.
- PCI 2.2 interface (six PCI req/grant pairs)
- Bus Master IDE controller (supports Ultra ATA 100/66/33)
- USB 2.0 controller

- SMBus controller
- FWH interface
- LPC interface
- AC'97 2.3 interface
- Integrated system management controller
- Alert-On-LAN
- IRQ controller

2.4.6 Packaging/Power

- 421-pin BGA (31mm x 31mm)
- VCC1_5 (1.5 V main logic voltage 550 mA); VCCSUS1_5 (1.5 V resume logic voltage 87.3 mA); VCC3_3 (3.3 V main I/O voltage 528 mA); VCCSUS3_3 (3.3 V resume I/O voltage 168 mA); V5REF (5 V); V5REF_SUS (5 V); VCCRTC (2.0 V-3.3 V); VCCHI (1.5 V 99 mA)

2.4.7 Firmware Hub (FWH)

- An integrated hardware Random Number Generator (RNG)
- Register-based locking
- Hardware-based locking
- Five GPIOs

2.4.7.1 Packaging/Power

- 32-pin TSOP/PLCC
- 3.3 V core and 3.3 V/12 V for fast programming
- Register-based locking

General Design Considerations

3

This section documents PCB layout and routing guidelines for Intel® 852GM chipset platforms. It does not discuss the functional aspects of a bus or the layout guidelines for an add-in device.

Note: If the guidelines listed in this document are not followed, then complete thorough signal integrity and timing simulations for each design. Even when the guidelines are followed, Intel recommends that critical signals be simulated to ensure proper signal integrity and flight time. Simulate any deviation from the guidelines.

The trace impedance typically noted, $55\ \Omega \pm 15\%$ (but $\pm 10\%$ preferred), is the nominal trace impedance for a 5 mil wide external trace and a 4 mil wide internal trace. However, some stack-ups may lead to narrower or wider traces on internal or external layers in order to meet the $55\ \Omega$ impedance target. It is important to consider the minimum and maximum impedance of a trace based on the switching of neighboring traces when calculating flight times. Using wider spaces between the traces may minimize this trace-to-trace coupling. In addition, these wider spaces reduce settling time.

Coupling between two traces is a function of the following:

- Coupled length
- Distance separating the traces
- Signal edge rate
- Degree of mutual capacitance and inductance

To minimize the effects of trace-to-trace coupling, follow the routing guidelines documented in this section. Verify that all high-speed impedance controlled signals (for example, FSB signals) have continuous ground referenced planes and are not routed over or under power/ground plane splits.

3.1 Board Stack-Up

The Intel 852GM chipset-based platforms require a board stack-up yielding a target impedance of $55\ \Omega \pm 15\%$. An example of an 8-layer board stack-up is shown in [Figure 4](#). The left side of the figure illustrates the starting dimensions of the metal and dielectric material thickness as well as drawn trace width dimensions prior to lamination, conductor plating, and etching. After the PCB materials are laminated, conductors plated, and etched, somewhat different dimensions result. Dielectric materials become thinner, under/over etching of conductors alters their trace width, and conductor plating makes them thicker.

Note: For the purpose of extracting electrical models from transmission line properties, use the final dimensions of signals after lamination, plating, and etching.

The stack-up uses 1.2 mil (1 oz.) copper on power planes to reduce I*R drops and 0.6 mil copper thickness on signal layers Layer 1 (L1) and Layer 8 (L8). Additionally, 1.2-mil copper thickness is used on the internal signal layers: Layer 3 (L3), and Layer 6 (L6). After plating, the external layers become 1.2 to 2 mils thick.

To ensure impedance control of 55 Ω , verify that the primary and secondary layer microstrip lines reference solid ground planes on Layer 2 (L2) and Layer 7 (L7), respectively.

Figure 4 shows the recommended board stack-up dimensions.

Figure 4. Example Board Stack-Up Dimensions

				Dielectric	Layer	Layer
				Thickness	No.	Type
S	Stackup			(mils)		
					1	SIGNAL
	PREPREG =>			5.0		
P	CORE =>			5.0	2	PLANE
S	PREPREG =>			12.0	3	SIGNAL
P	CORE =>			10.0	4	PLANE
P	PREPREG =>			12.0	5	PLANE
S	CORE =>			5.0	6	SIGNAL
P	PREPREG =>			5.0	7	PLANE
					8	SIGNAL
S						

- Internal signal traces on L3 and L6 are unbalanced strip lines. To meet the nominal 55 Ω characteristic impedance for these traces, they reference the solid ground plane on L2 and L7. Since the coupling to L4 and L5 is still significant, (especially true when thinner stack-ups use balanced strip lines on internal layers) these layers are converted to ground floods in the areas of the PCB where the speed critical interfaces like the FSB or DDR system memory are routed. In the remaining sections of the PCB layout, the L4 and L5 layers are used for power delivery.
- L8 is also used for power delivery in many cases since it benefits from the thick copper plating of the external layer plating as well as referencing the close (3.0 mil pre-peg thickness) L7 ground plane. The benefit of such a stack-up is low inductance power delivery.

3.2 Alternate Stack-Ups

Designers may choose to use different stack-ups (number of layers, thickness, trace width, etc.) from the one example outlined in [Figure 4](#). However, observe the following key elements:

- Use final post lamination, post etching, and post plating dimensions for electrical model extractions.
- Power plane layers should be 1 oz. thick and the outer signal layers should be 0.5 oz. thick, while the internal signal layers should be 1 oz. thick. External layers become 1-1.5 oz. (1.2-2 mils) thick after plating.
- Verify that all high-speed signals reference solid ground planes through the length of their routing and are not crossing plane splits. To ensure this, both planes surrounding strip lines should be ground.
- Intel recommends that high-speed signal routing be done on internal, strip-line layers.
- With high-speed signals transitioning between layers next to the component, account for signal pins by the ground stitching vias that would stitch all the ground plane layers in that area of the PCB. Due to the arrangement of the processor and Intel® 82852GM GMCH pin maps, ground vias placed near all ground lands are also be very close to high-speed signals that may be transitioning to an internal layer. Thus, no additional ground stitching vias (besides the ground pin vias) are required in the immediate vicinity of the Processor and Intel® 82852GM GMCH packages to accompany the signal transitions from the component side into an internal layer.
- Verify that high-speed routing on external layers is minimized to avoid EMI. Routing on external layers also introduces different delays compared to internal layers, making length matching extremely difficult if some routing is done on both internal and external layers.
- When recommended stackup guidelines are not used, the designers is liable for all aspects of their board design (for example, understanding impacts of signal integrity (SI) and power distribution, etc.)



Intel® Celeron® Processor Front Side Bus Design Guidelines

4

The Intel® Celeron® processor utilizes Flip-Chip Pin Grid Array (FC-PGA2) package technology and plugs into a 478-pin, surface-mount, Zero Insertion Force (ZIF) socket, referred to as the mPGA478B socket. The Intel Celeron processor maintains full compatibility with IA-32 software. The Intel Celeron processor's 400-MT/s Intel NetBurst® microarchitecture front side bus (FSB) utilizes a split-transaction, deferred reply.

The following layout guidelines support designs using the Intel Celeron processor and the Intel® 852GM chipset. Due to on-die Rtt resistors on both the processor and the chipset, additional resistors do not need to be placed on the PCB for most FSB signals. The exception to these are RESET# and BPM[5:0]# signals, which require a 51Ω pull-up, and the BR0 signal, which requires 220 Ω ± 5% pull-up to VCC_CPU on the processor end of the transmission line.

4.1 Processor Front Side Bus (FSB) Routing Guidelines

Table 3 presents and summarizes the layout recommendations for the Intel Celeron Processor and expands on specific design issues and their recommendations.

Table 3. FSB Routing Summary for the Processor (Sheet 1 of 2)

Parameter	Processor Routing Guidelines
Line-to-line spacing	Greater than or equal to 2:1 edge-to-edge spacing versus trace width for address and address strobes See Figure 5 for illustrations of this recommendation.
Data line lengths (agent-to-agent spacing)	<ul style="list-style-type: none"> 1.0 inches - 6.0 inches from pin-to-pin Data signals of the same source synchronous group to the same pad-to-pad length within ± 0.100 inches of the associated strobes. The pad is defined as the attach point of the silicon die to the package substrate. Length must be added to the system board to compensate for package length differences. Route signals in the same source synchronous group on the same layer and reference to Vss with 2:1 spacing.
DSTBn/p[3:0]#	<ul style="list-style-type: none"> Route a data strobe and its complement within ± 0.025 inch of the same pad-to-pad length. The pad is defined as the attach point of the silicon die to the package substrate. Length must be added to the system board to compensate for package length differences. Route DSTBN/P# on the same layer as their associated data group and reference to Vss.

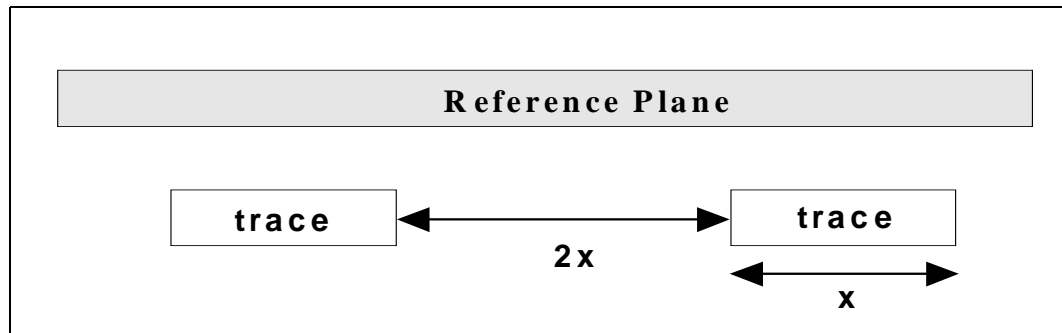
1. Refer to the Intel® 852GM Chipset GMCH Datasheet for GMCH package dimensions and refer to the Intel® Celeron® Processor Datasheet for processor package dimensions.

Table 3. FSB Routing Summary for the Processor (Sheet 2 of 2)

Parameter	Processor Routing Guidelines
Address line lengths (agent-to-agent spacing)	<ul style="list-style-type: none"> 1.0 inches - 6.0 inches pin-to-pin. Address signals of the same source synchronous group should be routed to the same pad-to-pad length within ± 0.200 inch of the associated strobes. The pad is defined as the attach point of the silicon die to the package substrate. Length must be added to the system board to compensate for package length differences. A layer transition may occur if the reference plane remains the same (Vss) and the layers are of the same configuration (all stripline or all microstrip).
ADSTBN/P[1:0]#	<ul style="list-style-type: none"> Route an address strobe and its complement within ± 0.200 inch of the same pad-to-pad length. The pad is defined as the attach point of the silicon die to the package substrate. Length must be added to the system board to compensate for package length differences. A layer transition may occur if the reference plane remains the same (Vss) and the layers are all of the same configuration (all stripline or all microstrip).
Common clock line lengths	2.0 inches - 6.0 inches
Topology	Stripline
Routing priorities	<ul style="list-style-type: none"> Route all associated signals and strobes on the same layer for entire length of bus. Reference all signals to Vss. Ideally, layer changes should not occur for any signals. When a layer change must occur, the reference plane must be Vss and the layers must all be of the same configuration (all stripline or all microstrip for example).
Clock keepout zones	Maintain a spacing requirement of 16-20 mils around all clocks.
Trace Impedance	$55 \Omega \pm 15\%$
Source synchronous routing restrictions	<ul style="list-style-type: none"> There are no length-matching routing restrictions between (or within) either the source-synchronous data or address groups. As long as the strobe and associated line length routing guidelines are met for each group, there is no need to length-match between the groups. For example, one data group may be routed to the minimum allowable length while another data group could be routed to the maximum allowable length. Simulations have verified that the FSB functions correctly even under this extreme condition.

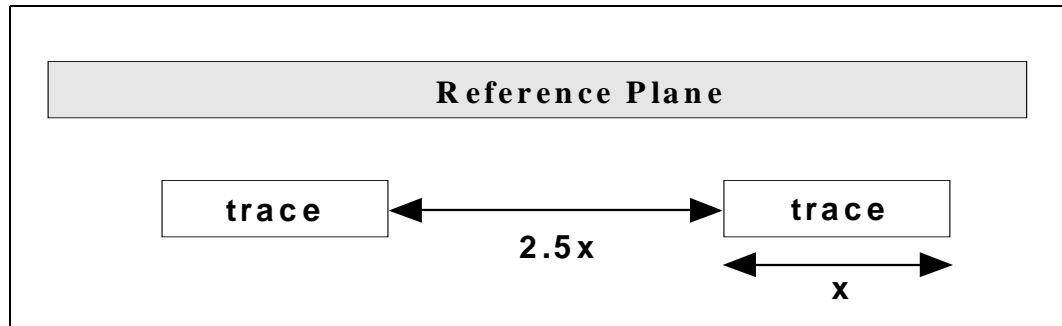
1. Refer to the *Intel® 852GM Chipset GMCH Datasheet* for GMCH package dimensions and refer to the *Intel® Celeron® Processor Datasheet* for processor package dimensions.

Figure 5. Cross-Sectional View of 2:1 Ratio



This is the edge-to-edge trace spacing versus width. For address and address strobes; a trace spacing-to-width ratio of 2 to 1 ensures a low crosstalk coefficient (based on geometries defined in 8 layer reference stackup). For data and data strobes, a trace spacing to width ratio of 2.5 to 1 or greater (as shown in Figure 6) ensures a low crosstalk coefficient (based on geometries defined in 8 layer reference stackup). All the effects of crosstalk are difficult to simulate. A smaller ratio would have an unpredictable impact due to crosstalk.

Figure 6. Cross-Sectional View of 2:5:1 Ratio



4.1.1 Return Path Evaluation

The return path is the route current takes to return to its source. It may take a path through ground planes, power planes, other signals, integrated circuits, vias, VRMs, etc. Think of the return path as following a path of least resistance back to the original source. Discontinuities in the return path often have signal integrity and timing effects that are similar to the discontinuities in the signal conductor. Therefore, the return paths must be given similar considerations. A way to evaluate return path parasitic inductance is to draw a loop that traces the current from the driver through the signal conductor to the receiver, then back through the ground/power plane to the driver again. The smaller the area of the loop, the lower the parasitic inductance.

The following sets of return path rules apply:

- Always trace out the return current path and provide as much care to the return path as the path of the signal conductor.
- Decoupling capacitors do not adequately compensate for a plane split.
- Do not allow splits in the reference planes in the path of the return current.
- Do not allow routing of signals on the reference planes near FSB signals.

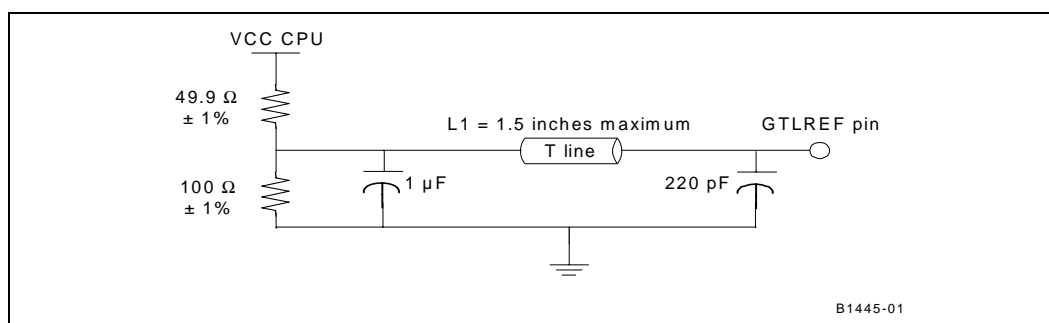
- Maintain VSS as a reference plane for all FSB signals.
- Do not route over via anti-pads or socket anti-pads.

4.2 GTLREF Layout and Routing Recommendations

There are four AGTL+ GTLREF pins on the processor that are used to set the reference voltage level for the AGTL+ signals (GTLREF). Because all of these pins are connected inside the processor package, the GTLREF voltage must be supplied to only one of the four pins.

Figure 7 shows an example of GTLREF routing.

Figure 7. GTLREF Routing



- The processor must have one dedicated voltage divider.
- Decouple the voltage divider with a 1µF capacitor.
- Keep the voltage divider within 1.5 inches of the GTLREF pin.
- Decouple the pin with a high-frequency capacitor (such as a 220 pF 603) as close to the pin as possible.
- Keep signal routing at least 10 mils separated from the GTLREF routes. Use at least a 7 mil trace for routing.
- Do not allow signal lines to use the GTLREF routing as part of their return path (that is, do not allow the GTLREF routing to create splits or discontinuities in the reference planes of the FSB signals).

4.3 Processor Configuration

This section provides more details for routing Intel Celeron Processor-based systems. This information is preliminary and subject to change. Both recommendations and considerations are presented.

For proper operation of the Intel Celeron Processor and the Intel 852GM chipset, it is necessary to meet the timing and voltage specifications of each component. The following recommendations are Intel's best guidelines based on extensive simulation and experimentation that make assumptions, which may be different than an OEM's system design. The most accurate way to understand the signal integrity and timing of the FSB in your platform is by performing a comprehensive simulation analysis. It is conceivable that adjustments to trace impedance, line length, termination impedance, board stackup and other parameters may improve system performance.

Refer to the *Intel Celeron Processor Datasheet* for a FSB signal list, signal types and definitions.

4.4 General Topology and Layout Guidelines

The following topology and layout guidelines are preliminary and subject to change. The guidelines are derived from empirical testing with preliminary Intel 852GM chipset package models.

4.4.1 Design Recommendations

This following subsections contain the design recommendations for the data, address, strobes, and common clock signals. For the following discussion, the pad is defined as the attach point of the silicon die to the package substrate.

4.4.1.1 Data

Route data signals of the same source-synchronous group to the same **pad-to-pad** length within ± 0.100 inch of the associated strobes. As a result, additional traces are added to some data nets on the system board in order for all trace lengths within the same data group to be the same length (± 0.100 inch) from the **pad** of the processor to the **associated pad** of the chipset.

Equation 1. Calculation to Determine Package Delta Addition to PCB Length for UP Systems

$$\text{delta}_{\text{net,stroke}} = (\text{cpu_pkglen}_{\text{net}} - \text{cpu_pkglen}_{\text{stroke}}) + (\text{cs_pkglen}_{\text{net}} - \text{cs_pkglen}_{\text{stroke}})$$

* Strobe package length is the average of the strobe pair.

Refer to the *Intel® 852GM Chipset GMCH Datasheet* for GMCH package dimensions and refer to the *Intel® Celeron Processor Datasheet* for package dimensions.

4.4.1.2 Address

Address signals follow the same rules as data signals except they should be routed to the same **pad-to-pad** length within ± 0.200 inch of the associated strobes. Address signals may change layers if the reference plane remains Vss.

4.4.1.3 Strobe

Route a strobe and its complement to a length equal to their corresponding data group's mean **pad-to-pad** length ± 0.025 inch.

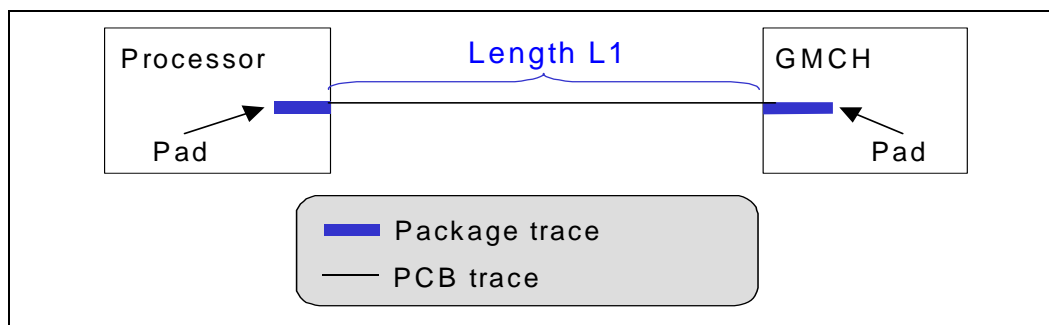
4.4.1.4 Common Clock

Route common clock signals to a minimum pin-to-pin PCB length of **2.0** inches and a maximum PCB length of **6.0** inches.

Route source synchronous groups and associated strobes on the same layer for the entire length of the bus. This results in a significant reduction of the flight time skew since the dielectric thickness, line width, and velocity of the signals will be uniform across a single layer of the stackup. A relationship of dielectric thickness, line width, and velocity between layers cannot be ensured.

Figure 8 shows the processor topology.

Figure 8. Processor Topology



4.4.2 Source Synchronous (SS) Signals

Table 4 presents the FSB data signal routing guidelines. Table 5 presents the FSB address signal routing guidelines.

Table 4. FSB Data Signal Routing Guidelines

Signal Names		Transmission Line Type	Total Trace Length		Nominal Impedance (Ω)	Width and Spacing (mils)
CPU	GMCH		Min. (inches)	Max. (inches)		
DBI[3:0]#	DINV[3:0]#	stripline	1.0	6.0	$55 \pm 15\%$	4.5 and 11.5
D[63:0]#	HD[63:0]#	stripline	1.0	6.0	$55 \pm 15\%$	4.5 and 11.5
DSTBN[3:0]#	HDSTBN[3:0]#	stripline	1.0	6.0	$55 \pm 15\%$	4.5 and 11.5
DSTBP[3:0]#	HDSTBP[3:0]#	stripline	1.0	6.0	$55 \pm 15\%$	4.5 and 11.5

NOTE: The data signals within each group must be routed to within ± 0.100 inch of its associated reference strobe. The complement strobe must be routed to within ± 0.025 inch of the associate reference strobe. All traces within each signal group must be routed on the same layer (required). Intel recommends that length of the strobes be centered to the average length of associated data or address traces to maximize setup/hold time margins.

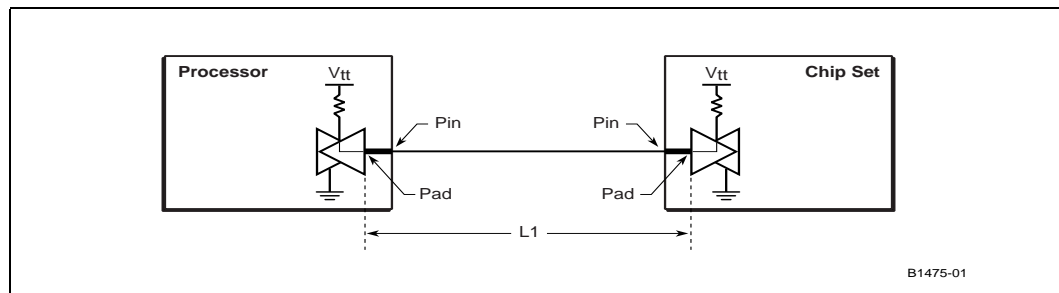
Table 5. FSB Address Signal Routing Guidelines

Signal Names		Transmission Line Type	Total Trace Length		Nominal Impedance (Ω)	Width and Spacing (mils)
CPU	GMCH		Min. (inches)	Max. (inches)		
A[31:3]#	HA[31:3]#	Stripline	1.0	6.0	55 \pm 15%	4.5 and 9
REQ[4:0]#	HREQ[4:0]#	Stripline	1.0	6.0	55 \pm 15%	4.5 and 9
ADSTB[1:0]#	HADSTB[1:0]#	Stripline	1.0	6.0	55 \pm 15%	4.5 and 9

NOTE: The address signals within each group must be routed to within ± 0.200 inch of its associated strobe. All traces within each signal group must be routed on the same layer (required). Intel recommends that length of the strobes be centered to the average length of associated data or address traces to maximize setup/hold time margins.

Figure 9 shows the SS topology for address and data.

Figure 9. SS Topology for Address and Data



4.4.3 Common Clock (CC) AGTL+ Signals

Table 6 presents the FSB control signal routing guidelines.

Table 6. FSB Control Signal Routing Guidelines (Sheet 1 of 2)

Signal Names		Topology	Routing Trace Length (Pin-to-Pin)		Nominal Impedance (Ω)	Width and spacing (mils)
CPU	GMCH		Max. (inches)	Min. (inches)		
RESET#	CPURST#	Stripline	6.0	2.0	55 \pm 15%	4.5 and 11.5
BR0#	BREQ0#	Stripline	6.0	2.0	55 \pm 15%	4.5 and 11.5
BNR#	BNR#	Stripline	6.0	2.0	55 \pm 15%	4.5 and 11.5
BPRI#	BPRI#	Stripline	6.0	2.0	55 \pm 15%	4.5 and 11.5
DEFER#	DEFER#	Stripline	6.0	2.0	55 \pm 15%	4.5 and 11.5
LOCK#	HLOCK#	Stripline	6.0	2.0	55 \pm 15%	4.5 and 11.5
TRDY#	HTRDY#	Stripline	6.0	2.0	55 \pm 15%	4.5 and 11.5

NOTE: Trace width of 4.5 mils and trace spacing of 11.5 mils within signal groups. The entire trace for each signal routed on one layer (recommended) RESET# and BR0# are CC AGTL+ signals without on-die termination (ODT). For these signals, place Rtt near CPU: L2 \leq 0.5 inch. Rtt = 51.1 \pm 1%. Routing these signals to four inches \pm 0.5 inch should maximize the setup and hold margin parameters while adhering to expected solution design constraints.

Table 6. FSB Control Signal Routing Guidelines (Sheet 2 of 2)

Signal Names		Topology	Routing Trace Length (Pin-to-Pin)		Nominal Impedance (Ω)	Width and spacing (mils)
CPU	GMCH		Max. (inches)	Min. (inches)		
DRDY#	DRDY#	Stripline	6.0	2.0	55 \pm 15%	4.5 and 11.5
ADS#	ADS#	Stripline	6.0	2.0	55 \pm 15%	4.5 and 11.5
DBSY#	DBSY#	Stripline	6.0	2.0	55 \pm 15%	4.5 and 11.5
HIT#	HIT#	Stripline	6.0	2.0	55 \pm 15%	4.5 and 11.5
HITM#	HITM#	Stripline	6.0	2.0	55 \pm 15%	4.5 and 11.5
RS[2:0]#	RS[2:0]#	Stripline	6.0	2.0	55 \pm 15%	4.5 and 11.5

NOTE: Trace width of 4.5 mils and trace spacing of 11.5 mils within signal groups. The entire trace for each signal routed on one layer (recommended) RESET# and BR0# are CC AGTL+ signals without on-die termination (ODT). For these signals, place Rtt near CPU: L2 \leq 0.5 inch. Rtt = 51.1 \pm 1%. Routing these signals to four inches \pm 0.5 inch should maximize the setup and hold margin parameters while adhering to expected solution design constraints.

4.4.4 Asynchronous AGTL+ and Other Signals

This section describes layout recommendations for signals other than data, strobe, and address. All signals must meet AC and DC specifications as documented in the respective Intel Celeron Processor Datasheets.

The following sections describe the topologies and layout recommendations for the miscellaneous signals.

4.4.4.1 Topology 1A: Asynchronous GTL+ Signal Driven by the Processor—IERR# and FERR#

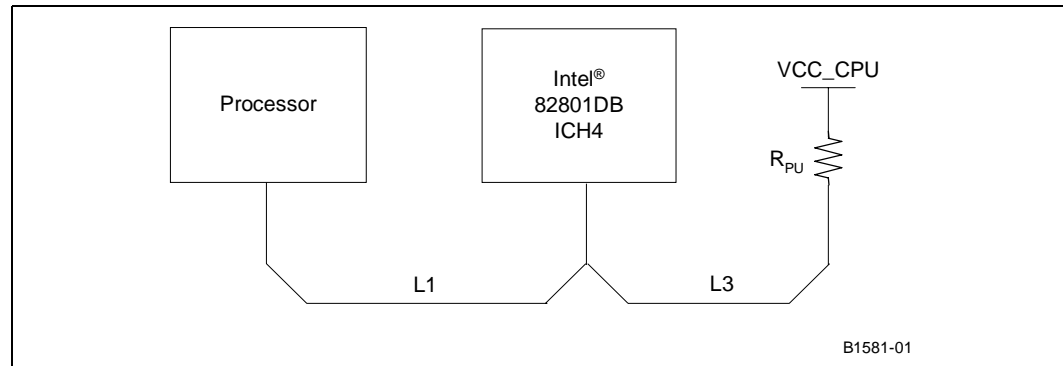
IERR# and FERR# should adhere to the routing and layout recommendations described and illustrated in Table 7 and Figure 10.

Due to the dependencies on system design implementation, IERR# may be implemented in a number of ways to meet design goals. IERR# may be routed as a test point or to any optional system receiver. Intel recommends that the FERR# signal of the Intel Celeron Processor to be routed to the FERR# signal of the Intel® 82801DB ICH4.

Table 7. Layout Recommendations for IERR# and FERR# Signal—Topology 1A

Trace Zo	Trace Spacing	L1	L3	Rpu
55 Ω	7 mil	1 in.—12 in.	3 in. max	62 $\Omega \pm 5\%$

Figure 10. Routing Illustration for FERR#



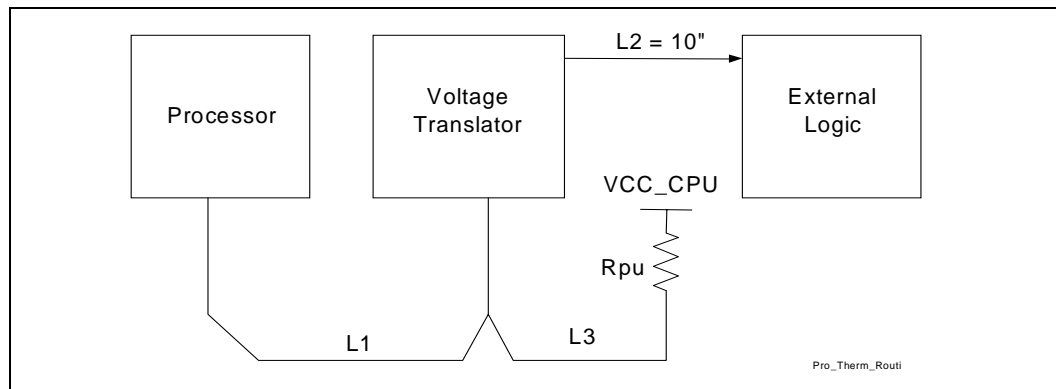
4.4.4.2 Topology 1B: Asynchronous GTL+ Signal Driven by the Processor—PROCHOT#

PROCHOT# should adhere to the routing and layout recommendations described and illustrated in Table 8 and Figure 11. When PROCHOT# is routed to external logic, voltage translation may be required to avoid excessive voltage levels at the processor and meet input thresholds for the external logic.

Table 8. Layout Recommendations for PROCHOT# Signal—Topology 1B

Trace Zo	Trace Spacing	L1	L2	L3	Rpu
55 Ω	7 mil	1 in.—17 in.	10 in. max	3 in. max	62 $\Omega \pm 5\%$

Figure 11. Routing Illustration for PROCHOT#



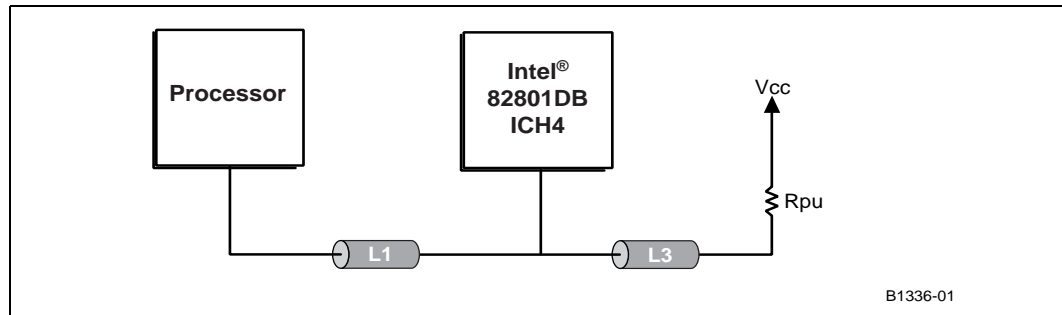
4.4.4.3 Topology 1C: Asynchronous GTL+ Signal Driven by the Processor—THERMTRIP#

THERMTRIP# should adhere to the routing and layout recommendations described and illustrated in Table 9 and Figure 12. When THERMTRIP# is routed to external logic, voltage translation may be required to avoid excessive voltage levels at the processor and meet input thresholds for the external logic.

Table 9. Layout Recommendations for THERMTRIP# Signal—Topology 1C

Trace Zo	Trace Spacing	L1	L3	Rpu
55 Ω	7 mil	1 in.—12 in.	3 in. max	62 $\Omega \pm 5\%$

Figure 12. Routing Illustration for THERMTRIP#



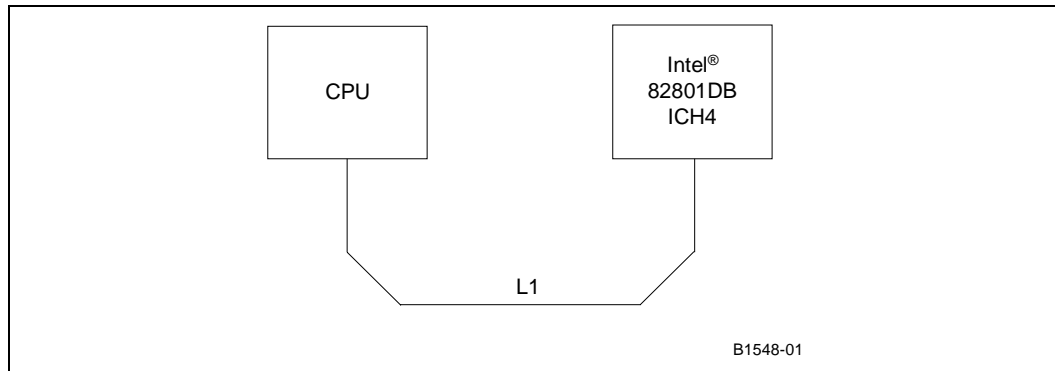
4.4.4.4 Topology 2A: Asynchronous GTL+ Signals Driven by the Intel® 82801DB ICH4—A20M#, IGNNE#, LINT[1:0], SLP#, SMI#, and STPCLK#

The Topology 2A CMOS A20M#, IGNNE#, LINT0/INTR, LINT1/NMI, SLP#, SMI#, and STPCLK# signals should implement a point-to-point connection between the ICH4 and the Celeron processor. The routing guidelines allow both signals to be routed as either microstrip or strip lines using $55\ \Omega \pm 15\%$ characteristic trace impedance. No additional PCB components are necessary for this topology. See [Table 10](#) and [Figure 13](#) for more information.

Table 10. Layout Recommendations for Topology 2A

L1	Transmission Line Type
0.5" - 12.0"	Microstrip
0.5" - 12.0"	Stripline

Figure 13. Routing Illustration Topology 2A



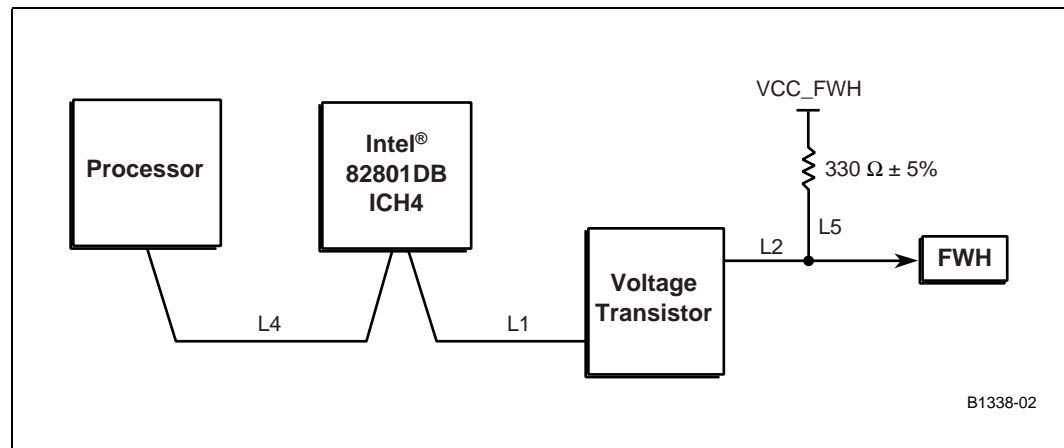
4.4.4.5 Topology 2B: Asynchronous GTL+ Signal Driven by the Intel® 82801DB ICH4—INIT#

INIT# should adhere to the routing and layout recommendations described and illustrated in Table 11 and Figure 14.

Table 11. Layout Recommendations for INIT#—Topology 2B

Trace Zo	Trace Spacing	L1	L2	L4	L5	Rpu
55 Ω	7 mils	2 in. max	10 in. max	17 in. max	3 in. max	330 $\Omega \pm 5\%$

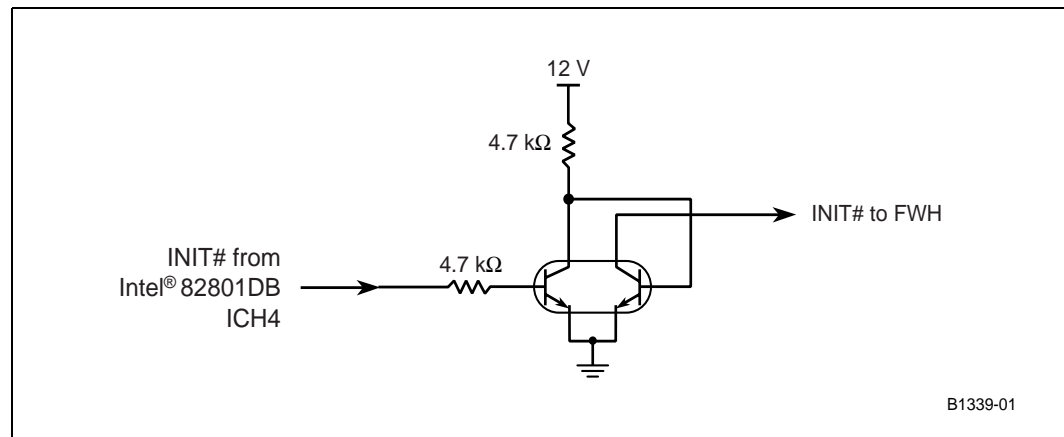
Figure 14. Routing Illustration for INIT#



Level shifting is required for the INIT# signal to the FWH to meet input logic levels of the FWH.

Figure 15 illustrates one method of level shifting.

Figure 15. Voltage Translation of INIT#



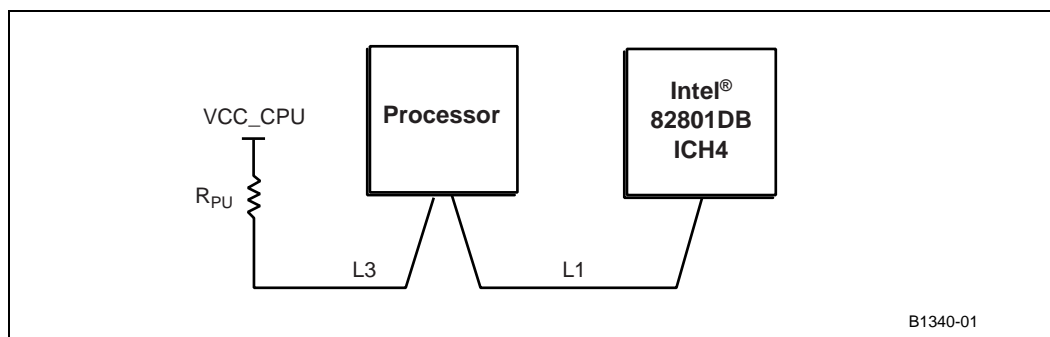
4.4.4.6 Topology 2C: Miscellaneous Signal Driven by the Intel® 82801DB ICH4 Open Drain—PWRGOOD

PWRGOOD should adhere to the routing and layout recommendations described and illustrated in Table 12 and Figure 16.

Table 12. Layout Recommendations for Miscellaneous Signals—Topology 2C

Trace Zo	Trace Spacing	L1	L3	Rpu
55 Ω	7 mil	1 in.–12 in.	3 in. max	300 $\Omega \pm 5\%$

Figure 16. Routing Illustration for PWRGOOD



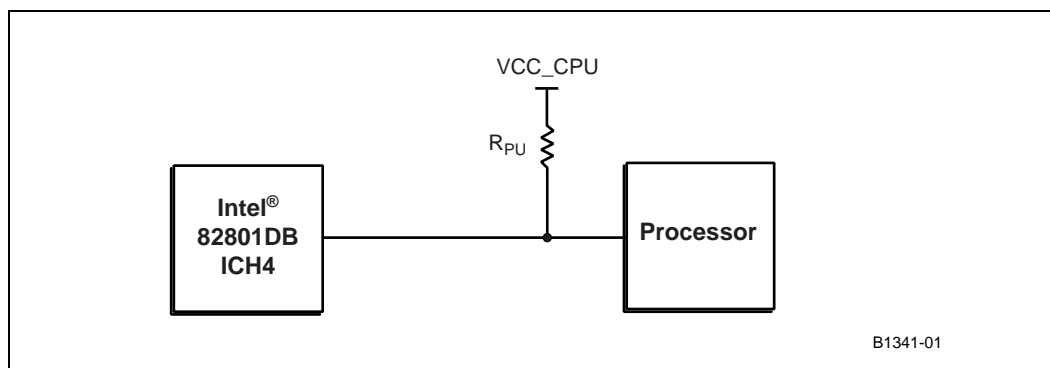
4.4.4.7 Topology 3: VCCIOPLL, VCCA and VSSA

VCCIOPLL and VCCA are isolated power for internal PLLs. It is critical that they have clean, noiseless power on their input pins. See Section 7.4.2. for further details.

4.4.4.8 Topology 4: BR0# and RESET#

Since the processor does not have on-die termination on the BR0# and RESET# signals, it is necessary to terminate the signals using discrete components on the system board. Connect the signals between the components as shown in Figure 17. The Intel 852GM chipset has on-die termination; therefore, it is necessary to terminate only at the processor end. The value of Rpu should be 51 $\Omega \pm 5\%$ for RESET#. BR0# signal requires 220 $\Omega \pm 5\%$ pull-up to VCC_CPU on the processor end of the transmission line.

Figure 17. Routing Illustration for BR0# and RESET#



4.4.4.9 Topology 5: COMP[1:0] Signals

The Intel Celeron Processor has two COMP[1:0] pins, and the Intel 82852GM GMCH has two pins, HXRCOMP and HYRCOMP, that require compensation resistors to adjust the AGTL+IO buffer characteristics to specific board and operating environment characteristics.

Terminate the COMP[1:0] pins to ground through a $51.1 \Omega \pm 1\%$ resistor as close as possible to the pin. Do not wire COMP pins together; connect each pin to its own termination resistor. RCOMP value may be adjusted to set external drive strength of I/O and to control the edge rate.

4.4.4.10 Topology 6: THERMDA/THERMDC Routing Guidelines

The processor incorporates an on-die thermal diode. THERMDA (diode anode) and THERMDC (diode cathode) pins on the processor can be connected to a thermal sensor located on the system board to monitor the die temperature of the processor for thermal management/long-term die temperature change monitoring purpose. This thermal diode is separate from the thermal monitor's thermal sensor and cannot be used to predict the behavior of the thermal monitor.

Since the thermal diode is used to measure a very small voltage from the remote sensor, take care to minimize noise induced at the sensor inputs. The following are some guidelines:

- Place the remote sensor as close as possible to THERMDA/THERMDC pins. It may be approximately four to eight inches away as long as the worst noise sources such as clock generators, data buses, and address buses, etc., are avoided.
- Route the THERMDA and THERMDC lines in parallel and close together with ground guards enclosed.
- Use wide tracks to reduce inductance and noise pickup that may be introduced by narrow ones. Intel recommends a width of 10 mils and spacing of 10 mils.

4.4.4.11 Topology 7: TESTHI Pins

Tie the TESTHI pins to the processor V_{CC} using a matched resistor, where a matched resistor has a resistance value within $\pm 20\%$ of the impedance of the board transmission line traces. For example, if the trace impedance is 50Ω then a value between 40Ω and 60Ω is required.

The TESTHI pins may use individual pull-up resistors or be grouped together as detailed below. Use a matched resistor for each group:

1. TESTHI[1:0]
2. TESTHI[7:2]
3. TESTHI[10:8]
4. TESTHI[12:11]

Additionally, if the ITPCLKOUT[1:0] pins are not used then they may be connected individually to V_{CC} using matched resistors or grouped with TESTHI[5:2] with a single matched resistor. When they are being used, individual termination with $1 \text{ k}\Omega$ resistors is acceptable. Tying ITPCLKOUT[1:0] directly to V_{CC} or sharing a pull-up resistor to V_{CC} prevents the use of debug interposers. This implementation is strongly discouraged for system boards that do not implement an onboard debug port.

As an alternative, group 2 (TESTHI [5:2]), and the ITPCLKOUT[1:0] pins may be tied directly to the processor V_{CC} . This has no impact on system functionality. TESTHI[0] and TESTHI[12] may also be tied directly to processor V_{CC} if resistor termination is a problem, but matched resistor termination is recommended. In the case of the ITPCLKOUT[1:0], direct tie to V_{CC} is strongly discouraged for system boards that do not implement an onboard debug port.

4.5 Additional Processor Design Considerations

This section documents system design considerations not addressed in previous sections.

4.5.1 Retention Mechanism Placement and Keepouts

The Retention Mechanism (RM) requires a keep-out zone for a limited component height area under the RM as shown in [Figure 18](#) and [Figure 19](#). The figures show the relationship between the RM mounting holes and pin one of the socket. They also document the keepouts.

The retention holes should be non-plated with primary and secondary side route keepout area of 0.409 inches diameter.

For heat sink volumetric information refer to:

- *Intel® Pentium® 4 Processor in the 478-pin package Thermal Design Guidelines*
- *Intel® Pentium® 4 Processor and Intel® Celeron® Processor in the 478-pin package Thermal Design Guide for Embedded Applications.*

Figure 18. Retention Mechanism Keep-Out Drawing 1

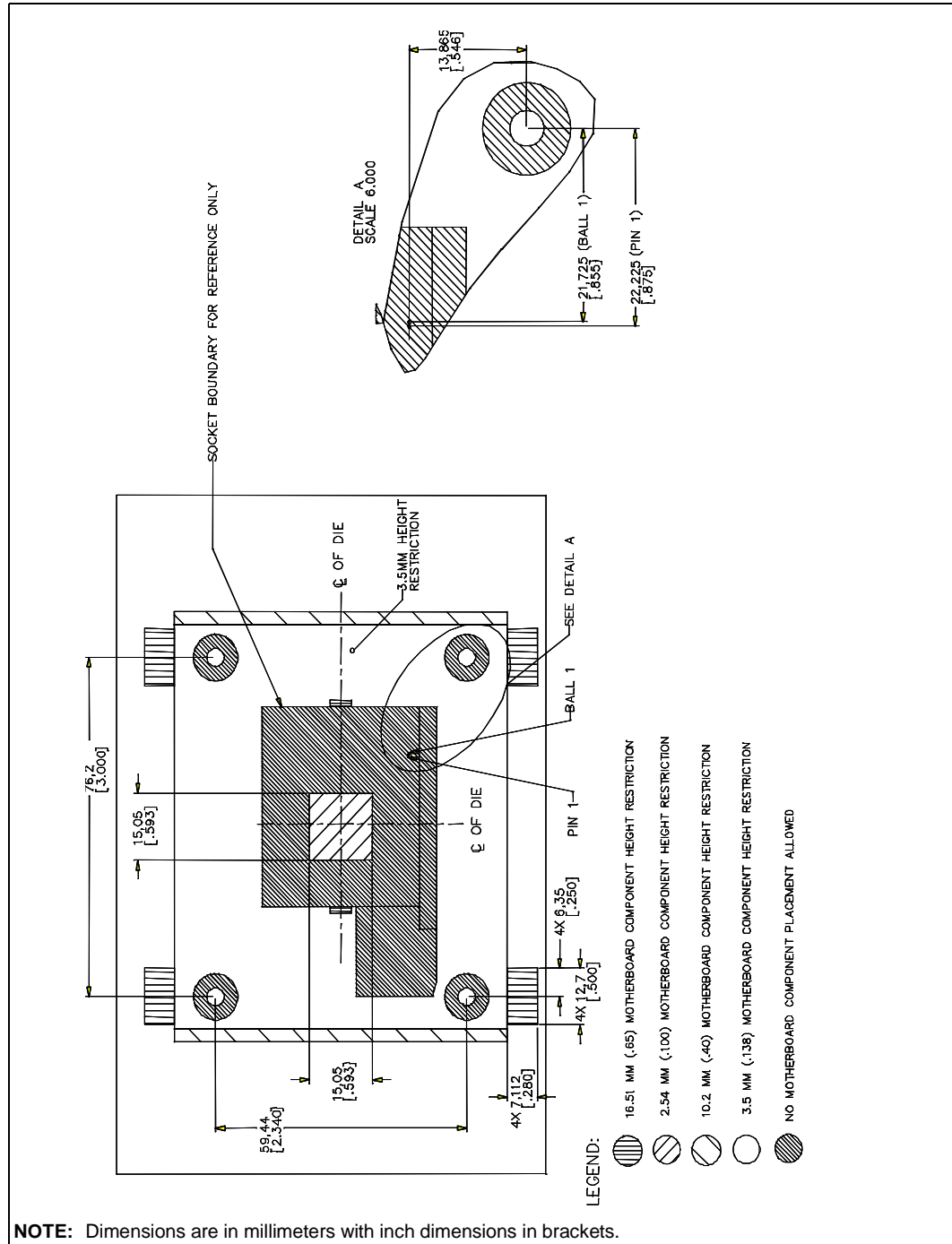
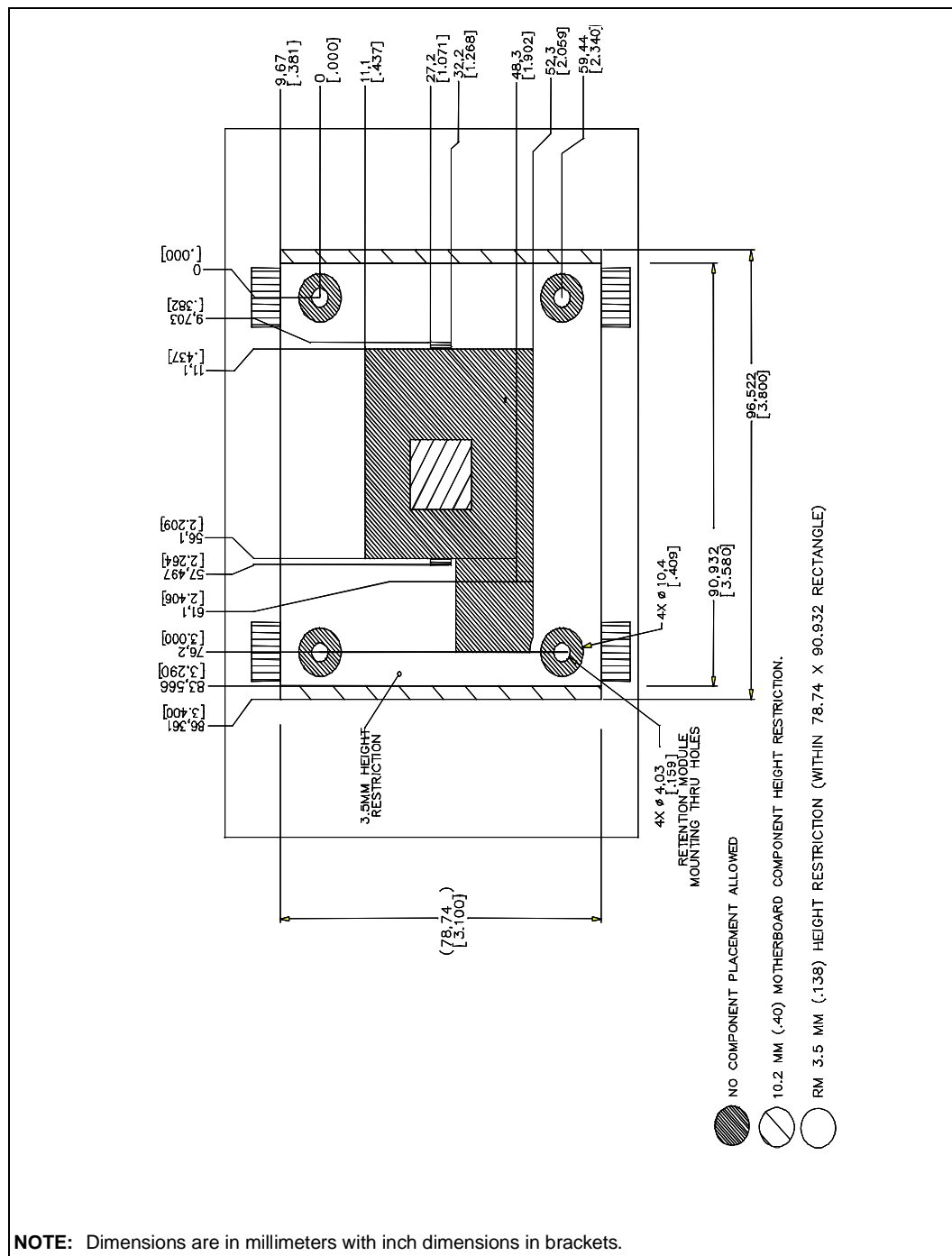


Figure 19. Retention Mechanism Keep-Out Drawing 2



4.5.2 Power Header for Active Cooling Solutions

The Intel reference-design heatsink includes an integrated fan. The recommended connector for the active cooling solution is a Walden*/Molex* 22-01-3037, AMP* 643815-3, or equivalent. The integrated fan requires the system board to supply a minimum of 740 mA at 12 V for proper operation. Table 13 presents the reference solution fan power header pinout.

Table 13. Reference Solution Fan Power Header Pinout

Pin Number	Signal
1	Ground
2	+12 V
3	No Connect

The Intel boxed processor heatsink includes an integrated fan. The recommended connector for the active cooling solution is a Walden*/Molex* 22-23-2037, AMP* 640456-3 or equivalent. The integrated fan requires the system board to supply a minimum of 740 mA at 12 V for proper operation. Table 14 presents the boxed processor fan power header pinout.

Table 14. Boxed Processor Fan Power Header Pinout

Pin Number	Signal
1	Ground
2	+12 V
3	Sense

The fan heatsink outputs a SENSE signal that is an open-collector output that pulses at a rate of two pulses per fan revolution. The system board requires a pull-up resistor to provide the appropriate V_{oh} level to match the fan speed monitor. Use of the SENSE signal is optional. Tie pin 3 to ground when the SENSE signal is not used.

For more information on boxed processor requirements, refer to the *Intel® Celeron® Processor on 0.13 Micron Process in the 478 Pin Package Datasheet*.

4.6 Debug Port Routing Guidelines

Refer to the latest revision of the *ITP700 Debug Port Design Guide* for details on the implementation of the debug port. The document can be found from <http://developer.intel.com/design/Xeon/guides/249679.htm>.

4.6.1 Debug Tools Specifications

4.6.1.1 Logic Analyzer Interface (LAI)

Intel is working with two logic analyzer vendors to provide logic analyzer interfaces (LAIs) for use in debugging the Celeron processor systems. Contact Tektronix, Inc.* and Agilent Technologies, Inc.* for specific information about their LAIs. The following information is general in nature. Specific information must be obtained from the logic analyzer vendor.

Due to the complexity of the Intel Celeron processor systems, the LAI is critical in providing the ability to probe and capture FSB signals. When designing a Intel Celeron processor system that may make use of an LAI, keep in mind mechanical and electrical considerations:

4.6.1.2 Mechanical Considerations

The LAI is installed between the processor socket and the Intel Celeron processor. The LAI pins plug into the socket, while the Intel Celeron processor plugs into a socket on the LAI. Cabling that is part of the LAI egresses the system to allow an electrical connection between the Intel Celeron processor and a logic analyzer. Contact the logic analyzer vendor to obtain the maximum volume occupied by the LAI, known as the keep-out volume, as well as the cable egress restrictions. System designers must verify that the keep-out volume remains unobstructed inside the system.

Note: It is possible that the keep-out volume reserved for the LAI may include space normally occupied by the Intel Celeron processor heat sink. When this is the case, the logic analyzer vendor provides a cooling solution as part of the LAI.

4.6.1.3 Electrical Considerations

The LAI also affects the electrical performance of the FSB; therefore, it is critical to obtain electrical load models for each of the logic analyzers to be able to run system level simulations to prove that they work in the system. Contact the logic analyzer vendor for electrical specifications and load models for the LAI solution they provide.

4.7 Intel® Celeron® Processor and Intel® 852GM Chipset FSB Signal Package Lengths

Table 15 lists the preliminary package trace lengths of the Celeron Processor and the Intel 82852GM GMCH for source synchronous data and address signals. All signals within the same group are routed to the same length as listed below with ± 100 mils (0.1 inch) accuracy. As a result of this package trace length matching, no PCB trace length compensation is needed for these signals. The Celeron Processor and Intel 82852GM GMCH package traces are routed as microstrip lines with a nominal characteristic impedance of $55 \Omega \pm 15\%$.

Table 15. Intel Celeron Processor and Intel® 852GM Chipset Package Lengths
(Sheet 1 of 4)

Processor lengths			GMCH Lengths		
Signal	Processor ball	Length (inches)	Signal	GMCH ball	Length (mils)
Address Group 0					
ADSTB[0]#	L5	0.210	HADSTB[0]#	T26	419
A[3]#	K2	0.368	HA[3]#	P23	468
A[4]#	K4	0.265	HA[4]#	T25	353
A[5]#	L6	0.155	HA[5]#	T28	551
A[6]#	K1	0.415	HA[6]#	R27	523
A[7]#	L3	0.304	HA[7]#	U23	274
A[8]#	M6	0.144	HA[8]#	U24	333
A[9]#	L2	0.372	HA[9]#	R24	327
A[10]#	M3	0.327	HA[10]#	U28	560
A[11]#	M4	0.246	HA[11]#	V28	566
A[12]#	N1	0.394	HA[12]#	U27	522
A[13]#	M1	0.408	HA[13]#	T27	501
A[14]#	N2	0.349	HA[14]#	V27	562
A[15]#	N4	0.241	HA[15]#	U25	375
A[16]#	N5	0.198	HA[16]#	V26	491
REQ[0]#	J1	0.427	HREQ[0]#	R28	569
REQ[1]#	K5	0.207	HREQ[1]#	P25	378
REQ[2]#	J4	0.270	HREQ[2]#	R23	247
REQ[3]#	J3	0.337	HREQ[3]#	R25	383
REQ[4]#	H3	0.356	HREQ[4]#	T23	276
Address Group 1					
ADSTB[1]#	R5	0.214	HADSTB[1]#	AA26	504
A[17]#	T1	0.470	HA[17]#	Y24	457
A[18]#	R2	0.404	HA[18]#	V25	389
A[19]#	P3	0.303	HA[19]#	V23	284

**Table 15. Intel Celeron Processor and Intel® 852GM Chipset Package Lengths
(Sheet 2 of 4)**

Processor lengths			GMCH Lengths		
Signal	Processor ball	Length (inches)	Signal	GMCH ball	Length (mils)
A[20]#	P4	0.246	HA[20]#	W25	414
A[21]#	R3	0.334	HA[21]#	Y25	429
A[22]#	T2	0.388	HA[22]#	AA27	545
A[23]#	U1	0.458	HA[23]#	W24	382
A[24]#	P6	0.156	HA[24]#	W23	353
A[25]#	U3	0.379	HA[25]#	W27	536
A[26]#	T4	0.281	HA[26]#	Y27	556
A[27]#	V2	0.417	HA[27]#	AA28	631
A[28]#	R6	0.166	HA[28]#	W28	579
A[29]#	W1	0.493	HA[29]#	AB27	558
A[30]#	T5	0.217	HA[30]#	Y26	484
A[31]#	U4	0.285	HA[31]#	AB28	617
Data Group 0					
DSTBN[0]#	E22	0.338	HDSTBN[0]#	J28	763
DSTBP[0]#	F21	0.326	HDSTBP[0]#	K27	662
D[0]#	B21	0.414	HD[0]#	K22	329
D[1]#	B22	0.475	HD[1]#	H27	620
D[2]#	A23	0.538	HD[2]#	K25	438
D[3]#	A25	0.608	HD[3]#	L24	387
D[4]#	C21	0.386	HD[4]#	J27	600
D[5]#	D22	0.386	HD[5]#	G28	693
D[6]#	B24	0.535	HD[6]#	L27	518
D[7]#	C23	0.464	HD[7]#	L23	329
D[8]#	C24	0.515	HD[8]#	L25	458
D[9]#	B25	0.590	HD[9]#	J24	438
D[10]#	G22	0.274	HD[10]#	H25	504
D[11]#	H21	0.203	HD[11]#	K23	319
D[12]#	C26	0.589	HD[12]#	G27	620
D[13]#	D23	0.462	HD[13]#	K26	494
D[14]#	J21	0.183	HD[14]#	J23	393
D[15]#	D25	0.550	HD[15]#	H26	554
DBI[0]#	E21	0.309	DINV[0]#	J25	514



**Table 15. Intel Celeron Processor and Intel® 852GM Chipset Package Lengths
(Sheet 3 of 4)**

Processor lengths			GMCH Lengths		
Signal	Processor ball	Length (inches)	Signal	GMCH ball	Length (mils)
Data Group 1					
DSTBN[1]#	K22	0.301	HDSTBN[1]#	C27	788
DSTBP[1]#	J23	0.306	HDSTBP[1]#	D26	736
D[16]#	H22	0.272	HD[16]#	F25	593
D[17]#	E24	0.480	HD[17]#	F26	634
D[18]#	G23	0.358	HD[18]#	B27	834
D[19]#	F23	0.418	HD[19]#	H23	412
D[20]#	F24	0.443	HD[20]#	E27	714
D[21]#	E25	0.508	HD[21]#	G25	522
D[22]#	F26	0.513	HD[22]#	F28	731
D[23]#	D26	0.597	HD[23]#	D27	766
D[24]#	L21	0.176	HD[24]#	G24	493
D[25]#	G26	0.524	HD[25]#	C28	837
D[26]#	H24	0.412	HD[26]#	B26	815
D[27]#	M21	0.171	HD[27]#	G22	453
D[28]#	L22	0.245	HD[28]#	C26	768
D[29]#	J24	0.401	HD[29]#	E26	691
D[30]#	K23	0.313	HD[30]#	G23	464
D[31]#	H25	0.473	HD[31]#	B28	914
DBI[1]#	G25	0.458	DINV[1]#	E25	628
Data Group 2					
DSTBN[2]#	K22	0.252	HDSTBN[2]#	E22	538
DSTBP[2]#	J23	0.266	HDSTBP[2]#	E21	502
D[32]#	M23	0.300	HD[32]#	B21	664
D[33]#	N22	0.226	HD[33]#	G21	501
D[34]#	P21	0.178	HD[34]#	C24	683
D[35]#	M24	0.371	HD[35]#	C23	675
D[36]#	N23	0.271	HD[36]#	D22	633
D[37]#	M26	0.454	HD[37]#	C25	747
D[38]#	N26	0.437	HD[38]#	E24	619
D[39]#	N25	0.383	HD[39]#	D24	655
D[40]#	R21	0.165	HD[40]#	G20	358
D[41]#	P24	0.343	HD[41]#	E23	608
D[42]#	R25	0.381	HD[42]#	B22	828

**Table 15. Intel Celeron Processor and Intel® 852GM Chipset Package Lengths
(Sheet 4 of 4)**

Processor lengths			GMCH Lengths		
Signal	Processor ball	Length (inches)	Signal	GMCH ball	Length (mils)
D[43]#	R24	0.329	HD[43]#	B23	726
D[44]#	T26	0.420	HD[44]#	F23	563
D[45]#	T25	0.380	HD[45]#	F21	460
D[46]#	T22	0.221	HD[46]#	C20	647
D[47]#	T23	0.279	HD[47]#	C21	654
DBI[2]#	P26	0.441	DINV[2]#	B25	784
Data Group 3					
DSTBN[3]#	W22	0.298	HDSTBN[3]#	D18	505
DSTBP[3]#	W23	0.300	HDSTBP[3]#	E18	463
D[48]#	U26	0.419	HD[48]#	G18	372
D[49]#	U24	0.324	HD[49]#	E19	511
D[50]#	U23	0.270	HD[50]#	E20	548
D[51]#	V25	0.384	HD[51]#	G17	326
D[52]#	U21	0.167	HD[52]#	D20	575
D[53]#	V22	0.252	HD[53]#	F19	469
D[54]#	V24	0.341	HD[54]#	C19	598
D[55]#	W26	0.447	HD[55]#	C17	541
D[56]#	Y26	0.454	HD[56]#	F17	372
D[57]#	W25	0.426	HD[57]#	B19	649
D[58]#	Y23	0.336	HD[58]#	G16	347
D[59]#	Y24	0.386	HD[59]#	E16	490
D[60]#	Y21	0.222	HD[60]#	C16	522
D[61]#	AA25	0.426	HD[61]#	E17	431
D[62]#	AA22	0.268	HD[62]#	D16	509
D[63]#	AA24	0.394	HD[63]#	C18	579
DBI[3]#	V21	0.202	DINV[3]#	G19	431

Mobile Intel® Celeron® Processor Front Side Bus Design Guidelines 5

The following layout guidelines support designs using the Mobile Intel® Celeron® Processor and the Intel® 852GM chipset. Due to on-die Rtt resistors on both the processor and the chipset, additional resistors do not need to be placed on the PCB for most FSB signals. The exception to these are RESET# and BPM[5:0]# signals, which require a 51 Ω pull-up, and the BR0# signal, which requires 220 $\Omega \pm 5\%$ pull-up to VCC_CPU on the processor end of the transmission line.

5.1 Processor Front Side Bus (FSB) Routing Guidelines

Table 16 presents and summarizes the layout recommendations for the Mobile Intel Celeron Processor and expands on specific design issues and their recommendations.

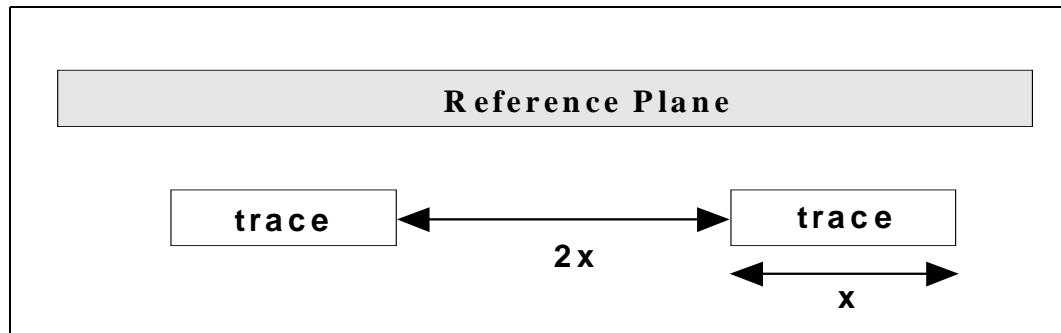
Table 16. FSB Routing Summary for the Processor (Sheet 1 of 2)

Parameter	Processor Routing Guidelines
Line-to-line spacing	Greater than or equal to 2:1 edge-to-edge spacing versus trace width for address and address strobes See Figure 20 for illustrations of this recommendation.
Data line lengths (agent-to-agent spacing)	0.5 inches-5.5 inches from pin-to-pin <ul style="list-style-type: none"> Data signals of the same source synchronous group to the same pad-to-pad length within ± 0.100 inches of the associated strobes. The pad is defined as the attach point of the silicon die to the package substrate. Length must be added to the system board to compensate for package length differences. Route signals in the same source synchronous group on the same layer and referenced to Vss with 2:1 spacing.
DSTBN/P[3:0]#	<ul style="list-style-type: none"> Route a data strobe and its complement within ± 0.025 inch of the same pad-to-pad length. The pad is defined as the attach point of the silicon die to the package substrate. Length must be added to the system board to compensate for package length differences. Route DSTBn/p# on the same layer as their associated data group and referenced to Vss.
NOTE: Refer to the Intel® 852GM Chipset GMCH Datasheet for GMCH package dimensions and refer to the Mobile Intel® Celeron Processor Datasheet for processor package dimensions.	

Table 16. FSB Routing Summary for the Processor (Sheet 2 of 2)

Parameter	Processor Routing Guidelines
Address line lengths (agent-to-agent spacing)	<p>0.5 inches - 6.5 inches pin-to-pin.</p> <ul style="list-style-type: none"> Address signals of the same source synchronous group should be routed to the same pad-to-pad length within ± 0.200 inch of the associated strobes. The pad is defined as the attach point of the silicon die to the package substrate. Length must be added to the system board to compensate for package length differences. A layer transition may occur if the reference plane remains the same (Vss) and the layers are of the same configuration (all stripline or all microstrip).
ADSTBN/P[1:0]#	<ul style="list-style-type: none"> Route an address strobe and its complement within ± 0.200 inch of the same pad-to-pad length. The pad is defined as the attach point of the silicon die to the package substrate. Length must be added to the system board to compensate for package length differences. A layer transition may occur if the reference plane remains the same (Vss) and the layers are all of the same configuration (all stripline or all microstrip).
Common clock line lengths	0.5 inches - 6.5 inches
Topology	Stripline
Routing priorities	<ul style="list-style-type: none"> Route all associated signals and strobes on the same layer for entire length of bus. Reference all signals to Vss. Ideally, layer changes should not occur for any signals. When a layer change must occur, the reference plane must be Vss and the layers must all be of the same configuration (all stripline or all microstrip for example).
Clock keepout zones	Maintain a spacing requirement of 16-20 mils around all clocks.
Trace Impedance	$55 \Omega \pm 15\%$
Source synchronous routing restrictions	<ul style="list-style-type: none"> There are no length-matching routing restrictions between (or within) either the source-synchronous data or address groups. As long as the strobe and associated line length routing guidelines are met for each group, there is no need to length-match between the groups. For example, one data group may be routed to the minimum allowable length while another data group could be routed to the maximum allowable length. Simulations have verified that the FSB functions correctly even under this extreme condition.
<p>NOTE: Refer to the <i>Intel® 852GM Chipset GMCH Datasheet</i> for GMCH package dimensions and refer to the <i>Mobile Intel® Celeron Processor Datasheet</i> for processor package dimensions.</p>	

Figure 20. Cross-Sectional View of 2:1 Ratio



A trace spacing to width ratio of 2 to 1 ensures a low crosstalk coefficient (based on geometries defined in 8 layer reference stackup). All the effects of crosstalk are difficult to simulate. The timing and layout guidelines for the processor have been created with the assumption of 2 to 1 trace spacing to width ratio. A smaller ratio would have an unpredictable impact due to crosstalk.

5.1.1 Return Path Evaluation

The return path is the route current takes to return to its source. It may take a path through ground planes, power planes, other signals, integrated circuits, vias, VRMs, etc. Think of the return path as following a path of least resistance back to the original source. Discontinuities in the return path often have signal integrity and timing effects that are similar to the discontinuities in the signal conductor. Therefore, the return paths must be given similar considerations. A way to evaluate return path parasitic inductance is to draw a loop that traces the current from the driver through the signal conductor to the receiver, then back through the ground/power plane to the driver again. The smaller the area of the loop, the lower the parasitic inductance.

The following sets of return path rules apply:

- Always trace out the return current path and provide as much care to the return path as the path of the signal conductor.
- Decoupling capacitors do not adequately compensate for a plane split.
- Do not allow splits in the reference planes in the path of the return current.
- Do not allow routing of signals on the reference planes near FSB signals.
- Maintain VSS as a reference plane for all FSB signals.
- Do not route over via anti-pads or socket anti-pads.

5.2 Processor Configuration

This section provides more details for routing Mobile Intel Celeron-based systems. This information is preliminary and subject to change. Both recommendations and considerations are presented.

For proper operation of the Mobile Intel Celeron and the Intel 852GM Chipset, it is necessary to meet the timing and voltage specifications of each component. The following recommendations are Intel's best guidelines based on extensive simulation and experimentation that make assumptions,

which may be different than an OEM's system design. The most accurate way to understand the signal integrity and timing of the FSB in your platform is by performing a comprehensive simulation analysis. It is conceivable that adjustments to trace impedance, line length, termination impedance, board stackup and other parameters may improve system performance.

Refer to the *Mobile Intel® Celeron Processor Datasheet* for a FSB signal list, signal types and definitions.

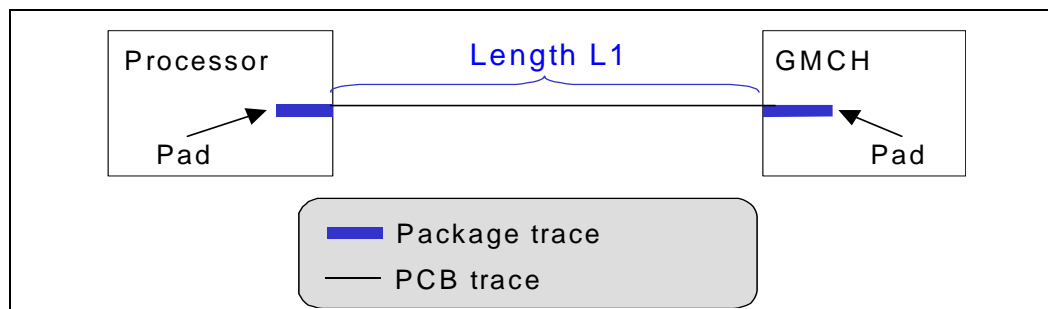
5.3 General Topology and Layout Guidelines

The following topology and layout guidelines are based on routing recommendations implemented on Intel Customer reference board. The guidelines are derived from empirical testing with Intel 852GM chipset package models. Below are the design recommendations for the data, address, strobes, and common clock signals. For the following discussion, the pad is defined as the attach point of the silicon die to the package substrate.

5.3.1 Source Synchronous (SS) Signal Group

Source synchronous groups and associated strobes should be routed on the same layer for the entire length of the bus. This results in a significant reduction of the flight time skew since the dielectric thickness, line width, and velocity of the signals will be uniform across a single layer of the stackup. There is no guarantee of a relationship of dielectric thickness, line width, and velocity between layers.

Figure 21. Processor Topology



5.3.1.1 Source Synchronous Data Group

Data signals of the same source synchronous group should be routed to the same pad-to-pad length within ± 0.100 of the associated strobes (within the min & max of both strobe). As a result, additional trace will be added to some data nets on the system board in order for all trace lengths within the same data group to be the same length (± 0.100 inches) from the pad of the processor to the associated pad of the chipset.

A data strobe and its complement should be routed to a length equal to their corresponding data group's mean pad-to-pad length ± 0.025 inches.

Equation 2. Calculation to Determine Package Delta Addition to PCB Length for UP Systems

$$\text{delta}_{\text{net,stroke}} = (\text{cpu_pkglen}_{\text{net}} - \text{cpu_pkglen}_{\text{stroke}}) + (\text{cs_pkglen}_{\text{net}} - \text{cs_pkglen}_{\text{stroke}})$$

* Strobe package length is the average of the strobe pair.

Refer to the *Intel® 852GM Chipset GMCH Datasheet* for GMCH package dimensions and refer to the *Mobile Intel® Celeron Processor Datasheet* for package dimensions.

Table 17. FSB Data Signal Routing Guidelines

Signal Names		Transmission Line Type	Total Trace Length		Nominal Impedance (Ω)	Width and Spacing (mils)
CPU	GMCH		Min. (inches)	Max. (inches)		
DBI[3:0]#	DINV[3:0]#	stripline	0.5	5.5	55 ± 15%	4 & 12
D[63:0]#	HD[63:0]#	stripline	0.5	5.5	55 ± 15%	4 & 12
DSTBN[3:0]#	HDSTBN[3:0]#	stripline	0.5	5.5	55 ± 15%	4 & 12
DSTBP[3:0]#	HDSTBP[3:0]#	stripline	0.5	5.5	55 ± 15%	4 & 12

NOTE: The data signals within each group must be routed to within ± 0.100 inch of its associated reference strobe. The complement strobe must be routed to within ± 0.025 inch of the associate reference strobe. All traces within each signal group must be routed on the same layer (required). Intel recommends that length of the strobes be centered to the average length of associated data or address traces to maximize setup/hold time margins.

5.3.1.2 Source Synchronous Address Group

Address signals follow the same rules as data signals except they should be routed to the same **pad-to-pad** length within ± 0.200 inch of the associated strobes. Address signals may change layers if the reference plane remains Vss.

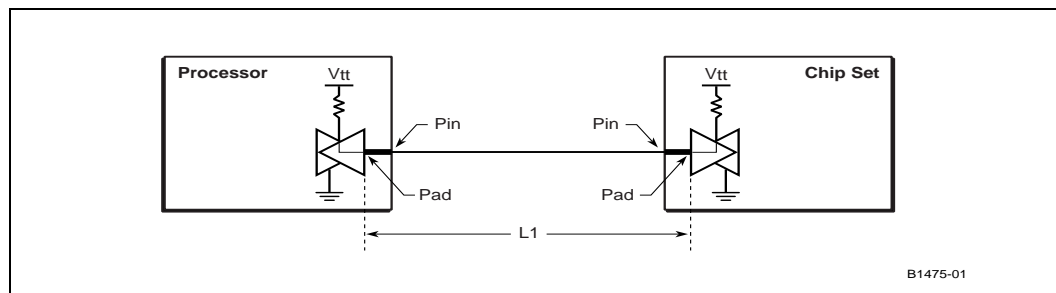
An Address strobe should be routed to a length equal to their corresponding signal group's mean **pad-to-pad** length ± 0.025 inch.

Table 18. Processor FSB Address Signal Routing Guidelines

Signal Names		Transmission Line Type	Total Trace Length		Nominal Impedance (Ω)	Width and Spacing (mils)
CPU	GMCH		Min. (inches)	Max. (inches)		
A[31:3]#	HA[31:3]#	Stripline	0.5	6.5	55 ± 15%	4 & 8
REQ[4:0]#	HREQ[4:0]#	Stripline	0.5	6.5	55 ± 15%	4 & 8
ADSTB[1:0]#	HADSTB[1:0]#	Stripline	0.5	6.5	55 ± 15%	4 & 8

NOTE: The address signals within each group must be routed to within ± 0.200 inch of its associated strobe. All traces within each signal group must be routed on the same layer (required). Intel recommends that length of the strobes be centered to the average length of associated data or address traces to maximize setup/hold time margins.

Figure 22. SS Topology for Address and Data



5.3.1.3 Strobe

Route a strobe and its complement to a length equal to their corresponding data group's mean **pad-to-pad** length ± 0.025 inch.

5.3.1.4 Common Clock

Route common clock signals to a minimum pin-to-pin PCB length of **2.0** inches and a maximum PCB length of **6.0** inches.

Route source synchronous groups and associated strobes on the same layer for the entire length of the bus. This results in a significant reduction of the flight time skew since the dielectric thickness, line width, and velocity of the signals will be uniform across a single layer of the stackup. A relationship of dielectric thickness, line width, and velocity between layers cannot be ensured.

Figure 21 shows the processor topology.

5.3.2 Front Side Bus Data and Address Routing Example

Figure 23, Figure 24, Figure 25, and Figure 26 provide examples of a board routing for the Data signal group. The majority of the Data signal route is on an internal layer; both external layers can be used for parallel termination R-pack placement.

Figure 23. FSB Data and Address Routing Example

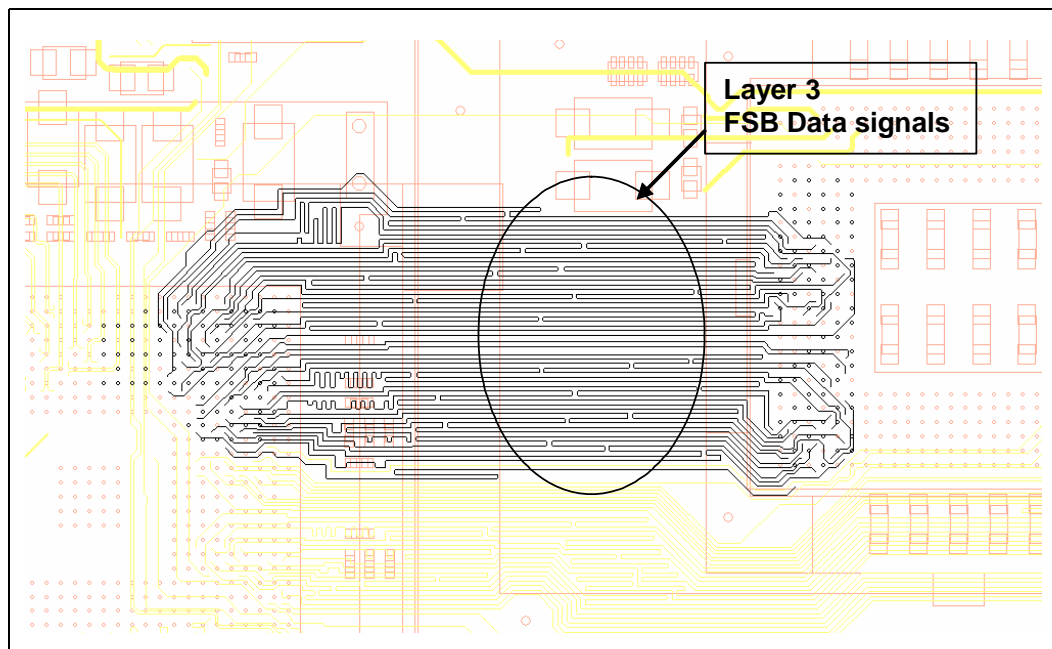


Figure 24. FSB Host Address Routing Example Layer 3

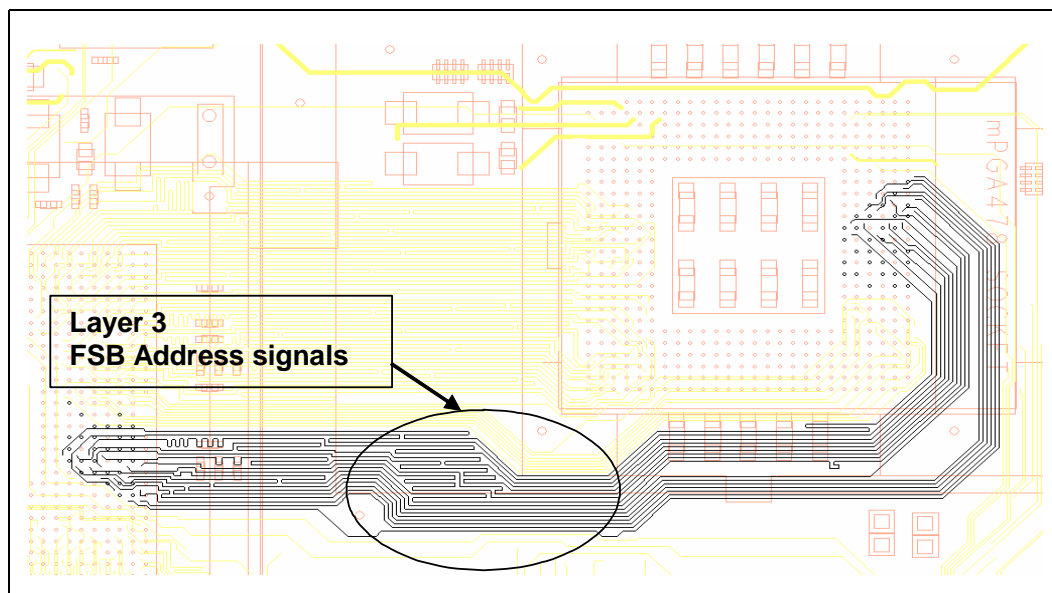


Figure 25. FSB Host Data Routing Example Layer 6

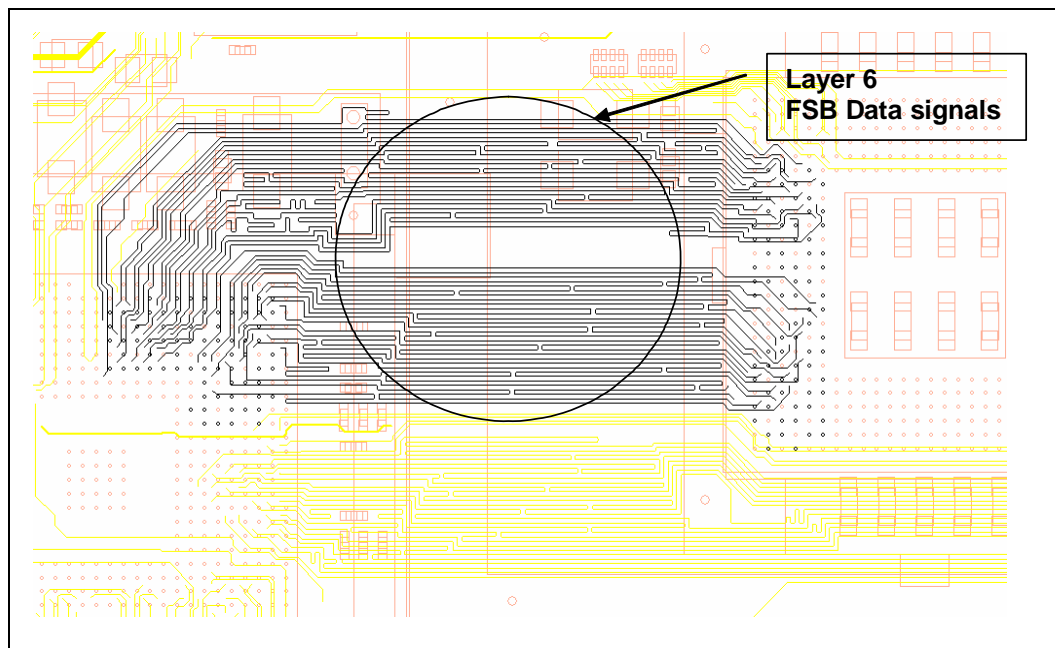
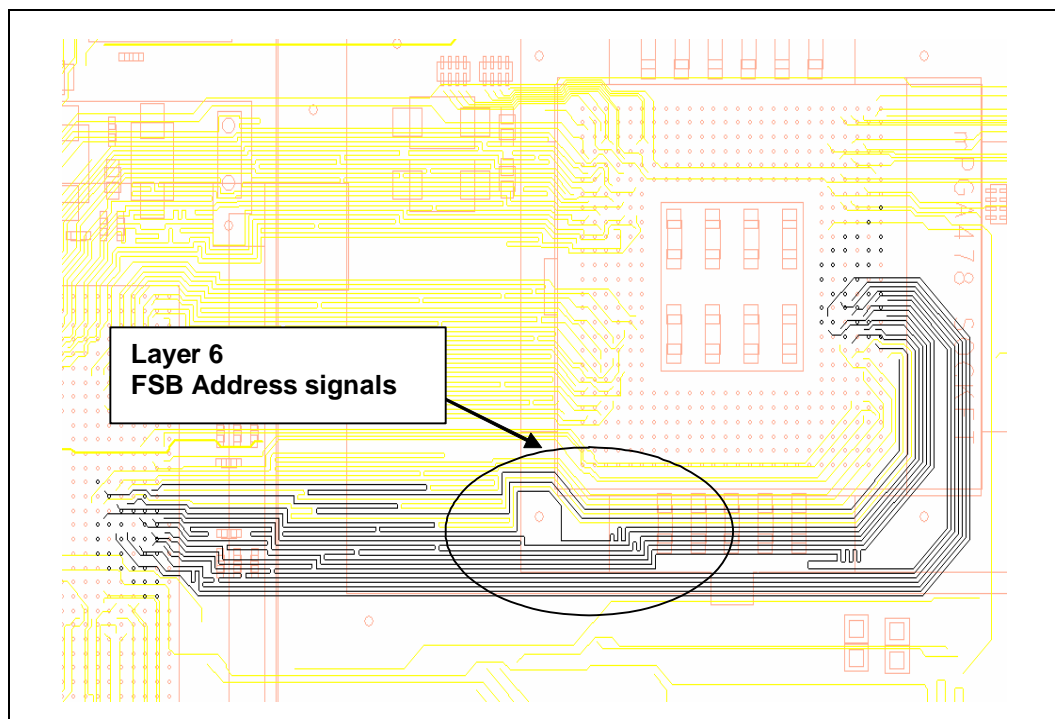


Figure 26. FSB Host Address Routing Example Layer 6



5.3.3 Common Clock (CC) AGTL+ Signal Group

Common clock signals should be routed to a minimum pin-to-pin PCB length of 0.5 inches and a maximum PCB length of 6.5 inches.

Table 19 presents the FSB control signal routing guidelines.

Table 19. FSB Control Signal Routing Guidelines

Signal Names		Topology	Routing Trace Length (Pin-to-Pin)		Nominal Impedance (Ω)	Width and spacing (mils)
CPU	GMCH		Min. (inches)	Max. (inches)		
RESET#	CPURST#	Stripline	0.5	6.5	55 \pm 15%	4 & 8
BR0#	BREQ0#	Stripline	0.5	6.5	55 \pm 15%	4 & 8
BNR#	BNR#	Stripline	0.5	6.5	55 \pm 15%	4 & 8
BPRI#	BPRI#	Stripline	0.5	6.5	55 \pm 15%	4 & 8
DEFER#	DEFER#	Stripline	0.5	6.5	55 \pm 15%	4 & 8
LOCK#	HLOCK#	Stripline	0.5	6.5	55 \pm 15%	4 & 8
TRDY#	HTRDY#	Stripline	0.5	6.5	55 \pm 15%	4 & 8
DRDY#	DRDY#	Stripline	0.5	6.5	55 \pm 15%	4 & 8
ADS#	ADS#	Stripline	0.5	6.5	55 \pm 15%	4 & 8
DBSY#	DBSY#	Stripline	0.5	6.5	55 \pm 15%	4 & 8
HIT#	HIT#	Stripline	0.5	6.5	55 \pm 15%	4 & 8
HITM#	HITM#	Stripline	0.5	6.5	55 \pm 15%	4 & 8
RS[2:0]#	RS[2:0]#	Stripline	0.5	6.5	55 \pm 15%	4 & 8

NOTE: Trace width of 4.0 mils and trace spacing of 8 mils within signal groups. The entire trace for each signal routed on one layer (recommended) RESET# and BR0# are CC AGTL+ signals without on-die termination (ODT). For these signals, place Rtt near CPU: L2 \leq 0.5 inch. Rtt = 51.1 Ω \pm 1%. Routing these signals to four inches \pm 0.5 inch should maximize the setup and hold margin parameters while adhering to expected solution design constraints.

5.3.4 Asynchronous AGTL+ and Other Signals

All signals must meet the AC and DC specifications as documented in the *Mobile Intel® Celeron Processor Datasheet*.

5.3.4.1 Topology 1A: Open Drain (OD) Signal Driven by the Processor—IERR# and FERR#

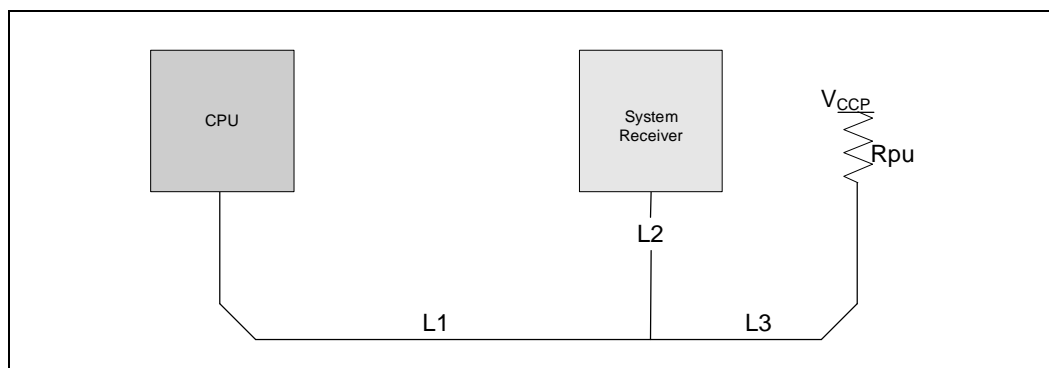
IERR# and FERR# should adhere to the routing and layout recommendations described and illustrated in Table 20 and Figure 27.

Due to the dependencies on system design implementation, IERR# may be implemented in a number of ways to meet design goals. IERR# may be routed as a test point or to any optional system receiver. Intel recommends that the FERR# signal of the Mobile Celeron Processor be routed to the FERR# signal of the Intel® 82801DB ICH4.

Table 20. Layout Recommendations for IERR# and FERR# Signal—Topology 1A

L1	L2	L3	Rpu	Transmission line Type
0.5" - 12.0"	0" - 3.0"	0" - 3.0"	$56 \Omega \pm 5\%$	Micro-strip
0.5" - 12.0"	0" - 3.0"	0" - 3.0"	$56 \Omega \pm 5\%$	Strip-line

Figure 27. Routing Illustration for FERR#



5.3.4.2 Topology 1B: Open Drain (OD) Signal Driven by the Processor—THERMTRIP#

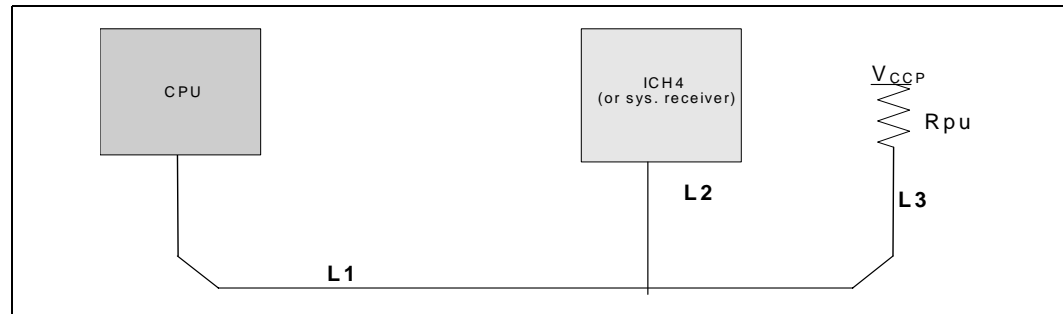
The Topology 1B OD signal THERMTRIP# should adhere to the following routing and layout recommendations. Table 21 lists the recommended routing requirements for the THERMTRIP# signals of the Mobile Intel Celeron Processor. The routing guidelines allow the signal to be routed as either micro-strip or strip-lines using $55 \Omega \pm 15\%$ characteristic trace impedance. The pull-up voltage for termination resistor R_{tt} is V_{CCP} .

THERMTRIP# can be implemented in a number of ways to meet design goals. It can be routed to the ICH4 or any optional system receiver. Intel recommends that the THERMTRIP# signal of the Mobile Intel Celeron Processor to be routed to the THERMTRIP# signal of the ICH4. The ICH4 THERMTRIP# signal is a new signal to the I/O controller hub architecture that allows the ICH4 to quickly put the whole system into an S5 state whenever the catastrophic thermal trip point has been reached.

Table 21. Layout Recommendations for THERMTRIP# Signal—Topology 1B

L1	L2	L3	Rpu	Transmission line Type
0.5" - 12.0"	0" - 3.0"	0" - 3.0"	$56 \Omega \pm 5\%$	Micro-strip
0.5" - 12.0"	0" - 3.0"	0" - 3.0"	$56 \Omega \pm 5\%$	Strip-line

Figure 28. Routing Illustration for THERMTRIP#



5.3.4.3 Topology 1C: Open Drain (OD) Signal Driven by the Processor—PROCHOT#

The Topology 1C OD signal PROCHOT#, should adhere to the following routing and layout recommendations. Table 22 lists the recommended routing requirements for the PROCHOT# signal. The routing guidelines allow the signal to be routed as either a micro-strip or strip-line using $55\Omega \pm 15\%$ characteristic trace impedance. Figure 29 shows the recommended implementation for providing voltage translation between the processor's PROCHOT# signal and a system receiver that utilizes a 3.3-V interface voltage (shown as V_{CCP}).

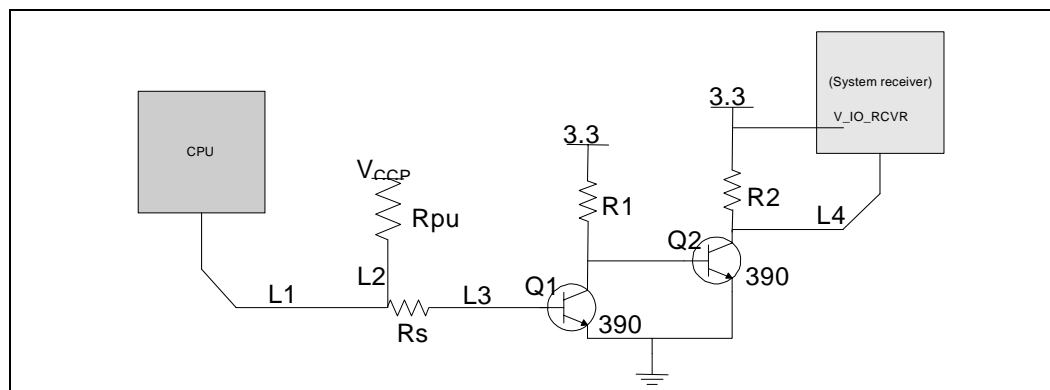
Series resistor R_s is a component of the voltage translation logic and serves as a driver isolation resistor. R_s is shown separated by distance L_3 from the first bipolar junction transistor (BJT), Q1, to emphasize the placement of R_s with respect to Q1. The placement of R_s a distance L_3 before the Q1 BJT is a specific implementation of the generalized voltage translator circuit shown in Figure 29. R_s should be placed at the beginning of the T-split from the PROCHOT# signal. The pull-up voltage for termination resistor R_{tt} is V_{CCP} .

Intel recommends that PROCHOT# be routed using the voltage translation logic shown in Figure 29.

Table 22. Layout Recommendations for PROCHOT# Signal—Topology 1C

L1	L2	L3	L4	R_s	R1	R2	R_{pu}	Transmission line Type
0.5"-12.0"	0"-3.0"	0"-3.0"	0.5"-12.0"	$330\Omega \pm 5\%$	$1.3\text{ k}\Omega \pm 5\%$	$330\Omega \pm 5\%$	$56\Omega \pm 5\%$	Micro-strip
0.5"-12.0"	0"-3.0"	0"-3.0"	0.5"-12.0"	$330\Omega \pm 5\%$	$1.3\text{ k}\Omega \pm 5\%$	$330\Omega \pm 5\%$	$56\Omega \pm 5\%$	Strip-Line

Figure 29. Routing Illustration for PROCHOT#



5.3.4.4 Topology 2A: Open Drain (OD) Source Driven by the Intel® 82801DB ICH4—PWRGOOD

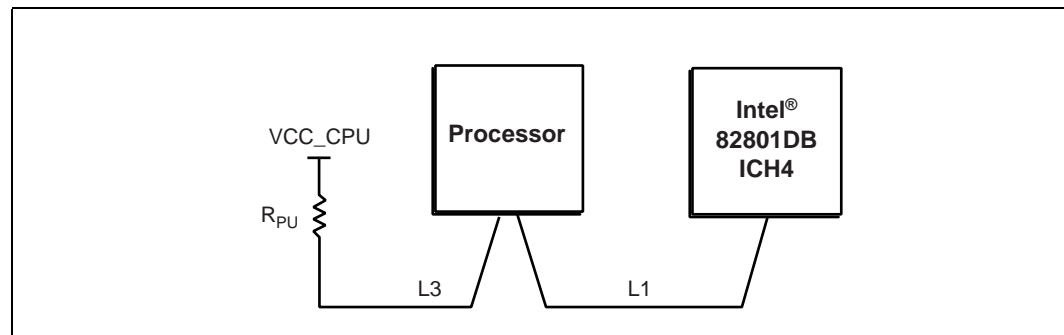
The Topology 2A OD signal PWRGOOD should adhere to the following routing and layout recommendations.

Figure 23 lists the recommended routing requirements for the PWRGOOD signal of the Mobile Intel Celeron Processor. The routing guidelines allow the signal to be routed as either micro-strip or strip-lines using $55\Omega \pm 15\%$ characteristic trace impedance. The pull-up voltage for termination resistor R_{tt} is V_{CCP} . Note that the Intel ICH4 CPUPWRGD signal should be routed point-to-point to the Mobile Intel Celeron Processor's PWRGOOD signal. The routing from the Mobile Intel Celeron Processor's PWRGOOD pin should fork out to both to the termination resistor, R_{tt} , and the ICH4. Segments L1 and L2 from Figure 13 should not T-split from a trace from the Mobile Intel Celeron Processor pin.

Table 23. Layout Recommendations for Miscellaneous Signals—Topology 2A

L1	L2	Rpu	Transmission Line Type
0.5" - 12.0"	0" - 3.0"	$300\Omega \pm 5\%$	Micro-strip
0.5" - 12.0"	0" - 3.0"	$300\Omega \pm 5\%$	Strip-line

Figure 30. Routing Illustration for PWRGOOD



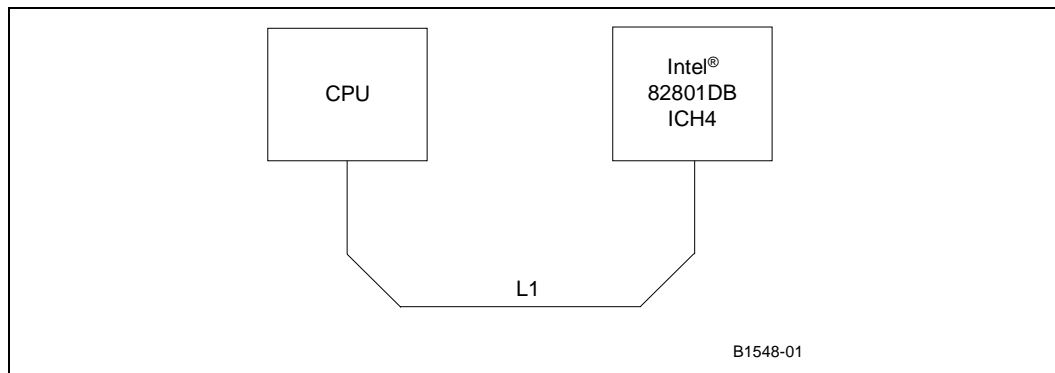
5.3.4.5 Topology 2B: CMOS Signals Driven by the Intel® 82801DB ICH4—A20M#, IGNNE#, LINT[1:0], SLP#, SMI#, and STPCLK#

The Topology 2A CMOS A20M#, IGNNE#, LINT0/INTR, LINT1/NMI, SLP#, SMI#, and STPCLK# signals should implement a point-to-point connection between the ICH4 and the Mobile Intel Celeron processor. The routing guidelines allow both signals to be routed as either microstrip or strip lines using $55 \Omega \pm 15\%$ characteristic trace impedance. No additional PCB components are necessary for this topology. See [Table 24](#) and [Figure 31](#) for more information.

Table 24. Layout Recommendations for Topology 2B

L1	Transmission Line Type
0.5" - 12.0"	Microstrip
0.5" - 12.0"	Stripline

Figure 31. Routing Illustration Topology 2BA



5.3.4.6 Topology 2C: CMOS Signal Driven by the Intel® 82801DB ICH4 to CPU and FWH—INIT#

The signal INIT# should adhere to the following routing and layout recommendations.

Table 25 lists the recommended routing requirements for the INIT# signal of the ICH4. The routing guidelines allow both signals to be routed as either micro-strip or strip-lines using $55\Omega \pm 15\%$ characteristic trace impedance.

Figure 32 shows the recommended implementation for providing voltage translation between the ICH4's INIT# voltage signaling level and any firmware hub (FWH) that utilizes a 3.3-V interface voltage (shown as a supply 3.3 V). For convenience, the entire topology and required transistors and resistors for the voltage translator is shown in Figure 32.

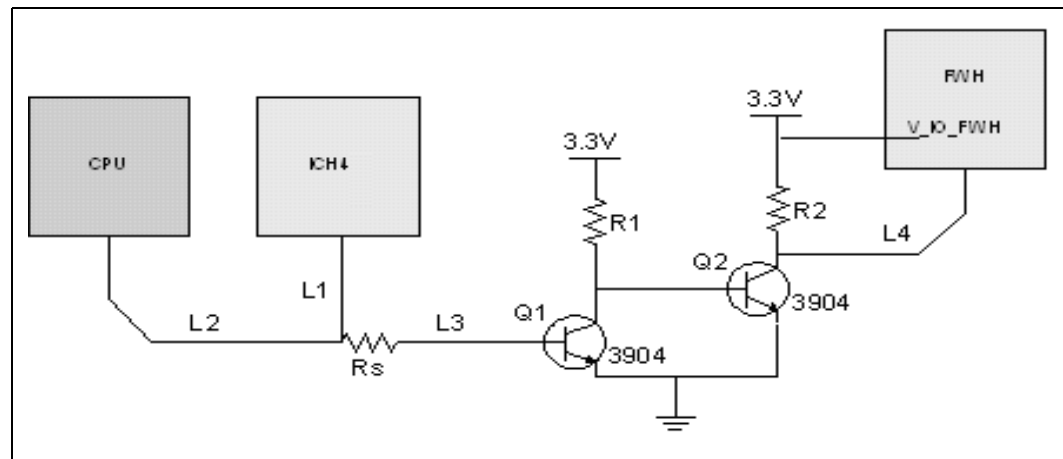
Series resistor R_s is a component of the voltage translator logic circuit and serves as a driver isolation resistor. R_s is shown separated by distance L_3 from the first bipolar junction transistor (BJT), Q1, to emphasize the placement of R_s with respect to Q1. The routing recommendations of transmission line L_3 in Figure 32 is listed in Table 25.

The resistor, R_s , should be placed at the beginning of the T-split of the trace from the ICH4's INIT# pin.

Table 25. Layout Recommendations for INIT#—Topology 2C

L1 + L2	L2	L4	R_s	R1	R2	Transmission Line Type
0.5"-12.0"	0"-3.0"	0.5"-6.0"	$300\Omega \pm 5\%$	$2k\Omega \pm 5\%$	$300\Omega \pm 5\%$	Micro-strip
0.5"-12.0"	0"-3.0"	0.5"-6.0"	$300\Omega \pm 5\%$	$2k\Omega \pm 5\%$	$300\Omega \pm 5\%$	Strip-line

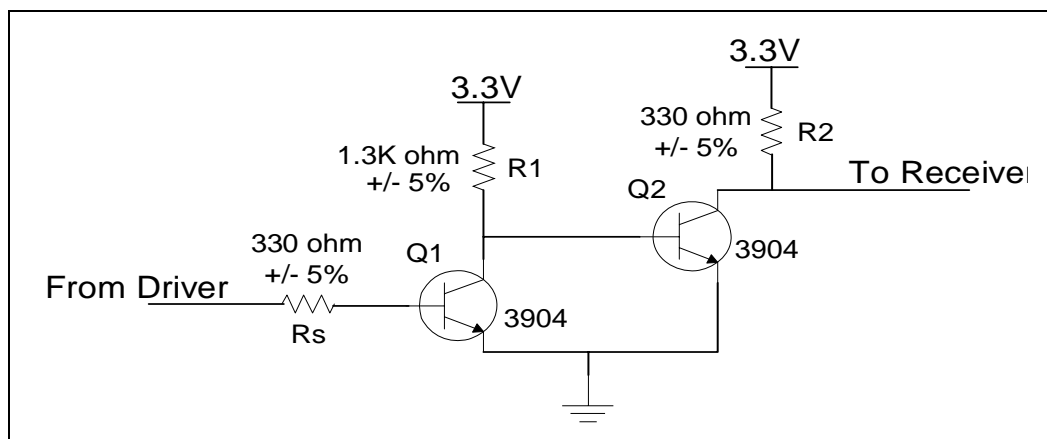
Figure 32. Routing Illustration for INIT#



Level shifting is required for the INIT# signal to the FWH to meet input logic levels of the FWH.

Figure 33 illustrates one method of level shifting.

Figure 33. Voltage Translation Circuit for 3.3-V Receivers



5.3.4.7 Topology 3: COMP[1:0] Signals

The Mobile Intel Celeron Processor has two COMP[1:0] pins, and the Intel 82852GM GMCH has two pins, HXRCOMP and HYRCOMP, that require compensation resistors to adjust the AGTL+IO buffer characteristics to specific board and operating environment characteristics. Also, the GMCH requires two special reference voltage generation circuits to pins HXSWING and HYSWING for the same purpose described above. Refer to the *Mobile Intel Celeron Processor Datasheet* and *Intel 852GM GMCH Chipset Datasheet* for details on resistive compensation.

For the Mobile Intel Celeron Processor, the COMP[1:0] pins must each be pulled down to ground with a $51 \Omega \pm 1\%$ resistors and should be connected to the Mobile Intel Celeron Processor with a $Z_o = 51 \Omega$ trace that is less than 0.5 inches from the processor pins. COMP[1:0] traces should be at least 25 mils (> 50 mils preferred) away from any other toggling signal.

5.3.4.8 Topology 4: THERMDA/THERMDC Routing Guidelines

The processor incorporates an on-die thermal diode. THERMDA (diode anode) and THERMDC (diode cathode) pins on the processor can be connected to a thermal sensor located on the system board to monitor the die temperature of the processor for thermal management/long-term die temperature change monitoring purpose. This thermal diode is separate from the thermal monitor's thermal sensor and cannot be used to predict the behavior of the thermal monitor.

Since the thermal diode is used to measure a very small voltage from the remote sensor, take care to minimize noise induced at the sensor inputs. The following are some guidelines:

- Place the remote sensor as close as possible to THERMDA/THERMDC pins. It may be approximately four to eight inches away as long as the worst noise sources such as clock generators, data buses, and address buses, etc., are avoided.
- Route the THERMDA and THERMDC lines in parallel and close together with ground guards enclosed.

Use wide tracks to reduce inductance and noise pickup that may be introduced by narrow ones. Intel recommends a width of 10 mils and spacing of 10 mils.

5.4 ITP Debug Port

Refer to the latest revision of the *ITP700 Debug Port Design Guide* for details on the implementation of the debug port. The document can be found from <http://developer.intel.com/design/Xeon/guides/249679.htm>.

5.4.1 Logic Analyzer Interface (LAI)

Intel is working with two logic analyzer vendors to provide logic analyzer interfaces (LAIs) for use in debugging the Mobile Intel Celeron based systems. Contact Tektronix, Inc.* and Agilent Technologies, Inc.* for specific information about their LAIs. The following information is general in nature. Specific information must be obtained from the logic analyzer vendor.

Due to the complexity of Mobile Intel Celeron Processor systems, the LAI is critical in providing the ability to probe and capture FSB signals. When designing a Mobile Intel Celeron system that may make use of an LAI, keep in mind mechanical and electrical considerations:

5.4.1.1 Mechanical Considerations

The LAI is installed between the processor socket and the Mobile Intel Celeron Processor. The LAI pins plug into the socket, while the Mobile Intel Celeron Processor plugs into a socket on the LAI. Cabling that is part of the LAI egresses the system to allow an electrical connection between the Mobile Intel Celeron Processor and a logic analyzer. The maximum volume occupied by the LAI, known as the keepout volume, as well as the cable egress restrictions, should be obtained from the logic analyzer vendor. It is possible that the keep-out volume reserved for the LAI may include space normally occupied by the Mobile Intel Celeron Processor heat sink. When this is the case, the logic analyzer vendor provides a cooling solution as part of the LAI.

5.4.1.2 Electrical Considerations

The LAI also affects the electrical performance of the FSB; therefore, it is critical to obtain electrical load models for each of the logic analyzers to be able to run system level simulations to prove that they work in the system. Contact the logic analyzer vendor for electrical specifications and load models for the LAI solution they provide.

5.5 Mobile Intel® Celeron® Processor and Intel® 852GM Chipset FSB Signal Package Lengths

Table 26 lists the preliminary package trace lengths of the Mobile Intel Celeron Processor and the Intel 852GM GMCH for source synchronous data and address signals. All signals within the same group are routed to the same length as listed below with ± 100 mils (0.1 inch) accuracy. As a result of this package trace length matching, no PCB trace length compensation is needed for these signals. The Mobile Intel Celeron Processor and Intel 852GM GMCH package traces are routed as microstrip lines with a nominal characteristic impedance of $55 \Omega \pm 15\%$.

Table 26. Mobile Intel Celeron Processor and Intel® 852GM Chipset Package Lengths (Sheet 1 of 4)

Processor lengths			GMCH Lengths		
Signal	Processor ball	Length (inches)	Signal	GMCH ball	Length (mils)
Address Group 0					
ADSTB[0]#	L5	0.210	HADSTB[0]#	T26	419
A[3]#	K2	0.368	HA[3]#	P23	468
A[4]#	K4	0.265	HA[4]#	T25	353
A[5]#	L6	0.155	HA[5]#	T28	551
A[6]#	K1	0.415	HA[6]#	R27	523
A[7]#	L3	0.304	HA[7]#	U23	274
A[8]#	M6	0.144	HA[8]#	U24	333
A[9]#	L2	0.372	HA[9]#	R24	327
A[10]#	M3	0.327	HA[10]#	U28	560
A[11]#	M4	0.246	HA[11]#	V28	566
A[12]#	N1	0.394	HA[12]#	U27	522
A[13]#	M1	0.408	HA[13]#	T27	501
A[14]#	N2	0.349	HA[14]#	V27	562
A[15]#	N4	0.241	HA[15]#	U25	375
A[16]#	N5	0.198	HA[16]#	V26	491
REQ[0]#	J1	0.427	HREQ[0]#	R28	569
REQ[1]#	K5	0.207	HREQ[1]#	P25	378
REQ[2]#	J4	0.270	HREQ[2]#	R23	247
REQ[3]#	J3	0.337	HREQ[3]#	R25	383
REQ[4]#	H3	0.356	HREQ[4]#	T23	276
Address Group 1					
ADSTB[1]#	R5	0.214	HADSTB[1]#	AA26	504
A[17]#	T1	0.470	HA[17]#	Y24	457
A[18]#	R2	0.404	HA[18]#	V25	389
A[19]#	P3	0.303	HA[19]#	V23	284

**Table 26. Mobile Intel Celeron Processor and Intel® 852GM Chipset Package Lengths
(Sheet 2 of 4)**

Processor lengths			GMCH Lengths		
Signal	Processor ball	Length (inches)	Signal	GMCH ball	Length (mils)
A[20]#	P4	0.246	HA[20]#	W25	414
A[21]#	R3	0.334	HA[21]#	Y25	429
A[22]#	T2	0.388	HA[22]#	AA27	545
A[23]#	U1	0.458	HA[23]#	W24	382
A[24]#	P6	0.156	HA[24]#	W23	353
A[25]#	U3	0.379	HA[25]#	W27	536
A[26]#	T4	0.281	HA[26]#	Y27	556
A[27]#	V2	0.417	HA[27]#	AA28	631
A[28]#	R6	0.166	HA[28]#	W28	579
A[29]#	W1	0.493	HA[29]#	AB27	558
A[30]#	T5	0.217	HA[30]#	Y26	484
A[31]#	U4	0.285	HA[31]#	AB28	617
Data Group 0					
DSTBN[0]#	E22	0.338	HDSTBN[0]#	J28	763
DSTBP[0]#	F21	0.326	HDSTBP[0]#	K27	662
D[0]#	B21	0.414	HD[0]#	K22	329
D[1]#	B22	0.475	HD[1]#	H27	620
D[2]#	A23	0.538	HD[2]#	K25	438
D[3]#	A25	0.608	HD[3]#	L24	387
D[4]#	C21	0.386	HD[4]#	J27	600
D[5]#	D22	0.386	HD[5]#	G28	693
D[6]#	B24	0.535	HD[6]#	L27	518
D[7]#	C23	0.464	HD[7]#	L23	329
D[8]#	C24	0.515	HD[8]#	L25	458
D[9]#	B25	0.590	HD[9]#	J24	438
D[10]#	G22	0.274	HD[10]#	H25	504
D[11]#	H21	0.203	HD[11]#	K23	319
D[12]#	C26	0.589	HD[12]#	G27	620
D[13]#	D23	0.462	HD[13]#	K26	494
D[14]#	J21	0.183	HD[14]#	J23	393
D[15]#	D25	0.550	HD[15]#	H26	554
DBI[0]#	E21	0.309	DINV[0]#	J25	514

**Table 26. Mobile Intel Celeron Processor and Intel® 852GM Chipset Package Lengths
(Sheet 3 of 4)**

Processor lengths			GMCH Lengths		
Signal	Processor ball	Length (inches)	Signal	GMCH ball	Length (mils)
Data Group 1					
DSTBN[1]#	K22	0.301	HDSTBN[1]#	C27	788
DSTBP[1]#	J23	0.306	HDSTBP[1]#	D26	736
D[16]#	H22	0.272	HD[16]#	F25	593
D[17]#	E24	0.480	HD[17]#	F26	634
D[18]#	G23	0.358	HD[18]#	B27	834
D[19]#	F23	0.418	HD[19]#	H23	412
D[20]#	F24	0.443	HD[20]#	E27	714
D[21]#	E25	0.508	HD[21]#	G25	522
D[22]#	F26	0.513	HD[22]#	F28	731
D[23]#	D26	0.597	HD[23]#	D27	766
D[24]#	L21	0.176	HD[24]#	G24	493
D[25]#	G26	0.524	HD[25]#	C28	837
D[26]#	H24	0.412	HD[26]#	B26	815
D[27]#	M21	0.171	HD[27]#	G22	453
D[28]#	L22	0.245	HD[28]#	C26	768
D[29]#	J24	0.401	HD[29]#	E26	691
D[30]#	K23	0.313	HD[30]#	G23	464
D[31]#	H25	0.473	HD[31]#	B28	914
DBI[1]#	G25	0.458	DINV[1]#	E25	628
Data Group 2					
DSTBN[2]#	K22	0.252	HDSTBN[2]#	E22	538
DSTBP[2]#	J23	0.266	HDSTBP[2]#	E21	502
D[32]#	M23	0.300	HD[32]#	B21	664
D[33]#	N22	0.226	HD[33]#	G21	501
D[34]#	P21	0.178	HD[34]#	C24	683
D[35]#	M24	0.371	HD[35]#	C23	675
D[36]#	N23	0.271	HD[36]#	D22	633
D[37]#	M26	0.454	HD[37]#	C25	747
D[38]#	N26	0.437	HD[38]#	E24	619
D[39]#	N25	0.383	HD[39]#	D24	655
D[40]#	R21	0.165	HD[40]#	G20	358
D[41]#	P24	0.343	HD[41]#	E23	608
D[42]#	R25	0.381	HD[42]#	B22	828

**Table 26. Mobile Intel Celeron Processor and Intel® 852GM Chipset Package Lengths
(Sheet 4 of 4)**

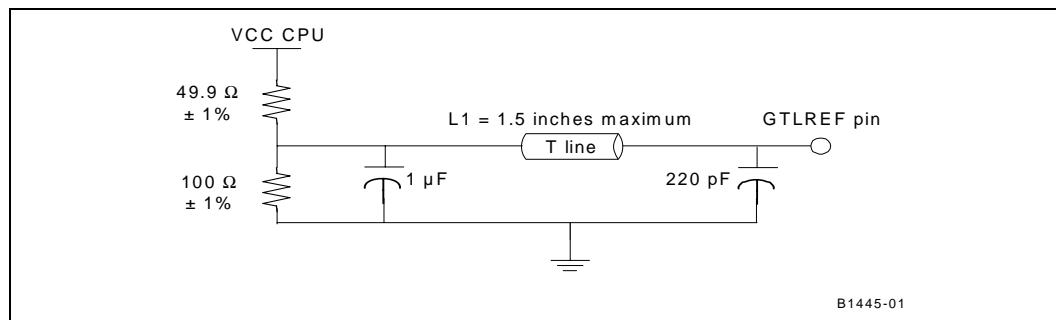
Processor lengths			GMCH Lengths		
Signal	Processor ball	Length (inches)	Signal	GMCH ball	Length (mils)
D[43]#	R24	0.329	HD[43]#	B23	726
D[44]#	T26	0.420	HD[44]#	F23	563
D[45]#	T25	0.380	HD[45]#	F21	460
D[46]#	T22	0.221	HD[46]#	C20	647
D[47]#	T23	0.279	HD[47]#	C21	654
DBI[2]#	P26	0.441	DINV[2]#	B25	784
Data Group 3					
DSTBN[3]#	W22	0.298	HDSTBN[3]#	D18	505
DSTBP[3]#	W23	0.300	HDSTBP[3]#	E18	463
D[48]#	U26	0.419	HD[48]#	G18	372
D[49]#	U24	0.324	HD[49]#	E19	511
D[50]#	U23	0.270	HD[50]#	E20	548
D[51]#	V25	0.384	HD[51]#	G17	326
D[52]#	U21	0.167	HD[52]#	D20	575
D[53]#	V22	0.252	HD[53]#	F19	469
D[54]#	V24	0.341	HD[54]#	C19	598
D[55]#	W26	0.447	HD[55]#	C17	541
D[56]#	Y26	0.454	HD[56]#	F17	372
D[57]#	W25	0.426	HD[57]#	B19	649
D[58]#	Y23	0.336	HD[58]#	G16	347
D[59]#	Y24	0.386	HD[59]#	E16	490
D[60]#	Y21	0.222	HD[60]#	C16	522
D[61]#	AA25	0.426	HD[61]#	E17	431
D[62]#	AA22	0.268	HD[62]#	D16	509
D[63]#	AA24	0.394	HD[63]#	C18	579
DBI[3]#	V21	0.202	DINV[3]#	G19	431

5.5.1 GTLREF Layout and Routing Recommendations

There are four AGTL+ GTLREF pins on the processor that are used to set the reference voltage level for the AGTL+ signals (GTLREF). Because all of these pins are connected inside the processor package, the GTLREF voltage must be supplied to only one of the four pins. The other three pins may be left as no connects.

Figure 34 shows an example of GTLREF routing.

Figure 34. GTLREF Routing



- The processor must have one dedicated voltage divider.
- Decouple the voltage divider with a $1\ \mu\text{F}$ capacitor.
- Keep the voltage divider within 1.5 inches of the GTLREF pin.
- Decouple the pin with a high-frequency capacitor (such as a $220\ \text{pF}$ 603) as close to the pin as possible.
- Keep signal routing at least 10 mils separated from the GTLREF routes. Use at least a 7 mil trace for routing.
- Do not allow signal lines to use the GTLREF routing as part of their return path (that is, do not allow the GTLREF routing to create splits or discontinuities in the reference planes of the FSB signals).

Intel® Celeron® M Processor Front Side Bus Design Guidelines 6

The following layout guidelines support designs using the Intel® Celeron® M processor and the Intel® 852GM chipset Graphics Memory Controller Hub (82852GM). Due to on-die Rtt resistors on both the processor and the chipset, additional resistors do not need to be placed on the PCB for most FSB signals. A simple point-to-point interconnect topology is used in these cases.

6.1 Intel® Celeron® M Processor Front Side Bus Design Recommendations

For proper operation of the Celeron M processor and the GMCH FSB interface, it is necessary that the system designer meet the timing and voltage specification of each component. The following recommendations are Intel's best guidelines based on extensive simulation and experimentation that make assumptions that may differ from an OEM's system design. The most accurate way to understand the signal integrity and timing of the Celeron M FSB in your platform is by performing a comprehensive simulation analysis. It is possible that adjustments to trace impedance, line length, termination impedance, board stack-up, and other parameters may be made that improve system performance.

Refer to the latest *Intel® Celeron® M Processor Datasheet* for a FSB signal list, signal types, and definitions. The following sections provide design recommendations for data, address, and strobes. For the following discussion, the pad is defined as the attach point of the silicon die to the package substrate. The following topology and layout guidelines are subject to change. The guidelines are derived from empirical testing with GMCH package models.

6.1.1 Recommended Stack-up Routing and Spacing Assumptions

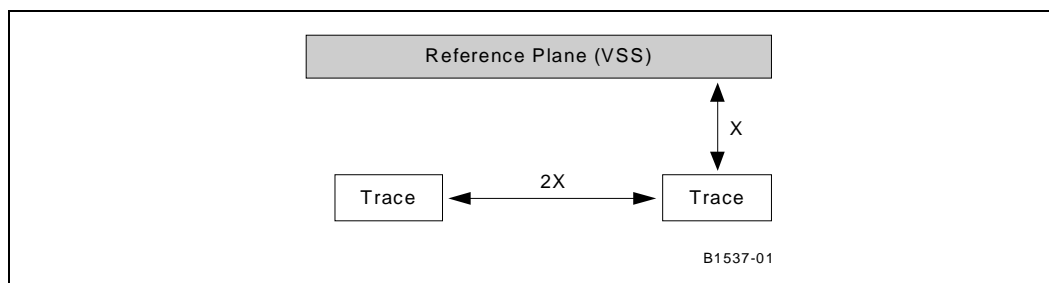
The following section describes in more detail the terminology and definitions used for different routing and stack-up assumptions that apply to Intel's recommended PCB stack-up described in [Section 3.1](#).

6.1.1.1 Trace to Trace Spacing – Reference Plane Separation Ratio

[Figure 35](#) illustrates Intel's recommended relationship between the edge-to-edge trace spacing (2X) versus the trace-to-reference plane separation (X). An edge-to-edge trace spacing (2X) to trace-reference plane separation (X) ratio of 2:1 ensures a low crosstalk coefficient. The timing and layout guidelines for the processor have been created with the assumption of a 2:1 trace spacing to reference plane ratio. A smaller ratio has an unpredictable impact due to crosstalk.

[Figure 35](#) illustrates the trace spacing versus trace-to-reference plane example.

Figure 35. Trace Spacing versus Trace-to-Reference Plane Example

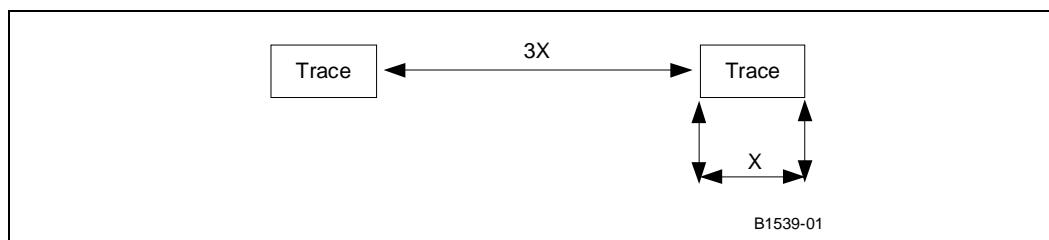


6.1.1.2 Trace Space to Trace Width Ratio

Figure 35 illustrates Intel's recommended relationship between the edge-to-edge trace spacing versus trace width for the best signal quality results. In general, a 3:1 trace space-to-trace width ratio (shown in Figure 36) is preferred. In case of routing difficulties on the PCB, using a 2:1 ratio would be acceptable **only** if additional simulations conclude that it is possible, which may include some changes to the stack-up or routing assumptions.

Figure 36 illustrates the three-to-one trace spacing-to-trace width example.

Figure 36. Three-to-One Trace Spacing-to-Trace Width Example



6.1.2 Common Clock Signals

All common clock signals use an AGTL+ bus driver technology with on-die integrated GTL termination resistors connected in a point-to-point, $Z_0 = 55 \Omega$, controlled impedance topology between the processor and the GMCH. No external termination is needed on these signals. These signals operate at the processor FSB frequency of 100 MHz.

Common clock signals should be routed on an internal layer while referencing solid ground planes. Based on current simulation results, routing on internal layers allows for a minimum pin-to-pin PCB length of one inch and a maximum of 6.5 inches. Trace length matching for the common clock signals is not required. For details on minimum PCB trace length requirements, refer to Section 6.1.2.1 and Table 27. Intel recommends routing these signals on the same internal layer for the entire length of the bus. If constraints require routing these signals with a transition to a different layer, a minimum of one ground stitching via for every two signals should be placed within 100 mils of the signal transition vias.

Routing of the common clock signals should use 2:1 trace spacing to trace width. This implies a minimum of 8 mils spacing (i.e., 12 mil minimum pitch) for a 4 mil trace width for routing on internal layers. Practical cases of escape routing under the GMCH or processor package outline and vicinity may not allow the implementation of 2:1 trace spacing requirements. Although every

attempt should be made to maximize the signal spacing in these areas, it is allowable to have 1:1 trace spacing underneath the GMCH and the Celeron M package outlines and up to 200 – 300 mils outside the package outline.

RESET# (CPURESET# of GMCH) is also a common clock signal but requires a special treatment for the case where an ITP700FLEX debug port is used. Refer to [Section 6.1.5](#) for further details.

[Table 27](#) presents the Celeron M processor FSB common clock signal internal layer routing guidelines.

Table 27. Celeron® M Processor FSB Common Clock Signal Internal Layer Routing Guidelines

Signal Names		Transmission Line Type	Total Trace Length		Nominal Impedance (Ω)	Spacing Width
CPU	GMCH		Min (mils)	Max (inches)		
ADS#	ADS#	Stripline	997	6.5	55 \pm 15%	2:1
BNR#	BNR#	Stripline	1298	6.5	55 \pm 15%	2:1
BPRI#	BPRI#	Stripline	1215	6.5	55 \pm 15%	2:1
BR0#	BR0#	Stripline	1411	6.5	55 \pm 15%	2:1
DBSY#	DBSY#	Stripline	1159	6.5	55 \pm 15%	2:1
DEFER#	DEFER#	Stripline	1291	6.5	55 \pm 15%	2:1
DPWR#	DPWR#	Stripline	1188	6.5	55 \pm 15%	2:1
DRDY#	DRDY#	Stripline	1336	6.5	55 \pm 15%	2:1
HIT#	HIT#	Stripline	1303	6.5	55 \pm 15%	2:1
HITM#	HITM#	Stripline	1203	6.5	55 \pm 15%	2:1
LOCK#	HLOCK#	Stripline	1198	6.5	55 \pm 15%	2:1
RS0#	RS0#	Stripline	1315	6.5	55 \pm 15%	2:1
RS1#	RS1#	Stripline	1193	6.5	55 \pm 15%	2:1
RS2#	RS2#	Stripline	1247	6.5	55 \pm 15%	2:1
TRDY#	HTRDY#	Stripline	1312	6.5	55 \pm 15%	2:1
RESET# [†]	CPURST#	Stripline	1101	6.5	55 \pm 15%	2:1

[†] For topologies where an ITP700FLEX debug port is implemented, refer to [Section 6.1.5](#) for RESET# (CPURESET#) implementation details.

6.1.2.1 Processor Common Clock Signal Package Length Compensation

Trace length matching for the common clock signals is not required. However, package compensation for the common clock signals is required for the minimum board trace. Refer to [Table 28](#) and the example for more details.

Package length compensation should not be confused with length matching. Length matching refers to constraints on the minimum and maximum length bounds of a signal group based on clock length, whereas package length compensation refers to the process of compensating for package length variance across a signal group.

All common clock signals are required to meet the minimum pad-to-pad requirement of 2212 mils based on ADS# (as this signal has the longest package lengths). This implies a minimum pin-to-pin PCB trace length of 997 mils additional PCB trace will be added to some of the shorter common clock nets on the system board. This trace length is added to meet the longest common clock signal total trace lengths from the die-pad of the processor to the associated die-pad of the chipset.

For example:

$ADS\# = 997 \text{ mils board trace} + 454 \text{ CPU PKG} + 761 \text{ GMCH PKG} = 2212 \text{ pad-to-pad length.}$

$BR0\# = X \text{ mils board trace} + 465 \text{ CPU PKG} + 336 \text{ GMCH PKG} = 2212 \text{ pad-to-pad length.}$

Therefore: $X = BR0\# \text{ board trace} = 2212 - 365 - 465 = 1411 \text{ pin-to-pin length.}$

[Figure 37](#) illustrates the common clock topology.

Figure 37. Common Clock Topology

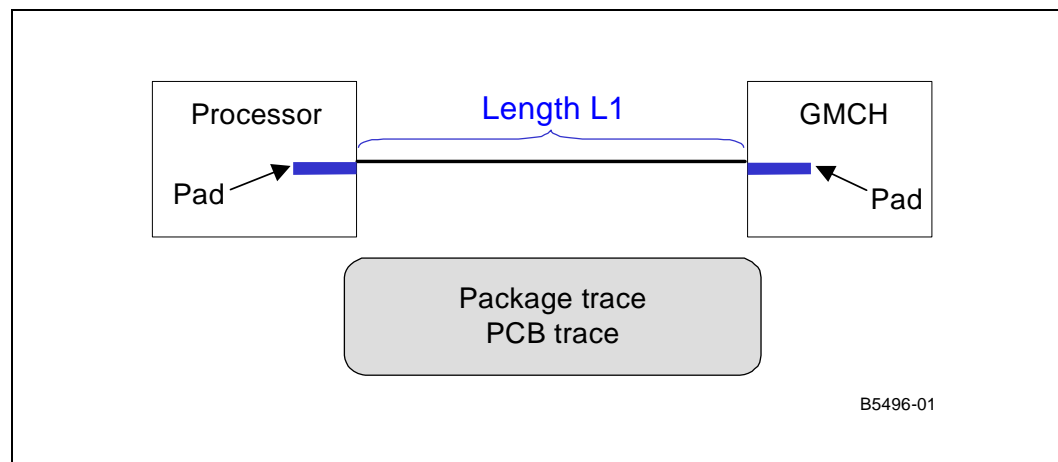


Table 28 presents the processor and GMCH FSB common clock signal length package lengths and minimum board trace lengths.

Table 28. Processor and GMCH FSB Common Clock Signal Package Lengths and Minimum Board Trace Lengths

Signal Names		Package Length		Total Pad-to-Pad Minimum Length Requirements L1 (mils)	Minimum Pin to Pin Routable Board Trace Length (mils)
CPU	GMCH	CPU	GMCH		
ADS#	ADS#	454	761	2212	997
BNR#	BNR#	506	408	2212	1298
BPRI#	BPRI#	424	573	2212	1215
BR0#	BR0#	336	465	2212	1411
DBSY#	DBSY#	445	608	2212	1159
DEFER#	DEFER#	349	572	2212	1291
DPWR#	DPWR#	506	518	2212	1188
DRDY#	DRDY#	529	347	2212	1336
HIT#	HIT#	420	489	2212	1303
HITM#	HITM#	368	641	2212	1203
LOCK#	HLOCK#	499	515	2212	1198
RS0#	RS0#	576	321	2212	1315
RS1#	RS1#	524	495	2212	1193
RS2#	RS2#	451	514	2212	1247
TRDY#	HTRDY#	389	511	2212	1312
RESET#	CPURESET#	455	656	2212	1101

6.1.3 Source Synchronous Signals General Routing Guidelines

All source synchronous signals use an AGTL+ bus driver technology with on-die GTL termination resistors connected in a point-to-point, $Z_0 = 55 \Omega$ controlled impedance topology between the Celeron M processor and the GMCH. No external termination is needed on these signals. The source synchronous Celeron M processor FSB address signals operate at a double-pumped rate of 200 MHz, while the source synchronous processor FSB data signals operate at a quad-pumped rate of 400 MHz. High-speed operation of the source synchronous signals requires careful attention to their routing considerations. Adhere to the following guidelines to ensure robust high-frequency operation of these signals.

Source synchronous data and address signals and their associated strobes are partitioned into groups of signals. Flight time skew minimization within the same group of source synchronous signals is a key parameter that allows their high-frequency (400 MHz) operation. All the source synchronous signals that belong to **the same group** should be routed on **the same internal layer** for the entire length of the bus. It is permissible to split different groups of source synchronous signals between different PCB layers as long as all the signals that belong to that group are kept on the same layer. Grouping of the Celeron M processor FSB source synchronous signals is summarized in Table 29 and Table 31. This practice results in a significant reduction of the flight

time skew because the dielectric thickness, line width, and velocity of the signals are uniform across a single layer of the stack-up. The relationship of dielectric thickness, line width, and velocity between layers cannot be ensured.

Source synchronous signals should be routed as a stripline on an internal layer with complete reference to ground planes both above and below the signal layer. Routing with references to split planes or power planes other than ground is **not** allowed. For Intel's stack-up example as shown in Figure 4, source synchronous Celeron M processor FSB signals are routed on Layer 3 and Layer 6. Layer 2 and Layer 7 are solid grounds across the entire PCB. However, this is not sufficient because significant coupling exists between signal Layer 3 and power plane Layer 4 as well as signal Layer 6 and power plane Layer 5. To ensure complete ground referencing, Layer 4 and Layer 5 are converted to ground plane floods in the areas where source synchronous processor FSB signals are routed. In addition, all ground plane areas are stitched with ground vias in the vicinity of the Celeron M processor and 852GM package outlines with the vias of the ground pins of the Celeron M processor and 852GM pin-map.

Figure 38 illustrates a PCB layout and a cross-sectional view of Intel's recommended stack-up of the Celeron M processor FSB source synchronous DATA and ADDRESS signals referencing ground planes on both Layer 7 and Layer 5.

Note: In the socket cavity of the Celeron M processor, Layer 5 and Layer 6 are used for V_{CC} core power delivery. However, outside the socket cavity, Layer 6 signals are routed on top of a solid Layer 7 ground plane. Layer 5 is converted to a ground flood under the shadow of the Celeron M processor FSB signals routing between the Celeron M processor and GMCH. Stitching of all the GND planes is provided by the ground vias in the pin map of the Celeron M processor and GMCH.

Figure 38. Layer 6 Intel® Celeron® M Processor FSB Source Synchronous Signals GND Referencing to Layer 5 and Layer 7 Ground Planes

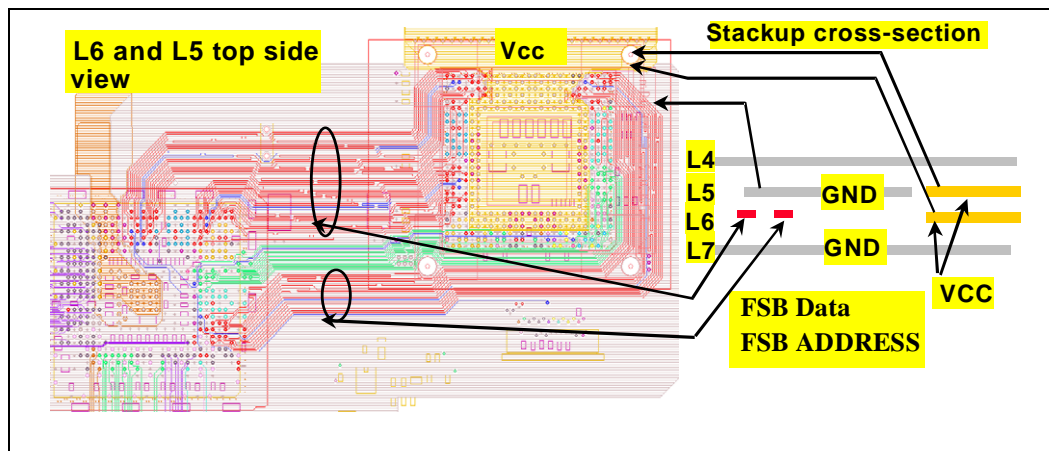


Figure 39 illustrates the Layer 6 Celeron M processor FSB source synchronous data signals.

Figure 39. Layer 6 Intel® Celeron® M Processor FSB Source Synchronous Data Signals

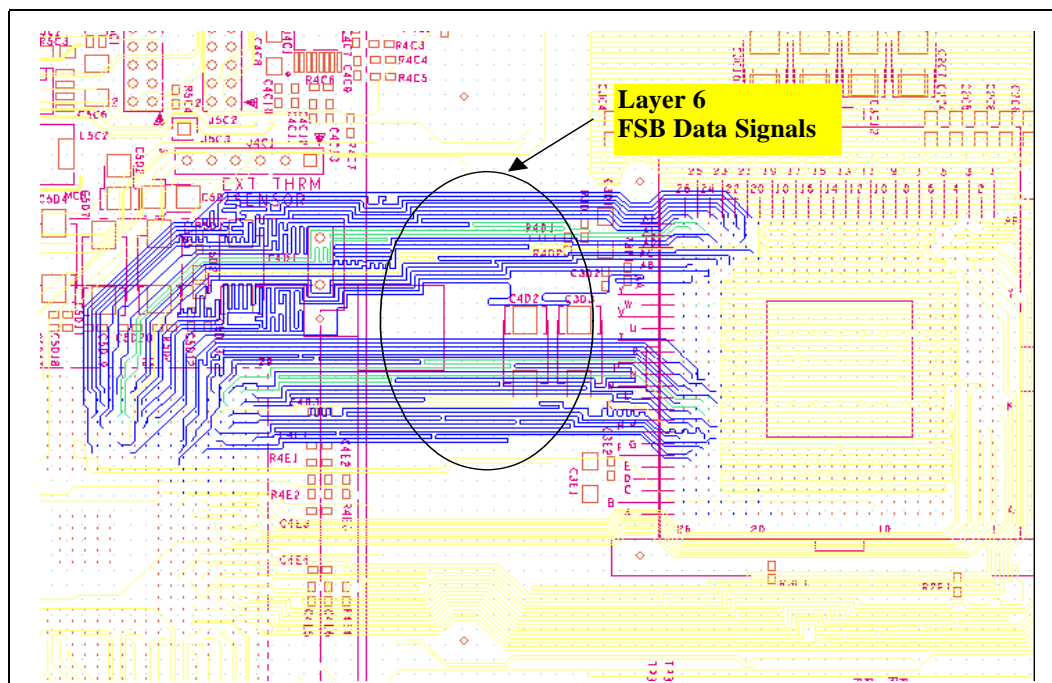
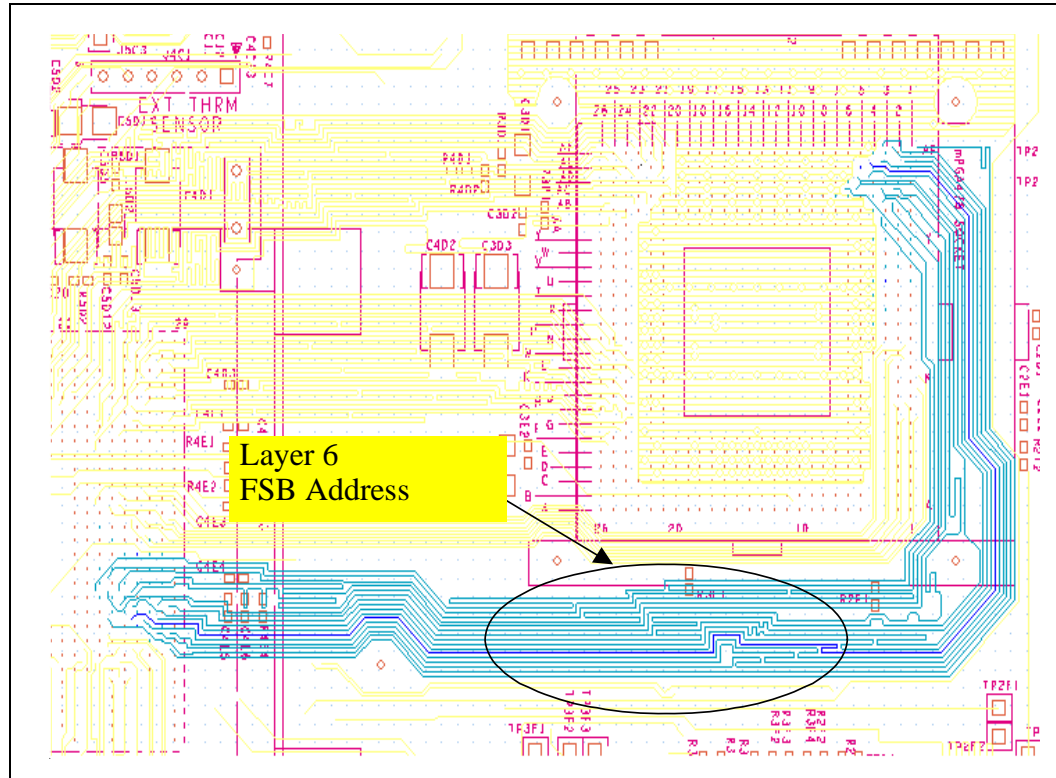


Figure 40. Layer 6 Intel® Celeron® M Processor FSB Source Synchronous Address Signals



Note: In the socket cavity of the Celeron M processor, Layer 3 is used for V_{CC} core power delivery to reduce the I*R drop. However, outside of the socket cavity Layer 3 signals are routed below a solid Layer 2 ground plane. Layer 4 is converted to a ground flood under the shadow of the Celeron M processor FSB signals routing between the Celeron M processor and GMCH. Figure 42 and Figure 43 show example routing for Intel customer reference board.

Figure 41 illustrates the Layer 3 Celeron M processor FSB source synchronous signals ground referencing to Layer 2 and Layer 4 ground planes.

Figure 41. Layer 3 Intel® Celeron® M Processor FSB Source Synchronous Signals GND Referencing to Layer 2 and Layer 4 Ground Planes

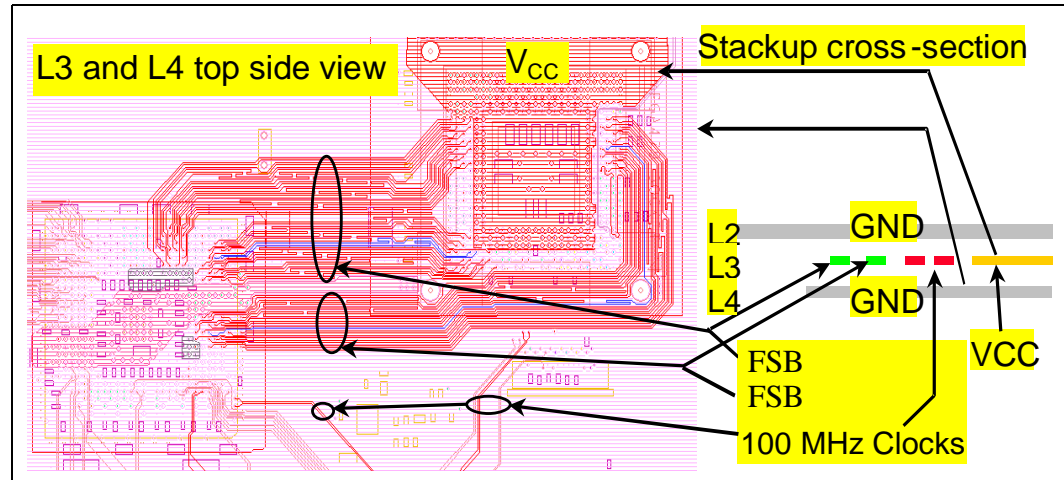


Figure 42 illustrates the Layer 3 Celeron M processor FSB source synchronous data signals.

Figure 42. Layer 3 Intel® Celeron® M Processor FSB Source Synchronous Data Signals

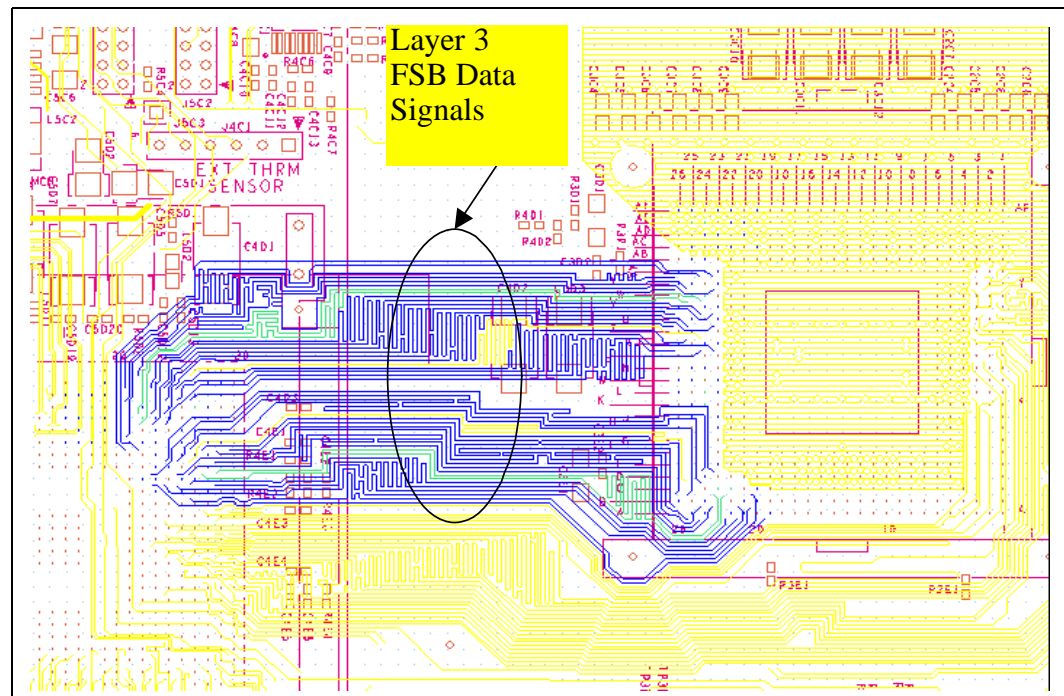
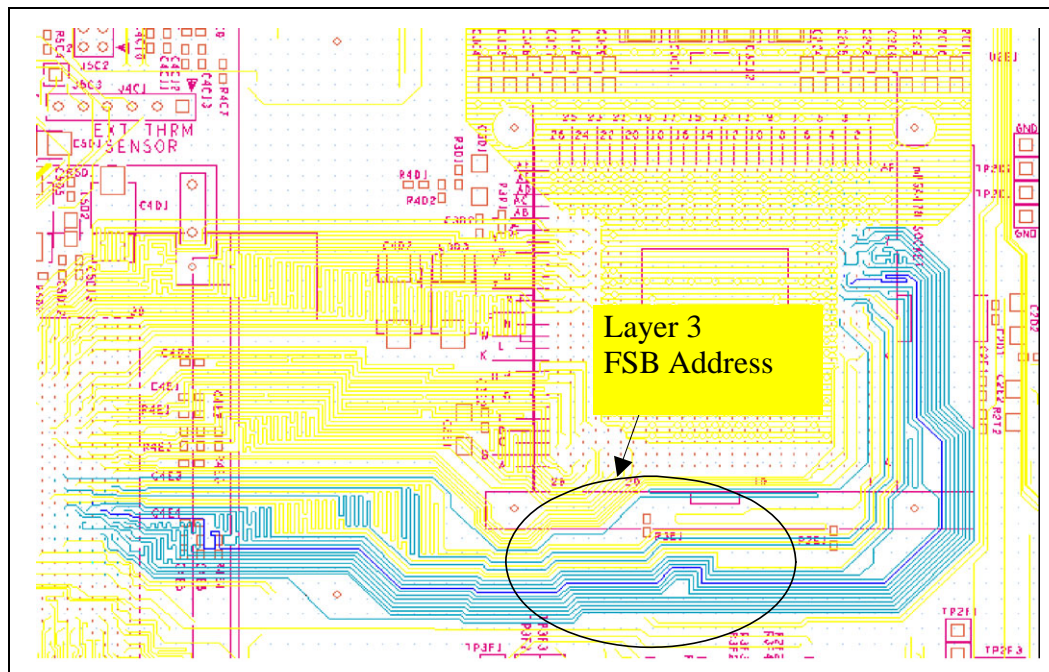


Figure 43 illustrates the Layer 3 Celeron M processor FSB source synchronous address signals.

Figure 43. Layer 3 Intel® Celeron® M Processor FSB Source Synchronous Address Signals



6.1.3.1 Source Synchronous Length-Matching Constraints

The routing guidelines presented in the following subsections define the recommended routing topologies, trace width and spacing geometries, and absolute minimum and maximum routed lengths for each signal group, all of which are recommended to achieve optimal SI and timing. In addition to the absolute length limits provided in the individual guideline tables are more restrictive length-matching requirements called length-matching constraints. These additional requirements further restrict the minimum-to-maximum length range of each signal group with respect to strobe, within the overall boundaries defined in the guideline tables, as required to guarantee adequate timing margins. The amount of minimum-to-maximum length variance allowed for each group around the strobe reference length varies from signal group to signal group depending on the amount of timing variation that may be tolerated.

6.1.3.2 Package Length Compensation

The Intel Celeron M processor package length does not need to be accounted for in the PCB routing since the Celeron M processor has the source synchronous signals and the strobes length matched within the group inside the package routing. However, trace length matching of the GMCH package length **does** need to be accounted for in the PCB routing because the package does not have the source synchronous signals and the strobes length matched within the group inside the package routing. Refer to Table 33 for the Celeron M processor and 852GM package lengths. Skew minimization requires 852GM die-pad to Celeron M processor pin (pad-to-pin) trace length matching of the FSB source synchronous signals belong to the same group including the strobe signals of that group.

Package length compensation should not be confused with length matching. Length matching refers to constraints on the minimum and maximum length bounds of a signal group based on clock length, whereas package length compensation refers to the process of adjusting package length variance across a signal group. There is some overlap in that both affect the target length of an individual signal. Intel recommends that the initial route be completed based on the length-matching formulas in conjunction with nominal package lengths and that package length compensation be performed as secondary operation.

6.1.3.3 Source Synchronous – Data Group

Robust operation of the 400 MHz, source synchronous data signals require tight skew control. For this reason, these signals are split into matched groups as outlined in [Table 29](#). All the signals within the same group should be kept on the same layer of PCB routing and should be routed to the same pad to pin length within ± 100 mils of the associated strobes. Only the Celeron M processor has the package trace equalization for signals within each data and address group. The GMCH does not have the package trace equalization for signals within each data and address group. See [Table 33](#) for the package lengths. Refer to [Section 6.1.2.1](#) for trace length and package compensation requirements. The two complementary strobe signals associated with each group should be length matched (pad-to-pin) to each other within ± 25 mils and tuned to the average length of the data signals (pad-to-pin) of their associated group. This will optimize setup/hold time margin.

Current simulation results provide routing guidelines using 3:1 spacing for the FSB source synchronous data and strobe signals. This implies a minimum of 12 mil spacing (i.e., 16 mil minimum pitch) for a four mil trace width. Practical cases of escape routing under the GMCH or the processor package outline and vicinity may not even allow the implementation of 2:1 trace spacing requirements. Although every attempt should be made to maximize the signal spacing in these areas, it is allowable to have 1:1 trace spacing underneath the GMCH and the processor package outlines and up to 200 – 300 mils outside the package outline. The benefits of additional spacing include increased signal quality and voltage margining. The trace routing and length-matching requirements are noted in [Section 6.1.3.1](#) to [Section 6.1.3.5](#).

Note: If trace impedance can be controlled to within ± 10 percent, the FSB data signals can then be routed using 2:1 spacing guidelines. The strobes, however, must still be routed with 3:1 spacing.

[Table 29](#) presents the Celeron M processor FSB data source synchronous signal trace length mismatch mapping.

Table 29. Intel® Celeron® M processor FSB Data Source Synchronous Signal Trace Length Mismatch Mapping

Data Group	DINV Signal for Associated Data Group	Signal Matching	Data Strobes Associated with the Group	Strobe Matching	Notes
D[15:0]#	DINV0#	± 100 mils	DSTBP0#, DSTBN0#	± 25 mils	1, 2
D[31:16]#	DINV1#	± 100 mils	DSTBP1#, DSTBN1#	± 25 mils	1, 2
D[47:32]#	DINV2#	± 100 mils	DSTBP2#, DSTBN2#	± 25 mils	1, 2
D[63:48]#	DINV3#	± 100 mils	DSTBP3#, DSTBN3#	± 25 mils	1, 2

NOTES:

1. Strobes of the same group should be trace length matched to each other within ± 25 mils and to the average length of their associated data signal group.
2. All length-matching formulas are based on GMCH die-pad to Celeron M processor pin total length per byte lane. Package length tables are provided for all signals to facilitate this pad-to-pin matching.

Table 30 lists the source synchronous data signal general routing requirements. Due to the 400 MHz high-frequency operation, the data signals should be limited to a pin-to-pin trace length minimum of 0.50 inch and maximum of 5.5 inches.

Table 30. Intel® Celeron® M Processor System Bus Source Synchronous Data Signal Routing Guidelines

Signal Names				Transmission Line Type	Total Trace Length		Nominal Impedance (Ω)	Spacing Width
Data Group #1	Data Group #2	Data Group #3	Data Group #4		Min (inches)	Max (inches)		
D[15:0]#	D[31:16]#	D[47:32]#	D[63:48]#	Stripline	0.5	5.5	55 \pm 15%	3:1
DINV0#	DINV1#	DINV2#	DINV3#	Stripline	0.5	5.5	55 \pm 15%	3:1
DSTBN[0]#	DSTBN[1]#	DSTBN[2]#	DSTBN[3]#	Stripline	0.5	5.5	55 \pm 15%	3:1
DSTBP[0]#	DSTBP[1]#	DSTBP[2]#	DSTBP[3]#	Stripline	0.5	5.5	55 \pm 15%	3:1
NOTES: 1. These data signals can be routed with 2:1 spacing if using 55 $\Omega \pm 15\%$ nominal impedance. However, spacing to associated strobes must still be kept at 3:1.								

6.1.3.4 Source Synchronous – Address Group

Source synchronous address signals operate at 200 MHz. Thus, their routing requirements are very similar to the data signals. Refer to [Section 6.1.3](#) and [Section 6.1.3.3](#) for further details. [Table 31](#) details the partition of the address signals into matched length groups. Due to the lower operating frequency of the address signals, pad-to-pin length matching is relaxed to ± 200 mils. Each group is associated with only one strobe signal. To maximize setup/hold time margin, the address strobes should be trace length matched to the average trace length of the address signals of their associated group. In addition, each address signal should be trace length matched within ± 200 mils of its associated strobe signal.

Table 31. Intel® Celeron® M Processor FSB Address Source Synchronous Signal Trace Length Mismatch Mapping

CPU Signal Name	Signal Matching	Strobe Associated with the Group	Strobe to Associated Address Signal Matching	Notes
REQ[4:0]#, A[16:3]#	± 200 mils	ADSTB0#	± 200 mils	1, 2, 3
A[31:17]#	± 200 mils	ADSTB1#	± 200 mils	1, 2, 3

NOTES:

- ADSTB[1:0]# should be trace length matched to the average length of their associated address signals group.
- Each address signal should be trace length matched to its associated address strobe within ± 200 mils.
- All length-matching formulas are based on GMCH die-pad to Celeron M processor pin total length per signal group. Package length tables are provided for all signals to facilitate this pad to pin matching.

[Table 32](#) lists the source synchronous address signal general routing requirements. They should be routed to a pin-to-pin length minimum of 0.50 inches and a maximum of 6.5 inches. Due to the 200 MHz high-frequency operation of the address signals, the routing guidelines listed in [Table 32](#) allow for 2:1 spacing for the address signals given a 55 $\Omega \pm 15\%$ characteristic trace impedance except for address strobe signals. But if space permits, 3:1 spacing is strongly advised for these signals.

Table 32. Intel® Celeron® M Processor FSB Source Synchronous Address Signal Routing Guidelines

Signal Names		Transmission Line Type	Total Trace Length		Nominal Impedance (Ω)	Width & Spacing
Address Group #1	Address Group #2		Min (inches)	Max (inches)		
A[16:3]#	A[31:17]#	Stripline	0.5	6.5	55 \pm 15%	4 & 8
REQ[4:0]#		Stripline	0.5	6.5	55 \pm 15%	4 & 8
ADSTB#[0]	ADSTB#[1]	Stripline	0.5	6.5	55 \pm 15%	4 & 12

6.1.3.5 Intel® Celeron® M Processor and Intel® 852GM Chipset GMCH (82852GM) FSB Signal Package Lengths

Table 33 presents package trace lengths of the Celeron M processor and the 82852GM for the source synchronous data and address signals. The Celeron M processor FSB package signals within the same group are routed to the same package trace length, but the 852GM chipset package signals within the same group are **not routed** to the same package trace length. As a result, package length compensation is required for GMCH. Refer [Section 6.1.3.2](#) for package length compensation. The Celeron M processor package traces are routed as microstrip lines with a nominal characteristic impedance of 55 $\Omega \pm 15\%$.

Table 33. Intel® Celeron® M Processor and GMCH Source Synchronous FSB Signal Package Lengths (Sheet 1 of 6)

Signal Group	CPU Signal Name	CPU package Trace Length (mils)	GMCH Signal Name	GMCH Package Trace Length (mils)
Data Group 1	D15#	721	HD15#	554
	D14#	721	HD14#	393
	D13#	721	HD13#	494
	D12#	721	HD12#	620
	D11#	721	HD11#	319
	D10#	721	HD10#	504
	D9#	721	HD9#	438
	D8#	721	HD8#	458
	D7#	721	HD7#	329
	D6#	721	HD6#	518
	D5#	721	HD5#	693
	D4#	721	HD4#	600
	D3#	721	HD3#	387
	D2#	721	HD2#	438
	D1#	721	HD1#	620
	D0#	721	HD0#	329
	DINV[0]#	721	DINV[0]#	514
	DSTBP[0]#	721	HDSTBP[0]#	662
	DSTBN[0]#	721	HDSTBN[0]#	763

**Table 33. Intel® Celeron® M Processor and GMCH Source Synchronous FSB
Signal Package Lengths (Sheet 2 of 6)**

Signal Group	CPU Signal Name	CPU package Trace Length (mils)	GMCH Signal Name	GMCH Package Trace Length (mils)
Data Group 2	D31#	564	HD31#	914
	D30#	564	HD30#	464
	D29#	564	HD29#	691
	D28#	564	HD28#	768
	D27#	564	HD27#	453
	D26#	564	HD26#	815
	D25#	564	HD25#	837
	D24#	564	HD24#	493
	D23#	564	HD23#	766
	D22#	564	HD22#	731
	D21#	564	HD21#	522
	D20#	564	HD20#	714
	D19#	564	HD19#	412
	D18#	564	HD18#	834
	D17#	564	HD17#	634
	D16#	564	HD16#	593
	DINV[1]#	564	DINV[1]#	628
	DSTBP[1]#	564	HDSTBP[1]#	736
	DSTBN[1]#	564	HDSTBN[1]#	787



**Table 33. Intel® Celeron® M Processor and GMCH Source Synchronous FSB
Signal Package Lengths (Sheet 3 of 6)**

Signal Group	CPU Signal Name	CPU package Trace Length (mils)	GMCH Signal Name	GMCH Package Trace Length (mils)
Data Group 3	D47#	661	HD47#	654
	D46#	661	HD46#	647
	D45#	661	HD45#	460
	D44#	661	HD44#	563
	D43#	661	HD43#	726
	D42#	661	HD42#	828
	D41#	661	HD41#	608
	D40#	661	HD40#	358
	D39#	661	HD39#	655
	D38#	661	HD38#	619
	D37#	661	HD37#	747
	D36#	661	HD36#	633
	D35#	661	HD35#	675
	D34#	661	HD34#	683
	D33#	661	HD33#	501
	D32#	661	HD32#	664
	DINV[2]#	661	DINV[2]#	784
	DSTBP[2]#	661	HDSTBP[2]#	502
	DSTBN[2]#	661	HDSTBN[2]#	538

**Table 33. Intel® Celeron® M Processor and GMCH Source Synchronous FSB
Signal Package Lengths (Sheet 4 of 6)**

Signal Group	CPU Signal Name	CPU package Trace Length (mils)	GMCH Signal Name	GMCH Package Trace Length (mils)
Data Group 4	D63#	758	HD63#	579
	D62#	758	HD62#	509
	D61#	758	HD61#	431
	D60#	758	HD60#	522
	D59#	758	HD59#	490
	D58#	758	HD58#	347
	D57#	758	HD57#	649
	D56#	758	HD56#	372
	D55#	758	HD55#	541
	D54#	758	HD54#	598
	D53#	758	HD53#	469
	D52#	758	HD52#	575
	D51#	758	HD51#	326
	D50#	758	HD50#	549
	D49#	758	HD49#	511
	D48#	758	HD48#	372
	DINV[3]#	758	DINV[3]#	431
	DSTBP[3]#	758	HDSTBP[3]#	463
	DSTBN[3]#	758	HDSTBN[3]#	505



**Table 33. Intel® Celeron® M Processor and GMCH Source Synchronous FSB
Signal Package Lengths (Sheet 5 of 6)**

Signal Group	CPU Signal Name	CPU package Trace Length (mils)	GMCH Signal Name	GMCH Package Trace Length (mils)
Address Group 1	REQ4#	616	HREQ4#	276
	REQ3#	616	HREQ3#	383
	REQ2#	616	HREQ2#	247
	REQ1#	616	HREQ1#	378
	REQ0#	616	HREQ0#	569
	A16#	616	HA16#	491
	A15#	616	HA15#	375
	A14#	616	HA14#	562
	A13#	616	HA13#	501
	A12#	616	HA12#	522
	A11#	616	HA11#	566
	A10#	616	HA10#	560
	A9#	616	HA9#	327
	A8#	616	HA8#	333
	A7#	616	HA7#	274
	A6#	616	HA6#	523
	A5#	616	HA5#	551
	A4#	616	HA4#	352
	A3#	616	HA3#	468
	ADSTB[0]#	616	HADSTB[0]#	419

**Table 33. Intel® Celeron® M Processor and GMCH Source Synchronous FSB
Signal Package Lengths (Sheet 6 of 6)**

Signal Group	CPU Signal Name	CPU package Trace Length (mils)	GMCH Signal Name	GMCH Package Trace Length (mils)
Address Group 2	A31#	773	HA31#	617
	A30#	773	HA30#	484
	A29#	773	HA29#	558
	A28#	773	HA28#	579
	A27#	773	HA27#	631
	A26#	773	HA26#	556
	A25#	773	HA25#	535
	A24#	773	HA24#	353
	A23#	773	HA23#	382
	A22#	773	HA22#	545
	A21#	773	HA21#	429
	A20#	773	HA20#	414
	A19#	773	HA19#	284
	A18#	773	HA18#	389
	A17#	773	HA17#	457
	ADSTB[1]#	773	HADSTB[1]#	504
Host Clocks	BCLK0	447	BCLK	1138
	BCLK1	447	BCLK#	1145

6.1.4 Asynchronous Signals

The following sections describe the topologies and layout recommendations for the Asynchronous Open Drain and CMOS signals found on the platform. All Open Drain signals listed in the following sections must be pulled up to V_{CCP} (1.05 V). If any of these Open Drain signals are pulled up to a voltage higher than V_{CCP} , the reliability and power consumption of the processor may be affected. Therefore, it is very important to follow the recommended pull-up voltage for these signals. All signals must meet the AC and DC specifications as documented in the *Intel® Celeron® M Processor Datasheet*.

Table 34 presents the asynchronous AGTL+ nets.

Table 34. Asynchronous AGTL+ Nets

Signal Names	Description	Topology #	CPU I/O Type	Output	Output Buffer Type	Input	Input Power Well
IERR#	Internal error	1A	O	CPU	AGTL+	System Receiver	Vcc_Receiver
FERR#	Floating point error	1B	O	CPU	AGTL+	Intel® 82801DB ICH4	Main I/O (3.3 V)
THRMTRIP#	Thermal sensor	1B	O	CPU	AGTL+	System Receiver	Vcc_Receiver
PROCHOT#	Thermal sensor	1C	O	CPU	AGTL+	System Receiver	Vcc_Receiver
PWRGOOD	System power good	2A	I	ICH4	OD CMOS	CPU	N/A
DPSLP#†	Deep sleep		I			CPU	
LINT0/INTR	Local interrupts	2B	I	ICH4	CMOS	CPU	N/A
LINT1/NMI	Local interrupts	2B	I	ICH4	CMOS	CPU	N/A
SLP#	Sleep	2B	I	ICH4	CMOS	CPU	N/A
STPCLK#	Processor stop clock	2B	I	ICH4	CMOS	CPU	N/A
IGNNE#	Ignore next numeric error	2B	I	ICH4	CMOS	CPU	N/A
SMI#	System management interrupt	2B	I	ICH4	CMOS	CPU	N/A
A20M#	Address 20 mask	2B	I	ICH4	CMOS	CPU	N/A
INIT#	Processor initialize	3	I	ICH4	CMOS	CPU, FWH	N/A, 3.3 V

† Only supported by ICH4M device. When not used, pull-up at CPU with 4.7 K Ω \pm 5% resistor at V_{CCP}

6.1.4.1 Topology 1A: Open Drain (OD) Signals Driven by the Celeron® M Processor – IERR#

The Topology 1A OD signal IERR# should adhere to the following routing and layout recommendations. Table 35 presents the layout recommendations for Topology 1A. The routing guidelines allow the signal to be routed as either microstrip or striplines using $55 \Omega \pm 15\%$ characteristic trace impedance. Series resistor R1 is a dampening resistor for reducing overshoot/undershoot reflections on the transmission line. The pull-up voltage for termination resistor Rtt is V_{CCP} (1.05 V). Due to the dependencies on system design implementation, IERR# may be implemented in a number of ways to meet design goals. IERR# may be routed as a test point or to any optional system receiver. Figure 44 illustrates the routing illustration for Topology 1A.

Figure 44. Routing Illustration for Topology 1A

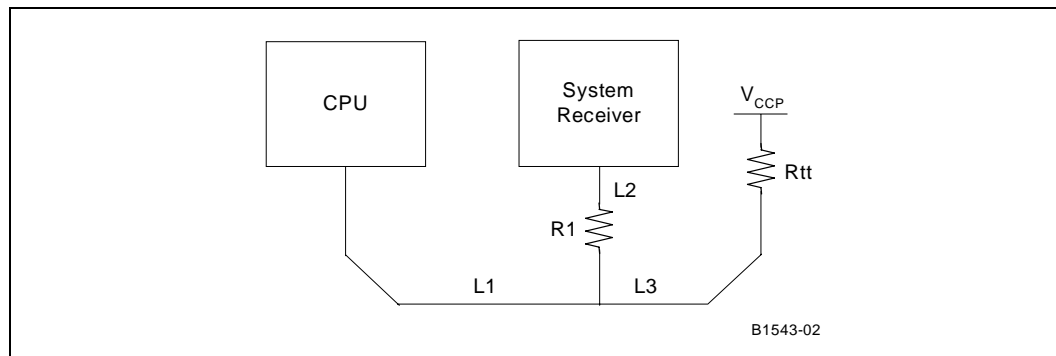


Table 35. Layout Recommendations for Topology 1A

L1	L2	L3	R1	Rtt	Transmission Line Type
0.5 – 12 inches	0 – 3 inches	0 – 3 inches	$56 \Omega \pm 5\%$	$56 \Omega \pm 5\%$	Microstrip
0.5 – 12 inches	0 – 3 inches	0 – 3 inches	$56 \Omega \pm 5\%$	$56 \Omega \pm 5\%$	Stripline

6.1.4.2 Topology 1B: Open Drain (OD) Signals Driven by the Intel® Celeron® M Processor – FERR# and THERMTRIP#

The Topology 1B OD signals FERR# and THERMTRIP# should adhere to the following routing and layout recommendations. Table 36 presents the layout recommendations for Topology 1B. The routing guidelines allow the signals to be routed as either microstrips or striplines using $55 \Omega \pm 15\%$ characteristic trace impedance. Series resistor R1 is a dampening resistor for reducing overshoot/undershoot reflections on the transmission line. The pull-up voltage for termination resistor Rtt is V_{CCP} (1.05 V).

Intel recommends that the FERR# signal of the Celeron M processor be routed to the FERR# signal of the ICH4. THERMTRIP# may be implemented in a number of ways to meet design goals. It may be routed to the ICH4 or any optional system receiver. Intel recommends that the THERMTRIP# signal of the Celeron M processor be routed to the THERMTRIP# signal of the ICH4. The ICH4's THERMTRIP# signal is a new signal to the I/O controller hub architecture that allows the ICH4 to quickly put the whole system into a S5 state whenever the catastrophic thermal trip point has been reached.

If either FERR# or THERMTRIP# is routed to an optional system receiver rather than the ICH4 and the interface voltage of the optional system receiver does not support a 1.05 V voltage swing, then a voltage translation circuit must be used. If the recommended voltage translation circuit described in Section 6.1.4.7 is used, the driver isolation resistor shown in Figure 50, Rs, should replace the series dampening resistor R1 in Topology 1B. Thus R1 is no longer required in such a topology. Figure 45 illustrates the routing illustration for Topology 1B.

Figure 45. Routing Illustration for Topology 1B

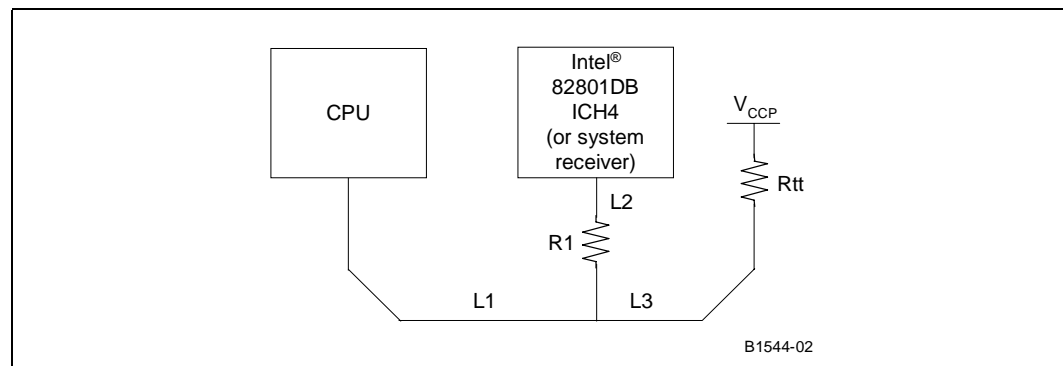


Table 36. Layout Recommendations for Topology 1B

L1	L2	L3	R1	Rtt	Transmission Line Type
0.5 – 12 inches	0 – 3 inches	0 – 3 inches	$56 \Omega \pm 5\%$	$56 \Omega \pm 5\%$	Microstrip
0.5 – 12 inches	0 – 3 inches	0 – 3 inches	$56 \Omega \pm 5\%$	$56 \Omega \pm 5\%$	Stripline

6.1.4.3 Topology 1C: Open Drain (OD) Signals Driven by the Intel® Celeron® M Processor – PROCHOT#

The Topology 1C OD signal PROCHOT# should adhere to the following routing and layout recommendations. Table 37 presents the layout recommendations for Topology 1C. The routing guidelines allow the signal to be routed as either a microstrip or stripline using $55 \Omega \pm 15\%$ characteristic trace impedance. Figure 46 illustrates Intel's recommended implementation for providing voltage translation between the Celeron M processor PROCHOT# signal and a system receiver that utilizes a 3.3 V interface voltage (shown as V_IO_RCVR). The receiver at the output of the voltage translation circuit may be any system receiver that may function properly with the PROCHOT# signal given the nature and usage model of this pin. PROCHOT# is capable of toggling hundreds of times per second to signal a hot temperature condition.

Series resistor R_s is a component of the voltage translation logic and serves as a driver isolation resistor. R_s is shown separated by distance L_3 from the first bipolar junction transistor (BJT), Q1, to emphasize the placement of R_s with respect to Q1. The placement of R_s a distance L_3 before the Q1 BJT is a specific implementation of the generalized voltage translator circuit shown in Figure 50. R_s should be placed at the beginning of the T-split from the PROCHOT# signal. The pull-up voltage for termination resistor R_{tt} is V_{CCP} (1.05 V).

Figure 46. Routing Illustration for Topology 1C

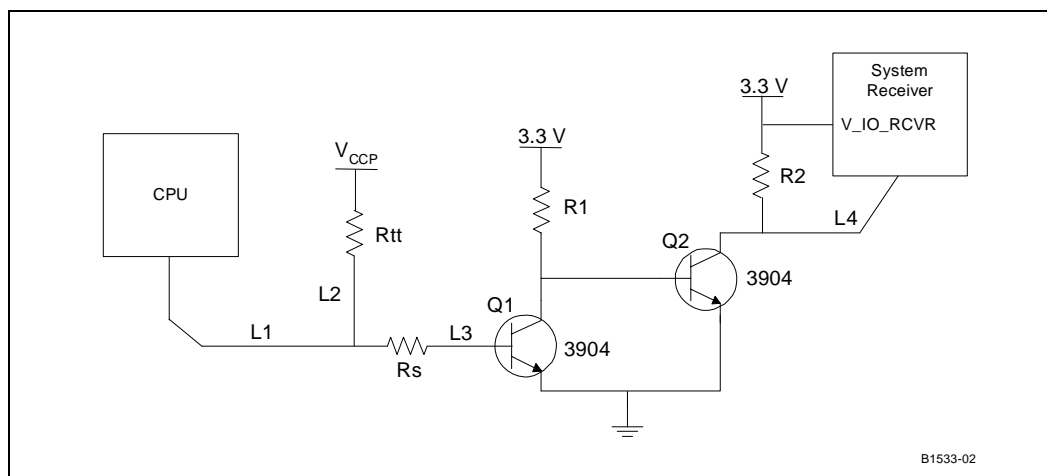


Table 37. Layout Recommendations for Topology 1C

L1	L2	L3	L4	R_s	R_1	R_2	R_{tt}	Transmission Line Type
0.5 – 12 inches	0 – 3 inches	0 – 3 inches	0.5 – 12 inches	$330 \Omega \pm 5\%$	$1.3 \text{ k}\Omega \pm 5\%$	$330 \Omega \pm 5\%$	$56 \Omega \pm 5\%$	Microstrip
0.5 – 12 inches	0 – 3 inches	0 – 3 inches	0.5 – 12 inches	$330 \Omega \pm 5\%$	$1.3 \text{ k}\Omega \pm 5\%$	$330 \Omega \pm 5\%$	$56 \Omega \pm 5\%$	Stripline

6.1.4.4 Topology 2A: Open Drain (OD) Signals Driven by ICH4 – PWRGOOD

The Topology 2A OD signal PWRGOOD, which is driven by the ICH4 (CMOS signal input to processor) should adhere to the following routing and layout recommendations. Table 38 presents the recommended routing requirements for the PWRGOOD signal of the processor. The routing guidelines allow the signal to be routed as either microstrip or striplines using $55 \Omega \pm 15\%$ characteristic trace impedance. The pull-up voltage for termination resistor R_{tt} is V_{CCP} (1.05 V).

The ICH4's CPUPWRGD signal should be routed point-to-point to the processor's PWRGOOD signal. The routing from the processor's PWRGOOD pin should fork out to both the termination resistor, R_{tt} , and the ICH4. Segments L1 and L2 should not T-split from a trace from the pin.

Figure 47 illustrates the routing illustration for Topology 2A.

Figure 47. Routing Illustration for Topology 2A

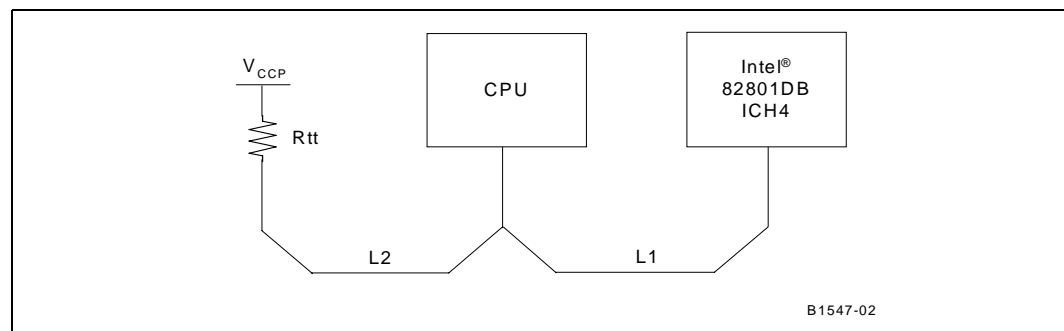


Table 38. Layout Recommendations for Topology 2A

L1	L2	R_{tt}	Transmission Line Type
0.5 – 12 inches	0 – 3 inches	$330 \Omega \pm 5\%$	Microstrip
0.5 – 12 inches	0 – 3 inches	$330 \Omega \pm 5\%$	Stripline

6.1.4.5 Topology 2B: CMOS Signals Driven by ICH4-LINT0/INTR, LINT1/NMI, A20M#, IGNNE#, SLP#, SMI#, and STPCLK#

The Topology 2B CMOS LINT0/INTR, LINT1/NMI, A20M#, IGNNE#, SLP#, SMI#, and STPCLK# signals should implement a point-to-point connection between the ICH4 and the Celeron M processor. Table 39 presents the layout recommendations for Topology 2B. Routing guidelines allow both signals to be routed as either microstrip or striplines using $55 \Omega \pm 15\%$ characteristic trace impedance. No additional PCB components are necessary for this topology.

Figure 48 illustrates the routing illustration for Topology 2B.

Figure 48. Routing Illustration for Topology 2B

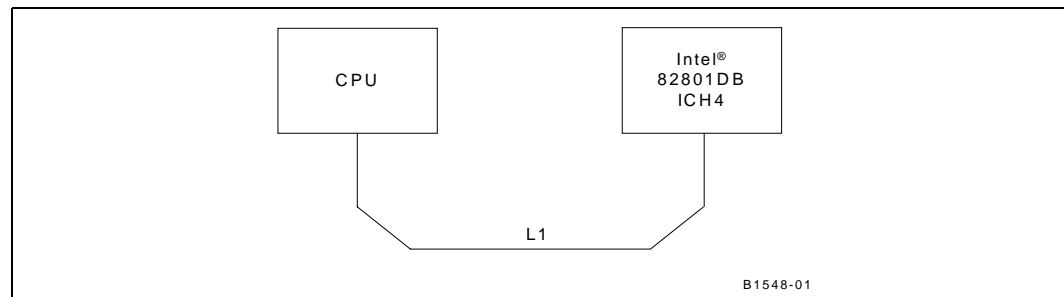


Table 39. Layout Recommendations for Topology 2B

L1	Transmission Line Type
0.5 – 12 inches	Microstrip
0.5 – 12 inches	Stripline

6.1.4.6 Topology 3: CMOS Signals Driven by ICH4 to CPU and FWH – INIT#

The signal INIT# should adhere to the following routing and layout recommendations. Table 40 presents the layout recommendations for Topology 3. The routing guidelines allow both signals to be routed as either microstrip or striplines using $55 \Omega \pm 15\%$ characteristic trace impedance. Figure 49 illustrates Intel's recommended implementation for providing voltage translation between the ICH4's INIT# voltage signaling level and any firmware hub (FWH) that utilizes a 3.3 V interface voltage (shown as a supply V_IO_FWH). Refer to Section 6.1.4.7 for more details on the voltage translator circuit. For convenience, the entire topology and required transistors and resistors for the voltage translator are shown in Figure 49.

Series resistor Rs is a component of the voltage translator logic circuit and serves as a driver isolation resistor. Rs is shown separated by distance L3 from the first bipolar junction transistor (BJT), Q1, to emphasize the placement of Rs with respect to Q1. The placement of Rs a distance of L3 before the Q1 BJT is a specific implementation of the generalized voltage translator circuit shown in Figure 50. The routing recommendations of transmission line L3 in Figure 49 is listed in Table 40 and Rs should be placed at the beginning of the T-split of the trace from the ICH4's INIT# pin.

Figure 49. Routing Illustration for Topology 3

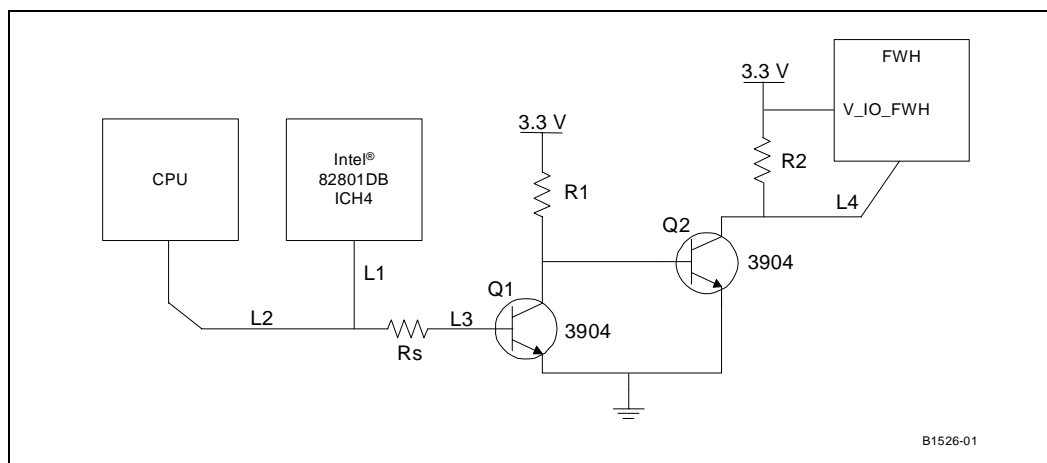


Table 40. Layout Recommendations for Topology 3

L1 + L2	L3	L4	Rs	R1	R2	Transmission Line Type
0.5 – 12 inches	0 – 3 inches	0.5 – 6 inches	$330 \Omega \pm 5\%$	$1.3 \text{ k}\Omega \pm 5\%$	$330 \Omega \pm 5\%$	Microstrip
0.5 – 12 inches	0 – 3 inches	0.5 – 6 inches	$330 \Omega \pm 5\%$	$1.3 \text{ k}\Omega \pm 5\%$	$330 \Omega \pm 5\%$	Stripline

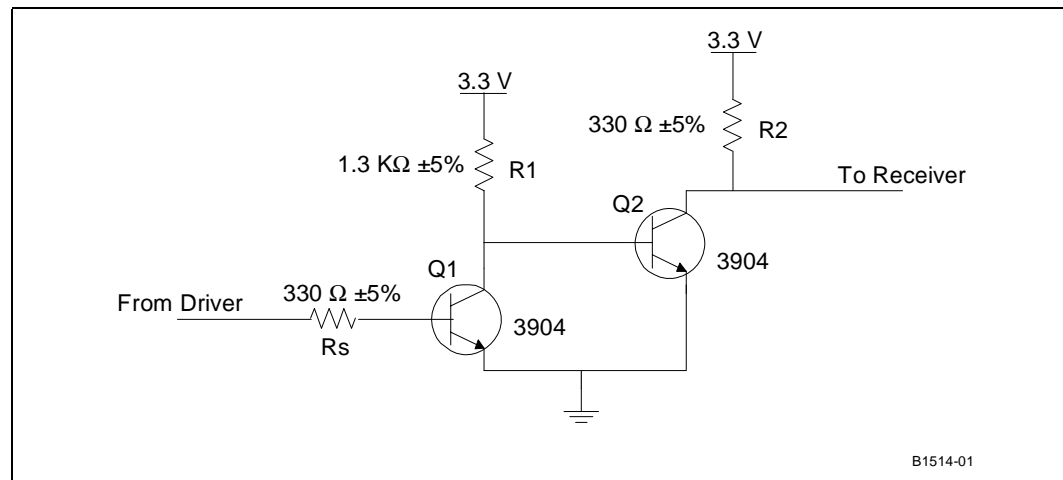
6.1.4.7 Voltage Translation Logic

A voltage translation circuit or component is required on any signals where the voltage signaling level between two components connected by a transmission line may cause unpredictable signal quality. Intel's recommended voltage translation circuit for the platform is shown in Figure 50. For the INIT# signal (Section 6.1.4.6), a specialized version of this voltage translator circuit is used where the driver isolation resistor, R_s , is placed at the beginning of a transmission line that connects to the first bipolar junction transistor, Q1. Though the circuit shown in Figure 50 was developed to work with signals that require translation from a 1.05 V to a 3.3 V voltage level, the same topology and component values, in general, may be adapted for use with other signals as well, provided the interface voltage of the receiver is also 3.3 V. Any component value changes or component placement requirements for other signals must be simulated to ensure good signal quality and acceptable performance from the circuit.

In addition to providing voltage translation between driver and receiver devices, Intel's recommended circuit also provides filtering for noise and electrical glitches. A larger first-stage collector resistor, R1, may be used on the collector of Q1. However, it results in a slower response time to the output falling edge. In the case of the INIT# signal, use resistors with values as close as possible to those listed in Figure 50.

With the low 1.05 V signaling level of the Celeron M processor system bus, the voltage translation circuit provides ample isolation of any transients or signal reflections at the input of transistor Q1 from reaching the output of transistor Q2. Based on simulation results, the voltage translation circuit may effectively isolate transients as large as 200 mV and that last as long as 60 ns.

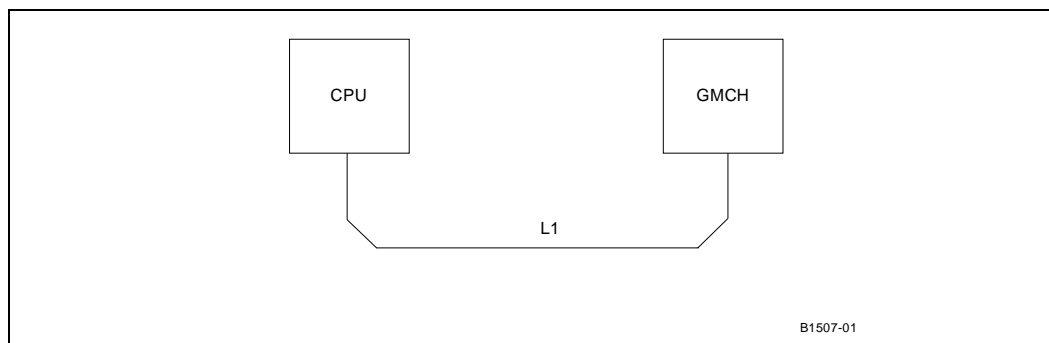
Figure 50. Voltage Translation Circuit



6.1.5 Processor RESET# Signal

The RESET# signal is a common clock signal driven by the GMCH CPURESET# pin. In a production system where no ITP700FLEX debug port is implemented, a simple point-to-point connection between the CPURESET# pin of the GMCH and the Celeron M processor RESET# pin is recommended (see Figure 51). On-die termination of the AGTL+ buffers on both the processor and the GMCH provide proper signal quality for this connection. This is the same case as for the other common clock signals listed Section 6.1.2. Length L1 of this interconnect should be limited to minimum of one inch and maximum of 6.5 inches.

Figure 51. Processor RESET# Signal Routing Topology With NO ITP700FLEX Connector



For a system that implements an ITP700FLEX debug port, a more elaborate topology is required to ensure proper signal quality at both the processor signal pad and the ITP700FLEX input receiver. In this case, implement the topology shown in Figure 52. The CPURESET# signal from the GMCH should fork out (do not route one trace from GMCH pin and then T-split) towards the processor's RESET# pin as well as toward the Rtt and Rs resistive termination network placed next to the ITP700FLEX debug port connector. Rtt ($220\ \Omega \pm 5\%$) pulls up to the V_{CCP} voltage and is placed at the end of the L2 line that is limited to a six inch maximum length. Place Rs ($22.6\ \Omega \pm 1\%$) next to Rtt to minimize routing between them in the vicinity of the ITP700FLEX connector to limit the L3 length to less than 0.5 inch. ITP700FLEX operation requires matching the $L2 + L3 - L1$ length to the length of the BPM[4:0]# signals within ± 250 mils. Refer to Table 41 for routing length summary and termination resistor values.

Figure 52 illustrates the processor RESET# signal routing topology with an ITP700FLEX connector.

Figure 52. Processor RESET# Signal Routing Topology With ITP700FLEX Connector

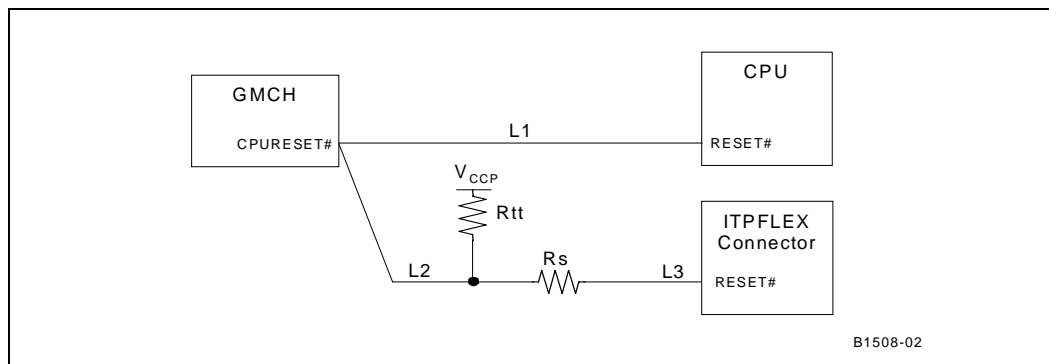


Table 41 presents processor RESET# signal routing guidelines with an ITP700FLEX connector.

Table 41. Processor RESET# Signal Routing Guidelines with an ITP700FLEX Connector

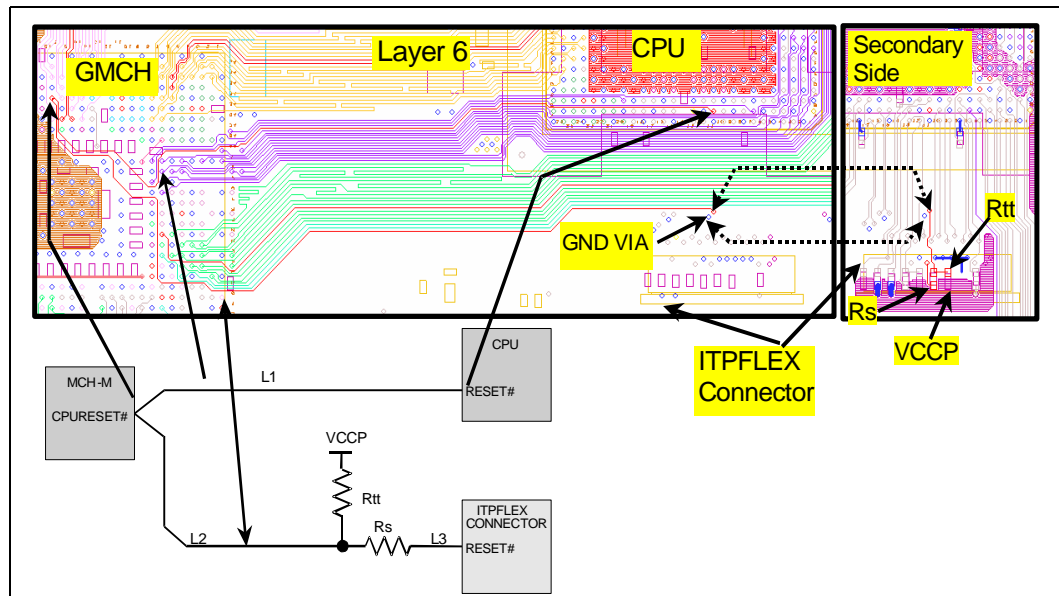
L1	L2 + L3	L3	Rs	Rtt
1 – 6 inches	6 inches max.	0.5 inch max.	$R_s = 22.6 \Omega \pm 1\%$	$R_{tt} = 220 \pm 5\%$

6.1.5.1 Processor RESET# Routing Example

Figure 53 illustrates a board routing example for the RESET# signal with an ITP700FLEX debug port implemented. Figure 53 illustrates how the CPURST# pin of GMCH forks out into two branches on Layer 6 of the PCB. One branch is routed directly to the Celeron M processor RESET# pin among the rest of the common clock signals. Another branch routes below the address signals and vias down to the secondary side that route to the Rs and Rtt resistors. These resistors are placed in the vicinity of the ITP700FLEX debug port.

Note: The placement of Rs and Rtt next to each other is to minimize the routing between Rs and Rtt as well as the minimal routing between Rs and the ITP700FLEX connector. Also, because a transition between Layer 6 and the secondary side occurs, a GND stitching via is added to ensure continuous ground reference of the secondary side routing of the RESET# signal to ITP700FLEX connector.

Figure 53. Processor RESET# Signal Routing Example with ITP700FLEX Debug Port



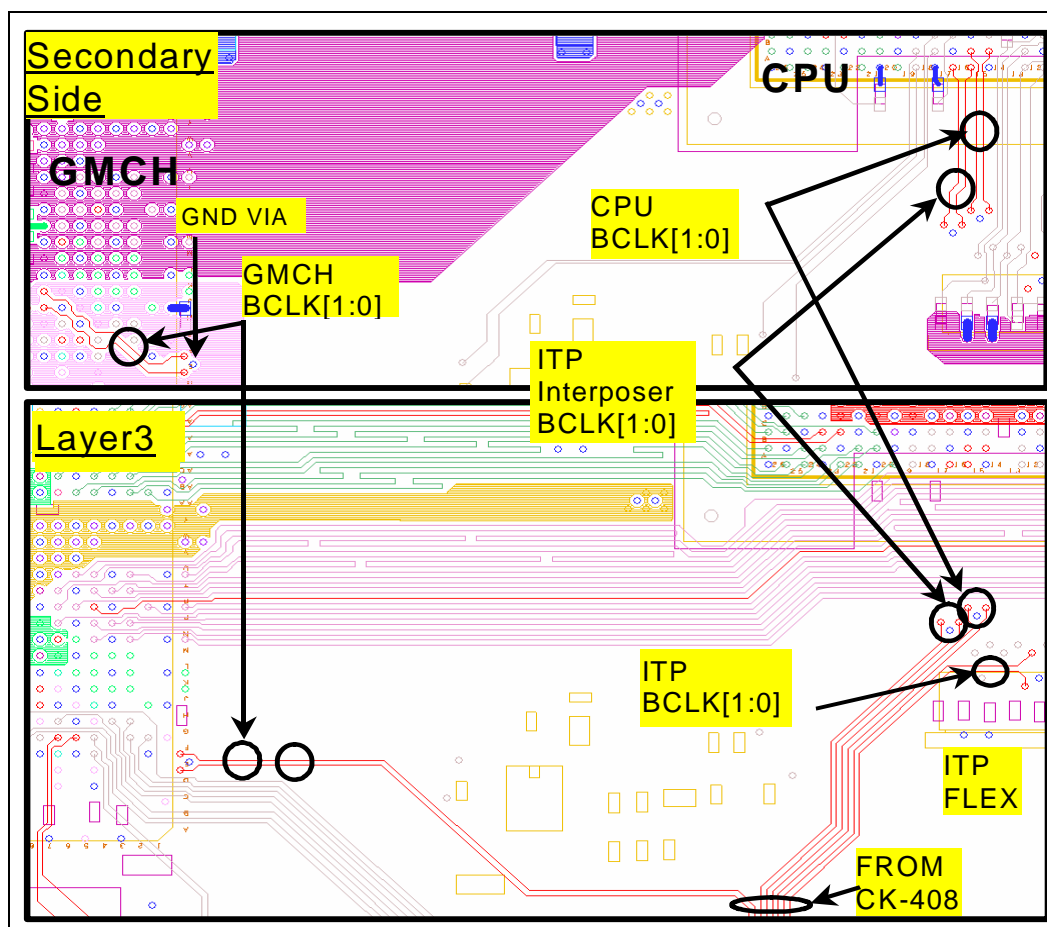
6.1.6 Processor and GMCH and Host Clock Signals

Figure 54 illustrates processor and GMCH host clock signal routing. Both the processor and the GMCH's BCLK[1:0] signals are initially routed from the CK-408 clock generator on Layer 3. In Intel's recommended routing example (Figure 54), secondary side layer routing of BCLK[1:0] is 507 mils long. To meet length-matching requirements between the processor and GMCH's BCLK[1:0] signals, a similar transition from Layer 3 to the secondary side layer is done next to the GMCH package outline. Routing of the GMCH's BCLK[1:0] signals on the secondary side is also trace tuned to 507 mils. BCLK[1:0] layer transition vias are accompanied by GND stitching vias. For similar reasons, routing for the ITP interposer's BCLK[1:0] signals also transition from Layer 3 to the secondary side layer and have 507-mil long traces on this layer. Throughout the routing length on Layer 3, BCLK[1:0] signals should reference a solid GND plane on Layer 2 and Layer 4 as shown in Figure 41.

If a system supports either the on-board ITP700FLEX connector or ITP Interposer only, then differential host clock routing to either the ITP700FLEX connector or CPU socket (but not both) is required.

Figure 54 illustrates the Celeron M processor and Intel 82852GM GMCH host clock layout routing example.

Figure 54. Intel® Celeron® M Processor and Intel® 852GM Chipset GMCH (82852GM) Host Clock Layout Routing Example



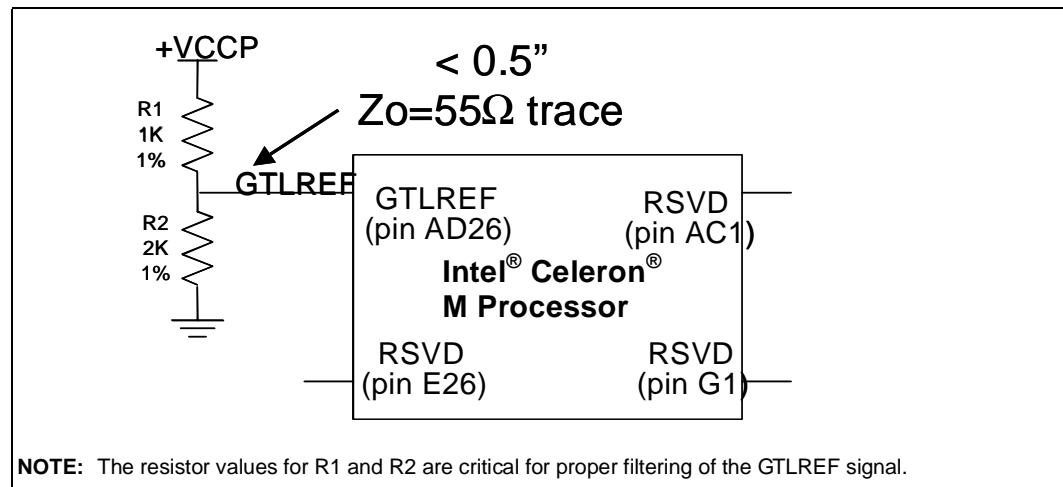
6.1.7 Processor GTLREF Layout and Routing Recommendations

There is one AGTL+ reference voltage pin on the Celeron M processor, GTLREF, used to set the reference voltage level for the AGTL+ signals (GTLREF). The reference voltage must be supplied to the GTLREF pin. The voltage level supplied to GTLREF must be equal to $\frac{2}{3} * V_{CCP} \pm 2\%$. The GMCH also requires a reference voltage (MCH_GTLREF) to be supplied to its HVREF[4:0] pins. The GTLREF voltage divider for both the processor and GMCH cannot be shared. Thus, both the processor and GMCH must have their own locally generated GTLREF networks. Figure 55 illustrates Intel's recommended topology for generating GTLREF for the processor using a $R1 = 1\text{ k}\Omega \pm 1\%$ and $R2 = 2\text{ k}\Omega \pm 1\%$ resistive divider.

Since the input buffer trip point is set by the $\frac{2}{3} * V_{CCP}$ on GTLREF and to allow tracking of V_{CCP} voltage fluctuations, **no** decoupling should be placed on the GTLREF pin. The node between R1 and R2 (GTLREF) should be connected to the GTLREF pin of the processor with $Z_o = 55\ \Omega$ trace shorter than 0.5 inch. Space any other switching signals away from GTLREF with a minimum separation of 25 mils. Do not allow signal lines to use the GTLREF routing as part of their return path (i.e., do not allow the GTLREF routing to create splits or discontinuities in the reference planes of the FSB signals).

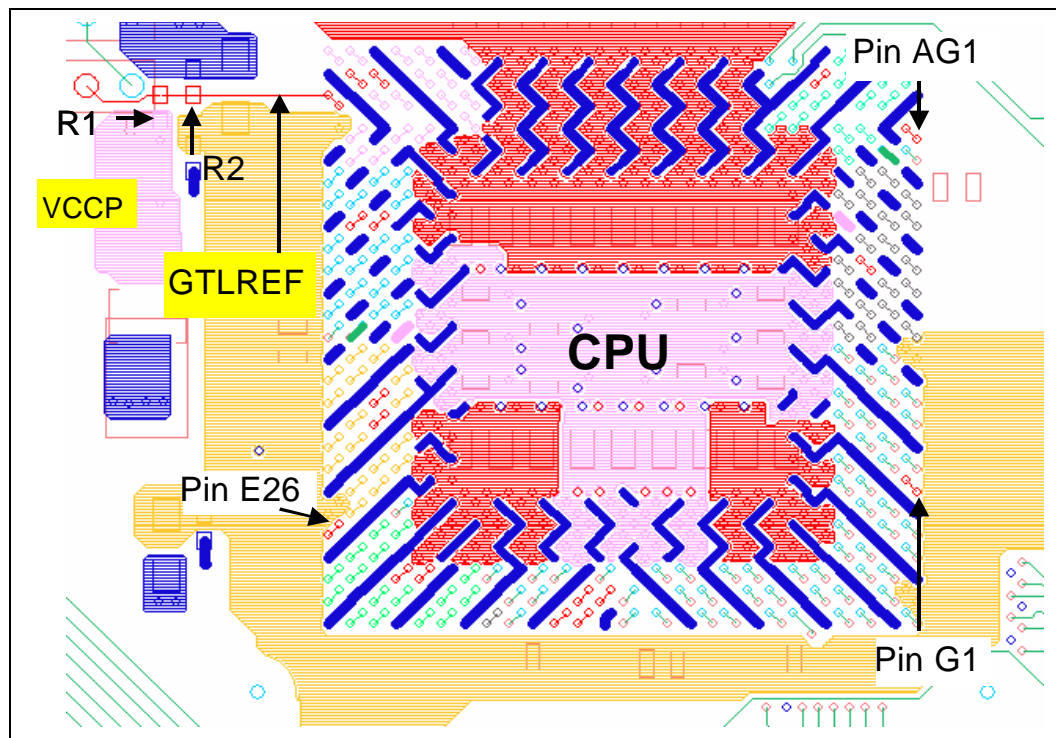
RSVD signal pins E26, G1, and AC1 are to be left unconnected on Celeron M processor based systems.

Figure 55. Intel® Celeron® M Processor GTLREF Voltage Divider Network



Intel's recommended layout of GTLREF for the Celeron M processor is shown in Figure 56. To avoid interaction with FSB routing and power delivery, GTLREF's R1 and R2 components are placed next to each other on the primary side of the PCB and connected with a $Z_o = 55\ \Omega$ to the GTLREF pin on the processor. The BGA ball lands on the primary side for the RSVD signal pins E26, G1, and AC1 are shown for illustrative purposes and are not routed.

Figure 56. Intel® Celeron® M Processor GTLREF PCB Layout



6.1.8 AGTL+ I/O Buffer Compensation

The Celeron M processor has four pins, COMP[3:0], and the GMCH has two pins, HRCOMP[1:0], that require compensation resistors to adjust the AGTL+ I/O buffer characteristics to specific board and operating environment characteristics. The GMCH requires two special reference voltage generation circuits to pins HSWNG[1:0] for the same purpose described above. Refer to the *Intel® 852GM Chipset Graphics and Memory Controller Hub (GMCH) Datasheet* and *Intel® Celeron® M Processor Datasheet* for details on resistive compensation.

6.1.8.1 Intel® Celeron® M Processor AGTL+ I/O Buffer Compensation

For the Celeron M processor, the COMP[2] and COMP[0] pins (see Figure 57) each must be pulled down to ground with $27.4 \Omega \pm 1\%$ resistors and should be connected to the Celeron M processor with a $Z_0 = 27.4 \Omega$ trace that is less than 0.5 inch from the processor pins. The COMP[3] and COMP[1] pins (see Figure 58) each must be pulled down to ground with $54.9 \Omega \pm 1\%$ resistors and should be connected to the Celeron M processor with a $Z_0 = 55 \Omega$ trace that is less than 0.5 inch from the processor pins. COMP[3:0] traces should be at least 25 mils (> 50 mils preferred) away from any other toggling signal.

Figure 57 illustrates the Celeron M processor COMP[2] and COMP[0] resistive compensation.

Figure 57. Intel® Celeron® M Processor COMP[2] and COMP[0] Resistive Compensation

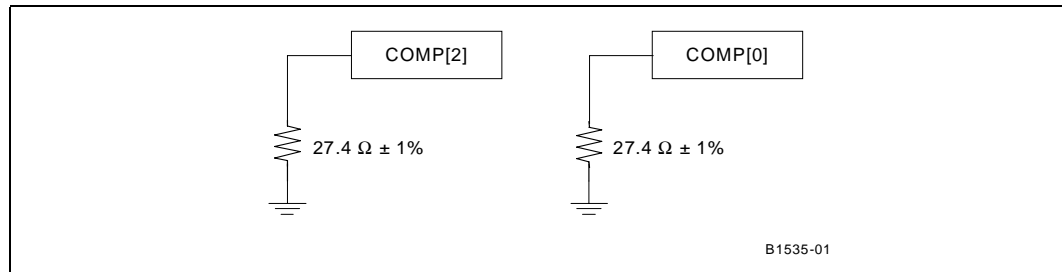
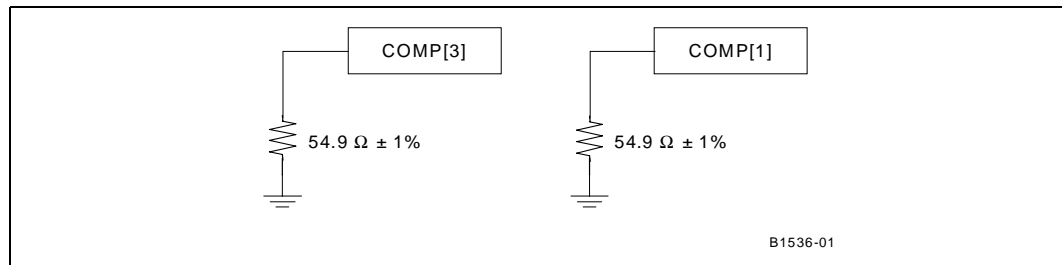


Figure 58 illustrates the Celeron M Processor COMP[3] and COMP[1] resistive compensation.

Figure 58. Intel® Celeron® M Processor COMP[3] and COMP[1] Resistive Compensation



Intel's recommended layout of the Celeron M processor COMP[3:0] resistors is shown in Figure 59. To avoid interaction with Celeron M processor FSB routing on internal layers and V_{CCA} power delivery on the primary side, Layer 1, COMP[1:0] resistors are placed on the secondary side. Ground connections to the COMP[1:0] resistors use a small ground flood on the secondary side layer and connect only with a single GND via to stitch the GND planes. The compact layout as shown in Figure 59 should be used to avoid excessive perforation of the V_{CCP} plane power delivery. Figure 59 illustrates how a 27.4 Ω resistor connects with an ~18 mil wide ($Z_o = 27.4 \Omega$) and 160 mil long trace to COMP0. Necking down to 14 mils is allowed for a short length to pass between the dog bones. The 54.9 Ω resistor connects with a regular 5 mil wide ($Z_o = 55 \Omega$) and 267 mil long trace to COMP1. Placement of COMP[1:0] on the primary side is possible as well. An alternative placement implementation is shown in Figure 60.

To minimize PCB space usage and produce a robust connection, the COMP[3:2] resistors are also placed on the secondary side (Figure 59, right side). A 27.4 Ω resistor connects with an 18 mil wide ($Z_o = 27.4 \Omega$) and 260 mil long trace to COMP2. Necking down to 14 mils is allowed for a short length to pass in between the dog bones. The COMP2 (Figure 59, left side) dog bone trace connection on the primary side is also widened to 14 mils to meet the $Z_o = 27.4 \Omega$ characteristic impedance target. The right side of Figure 59 also illustrates how the 54.9 Ω ± 1% resistor connects with a regular 5 mil wide ($Z_o = 55 \Omega$) and 100 mil long trace to COMP3. The ground connection of COMP[3:2] is done with a small flood plane on the secondary side that connects to the GND vias of pins AA1 and Y2 of the Celeron M processor pin-map. This is done to avoid via interaction with the Celeron M processor FSB routing on Layer 3 and Layer 6.

For COMP2 and COMP0, it is extremely important that 18 mil wide dog bone connections on the primary side and 18 mil wide traces on the secondary sides be used to connect the signals to compensation resistors on the secondary side, as shown in Figure 61. The 18 mil wide dog bones and traces are used to achieve the $Z_o = 27.4 \Omega$ target to ensure proper operation of the Celeron M processor FSB. Refer to Figure 57 for more details.

Figure 59 illustrates the Celeron M processor COMP[3:0] resistor layout.

Figure 59. Intel® Celeron® M Processor COMP[3:0] Resistor Layout

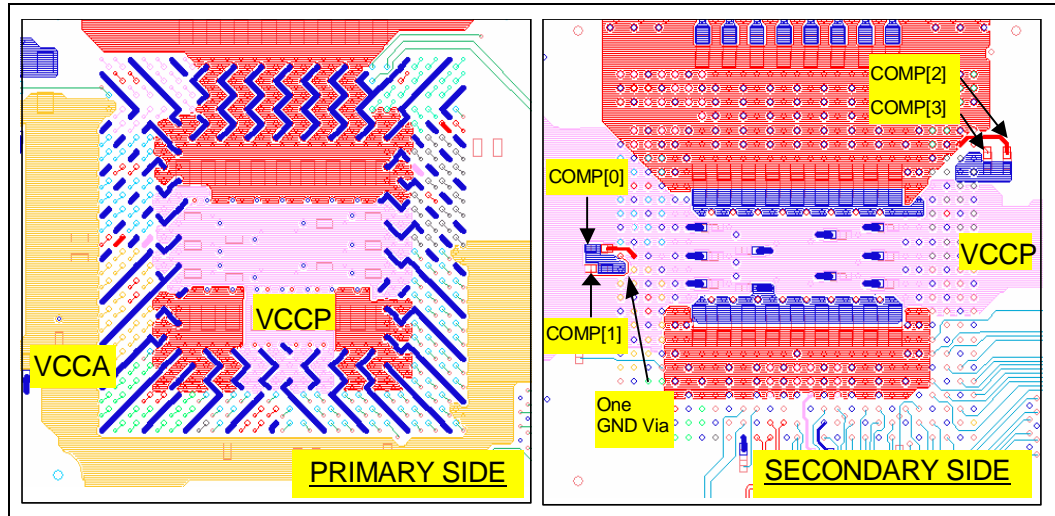


Figure 60 illustrates the Celeron M processor COMP[1:0] resistor alternative primary side layout.

Figure 60. Intel® Celeron® M Processor COMP[1:0] Resistor Alternative Primary Side Layout

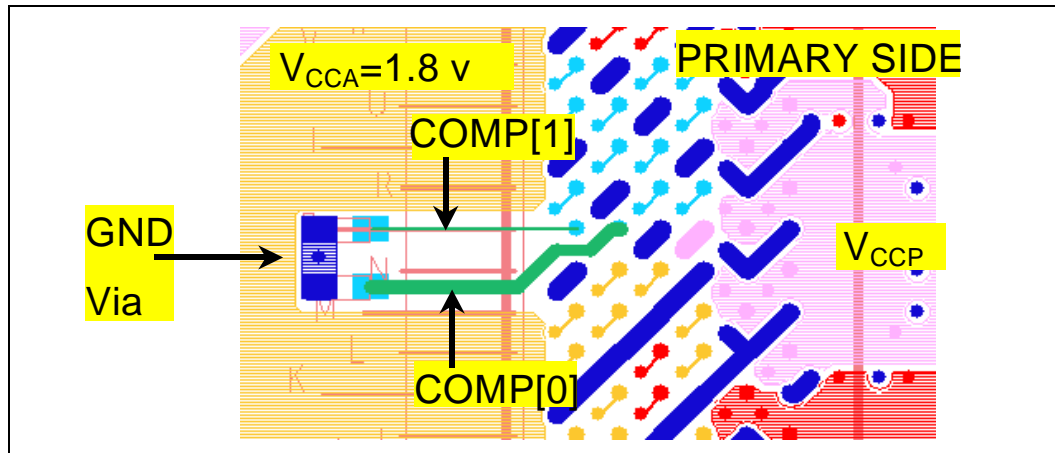
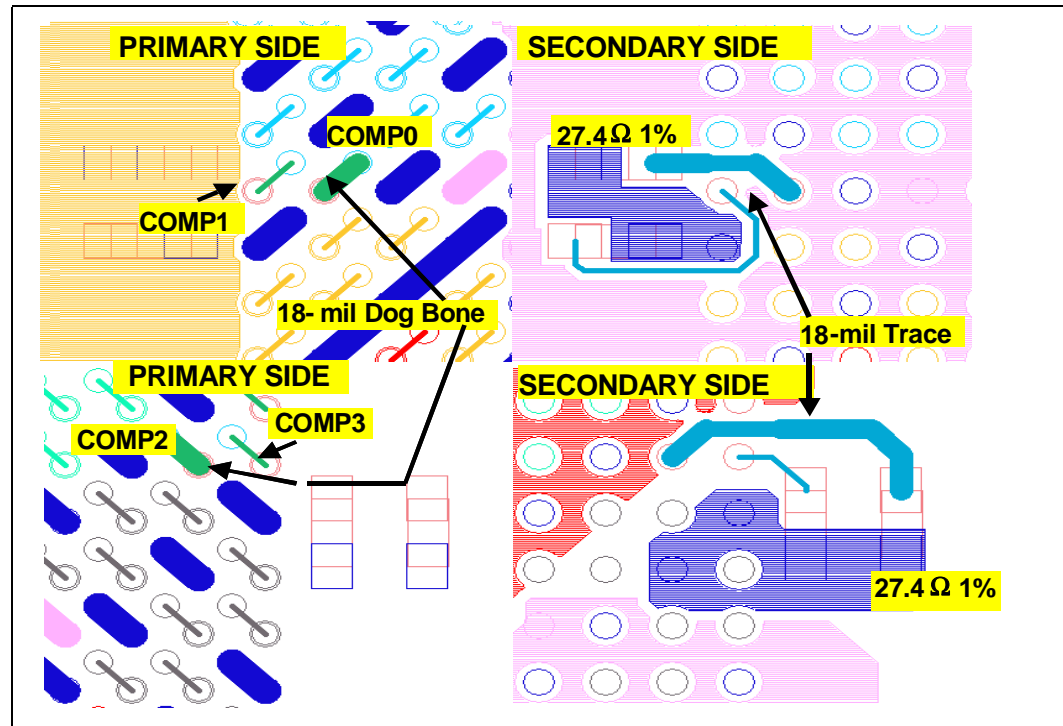


Figure 61 illustrates the COMP2 and COMP0 18-mil wide dog bones and traces.

Figure 61. COMP2 and COMP0 18-mil Wide Dog Bones and Traces



6.1.9 Intel® Celeron® M Processor System Bus Strapping

The Celeron M processor and GMCH both have pins that require termination for proper component operation.

1. For the processor, provide a stuffing option for the TEST[3:1] pin to allow a $1\text{ k}\Omega \pm 5\%$ pull-down to ground for testing purposes. For proper processor operation, the resistor should not be stuffed. Resistors for the stuffing option on these pins should be placed within two inches of the processor. For normal operation, these resistors should not be stuffed.
2. The processor's ITP signals, TDI, TMS, TRST and TCK should assume default logic values even if the ITP debug port is not used. The TDO signal may be left open or no connect in this case. These resistors should be connected to the processor within two inches from their respective pins.

Note: Table 42 is applicable only when neither the onboard ITP nor ITP interposer are planned to be used. Intel does not recommend use of the ITP interposer debug port if there is a dependence only on the PCB termination resistors

The signals below should be isolated from the PCB via specific termination resistors on the ITP interposer itself per interposer debug port recommendations.

Table 42 presents the ITP signal default strapping when an ITP debug port is not used.

Table 42. ITP Signal Default Strapping When ITP Debug Port is Not Used

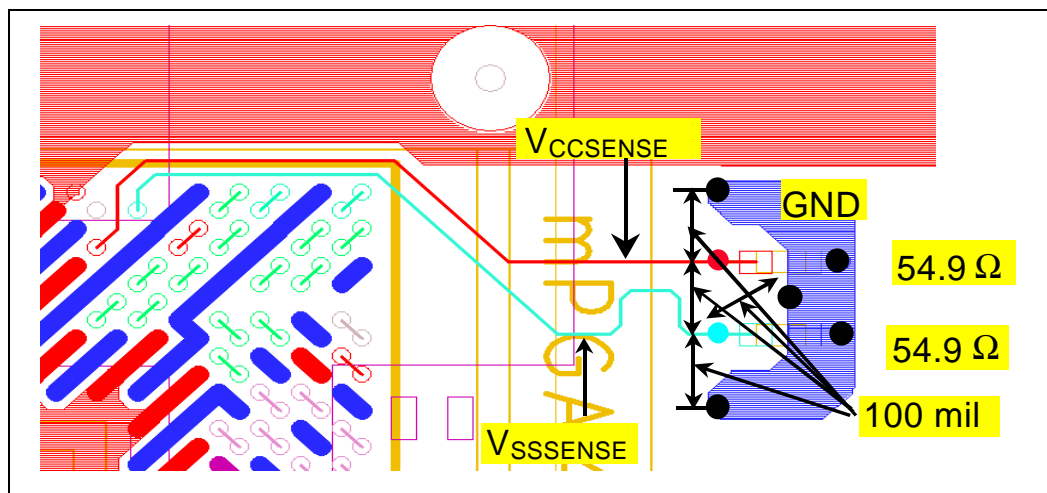
Signal	Resistor Value	Connect To	Resistor Placement
TDI	$150\ \Omega \pm 5\%$	V_{CCP}	Within 2 inches of the CPU
TMS	$39\ \Omega \pm 5\%$	V_{CCP}	Within 2 inches of the CPU
TRST#	$680\ \Omega \pm 5\%$	GND	Within 2 inches of the CPU
TCK	$27\ \Omega \pm 5\%$	GND	Within 2 inches of the CPU
TDO	Open	NC	N/A

6.1.10 Intel® Celeron® M Processor $V_{CCSENSE}/V_{SSSENSE}$ Design Recommendations

The $V_{CCSENSE}$ and $V_{SSSENSE}$ signals of the Celeron M processor provide isolated, low-impedance connections to the processor's core power (V_{CC}) and ground (V_{SS}). These pins may be used to sense or measure power (V_{CC}) or ground (V_{SS}) near the silicon with little noise. To make them available for measurement purposes, Intel recommends that $V_{CCSENSE}$ and $V_{SSSENSE}$ both be routed with a $Z_o = 55\ \Omega \pm 15\%$ trace of equal length. Use 3:1 spacing between the routing for the two signals and all other signals should be a minimum of 25 mils (preferably 50 mils) from $V_{CCSENSE}$ and $V_{SSSENSE}$ routing. Terminate each line with an optional (default is No Stuff) $54.9\ \Omega \pm 1\%$ resistor. Also, add a ground via spaced 100 mils away from each of the test point vias for $V_{CCSENSE}$ and $V_{SSSENSE}$. Place a third ground via between them to allow for a differential probe ground.

Figure 62 illustrates the $V_{CCSENSE}/V_{SSSENSE}$ routing example.

Figure 62. $V_{CCSENSE}/V_{SSSENSE}$ Routing Example



Intel® 852GM Chipset and Processor Platform Power Delivery Guidelines 7

7.1 Definitions

Suspend-To-RAM (STR):

In the STR state, the system state is stored in main memory and all unnecessary system logic is turned off. Only main memory and logic required to wake the system remain powered.

Full-power operation:

During full-power operation, all components on the PCB remain powered. Full-power operation includes both the full-on operating state and the S1 (PROCESSOR stop-grant) state.

Suspend operation:

During suspend operation; power is removed from some components on the PCB. The board supports three suspend states: Suspend-to-RAM (S3), Suspend-to-Disk (S4), and Soft-off (S5).

Power rails:

An ATX power supply has six power rails: +5 V, -5 V, +12 V, -12 V, +3.3 V, 5 Vsb. In addition to these power rails, several other power rails are created with voltage regulators.

Core power rail:

Power rail that is only on during full-power operation. These power rails are on when the PSON signal is asserted to the ATX power supply. The core power rails that are distributed directly from the ATX 12 V power supply are +5 V, -5 V, +12 V, -12 V, +3.3 V.

Standby power rail:

A power rail that is on during suspend operation (these rails are also on during full-power operation). These rails are on at all times (when the power supply is plugged into AC power). The only standby power rail that is distributed directly from the ATX power supply is: 5 Vsb (5V Standby). There are other standby rails that are created with voltage regulators on the PCB.

Derived power rail:

A derived power rail is any power rail that is generated from another power rail using an on-board voltage regulator. For example, 3.3 Vsb is usually derived (on the PCB) from 5 Vsb using a voltage regulator.

Dual power rail:

A dual power rail is derived from different rails at different times (depending on the power state of the system). Usually, a dual power rail is derived from a standby supply during suspend operation and derived from a core supply during full-power operation.

Note: The voltage on a dual power rail may be misleading.

7.2 Mobile Intel® Celeron® Processor Power Sequence Requirements

Contact your Intel Field Representative for details on the Mobile Celeron processor with the Intel IMVP-III voltage regulator.

7.3 Intel® Celeron® M Processor Power Sequence Requirements

Contact your Intel Field Representative for details on the Celeron M processor with the Intel IMVP-IV voltage regulator.

7.4 Intel® Celeron® Processor Power Sequence Requirements

Intel recommends using a *Voltage Regulator-Down VRD 10.0 Design Guidelines*-compliant regulator for the processor system board designs. An Intel Celeron Processor and VR Down Design Guidelines-compliant regulator may be integrated as part of the system board or on a module. To ensure that voltage fluctuations remain within the processor datasheet, properly place high-frequency and bulk-decoupling capacitors as needed between the voltage regulator and the processor. See [Section 7.4.7](#) for recommendations on the amount of decoupling required.

Specifications for the processor voltage are contained in the *Intel® Celeron® Processor on 0.13 Micron Process in the 478-Pin Package*. These specifications are for the processor. For guidance on correlating the die specifications to socket level measurements, refer to the *Voltage Regulator-Down (VRD) 10.0 Design Guidelines*.

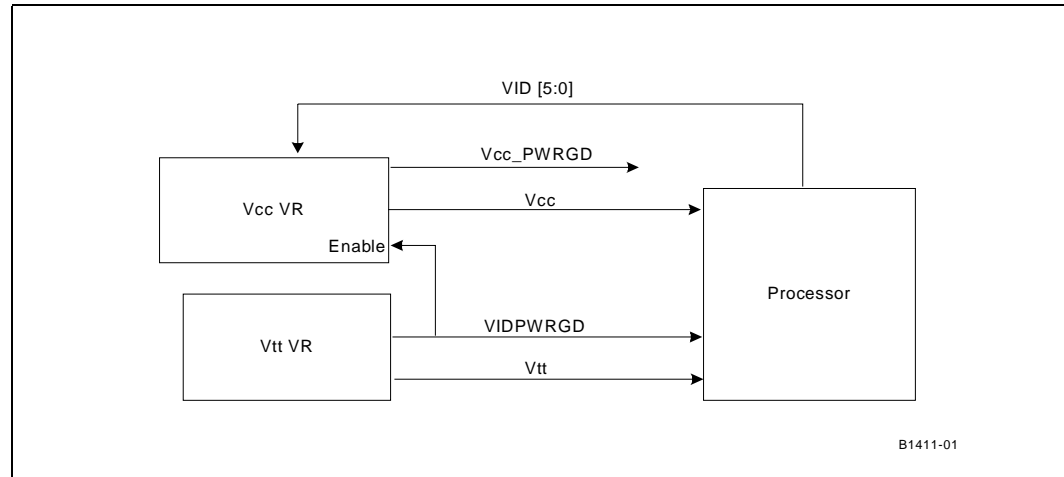
The voltage tolerance of the loadlines contained in these documents help the system designer achieve a flexible PCB design solution for all processor frequencies. Failure to meet the load line requirements when modeling the system power delivery may result in a system that is not upgradeable.

The processor requires local regulation because of its higher current requirements and to maintain power supply tolerance. For example, an onboard DC-to-DC converter converts a higher DC voltage to a lower level using a switching regulator. Distributing lower current at a higher voltage to the converter minimizes unwanted losses ($I \times R$). More important, however, an onboard regulator regulates the voltage locally, which minimizes DC line losses by reducing PCB resistance on the processor voltage.

7.4.1 Power Delivery Architectural Block Diagram

Figure 63 shows the VRM/EVRD 10.0 voltage regulator block diagram.

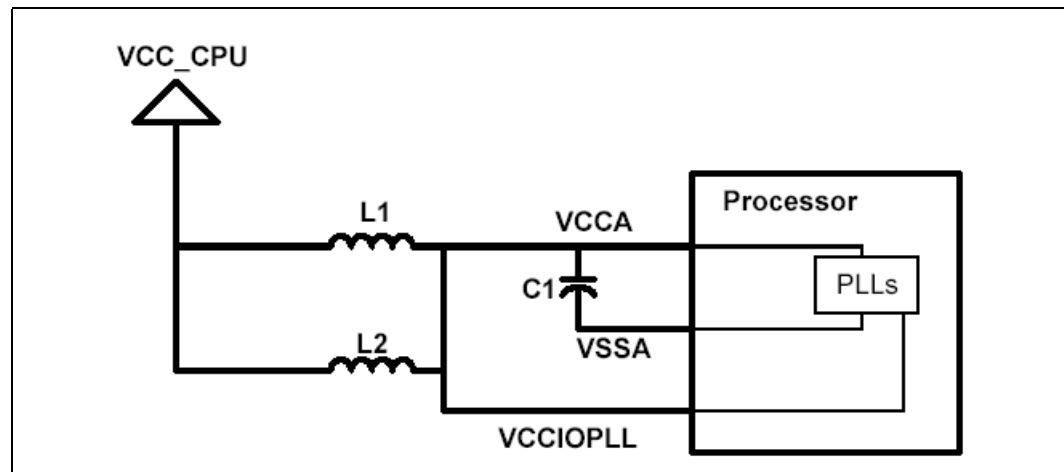
Figure 63. VRM/EVRD 10.0 Voltage Regulator Block Diagram



7.4.2 Processor Phase Lock Loop Design Guidelines

VCCA and VCCIOPLL are power sources required by the PLL clock generators on the processor silicon. Since these PLLs are analog in nature, they require quiet power supplies for minimum jitter. Jitter is detrimental to the system. It degrades external I/O timings as well as internal core timings (that is, maximum frequency). To prevent this degradation, these supplies must be low-pass filtered from V_{CC} . The general desired filter topology is shown in Figure 64. Not shown in the core is parasitic routing. Excluded from the external circuitry are parasitics associated with each component.

Figure 64. Typical VCCIOPLL, VCCA and VSSA Power Distribution



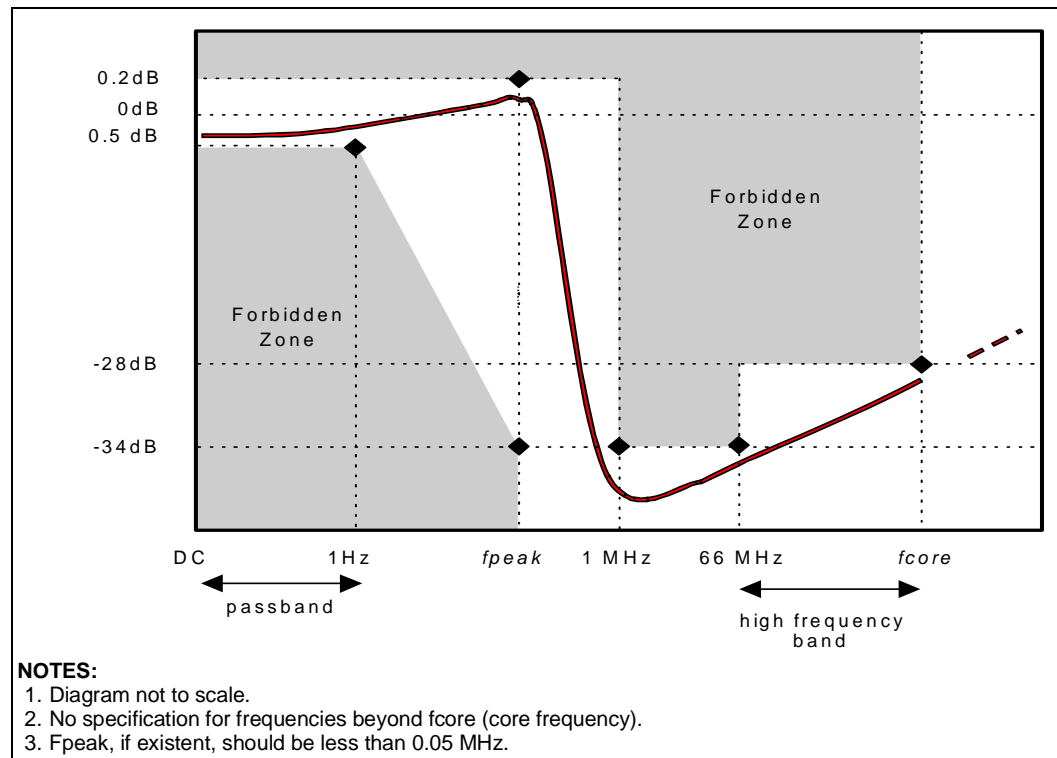
The function of the filter is twofold. It protects the PLL from external noise through low-pass attenuation. It also protects the PLL from internal noise through high-pass filtering. In general, the low-pass description forms an adequate description for the filter. For simplicity, this document addresses the recommendation for the VCCA filter design. The same characteristics and design approach are applicable for the VCCIOPLL filter design.

The AC low-pass recommendation, with input at V_{CC} and output measured across the capacitor (CA or CIO in Figure 64), is as follows:

- < 0.2 dB gain in pass band
- < 0.5 dB attenuation in pass band < 1 Hz (see DC drop in next set of requirements)
- > 34 dB attenuation from 1 MHz to 66 MHz
- > 28 dB attenuation from 66 MHz to core frequency

The AC filter recommendation is graphically shown in Figure 65.

Figure 65. AC Filter Recommendation



7.4.2.1 Other Recommendations

- Use shielded type inductors to reduce crosstalk.
- Capacitor C1: $22 \mu F \pm 20\%$ to $33 \mu F \pm 20\%$. The ESL is ≤ 2.5 nH and the ESR $\leq 0.225 \Omega$.
- Inductor: $10 \mu H \pm 25\%$. $R_{dc} = 0.4 \pm 30\%$. Self-Resonant Frequency > 30 MHz. IDC = 60 mA.
- Filter should support DC current of 100 mA.

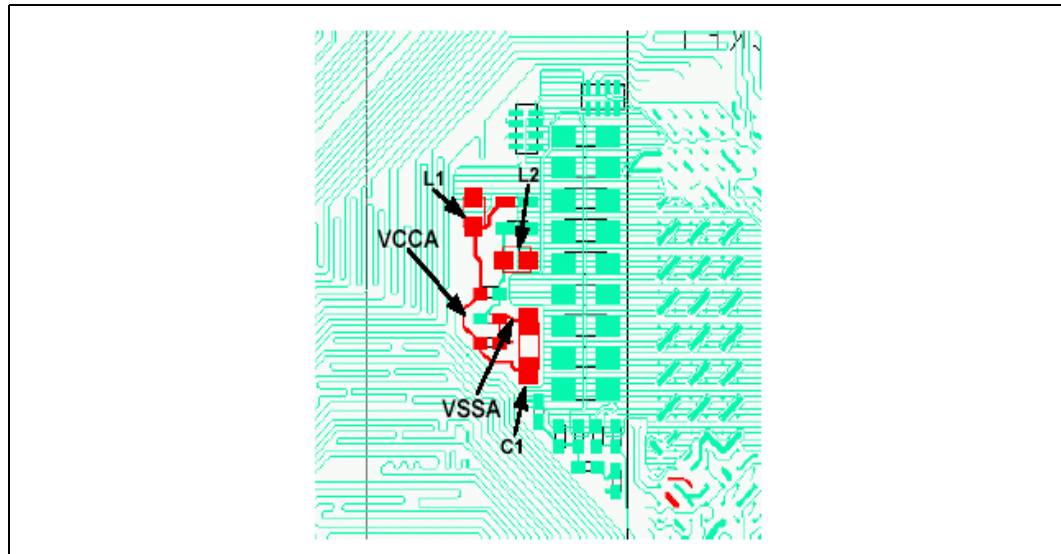
- DC voltage drop from VCC_CPU to VCCA is < 70 mV.
- In order to maintain a DC drop of less than 70 mV, the total DC resistance of the filter from processor V_{CC} to the processor socket should be a maximum of 0.7 Ω .

Other routing requirements:

- C1 should be within 600 mils of the VCCA and VSSA pins. An example of the component placement is shown in Figure 66.
- VCCA route should be parallel and next to VSSA route (minimize loop area).
- A minimum of a 12 mil trace should be used to route the filter to the processor pins.
- The inductors (L1 and L2) should be close to the capacitor C1.
- It is recommended that the total resistance of DCR plus routing does not exceed 0.36 Ω . This results in a maximum drop of 36 mV for 100 mA maximum.

Figure 66 shows a VCCA and VSSA Layer 1 routing example.

Figure 66. VCCA and VSSA Layer 1 Routing Example



7.4.3 Voltage and Current

A VRM/EVRD 10.0 processor core regulator supplies the required voltage and current to a single processor. VRM/EVRD 10.0 supports dynamic voltage identification (VID), which requires the ability to reduce the load line voltage in Figure 67 by 250 mV. The VRM/EVRD must be capable of accepting voltage level changes of 12.5 mV steps every 5 μ s, up to 20 steps (250 mV) in 100 μ s. The low voltage state is maintained for at least 1 ms. The worst-case settling time, including line-to-line skew, for the six VID lines is 400 ns. The VID inputs should contain circuitry to prevent false tripping or latching of VID codes during the settling time.

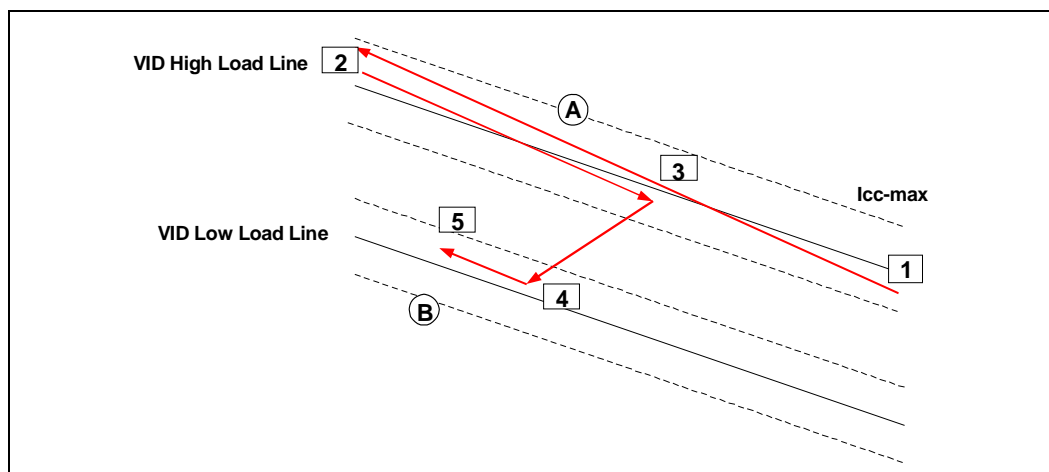
During a transition the output voltage must be between the maximum voltage of the high range ('A' in Figure 67) and the minimum voltage of the low range ('B'). The VRM/EVRD must respond to a transition from VID-low to VID-high by regulating its V_{CC} output to the range defined by the new,

final VID code within 50 μ s of the final step. The time to move the output voltage from VID-high to VID-low depends on the PWM controller design, the amount of system decoupling capacitance, and the processor load.

Figure 67 shows operating states as a representative processor changes levels. The diagram assumes steady state, maximum current during the transition for ease of illustration; actual processor behavior allows for any di/dt event during the transitions, depending on the code it is executing at that time. In the example, the processor begins in a high-load condition. In transitions 1 to 2 and 2 to 3, the processor prepares to switch to the low-voltage range with a transition to a low-load condition followed by an increased activity level. Transition 3 to 4 is a simplification of the multiple steps from the high-voltage load line to the low-voltage load line. Transition 4 to 5 is an example of a response to a load change during normal operation in the lower range.

The processor load may not be sufficient to absorb all of the energy from the output capacitors on the PCB when VID changes to a lower output voltage. The VRM/EVRD design should ensure that any energy transfer from the capacitors does not impair the operation of the VRM/EVRD, the AC-DC supply, or any other parts of the system.

Figure 67. Processor Transition States



7.4.4 Voltage Identification for VRM/EVRD 10.0

There are five VID balls/pins on the processor. These signals may be used to support automatic selection of V_{CC} voltages. They are needed to cleanly support voltage specification variations for current and future processors. VIDs are defined in Table 44. The VID[4:0] signals are open drain on the processor and need pull-up resistors to 3.3 V on the PCB.

The VRM/EVRD accepts six lines to set the nominal voltage. When the VID[4:0] inputs are all high (in this case, VID5 is not important), such as when no processor is installed, the VRM/EVRD should disable its output. When this disable code appears during previously normal operation, the VRM/EVRD should turn off its output within 500 ms. Other platform components may use VID inputs and may require tighter limits than specified in Table 44.

VID[4:0] are compatible with the Celeron using five-bit VID codes. VID [5] has to be set as high when five-bit VID codes are used. VID [5:0] will be used on processors with six-bit VID codes.

Table 43 presents the VID specifications.



Table 43. VID Specifications

Symbol	Parameter	Min	Max	Units	Notes
V_{IH}	Input High Voltage	0.8	3.465	V	†
V_{IL}	Input Low Voltage	0	0.4	V	†

† Other platform components may use VID inputs and may require tighter limits.

Table 44 presents VID information.

Table 44. Voltage Identification (VID)

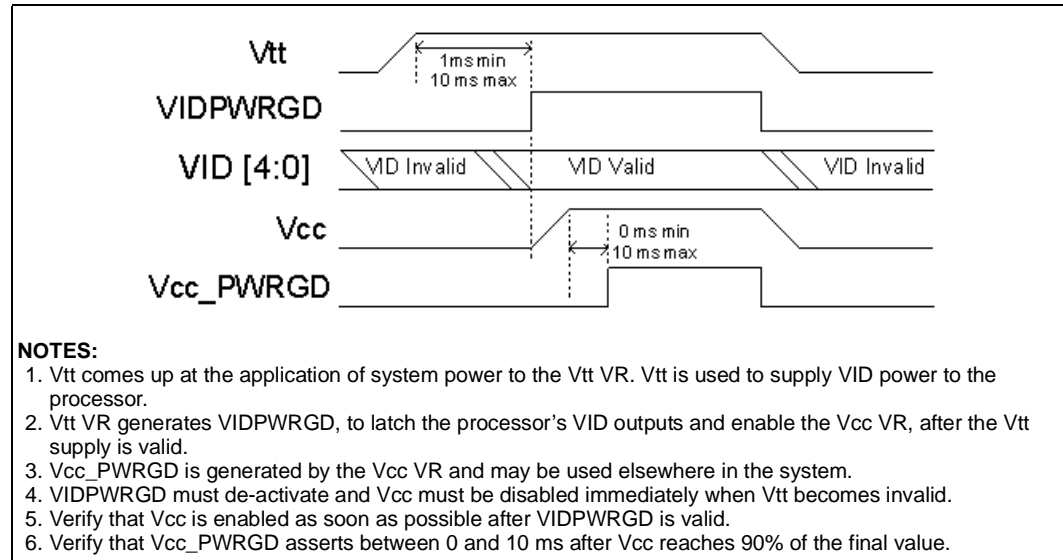
Processor Pins (0 = low, 1 = high)						Vout (V)
VID4	VID3	VID2	VID1	VID0	VID5	
0	1	0	1	0	0	0.8375
0	1	0	0	1	1	0.8500
0	1	0	0	1	0	0.8625
0	1	0	0	0	1	0.8750
0	1	0	0	0	0	0.8875
0	0	1	1	1	1	0.9000
0	0	1	1	1	0	0.9125
0	0	1	1	0	1	0.9250
0	0	1	1	0	0	0.9375
0	0	1	0	1	1	0.9500
0	0	1	0	1	0	0.9625
0	0	1	0	0	1	0.9750
0	0	1	0	0	0	0.9875
0	0	0	1	1	1	1.0000
0	0	0	1	1	0	1.0125
0	0	0	1	0	1	1.0250
0	0	0	1	0	0	1.0375
0	0	0	0	1	1	1.0500
0	0	0	0	1	0	1.0625
0	0	0	0	0	1	1.0750
0	0	0	0	0	0	1.0875
1	1	1	1	1	1	OFF [†]
1	1	1	1	1	0	OFF [†]
1	1	1	1	0	1	1.1000
1	1	1	1	0	0	1.1125
1	1	1	0	1	1	1.1250
1	1	1	0	1	0	1.1375
1	1	1	0	0	1	1.1500
1	1	1	0	0	0	1.1625
1	1	0	1	1	1	1.1750
1	1	0	1	1	0	1.1875
1	1	0	1	0	1	1.2000
1	1	0	0	1	1	1.2125
1	1	0	0	1	0	1.2250
1	1	0	0	0	1	1.2375
1	1	0	0	0	0	1.2500
1	0	1	1	1	1	1.2625
1	0	1	1	1	0	1.2750
1	0	1	1	0	1	1.2875
1	0	1	1	0	0	1.3000
1	0	1	0	1	1	1.3125
1	0	1	0	1	0	1.3250
1	0	1	0	0	1	1.3375
1	0	1	0	0	0	1.3500
1	0	0	1	0	0	1.3625
1	0	0	1	1	1	1.3750
1	0	0	1	1	0	1.3875
1	0	0	1	0	1	1.4000
1	0	0	0	1	0	1.4125
1	0	0	0	0	1	1.4250
1	0	0	0	0	0	1.4375
1	0	0	0	0	1	1.4500
1	0	0	0	0	0	1.4625
0	1	1	1	1	1	1.4750
0	1	1	1	1	0	1.4875
0	1	1	1	0	1	1.5000
0	1	1	1	0	0	1.5125
0	1	1	0	1	1	1.5250
0	1	1	0	1	0	1.5375
0	1	1	0	0	1	1.5500
0	1	1	0	0	0	1.5625
0	1	0	1	1	1	1.5750
0	1	0	1	1	0	1.5875
0	1	0	1	0	1	1.6000

† Output disabled - the same as de-asserting the output enable input.

7.4.5 V_{CC_CORE} Power Sequencing

The VRM/EVRD must support platforms with defined power-up sequences. Figure 63 shows a block diagram of a power sequencing implementation, and Figure 68 shows a timing diagram of the power sequencing requirements.

Figure 68. Power-On Sequence Timing Diagram



7.4.6 Voltage Regulator Design Recommendations

Intel recommends using a VRD 10.0 voltage regulator DC-to-DC converter for processor Vcc core voltage rail. These regulators should be capable of accepting a 5-bit VID code to indicate the voltage required by the individual processor unit. For more information, refer to *Voltage Regulator-Down (VRD) 10.0 Design Guidelines* for the actual specifications. The following section describes some guidelines for the design of the voltage regulator in terms of design topology and component selection. This is done to ensure design and component compatibility.

7.4.7 Decoupling Requirements for the Intel Celeron Processor

For the Intel Celeron processor voltage regulatory circuitry to meet the transient specifications of the Intel Celeron processor, proper bulk and high-frequency decoupling is required. The decoupling requirements for the processor power delivery in this case are presented in [Table 45](#).

Table 45. Decoupling Requirements for the Intel Celeron processor

Capacitance	ESR (each)	ESL (each)	Filter	Notes
(10) AL Polymer 560 μ F	5 mW	4 nH	Output	1
(40) 1206 pkg 22 μ F X5R	3.5 mW	1.4 nH	Output	1, 2
(4) AL Electrolytic 1200 μ F 16 V 2.1 A Ripple	22 mW	30 nH	Input	1
(4) 1206 pkg 4.7 μ F	6 mW	1.1 nH	Input	1

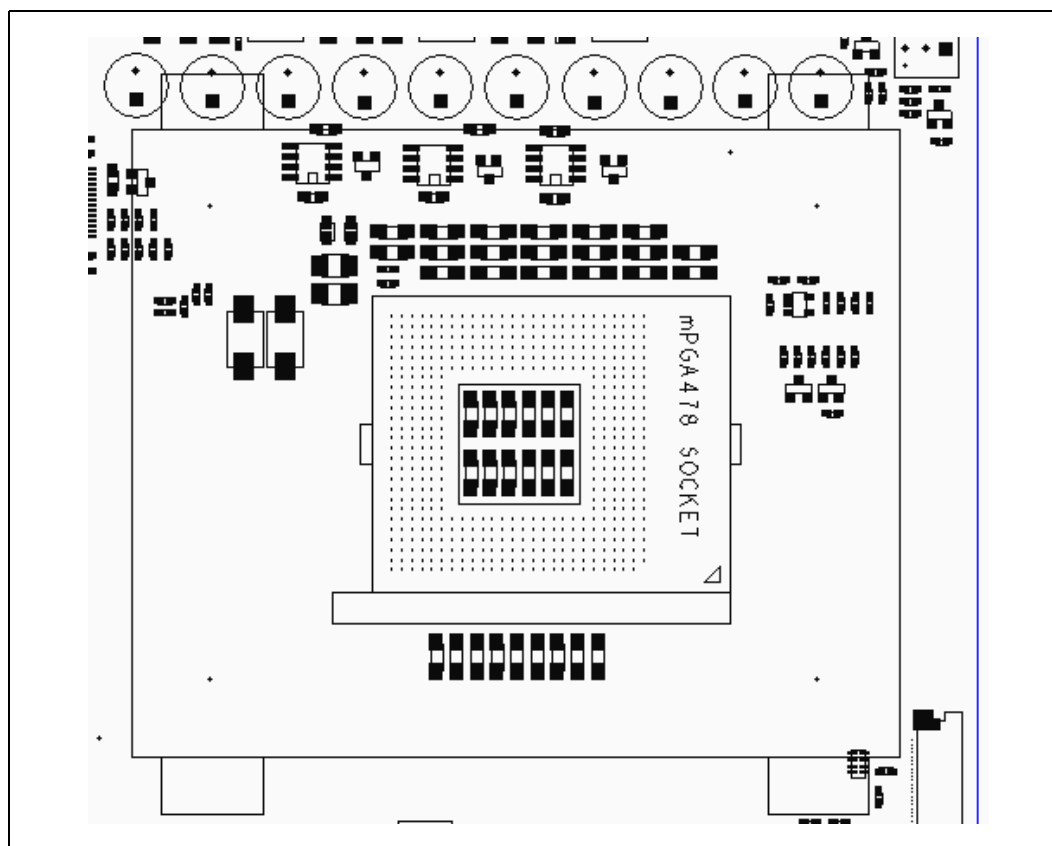
NOTES:

1. The ESR, ESL, and ripple current values in this table are based on the values used in power delivery simulations used by Intel, and they are not vendor specifications.
2. The decoupling should be placed as close as possible to the processor pins. This table details the recommended values, and [Figure 69](#) illustrates the recommended placement. The placement shows sites for (10) AL Polymer capacitors and (40) 1206 package 22 μ F capacitors. The sites are populated as presented in [Table 46](#). The voltage regulator designer should ensure that an adequate amount of decoupling is present such that the circuit meets the processor specifications.

Table 46. Decoupling Location

Type	Number	Location
560 μ F AL Polymer	10	North side of processor, as close as possible to the keep-out area for the retention mechanism.
22 μ F	12	Inside the processor socket cavity; all sites stuffed.
22 μ F	9	West side of the processor, as close to the socket as possible; all sites stuffed.
22 μ F	19	East of processor socket; six sites stuffed.

Figure 69. Decoupling Placement



7.4.8 Layout

In an eight-layer board, two layers should be used for VCC_CPU, and two layers should be used for ground. Traces are not sufficient for supplying power to the processor due to the high current and low resistance required to meet the processor voltage specifications. To satisfy these requirements, shapes that encompass the power delivery part of the processor pin field are required. Figure 70 through Figure 72 show examples of how to use shapes to deliver power to the processor.

The processor socket has 478 pins with 50 mil pitch. The routing of the signals, power and ground pins require creation of many vias. These vias cut up the power and ground planes beneath the processor resulting in increased inductance of these planes. To provide the best path through the via field, Intel recommends that vias be shared for two processor ground pins and for two processor power pins. Figure 73 shows this via sharing.

Figure 70. Top Layer Power Delivery Shape (VCCP)

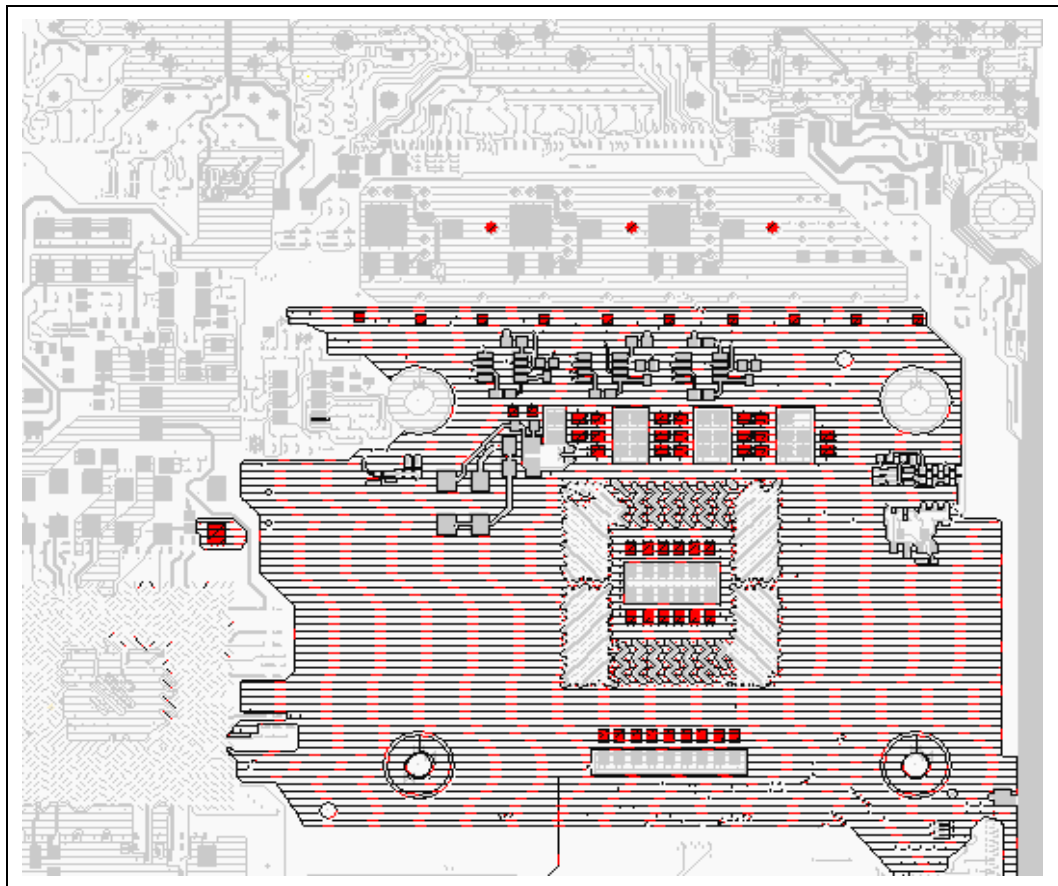


Figure 71. Layer 2 and Layer 7 Power Delivery Shape (VSS)

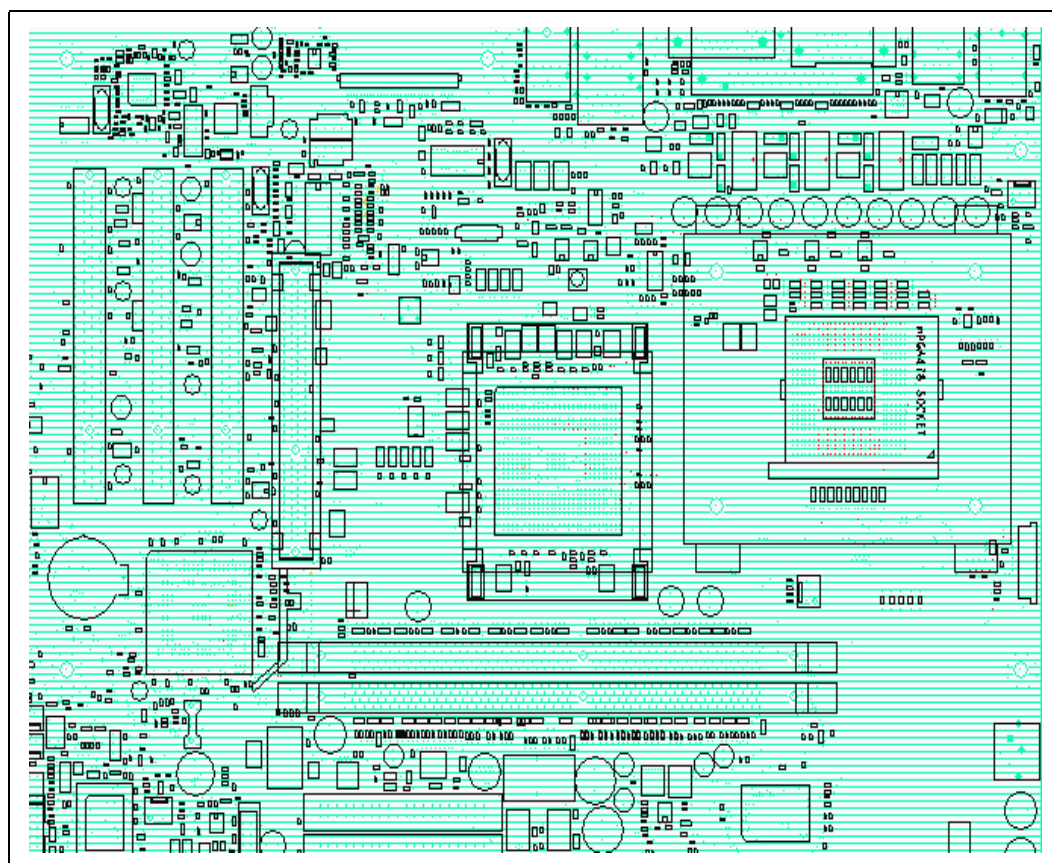


Figure 72. Bottom Layer Power Delivery Shape (VCCP)

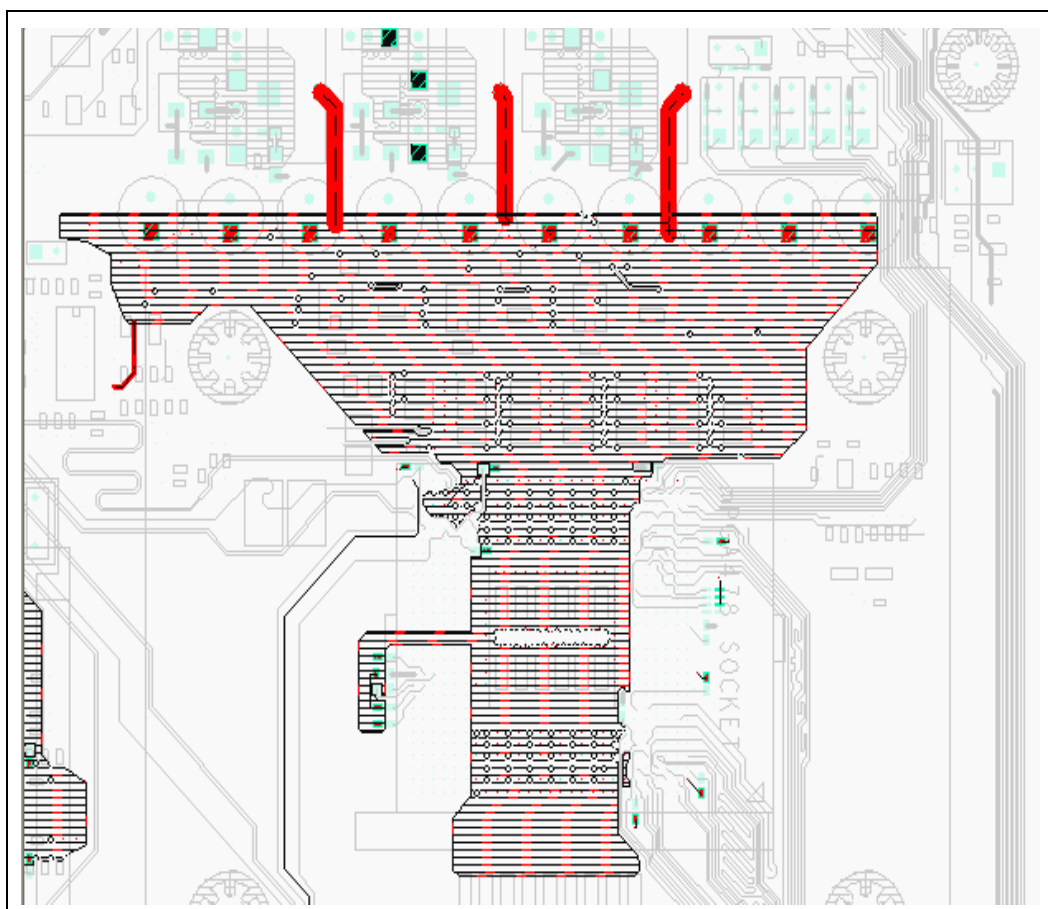
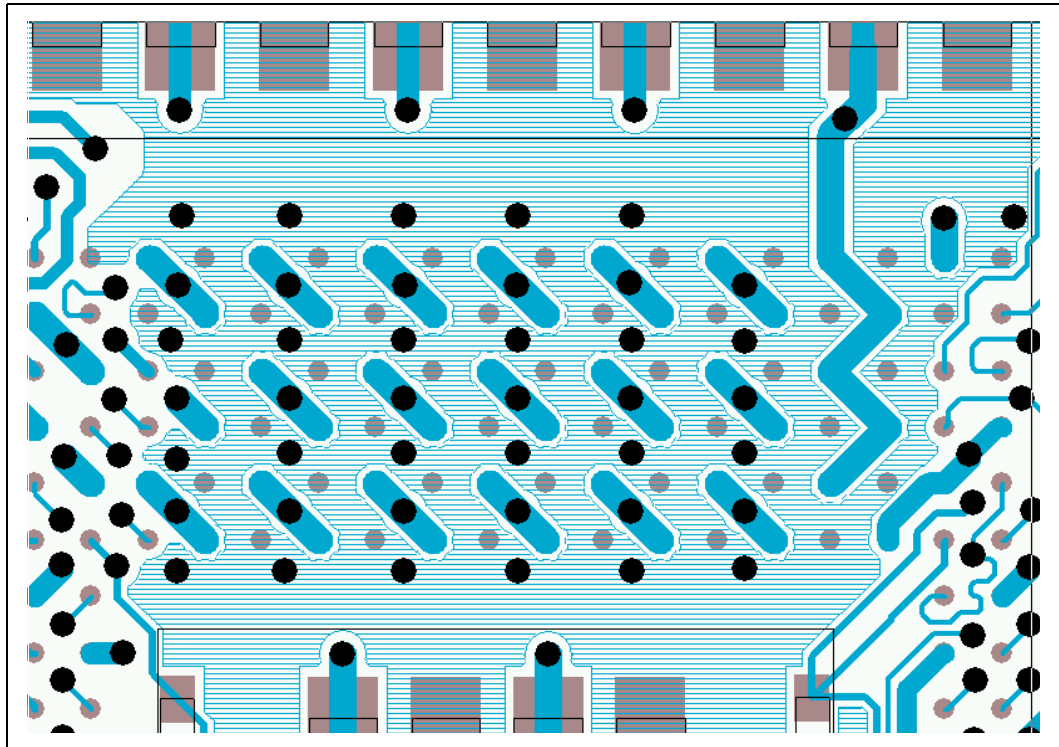


Figure 73. Shared Power and Ground Vias

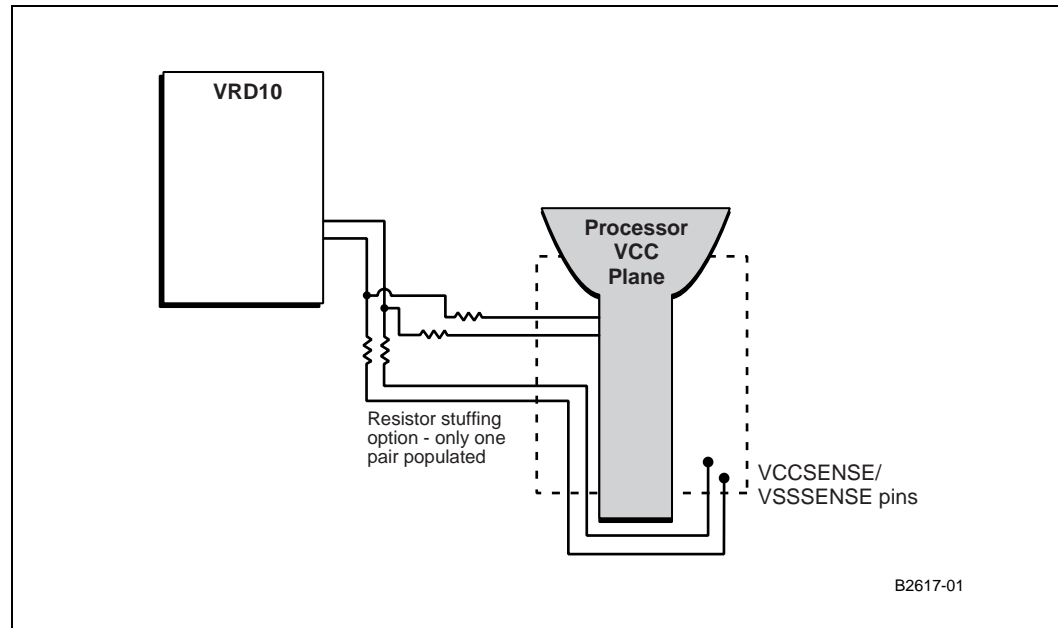


The switching voltage regulators typically used for processor power delivery require the use of the feedback signal for output error correction. Previous 478-pin socket platforms required sensing the voltage regulator feedback from the socket or the system board voltage plane. For this platform using VRD10 controllers, Intel is evaluating whether die sense provides a performance benefit versus socket sense. To provide maximum flexibility for this design, Intel recommends that the system board be routed with an option for both socket feedback and die feedback. This design guide will be updated with the final recommendation for either socket or die sense once the analysis has been completed.

The socket load line defined in the *Voltage Regulator-Down (VRD 10.0) Design Guidelines* is defined at pins AC14 (VCC_CPU) and AC15 (VSS); validate the socket load line from these pins as well. These pins are located approximately in the center of the pin field on the north side of the processor. Connect socket feedback for the voltage regulator controller close to this area of the power delivery shape using wide, low inductive traces. The die loadline is defined at the processor VCC_SENSE and VSS_SENSE pins. Take the die feedback from these pins using wide, low inductive traces.

Four 0 Ω resistors may be used as shown in Figure 74 to create a manufacturing stuffing option to implement either die or socket sense.

Figure 74. Routing of VR Feedback Signals



7.4.9 Thermal Considerations

For a power delivery solution to meet the Flexible PCB (FMB) requirements, it must be able to deliver a fairly high amount of current. This high amount of current also requires that the solution is able to dissipate the associated heat generated by the components and keep all of the components and the PCB within their thermal specifications. It is the responsibility of OEMs to evaluate their component configurations, system airflow, and layout to ensure adequate thermal performance of the processor power delivery solution.

Intel recommends that the system boards be designed to support the full Celeron Processor FMB guidelines. These guidelines include an ICC_MAX electrically for brief time periods. Design the voltage regulator solution to support a minimum of VR_TDC indefinitely within the envelope of operation conditions of the system. The VR_TDC limits of the system board are typically governed by the system board thermal limits. Intel recommends that system boards designed to the above guidelines implement a VR thermal monitor circuit.

The voltage regulator shown is a two-phase solution with four FETs per phase. The layout is optimized to provide adequate thermal relief for the PCB and other components. The voltage regulator thermal performance was validated using the Intel reference heatsink and the boxed processor heatsink in a representative chassis running in a 25° C and 35° C external ambient environment.

The specifications for ICC_MAX of the Celeron Processor are contained in the processor datasheet.

7.4.10 Simulation

To completely model the system board, include the inductance and resistance that exists in the cables, connectors, PCB planes, pins and body of components (such as resistors and capacitors), processor socket, and the voltage regulator module. More detailed models showing these effects are shown in [Figure 75](#).

Figure 75. Detailed Power Distribution Model for Processor with Voltage Regulator on System Board

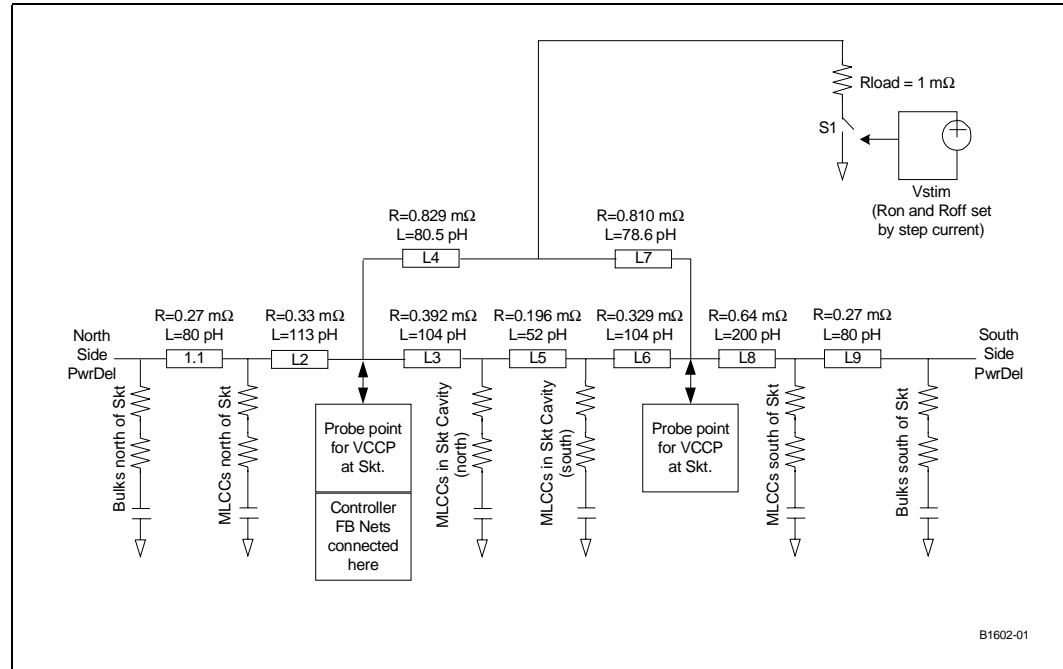


Table 47 lists model parameters for the system board shown in [Figure 75](#).

Table 47. Celeron Processor Power Delivery Model Parameters

Segment	Resistance	Inductance
L1	0.27 mΩ	80 pH
L2	0.33 mΩ	113 pH
L3	0.392 mΩ	104 pH
L4	0.829 mΩ	80.5 pH
L5	0.196 mΩ	52 pH
L6	0.329 mΩ	104 pH
L7	0.810 mΩ	78.6 pH
L8	0.64 mΩ	200 pH
L9	0.27 mΩ	80 pH

7.5 Power Delivery Map

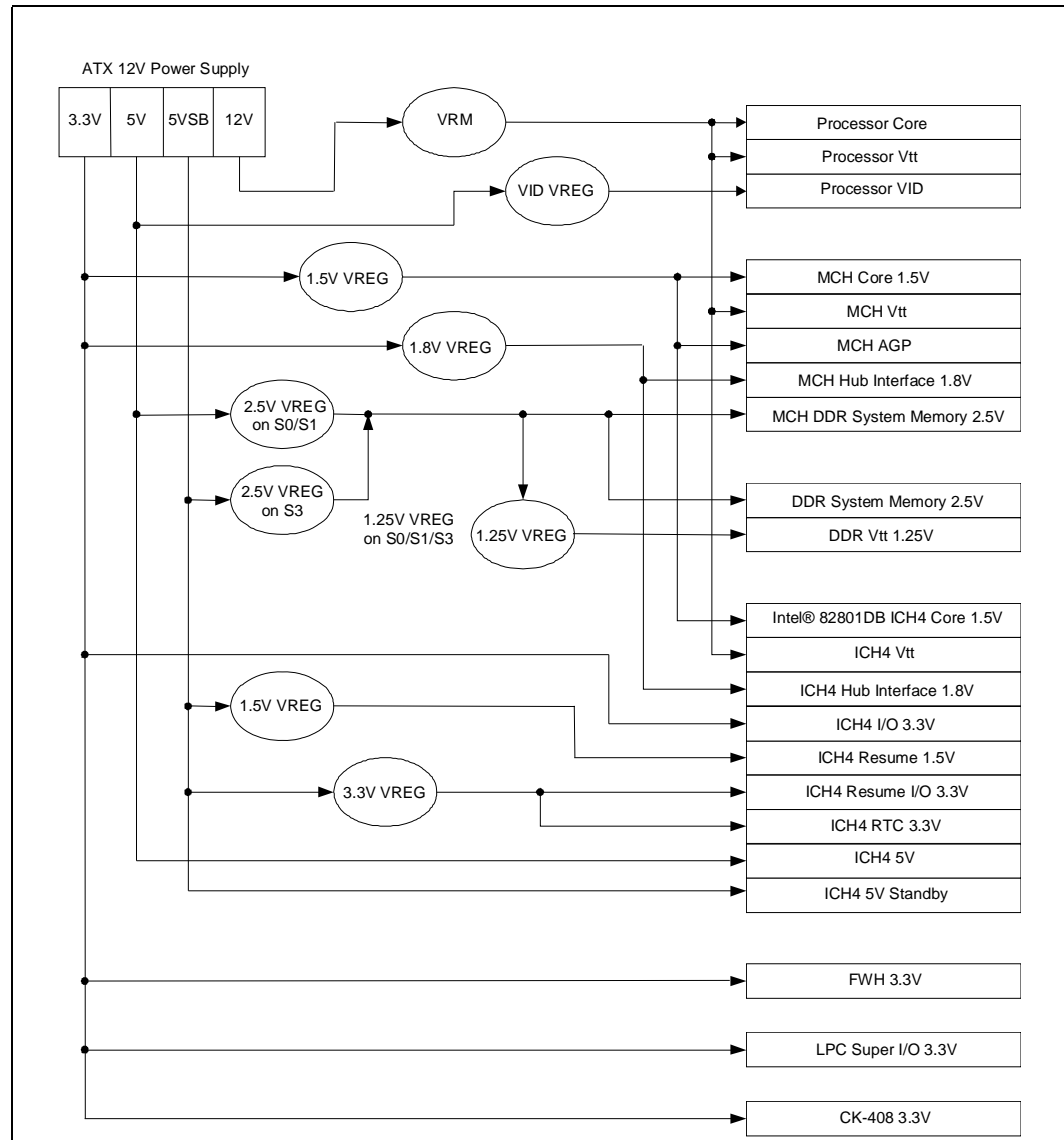
Figure 76 shows the power delivery architecture for an example Intel® 852GM chipset platform.

During STR, only the necessary devices are powered. These devices include: main memory, the ICH4 resume well, PCI wake devices (via 3.3 Vaux), AC'97, and USB. To ensure that enough power is available during STR, complete a thorough power budget. The power requirements should include each device's power requirements, both in suspend and in full-power. Compare the power requirements with the power budget supplied by the power supply. Due to the requirements of main memory and the PCI 3.3 Vaux (and possibly other devices in the system), it is necessary to create dual power rails.

The solutions in this design guide are only examples. Many power distribution methods achieve the similar results. When deviating from these examples, it is critical to consider the effect of a change.

Figure 76 shows the platform power delivery map.

Figure 76. Platform Power Delivery Map





7.6 GMCH/Intel® 82801DB ICH4 Platform Power-Up Sequence

Figure 77 shows the power-on timing sequence for a GMCH/Intel® 82801DB ICH4-based platform.

Figure 77. GMCH/Intel® 82801DB ICH4 Platform Power-Up Sequence

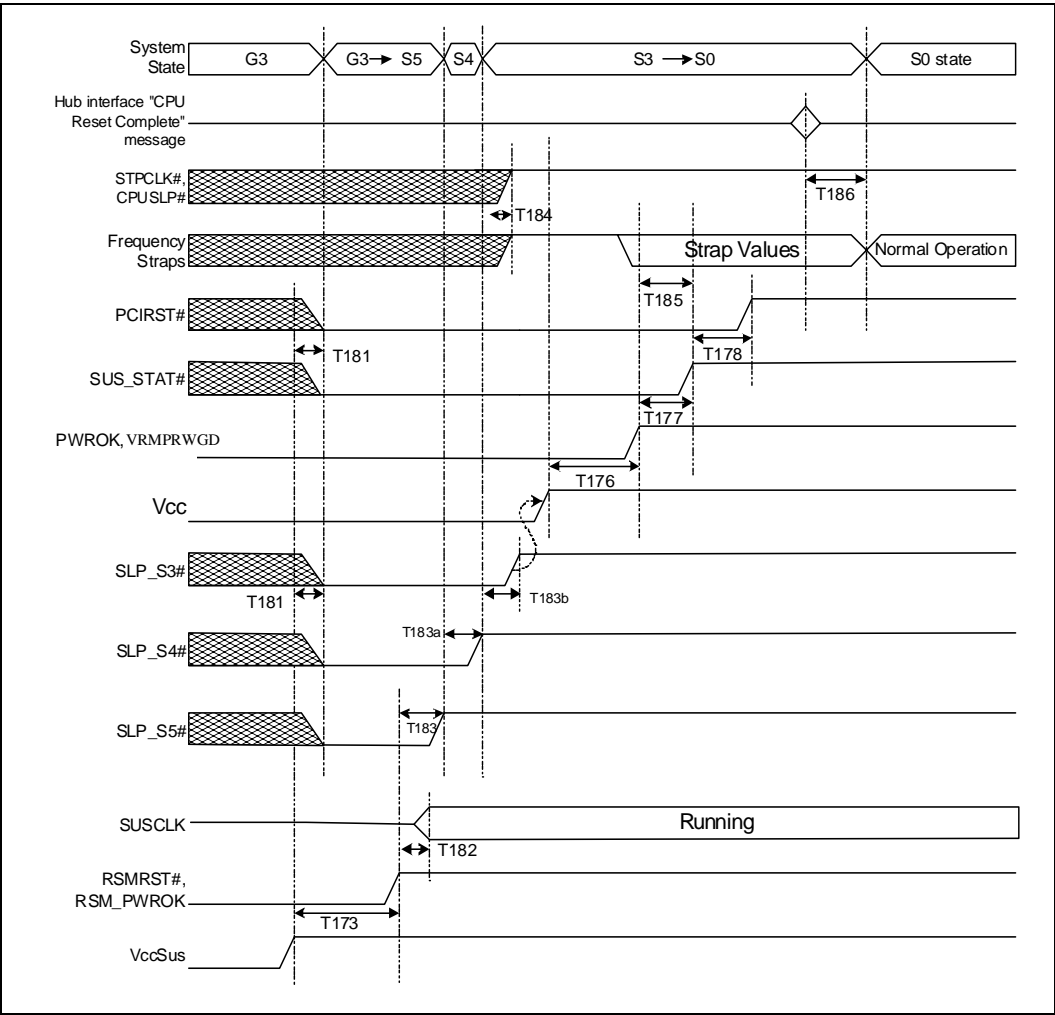


Table 48 presents the timing sequence parameters for Figure 77.

Table 48. Timing Sequence Parameters for Figure 77

Symbol	Description	Min	Max	Units	Notes	Fig
T173	V _{CC} Sus supplies active to RSMRST# inactive.	5	-	ms		Figure 77
T176	V _{CC} supplies active to PWROK, VRMPWRGD active.	10	-	ms		Figure 77
T177	PWROK and VRMPWRGD active and SYS_RESET# inactive to SUS_STAT# inactive.	32	38	RTCCLK		Figure 77
T178	SUS_STAT# inactive to PCIRST# inactive.	1	3	RTCCLK		Figure 77
T181	V _{CC} Sus active to SLP_S5#, SUS_STAT# and PCIRST# active.		50	ns		Figure 77
T182/T183	RSMRST# inactive to SUSCLK running, SLP_S5# inactive.		110	ms	1	Figure 77
T183a	SLP_S5# inactive to SLP_S4# inactive.	1	2	RTCCLK		Figure 77
T183b	SLP_S4# inactive to SLP_S3# inactive.	1	2	RTCCLK		Figure 77
T184	V _{CC} active to STPCLK#, CPUSLP#, STP_CPU#, STP_PCI#, SLP_S1#, C3_STAT# inactive, and CPU Frequency Strap signals high.		50	ns		Figure 77
T185	PWROK and VRMPWRGD active and SYS_RESET# inactive to SUS_STAT# inactive and CPU Frequency Straps latched to strap values.	32	38	RTCCLK	2	Figure 77
T186	CPU Reset Complete to Frequency Straps signals unlatched from strap values.	7	9	CLK66	3	Figure 77

NOTES:

1. When there is no RTC battery in the system, so V_{CC}RTC and the V_{CC}Sus supplies come up together, the delay from RTCRST# and the RSMRST# inactive to SUSCLK toggling may be as much as 1000 ms.
2. These transitions are clocked off the internal RTC. One RTC clock is approximately 32 μ s.
3. This transition is clocked off the 66 MHz CLK66. On4 CLK66 is approximately 15 ns.

Table 49 shows the power on sequencing timing diagram (VR circuitry).

Table 49. Power On Sequencing Timing Diagram (VR Circuitry)

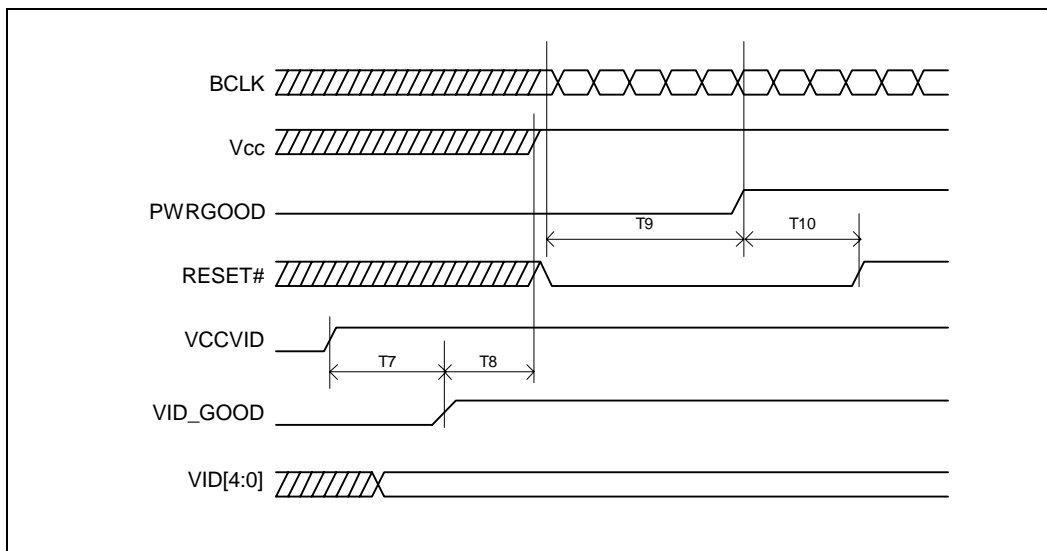


Table 50 presents the timing parameters for Figure 49.

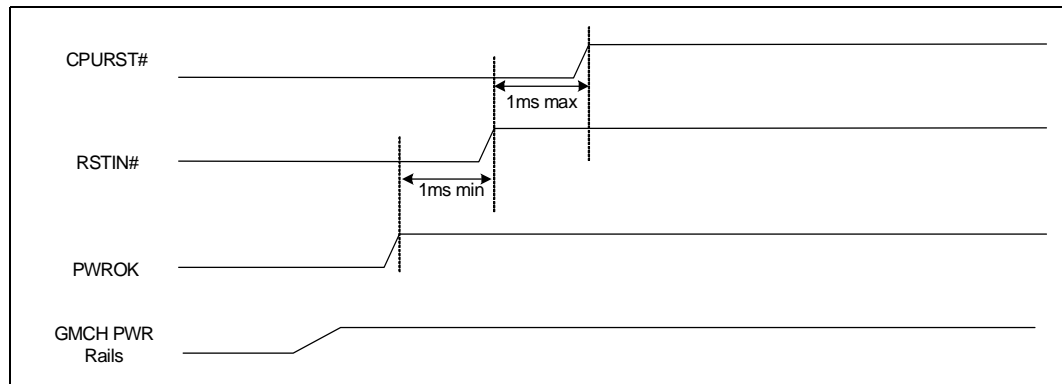
Table 50. Timing Sequence Parameters for Figure 79

Sym	Description	Min	Max	Units	Notes	Fig
T7	V _{CC} VID > 1V to VID_GOOD high	1		us		Figure 49
T8	VID_GOOD to V _{CC} valid maximum time		50	ms		Figure 49
T9	PWRGOOD inactive pulse width	10		BCLKS		Figure 49
T10	PWRGOOD to RESET# deassertion time	1		ms		Figure 49

7.6.1 GMCH Power Sequencing Requirements

All GMCH power rails shall be stable before PWROK is asserted. The power rails may be brought up in any order desired. **However, good design practice would have all GMCH power rails come up as close in time as practical, with the core voltage (1.2 V) coming up first.** RSTIN#, which brings GMCH out of reset, shall be deasserted only after PWROK has been active for 1 ms. After GMCH is out of reset, it deasserts CPURST# within 1 ms.

Figure 78. GMCH Power-up Sequence



7.6.2 ICH4 Power Sequencing Requirements

7.6.2.1 3.3/1.5 V Power Sequencing

The ICH4 has power sequencing requirements for the 3.3 V and 1.5 V rails in respect to each other. This requirement is as follows: The 3.3 V and 1.5 V rails must power up or down simultaneously.

The majority of the ICH4 I/O buffers are driven by the 3.3 V supplies but are controlled by logic powered by the 1.5 V supplies. Therefore, another consequence of faulty power sequencing arises when the 3.3 V supply comes up first. In this case, the I/O buffers may be in an undefined state until the 1.5 V logic is powered up. Some signals that are defined as 'Input-only' actually have output buffers that are normally disabled, and the Intel ICH4 may unexpectedly drive these signals when the 3.3 V supply is active while the 1.5 V supply is not.

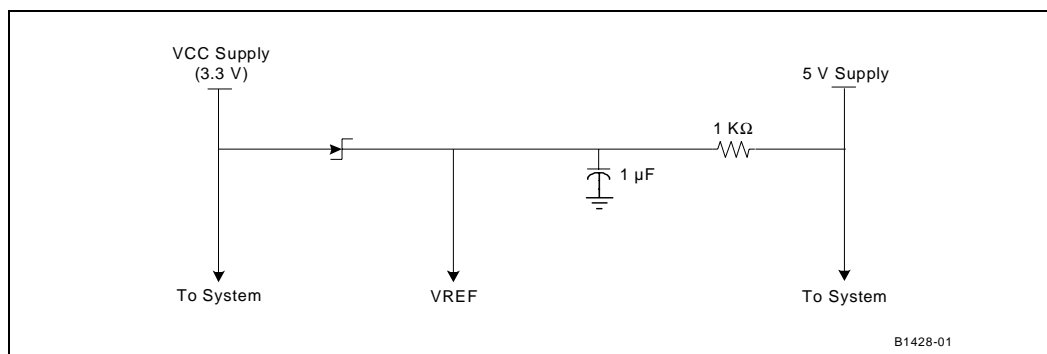
7.6.2.2 V5REF/ V5REFSUS Sequencing

V5REF is the reference voltage for 5 V tolerance on inputs to the ICH4. V5REF must be powered up before V_{CC3_3} , or after V_{CC3_3} within 0.7 V. Also, V5REF must power down after V_{CC3_3} , or before V_{CC3_3} within 0.7 V. These rules must be followed to ensure the safety of the ICH4. When the rule is violated, internal diodes attempt to draw power sufficient to damage the diodes from the V_{CC3_3} rail. Figure 79 shows a sample implementation of how to satisfy the V5REF/ 3.3 V sequencing rule.

This rule also applies to the stand-by rails, but in most platforms, the V_{CCSUS3_3} rail is derived from the V_{CCSUS5} and therefore, the V_{CCSUS3_3} rail always comes up after the V_{CCSUS5} rail. As a result, V5REF_SUS is always powered up before V_{CCSUS3_3} . In platforms that do not derive the V_{CCSUS3_3} rail from the V_{CCSUS5} rail, this rule must be comprehended in the platform design.

Additionally, the ICH4 requires the V5REF_Sus rail to be hooked to a 5 V sustained source. Figure 79 shows an example of V5REF/V5REFSUS sequencing circuitry.

Figure 79. Example V5REF/V5REFSUS Sequencing Circuitry



7.6.2.3 Power Supply PS_ON Consideration

When a pulse on SLP_S3# or SLP5# is short enough (~ 10 – 100 ms) such that PS_ON is driven active during the exponential decay of the power rails, a few power supply designs may not be designed to handle this short pulse condition. In this case, the power supply does not respond to this event and never powers back up. These power supplies would need to be unplugged and plugged back into an outlet to bring the system back up. Power supplies not designed to handle this condition must have their power rails decay to a certain voltage level before they may properly respond to PS_ON. This level varies with affected power supply.

The ATX spec does not specify a minimum pulse width on PS_ON de-assertion, which means power supplies must be able to handle any pulse width. This issue may affect any power supply (beyond ATX) with similar PS_ON circuitry. Due to variance in the decay of the core power rails per platform, a single board or chipset silicon fix would be non-deterministic (may not solve the issue in all cases).

The platform designer must ensure that the power supply used with the platform is not affected by this issue.

7.6.3 GMCH Power Sequencing Requirements

No GMCH power sequencing requirements exist for the Intel® 82852GM GMCH platform. Verify that all GMCH power rails are stable before de-asserting reset, but the power rails may be brought up in any order desired. Good design practice would have all GMCH power rails come up as close in time as practical, with the core voltage coming up first.

The ICH4's CPUPWRGOOD output represents the logical AND of its PWROK and VRMPWRGD inputs. When VRMPWRGD is asserted, it indicates that core power and the PCICLK are stable and PCIRST# will be de-asserted a minimum of 1 ms later. It is the responsibility of the system designers to ensure that the power and timing requirements for the processor and GMCH are met.

7.6.4 DDR Memory Power Sequencing Requirements

No DDR-SDRAM power sequencing requirements are specified during power up or power down if the following criteria are met:

- VDD and VDDQ are driven from a single power converter output.

- VTT is limited to 1.44 V (reflecting $VDDQ(max)/2 + 50\text{ mV}$ VREF variation + 40 mV VTT variation)
- VREF tracks $VDDQ/2$
- A minimum resistance of 42 Ω (22 Ω series resistor + 22 Ω parallel resistor $\pm 5\%$ tolerance) limits the input current from the VTT supply into any pin.

When the above criteria cannot be met by the system design, [Table 51](#) must be adhered to during power up. Refer to *Intel® DDR 200 JEDEC Spec Addendum* for more details.

Table 51. DDR Power-Up Initialization Sequence

Voltage Description	Sequencing	Voltage Relationship to Avoid Latch-up
VDDQ	After or with VDD	$< VDD + 0.3\text{ V}$
VTT	After or with VDDQ	$< VDDQ + 0.3\text{ V}$
VREF	After or with VDDQ	$< VDDQ + 0.3\text{ V}$

7.6.4.1 VTT Rail Power Down Sequencing During Suspend

The VTT termination voltage for the DDR bus must not be turned off until all populated rows of memory have been placed into power down mode through the deassertion of the SCKE signals. After all rows of memory are powered off, the VTT termination voltage may be removed. During entry into suspend and during suspend, VTT must not glitch. VTT must not be turned off until after the deassertion of the SCKE signals.

The voltage supplied to SMVREF, VREF, and SMRCOMP may also be removed once all rows of memory are powered off and SCKE must not glitch during entry into suspend and during suspend. Power to these pins must not be turned off until after the deassertion of the SCKE signals.

7.6.4.2 VTT Rail Power Up Sequencing During Resume

During resume from the S3 state, the reverse sequencing of the power rails and control signals must occur to ensure a smooth exit from suspend. The VTT termination voltage must be supplied and steady before the system begins exit from suspend. VTT must not glitch during resume. SMVREF, VREF, and SMRCOMP also need to be supplied and valid before the assertion of the SCKE signals. These reference voltages and resistive compensation are necessary in order for the GMCH and the memory devices to recognize the valid assertion of SCKE. SCKE must not glitch during resume and must rise monotonically.

VTT and VREF to the DIMMs and SMVREF and SMRCOMP to the GMCH must all be up and stable before the deassertion of PCIRST#.

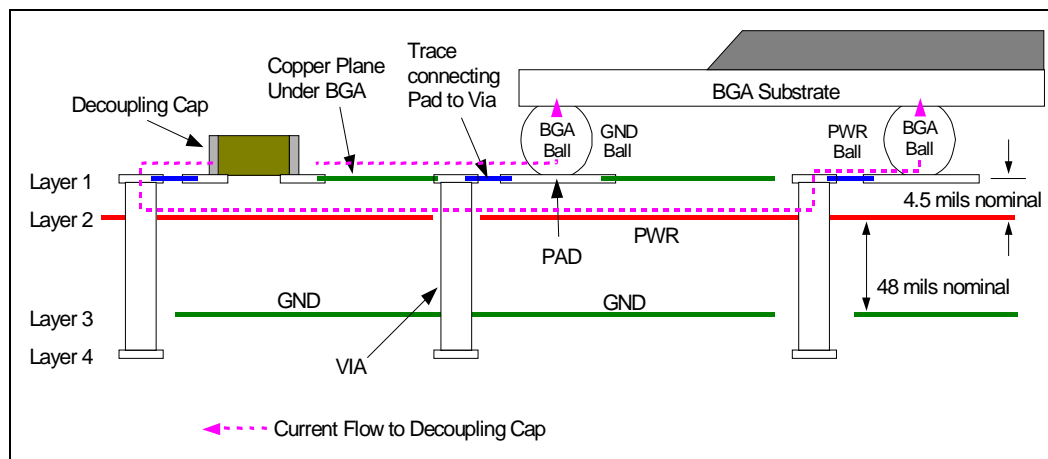
7.7 Intel® 852GM Chipset Platform Power Delivery Guidelines

Each component is capable of generating large current swings when switching between logic high and logic low. This condition could cause the component voltage rails to drop below specified limits. To avoid this type of situation, ensure that the appropriate amount of bulk capacitance is added in parallel to the voltage input pins. Intel recommends that the developer use the amount of decoupling capacitors specified in this document to ensure the component maintains stable supply

voltages. Place the capacitors as close to the package as possible. Rotate caps that set over power planes so that the loop inductance is minimized (see Figure 80). The basic theory for minimizing loop inductance is to consider which voltage is on Layer 2 (power or ground) and spin the decoupling cap with the opposite voltage toward the BGA (Ball Grid Array). This greatly minimizes the total loop inductance. Intel recommends that for prototype board designs, the designer should include pads for extra power plane decoupling caps.

Figure 80 shows an example for minimizing loop inductance.

Figure 80. Example for Minimizing Loop Inductance



7.7.1 Processor Decoupling Guidelines

Contact your Intel Field Representative for the details on the Mobile Intel Celeron processor with IMVP-III voltage regulator. Also refer to the *Mobile Intel Celeron Processor on 0.13 Micron Process and in Micro-FCPGA Package Datasheet* for details.

Contact your Intel Field Representative for the details on the Intel Celeron M processor with IMVP-IV voltage regulator. Also refer to the *Intel Celeron M Processor Datasheet* for more details.

See Section 7.4.7, “Decoupling Requirements for the Intel Celeron Processor” on page 122 for details on the Intel Celeron processor with VRD 10.0 voltage regulator. Also refer to the *Intel Celeron Processor on 0.13 Micron Process in the 478-Pin Package Datasheet* for more details.

7.7.2 Intel® 82852GM GMCH Decoupling Guidelines

Bulk decoupling is based on the VR solution used on the board design. [Table 52](#) presents the minimum GMCH decoupling requirements.

Table 52. Intel® 82852GM GMCH Decoupling Recommendations

Pin Name	Configuration	F	Qty	Type	Notes
V _{CC}	Tie to V _{CC1_2S}	0.1 µF 10 µF 150 µF	4 1 2	XR7, 0603, 16 V, 10% XR5, 1206, 6.3 V, 20% SPC, E, 6.3 V, 20%	1 X 0.1 µF with in 200mils 3 X 0.1 µF on bottom side
VTTLF	Tie to V _{CCP}	0.1 µF 10 µF 150 µF	2 1 1	XR7, 0603, 16 V, 10% XR5, 1206, 6.3 V, 20% SPC, E, 6.3 V, 20%	2 X 0.1 µF on bottom side
VTTHF	Tie to Ground	0.1 µF	5	XR7, 0603, 16 V, 10%	
V _{CC} HL	Tie to V _{CC1_2S}	0.1 µF 10 µF	2 1	XR7, 0603, 16 V, 10% XR5, 1206, 6.3 V, 20%	1 X 0.1 µF with in 200 mils 1 X 0.1 µF on bottom side
V _{CC} SM	Tie to V _{CC2_5}	0.1 µF 100 µF	11 2	XR7, 0603, 16 V, 10% TANT, D, 10 V, 20%	10 X 0.1 µF with in 200 mils 1 X 0.1 µF on bottom side
V _{CC} DVO	Tie to V _{CC1_5S}	0.1 µF 10 µF 150 µF	2 1 1	XR7, 0603, 16 V, 10% XR5, 1206, 6.3 V, 20% SPC, E, 6.3 V, 20%	1 X 0.1 µF with in 200 mils 1 X 0.1 µF on bottom side
V _{CC} DLVDS	Tie to V _{CC1_5S}	0.1 µF 22 µF 47 µF	1 1 1	XR7, 0603, 16 V, 10% TANT, B, 10 V, 20% TANT, D, 10 V, 20%	1 X 0.1 µF with in 200 mils
V _{CC} TXLVDS	Tie to V _{CC} Sus2_5	0.1 µF 22 µF 47 µF	3 1 1	XR7, 0603, 16 V, 10% TANT, B, 10 V, 20% TANT, D, 10 V, 20%	1 X 0.1 µF with in 200 mils 2 X 0.1 µF on bottom side
V _{CC} GPIO	Tie to V _{CC3_3S}	0.1 µF	1	XR7, 0603, 16 V, 10%	
SMVREF		0.1 µF	1	XR7, 0603, 16 V, 10%	1 X 0.1 µF on bottom side
SMVSWINGL		0.1 µF	1	XR7, 0603, 16 V, 10%	
SMVSWINGH		0.1 µF	1	XR7, 0603, 16 V, 10%	
HDRVREF		220 pF 1 µF	3 3	XR7, 0603, 25 V, 10% XR5, 0603, 6.3 V, 20%	
HAVREF		0.1 µF	1	XR7, 0603, 16 V, 10%	
HCCREF		0.1 µF	1	XR7, 0603, 16 V, 10%	
HXVSWING		0.1 µF	1	XR7, 0603, 16 V, 10%	

7.7.3 GMCH V_{CCSM} Decoupling

Every GMCH ground and V_{CCSM} power ball in the system memory interface should have its own via. For the V_{CCSM} pins of the GMCH, a minimum of eleven 0603 form factor 0.1 μ F high frequency capacitors is required and must be placed within 150 mils of the GMCH package. Distribute the eleven capacitors evenly along the GMCH DDR system memory interface and they must be placed perpendicular to the GMCH with the power (2.5 V) side of the capacitors facing the GMCH. The trace from the power end of the capacitor should be as wide as possible and it must connect to a 2.5 V power ball on the outer row of balls on the GMCH. Each capacitor should have their 2.5 V via placed directly over and connected to a separate 2.5 V copper finger, and they should be as close to the capacitor pad as possible, within 25 mils. The ground end of the capacitors must connect to the ground flood and to the ground plane through a via. Place this via as close to the capacitor pad as possible, within 25 mils with as thick a trace as possible.

7.7.4 DDR SDRAM VDD Decoupling

Discontinuities in the DDR signal return paths occur when the signals transition between the PCB and the DIMMs. To account for this ground to 2.5 V discontinuity, a minimum of nine 0603 form factor 0.1 μ F high-frequency bypass capacitors are required between the DIMMs to help minimize any anticipated return path discontinuities that are created. Distribute the capacitors as evenly as possible between the two DIMMs.

- Connect the wide ground trace from each capacitor to a via that transitions to the ground plane. Place each ground via as close to the ground pad as possible.
- Connect the wide 2.5 V trace from each capacitor to a via that transitions to the 2.5 V copper flood. Place each via as close to the capacitor pad as possible. Connect each capacitor pad to the closest 2.5 V DIMM pin on either the first or second DIMM connector with a wide trace.

7.7.5 DDR VTT Decoupling Placement and Layout Guidelines

The VTT termination rail must be decoupled using high-speed bypass capacitors, one 0603 form factor, 0.1 μ F capacitor and one 0603 form factor, 0.01 μ F capacitor per four DDR signals. They must be placed no more than 100 mils from the termination resistors.

- A VTT copper flood must be used. The decoupling capacitors must be spread out across the termination island so that all the parallel termination resistors are near high-frequency capacitors.
- Place each capacitor ground via as close to the capacitor pad as possible, within 25 mils with as thick a trace as possible.

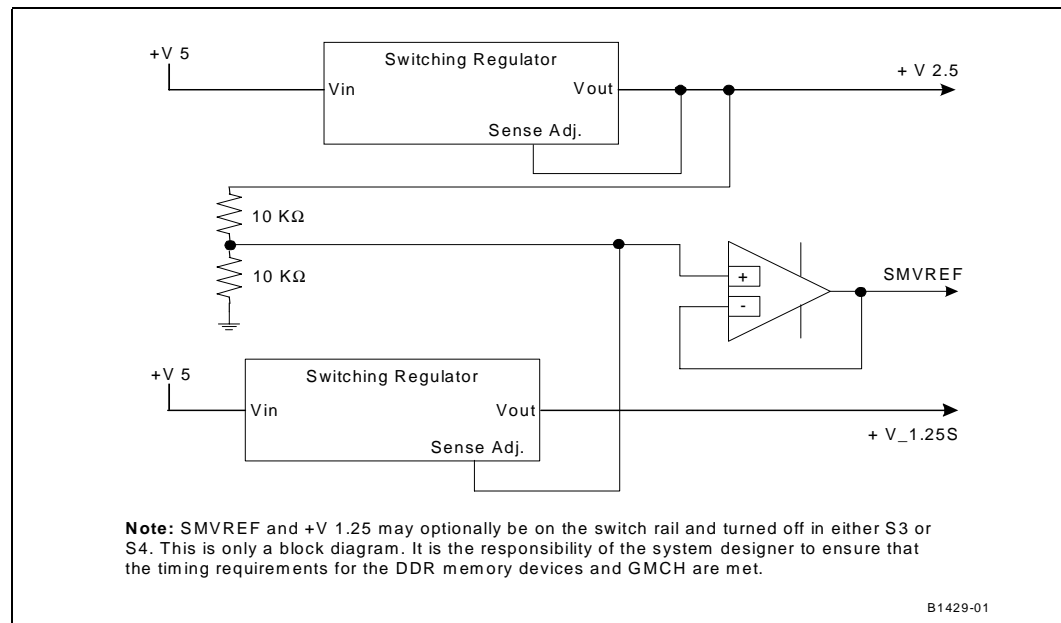
7.7.6 DDR Power Delivery Design Guidelines

The main focus of these GMCH guidelines is to minimize signal integrity problems and improve the power delivery to the GMCH system memory interface and the DDR memory DIMMs. This section discusses the DDR memory system voltage and current requirements as determined at publishing of this document. This document is not the original source for these guidelines. Figure 81 shows the implementation of 2.5 V, 1.25 V and SMVREF on the board only as an example. It is the responsibility of the system designer to ensure that the power requirements for the DDR and GMCH are met. Refer to the following documents for the latest details on voltage and current requirements found in this design guide.

- *Double Data Rate (DDR) SDRAM Specification*, JEDEC Standard, JESD79
- *Intel DDR 20 JEDEC Spec Addendum*, Rev 0.9 or later

Figure 81 shows the DDR power delivery block diagram.

Figure 81. DDR Power Delivery Block Diagram



7.7.6.1 2.5 V Power Delivery Guidelines

The 2.5 V power for the GMCH system memory interface and the DDR DIMMs is delivered around the DDR command, control, and clock signals. Special attention must be paid to the 2.5 V copper flooding to ensure proper GMCH and DIMM power delivery. This 2.5 V flood must extend from the GMCH 2.5 V power vias all the way to the 2.5 V DDR voltage regulator and its bulk capacitors. The 2.5 V DDR voltage regulator must connect to the 2.5 V flood with a minimum of six vias. The DIMM connector 2.5 V pins as well as the GMCH 2.5 V power vias must connect to the 2.5 V copper flood.

In the areas where the copper flooding necks down around the GMCH make sure to keep these neck down lengths as short as possible. The 2.5 V copper flooding under the DIMM connectors must encompass all the DIMM 2.5 V pins and must be solid except for the small areas where the clocks are routed within the DIMM pin field to their specified DIMM pins.

Maintain a minimum of 12 mil isolation spacing between the copper flooding and any signals on the same layer.

Table 53 shows the voltage and current specifications for each the GMCH and memory reference and termination voltages. For convenience, tolerances are given in both percent and volts, although validation should be done using the specifications exactly as they are written. When the spec states a tolerance in terms of volts (for example, VREF states ± 0.025 V), use that specific voltage tolerance, not a percentage of the measured value. Likewise, use percentages where stated.

As presented in the following tables, only the 2.5 V supply has an absolute specification. The 1.25 V supply for both VREF and VTT need to track the 2.5 V supply closely.

Table 53 presents the DDR SDRAM memory supply voltage and current specification.

Table 53. DDR SDRAM Memory Supply Voltage and Current Specification

Name	VDD	VDDQ	VREF	Description
Purpose	Core Supply Voltage	I/O Supply Voltage	I/O Reference Supply Voltage	
Specification Definition	VDD	VDDQ	$VREF = (Vdd/2) \pm 0.050$ V	$((2.5 \text{ V} \pm 8\%) / 2) \pm 0.050$ V
Voltage Nominal (V)	2.500	2.500	1.250	
Tolerance ($\pm\%$)	8.0%	8.0%	4.0%	
Tolerance (\pm V)	0.200	0.200	0.050	
Max Absolute Spec Value (V)	2.700	2.700	1.400	$((2.5 \text{ V} + 8\%) / 2) + 0.050$ V
Min Absolute Spec Value (V)	2.300	2.300	1.100	$((2.5 \text{ V} - 8\%) / 2) - 0.050$ V
MAX RELATIVE SPEC	NA	NA	$(\text{measured } Vdd/2) + 0.050$ V	Calculated from measured V_{CCSM} value.
MIN RELATIVE SPEC	NA	NA	$(\text{measured } Vdd/2) - 0.050$ V	Calculated from measured V_{CCSM} value.
	$I_{DD} (\text{max})$	$I_{DDQ} (\text{max})$	$I_{REF} (\text{max})$	
Absolute Maximum Current Requirements (A)	5.000	0.920	0.001	

Table 54 presents the GMCH system memory supply voltage and current specification.

Table 54. GMCH System Memory Supply Voltage and Current Specification

Name	V _{CCSM}	SMVREF	VTT = SMRCOMP	Description
Purpose	GMCH DDR Supply Voltage (I/O)	GMCH Reference Supply Voltage	SMRCOMP Termination Supply Voltage	
Definition	V _{CCSM}	SMVREF = (V _{CCSM} /2) ± 2%	VTT = (Vref) ± 0.040V	((2.5V ± 5%) / 2) ± 0.050V ± 0.040V
Voltage Nominal	2.500 V	1.250 V	1.250 V	
Tolerance	± 5.0%	± 2.0%	± 3.2%	
Tolerance	± 0.125	± 0.025	± 0.040	
Max Absolute Spec Value	2.625 V	1.339 V	1.440 V	((2.5V + 5%) / 2) + 0.050V + 0.040V
Min Absolute Spec Value	2.375 V	1.164 V	1.060 V	((2.5V - 5%) / 2) - 0.050V - 0.040V
Max Relative Spec	NA	(Measured V _{CCSM} /2) + 2%	(Measured Vref) + 0.04V	Calculated from measured V _{CCSM} value.
Min Relative Spec	NA	(Measured V _{CCSM} /2) - 2%	(Measured Vref) - 0.040V	Calculated from measured V _{CCSM} value.
	I _{VCCSM} (max)	I _{SMVREF} (max)	I _{TTRC} (max)	
Absolute Maximum Current Requirements	1.900 A	0.00005A 5	0.040A	

Table 55 presents the termination voltage and current specifications.

Table 55. Termination Voltage and Current Specifications

Name	VTT	Description
Purpose	Termination Supply Voltage, Static	
Definition	Vtt = (Vref) ± 0.040V	((2.5 V ± 8%) / 2) ± 0.050V ± 0.040V
Voltage Nominal (V)	1.250	
Tolerance (+/-%)	3.2%	
Tolerance (+/-V)	0.040	
Max Absolute Spec Value (V)	1.440	((2.5V + 8%) / 2) + 0.050V + 0.040V
Min Absolute Spec Value (V)	1.060	((2.5V - 8%) / 2) - 0.050V - 0.040V
Max Relative Spec	(Measured Vref) + 0.040V	Calculated from measured V _{CCSM} value.
Min Relative Spec	(Measured Vref) - 0.040V	Calculated from measured V _{CCSM} value.
	I _{TT} (max)	
Absolute Maximum Current Requirements (A)	2.400	

7.7.6.2 GMCH and DDR SMVREF Design Recommendations

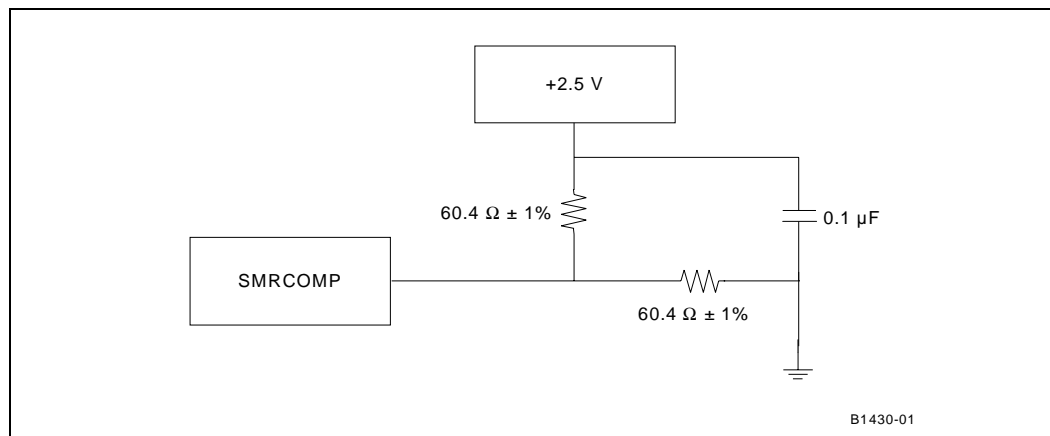
There is one SMVREF pin on the GMCH that is used to set the reference voltage level for the DDR system memory signals (SMVREF). The voltage level that needs to be supplied to this pin must be equal to $V_{CCSM}/2$. As shown in Figure 79, Intel recommends the use of an OpAmp buffer to generate SMVREF from the 2.5 V supply. This should be used as the VREF signals to both the DDR memory devices and the SMVREF signal to the GMCH.

7.7.6.3 DDR SMRCOMP Resistive Compensation

The GMCH requires a system memory compensation resistor, SMRCOMP, to adjust buffer characteristics to specific board and operation environment characteristics. Refer to Figure 82 for details on resistive compensation. The SMRCOMP signal should be routed with as wide a trace as possible. It should be a minimum of 12 mils wide and be isolated from other signals with a minimum of 10 mils spacing.

Figure 82 shows the GMCH SMRCOMP resistive compensation.

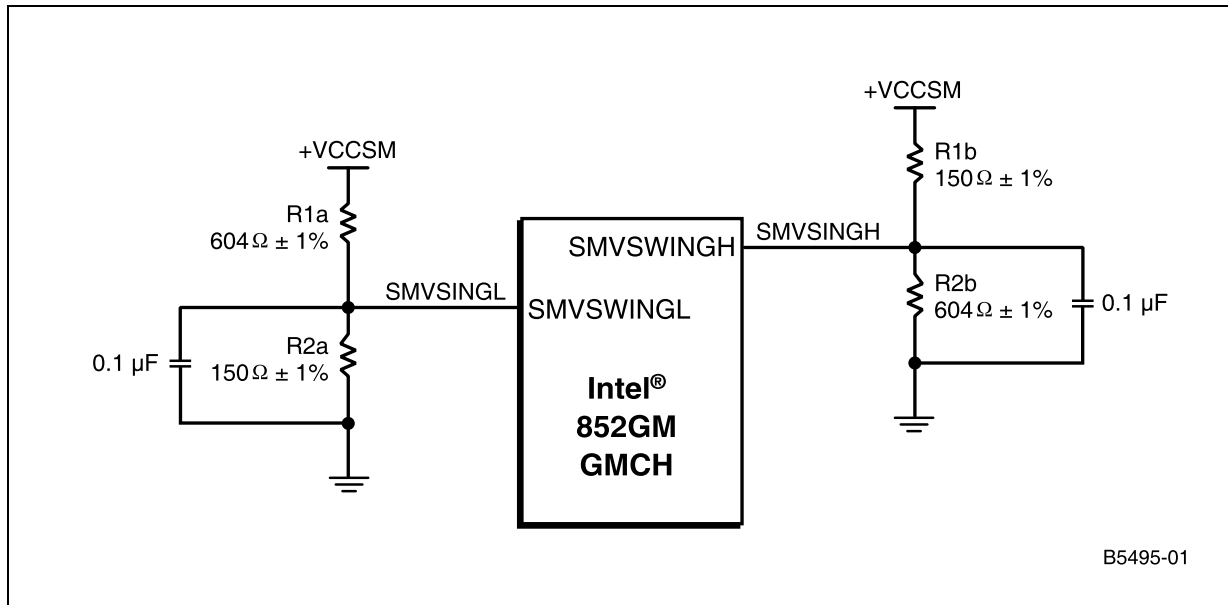
Figure 82. GMCH SMRCOMP Resistive Compensation



The GMCH's system memory resistive compensation mechanism also requires the generation of reference voltages to the SMVSWINGL and SMVSWINGH pins. The schematic for SMVSWINGL and SMVSWINGH voltage generation is illustrated in Figure 83. Two resistive dividers with $R1b = R2a = 150 \Omega \pm 1\%$ and $R1a = R2b = 604 \Omega \pm 1\%$ generate the SMVSWINGL and SMVSWINGH voltages. SMVSWINGL and SMVSWINGH components should be placed within 0.5 inch of their respective pins and connected with a 15 mil wide trace. To avoid coupling with any other signals, maintain a minimum of 25 mils of separation to other signals.

Figure 83 shows the GMCH system memory reference voltage generation circuit.

Figure 83. GMCH System Memory Reference Voltage Generation Circuit



7.7.6.4 DDR VTT Termination

The recommended topology for DDR-SDRAM Data, Control, and Command signal groups requires that all these signals to be terminated to a 1.25 V source, VTT, at the end of the memory channel opposite the GMCH. It is recommended that this VTT be generated from the same source as used for V_{CCSM} , and not be used for GMCH and DDR SMVREF. This is because SMVREF has a much tighter tolerance and VTT may vary more easily depending on signal states. A solid 1.25 V termination island should be used to for this purpose and be placed on the surface signal layer, just beyond the last DIMM connector and must be at least 50 mils wide. The data and command signals should be terminated using one resistor per signal. Resistor packs and $\pm 5\%$ tolerant resistors are acceptable for this application. Only signals from the same DDR signal group may share a resistor pack. See [Section 9](#) for system memory guidelines.

7.7.6.5 DDR SMRCOMP, SMVREF and VTT 1.25 V Supply Disable in S3/Suspend

Regardless of how these 1.25 V supplies for GMCH are generated, they may be disabled during the S3 suspend state to further save power on the platform. This is possible because the GMCH does not require a valid reference voltage nor does it require the enabling of resistive compensation during suspend. However, some DDR memory devices may require a valid reference voltage during suspend. It is the responsibility of the system designer to ensure that requirements of the DDR memory devices are met.

The 2.5 V V_{CCSM} power pins of the GMCH and the VDD power pins of the DDR memory devices do need to be on in S3 state.

7.7.7 Other GMCH Reference Voltage and Analog Power Delivery

7.7.7.1 GMCH GTLVREF

For GMCH, the GTLVREF generation circuit has been broken down into three separate voltage references: host data reference voltage (HDVREF[2:0]), host address reference voltage (HAVREF) and host common clock reference voltage (HCCVREF). Maximum length from pin to voltage divider for each reference voltage should be less than 0.5 inch. Intel recommends traces that are ten mil wide. GMCH VREF may be maintained as individual voltage dividers as shown in Figure 84, Figure 85, and Figure 86.

Figure 84 shows the GMCH HDVREF[2:0] reference voltage generation circuit.

Figure 84. GMCH HDVREF[2:0] Reference Voltage Generation Circuit

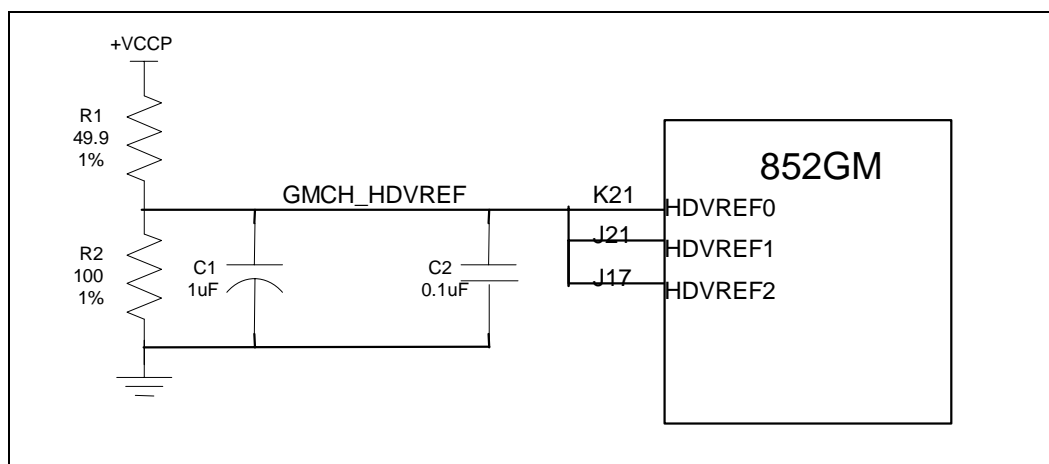


Figure 85 shows the GMCH HAVREF reference voltage generation circuit.

Figure 85. GMCH HAVREF Reference Voltage Generation Circuit

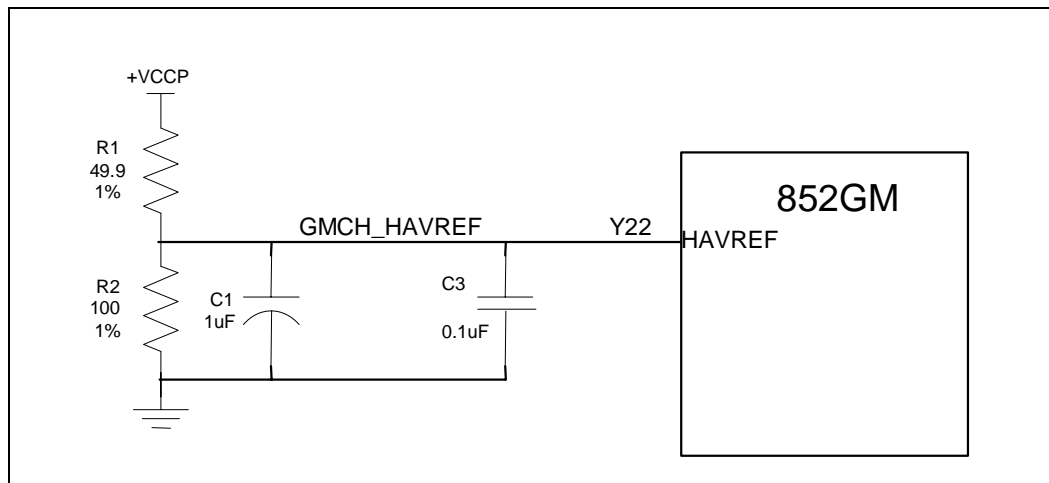
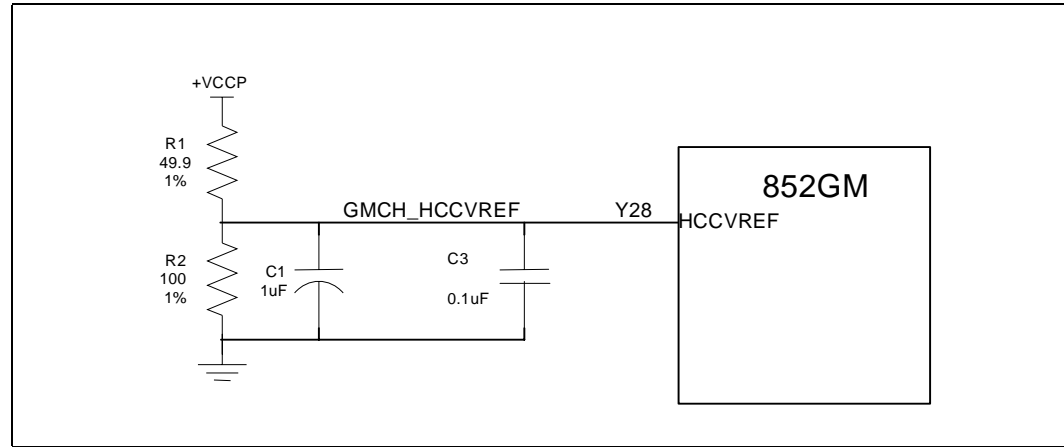


Figure 86 shows the GMCH HCCVREF reference voltage generation circuit.

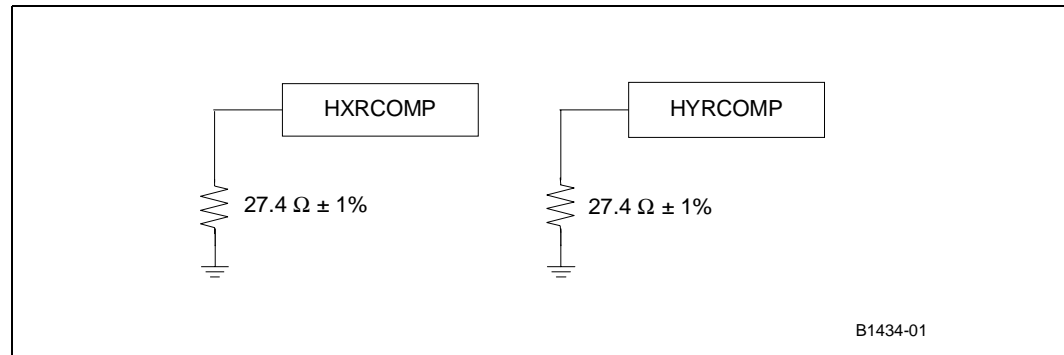
Figure 86. GMCH HCCVREF Reference Voltage Generation Circuit



7.7.7.2 GMCH AGTL+ I/O Buffer Compensation

The HXRCOMP and HYRCOMP pins of the GMCH should each be pulled-down to ground with a $27.4 \Omega \pm 1\%$ resistor (see Figure 87). The maximum trace length from pin to resistor should be less than 0.5 inch and should be 18 mils wide to achieve the $Z_0 = 27.4 \Omega$ target. Also, the routing for HRCOMP should be at least 25 mils away from any switching signal.

Figure 87. GMCH HXRCOMP and HYRCOMP Resistive Compensation

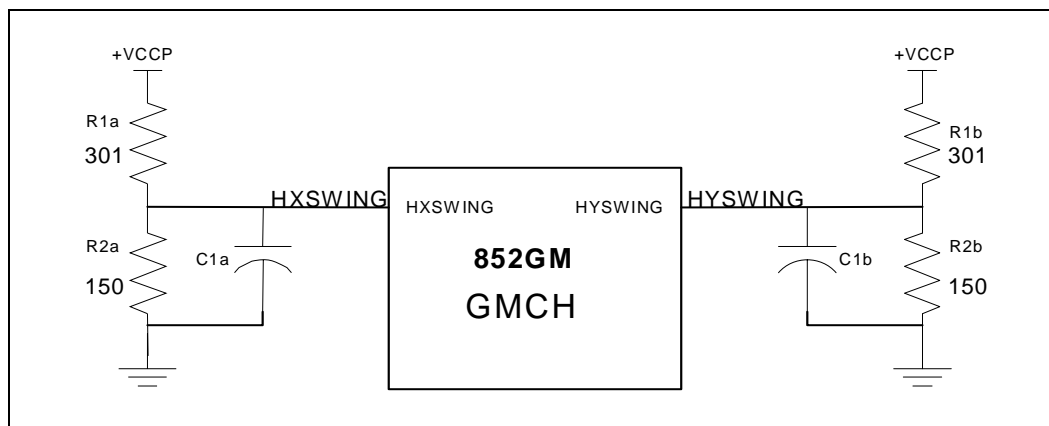


7.7.7.3 GMCH AGTL+ Reference Voltage

The GMCH's AGTL+ I/O buffer resistive compensation mechanism also requires the generation of reference voltages to the HXSWING and HYSWING pins with a value of $1/3 * V_{CCP}$. Implementations for HXSWING and HYSWING voltage generation are illustrated in Figure 88. Two resistive dividers with $R1a = R1b = 301 \Omega \pm 1\%$ and $R2a = R2b = 150 \Omega \pm 1\%$ generate the HXSWING and HYSWING voltages. $C1a = C1b = 0.1 \mu F$ act as decoupling capacitors and connect HXSWING and HYSWING to V_{CC_CORE} . HSWING components should be placed within 0.5 inch of their respective pins and connected with a 15 mil wide trace. To avoid coupling with any other signals, maintain a minimum of 25 mils of separation to other signals.

Figure 88 shows the GMCH HXSWING and HYSWING reference voltage generation circuit.

Figure 88. GMCH HXSWING and HYSWING Reference Voltage Generation Circuit



7.7.7.4 GMCH Analog Power

Table 56 summarizes the eight analog circuits that require filtered supplies on the Intel 82852GM GMCH. The analog circuits are: VCCASM, VCCQSM, VCCAHPDLL, VCCADPLLA, VCCADPLLB, VCCADAC, VCCAGPLL, and VCCALVDS.

VCCADAC, VCCAHPDLL, VCCAGPLL, and VCCALVDS do not require an RLC filter but do require decoupling capacitors. Figure 89 shows an example analog supply filter.

Figure 89. Example Analog Supply Filter

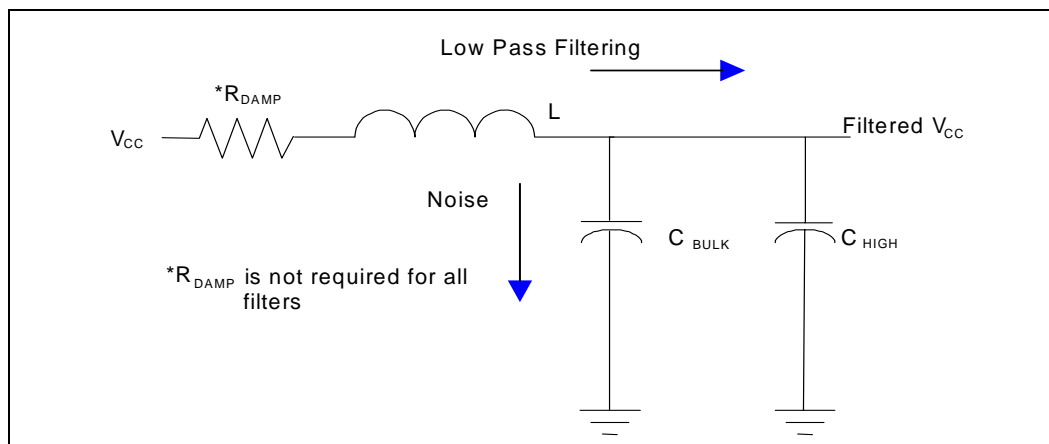




Table 56 presents the analog supply filter requirements.

Table 56. Analog Supply Filter Requirements

Required 852GM Chipset Filters	R_{DAMP}	R_{DAMP} Location	L	C_{BULK}	C_{HIGH}
VCCASM	None	N/A	1210 1 μ H DCRmax 0.169 Ω s	100 μ F	0603 0.1 μ F X5R
VCCQSM	1 Ω	In series with capacitor	0805 0.68 μ H DCRmax 0.80 Ω s	1206 4.7 μ F X5R	0603 0.1 μ F X5R
VCCAHPLL	None	N/A	None	None	0603 0.1 μ F X5R
VCCADPLLA	1 Ω	In series with inductor	0805 0.10 μ H	220 μ F	0603 0.1 μ F X5R
VCCADPLLB	1 Ω	In series with inductor	0805 0.10 μ H	220 μ F	0603 0.1 μ F X5R
VCCADAC	None	N/A	None	None	0603 0.1 μ F X5R 0603 0.01 μ F X5R
VCCAGPLL	None	N/A	None	None	0603 0.1 μ F X5R
VCCALVDS	None	N/A	None	None	0603 0.1 μ F X5R

7.7.8 Intel® 82801DB ICH4 Decoupling/Power Delivery Guidelines

7.7.8.1 ICH4 Decoupling

The ICH4 is capable of generating large current swings when switching between logic high and logic low. This condition could cause the component voltage rails to drop below specified limits. To avoid this type of situation, ensure that the appropriate amount of decoupling capacitance is added in parallel to the voltage input pins. Intel recommends that the developer use the amount of high-frequency decoupling capacitors specified in table below to ensure that component maintains stable supply voltages. Low-frequency decoupling is dependent on layout and system power supply design. Table 57 presents the ICH4 decoupling requirements.

Table 57. Intel® 82801DB ICH4 Decoupling Requirements

Pin	Decoupling Requirements	Decoupling Type (Ball type)	Decoupling Placement
VCC3_3	(6) 0.1 μ F	Decoupling Cap (Vss)	Place near balls: A4, A1, H1, T1, AC10, and AC18
VCCSUS3_3	(2) 0.1 μ F	Decoupling Cap (Vss)	Place near balls: A22 and AC5
V_CPU_IO	(1) 0.1 μ F	Decoupling Cap (Vcc)	Place near ball: AA23
VCC1_5	(2) 0.1 μ F	Decoupling Cap (Vss)	Place near balls: K23 and C23
VCCSUS1_5	(2) 0.1 μ F	Decoupling Cap (Vss)	Place near balls: A16 and AC1
V5REF	(1) 0.1 μ F	Decoupling Cap (Vcc)	Place near ball: E7
V5_REF_SUS	(1) 0.1 μ F	Decoupling Cap (Vss)	Place near ball: A16
VCCRTC	(1) 0.1 μ F	Decoupling Cap (Vcc)	Place near ball: AB5
VCCHI	(2) 0.1 μ F	Decoupling Cap (Vss)	Place near balls: T23 and N23
VCCPLL	(1) 0.1 μ F (1) 0.01 μ F	Decoupling Cap (Vcc)	Place near ball: C22

NOTE: Place capacitors less than 100 mils from the package.

7.8 Clock Driver Power Delivery Guidelines

Special care must be taken to provide a quiet VDDA supply to the Ref VDD, VDDA, and the 48 MHz VDD. These VDDA signals are especially sensitive to switching noise induced by the other VDDs on the clock chip. They are also sensitive to switching noise generated elsewhere in the system such as the CPU VRM. Design the CLC pi-filter to provide the best reasonable isolation. Intel recommends that a solid ground plane be underneath the clock chip on Layer 2 (assuming top trace is Layer 1). Intel also recommends that a ground flood be placed directly under the clock chip to provide a low impedance connection for the VSS pins.

For ALL power connections to planes, decoupling capacitors and vias, use the MAXIMUM trace width allowable and shortest possible lengths to ensure lowest possible inductance. The decoupling capacitors should be connected as shown in Figure 90, taking care to connect the VDD pins directly to the VDD side of the capacitors. However, the VSS pins should not be connected directly to the VSS side of the capacitors. Instead, connect them to the ground flood under the part that is viaed to the ground plane. This is done to avoid VDD glitches propagating out and getting coupled through the decoupling capacitors to the VSS pins. This method has been shown to provide the best clock performance.

The ground flood should be viaed through to the ground plane with no less than 12 to 16 vias under the part and ensure that it is well connected. For all power connections, use heavy duty and/or dual vias. It is imperative that the standard signal vias and small traces not be used for connecting decoupling capacitors and ground floods to the power and ground planes. Generate VDDA by using a CLC pi-filter. Connect this VDDA to the VDD side of the three capacitors that require it, using a significant trace on the top layer. Route this trace from the CLC pi-filter using a star topology.

7.8.1 CK-408 Clock Driver Decoupling

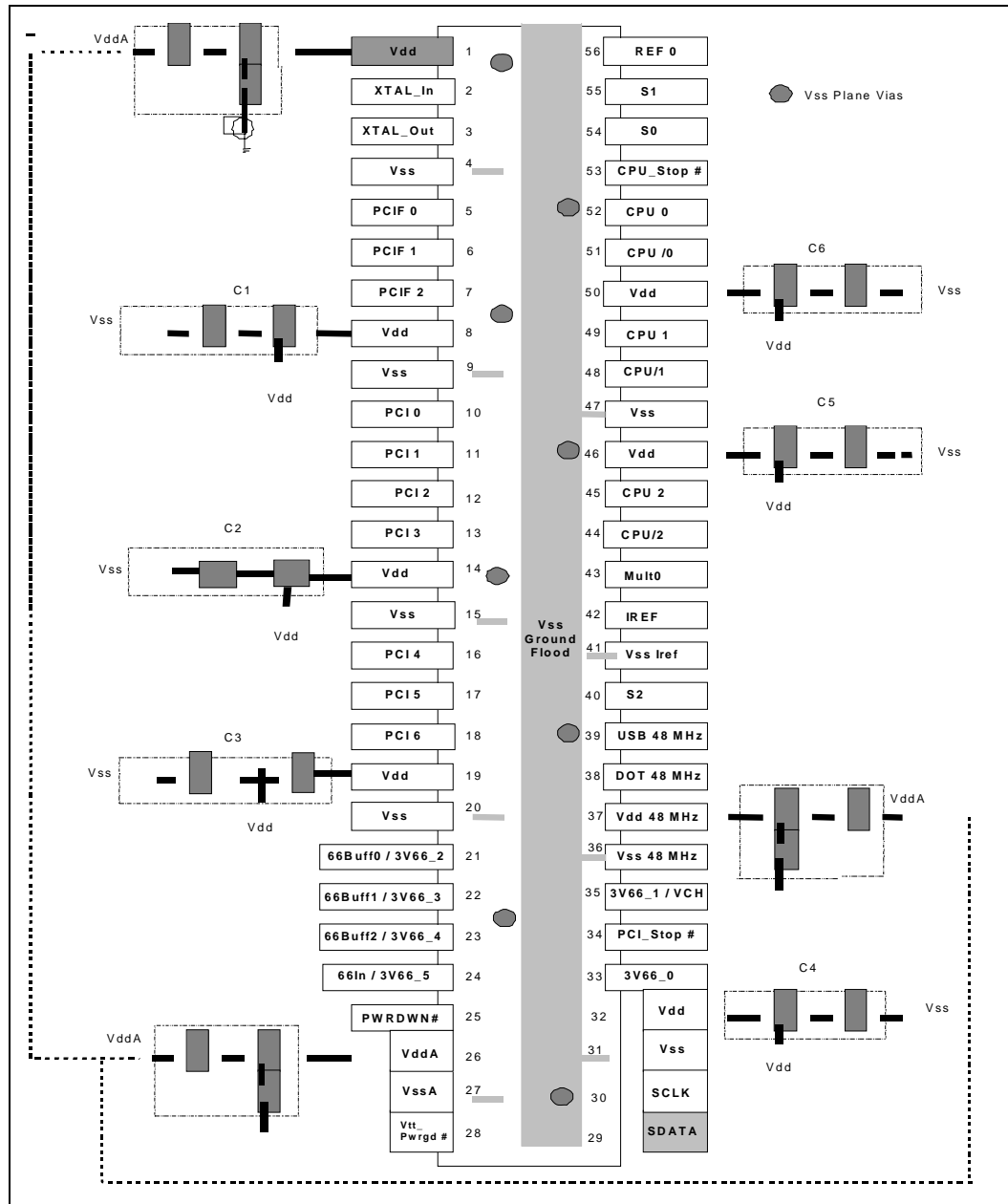
When connecting the decoupling caps, connect the VDD pins directly to the VDD side of the caps. However, the VSS pins should not be connected directly to the VSS side of the caps. Instead, they should be connected to the ground flood under the part that is viaed to the ground plane. This is done to avoid VDD glitches propagating out and getting coupled through the decoupling caps to the VSS pins. This method has been shown to provide the best clock performance.

The decoupling requirements for a CK-408 compliant clock synthesizer are as follows:

- One 10 μ F bulk decoupling cap in a 1206 package placed close to the VDD generation circuitry.
- Six 0.1 μ F high frequency decoupling caps in a 0603 package placed close to the VDD pins on the CK-408.
- Three 0.1 μ F high frequency decoupling caps in a 0603 package placed close to the VDDA pins on the CK-408.
- One 10 μ F bulk decoupling cap in a 1206 package placed close to the VDDA generation circuitry.

Figure 90 shows the placement and connectivity for decoupling capacitors.

Figure 90. Placement and Connectivity for Decoupling Capacitors



7.8.2 Hub Interface Decoupling

See [Section 10.3.4](#) for details.

7.8.3 FWH Decoupling

Place a 0.1 μ F capacitor between the VCC supply pins and the VSS ground pins to decouple high-frequency noise, which may affect the programmability of the device. The value of the low-frequency bulk decoupling capacitor is dependent on board layout and system power supply design.

7.8.4 General LAN Decoupling

- All VCC pins should be connected to the same power supply.
- All VSS pins should be connected to the same ground plane.
- Four to six decoupling capacitors, including two 4.7 μ F capacitors are recommended.
- Place decoupling as close as possible to power pins.

7.9 Thermal Design Power

For information on the ICH4 thermal design, refer to the *Intel® I/O Controller Hub 4 (ICH4) Thermal Design Guidelines*.

Integrated Graphics Display Port

8

The GMCH has three dedicated display ports:

- Analog RAMDAC port
- Dedicated LVDS port
- 12-bit Digital Video Out port, DVOC.

Section 8.1 discusses the CRT and RAMDAC routing requirements. Section 8.2 discusses the dedicated LVDS port. Section 8.3 discusses the DVOC design guideline. Section 8.4 provides recommendations for a flexible modular design guideline for DVOC muxed interfaces. Section 8.5 provides recommendations for the GPIO signal group.

8.1 Analog RGB/CRT Guidelines

8.1.1 RAMDAC/Display Interface

The GMCH integrated graphics/chipset design interfaces to an analog display using a RAMDAC. The RAMDAC is a subsection of the graphics controller display engine and consists of three identical 8-bit digital-to-analog converter (DAC) channels, one for the display's red, green, and blue electron guns.

Each RGB output is doubly terminated with a 75 Ω resistor: One 75 Ω resistor is connected from the DAC output to the board ground, and the other termination resistor exists within the display. The equivalent DC resistance at the output of each DAC is 37.5 Ω . The current output from each DAC flows into this equivalent resistive load to produce a video voltage, without the need for external buffering. There is also an LC pi-filter on each channel that is used to reduce high-frequency noise and to reduce EMI. To maximize performance, the filter impedance, cable impedance, and load impedance should be matched.

Since the DAC runs at speeds up to 350 MHz, special attention should be paid to signal integrity and EMI, RGB routing, component placement, component selection, and cable and load impedance (monitor). They all play a large role in the analog display's quality and robustness. This holds true for all resolutions, but especially for those at 1600 x 1200 resolutions or higher.

8.1.2 Reference Resistor (REFSET)

A reference resistor, REFSET, is used to set the reference current for the DAC. This resistor is an external resistor with a 1% tolerance that is placed on the circuit board. A reference resistor may be selected from a range between 124 Ω to 137 Ω (1%). Based on board design, DAC RGB outputs may be measured when the display is completely white. When the RGB voltage value is between 665 mV and 770 mV, the video level is within VESA specification and the resistor value that was chosen is optimal for board design.

Use this formula to calculate the value of REFSET.

$$REFSET = \frac{V_{reference}}{I_{reference}} = \frac{V_{bg}/4}{32 \cdot 73.2\mu A}$$

Intel recommends using a 137 Ω , one percent resistor for REFSET. See [Figure 92](#) for Intel's recommended REFSET resistor placement.

A reference voltage is generated on the GMCH from a bandgap voltage reference circuit. The bandgap reference voltage level is approximately 1.2 V and this voltage is divided by four to generate the reference voltage. The VESA video standard defines the LSB current for each DAC channel. The RAMDAC reference current is designed on-die to be equal to 32LSB.

8.1.3 RAMDAC Board Design Guidelines

Take care when routing the analog RAMDAC signals. This is especially true to successfully support high display resolution where pixel frequency may be as high as 350 MHz. Intel recommends that each analog R, G, B signal be routed single-endedly. The analog RGB signals should be routed with an impedance of 37.5 Ω . Intel recommends that these routes be routed on an inner routing layer and that it be shielded with VSS planes, if possible. Spacing between DAC channels and to other signals should be maximized; Intel recommends 20-mil spacing. The RGB signals require pi filters that should be placed near the VGA connector. It consists of two 3.3 pF caps with a 75 Ω ferrite bead at 100 MHz between them. The RGB signals should have a 75 Ω , one percent terminating pull-down resistor. The complement signals (R#, G#, and B#) should be grounded to the ground plane.

Intel recommends that the pi filter and terminating resistors be placed as close as possible to the VGA connector. After the 75 Ω termination resistor, the RGB signals routing to the pi-filters and the VGA connector *should ideally be routed with 75 Ω impedance (~ 5 mil traces), or as close to 75 Ω impedance as possible.*

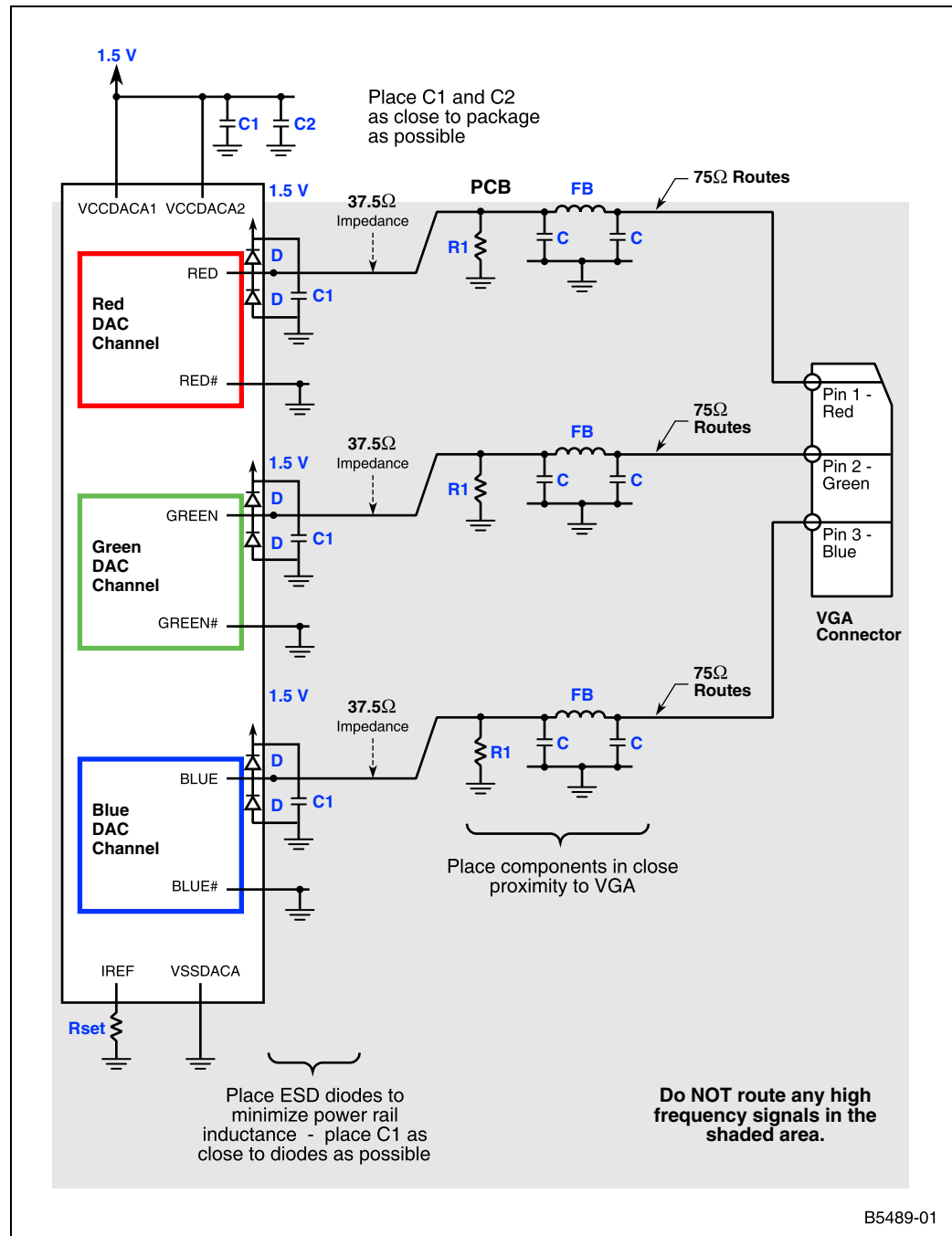
The RGB signals also require protection diodes between 1.5 V and ground. These diodes should have low C ratings (~5 pF max) and small leakage current (~ 10 mA at 120° C) and should be properly decoupled with a 0.1 μ F cap. These diodes and decoupling should be placed to minimize power rail inductance. The choice between diodes (or diode packs) should comprehend the recommended electrical characteristics in addition to cost.

The RGB signals should be length matched as closely as possible (from the Intel 852GM GMCH to VGA connector) and should not exceed 200 mils of mismatch.

8.1.4 Intel® 852GM Chipset RAMDAC Routing Guidelines

Figure 91 illustrates the Intel 852GM chipset RAMDAC routing guidelines.

Figure 91. Intel® 852GM chipset RAMDAC Routing Guidelines



The RAMDAC channel (red, green, blue) outputs are routed as single-ended shielded current output routes that are terminated prior to connecting to the video PI-filter and VGA connector.
Table 58 presents Intel's recommended Intel 852GM RAMDAC components.

Table 58. Recommended Intel® 852GM RAMDAC Components

Recommended DAC Board Components				
Component	Value	Tolerance	Power	Type
R1	75 Ω	1 %	1/16 W	SMT, Metal Film
REFSET	137 Ω	1 %	1/16 W	SMT, Metal Film
C1	0.1 μ F	20 %	-----	SMT, Ceramic
C2	0.01 μ F	20 %	-----	SMT, Ceramic
C	3.3 pF	10 %	-----	SMT, Ceramic
D	PAC DN006	-----	350 mW	California Micro Devices – ESD diodes for VGA SOIC package Or equivalent diode array
FB	75 Ω @ 100 MHz	-----	-----	MuRata* BLM11B750S

Figure 92 illustrates the REFSET placement.

Figure 92. REFSET Resistor Placement

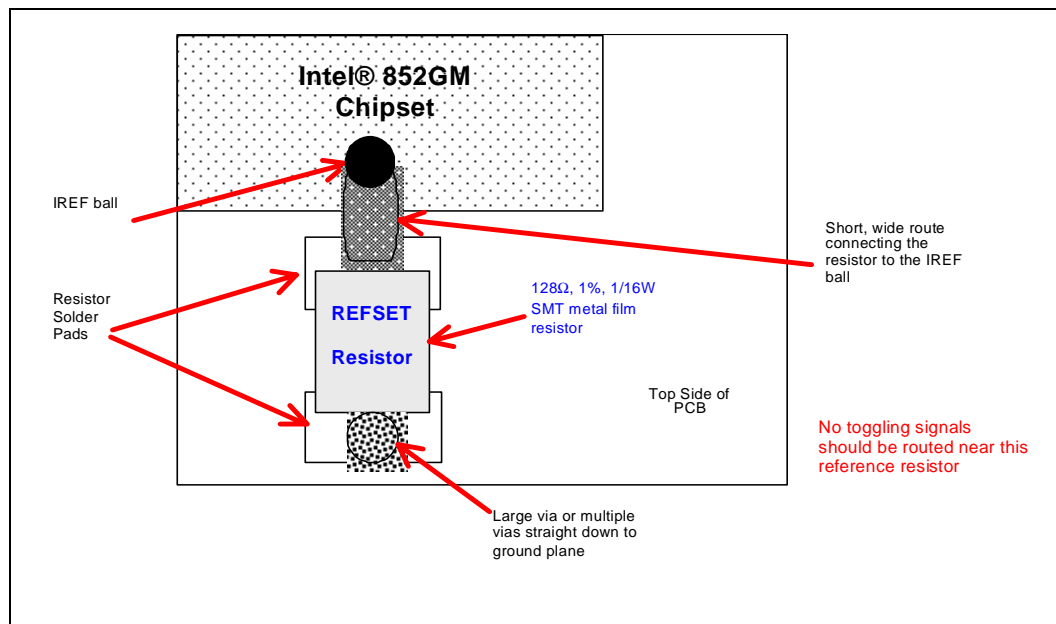
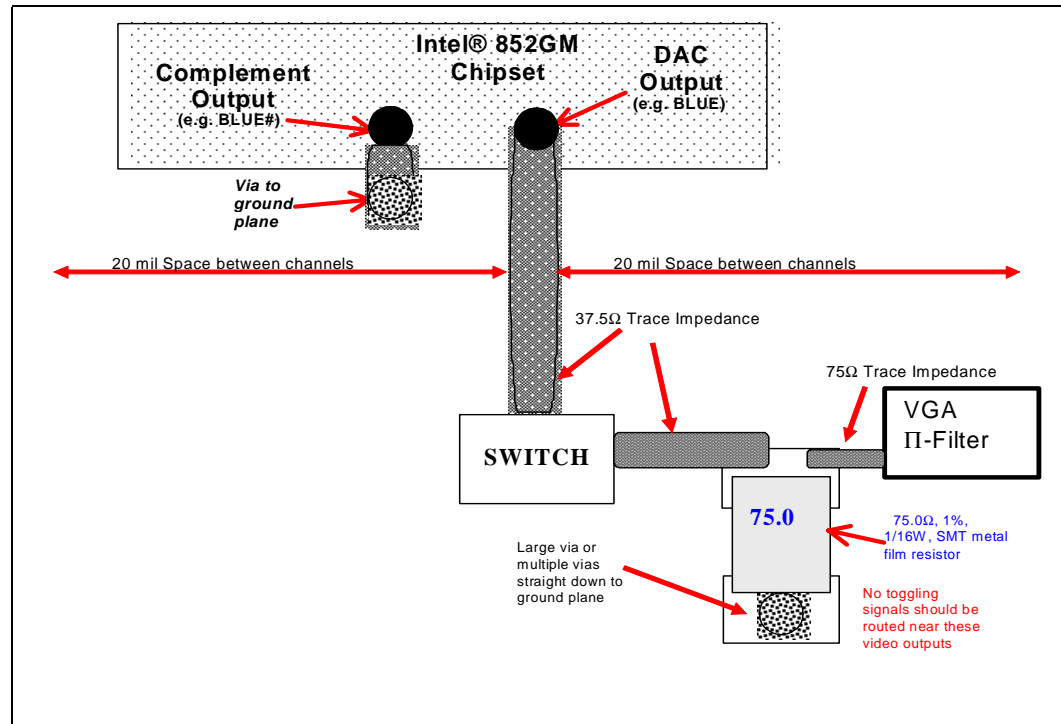


Figure 93 illustrates Intel's recommended routing of the termination resistors.

Figure 93. Recommended RAMDAC R, G, B Routing and Resistor Layout Example



8.1.5 DAC Power Requirements

The DAC requires a 1.5 V supply through its two V_{CCADAC} balls. The two may share a set of capacitors, 0.1 μ F and 0.01 μ F, but this connection should have low inductance. Separate analog power or ground planes are not required for the DAC.

However, because the DAC is an analog circuit, it is particularly sensitive to AC noise seen on its power rail. Designs should provide as clean and quiet a supply as possible to the V_{CCA_DAC} . Additional filtering and/or separate voltage rail may be needed to do so. .

- Video DAC Power Supply DC Specification: 1.50 V \pm 5%
- Video DAC Power Supply AC Specification:
 - \pm 0.3% from 0.10 Hz to 10 MHz
 - \pm 0.95% from 10 MHz to maximum pixel clock frequency
- Absolute minimum voltage at the V_{CCA} package ball = 1.40 V

Refer to the latest Intel® 852GM/GMV Chipset Graphics and Memory Controller Hub (GMCH) Datasheet for AC/DC specification.

8.1.6 HSYNC and VSYNC Design Considerations

HSYNC and VSYNC signals are connected to the analog display attached to the VGA connector. These are 3.3 V outputs from the GMCH. Some monitors have been found to drive HSYNC and VSYNC signals during reset. Because these signals are used as straps on the 852GM, the GMCH can enter into an illegal state under these conditions. In order to prevent these signals from being driven to the GMCH during reset, system designers must ensure GMCH is isolated from any monitor driving HSYNC or VSYNC while PCI_RST# is active. Appropriate logic is required between the GMCH and the VGA connector.

The recommended option is to use a unidirectional buffers (high impedance buffers) on each of these signals. For each of the HSYNCH and VSYNCH signals, a footprint for a series resistors must be placed between GMCH and the unidirectional buffer to prevent excessive overshoot and undershoot at the input of the buffer. Consideration should also be taken in designing the filter circuit on the output of these buffers to ensure that the VESA electrical specifications for video signals are met at the VGA connector. Customers are strongly encouraged to perform complete signal integrity validation at the input of the buffer and the VGA connectors.

8.1.7 DDC and I²C Design Considerations

DDCADATA and DDCACLK are 3.3 V I/O buffers connecting the GMCH to the monitor. To avoid potential electrical overstress on these signals, bidirectional level-shifting devices are required. These signals require 2.2 k Ω pull-ups (or pull-ups with the appropriate value derived from simulation) on each of these signals. See [Section 8.5](#) for additional pull up recommendations for the DDC (GPIO) signal group.

8.2 LVDS Transmitter Interface

The Low Voltage Differential Signaling (LVDS) transmitter serializer converts up to 18 bits of parallel digital RGB data, (6 bits per RGB), along with up to four bits for control (SHFCLK, HSYNC, VSYNC, DE) into two 4-channel serial bit streams for output by the LVDS transmitter.

The transmitter is fully differential and utilizes a current mode drive with a high impedance output. The drive current develops a differential swing in the range of 250 mV to 450 mV across a 100 Ω termination load.

The parallel digital data is serially converted to a 7-bit serial bit stream that is transmitted over the 8-channel LVDS interface at 7x the input clock. The differential output clock channel transmits the output clock at the input clock frequency. While the differential output channels transmit the data at the 7x clock rate (1 bit time is 7x the input clock). The 7x serializer synchronizes and regenerates an input clock from 35 MHz to 112 MHz. Typical operation is at 65 MHz (15.4 ns), therefore, at a 7x clock rate, 1bit time would be 2.2 ns. With data cycle times as small as 2.2 ns, propagation delay mismatch is critical, such that intra-channel skew (skew between the inverting and non-inverting output) must be minimized.

The following differential signal groups comprise the LVDS interface. The topology rules for each group are defined in subsequent sections.

Table 59. Signal Group and Signal Pair Names

Channel	Signal Group	Signal Pair Names
Channel A	Clocks	ICLKAM, ICLKAP
	Data Bus	IYAM[2:0], IYAP[2:0]
Channel B	Clocks	ICLKBM, ICLKBP
	Data Bus	IYBM[2:0], IYBP[2:0]

8.2.1 LVDS Length Matching Constraints

The routing guidelines presented in the following subsections define the recommended routing topologies, trace width and spacing geometries, and absolute minimum and maximum routed lengths for each signal group. These recommendations are provided to achieve optimal SI and timing. In addition to the absolute length limits provided, more restrictive length matching requirements are also provided. The additional requirements further restrict the minimum to maximum length range of each signal group with respect to clock strobe, within the overall boundaries defined in the guideline tables, as required to ensure adequate timing margins. These secondary constraints are referred to as length matching constraints. The amount of minimum to maximum length variance allowed for each group around the clock strobe reference length varies from signal group to signal group depending on the amount of timing variation that may be tolerated. Refer to [Table 60](#) for LVDS length matching requirements.

Each LVDS channel is length matched to the LVDS strobe signals. The strobes on a given channel are matched to within ± 25 mils of the target length.

Table 60. LVDS Signal Trace Length Matching Requirements

Signal Group	Data pair	Signal Matching	Clock Strobes Associated With the Channel	Strobe Matching
Channel A	IYAM0, IYAP0	± 20 mils	ICLKAM, ICLKAP	± 25 mils
	IYAM1, IYAP1	± 20 mils		
	IYAM2, IYAP2	± 20 mils		
Channel B	IYBM0, IYBP0	± 20 mils	ICLKAM, ICLKAP	± 25 mils
	IYBM1, IYBP1	± 20 mils		
	IYBM2, IYBP2	± 20 mils		

NOTE: All length matching formulas are based on GMCH die-pad to LVDS connector pin total length. Package length tables are provided for all signals in order to facilitate this pad to pin matching.

8.2.1.1 LVDS Package Length Compensation

As mentioned in [Section 8.2.1](#), all length matching is done from GMCH die-pad to LVDS connector pin. The reason for this is to compensate for the package length variation across each signal group to minimize timing variance. The GMCH does not equalize package lengths internally as some previous GMCH components have, and therefore, the GMCH requires a length matching process. Refer to [Table 62](#) for the Intel® 852GM chipset LVDS package lengths information.

Package length compensation should not be confused with length matching as discussed in the previous section. Length matching refers to constraints on the minimum and maximum length bounds of a signal group based on clock length, whereas package length compensation refers to the process of adjusting package length variance across a signal group. Of course, there is some overlap in that both affect the target length of an individual signal. Intel recommends that the initial route be completed based on the length matching formulas in conjunction with nominal package lengths and that package length compensation be performed as secondary operation.

8.2.2 LVDS Routing Guidelines

Each LVDS channel is required to be length matched to within ± 20 mils of the LVDS clock strobe signals. The two complementary signals in each clock strobe pair, as well as in each data pair, are also required to be length matched to within ± 20 mils of each other. See [Table 61](#) for a summary of LVDS signal group routing guidelines.

Table 61. LVDS Signal Group Routing Guidelines

Parameter	Definition
Signal Group	LVDS
Topology	Differential Pair Point to Point
Reference Plane	Ground Referenced
Differential Mode Impedance (Z_{diff})	$100 \Omega \pm 15\%$
Nominal Trace Width	4 mils
Nominal Pair Spacing (edge to edge)	7 mils
Minimum Pair to Pair Spacing (See exceptions for breakout region below.)	20 mils
Minimum Serpentine Spacing	20 mils
Minimum Spacing to Other LVDS Signals (See exceptions for breakout region below.)	20 mils
Minimum Isolation Spacing to non-LVDS Signals	20 mils
Maximum Via Count	2 (per line)
Package Length Range	$550 \text{ mils} \pm 150 \text{ mils}$ (Refer to Table 62 for exact lengths.)
Total Length	Maximum 10 inches
Data to Clock Length Matching	Match all segments to ± 20 mils. (Refer to Section 8.2.1 for more information.)
Clock to Clock# Length Matching (Total Length)	Match clocks to $X0 \pm 20$ mils.
Data to Data# Length Matching (Total Length)	Match data to ± 20 mils.
Breakout Exceptions (Reduced geometries for GMCH breakout region)	Breakout section should be as short as possible. Try to maintain trace width as 4 mils, spacing 7 mils, while the spacing between pairs may be 10-20 mils.

The traces associated with the LVDS Transmitter timing domain signals are differential traces terminated across $100 \Omega \pm 15 \Omega$ and should be routed as:

- Stripline only.

- Isolate all other signals from the LVDS signals to prevent coupling from other sources onto the LVDS lines.
- Use controlled impedance traces that match the differential impedance of your transmission medium (i.e., cable) and termination resistor.

Note: Maintain the transmission medium's Zdiff to 100 $\Omega \pm 15\%$.)

- Run the differential pair trace lines as close together as possible as soon as they leave the IC, not greater than 10 mils. This helps eliminate reflections and ensure noise is coupled as common mode. Plus, noise induced on the differential lines is much more likely to appear as common mode, which is rejected by the receiver.
- The LVDS transmitter timing domain signals have a maximum trace length of 10 inches. This maximum applies to all of the LVDS transmitter signals.
- Traces must be ground referenced and must not switch layers between the GMCH and connector.

When choosing cables, it is important to remember:

- Use controlled impedance media. The differential impedance of cable LVDS uses should be 100 Ω . Cables should not introduce major impedance discontinuities that cause signal reflection.
- Balanced cables (twisted pair) are usually better than unbalanced cables (ribbon cable, multi-conductor) for noise reduction and signal quality.
- Cable length must be less than 16 inches.

Table 62. LVDS Package Lengths

Signal Group	GMCH Signal Name	Package Trace Length (mils)	Signal Group	GMCH Signal Name	Package Trace Length (mils)
CHANNEL A	ICLKAP	503.7	CHANNEL B	ICLKAP	502.0
	ICLKAM	498.8		ICLKAM	499.1
	IYAP0	399.6		IYBP0	359.8
	IYAM0	385.4		IYBM0	353.7
	IYAP1	487.5		IYBP1	524.7
	IYAM1	466.2		IYBM1	516.6
	IYAP2	572.6		IYBP2	623.3
	IYAM2	566.2		IYBM2	604.2

8.3 Digital Video Out Port

The GMCH DVO port interface supports a wide variety of third party DVO compliant devices (e.g., TV encoder, TMDS transmitter or integrated TV encoder, and TMDS transmitter). The 852GM chipset has a single dedicated Digital Video Out port (DVOC). Intel's DVO port is a 1.5-V only interface that can support transactions up to 165 MHz. Some of the DVO command signals may require voltage translation circuit depending on the third party device.

8.3.1 DVO Interface Signal Groups

8.3.1.1 DVOC Interface Signals

8.3.1.1.1 Input Signals

- DVOCFLDSTL
- DVOBCCLKINT
- DVOBCINTR#
- ADDID[7:0]
- DVODETECT

8.3.1.1.2 Output Data Signals

- DVOCHSYNC
- DVOCVSYNC
- DVOCBLANK#
- DVOCD[11:0]

8.3.1.1.3 Output Strobe Signals

- DVOCLK
- DVOCLK#

8.3.1.1.4 Voltage References, PLL Power Signals

- DVORCOMP
- GVREF

8.3.2 DVOC Port Interface Routing Guidelines

8.3.2.1 Length Matching Constraints

The routing guidelines presented in the following subsections define Intel's recommended routing topologies, trace width and spacing geometries, and absolute minimum and maximum routed lengths for each signal group, which are recommended to achieve optimal SI and timing. In addition to the absolute length limits provided in the individual guideline tables, more restrictive length matching requirements are also provided which further restrict the minimum to maximum length range of each signal group with respect to clock strobe, as required to ensure adequate timing margins. Refer to [Table 63](#) for DVOC interface trace length matching requirements.

Table 63. DVO Interface Trace Length Mismatch Requirements

Data Group	Signal Matching to Strobe Clock	DVO Clock Strokes Associated With the Group	Clock Strobe Matching	Notes
DVOC [11:0]	±100 mils	DVOCLK/DVOCLK#	± 10 mils	1, 2

NOTES:

1. Data signals of the same group should be trace length matched to the clock within ± 100 mil including package lengths.
2. **All length matching formulas are based on GMCH die-pad to DVO device pin total length.** Package length tables are provided for all signals to facilitate this pad-to-pin matching.

8.3.2.2 Package Length Compensation

As mentioned in [Section 8.3.2.1](#), all length matching is done from GMCH die-pad to DVOC connector pin. The reason for this is to compensate for the package length variation across each signal group to minimize timing variance. The GMCH does not equalize package lengths internally as some previous GMCH components have, and therefore, the GMCH requires a length matching process. Refer to [Table 65](#) for the DVOC interface package lengths information.

Package length compensation should not be confused with length matching as discussed in the previous section. Length matching refers to constraints on the minimum and maximum length bounds of a signal group based on clock length, whereas package length compensation refers to the process of adjusting out package length variance across a signal group. There is of course some overlap in that both affect the target length of an individual signal. Intel recommends that the initial route be completed based on the length matching formulas in conjunction with nominal package lengths and that package length compensation be performed as secondary operation.

8.3.2.3 DVOC Routing Guidelines

Table 64 provides the DVOC routing guideline summary.

Table 64. DVOC Routing Guideline Summary

Parameter	Definition
Signal Group	DVOC [11:0]
PCB Topology	Point to point
Reference Plane	Ground Referenced
Characteristic Trace Impedance (Z_0)	55 $\Omega \pm 15\%$
Nominal Trace Width	Inner layers: 4 mils
Minimum Spacing to Trace Width Ratio	2:1 (e.g., 8 mil space to 4 mil trace)
Minimum Isolation Spacing to non-DVO Signals	20 mils
Minimum Spacing to Other DVO Signals	12 mils (See exceptions for breakout region below.)
Minimum Spacing of DVOCCLK/DVOCCLK# to any other signals	12 mils
Package Length Range	Refer to Table 65 for package lengths.
Total Length	Minimum = 1.5 inches Maximum = 6 inches
Data to Clock Strobe Length Matching Requirements	± 100 mils (See Table 63 for length matching requirements)
CLK0 to CLK1 Length Matching Requirements	± 10 mils (See Table 63 for length matching requirements)

The DVOC interface does not require any external termination. They are routed point-to-point as follows:

- All signals should be routed as striplines (inner layers).
- All signals in a signal group should be routed on the same layer. Routing studies have shown that these guidelines can be met. The trace length and trace spacing requirements *must* not be violated by any signal.
- Route the DVOCCLK/DVOCCLK# signal pairs 4 mils wide and 8 mils apart with a max trace length of 6 inches. This signal pair should be a minimum of 12 mils from any adjacent signals.
- To break out of the 852GM GMCH, the DVOC data signals can be routed with a trace width of 4 mils and a trace spacing of 7 mils. The signals should be separated to a trace width of 4 mils and a trace spacing of 8 mils within 0.3 inch of the GMCH component.

Table 65. DVOC Interface Package Length (Sheet 1 of 2)

Signal	Pin Number	Package Length (mils)
DVOCBLANK#	L3	541
DVOCCLK	J3	601
DVOCCLK#	J2	675
DVOC[0]	K5	489
DVOC[1]	K1	692
DVOC[2]	K3	622

Table 65. DVOC Interface Package Length (Sheet 2 of 2)

Signal	Pin Number	Package Length (mils)
DVOC[3]	K2	685
DVOC[4]	J6	536
DVOC[5]	J5	518
DVOC[6]	H2	720
DVOC[7]	H1	771
DVOC[8]	H3	649
DVOC[9]	H4	625
DVOC[10]	H6	521
DVOC[11]	G3	762
DVOCFLDSTL	H5	566
DVOCHSYNC	K6	491
DVOCVSYNC	L5	440

8.3.2.4 DVOC Port Termination

The DVO interface does not require external termination.

8.3.3 DVOC Assumptions, Definitions, and Specifications

The source synchronous solution space consists of all designs in which the flight time mismatch between a strobe and its associated data is less than the total allowable skew:

$$T_{\text{skew}} = T_{\text{flightdata}} - T_{\text{flightstrobe}}$$

Where $T_{\text{flightdata}}$ and $T_{\text{flightstrobe}}$ are the driver-pad-to-receiver-pin flight times of the data and the strobe respectively.

The DVO physical interface is a point-to-point topology using 1.5 V signaling. The DVO uses a 165 MHz clock.

The flight time skew simulations reproduce all parameters that could cause a skew between two signals, including PCB and add-in card line lengths, effective capacitance in the buffer models, crosstalk on each of the different interconnect combinations, data pattern dependencies, and Inter-Symbol Interference (ISI) induced skews.

8.3.4 DVOC Simulation Method

Figure 94 illustrates a DVOC simulations model. The DVO component is a third-party chip.

Figure 94. DVOC Simulations Model

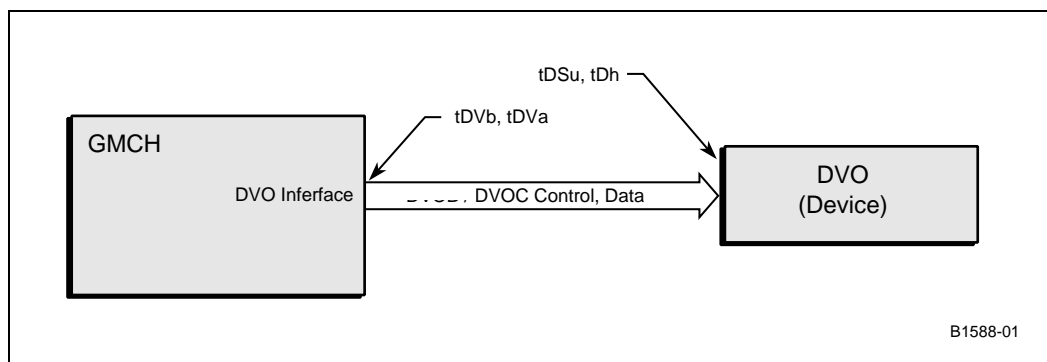
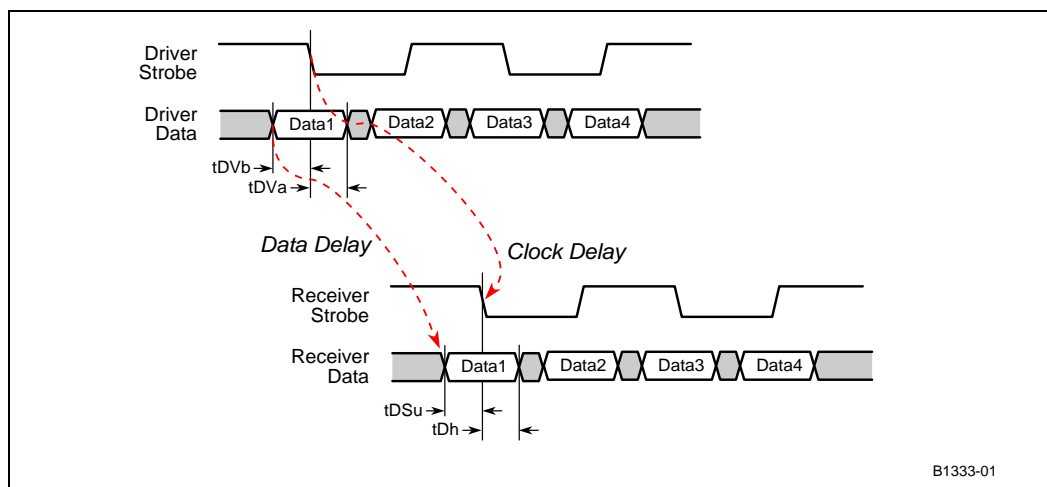


Figure 95 illustrates the driver-receiver waveforms relationship specification.

Figure 95. Driver-Receiver Waveforms Relationship Specification



The setup margin and the hold margin for a particular design depends on the values of the data valid times and the data setup and hold times on both the driver and the receiver sides. However, available margins are not absolute values. Any skew due to routing and loading differences, any coupling differences in the parallel traces, and any effects of Simultaneous Switching Output (such as ISI, ground bounce, etc.) should be accounted for in the timing budget as they reduce the total available margin for the design.

Table 66 presents the allowable interconnect skew calculations.

Table 66. Allowable Interconnect Skew Calculation

Component	Skew Element	Symbol	Setup	Hold	Units
Driver	Data Valid before Strobe	tDVb	570		ps
	Data Valid after Strobe	tDVa		770	ps
Interconnect	Allowable Skew		Vendor specific	Vendor specific	ps
Receiver	Data Setup to Strobe	tDSu	Vendor specific		ps
	Data Hold from Strobe	tDh		Vendor specific	ps

All numbers in this table are from the 82852GM specification documents that are applicable for this interface. For third-party receiver devices, refer to appropriate third-party vendor specifications.

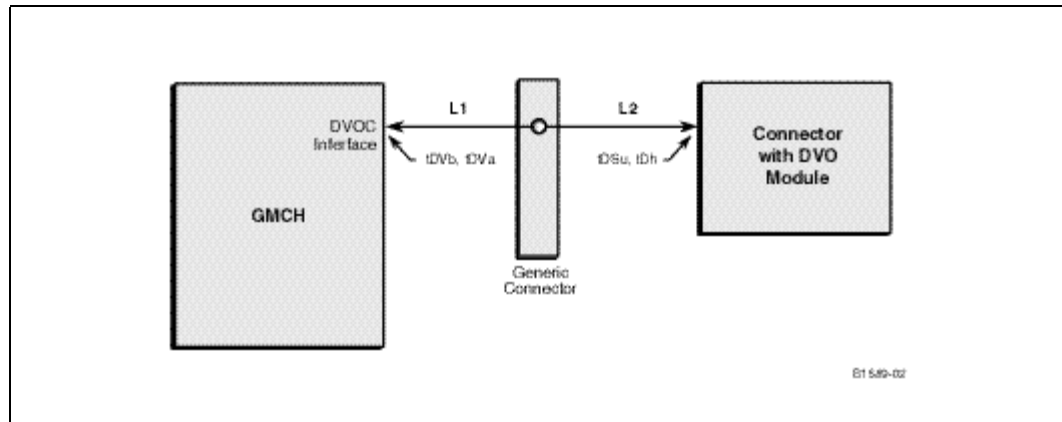
8.4 DVOC Port Flexible (Modular) Design

The GMCH supports flexible design interfaces described in this section.

8.4.1 DVOC Module Design

The 82852GM supports a DVO module design connected to the GMCH through a generic connector. Simulation method is the same as in [Section 8.3.4](#). Lengths L1 and L2 are determined by simulation as L1 = 4 inches and L2 = 2 inches. Refer to [Figure 97](#) for the generic connector parasitic model.

Figure 96. DVO Enabled Simulation Model



All signals should be routed as striplines (inner layers). All signals in a signal group should be routed on the same layer. Routing studies have shown that these guidelines can be met. The trace length and trace spacing requirements *must* not be violated by any signal. Trace length mismatch for all signals within a signal group should be as close to ± 100 mils with respect to the strobe clocks as possible to provide optimal timing margin. Each strobe pair must be separated from other signals by at least 12 mils.

[Table 67](#) presents the DVO enabled routing guideline summary.

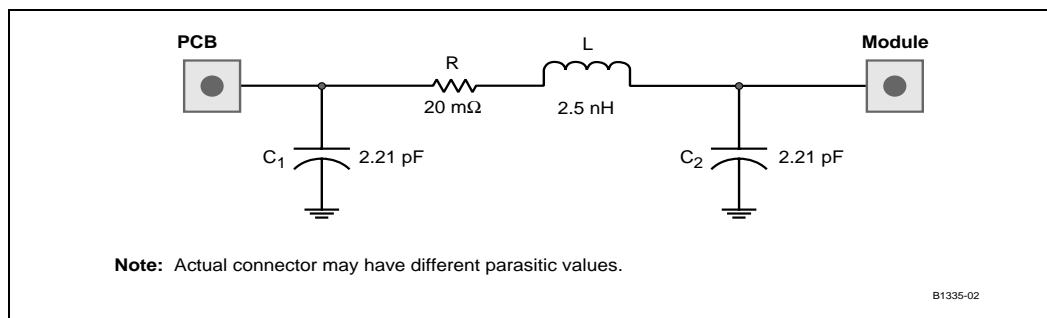
Table 67. DVO Enabled Routing Guideline Summary

Signal	Maximum Length	Trace Width	Trace Spacing	Length Mismatch	Notes
DVO Timing Domain	L1=4 in L2=2 in	4 mils	8 mils	± 100 mils	

8.4.1.1 Generic Connector Model

Figure 97 illustrates the generic connector model used in simulation for flexible DVO implementation. This is only for reference. The actual connector may have different parasitic values. Designs using this approach need to be simulated first.

Figure 97. Generic Module Connector Parasitic Model



8.5 DVO GMBUS and DDC Interface Considerations

The GMCH DVOC port controls the video front-end devices via the GMBUS (I²C) interface. DDCADATA and DDCACLK should be connected to the CRT connector. The GMBUS should be connected to the DVO device, as required by the specifications for those devices. The protocol and bus may be used to configure registers in the TV encoder, TMDS transmitter, or any other external DVI device. The GMCH also has an option to utilize the DDCPCLK and DDCPDATA to collect EDID (Extended Display Identification) from a digital display panel.

Pull-ups (or pull-ups with the appropriate value derived from simulating the signal) typically ranging from 2.2 kΩ to 10 kΩ are required on each of these signals.

The GMCH signal groups in Table 68 list the six possible GMBUS pairs.

Table 68. GMBUS Pair Mapping and Options (Sheet 1 of 2)

Pair #	Signal Name	Buffer Type	Description	Notes
0	DDCADATA	3.3 V	DDC for Analog monitor (CRT) connection	This cannot be shared with other DDC or I2C pairs due to legacy monitor issues.
	DDCACLK			
1	LCLKCTRLA	3.3 V	For control of SSC clock generator devices down on PCB	If SSC is not supported, then may optionally use as GMBUS for DVOC.
	LCLKCTRLB			
2	DDCPDATA	3.3 V	DDC for Digital Display connection via the integrated LVDS display port for support for EDID panel	If EDID panels are not supported, then may optionally use as GMBUS for DVOC.
	DDCPCLK			
3	MDVIDATA	1.5 V	GMBUS control of DVI devices (TMDS or TV encoder)	May optionally use as GMBUS for DVOC.
	MDVICLK			

NOTE: All GMBUS pairs may be optionally programmed to support any interface and is programmed through the BIOS Modification Program (BMP) utility. Contact your local Intel Field Application Engineer for more information.

Table 68. GMBUS Pair Mapping and Options (Sheet 2 of 2)

Pair #	Signal Name	Buffer Type	Description	Notes
4	MI2CDATA	1.5 V	GMBUS control of DVI devices (TMDS or TV encoder)	May optionally use as GMBUS for DVOC.
	MI2CCLK			
5	MDDCDATA	1.5 V	DDC for Digital Display connection via TMDS device	May optionally use as GMBUS for DVOC.
	MDDCCLK			

NOTE: All GMBUS pairs may be optionally programmed to support any interface and is programmed through the BIOS Modification Program (BMP) utility. Contact your local Intel Field Application Engineer for more information.

If any of GMBUS pairs are not used, 2.2 k-100 k Ω pull-up (or pull-ups with the appropriate value derived from simulating the signal) resistors are required, except for CRT DDCADATA/DDCCLK and LCLKCTRLA/LCLKCTRLB GMBUS pair. LCLKCTRLA/LCLKCTRLB are used as bootup straps. This will prevent the GMCH DVOC from confusing noise on these lines for false cycles.

8.5.1 Leaving the GMCH DVOC Port Unconnected

When the PCB does not implement any of the possible video devices with the DVO port, follow the guidelines recommended on the PCB. DVO Output signals may be left unconnected if they are not used.

Pull-down resistors are required for the following signals if not used:

- DVOCFLDSTL
- DVOCCLKINT

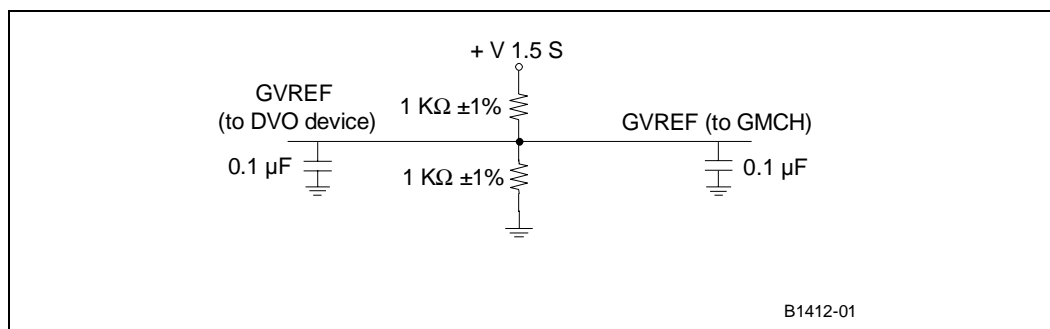
Pull-up resistors are required for the following signals if not used:

- DVOCINTR#

8.6 Miscellaneous Input Signals and Voltage Reference

- ADDID[7]: Pull-down to ground with a 1 K Ω resistor when using the DVOC port. This is a vBIOS strapping option to load the TPV AIM module for DVOC port. Pull-down not required if DVOC is not enabled.
- ADDID[6:0]: Leave unconnected (NC).
- DVODETECT: Leave unconnected (NC) when using the DOVC port.
- DVORCOMP is used to calibrate the DVO buffers. It should be connected to ground via a 40.2 Ω 1% resistor using a routing guideline of 10 mil trace and 20 mil spacing.
- DPMS: connects to 1.5 V version of the Intel® 82801DB I/O Controller Hub (ICH4) SUSCLK or a clock that runs during S1.
- GVREF: Reference voltage for the DVOC input buffers. [Figure 98](#) illustrates the GVREF reference voltage information.

Figure 98. GVREF Reference Voltage



System Memory Design Guidelines (DDR-SDRAM)

9

9.1 Introduction

The Intel® 852GM Chipset Double Data Rate (DDR) SDRAM system memory interface consists of SSTL-2 compatible signals. These SSTL-2 compatible signals have been divided into several signal groups: data, control, command, CPC, clock, and feedback signals.

Table 69 presents the signal grouping. Refer to the *Intel® 852GM GMCH Chipset Datasheet* for details on these signals listed.

Table 69. Intel® 852GM GMCH Chipset DDR Signal Groups

Group	Signal Name	Description
Clocks	SCK[5:0]	DDR-SDRAM differential clocks - (three per DIMM)
	SCK[5:0]#	DDR-SDRAM inverted differential clocks - (three per DIMM)
Data	SDQ[71:64]	ECC error detection is NOT supported on the Intel 852GM GMCH. These signals should be left as NC (no connect).
	SDQ[63:0]	Data bus
	SDQS[8]	ECC error detection is NOT supported on the Intel 852GM GMCH. This signal should be left as NC (no connect).
	SDQS[7:0]	Data strobes
	SDM[8]	ECC error detection is NOT supported on the Intel 852GM GMCH. This signal should be left as NC (no connect).
	SDM[7:0]	Data mask
Control	SCKE[3:0]	Clock enable - (one per Device Row)
	SCS[3:0]#	Chip select - (one per Device Row)
Command	SMA[12:6,3,0]	Memory address bus
	SBA [1:0]	Bank select
	SRAS#	Row address select
	SCAS#	Column address select
	SWE#	Write enable
CPC	SMA[5,4,2,1]	Command per clock (DIMM0)
	SMAB[5,4,2,1]	Command per clock (DIMM1)
Feedback	RCVENOUT#	Receive enable output (no external connection)
	RCVENIN#	Receive enable input (no external connection)

9.2 Length Matching and Length Formulas

The routing guidelines presented in the following subsections define Intel's recommended routing topologies, trace width and spacing geometries, and absolute minimum and maximum routed lengths for each signal group, which are recommended to achieve optimal SI and timing. In addition to the absolute length limits provided in the individual guideline tables, more restrictive length matching formulas are also provided that further restrict the minimum to maximum length range of each signal group with respect to clock, within the overall boundaries, as required to ensure adequate timing margins. These secondary constraints are referred to as length matching constraints and the formulas used are referred to as length matching formulas.

All signal groups, except feedback signals, are length matched to the DDR clocks. The clocks on a given DIMM are matched to within ± 25 mils of the target length. A different clock target length may be used for each DIMM. The difference in clock target lengths between DIMM0 and DIMM1 should not exceed one inch. Table 70 presents a simple summary of the length matching formulas for each signal group.

Table 70. Length Matching Formulas

Signal Group	Minimum Length	Maximum Length
Control to Clock	Clock – 1.5 inches	Clock - 0.5 inch
Command to Clock	Clock – 1.5 inches	Clock + 1 inch
CPC to Clock	Clock – 1.5 inches	Clock - 0.5 inch
Strobe to Clock	Clock – 1.5 inches	Clock - 0.5 inch
Data to Strobe	Strobe – 25 mils	Strobe + 25 mils

NOTE: All length matching formulas are based on GMCH die-pad to DIMM pin total length.

Package length tables are provided for all signals to facilitate this pad-to-pin matching. Length formulas should be applied to each DIMM slot separately. The full geometry and routing guidelines along with the exact length matching formulas and associated diagrams are provided in the individual signal group guidelines sections to follow.

9.3 Package Length Compensation

As mentioned above, all length matching is done for GMCH die-pad to DIMM pin. This is done to compensate for package length variation across each signal group in order. The 852GM chipset Graphics Memory Controller Hub (82852GM) does not equalize package lengths internally as some previous GMCH components have; the 82852GM requires a length matching or tuning process. The justification for this is based on the belief that length variance in the package based on ball position is naturally tuned out when the pin escape is completed to the edge of the package. Length matching in the package would then tend to create a mismatch at the package edge.

Package length compensation should not be confused with length matching as discussed in the previous section. Length matching refers to constraints on the minimum and maximum length bounds of a signal group based on clock length, whereas package length compensation refers to the process of adjusting package length variation across a signal group. There is some overlap in that both affect the target length of an individual signal. Intel recommends that the initial route be completed based on the length matching formulas in conjunction with nominal package lengths and that package length compensation be performed as secondary operation where required.

9.4 Topologies and Routing Guidelines

The Intel 852GM GMCH chipset's Double Data Rate (DDR) SDRAM system memory interface implements the low swing, high-speed, terminated SSTL_2 topology. This section contains information related to the recommended interconnect topologies and routing guidelines for each of the signal groups that comprise the DDR interface. When implemented as defined, these guidelines provide for a robust DDR solution on an Intel 852GM GMCH chipset based design. The clock signal group is presented first, since most of the signal groups have length formulas that are based on clock length.

9.4.1 Clock Signals – SCK[5:0], SCK[5:0]#

The clock signal group includes the differential clock pairs SCK[5:0]/SCK[5:0]#. The GMCH generates and drives these differential clock signals required by the DDR interface; therefore, no external clock driver is required for the DDR interface. The GMCH only supports unbuffered DDR DIMMs. Three differential clock pairs are routed to each DIMM connector. Table 71 presents the clock signal mapping.

Table 71. Clock Signal Mapping

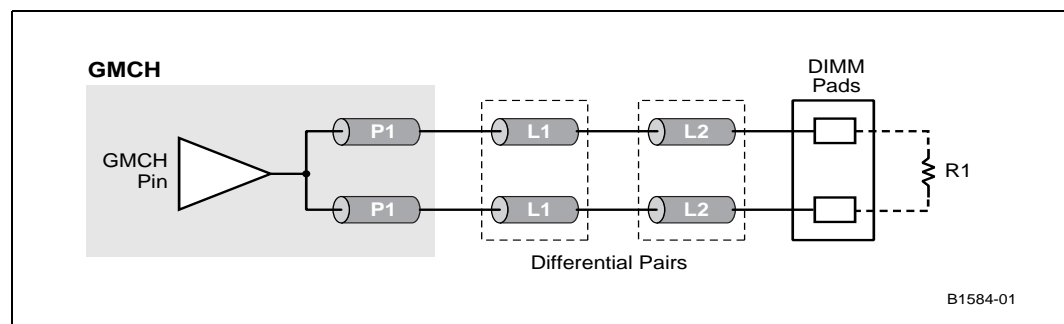
Signal	Relative To
SCK[2:0]/SCK[2:0]#	DIMM0
SCK[5:3]/SCK[5:3]#	DIMM1

9.4.2 Clock Topology Diagram

The 82852GM provides six differential clock output pairs, or three clock pairs per DIMM socket. Refer to the routing guidelines in Section 9.4.3 for detailed length and spacing rules for each segment. The clock signals should be routed as closely-coupled differential pairs over the entire length. Spacing to other DDR signals should not be less than 20 mils. Isolation spacing to non-DDR signals should be 25 mils.

Figure 99 illustrates the DDR clock routing topology (SCK[5:0]/SCK[5:0]#).

Figure 99. DDR Clock Routing Topology (SCK[5:0]/SCK[5:0]#)



9.4.3 DDR Clock Routing Guidelines

Table 72 presents the DDR clock signal group routing guidelines.

Table 72. DDR Clock Signal Group Routing Guidelines

Parameter	Definition
Signal Group	SCK[5:0] and SCK[5:0]#
Topology	Differential Pair Point to Point
Reference Plane	Ground Referenced
Single Ended Trace Impedance (Z_0)	$42 \Omega \pm 15\%$
Differential Mode Impedance (Z_{diff})	$70 \Omega \pm 15\%$
Nominal Trace Width (See exceptions for breakout region below.)	Inner Layers: 7 mils Outer Layers: 8 mils (pin escapes only)
Nominal Pair Spacing (edge to edge) (See exceptions for breakout region below.)	Inner Layers: 4 mils Outer Layers: 5 mils (pin escapes only)
Minimum Pair-to-Pair Spacing (See exceptions for breakout region below.)	20 mils
Minimum Serpentine Spacing	20 mils
Minimum Spacing to Other DDR Signals (See exceptions for breakout region below.)	20 mils
Minimum Isolation Spacing to Non-DDR Signals	25 mils
Maximum Via Count	2 (per side)
Package Length Range – P1	1000 mils \pm 350 mils (See clock package length Table 73 for exact lengths.)
Trace Length Limits – L1	Max = 300 mils (breakout segment)
Total MB Length Limits – P1 + L1 + L2	Min = 3.5 inches Max = 6.5 inches
Total Length – P1 + L1 + L2	Total length target is determined by placement Total length for DIMM0 group = X0 (see Figure 100) Total length for DIMM1 group = X1 (see Figure 100)
SCK to SCK# Length Matching	Match total length to ± 10 mils
Clock to Clock Length Matching (Total Length)	Match all DIMM0 clocks to $X0 \pm 25$ mils (see Figure 100) Match all DIMM1 clocks to $X1 \pm 25$ mils (see Figure 100)
Breakout Exceptions (Reduced geometries for MCH breakout region)	Inner Layers: 4 mil trace, 4 mil pair space allowed Outer Layers: 5 mil trace, 5 mil pair space allowed Pair-to-pair spacing of 5 mils allowed Spacing to other DDR signals of 5 mils allowed Maximum breakout length is 0.3 inch

NOTES:

1. Pad-to-pin length tuning is used on clocks to achieve minimal variance. Package lengths range between approximately 600 mils and 1400 mils. Exact package lengths for each clock signal are provided at the end of this section. Overall target length should be established based on placement and routing flow. The resulting PCB segment lengths must fall within the ranges specified.
2. The DDR clocks should be routed on internal layers, except for pin escapes. Intel recommends that pin escape vias be located directly adjacent to the ball pads on all clocks. Surface layer routing should be minimized.
3. Exceptions to the trace width and spacing geometries are allowed in the breakout region to fan-out the interconnect pattern. Reduced spacing should be avoided as much as possible.

9.4.3.1 Clock Length Matching Requirements

The Intel 82852GM GMCH provides two differential clock pairs for each DIMM. A differential clock pair is made up of a SCK signal and its complement signal SCK#. Refer to [Section 9.2](#) for more details on length matching requirements.

The differential pairs for one DIMM are:

SCK[0]/SCK[0]#
SCK[1]/SCK[1]#
SCK[2]/SCK[2]#

The differential pairs for the second DIMM are:

SCK[3]/SCK[3]#
SCK[4]/SCK[4]#
SCK[5]/SCK[5]#

The two sets of differential clocks must be length tuned on the PCB such that any pair to pair package length variation is tuned out. The three pairs associated with DIMM0 are tuned to a fixed overall length, including package, and the three pairs associated with DIMM1 are tuned to a fixed overall length.

The two traces associated with each clock pair are length matched within the package, however some additional compensation may be required on the PCB to achieve the ± 10 -mil length tolerance within the pair.

Between clock pairs the package length varies substantially. The PCB length of each clock pair must be length adjusted to tune out package variance. The total length including package should be matched to within ± 25 mils of each other. This may result in a clock length variance of as much as 700 mils on the PCB.

The first step in determining the routing lengths for clocks and all other clock-relative signal groups is to establish the target length for each DIMM clock group. These target lengths are shown as X0 and X1 in [Figure 100](#). These are the lengths to which all clocks within the corresponding group are matched and the reference length values used to calculate the length ranges for the other signal groups.

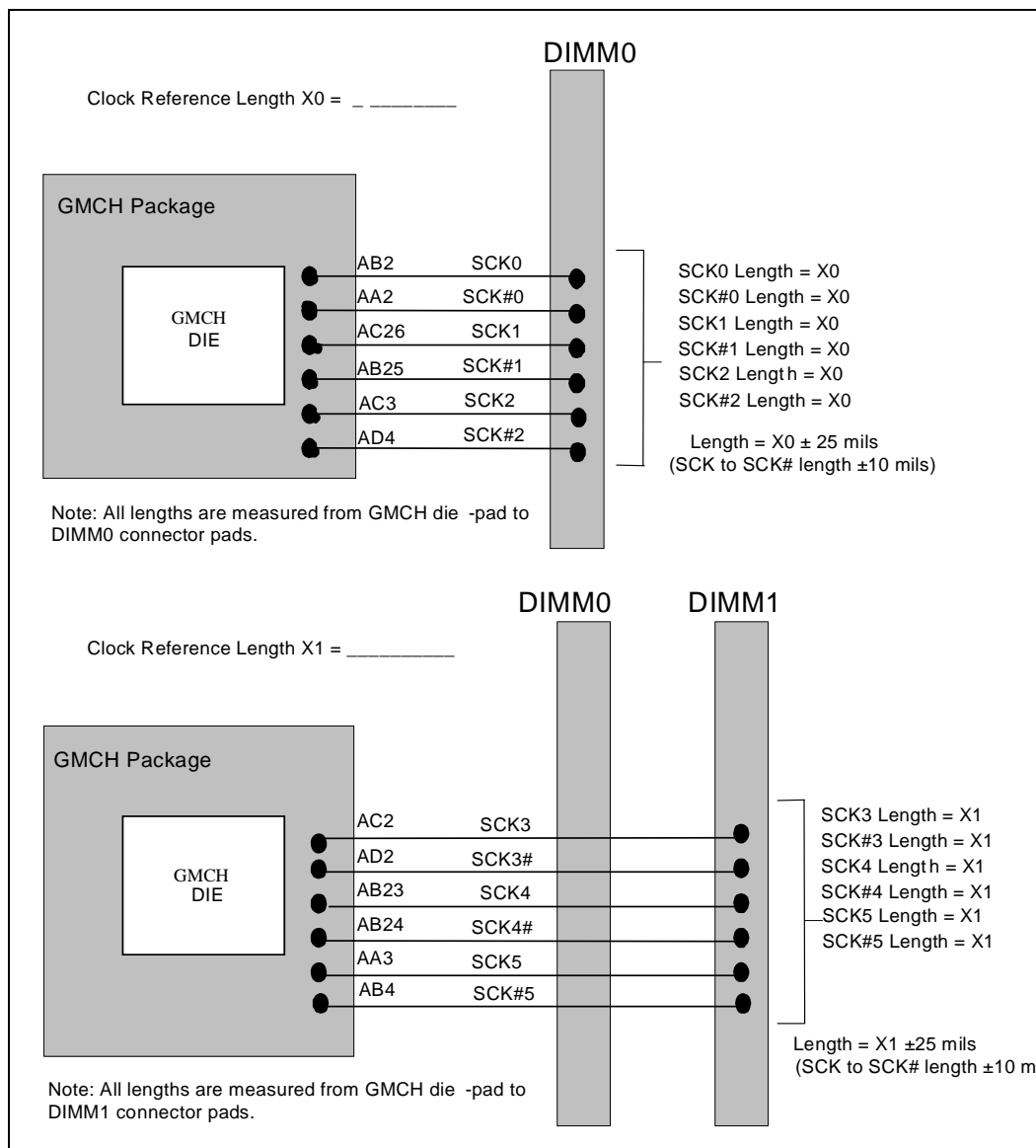
9.4.3.2 Clock Reference Lengths

The clock reference length for each DIMM clock group is calculated by first determining the longest total clock length required to complete the clock routing. A table of clock package lengths is provided in [Table 73](#) to assist with this calculation. After the longest total length is determined for each clock group, this figure becomes a lower bound for the associated clock reference length. At this point it is helpful to have completed a test route of the SDQ/SDQS bus such that final clock reference lengths may be defined with consideration of the impact on SDQ/SDQS bus routability. Some iteration may be required.

Once the reference lengths X0 and X1 are defined then the next step is to tune each clock pair's PCB trace segment lengths as required such that the overall length of each clock equals the associated clock reference length plus or minus the 25 mil tolerance. Again, the reference length for the two sets of clocks should be offset by the nominal routing length between DIMM connectors.

Figure 100 illustrates the DDR clock trace length matching diagram.

Figure 100. DDR Clock Trace Length Matching Diagram



9.4.3.3 Clock Length Package Table

The package length data in [Table 73](#) should be used to tune the PCB length of each SCK/SCK# clock pair between the GMCH and the associated DIMM socket. Intel recommends that die-pad to DIMM pin length be tuned to within ± 25 mils to optimize timing margins on the interface.

Table 73. DDR Clock Package Lengths

Signal	Pin Number	Package Length (mils)
SCK[0]	AB2	1177
SCK[0]#	AA2	1169
SCK[1]	AC26	840
SCK[1]#	AB25	838
SCK[2]	AC3	1129
SCK[2]#	AD4	1107
SCK[3]	AC2	1299
SCK[3]#	AD2	1305
SCK[4]	AB23	643
SCK[4]#	AB24	656
SCK[5]	AA3	1128
SCK[5]#	AB4	1146

Package length compensation may be performed on each individual clock output thereby matching total length on SCK/SCK# exactly, or alternatively the average package length may be used for both outputs of a pair and length tuning done with respect to the PCB portion only.

9.4.4 Data Signals – SDQ[71:0], SDM[8:0], SDQS[8:0]

The GMCH data signals are source synchronous signals that include a 64-bit wide data bus, a set of 8 data mask bits, and a set of 8 data strobe signals. There is an associated data strobe and data mask bit for each of the eight data byte groups, making for a total of eight 10-bit byte lanes. This section summarizes the SDQ/SDM to SDQS routing guidelines and length matching recommendations.

- The data signals include SDQ[63:0], SDM[7:0], and SDQS[7:0].
- SDQ[71:64], SDM[8], and SDQS[8] are left as NC (No Connect). ECC error detection is not supported on the 852GM GMCH.
- The data signals should transition from an external layer to an internal signal layer under the GMCH. Keep to the same internal layer until transitioning back to an external layer at the series resistor.
- After the series resistor, the signal should transition from the external layer to the same internal layer and route to DIMM0.
- At DIMM0, the signal should transition to an external layer and connect to the appropriate pad of the connector.
- After the DIMM0 transition, continue to route the signal on the same internal layer to DIMM1.
- Transition back out to an external layer and connect to the appropriate pad of DIMM1.

- Connection to the termination resistor should be through the same internal layer with a transition back to the external layer near the resistor. External trace lengths should be minimized.

To facilitate routing, swapping of the byte lanes is allowed for SDQ[63:0]. Bit swapping within the byte lane is also allowed for SDQ[63:0] only. It is suggested that the parallel termination be placed on both sides of DIMM1 to simplify routing and minimize trace lengths. All internal and external signals should be ground referenced to keep the path of the return current continuous.

Resistor packs are acceptable for the series (R_s) and parallel (R_t) data and strobe termination resistors, but data and strobe signals cannot be placed within the same R pack as the command or control signals. The tables and diagrams below present Intel's recommended topology and layout routing guidelines for the DDR-SDRAM data signals.

Intel recommends that the full data bus SDQ[63:0], mask bus SDM[7:0], and strobe signals SDQS[7:0] be routed on the same internal signal layer. It is required that the SDQ byte group and the associated SDM and SDQS signals within a byte lane be routed on the same internal layer.

The total length of SDQ, SDM, and SDQS traces between the GMCH and the DIMMs must be within the range defined in the overall guidelines, and is also constrained by a length range boundary based on SCK/SCK# clock length, and an SDQ/SDM to SDQS length matching requirement within each byte lane.

Note: All length matching must be done inclusive of package length. SDQ, SDM, and SDQS package lengths are provided in [Table 76](#) to facilitate this process.

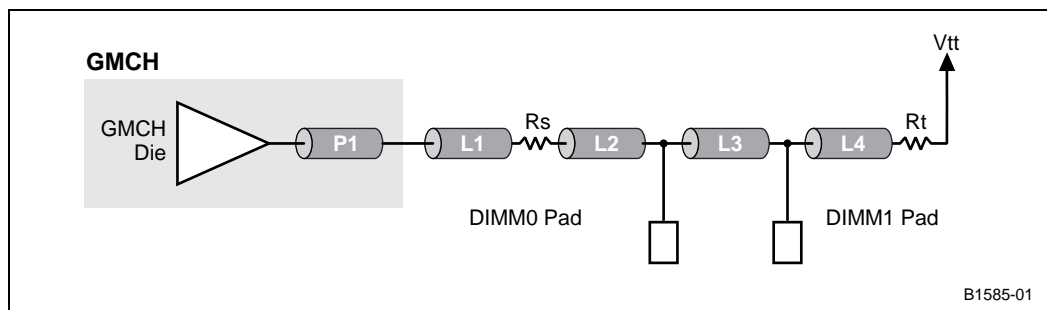
There are two levels of matching implemented on the data bus signals. The first is the length range constraint on the SDQS signals based on clock reference length. The second is SDQ/SDM to SDQS length matching within a byte lane. The length of the SDQS signal for each byte lane must fall within a range determined by the clock reference length, as defined in the SDQS to SCK/SCK# length matching section. The actual length of SDQS for each byte lane may fall anywhere within this range based on placement and routing flow.

After the SDQS length for a byte lane is established, the SDQ, SDM, and SDQS signals within the byte lane must be length matched to each other, inclusive of package length, as described in the SDQ to SDQS length matching section.

9.4.4.1 Data Bus Topology

Figure 101 illustrates the data signal routing topology.

Figure 101. Data Signal Routing Topology



The data signals should be routed using a 2:1 trace spacing to trace width ratio for signals within the DDR group, except for clocks and strobes. Data signals should be routed on inner layers with minimized external trace lengths.

Table 74 presents the data signal group routing guidelines.

Table 74. Data Signal Group Routing Guidelines

Parameter	Definition
Signal Group	SDQ[63:0], SDQS[7:0], SDM[7:0]
PCB Topology	Daisy Chain with Parallel Termination
Reference Plane	Ground Referenced
Characteristic Trace Impedance (Z_0)	55 $\Omega \pm 15\%$
Nominal Trace Width	Inner layers: 4 mils Outer layers: 5 mils
Minimum Spacing to Trace Width Ratio	SDQ/SDM: 2:1 (e.g., 8 mil space to 4 mil trace) SDQS: 3 to 1 (e.g., 12 mil space to 4 mil trace)
Minimum Isolation Spacing to non-DDR Signals	20 mils
Package Length P1	700 mils \pm 300 mils Refer to Table 76 for package length details.
Trace Length P1+ L1 – GMCH Die-Pad to Series Termination Resistor Pad	Min = 2 inches - L2 Max = 6 inches - L3 - L2
Trace Length L2 – Series Termination Resistor Pad to First DIMM Pad	Max = 0.75 inch
Total Length P1+ L1+L2 – Total Length from GMCH to First DIMM Pad	Min = 2 inches Max = 6 inches - L3
Trace Length L3 – First DIMM Pad to Last DIMM Pad	Min = 0.25 inch Max = 2 inches
Trace Length L4 – Last DIMM Pad to Parallel Termination Resistor Pad	Max = 1 inch
Total Length P1+ L1+L2+L3 – Total Length from GMCH to Second DIMM Pad	Min = 2 inches + L3 Max = 6 inches
Series Termination Resistor (R_s)	10 $\Omega \pm 5\%$
Parallel Termination Resistor (R_t)	56 $\Omega \pm 5\%$
Maximum Recommended PCB Via Count Per Signal	6
Length Matching Requirements	Match SDQS to SCK/SCK# Refer to length matching Section 9.4.4.2 and Figure 102. SDQ/SDM to SDQS, to ± 25 mils, within each byte lane. Refer to length matching Section 9.4.4.3 and Figure 103.

NOTES:

1. Power distribution vias from R_t to V_{tt} are not included in this count.
2. The overall minimum and maximum length to the DIMM must comply with clock length matching requirements.

9.4.4.2 SDQS to Clock Length Matching Requirements

The first step in length matching is to determine the SDQS length range based on the SCK/SCK# reference length defined previously. The total length of the SDQS strobe signals, including package length, between the GMCH die-pad and the DIMMs must fall within the range defined in the formulas below. Refer to the clock section for the definition of the clock reference length. Refer to [Table 74](#) for the definition of the various trace segments.

Length range formula for DIMM0:

$X_0 = \text{SCK}[2:0]/\text{SCK}[2:0]\#$ total reference length, including package length. Refer to [Section 9.4.3.1](#) for more information.

$Y_0 = \text{SDQS}[7:0]$ total length = GMCH package + L1 + L2, as shown in [Figure 101](#), where:

$$(X_0 - 1.5 \text{ inches}) \leq Y_0 \leq (X_0 - 0.5 \text{ inch})$$

Length range formula for DIMM1:

$X_1 = \text{SCK}[5:3]/\text{SCK}[5:3]\#$ total reference length, including package length. Refer to [Section 9.4.3.1](#) for more information.

$Y_1 = \text{SDQS}[7:0]$ total length = GMCH package + L1 + L2 + L3, as shown in [Figure 101](#) where:

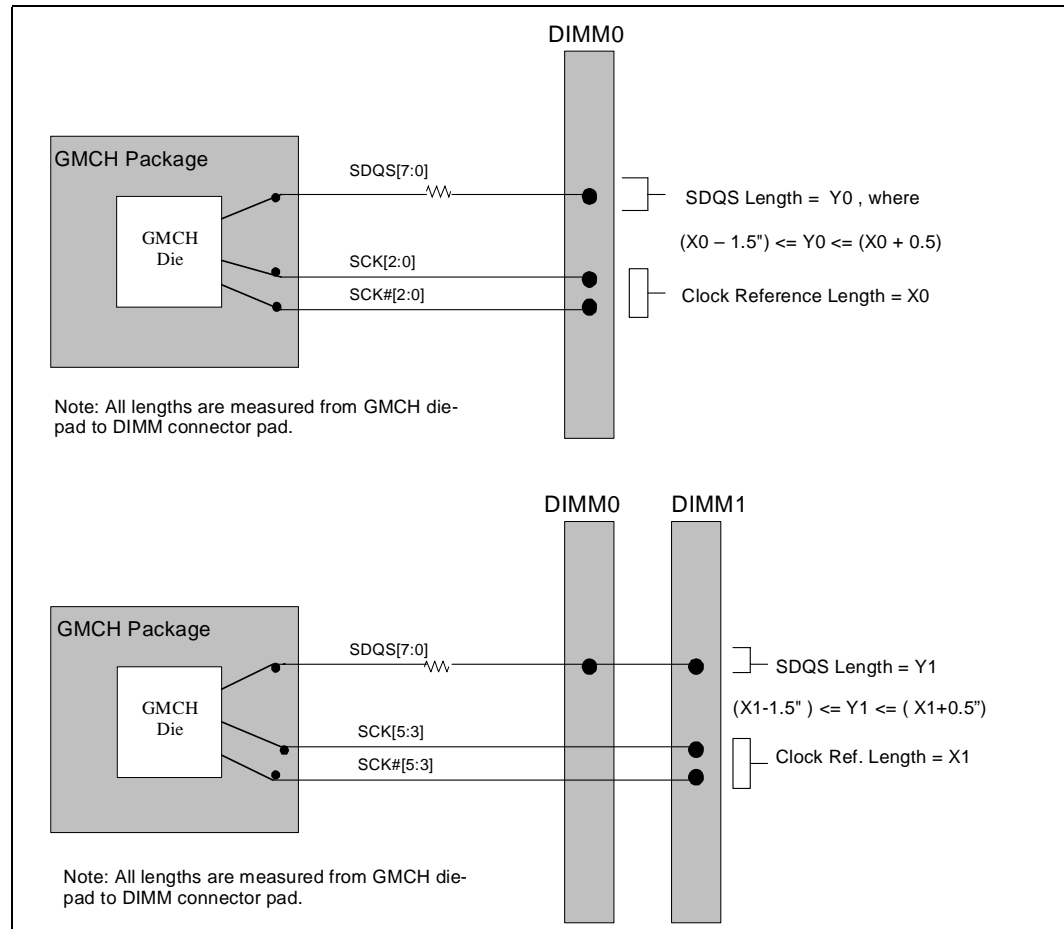
$$(X_1 - 1.5 \text{ inches}) \leq Y_1 \leq (X_1 - 0.5 \text{ inch})$$

Length matching is only performed from the GMCH to the DIMMs, and does not involve the length of L4, which may vary over its entire range. Intel recommends that routing segment length L3 between DIMM0 to DIMM1 be held fairly constant and equal to the offset between clock reference lengths X_0 and X_1 . This produces the most straightforward length-matching scenario.

Note: A nominal SDQS package length of 700 mils may be used to estimate byte lane lengths prior to performing package length compensation.

Figure 102 illustrates the SDQS to clock trace length matching diagram.

Figure 102. SDQS to Clock Trace Length Matching Diagram



9.4.4.3 Data to Strobe Length Matching Requirements

The data bit signals SDQ[63:0] are grouped by byte lanes and associated with a data mask signal, SDM[7:0], and a data strobe, SDQS[7:0]. The guidelines are as follows:

For DIMM0, this length matching includes the PCB trace length to the pads of the DIMM0 connector (L1 + L2) plus package length.

For DIMM1, the PCB trace length to the pads of the DIMM1 connector (L1 + L2 + L3) plus package length.

Length range formula for SDQ and SDM:

X = SDQS total length, including package length, as defined previously

Y = SDQ, SDM total length, including package length, within same byte lane, where

$$(X - 25 \text{ mils}) \leq Y \leq (X + 25 \text{ mils})$$

Length matching is not required from the DIMM1 to the parallel termination resistors.

9.4.4.4 SDQ to SDQS Mapping

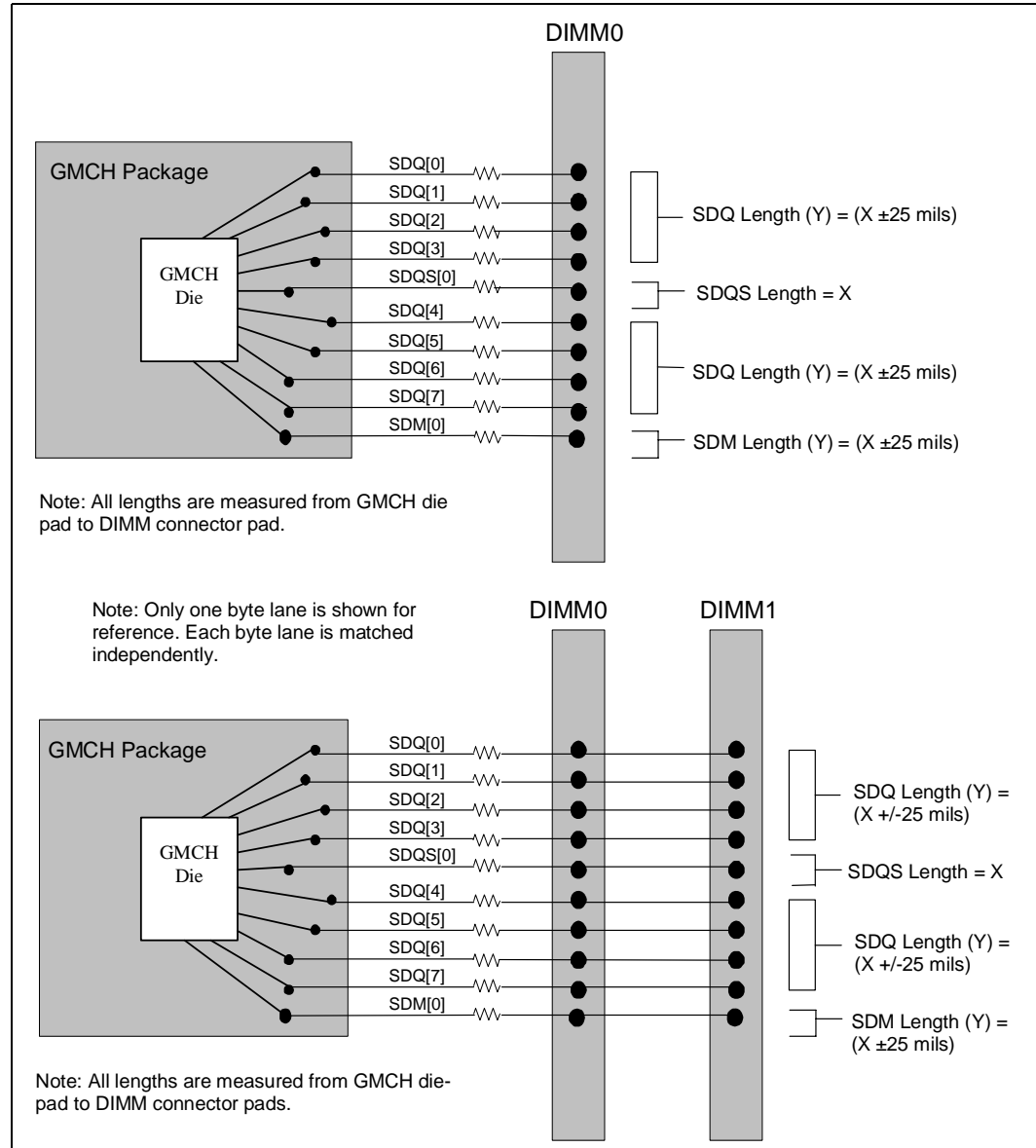
Table 75 defines the mapping between the nine byte lanes, nine mask bits, and the nine SDQS signals, as required to do the required length matching.

Table 75. SDQ/SDM to SDQS Mapping

Signal	Mask	Relative To
SDQ[7:0]	SDM[0]	SDQS[0]
SDQ[15:8]	SDM[1]	SDQS[1]
SDQ[23:16]	SDM[2]	SDQS[2]
SDQ[31:24]	SDM[3]	SDQS[3]
SDQ[39:32]	SDM[4]	SDQS[4]
SDQ[47:40]	SDM[5]	SDQS[5]
SDQ[55:48]	SDM[6]	SDQS[6]
SDQ[63:56]	SDM[7]	SDQS[7]

Figure 103 illustrates the length matching requirements between the SDQ, SDM, and SDQS signals within a byte lane.

Figure 103. SDQ/SDM to SDQS Trace Length Matching Diagram



9.4.4.5 SDQ/SDQS Signal Package Lengths

The package length data in [Table 76](#) should be used to tune the length of each SDQ, SDM, and SDQS PCB trace as required to achieve the overall length matching requirements defined in the prior sections.

Table 76. DDR SDQ/SDM/SDQS Package Lengths (Sheet 1 of 2)

Signal	Pin Number	Pkg Length (mils)	Signal	Pin Number	Pkg Length (mils)
SDQ[0]	AF2	785	SDQ[32]	AH16	766
SDQ[1]	AE3	751	SDQ[33]	AG17	558
SDQ[2]	AF4	690	SDQ[34]	AF19	510
SDQ[3]	AH2	903	SDQ[35]	AE20	579
SDQ[4]	AD3	682	SDQ[36]	AD18	408
SDQ[5]	AE2	739	SDQ[37]	AE18	458
SDQ[6]	AG4	741	SDQ[38]	AH18	658
SDQ[7]	AH3	845	SDQ[39]	AG19	596
SDQ[8]	AD6	607	SDQ[40]	AH20	677
SDQ[9]	AG5	756	SDQ[41]	AG20	730
SDQ[10]	AG7	685	SDQ[42]	AF22	562
SDQ[11]	AE8	558	SDQ[43]	AH22	702
SDQ[12]	AF5	734	SDQ[44]	AF20	563
SDQ[13]	AH4	825	SDQ[45]	AH19	644
SDQ[14]	AF7	644	SDQ[46]	AH21	716
SDQ[15]	AH6	912	SDQ[47]	AG22	783
SDQ[16]	AF8	622	SDQ[48]	AE23	592
SDQ[17]	AG8	624	SDQ[49]	AH23	752
SDQ[18]	AH9	676	SDQ[50]	AE24	666
SDQ[19]	AG10	634	SDQ[51]	AH25	817
SDQ[20]	AH7	710	SDQ[52]	AG23	639
SDQ[21]	AD9	508	SDQ[53]	AF23	667
SDQ[22]	AF10	569	SDQ[54]	AF25	707
SDQ[23]	AE11	469	SDQ[55]	AG25	783
SDQ[24]	AH10	648	SDQ[56]	AH26	834
SDQ[25]	AH11	622	SDQ[57]	AE26	701
SDQ[26]	AG13	572	SDQ[58]	AG28	808
SDQ[27]	AF14	655	SDQ[59]	AF28	756
SDQ[28]	AG11	599	SDQ[60]	AG26	782
SDQ[29]	AD12	460	SDQ[61]	AF26	748
SDQ[30]	AF13	536	SDQ[62]	AE27	673

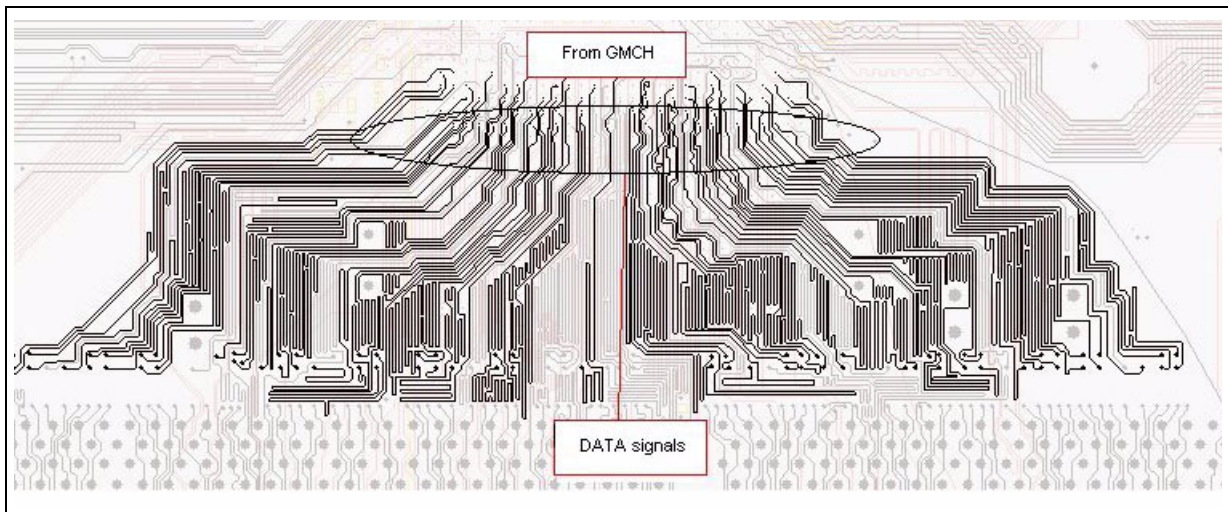
Table 76. DDR SDQ/SDM/SDQS Package Lengths (Sheet 2 of 2)

Signal	Pin Number	Pkg Length (mils)	Signal	Pin Number	Pkg Length (mils)
SDQ[31]	AH13	642	SDQ[63]	AD27	608
SDQS[0]	AG2	925	SDM[0]	AE5	838
SDQS[1]	AH5	838	SDM[1]	AE6	693
SDQS[2]	AH8	756	SDM[2]	AE9	538
SDQS[3]	AE12	466	SDM[3]	AH12	606
SDQS[4]	AH17	678	SDM[4]	AD19	492
SDQS[5]	AE21	487	SDM[5]	AD21	470
SDQS[6]	AH24	770	SDM[6]	AD24	557
SDQS[7]	AH27	858	SDM[7]	AH28	917

9.4.4.6 Memory Data Routing Example

Figure 104 is an example of a board routing for the Data signal group. The majority of the data signal route is on an internal layer. Both external layers may be used for parallel termination R-pack placement.

Figure 104. Data Signal Group Routing Example



9.4.5 Control Signals – SCKE[3:0], SCS[3:0]#

The Intel 852GM GMCH control signals, SCKE[3:0] and SCS[3:0]#, are clocked into the DDR SDRAM devices using clock signals SCK[5:0]/SCK[5:0]#. The GMCH drives the control and clock signals together, with the clocks crossing in the valid control window. The GMCH provides one chip select (CS) and one clock enable (CKE) signal per DIMM physical device row. Two chip select and two clock enable signals are routed to each DIMM. Refer to Table 77 for the CKE and CS# signal to DIMM mapping.

Table 77. Control Signal to DIMM Mapping

Signal	Relative To	GMCH Pin
SCS#[0]	DIMM0	AD23
SCS#[1]	DIMM0	AD26
SCS#[2]	DIMM1	AC22
SCS#[3]	DIMM1	AC25
SCKE[0]	DIMM0	AC7
SCKE[1]	DIMM0	AB7
SCKE[2]	DIMM1	AC9
SCKE[3]	DIMM1	AC10

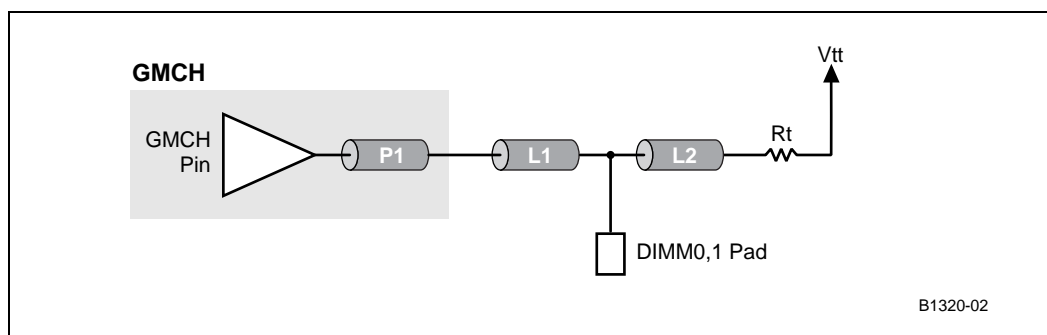
The control signal routing should transition from an external layer to an internal signal layer under the GMCH, keep to the same internal layer until transitioning back out to an external layer to connect to the appropriate pad of the DIMM connector and the parallel termination resistor. When the layout requires additional routing before the termination resistor, return to the same internal layer and transition back out to an external layer immediately prior to parallel termination resistor.

External trace lengths should be minimized. Intel suggests that the parallel termination be placed on both sides of the board to simplify routing and minimize trace lengths. All internal and external signals should be ground referenced to keep the path of return current continuous. Intel suggests that all control signals be routed on the same internal layer.

Resistor packs are acceptable for the parallel (R_t) control termination resistors, but control signals cannot be placed within the same R pack as the data or command signals. [Figure 105](#) and [Table 78](#) below present Intel's recommended topology and layout routing guidelines for the DDR-SDRAM control signals.

9.4.5.1 Control Signal Routing Topology

Figure 105. Control Signal Routing Topology



The control signals should be routed using 2:1 trace spacing to trace width ratio for signals within the DDR group, except clocks and strobes. Control signals should be routed on inner layers with minimized external trace lengths.

9.4.5.2 Control Signal Routing Guidelines

Table 78. Control Signal Routing Guidelines

Parameter	Routing Guidelines
Signal Group	SCKE[3:0], SCS[3:0]#
PCB Topology	Point-to-Point with Parallel Termination
Reference Plane	Ground Referenced
Characteristic Trace Impedance (Z_0)	$55 \Omega \pm 15\%$
Nominal Trace Width	Inner layers: 4 mils Outer layers: 5 mils
Minimum Spacing to Trace Width Ratio	2:1 (e.g., 8 mil space to 4 mil trace)
Minimum Isolation Spacing to non-DDR Signals	20 mils
Package Length P1	500 mils \pm 250 mils Refer to Table 79 for package length details.
Trace Length P1 + L1 – GMCH Die-Pad to DIMM Pad	Min = 2 inches Max = 6 inches
Trace Length L2 – DIMM Pad to Parallel Termination Resistor Pad	Max = 2 inches
Parallel Termination Resistor (R_t)	$56 \Omega \pm 5\%$
Maximum Recommended PCB Via Count Per Signal	3
Length Matching Requirements	Match CTRL to SCK[5:0]/SCK[5:0]# Refer to length matching in Section 9.4.5.3 and Figure 106 .

NOTES:

1. Recommended resistor values and trace lengths may change in a later revision of the design guide.
2. Power distribution vias from R_t to V_{tt} are not included in this count.
3. It is possible to route using two vias if one via is shared that connects to the DIMM pad and parallel termination resistor.
4. The overall maximum and minimum length to the DIMM must comply with clock length matching requirements.

9.4.5.3 Control to Clock Length Matching Requirements

The length of the control signals, between the GMCH die-pad and the DIMM must fall within the range defined below, with respect to the associated clock reference length. Refer to [Figure 105](#) for a definition of the various trace segments that make up this path. The length of trace from the DIMM to the termination resistor need not be length matched. The length matching requirements are also shown in [Figure 106](#).

Length range formula for DIMM0:

$X_0 = \text{SCK}[2:0]/\text{SCK}[2:0]\#$ total reference length, including package length. Refer to [Section 9.4.3.1](#) for more information.

$Y_0 = \text{SCS}[1:0]\#$ and $\text{SCKE}[1:0]$ total length = GMCH package length + L1, as shown in [Figure 105](#), where:

$$(X_0 - 1.5 \text{ inches}) \leq Y_0 \leq (X_0 - 0.5 \text{ inch})$$

Length range formula for DIMM1:

$X_1 = \text{SCK}[5:3]/\text{SCK}[5:3]\#$ total reference length, including package length. Refer to [Section 9.4.3.1](#) for more information.

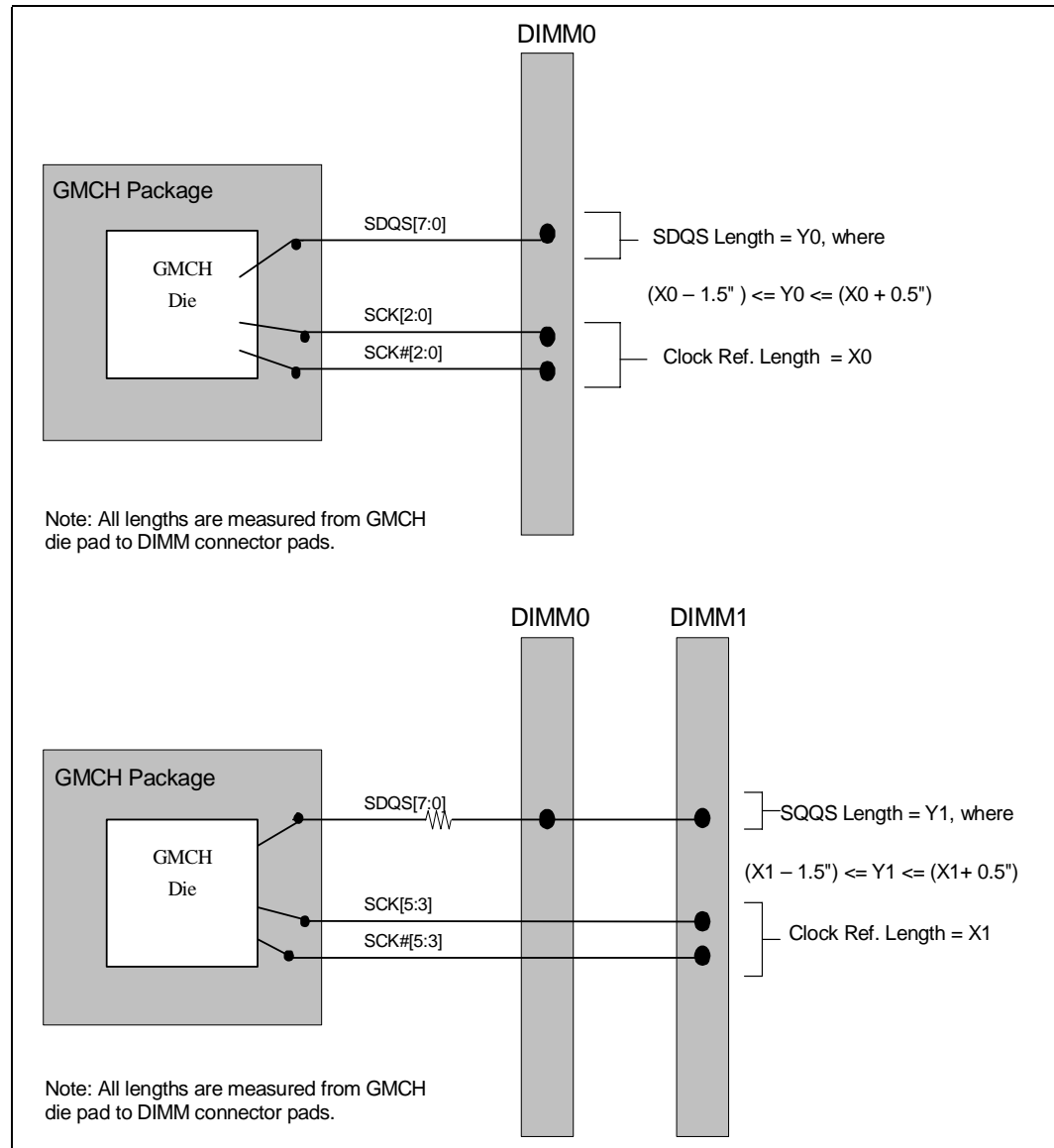
$Y_1 = \text{SCS}[3:2]\#$ and $\text{SCKE}[3:2]$ total length = GMCH package length + L1, as shown in [Figure 105](#), where:

$$(X_1 - 1.5 \text{ inches}) \leq Y_1 \leq (X_1 - 0.5 \text{ inch})$$

No length matching is required from the DIMM to the termination resistor. A nominal CS/CKE package length of 500 mils may be used to estimate baseline Mbyte lengths.

Figure 106 illustrates the length matching requirements between the control signals and clock.

Figure 106. Control Signal to Clock Trace Length Matching Diagram



9.4.5.4 Control Group Package Length Table

The package length data in the [Table 79](#) should be used to match the overall length of each command signal to its associated clock reference length.

Note: Due to the relatively small variance in package length and adequate timing margins it is acceptable to use a fixed 500 mil nominal package length for all control signals, thereby reducing the complexity of the PCB length calculations.

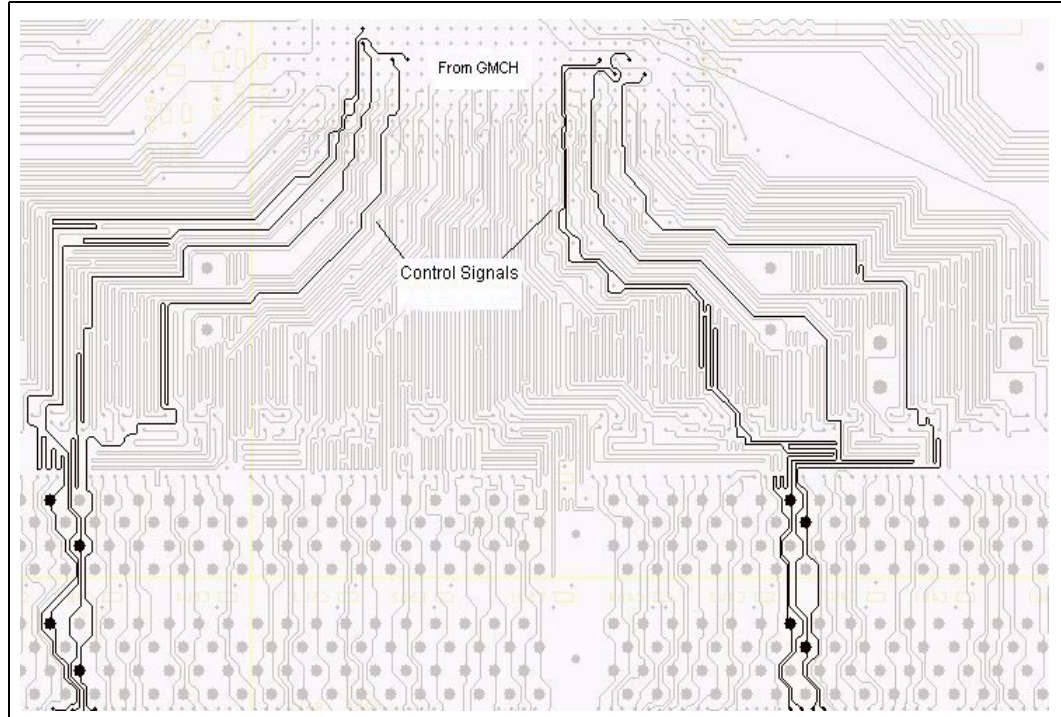
Table 79. Control Group Package Lengths

Signal	Pin Number	Package Length (mils)
SCS[0]#	AD23	502
SCS[1]#	AD26	659
SCS[2]#	AC22	544
SCS[3]#	AC25	612
SCKE[0]	AC7	443
SCKE[1]	AB7	389
SCKE[2]	AC9	386
SCKE[3]	AC10	376

9.4.5.5 Control Topology Routing Example

Figure 107 is an example of a board routing for the Control signal group.

Figure 107. Control Signal Group Routing Example



9.4.6 Command Signals – SMA[12:6,3,0], SBA[1:0], SRAS#, SCAS#, SWE#

The 82852GM command signals, SMA[12:6,3,0], SBA[1:0], SRAS#, SCAS#, and SWE#, are clocked into the DDR SDRAMs using the clock signals SCK[5:0]/SCK[5:0]#. The GMCH drives the command and clock signals together, with the clocks crossing in the valid command window. The command signal group is supported by a daisy-chain topology.

9.4.6.1 Command Signal Routing Topology

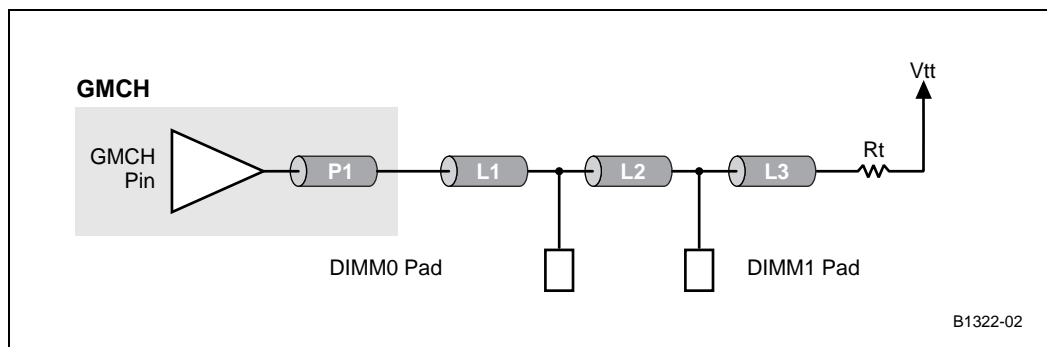
The command signal routing should transition from an external layer to an internal signal layer under the GMCH. Keep the same internal layer until transitioning to an external layer immediately prior to connecting the DIMM0 connector pad. At the via transition for DIMM0, continue the signal route on the same internal layer until transitioning back out to an external layer to connect to the pad of DIMM1. After DIMM1, transition to the same internal layer or stay on the external layer and route the signal to Rt.

Intel suggests that the parallel termination (Rt) be placed on both sides of the board to simplify routing and minimize trace lengths. All internal and external signals should be ground referenced to keep the path of the return current continuous.

Resistor packs are acceptable for the parallel command termination resistors but command signals cannot be placed within the same R-packs as data, strobe, or control signals.

Figure 108 illustrates the command routing for topology.

Figure 108. Command Routing for Topology



The command signals should be routed using a 2:1 trace spacing to trace width ratio for signals within the DDR group, except clocks and strobes. Command signals should be routed on inner layers with minimized external traces.

9.4.6.2 Command Topology Routing Guidelines

Table 80 presents Intel's recommended topology and layout routing guidelines for the DDR-SDRAM command signals routing to DIMM0 and DIMM1.

Table 80. Command Topology Routing Guidelines (Sheet 1 of 2)

Parameter	Routing Guidelines
Signal Group	SMA[12:6,3,0], SBA[1:0], SRAS#, SCAS#, SWE#
PCB Topology	Daisy-Chain with Parallel Termination
Reference Plane	Ground Referenced
Characteristic Trace Impedance (Z_0)	55 $\Omega \pm 15\%$
Nominal Trace Width	Inner layers: 4 mils Outer layers: 5 mils
Minimum Spacing to Trace Width Ratio	2:1 (e.g., 8 mil space to 4 mil trace)
Minimum Isolation Spacing to non-DDR Signals	20 mils
Package Length P1	500 mils \pm 250 mils Refer to Table 81 for package length details.
Trace Length P1+ L1	Min = 2 inches Max = 5.5 inches
Trace Length P1+ L1+L2+L3	Max = 7.5 inches
Trace Length L2 – Total DIMM to DIMM spacing	Max = 2 inches

NOTES:

1. Recommended resistor values and trace lengths may change in a later revision of the design guide.
2. Power distribution vias from Rt to Vtt are not included in this count.
3. The overall maximum and minimum length to the DIMM must comply with clock length matching requirements.
4. It is possible to route using three vias if one via is shared that connects to the DIMM1 pad and parallel termination resistor.

Table 80. Command Topology Routing Guidelines (Sheet 2 of 2)

Parameter	Routing Guidelines
Trace Length L3 – Second DIMM Pad to Parallel Resistor Pad	Max = 1.5 inches
Parallel Termination Resistor (Rt)	56 Ω \pm 5%
Maximum Recommended PCB Via Count Per Signal	6
Length Matching Requirements	CMD to SCK/SCK# Refer to length matching Section 9.4.6.3 and Figure 109 for details.

NOTES:

1. Recommended resistor values and trace lengths may change in a later revision of the design guide.
2. Power distribution vias from Rt to Vtt are not included in this count.
3. The overall maximum and minimum length to the DIMM must comply with clock length matching requirements.
4. It is possible to route using three vias if one via is shared that connects to the DIMM1 pad and parallel termination resistor.

9.4.6.3 Command Topology Length Matching Requirements

The routing length of the command signals, between the GMCH die-pad and the DIMM must be within the range defined below, with respect to the associated clock reference length. Refer to [Figure 108](#) for a definition of the various PCB trace segments. The length of trace from the DIMM to the termination resistor need not be length matched.

Length range formula for DIMM0:

X_0 = SCK[2:0]/SCK[2:0]# total reference length, including package length. Refer to [Section 9.4.3.1](#) for more information.

Y_0 = CMD signal total length = GMCH package + L1, as shown in [Figure 108](#), where:

$$(X_0 - 1.5 \text{ inches}) \leq Y_0 \leq (X_0 + 1 \text{ inch})$$

Length range formula for DIMM1:

X_1 = SCK[5:3]/SCK[5:3]# total reference length, including package length. Refer to [Section 9.4.3.1](#) for more information.

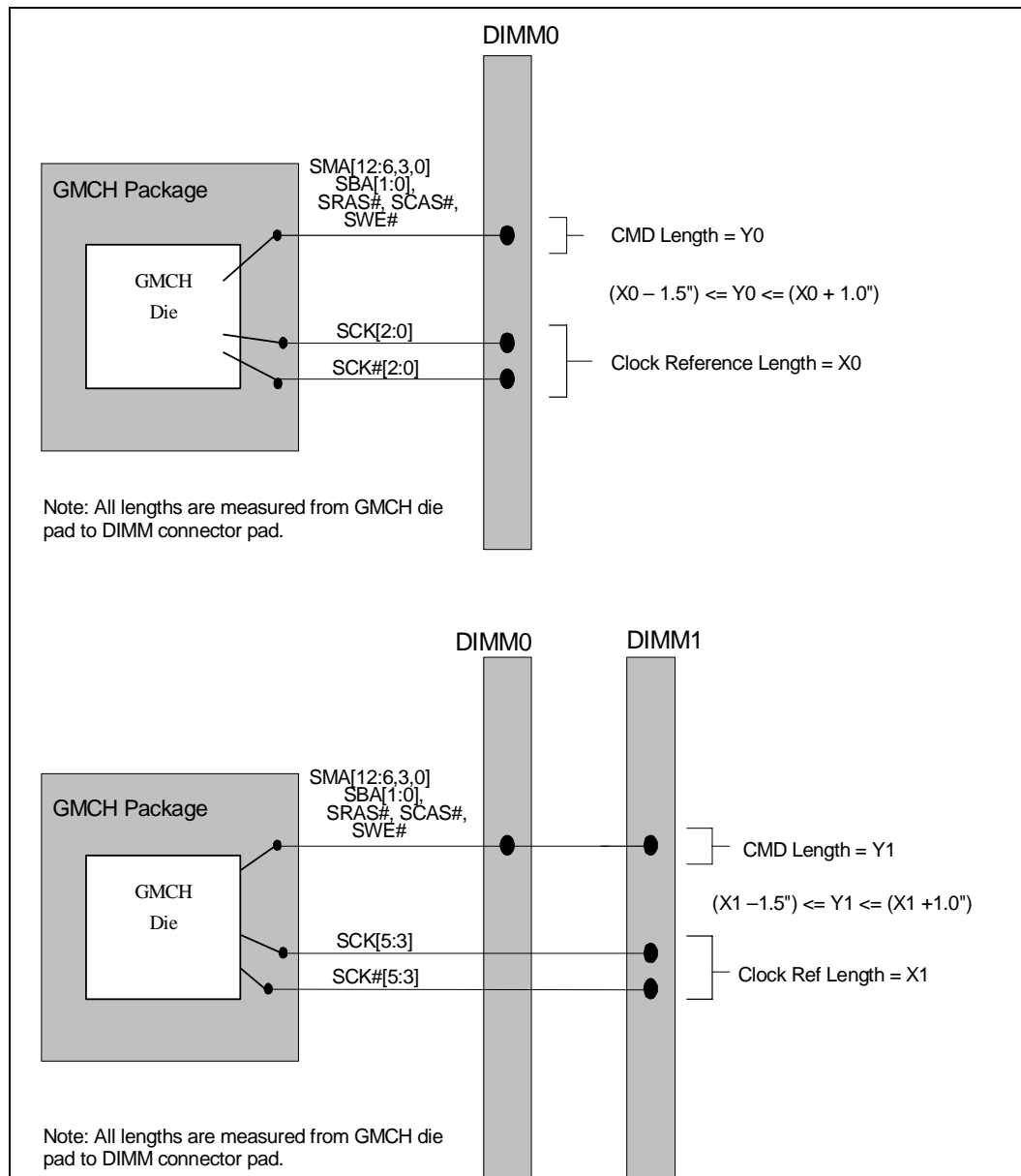
Y_1 = CMD signal total length = GMCH package + L1 + L2 + L3, as shown in [Figure 108](#), where:

$$(X_1 - 1.5 \text{ inches}) \leq Y_1 \leq (X_1 + 1 \text{ inch})$$

No length matching is required from DIMM1 to the termination resistor. A nominal CMD package length of 500 mils may be used to estimate baseline PCB lengths. Refer to [Section 9.3](#) for more details on package length compensation.

Figure 109 illustrates the length matching requirements between the command signals and clock.

Figure 109. Topology Command Signal to Clock Trace Length Matching Diagram



9.4.6.4 Command Group Package Length Table

The package length data in [Table 81](#) should be used to match the overall length of each command signal to its associated clock reference length.

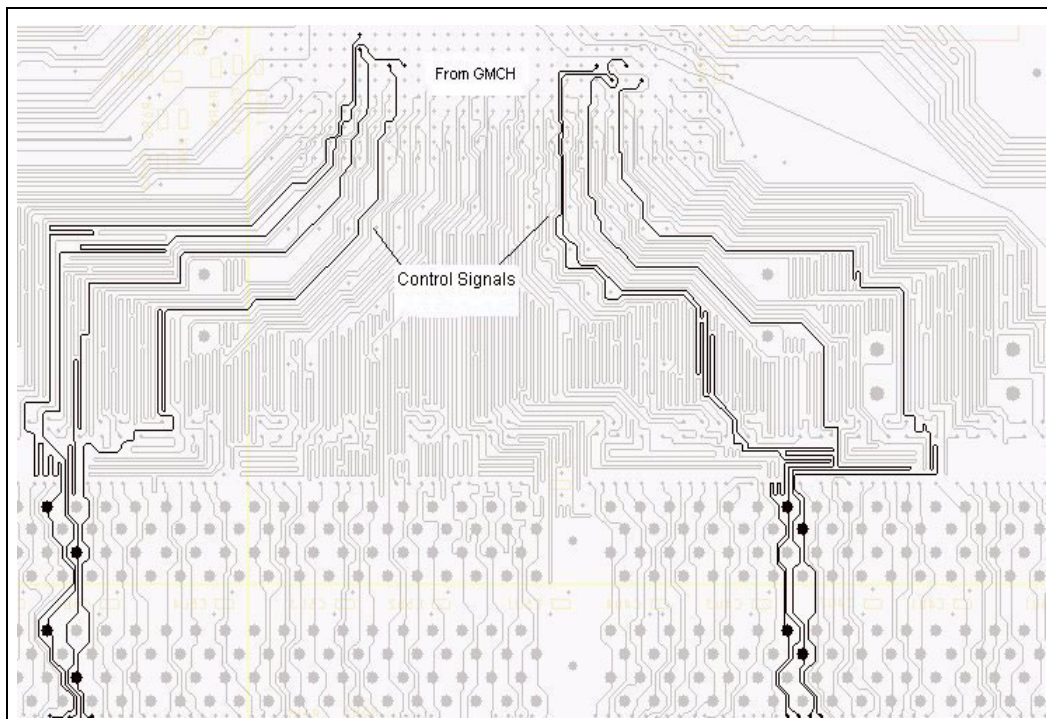
Table 81. Command Group Package Lengths

Signal	Pin Number	Pkg Length (mils)
SMA[0]	AC18	420
SMA[3]	AD17	472
SMA[6]	AD8	591
SMA[7]	AD7	596
SMA[8]	AC6	630
SMA[9]	AC5	681
SMA[10]	AC19	377
SMA[11]	AD5	683
SMA[12]	AB5	609
SBA[0]	AD22	592
SBA[1]	AD20	435
SCAS#	AC24	562
SRAS#	AC21	499
SWE#	AD25	751

9.4.6.5 Control Topology Routing Example

Figure 110 is an example of a board routing for the Control signal group.

Figure 110. Control Signal Group Routing Example



9.4.7 CPC Signals – SMA[5,4,2,1], SMAB[5,4,2,1]

The 82852GM control signals, SMA[5,4,2,1] and SMAB[5,4,2,1], are common clocked signals. They are clocked into the DDR SDRAM devices using clock signals SCK[5:0]/SCK[5:0]#. The GMCH drives the CPC and clock signals together, with the clocks crossing in the valid control window. The GMCH provides one set of CPC signals per DIMM slot. Refer to Table 82 for the SMA and SMAB signal to DIMM mapping.

Table 82. Control Signal to DIMM Mapping

Signal	Relative To	GMCH Pin
SMA[1]	DIMM0	AD14
SMA[2]	DIMM0	AD13
SMA[4]	DIMM0	AD11
SMA[5]	DIMM0	AC13
SMAB[1]	DIMM1	AD16
SMAB[2]	DIMM1	AC12
SMAB[4]	DIMM1	AF11
SMAB[5]	DIMM1	AD10

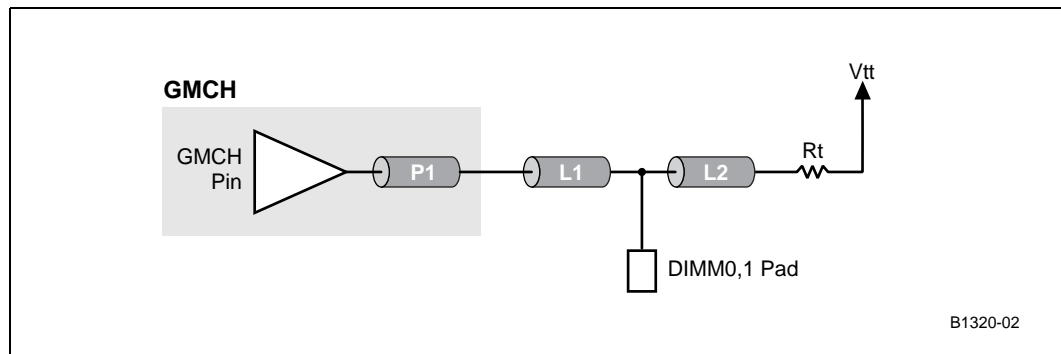
The guidelines below should be followed.

- The CPC signal routing should transition from an external layer to an internal signal layer under the GMCH.
- Keep to the same internal layer until transitioning back out to an external layer to connect to the appropriate pad of the DIMM connector and the parallel termination resistor.
- If the layout requires additional routing before the termination resistor, return to the same internal layer and transition back out to an external layer immediately prior to parallel termination resistor.
- External trace lengths should be minimized. Intel suggests that the parallel termination be placed on both sides of the board to simplify routing and minimize trace lengths.
- All internal and external signals should be ground reference to keep the path of return current continuous. Intel suggests that all CPC signals be routed on the same internal layer.
- Resistor packs are acceptable for the parallel (R_t) CPC termination resistors. [Figure 111](#) and [Table 83](#) present the recommended topology and layout routing guidelines for the DDR-SDRAM CPC signals.

9.4.7.1 CPC Signal Routing Topology

[Figure 111](#) illustrates the CPC control signal routing topology.

Figure 111. CPC Control Signal Routing Topology



The CPC signals should be routed using 2:1 trace space to width ratio for signals within the DDR group, except clocks and strobes. CPC signals should be routed on inner layers with minimized external trace lengths.

9.4.7.2 CPC Signal Routing Guidelines

Table 83 presents CPC control signal routing guidelines.

Table 83. CPC Control Signal Routing Guidelines

Parameter	Routing Guidelines
Signal Group	SMA[5,4,2,1], SMAB[5,4,2,1]
PCB Topology	Point-to-Point with Parallel Termination
Reference Plane	Ground Referenced
Characteristic Trace Impedance (Z_0)	$55 \Omega \pm 15\%$
Nominal Trace Width	Inner layers: 4 mils Outer layers: 5 mils
Minimum Spacing to Trace Width Ratio	2:1 (e.g., 8 mil space to 4 mil trace)
Minimum Isolation Spacing to non-DDR Signals	20 mils
Package Length P1	500 mils \pm 250 mils Refer to Table 84 for package length details.
Trace Length P1 + L1	Min = 2 inches Max = 6 inches
Trace Length L2 – DIMM Pad to Parallel Termination Resistor Pad	Max = 2 inches
Parallel Termination Resistor (R_t)	$56 \Omega \pm 5\%$
Maximum Recommended PCB Via Count Per Signal	3
Length Matching Requirements	Match CPC to SCK[5:0]/SCK[5:0]# Refer to length matching Section 9.4.7.3 and Figure 112 for details.

NOTES:

1. Recommended resistor values and trace lengths may change in a later revision of the design guide.
2. Power distribution vias from R_t to V_{tt} are not included in this count.
3. It is possible to route using two vias if one via is shared that connects to the DIMM pad and parallel termination resistor.
4. The overall maximum and minimum length to the DIMM must comply with clock length matching requirements.

9.4.7.3 CPC to Clock Length Matching Requirements

The total length of the CPC signals, between the GMCH die-pad and the DIMM must fall within the range defined below, with respect to the associated clock reference length. Refer to Figure 111 for a definition of the various trace segments. The length the trace from the DIMM to the termination resistor need not be length matched. The length matching requirements are also shown in Figure 112. A table of CPC signal package length is provided at the end of this section.

Length range formula for DIMM0:

X_0 = SCK[2:0]/SCK[2:0]# total reference length, including package length. Refer to Section 9.4.1 for more information.

Y_0 = SMA[5,4,2,1] total length = GMCH Package + L1, as shown in Figure 111, where:

$$(X_0 - 1.5 \text{ inches}) \leq Y_0 \leq (X_0 - 0.5 \text{ inch})$$

Length range formula for DIMM1:

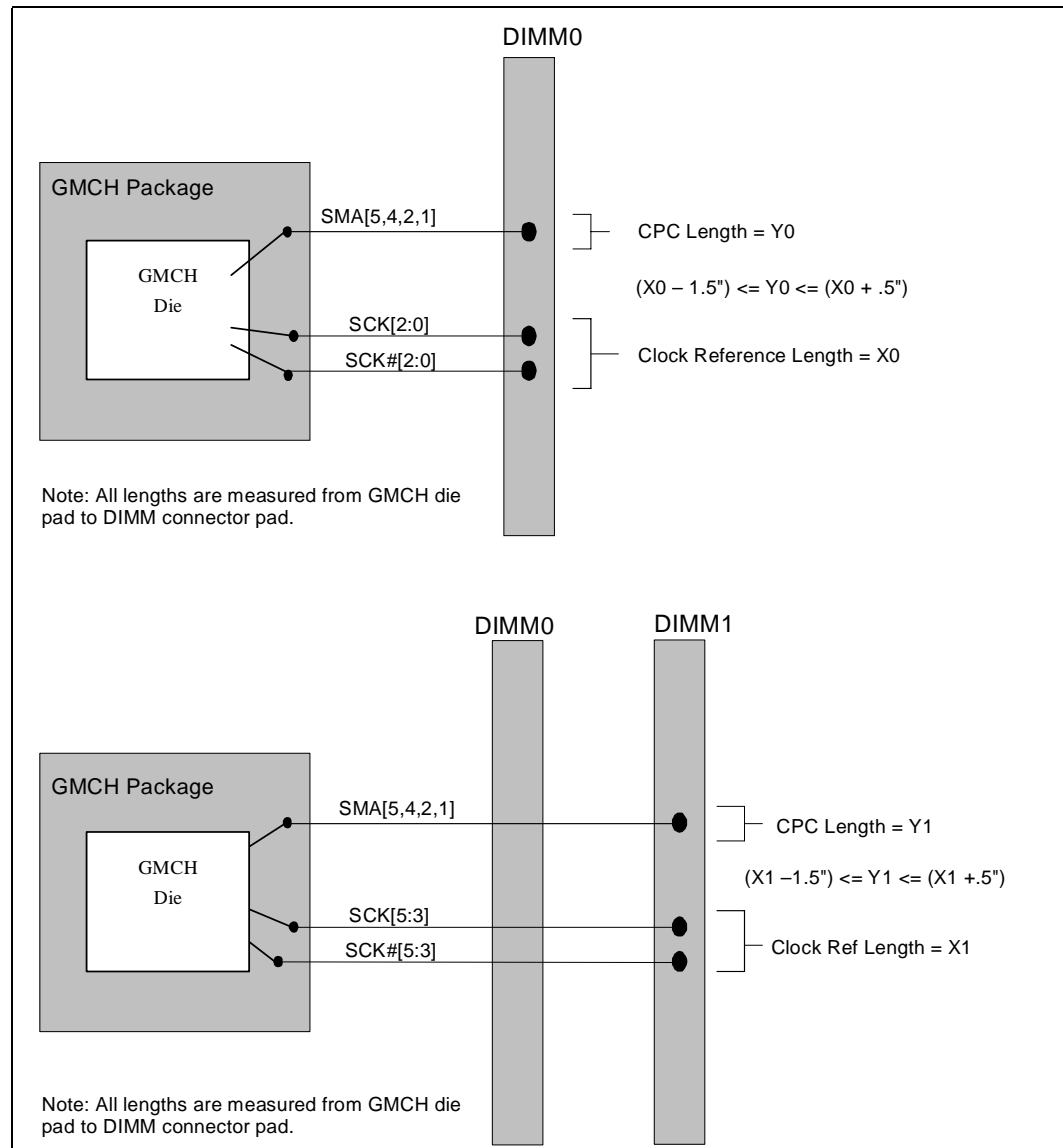
$X_1 = \text{SCK}[5:3]/\text{SCK}[5:3]\#$ total reference length, including package length. Refer to [Section 9.4.1](#) for more information.

$Y_1 = \text{SMAB}[5,4,2,1]$ total length = GMCH Package + L1, as shown in [Figure 111](#), where:

$$(X_1 - 1.5 \text{ inches}) \leq Y_1 \leq (X_1 + 0.5 \text{ inch})$$

No length matching is required from DIMM1 to the termination resistor. [Figure 112](#) illustrates the length matching requirements between the CPC signals and clock. A nominal CPC package length of 500 mils may be used to estimate baseline PCB lengths.

Figure 112. CPC Signals to Clock Length Matching Diagram



9.4.7.4 CPC Group Package Length Table

The package length data in [Table 84](#) should be used to match the overall length of each CPC signal to its associated clock reference length.

Table 84. CPC Group Package Lengths

Signal	Pin Number	Pkg Length (mils)
SMA[1]	AD14	398
SMA[2]	AD13	443
SMA[4]	AD11	430
SMA[5]	AC13	346
SMAB[1]	AD16	427
SMAB[2]	AC12	395
SMAB[4]	AF11	716
SMAB[5]	AD10	631

9.4.8 Feedback – RCVENOUT#, RCVENIN#

The 82852GM provides a feedback signal called 'receive enable' (RCVENIN#), which is used to measure timing for memory read data. The Intel® 852GM chipset has the RCVENOUT# signal shunted directly to RCVENIN# inside the package to reduce timing variation. With this change it is no longer necessary to provide an external connection. However, Intel recommends that both signals be transitioned to the bottom side with vias located adjacent to the package ball to facilitate probing.

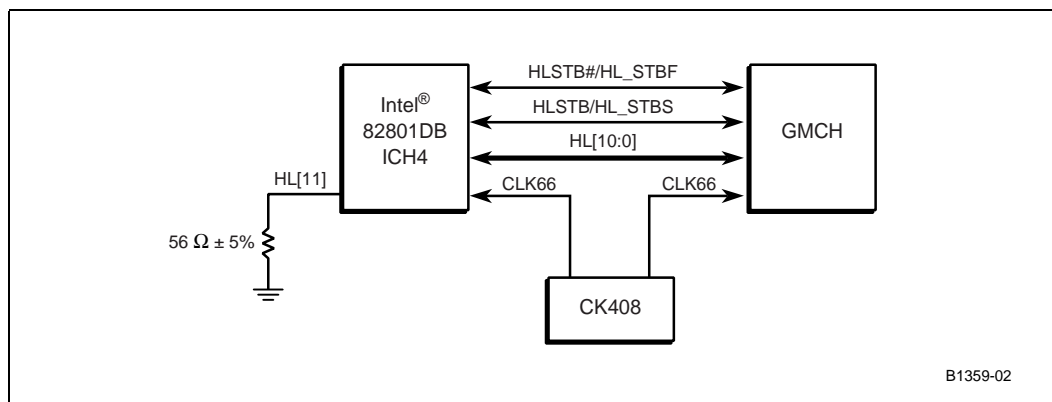
Hub Interface

10

The Intel® 82852GM GMCH and Intel® 82801DB ICH4 (ICH4) pin-map assignments have been optimized to simplify the hub interface routing between these devices. Intel recommends that the hub interface signals be routed directly from the GMCH to the ICH4 with all signals referenced to VSS. Keep layer transitions to a minimum. When a layer change is required, use only two vias per net and keep all data signals and associated strobe signals on the same layer.

The hub interface signals are broken into two groups: data signals (HL) and strobe signals (HLSTB). For the 8-bit hub interface, HL[10:0] are associated with the data signals while HLSTB/HLSTBS and HLSTB#/HLSTBF are associated with the strobe signals. Figure 113 shows the hub interface routing example.

Figure 113. Hub Interface Routing Example



10.1 Hub Interface Compensation

This section documents the routing guidelines for the 8-bit Hub Interface using enhanced (parallel) termination. This Hub Interface connects the ICH4 to the Intel® 852GM chipset Graphics Memory Controller Hub (82852GM). The ICH4 should strap its HLRCOMP pin to $V_{CCH1} = 1.5$ V, as summarized in Table 85. The GMCH should strap its HLRCOMP pin to $V_{CCHL} = 1.2$ V, as summarized in Table 85. The trace impedance must equal $55 \Omega \pm 15\%$.

Table 85. Hub Interface RCOMP Resistor Values

Component	Trace Impedance	HLRCOMP Resistor Value	HLRCOMP Resistor Tied to
Intel® 82801DB ICH4	$55 \Omega \pm 15\%$	$48.7 \Omega \pm 1\%$	V_{CC1_5}
GMCH	$55 \Omega \pm 15\%$	$27.4 \Omega \pm 1\%$	V_{CC1_2}

10.2 Hub Interface Data HL[10:0] and Strobe Signals

The Hub Interface HL[10:0] data signals should be routed on the same layer as Hub Interface Strobe signals.

10.2.1 HL[10:0] and Strobe Signals Internal Layer Routing

Route the traces 4 mils wide with 8 mils trace spacing (4 on 8) and 20 mils spacing from other signals. In order to break out of the GMCH and ICH4 packages, the HL[10:0] signals may be routed 4 on 7. The signal must be separated to 4 on 8 within 300 mils from the package.

The maximum HL[10:0] signal trace length is six inches. The HL[10:0] signals must be matched within ± 100 mils of the HLSTB differential pair. There is no explicit matching requirement between the individual HL[10:0] signals.

Route the hub interface strobe signals HLSTB and HLSTB# as a differential pair, 4 mils wide with 8 mils trace spacing (4 on 8). The maximum length for strobe signals is six inches. Each strobe signal must be the same length and each HL[10:0] signal must be matched to within ± 100 mils of the strobe signals. Perform all length matching from the GMCH die to the ICH4 die (pad-to-pad). [Table 86](#) presents the hub interface signals internal layer routing summary. Refer to package lengths in [Table 87](#) and [Table 88](#).

Table 86. Hub Interface Signals Internal Layer Routing Summary

Signal	Min. length (inches)	Max. length (inches)	Width (mils)	Space (mils)	Mismatch length (mils)	Relative To	Space with other signals (mils)	Notes
HL[10:0]	1.5	6	4	8	± 100	Differential HLSTB pair	20	
HLSTB and HLSTB#	1.5	6	4	8	± 100	Data lines	20	HLSTB and HLSTB# must be the same length (± 10 mils)

Table 87. Hub Interface Package Lengths for Intel® 82801DB ICH4 (A1/A2 and B0 stepping)

Signal	Pin Number	Package Length (mils) A1/A2	Package Length (mils) B0
HI[0]	L19	551	584
HI[1]	L20	562	596
HI[2]	M19	552	588
HI[3]	M21	567	602
HI[4]	P19	599	645
HI[5]	R19	627	669
HI[6]	T20	623	674
HI[7]	R20	593	622
HI[8]	P23	668	701
HI[9]	L22	559	593
HI[10]	N22	682	729
clk66	T21	605	643
HI_STB/ HI_STBFS	P21	541	604
HI_STB#/ HI_STBS	N20	565	612

Table 88. Hub Interface Package Lengths for the Intel® 852GM Chipset

Signal	Pin Number	Package Length (mils)
HL[0]	U7	281
HL[1]	U4	408
HL[2]	U3	476
HL[3]	V3	484
HL[4]	W2	551
HL[5]	W6	355
HL[6]	V6	328
HL[7]	W7	343
HL[8]	T3	499
HL[9]	V5	399
HL[10]	V4	457
GCLKIN	Y3	539
HLSTB	W3	504
HLSTB#	V2	548

10.2.2 Terminating HL[11]

The HL[11] signal exists on the ICH4 but not the GMCH and is not used on the platform. HL[11] must be pulled down to ground via a 56 Ω resistor.

10.2.3 Intel® 82801DB I/O Controller Hub 4 (ICH4) Strobe Signal Pin Map Change

As a clarification, previous revisions of the *Intel® I/O Controller Hub (ICH4) Datasheet* may have the balls for the Hub Interface side band strobes incorrectly labeled in the ICH4 pin map. The correct signal names on the pin map that correspond to balls P21 and N20 are HLSTB and HLSTB#, respectively.

10.3 Hub VREF/VSWING Generation/Distribution

The Hub Interface reference voltage (V_{REF}) is used on both the GMCH (HLVREF) and the ICH4 (HIREF). The Hub interface also has a reference voltage (V_{SWING}) for the GMCH (PSWING) and the ICH4 (HI_VSWING), to control voltage swing and impedance strength of the Hub Interface buffers. The V_{REF} voltage requirements must be set appropriately for proper operation. [Section 10.3.1](#) to [Section 10.3.3](#) provides details on the different options for V_{REF} and V_{SWING} voltage divider circuitry requirements.

[Table 89](#) presents the V_{REF} and V_{SWING} voltage specifications.

Table 89. Hub Interface V_{REF}/V_{SWING} Generation Circuit Specifications

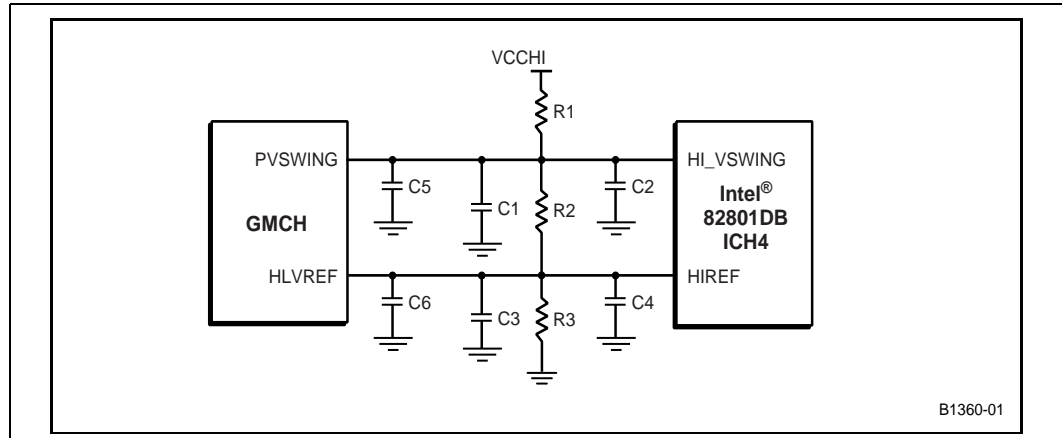
V_{REF}	V_{SWING}	Notes
HIREF (ICH4) HLVREF (GMCH)	HI_VSWING (ICH4) PSWING (GMCH)	
350 mV \pm 8%	800 mV \pm 8%	Refer to Section 10.3.1 , Section 10.3.2 and Section 10.3.3 for recommendations for the V_{REF}/V_{SWING} voltage generation circuitry. Refer to Table 90 through Table 92 for Intel's recommended resistor values.

10.3.1 Single Generation Reference Voltage Divider Circuit

The GMCH and ICH4 may share the same single voltage divider circuit. This option provides one voltage divider circuit to generate both V_{REF} and V_{SWING} reference voltage. The reference voltage for both V_{REF} and V_{SWING} must meet the voltage specification in [Table 89](#). When the voltage specifications are not met, an individual locally generated voltage divider circuit is required. The maximum trace length from the GMCH to ICH4 is four inches or less. The voltage divider circuit should be placed midway between the GMCH and ICH4. Normal care needs to be taken to minimize crosstalk to other signals (< 10-15 mV). When the trace length exceeds four inches, the locally generated voltage reference divider should be used. Refer to [Section 10.3.2](#) for more details.

[Figure 114](#) illustrates the single V_{REF}/V_{SWING} voltage generation circuit for Hub Interface.

Figure 114. Single V_{REF}/V_{SWING} Voltage Generation Circuit for Hub Interface



The resistor values, R1, R2, and R3 must be rated at one percent tolerance. Refer to Table 90 for Intel's recommended resistor values. The selected resistor values ensure that the reference voltage tolerance is maintained over the input leakage specification. Two 0.1 μ F capacitors (C1 and C3) should be placed close to the divider. In addition, the 0.01- μ F bypass capacitor (C2, C4, C5, and C6) should be placed within 0.25 inch of HLVSING/HIREF pin (for C4 and C6) and HI_VSWING/PVSING pin (for C2 and C5).

Table 90 presents the recommended resistor values for a single V_{REF}/V_{SWING} divider circuit.

Table 90. Recommended Resistor Values for Single V_{REF}/V_{SWING} Divider Circuit

	Recommended Resistor Values			V_{CCHI}
Option 1	$R1 = 80.6 \Omega \pm 1\%$	$R2 = 51.1 \Omega \pm 1\%$	$R3 = 40.2 \Omega \pm 1\%$	1.5 V
Option 2	$R1 = 255 \Omega \pm 1\%$	$R2 = 162 \Omega \pm 1\%$	$R3 = 127 \Omega \pm 1\%$	1.5 V
Option 3	$R1 = 226 \Omega \pm 1\%$	$R2 = 147 \Omega \pm 1\%$	$R3 = 113 \Omega \pm 1\%$	1.5 V
	C1 and C3 = 0.1 μ F (near divider) C2, C4, C5, C6 = 0.01 μ F (near component)			

10.3.2 Locally Generated Reference Voltage Divider Circuit

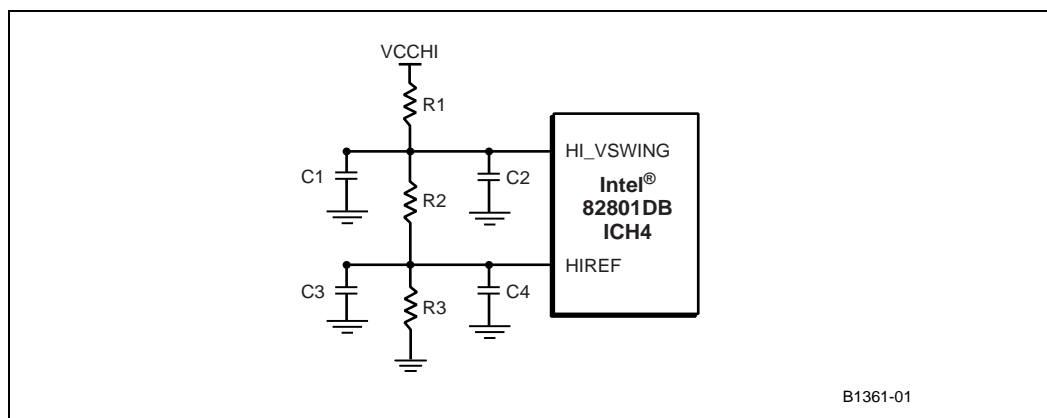
Section 10.3.2.1 and Section 10.3.2.2 provides the option to generate the voltage references separately for GMCH and ICH4. Use this option if the routing distance between GMCH and ICH4 is greater than 4 inches.

10.3.2.1 ICH4 Single Generated Voltage Reference Divider Circuit

This option allows the ICH4 to use one voltage divider circuit to generate both HIREF and HI_VSWING voltage references. The reference voltage for both HIREF and HI_VSWING must meet the voltage specification in Table 89. The resistor values R1, R2, and R3 must be rated at 1% tolerance (see Table 90). Normal care needs to be taken to minimize crosstalk to other signals (< 10-15 mV). When the voltage specifications are not met, individually generated voltage divider circuit for HIREF and HI_VSWING are required.

Figure 115 shows an ICH4 locally generated voltage divider circuit.

Figure 115. Intel® 82801DB ICH4 Locally Generated Reference Voltage Divider Circuit

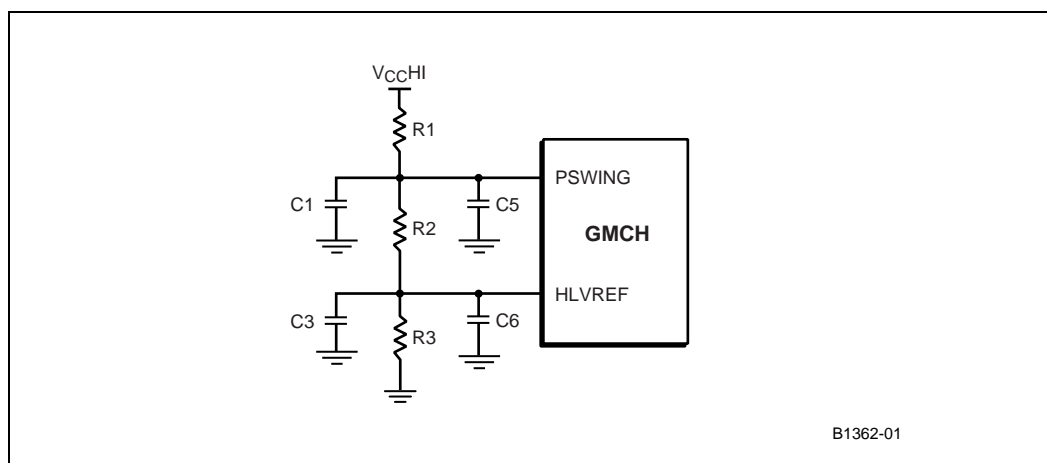


10.3.2.2 GMCH Single Generated Voltage Reference Divider Circuit

This option allows the GMCH to use one voltage divider circuit to generate both HLVREF and HLPVSWING voltage references. The reference voltage for both HLVREF and HLPVSWING must meet the voltage specification in Table 89. The resistor values R1, R2, and R3 must be rated at 1% tolerance (see Table 90). Normal care needs to be taken to minimize crosstalk to other signals (< 10-15 mV). When the voltage specifications are not met, individually generated voltage divider circuits for HLVREF and PSWING are required.

Figure 116 shows the GMCH locally generated reference voltage divider circuit.

Figure 116. GMCH Locally Generated Reference Voltage Divider Circuit



10.3.3 Separate GMCH and Intel® 82801DB I/O Controller Hub (ICH4) Voltage Generation/Separate Divider Circuits for VREF and VSWING

Section 10.3.3.1 and Section 10.3.3.2 provides the option to generate individual voltage reference for VREF and VSWING separately for GMCH and ICH4.

10.3.3.1 Separate ICH4 Voltage Divider Circuits for HIVREF and HI_VSWING

This option allows for tuning the voltage references HIVREF and HI_VSWING individually. The reference voltage for both HIVREF and HI_VSWING must meet the voltage specification in Table 89. Normal care needs to be taken to minimize crosstalk to other signals (< 10-15 mV).

Figure 117 shows individual HIVREF and HI_VSWING voltage reference divider circuits for the ICH4.

Figure 117. Individual HIVREF and HI_VSWING Voltage Reference Divider Circuits for the Intel® 82801DB ICH4

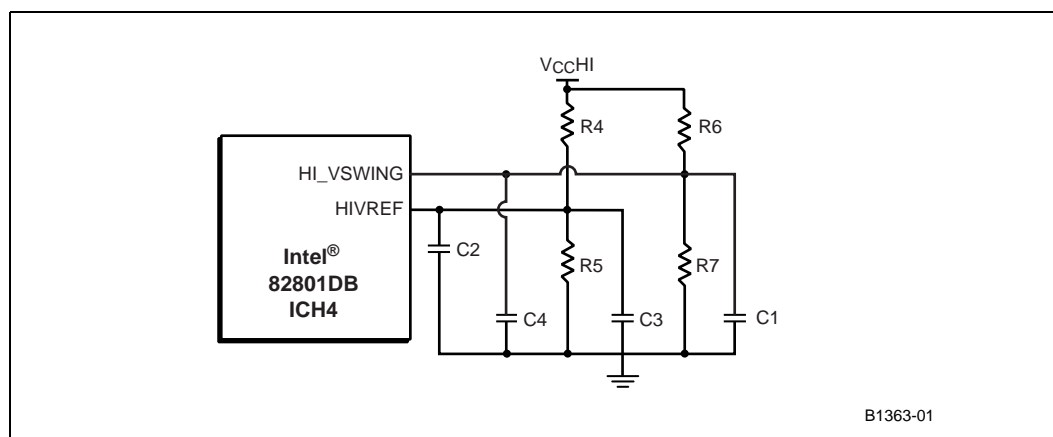


Table 91 presents the recommended resistor values for HIVREF and HIVSWING divider circuits for the ICH4.

Table 91. Recommended Resistor Values for HIVREF and HI_VSWING Divider Circuits for the Intel® 82801DB ICH4

Signal	Recommended Resistor Values	V _{CCHI}	Capacitor value
HIVREF (350 mV)	R4 = 487 Ω ± 1% R5 = 150 Ω ± 1%	V _{CCHI} = 1.5 V	C3 = 0.1 μF (near divider) C2 = 0.01 μF (near component)
HI_VSWING (800 mV)	R6 = 130 Ω ± 1% R7 = 150 Ω ± 1%	V _{CCHI} = 1.5 V	C1 = 0.1 μF (near divider) C4 = 0.01 μF (near component)

10.3.3.2 Separate GMCH Voltage Divider Circuits for HLVREF and PSWING

This option allows for tuning the voltage references HLVREF and PSWING individually. The reference voltage for both HLVREF and PSWING must meet the voltage specification in Table 89. Normal care needs to be taken to minimize crosstalk to other signals (< 10-15 mV).

Figure 118 shows the individual HLVREF and PSWING voltage reference divider circuits for GMCH.

Figure 118. Individual HLVREF and PSWING Voltage Reference Divider Circuits for GMCH

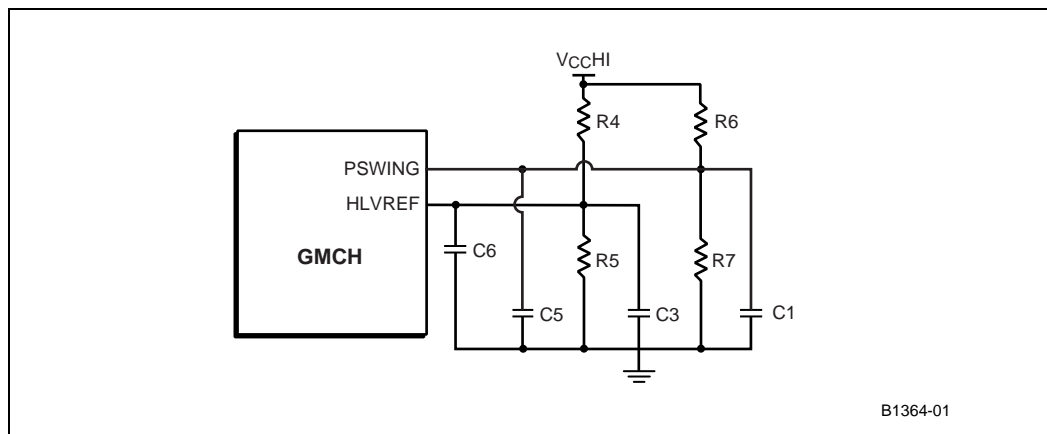


Table 92 presents the recommended resistor values for HLVREF and PSWING divider circuits for GMCH.

Table 92. Recommended Resistor Values for HLVREF and PSWING Divider Circuits for GMCH

Signal Name	Recommended Resistor Values	V _{CCHI}	Capacitor
HLVREF (350 mV)	R4 = 324 Ω ± 1% R5 = 100 Ω ± 1%	V _{CCHI} = 1.5 V	C3 = 0.1 μF (near divider); C6 = 0.01 μF (near component)
PSWING (800 mV)	R6 = 86.6 Ω ± 1% R7 = 100 Ω ± 1%	V _{CCHI} = 1.5 V	C1 = 0.1 μF (near divider) C5 = 0.01 μF (near component)

10.3.4 Hub Interface Decoupling Guidelines

To improve I/O power delivery, use two 0.1 μF capacitors per each component (i.e., the ICH4 and GMCH). These capacitors should be placed within 50 mils from each package, adjacent to the rows that contain the Hub Interface. When the layout allows, wide metal fingers running on the V_{SS} side of the board should connect the V_{CCHI} side of the capacitors to the V_{CCHI} power pins. Similarly, if layout allows, metal fingers running on the V_{CCHI} side of the board should connect the ground side of the capacitors to the V_{SS} power pins.

I/O Subsystem

11

11.1 SYS_RESET# Usage Model

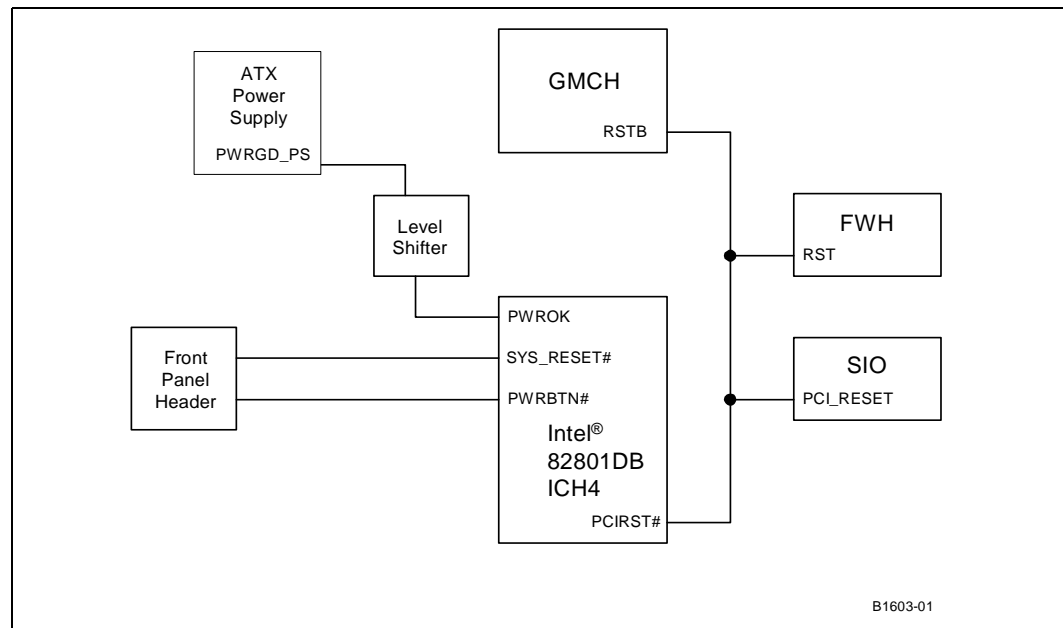
The System Reset signal (SYS_RESET#) on the Intel® 82801DB I/O Controller Hub 4 (ICH4) may be connected directly to the reset button on the system's front panel, provided that the front panel header pulls this signal up to 3.3 V standby through a weak pull-up resistor. The ICH4 has internal logic to debounce this signal for 16 ms, allowing the SMBus to go idle before resetting the system. This helps prevent slave devices on the SMBus from hanging because they are reset in the middle of a cycle.

When a Celeron Processor ITP700FLEX debug port is implemented on the system, Intel recommends that the DBR# signal of the ITP interface be connected to SYS_RESET# as well.

11.2 PWRBTN# Usage Model

The Power Button signal (PWRBTN#) on the ICH4 may be connected directly to the power button on the system's front panel. This signal is internally pulled-up to 3.3 V standby through a weak pull-up resistor (24 kΩ nominal). The ICH4 has internal logic to debounce this signal for 16 ms. [Figure 119](#) illustrates the SYS_RESET# and PWRBTN# connection.

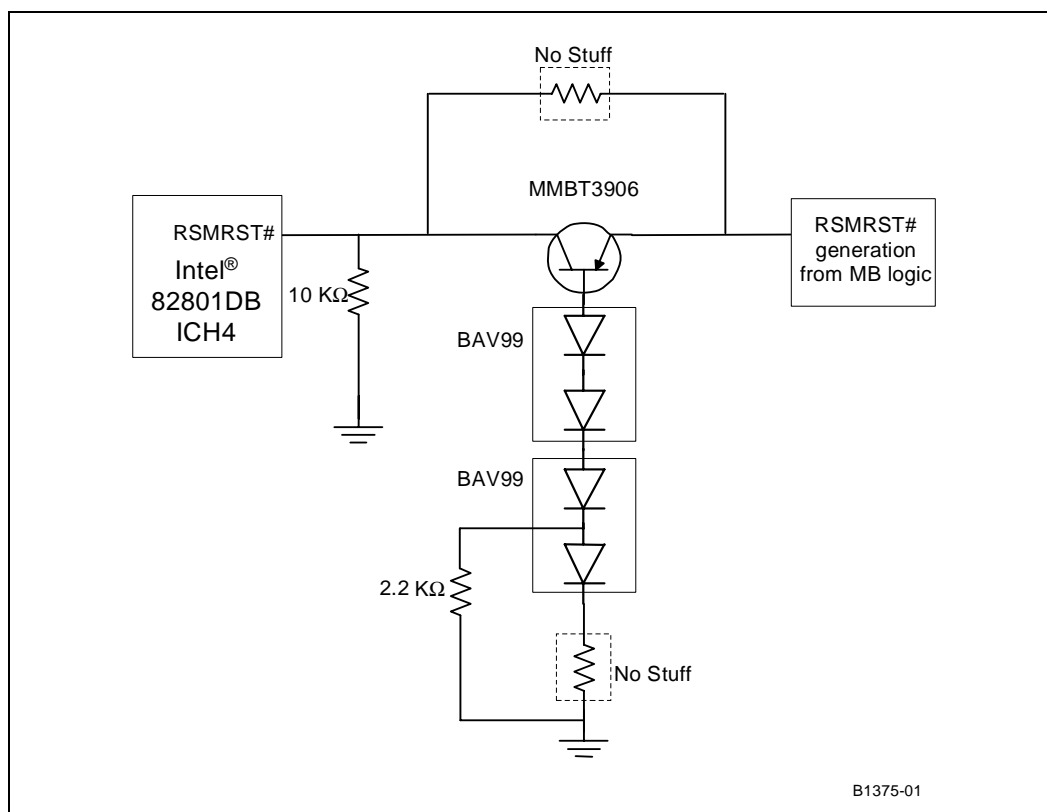
Figure 119. SYS_RESET# and PWRBTN# Connection



11.2.1 Power Well Isolation Control Strap Requirements

The circuit shown in Figure 120 may be implemented to control well isolation between the $V_{CCSUS}^{3_3}$ and RTC power wells in the event that RSMRST# is not being actively asserted during the discharge of the standby rail. Failure to implement this circuit or a circuit that functions similar to this may result in excessive droop on the V_{CCRTC} node during Sx-to-G3 power state transitions (removal of AC power and battery power). Droop on this node may potentially cause the CMOS to be cleared or corrupted, the RTC to lose time after several AC/battery power cycles, or the intruder bit might assert erroneously. Figure 120 illustrates the RTC power well isolation control.

Figure 120. RTC Power Well Isolation Control



11.3 IDE Interface

This section contains guidelines for connecting and routing the ICH4 IDE interface. The ICH4 has two independent IDE channels. The ICH4 has integrated the series resistors that have been typically required on the IDE data signals (PDD[15:0] and SDD[15:0]) running to the two ATA connectors. While it is not anticipated that additional series termination resistors may be required, OEMs should verify PCB signal integrity through simulation. Additional external 0 Ω resistors may be incorporated into the design to address possible noise issues on the PCB. The additional resistor layout increases flexibility by offering stuffing options at a later date.

The IDE interface may be routed with 5 mil traces on 7 mil spaces, and must be less than eight inches long (from ICH4 to IDE connector). Additionally, the maximum length difference between the shortest data signal and the longest strobe signal of a channel is 0.5 inch.

11.3.1 Cabling

- Length of cable: Each IDE cable must be equal to or less than 18 inches.
- Capacitance: Less than 35 pF.
- Placement: A maximum of six inches between drive connectors on the cable. When a single drive is placed on the cable it should be placed at the end of the cable. When a second drive is placed on the same cable, it should be placed on the next closest connector to the end of the cable (six inches away from the end of the cable).
- Grounding: Provide a direct low impedance chassis path between the PCB ground and hard disk drives.
- ICH4 Placement: The ICH4 must be placed eight inches or less from the ATA connector(s).

11.3.1.1 Cable Detection for Ultra ATA 66 and Ultra ATA100

The ICH4 IDE controller supports PIO, Multi-word (8237 style) DMA, Ultra DMA modes 0 through 5, and Native Mode IDE.

Note: There are no PCB hardware requirements for supporting Native Mode IDE. Native Mode IDE is supported through the operating system and system drivers. The ICH4 must determine the type of cable that is present to configure itself for the fastest possible transfer mode that the hardware may support.

An 80-conductor IDE cable is required for Ultra DMA modes greater than two (Ultra ATA/33). This cable uses the same 40 pin connector as the old 40 pin IDE cable. The wires in the cable alternate: ground, signal, ground, signal, ground, signal, ground, and so on. All the ground wires are tied together on the cable (and they are tied to the ground on the PCB through the ground pins in the 40 pin connector). This cable conforms to the Small Form Factor Specification SFF-8049. This specification may be obtained from the Small Form Factor Committee.

To determine if Ultra DMA modes greater than two (Ultra ATA/33) may be enabled, the ICH4 requires the system software to attempt to determine the cable type used in the system. When the system software detects an 80 conductor cable, it may use any Ultra DMA mode up to the highest transfer mode supported by both the chipset and the IDE device. When a 40 conductor cable is detected, the system software must not enable modes faster than Ultra DMA Mode 2 (Ultra ATA/33).

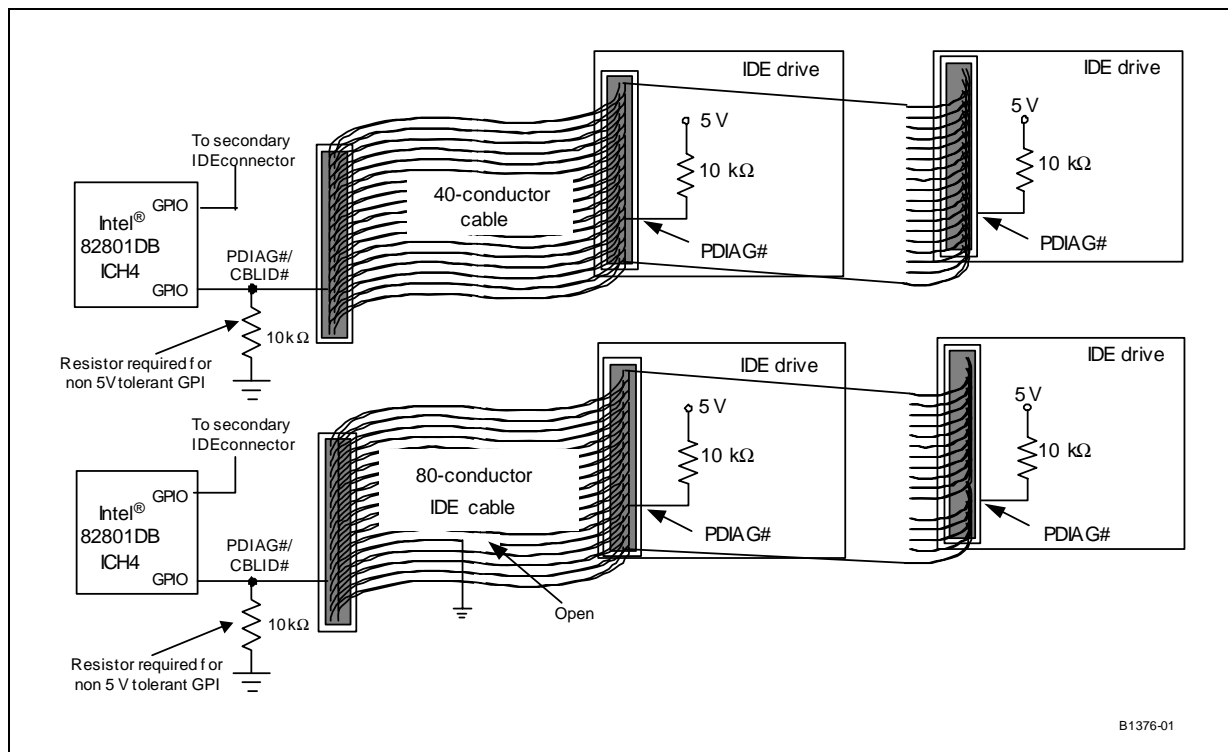
Intel recommends that cable detection be done using a combination host-side/device-side detection mechanism.

Note: Host-Side detection cannot be implemented on an NLX form factor system because this configuration does not define interconnect pins for the PDIAG#/CBLID# from the riser (containing the ATA connectors) to the PCB. These systems must rely on the device-side detection mechanism only.

11.3.1.2 Combination Host-Side/Device-Side Cable Detection

Host-side detection (described in the *ATA/ATAPI-6 Standard*) requires the use of two GPIO pins (one for each IDE channel). [Figure 121](#) illustrates the proper way to connect the PDIAG#/CBLID# signal of the IDE connector to the host. All IDE devices have a 10 kΩ pull-up resistor to 5 V on this signal. A 10 kΩ pull-down resistor on PDIAG#/CBLID# is required to prevent the GPIO from floating if a device is not present, and allows for use of a non-5 V tolerant GPIO.

Figure 121. Combination Host-Side/Device-Side IDE Cable Detection



This mechanism allows the BIOS, after diagnostics, to sample PDIAG#/CBLID#. When the signal is high, there is 40 conductor cable in the system and Ultra DMA modes greater than two must not be enabled.

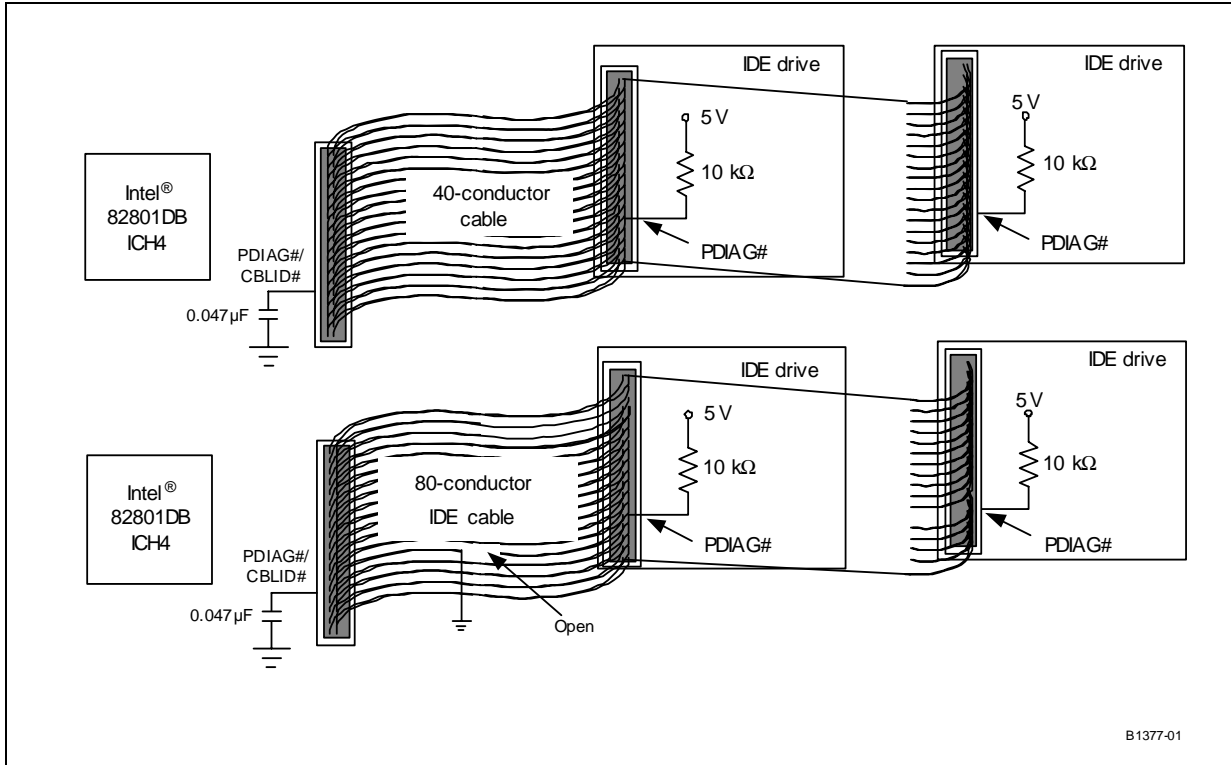
When PDIAG#/CBLID# is detected low, there may be an 80 conductor cable in the system, or there may be a 40 conductor cable and a legacy slave device (Device 1) that does not release the PDIAG#/CBLID# signal as required by the *ATA/ATAPI-6 Standard*. In this case, BIOS should check the IDENTIFY DEVICE information in a connected device that supports Ultra DMA modes higher than two. When ID Word 93, bit 13, is a '1', an 80 conductor cable is present. When this bit is '0', a legacy slave (Device 1) is preventing proper cable detection, and BIOS should configure the system as though a 40 conductor cable is present and should notify the user of the problem.

11.3.1.3 Device-Side Cable Detection

For platforms that must implement device-side detection only (e.g., NLX platforms), a $0.047\ \mu\text{F}$ capacitor is required on the PCB as shown in Figure 122. This capacitor should not be populated when implementing Intel's recommended combination host-side/device-side cable detection mechanism described above.

Note: Some drives may not support device-side cable detection.

Figure 122. Device Side IDE Cable Detection



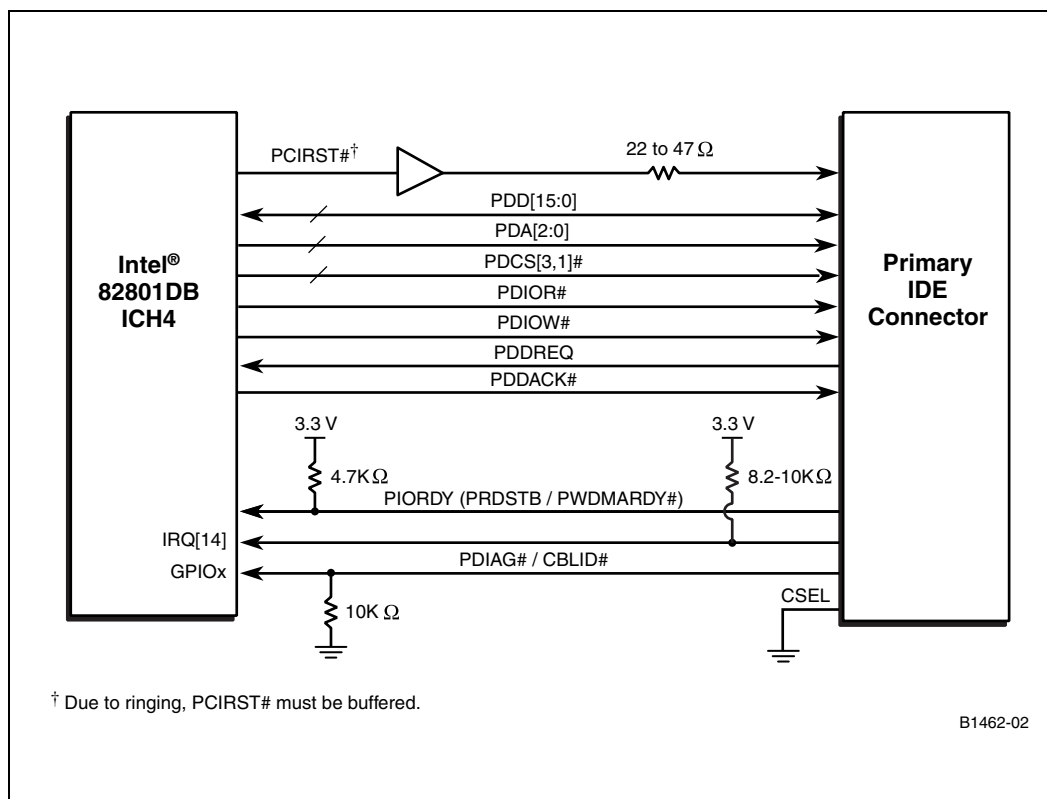
This mechanism creates a resistor-capacitor (RC) time constant. Drives supporting Ultra DMA modes greater than two (Ultra DMA/33) drives PDIAG#/CBLID# low, then releases it (pulled up through a $10\ \text{k}\Omega$ resistor). The drive samples the signal after releasing it. In an 80 conductor cable, PDIAG#/CBLID# is not connected through to the host; therefore the capacitor has no effect.

In a 40 conductor cable, the signal is connected to the host. Therefore the signal rises more slowly as the capacitor charges. The drive may detect the difference in rise times, and reports the cable type to the BIOS when it sends the IDENTIFY_DEVICE packet during system boot as described in the ATA/ATAPI-6 Standard.

11.3.2 Primary IDE Connector Requirements

Figure 123 illustrates connections requirements for the Primary IDE connector.

Figure 123. Connection Requirements for the Primary IDE Connector



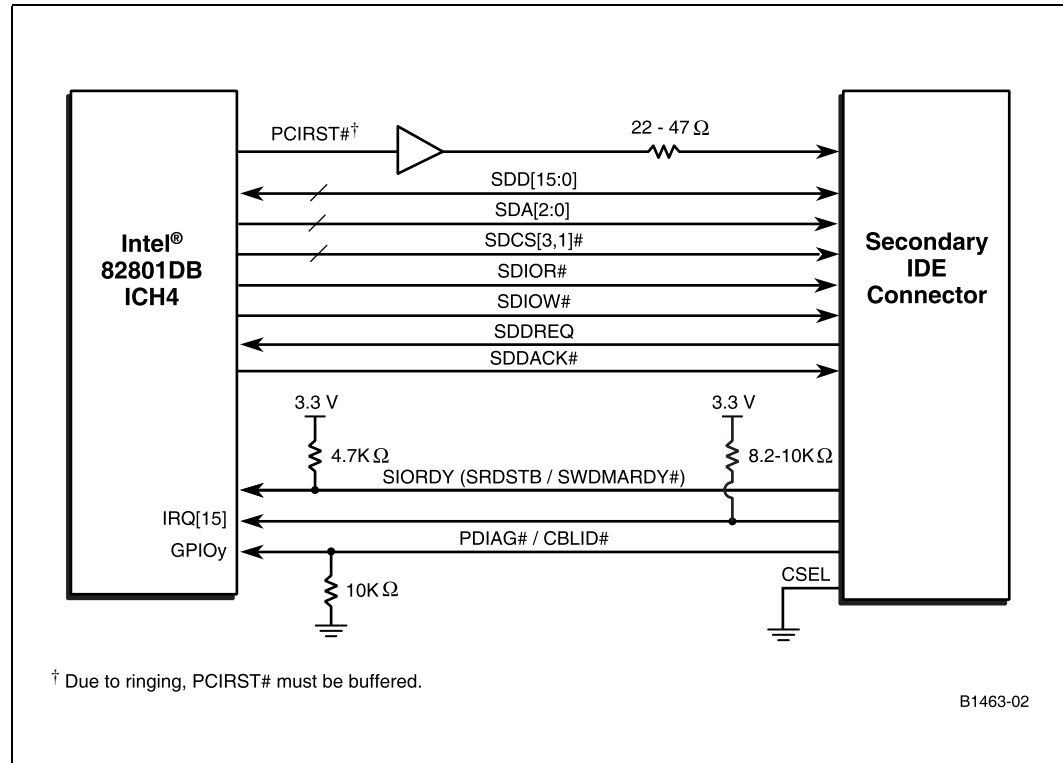
Follow these requirements for the Primary IDE connector.

- 22 Ω - 47 Ω series resistors are required on RESET#. The correct value should be determined for each unique PCB design, based on signal quality.
- An 8.2 KΩ - 10 KΩ pull-up resistor is required on IRQ14 to V_{CC3_3}.
- A 4.7 KΩ, pull-up resistor to V_{CC3_3} is required on PIORDY.
- Series resistors may be placed on the control and data line to improve signal quality. The resistors are placed as close to the connector as possible. Values are determined for each unique PCB design.
- The 10 KΩ resistor to ground on the PDIAG#/CBLID# signal is required on the primary connector. This change is to prevent the GPI pin from floating if a device is not present on the IDE interface.

11.3.3 Secondary IDE Connector Requirements

Figure 124 illustrates connection requirements for the Secondary IDE connector.

Figure 124. Connection Requirements for Secondary IDE Connector



Follow these requirements for the Secondary IDE connector.

- 22 Ω - 47 Ω series resistors are required on RESET#. The correct value should be determined for each unique PCB design, based on signal quality.
- An 8.2 K Ω - 10 K Ω pull-up resistor is required on IRQ15 to V_{CC3_3}.
- A 4.7 K Ω , pull-up resistor to V_{CC3_3} is required on SIORDY.
- Series resistors may be placed on the control and data line to improve signal quality. The resistors are placed as close to the connector as possible. Values are determined for each unique PCB design.
- The 10 K Ω resistor to ground on the PDIAG#/CBLID# signal is required on the secondary connector. This change is to prevent the GPI pin from floating if a device is not present on the IDE interface.

11.4 PCI

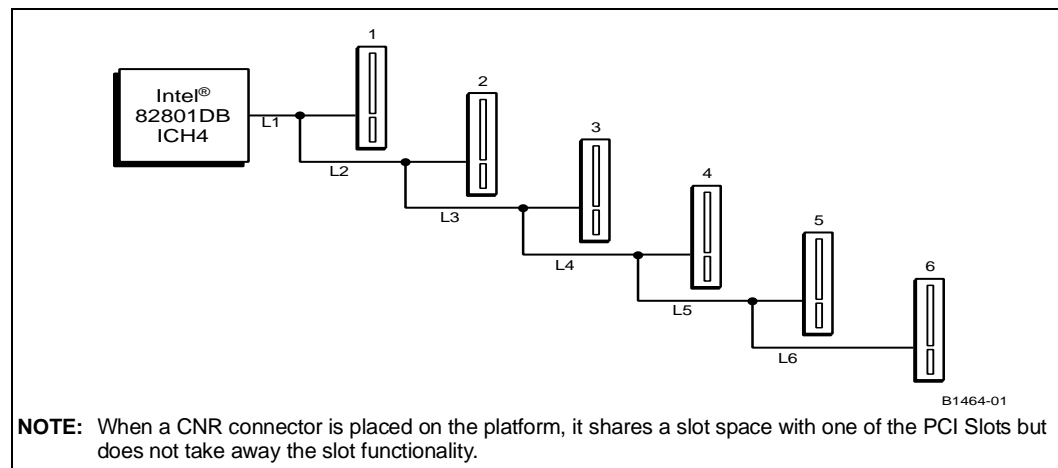
The ICH4 provides a PCI Bus interface that is compliant with the *PCI Local Bus Specification*, Revision 2.2. The implementation is optimized for high performance data streaming when the ICH4 is acting as either the target or the initiator in the PCI bus.

The ICH4 supports six PCI Bus masters (excluding the ICH4), by providing six REQ#/GNT# pairs. In addition, the ICH4 supports two PC/PCI REQ#/GNT# pairs, one of which is multiplexed with a PCI REQ#/GNT# pair.

11.4.1 PCI Routing Summary

The following represents a summary of the routing guidelines for the PCI slots, [Figure 125](#) illustrates the PCI bus layout example. Simulations assume that PCI cards follow the PCI Revision 2.2 specification trace length guidelines.

Figure 125. PCI Bus Layout Example



[Figure 126](#) illustrates the PCI bus layout with IDSEL.

Figure 126. PCI Bus Layout with IDSEL

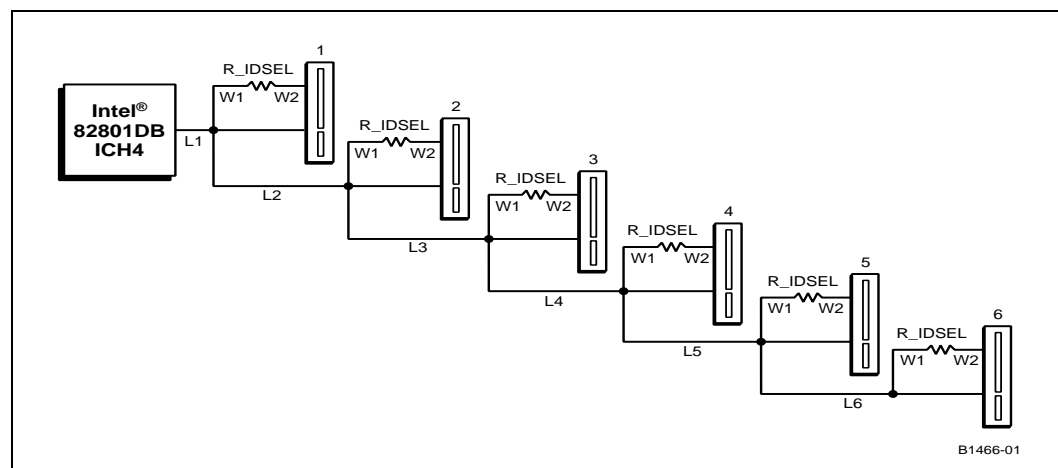


Table 93 presents the PCI data signals routing summary.

Table 93. PCI Data Signals Routing Summary

PCI Routing Req.	Trace Impedance	Topology	Maximum Trace Length (Inches)					
			L1	L2	L3	L4	L5	L6
5 on 7	47 Ω to 69 Ω 60 Ω target	Two Slots W1=W2= 0.5 inch, R_IDSEL = 300 to 900 Ω	5 to 10	1.5	N/A	N/A	N/A	N/A
		Two Slots with one down device W1=W2= 0.5 inch, R_IDSEL = 300 to 900 Ω	5 to 10	1	3	N/A	N/A	N/A
		Three Slots W1=W2= 0.5 inch, R_IDSEL = 300 to 900 Ω	5 to 10	1.5	1.5	N/A	N/A	N/A
		Three Slots with one down device W1=W2= 0.5 inch, R_IDSEL = 300 to 900 Ω	5 to 10	1	1	3	N/A	N/A
		Four Slots W1=W2= 0.5 inch, R_IDSEL = 300 to 900 Ω	5 to 10	1	1	1	N/A	N/A
		Four Slots with one down device W1=W2= 0.5 inch, R_IDSEL = 300 to 900 Ω	5 to 10	1	1	1	3	N/A
	51 Ω to 69 Ω 60 Ω target	Five Slots W1=W2= 0.5 inch, R_IDSEL = 300 to 900 Ω	5 to 8	1	1	1	1	N/A
		Six Slots W1=W2= 0.5 inch, R_IDSEL = 300 to 900 Ω	5 to 7	1	1	1	1	1

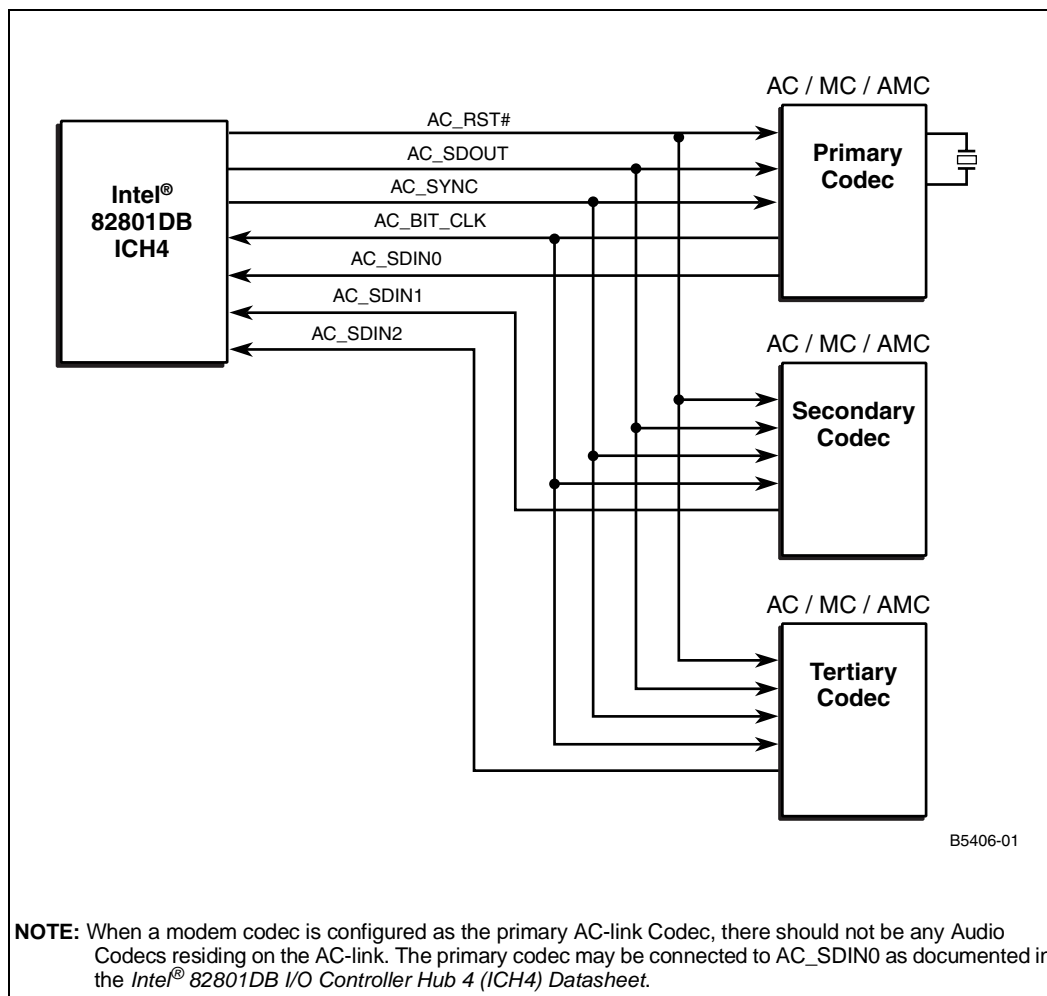
11.5 AC'97

The ICH4 implements an AC'97 2.3 compliant digital controller. Contact your codec IHV (Independent Hardware Vendor) for information on 2.3 compliant products. The AC'97 2.3 specification is on the Intel website at: <http://www.intel.com/design/chipsets/audio>

The AC-link is a bi-directional, serial PCM digital stream. It handles multiple input and output data streams, as well as control register accesses, employing a time division multiplexed (TDM) scheme. The AC-link architecture provides for data transfer through individual frames transmitted in a serial fashion. Each frame is divided into 12 outgoing and 12 incoming data streams, or slots. The architecture of the ICH4 AC-link allows a maximum of three codecs to be connected.

Figure 127 illustrates a three-codec topology of the AC-link for the ICH4.

Figure 127. Intel® 82801DB I/O Controller Hub 4 (ICH4) AC'97 – Codec Connection



Clocking is provided from the primary codec on the link via AC_BIT_CLK, and is derived from a 24.576 MHz crystal or oscillator. Refer to the primary codec vendor for crystal or oscillator requirements. AC_BIT_CLK is a 12.288 MHz clock driven by the primary codec to the digital controller (ICH4) and to any other codec present. That clock is used as the time base for latching and driving data. **Clocking AC_BIT_CLK directly off the CK-408 clock chip's 14.31818 MHz output is not supported.**

The ICH4 supports wake-on-ring from S1-S5 via the AC'97 link. The codec asserts AC_SDIN to wake the system. To provide wake capability and/or caller ID, standby power must be provided to the modem codec.

The ICH4 has weak pull-down/pull-ups that are always enabled. This keeps the link from floating when the AC-link is off or there are no codecs present.

When the shut-off bit is not set, it implies that there is a codec on the link. Therefore, AC_BIT_CLK and AC_SDOUT are driven by the codec and the ICH4 respectively. However, AC_SDIN0, AC_SDIN1, and AC_SDIN2 may not be driven. When the link is enabled, the assumption may be made that there is at least one codec.

Figure 128 illustrates the ICH4 AC'97 - AC_BIT_CLK topology.

Figure 128. Intel® 82801DB I/O Controller Hub 4 (ICH4) AC'97 – AC_BIT_CLK Topology

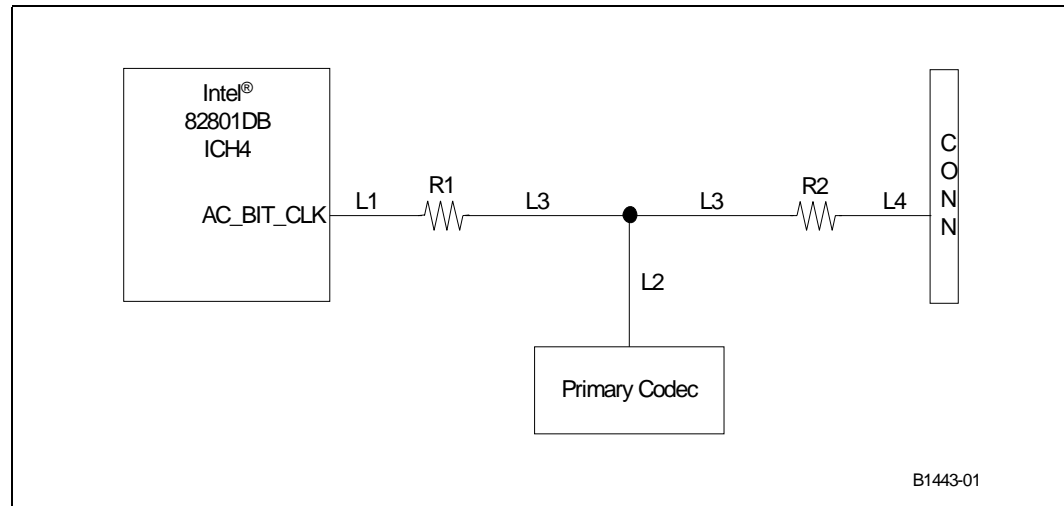


Table 94 presents the AC'97 AC_BIT_CLK routing summary.

Table 94. AC'97 AC_BIT_CLK Routing Summary

AC'97 Routing Requirements	Maximum Trace Length (inches)	Series Termination Resistance	AC_BIT_CLK Signal Length Matching
5 on 5	L1 = (1 to 8) – L3 L2 = 0.1 to 6 L3 = 0.1 to 0.4 L4 = (1 to 6) – L3	R1 = 33 Ω - 47 Ω R2 = Option 0 Ω resistor for debugging purposes	N/A

NOTES:

1. Simulations were performed using Analog Device's* Codec (AD1885) and the Cirrus Logic's* Codec (CS4205b). Results showed that if the AD1885 codec was used a 33 Ω resistor was best for R1 and if the CS4205b codec was used a 47 Ω resistor for R1 was best.
2. Bench data indicates that a 47 Ω resistor for R1 is best for the Sigmatel* 9750 codec.

Figure 129 illustrates the ICH4 AC’97 – AC_SDOUT/ AC_SYNC topology.

Figure 129. Intel® 82801DB I/O Controller Hub 4 (ICH4) AC’97 – AC_SDOUT/AC_SYNC Topology

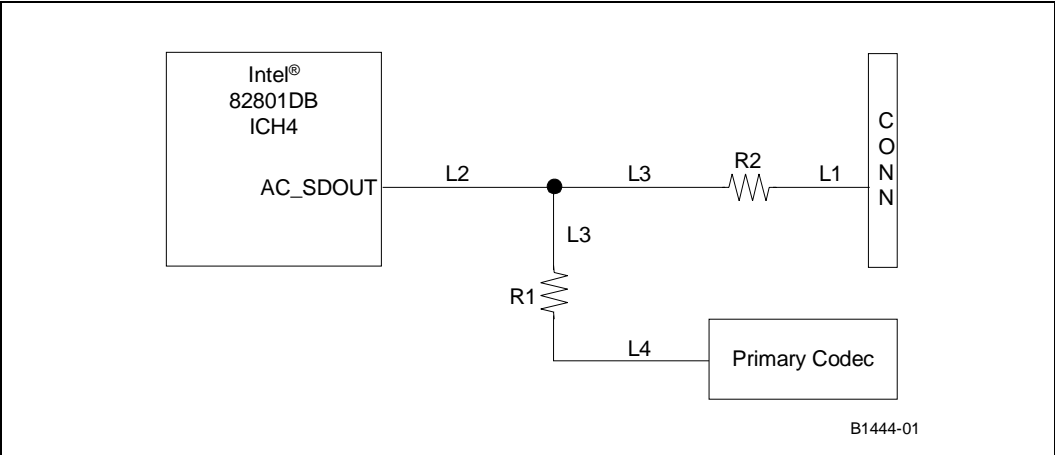


Table 95 presents the AC’97 AC_SDOUT/AC_SYNC routing summary.

Table 95. AC’97 AC_SDOUT/AC_SYNC Routing Summary

AC’97 Routing Requirements	Maximum Trace Length (inches)	Series Termination Resistance	AC_SDOUT/AC_SYNC Signal Length Matching
5 on 5	L1 = (1 to 6) – L3 L2 = 1 to 8 L3 = 0.1 to 0.4 L4 = (0.1 to 6) – L3	R1 = 33 Ω - 47 Ω R2 = R1 if the connector card that is going to be used with the platform does not have a series termination on the card. Otherwise R2 = 0 Ω.	N/A

- NOTES:**
1. Simulations were performed using Analog Device’s Codec (AD1885) and the Cirrus Logic’s Codec (CS4205b). Results showed that if the AD1885 codec was used a 33 Ω resistor was best for R1 and if the CS4205b codec was used a 47 Ω resistor for R1 was best.
 2. Bench data shows that a 47 Ω resistor for R1 is best for the Sigmatel* 9750 codec.

Figure 130 illustrates the ICH4 AC'97 – AC_SDIN topology.

Figure 130. Intel® 82801DB I/O Controller Hub 4 (ICH4) AC'97 – AC_SDIN Topology

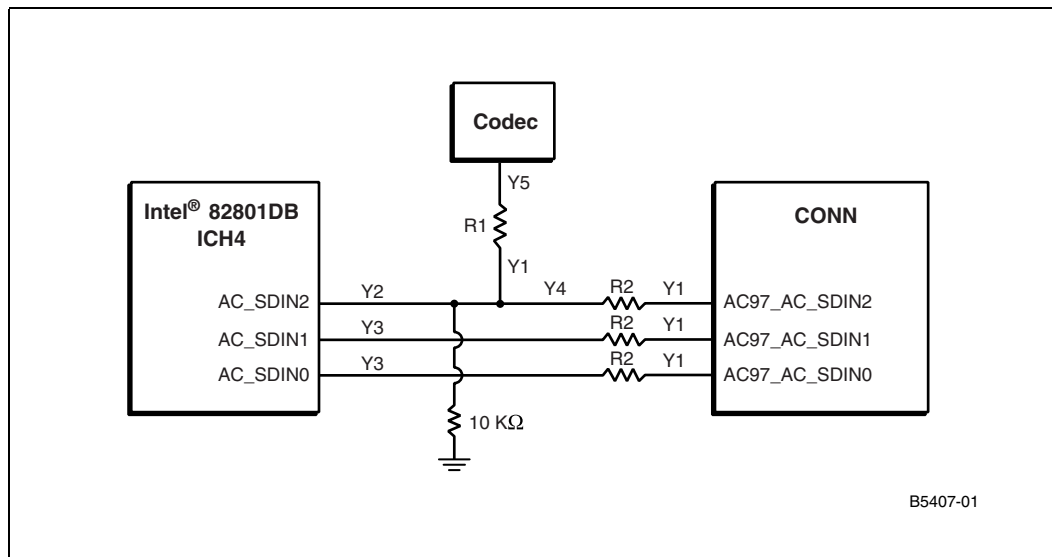


Table 96 presents the AC'97 AC_SDIN routing summary.

Table 96. AC'97 AC_SDIN Routing Summary

AC'97 Routing Requirements	Maximum Trace Length (inches)	Series Termination Resistance	AC_SDIN Signal Length Matching
5 on 5	$Y1 = 0.1 \text{ to } 0.4$ $Y2 = (1 \text{ to } 8) - Y1$ $Y3 = (1 \text{ to } 14) - Y1$ $Y4 = (1 \text{ to } 6) - Y1$ $Y5 = (0.1 \text{ to } 6) - Y1$	$R1 = 33 \Omega - 47 \Omega$ $R2 = R1$ if the connector card that is going to be used with the platform does not have a series termination on the card. Otherwise $R2 = 0 \Omega$	N/A

NOTES:

1. Simulations were performed using Analog Device's Codec (AD1885) and the Cirrus Logic's Codec (CS4205b). Results showed that if the AD1885 codec was used a 33Ω resistor was best for R1 and if the CS4205b codec was used a 47Ω resistor for R1 was best.
2. Bench data shows that a 47Ω resistor for R1 is best for the Sigmatel 9750 codec.

11.5.1 AC'97 Routing

To ensure the maximum performance of the codec, proper component placement and routing techniques are required. These techniques include properly isolating the codec, associated audio circuitry, analog power supplies, and analog ground planes from the rest of the PCB. This includes plane splits and proper routing of signals not associated with the audio section. Contact your vendor for device-specific recommendations.

The basic recommendations are as follows:

- Special consideration must be given for the ground return paths for the analog signals.
- Digital signals routed in the vicinity of the analog audio signals must not cross the power plane split lines. Analog and digital signals should be located as far as possible from each other.
- Partition the board with all analog components grouped together in one area and all digital components in another.
- Separate analog and digital ground planes should be provided, with the digital components over the digital ground plane, and the analog components, including the analog power regulators, over the analog ground plane. The split between planes must be a minimum of 0.05 inch wide.
- Keep digital signal traces, especially the clock, as far as possible from the analog input and voltage reference pins.
- Do not completely isolate the analog/audio ground plane from the rest of the board ground plane. There should be a single point (0.25 inch to 0.5 inch wide) where the analog/isolated ground plane connects to the main ground plane. The split between planes must be a minimum of 0.05 inch wide.
- Any signals entering or leaving the analog area must cross the ground split in the area where the analog ground is attached to the main PCB ground. That is, no signal should cross the split/gap between the ground planes, which would cause a ground loop, thereby greatly increasing EMI emissions and degrading the analog and digital signal quality.
- Analog power and signal traces should be routed over the analog ground plane.
- Digital power and signal traces should be routed over the digital ground plane.
- Bypassing and decoupling capacitors should be close to the IC pins, or positioned for the shortest connections to pins, with wide traces to reduce impedance.
- All resistors in the signal path or on the voltage reference should be metal film. Carbon resistors may be used for DC voltages and the power supply path, where the voltage coefficient, temperature coefficient, and noise are not factors.
- Regions between analog signal traces should be filled with copper and electrically attached to the analog ground plane. Regions between digital signal traces should be filled with copper and electrically attached to the digital ground plane.
- Locate the crystal or oscillator close to the codec.

11.5.2 PCB Implementation

The following design considerations are provided for the implementation of an ICH4 platform using AC'97. These design guidelines have been developed to ensure maximum flexibility for board designers, while reducing the risk of board-related issues. These recommendations are not the only implementation or a complete checklist, but they are based on the ICH4 platform.

- Active components such as FET switches, buffers or logic states should not be implemented on the AC-link signals, except for AC_RST#. Doing so would potentially interfere with timing margins and signal integrity.
- The ICH4 supports wake-on-ring from S1-S5 states via the AC'97 link. The codec asserts AC_SDIN to wake the system. To provide wake capability and/or caller ID, standby power must be provided to the modem codec. When no codec is attached to the link, internal pull-downs prevent the inputs from floating, so external resistors are not required.
- PC_BEEP should be routed through the audio codec. Care should be taken to avoid the introduction of a pop when powering the mixer up or down.

11.5.2.1 Valid Codec Configurations

Table 97 presents supported codec configurations.

Table 97. Supported Codec Configurations

Option	Primary Codec	Secondary Codec	Tertiary Codec	Notes
1	Audio	Audio	Audio	1
2	Audio	Audio	Modem	1
3	Audio	Audio	Audio/Modem	1
4	Audio	Modem	Audio	1
5	Audio	Audio/Modem	Audio	1
6	Audio/Modem	Audio	Audio	1

NOTES:

1. For power management reasons, codec power management registers are in audio space. As a result, if there is an audio codec in the system it must be primary.
2. There cannot be two modems in a system because there is only one set of modem DMA channels.
3. The ICH4 supports a modem codec on any of the AC-SDIN lines. However the modem codec ID must be either 00 or 01.

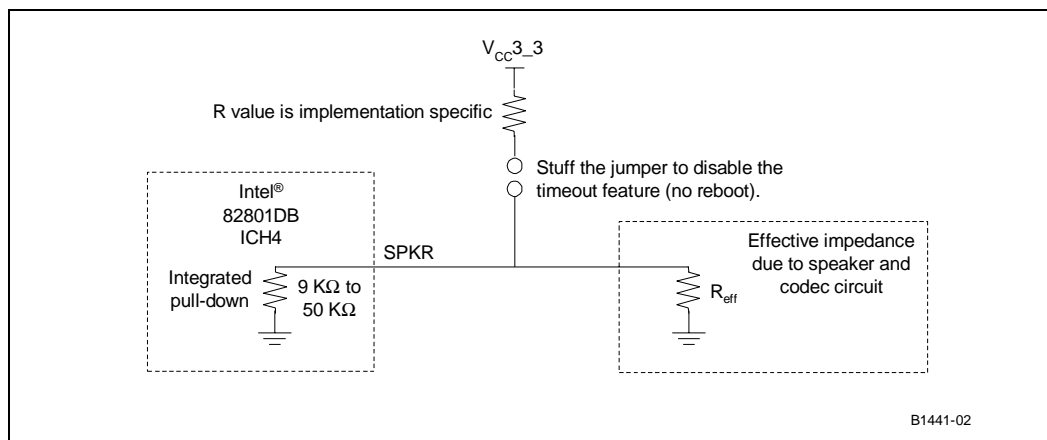
11.5.3 SPKR Pin Configuration

SPKR is used as both the output signal to the system speaker and as a functional strap. The strap function enables or disables the TCO Timer Reboot function based on the state of the SPKR pin on the rising edge of PWROK. When enabled, the ICH4 sends an SMI# to the processor upon a TCO timer timeout. The status of this strap is readable via the NO_REBOOT bit (bit 1, D31: F0, Offset D4h). The SPKR signal has a weak integrated pull-down resistor (the resistor is only enabled during boot/reset). Its default state is a logical zero or set to reboot. To disable the feature, a jumper may be populated to pull the signal line high (see [Figure 131](#)).

The value of the pull-up must be such that the voltage divider output caused by the pull-up, the effective pull-down (R_{eff}), and the ICH4's integrated pull-down resistor are read as logic high ($0.5 * V_{CC3_3}$ to $V_{CC3_3} + 0.5$ V).

Figure 131 illustrates an example of the speaker circuit.

Figure 131. Example Speaker Circuit



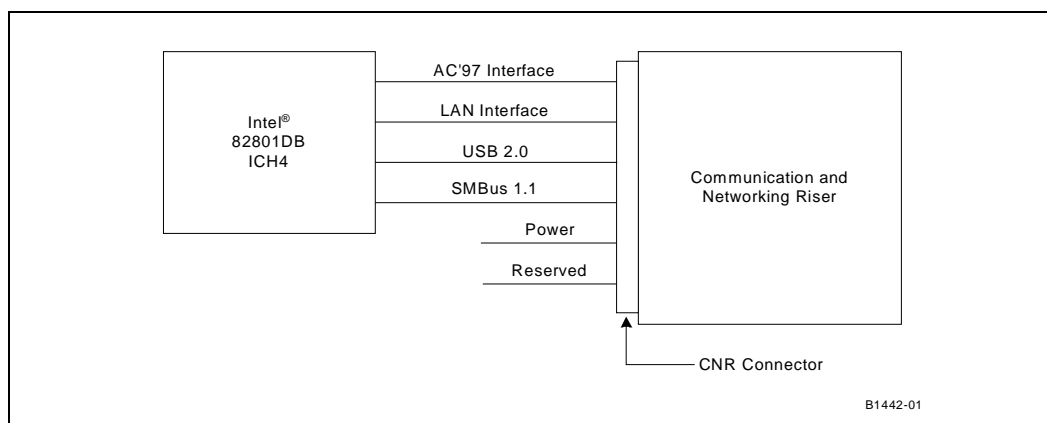
11.6 CNR

Refer to the related documents, *Communication and Network Riser Specification*, Revision 1.2.

The Communication and Networking Riser (CNR) specification defines a hardware scalable Original Equipment Manufacturer (OEM) PCB riser and interface. This interface supports multi-channel audio, V.90 analog modem, phone-line based networking, 10/100 Ethernet-based networking, SMBus Interface Power Management Rev 1.1, and USB 2.0. The CNR specification defines the interface, which should be configured prior to shipment of the system. Standard I/O expansion slots, such as those supported by the PCI bus architecture, are intended to continue serving as the upgrade medium. The CNR mechanically shares a PCI slot, therefore the system designer may not sacrifice a PCI slot if he decides not to include a CNR in a particular build.

Figure 132 illustrates the interface for the CNR connector. Refer to the appropriate section of this document for the corresponding design and layout guidelines. The Platform LAN Connection (PLC) may be either an Intel® 82562ET, or an Intel® 82562EM device. Refer to the CNR specification for additional information.

Figure 132. CNR Interface



11.6.1 AC'97 Audio Codec Detect Circuit and Configuration Options

Table 98 presents signal descriptions of general circuits to implement a number of different codec configurations.

Refer to the *Communication and Network Riser Specification*, Revision 1.2, for Intel's recommended codec configurations.

Table 98. Signal Descriptions

Signal	Description
CDC_DN_ENAB#	When low, indicates that the codec on the PCB is enabled and primary on the AC'97 Interface. When high, indicates that the PCB codec(s) must be removed from the AC'97 Interface (held in reset), because the CNR codec(s) is going to be the primary device(s) on the AC'97 Interface.
AC_RST#	Reset signal from the AC'97 Digital Controller (ICH4).
AC_SDINn	AC'97 serial data from an AC'97-compliant codec to an AC'97-compliant controller (i.e., the ICH4).

11.6.2 CNR 1.2 AC'97 Disable and Demotion Rules for the PCB

The following are the CNR1.1/1.2 AC'97 Disable and Demotion Rules for the PCB:

1. All AC'97 Rev. 2.2.non-chaining codecs on the PCB must always disable themselves when the CDC_DN_ENAB# signal is in a high state.
2. A PCB AC'97 Codec must never change its address or AC_SDIN line used, regardless of the state of the CDC_DN_ENAB# signal.
3. On a PCB containing an AC'97 controller supporting three AC'97 Codecs, the AC'97 Revision 2.2, or AC'97 Revision 2.3 codec on the PCB, must be connected to the AC_SDIN2 signal of the CNR connector.
4. A PCB should not contain more than a single AC'97 codec.

These rules allow for forward and backward compatibility between CNR Version 1.1/1.2 cards.

For more information on chaining, consult the *Communication and Network Riser Specification*, Revision 1.2.

Figure 133 illustrates PCB AC'97 CNR implementation with a single codec down onboard.

Figure 133. PCB AC'97 CNR Implementation with a Single Codec Down Onboard

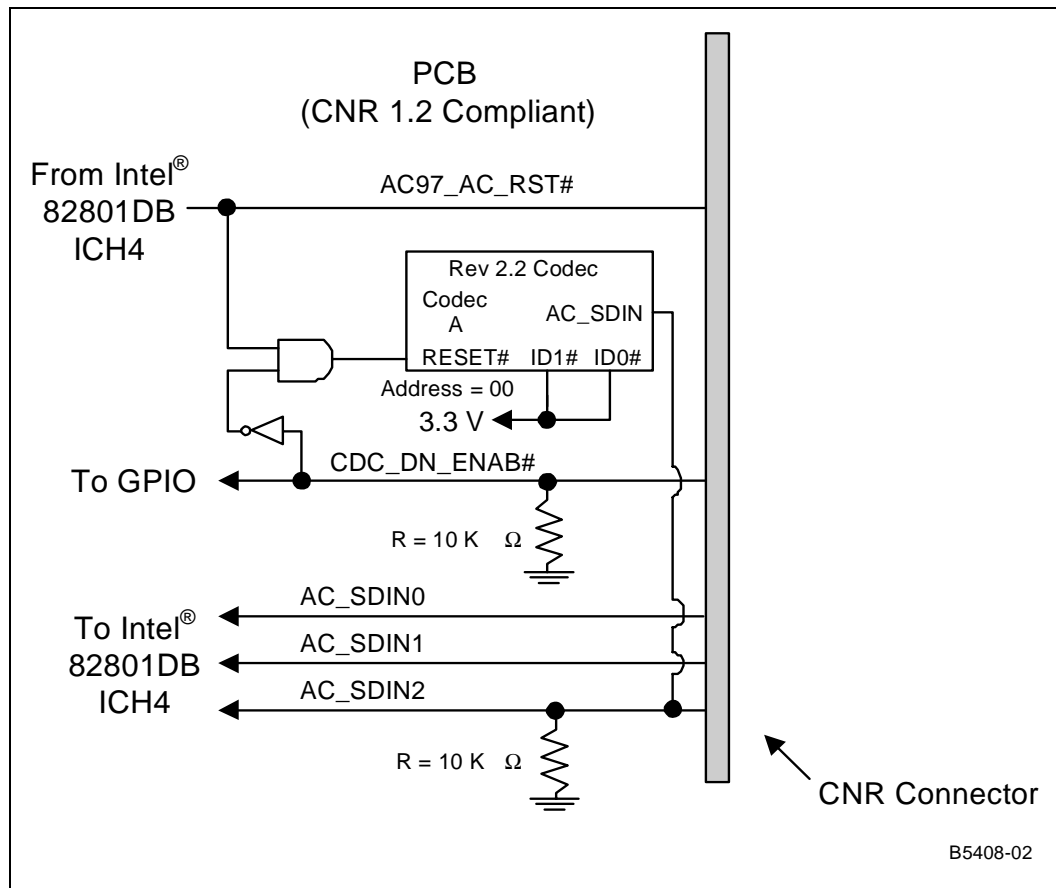
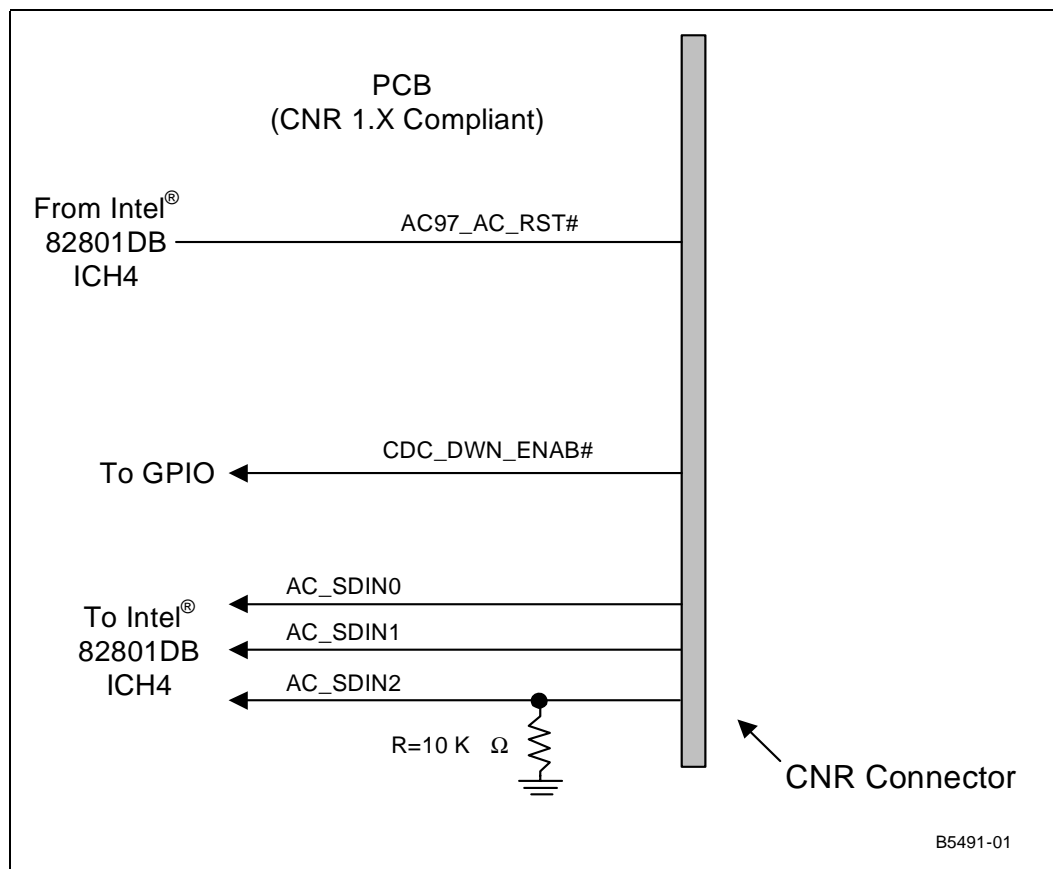


Figure 134 illustrates PCB AC'97 CNR implementation with no codec down onboard.

Figure 134. PCB AC'97 CNR Implementation with No Codec Down Onboard



11.6.3 CNR Routing Summary

Table 99 presents a summary of the various interface routing requirements of the CNR Riser.

Table 99. CNR Routing Summary

CNR Routing Requirements	Maximum Trace Length	Signal Length Matching	Signal Referencing
USB (4 on 4.5) Data pair must be at least 20 mils from nearest neighbor	10 inches	No more than 150 mils trace mismatch.	Ground
AC '97 (5 on 5)	AC_BIT_CLK (Refer to Table 94.) AC_SDOUT (Refer to Table 95.) AC_SDIN (Refer to Table 96.)	N/A	Ground
LAN (5 on 10)	9.5 inches (Refer to Table 108.)	Equal to or up to 500 mils shorter than the LAN_CLK trace.	Ground

11.7 USB 2.0 Guidelines and Recommendations

11.7.1 Layout Guidelines

11.7.1.1 General Routing and Placement

Use the following general routing and placement guidelines when laying out a new design. These guidelines help minimize signal quality and EMI problems. The USB 2.0 validation efforts focused on a four-layer PCB where the first layer is a signal layer, the second plane is power, the third plane is ground and the fourth is a signal layer. This results in the placement of most of the routing on the fourth plane (closest to the ground plane), allowing a higher component density on the first plane.

1. Place the ICH4 and major components on the un-routed board first. With minimum trace lengths, route high-speed clock, periodic signals, and USB 2.0 differential pairs first. Maintain maximum possible distance between high-speed clocks/periodic signals to USB 2.0 differential pairs and any connector leaving the PCB (i.e., I/O connectors, control and signal headers, or power connectors).
2. USB 2.0 signals should be **ground referenced**.
3. Route USB 2.0 signals using a minimum of vias and corners. This reduces reflections and impedance changes.
4. When it becomes necessary to turn 90°, use two 45° turns or an arc instead of making a single 90° turn. This reduces reflections on the signal by minimizing impedance discontinuities.
5. Do not route USB 2.0 traces under crystals, oscillators, clock synthesizers, magnetic devices or ICs that use and/or duplicate clocks.
6. Stubs on high-speed USB signals should be avoided, as stubs cause signal reflections and affect signal quality. When a stub is unavoidable in the design, the sum of all stubs for a particular signal line should not exceed 200 mils.

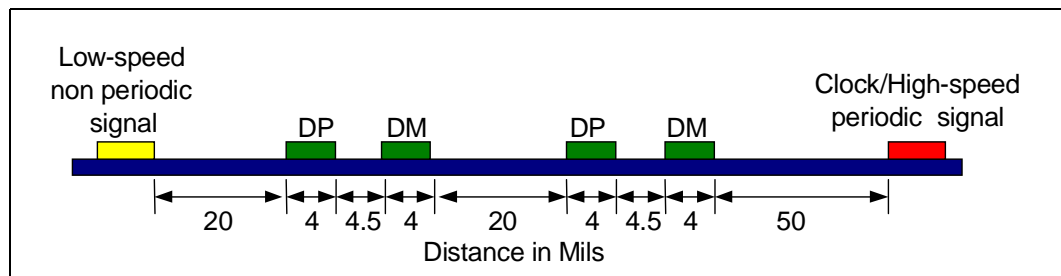
7. Route all traces over continuous planes (V_{CC} or GND), with no interruptions. Avoid crossing over anti-etch if at all possible. Crossing over anti-etch (plane splits) increases inductance and radiation levels by forcing a greater loop area. Likewise, avoid changing layers with USB 2.0 traces as much as practical. It is preferable to change layers to avoid crossing a plane split. Refer to [Section 11.7.2](#) for more information.
8. Separate signal traces into similar categories and route similar signal traces together (such as routing differential pairs together).
9. Keep USB 2.0 USB signals clear of the core logic set. High current transients are produced during internal state transitions and may be very difficult to filter out.
10. Follow the 20*h thumb rule by keeping traces at least 20*(height above the plane) away from the edge of the plane (V_{CC} or GND, depending on the plane the trace is over). For the suggested stack-up the height above the plane is 4.5 mils. This calculates to a 90-mil spacing requirement from the edge of the plane. This helps prevent the coupling of the signal onto adjacent wires and also helps prevent free radiation of the signal from the edge of the PCB.

11.7.1.2 USB 2.0 Trace Separation

Use the following separation guidelines. [Figure 135](#) illustrates Intel's recommended USB trace spacing.

1. Maintain parallelism between USB differential signals with the trace spacing needed to achieve 90 Ω differential impedance. Deviations normally occur due to package breakout and routing to connector pins. Just ensure the amount and length of the deviations are kept to the least possible.
2. Use an impedance calculator to determine the trace width and spacing required for the specific board stack-up being used. 4 mil traces with 4.5 mil spacing results in approximately 90 Ω differential trace impedance.
3. Minimize the length of high-speed clock and periodic signal traces that run parallel to high-speed USB signal lines, to minimize crosstalk. Based on EMI testing experience, the minimum suggested spacing to clock signals is 50 mils.
4. Based on simulation data, use 20 mil minimum spacing between high-speed USB signal pairs and other signal traces for optimal signal quality. This helps to prevent crosstalk.

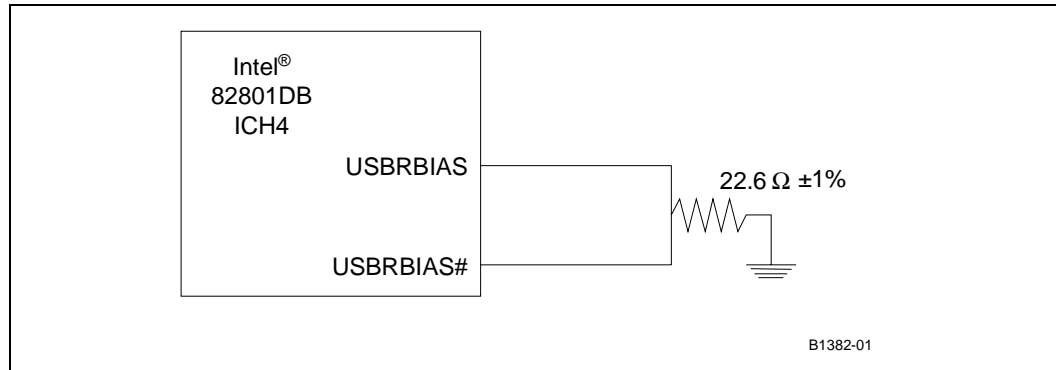
Figure 135. Recommended USB Trace Spacing



11.7.1.3 USBRBIAS Connection

The USBRBIAS pin and the USBRBIAS# pin may be shorted and routed 5 on 5 to one end of a $22.6\ \Omega \pm 1\%$ resistor to ground. Place the resistor within 500 mils of the ICH4 and avoid routing next to clock pins. [Figure 136](#) illustrates a USBRBIAS connection.

Figure 136. USBRBIAS Connection



[Table 100](#) presents the USBRBIAS/USBRBIAS# routing summary.

Table 100. USBRBIAS/USBRBIAS# Routing Summary

USBBIAS/USBBIAS# Routing Requirements	Maximum Trace Length	Signal Length Matching	Signal Referencing
5 on 5	500 mils	N/A	N/A

11.7.1.4 USB 2.0 Termination

A common-mode choke should be used to terminate the USB 2.0 bus. Place the common-mode choke as close as possible to the connector pins. Refer to [Section 11.7.4](#) for details.

11.7.1.5 USB 2.0 Trace Length Pair Matching

USB 2.0 signal pair traces should be trace length matched. Maximum trace length mismatch between USB 2.0 signal pair should be no greater than 150 mils.

11.7.1.6 USB 2.0 Trace Length Guidelines

Table 101 presents the USB 2.0 trace length preliminary guidelines, with common-mode choke.

Table 101. USB 2.0 Trace Length Preliminary Guidelines with Common-Mode Choke)

Topology	USB 2.0 Routing Requirements/ Trace Impedance	Signal Referencing	Signal Matching	Cable Length	PCB Trace Length	Card Trace Length	Maximum Total Length
Back Panel	4 on 4.5/90 Ω differential	Ground	The max mismatch between data pairs should not be greater than 150 mils	N/A	17 inches	N/A	17 inches
CNR	4 on 4.5/90 Ω differential	Ground		N/A	8 inches	6 inches	14 inches
Front Panel	4 on 4.5/90 Ω differential	Ground		9	6	2	17
				10.5	5	2	17.5
				12	4	2	18
				13.5	3	2	18.5
				15	2	2	19

NOTES:

- These lengths are based on simulation results and may be updated in the future.
- All lengths are based on using a common-mode choke. Refer to [Section 11.7.4](#) for details on common-mode choke.
- Numbers in this table are based on the following assumptions:
 - CNR configuration: maximum six inches trace on add-on card.
- An approximate 1:1 trade-off may be assumed from PCB trace length vs. daughtercard trace length (e.g., trade one inch of daughtercard for one inch of PCB trace lengths).
- Numbers in the table are based on the following simulation assumptions:
 - Trace length on front panel connector card assumed a maximum of two inches.
 - USB twisted pair shielded cable as specified in *USB 2.0 specification* was used.

11.7.2 Plane Splits, Voids, and Cut-Outs (Anti-Etch)

The following guidelines apply to the use of plane splits voids and cutouts.

11.7.2.1 V_{CC} Plane Splits, Voids, and Cut-Outs (Anti-Etch)

Use the following guidelines for the V_{CC} plane.

- Traces should not cross anti-etch, for it greatly increases the return path for those signal traces. This applies to USB 2.0 signals, high-speed clocks, and signal traces as well as slower signal traces that might be coupling to them. USB signaling is not purely differential in all speeds (i.e., the Full-speed Single Ended Zero is common mode).
- Avoid routing of USB 2.0 signals 25 mils of any anti-etch to avoid coupling to the next split or radiating from the edge of the PCB.

When breaking signals out from packages it is sometimes very difficult to avoid crossing plane splits or changing signal layers, particularly in today's PCB environment that uses several different voltage planes. Changing signal layers is preferable to crossing plane splits if a choice has to be made between one or the other.

When crossing a plane split is completely unavoidable, proper placement of stitching caps may minimize the adverse effects on EMI and signal quality performance caused by crossing

the split. Stitching capacitors are small-valued capacitors (1 μ F or lower in value) that bridge voltage plane splits close to where high speed signals or clocks cross the plane split. The capacitor ends should tie to each plane separated by the split. They are also used to bridge or bypass power and ground planes close to where a high-speed signal changes layers. As an example of bridging plane splits, a plane split that separates V_{CC5} and V_{CC3_3} planes should have a stitching cap placed near any high-speed signal crossing. One side of the cap should tie to V_{CC5} and the other side should tie to V_{CC3_3} . Stitching caps provide a high-frequency current return path across plane splits. They minimize the impedance discontinuity and current loop area that crossing a plane split creates.

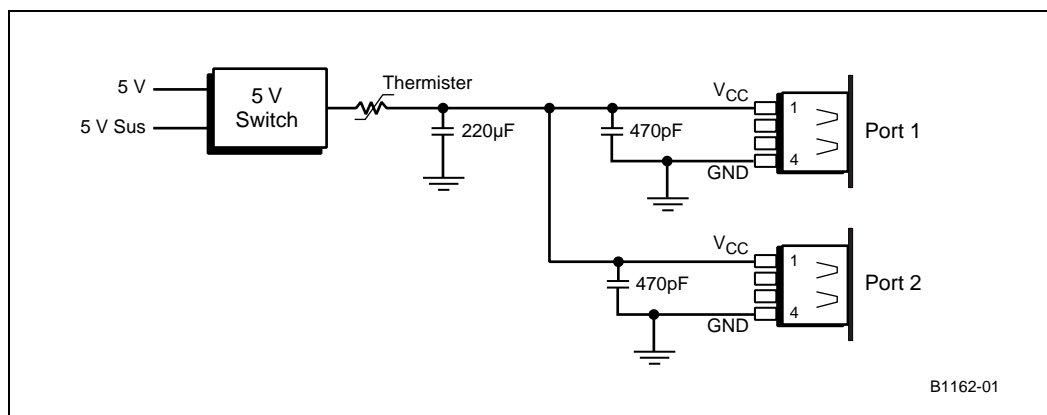
11.7.2.2 GND Plane Splits, Voids, and Cut-Outs (Anti-Etch)

Avoid anti-etch on the GND plane.

11.7.3 USB Power Line Layout Topology

This section presents a suggested topology for power distribution of Vbus to USB ports. Circuits of this type provide two types of protection during dynamic attach and detach situations on the bus: inrush current limiting (droop) and dynamic detach fly-back protection. These two different situations require both bulk capacitance (droop) and filtering capacitance (for dynamic detach fly-back voltage filtering). It is important to minimize the inductance and resistance between the coupling capacitors and the USB ports. That is, capacitors should be placed as close as possible to the port and the power carrying traces should be as wide as possible, preferably, a plane. A good rule-of-thumb is to make the power-carrying traces wide enough that the system fuse blows on an over-current event. When the system fuse is rated at 1 A, the power carrying traces should be wide enough to carry at least 1.5 A. Figure 137 illustrates a good downstream power connection.

Figure 137. Good Downstream Power Connection



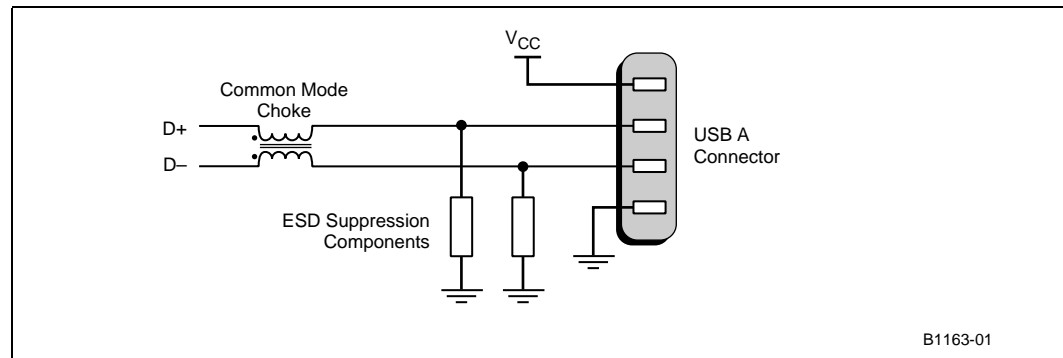
11.7.4 EMI Considerations

The following guidelines apply to the selection and placement of common-mode chokes and ESD protection devices.

11.7.4.1 Common Mode Chokes

Testing has shown that common-mode chokes may provide required noise attenuation. A design should include a common-mode choke footprint to provide a stuffing option **in the event** the choke is needed to pass EMI testing. Figure 138 illustrates the schematic of a typical common-mode choke and ESD suppression components. The choke should be placed as close as possible to the USB connector signal pins. In systems that route USB to a front panel header, the choke should be placed on the front panel card.

Figure 138. Common-Mode Choke Schematic



Common-mode chokes distort full-speed and high-speed signal quality. As the common-mode impedance increases, the distortion increases, so you need to test the effects of the common-mode choke on full speed and high-speed signal quality. Common-mode chokes with a target impedance of 80 Ω to 90 Ω at 100 MHz generally provide adequate noise attenuation.

Finding a common-mode choke that meets the designer's needs is a two-step process.

1. A part must be chosen with the impedance value that provides the required noise attenuation. This is a function of the electrical and mechanical characteristics of the part chosen and the frequency and strength of the noise present on the USB traces that you are trying to suppress.
2. After you have a part that gives passing EMI results the second step is to test the effect this part has on signal quality. Higher impedance common-mode chokes generally have a greater damaging effect on signal quality, so care must be used when increasing the impedance without doing thorough testing. Thorough testing means that the signal quality must be checked for low-speed, full-speed and high-speed USB operation.

11.7.5 ESD

Classic USB (1.0/1.1) provided ESD suppression using in-line ferrites and capacitors that formed a low pass filter. This technique does not work for USB 2.0 due to the much higher signal rate of high-speed data. A device that has been tested successfully is based on spark gap technology. Proper placement of any ESD protection device is on the data lines between the common-mode choke and the USB connector data pins as shown in Figure 138. Other types of low-capacitance ESD protection devices may work as well but were not investigated. As with the common-mode choke solution, Intel recommends including footprints for some type of ESD protection device as a stuffing option in case it is needed to pass ESD testing.

For more information refer to the *Intel ICH Family USB ESD Considerations*.

11.7.6 Front Panel Solutions

11.7.6.1 Internal USB Cables

The front panel internal cable solution chosen must meet all the requirements of Chapter 6 of the *USB 2.0 specification* for high-/full-speed cabling for each port with the exceptions described in Cable Option 2.

11.7.6.1.1 Internal Cable Option 1

Use standard high-speed/full-speed compatible USB cables. These must meet all cabling requirements called out in Chapter 6 of the *USB 2.0 specification*. Intel's recommended PCB mating connector pin-out is covered in detail later in this document.

11.7.6.1.2 Internal Cable Option 2

Use custom cables that meet all of the requirements of Chapter 6 of the *USB 2.0 specification* with the following additions/exceptions.

- They may share a common jacket, shield and drain wire.

Two ports with signal pairs that share a common jacket may combine Vbus and ground wires into a single wire provided the following conditions are met:

- The bypass capacitance required by Section 7.2.4.1 of the *USB 2.0 specification* is physically located near the power and ground pins of the USB connectors. This is easiest to achieve by mounting the front panel USB connectors and the bypass capacitance on a small PCB (daughtercard). Refer to the front panel daughtercard referenced later for details.
- Selecting proper wire size: A general rule for replacing two power or ground wires with a single wire is to choose a wire size from Table 6-6 in Section 6.6.3 of the *USB 2.0 specification* that has $\approx \frac{1}{2}$ the resistance of either of the two wires being combined. The data is provided for reference in Table 102.

Table 102. Conductor Resistance

American Wire Gauge (AWG)	$\Omega/100$ Meters Maximum
28	23.20
26	14.60
24	9.09
22	5.74
20	3.58

NOTE: This table is the same as Table 6-6 of the Universal Serial Bus 2.0 Specification.

Example 1. Two 24-gauge (AWG) power or ground wires may be replaced with one 20-gauge wire.

Proper wire gauge selection is important to meet the voltage drop and droop requirements called out in the *USB 2.0 specification* at the USB connectors as well as at the stake pins on the PCB.

Placing the capacitance near the USB connectors for cables that share power and ground conductors is required to ensure the system passes droop requirements. Cables that provide individual power and ground conductors for each port may usually meet droop requirements by providing adequate capacitance near the PCB mating connector because droop is actually an effect felt by adjacent ports due to switching transients on the aggressor port. In the separate conductor case, all transients are seen/dampened by the capacitance at the PCB mating connector before they may cause problems with the adjacent port sharing the same cable. Refer to Section 7.2.2 and 7.2.4.1 of the *USB 2.0 specification* for more details.

Note: Cables that contain more than two signal pairs are not recommended by Intel due to unpredictable impedance characteristics.

11.7.6.2 PCB Mating Connector

Proper selection of a PCB mating connector for front panel USB support is important to ensure that signal quality is not adversely affected because of poor connector interface. The cable and PCB mating connector must also pass the TDR requirements listed in the *USB 2.0 specification*.

11.7.6.2.1 Pin-Out

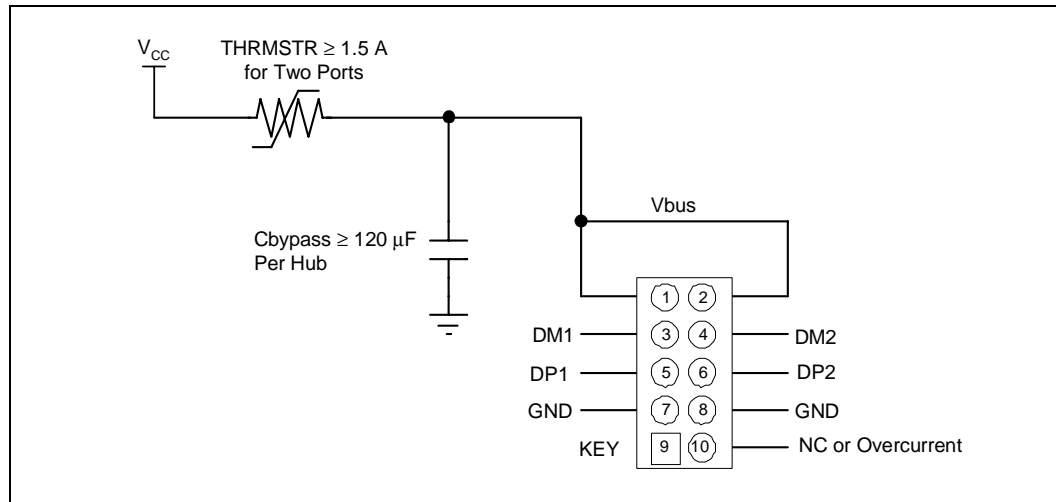
Intel recommends a 10 pin, 0.1-inch pitch stake pin assembly with the pin-out listed in [Table 103](#) and shown in [Figure 139](#).

Table 103. Front Panel Header Pin-Out

Pin	Description
1	V _{CC}
2	V _{CC}
3	dm1
4	dm2
5	dp1
6	dp2
7	Gnd
8	Gnd
9	key
10	No connect or over-current sense

Figure 139 illustrates the front panel header schematic.

Figure 139. Front Panel Header Schematic



Intel recommends that the fuse element (thermistor) for the front panel header be included on the PCB to protect the PCB from damage.

- This protects the PCB from damage in the case where an un-fused front panel cable solution is used.
- It also provides protection from damage if an un-keyed cable is inadvertently plugged onto the front panel USB connector.
- It provides protection to the PCB in the case where the front panel cable is cut or damaged during assembly or manufacturing resulting in a short between Vbus and ground.

11.7.6.2.2 Routing Considerations

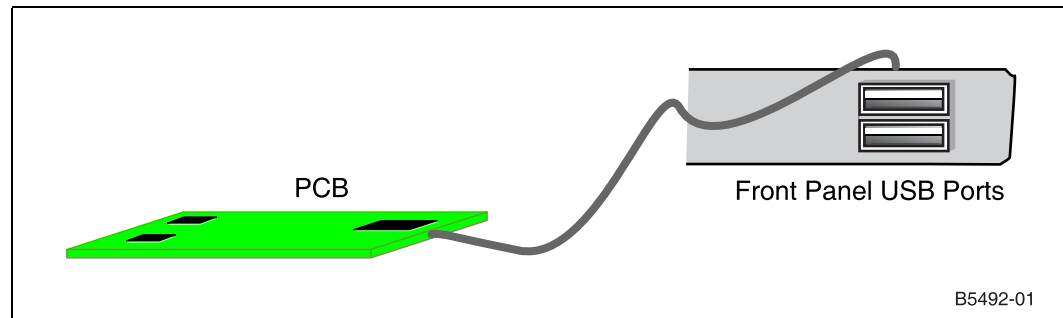
Traces or surface shapes from V_{CC} to the thermistor, to C_{bypass} and to the connector power and ground pins should be at least 50 mils wide to ensure adequate current carrying capability.

There should be double vias on power and ground nets, and the trace lengths should be kept as short as possible.

11.7.6.3 Front Panel Connector Card

The best way to provide front or side panel support for USB is to use a daughtercard and cable assembly. This allows the placement of the EMI/ESD suppression components right at the USB connector where they are the most effective. [Figure 140](#) illustrates the major components associated with a typical front/side panel USB solution that uses a front panel connector card.

Figure 140. PCB Front Panel USB Support



Note: The terms ‘connector card’ and ‘daughtercard’ are used interchangeably.

When designing the PCB with front/side panel support, the system integrator should know which type of cable assembly should be used. When the system integrator plans to use a connector card, ensure that there are not duplicate EMI/ESD/thermistor components placed on the PCB because this usually causes drop/droop and signal quality degradation or failure.

11.7.6.3.1 Front Panel daughtercard Design Guidelines

Place the Vbus bypass capacitance, common-mode choke, and ESD suppression components on the daughtercard as close as possible to the connector pins.

Follow the same layout, routing and impedance control guidelines as specified for PCBs.

Minimize the trace length on the front panel connector card. Intel recommends using a trace length less than two inches.

Use the same mating connector pin-out as outlined for the PCB in [Section 11.7.6.2.1](#). Use the same routing guidelines as described in [Section 11.7.1](#).

Trace length guidelines are presented in [Table 101](#).

11.8 I/O Advanced Programmable Interrupt Controller (IOAPIC)

The Intel® 852GM chipset platform does not support IOAPIC when C2/C3/C4 states are enabled.

11.8.1 IOAPIC Disabling Options (Recommended Implementation)

Intel recommends that IOAPIC be disabled in software while the connections to the board are as shown in Figure 141. Software may be used to turn off PICCLK from clock generator.

To disable IOAPIC in BIOS:

1. ICH4: D31:F0; Offset: D1; bit 0 (0=disable);
2. Celeron Processor: MSR 1Bh bit 11 (0 = Disable)

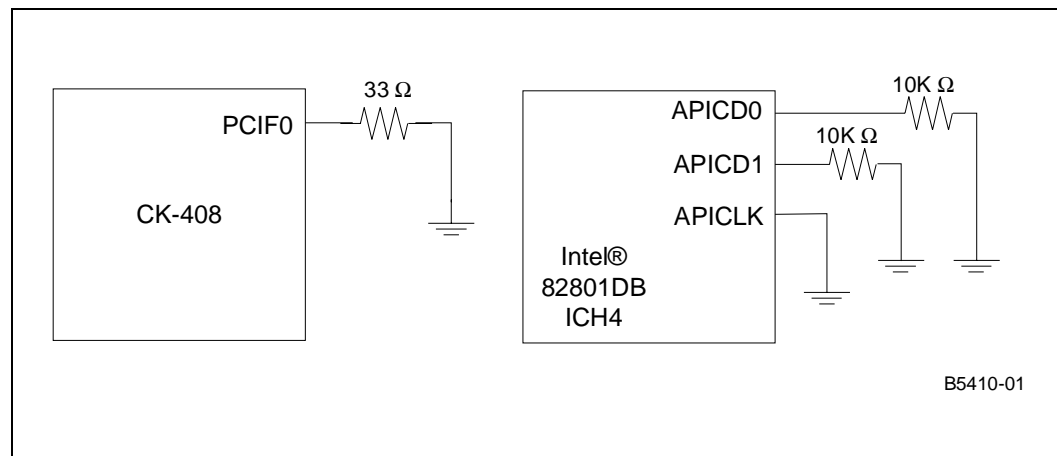
UP systems not using the IOAPIC Bus should follow these recommendations:

On the ICH4:

3. Tie APICCLK directly to ground.
4. Tie APICD0, APICD1 to ground through a 10 k Ω resistor (separate pull-downs are required if using XOR chain testing).

Figure 141 shows the minimum IOAPIC disable topology.

Figure 141. Minimum IOAPIC Disable Topology



11.8.2 PIRQ Routing Example

Table 104 presents how the ICH4 uses the PCI IRQ when the IOAPIC is active.

Table 104. IOAPIC Interrupt Inputs 16 Through 23 Usage

Number	IOAPIC INTIN Pin	Function in Intel® ICH4 Using the PCI IRQ in IOAPIC
1	IOAPIC INTIN PIN 16 (PIRQA)	USB UHCI Controller #1
2	IOAPIC INTIN PIN 17 (PIRQB)	AC'97 Audio and Modem; option for SMBus
3	IOAPIC INTIN PIN 18 (PIRQC)	USB UHCI Controller #3; Native IDE
4	IOAPIC INTIN PIN 19 (PIRQD)	USB UHCI Controller #2
5	IOAPIC INTIN PIN 20 (PIRQE)	Internal LAN; option for SCI, TCO, MMT #0,1,2
6	IOAPIC INTIN PIN 21 (PIRQF)	Option for SCI, TCO, MMT #0,1,2
7	IOAPIC INTIN PIN 22 (PIRQG)	Option for SCI, TCO, MMT #0,1,2
8	IOAPIC INTIN PIN 23 (PIRQH)	USB EHCI Controller, Option for SCI, TCO, MMT #0,1,2

Due to different system configurations, IRQ line routing to the PCI slots (swizzling) should be made to minimize sharing of interrupts between both internal ICH4 functions and PCI functions.

Note: It is not necessarily an optimal routing scheme; an optimal scheme depends on individual system PCI IRQ usage.

Figure 142 shows an example of IRQ line routing to the PCI slots.

Figure 142. Example PIRQ Routing

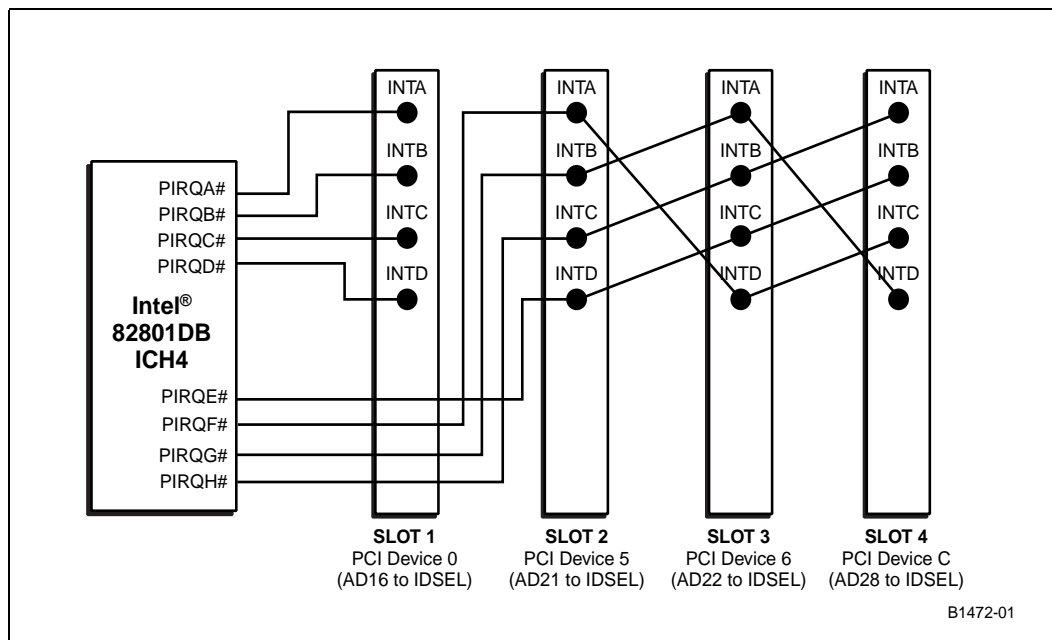


Figure 142 is an example. It is up to board designers to route these signals in a way that proves the most efficient for their particular system. A PCI slot may be routed to share interrupts with any of the ICH4's internal device/functions, but at a higher latency cost.

11.9 SMBus 2.0/SMLink Interface

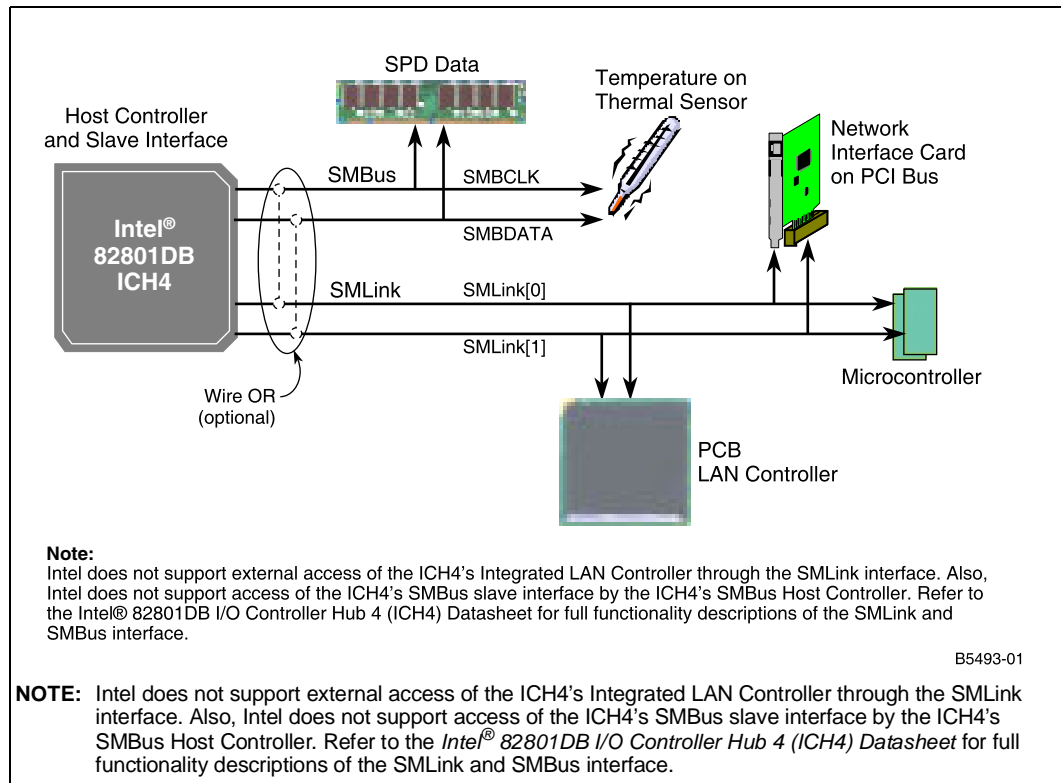
The SMBus interface on the ICH4 uses two signals, SMBCLK and SMBDATA, to send and receive data from components residing on the bus. These signals are used exclusively by the SMBus host controller. The SMBus host controller resides inside the ICH4.

The ICH4 incorporates an SMLink interface supporting Alert-on-LAN*, Alert-on-LAN2*, and a slave functionality. It uses two signals, SMLINK[1:0]. SMLINK[0] corresponds to an SMBus clock signal and SMLINK[1] corresponds to an SMBus data signal. These signals are part of the SMB slave interface.

For Alert-on-LAN* functionality, the ICH4 transmits heartbeat and event messages over the interface. When using the Intel® 82562EM Platform LAN Connect component, the ICH4's integrated LAN controller claims the SMLink heartbeat and event messages and sends them out over the network. An external, Alert-on-LAN2*-enabled LAN Controller (i.e., Intel 82562EM 10/100 Mbps Platform LAN Connect) connects to the SMLink signals to receive heartbeat and event messages, as well as access the ICH4 SMBus slave interface. The slave interface function allows an external microcontroller to perform various functions. For example, the slave write interface may reset or wake a system, generate SMI# or interrupts, and send a message. The slave-read interface may read the system power state, read the watchdog timer status, and read system status bits.

Both the SMBus host controller and the SMBus slave interface obey the SMBus 1.0 protocol, so the two interfaces may be externally wire-OR'ed together to allow an external management ASIC (such as Intel 82562EM 10/100 Mbps Platform LAN Connect) to access targets on the SMBus as well as the ICH4 slave interface. Additionally, the ICH4 supports slave functionality, including the host notify protocol, on the SMLink pins. To be fully compliant with the SMBus 2.0 specification (which requires the host notify cycle), the SMLink and SMBus signals **must** be tied together externally. This is done by connecting SMLink[0] to SMBCLK and SMLink[1] to SMBDATA. [Figure 143](#) illustrates SMBUS 2.0/SMLink protocol.

Figure 143. SMBUS 2.0/SMLink Protocol



11.9.1 SMBus Architecture and Design Considerations

11.9.1.1 SMBus Design Considerations

There is not a single SMBus design solution that works for all platforms. One must consider the total bus capacitance and device capabilities when designing SMBus segments. Routing SMBus to the PCI slots makes the design process even more challenging because they add so much capacitance to the bus. This extra capacitance has a large effect on the bus time constant which in turn affects the bus rise and fall times.

Primary considerations in the design process are:

- Device class (high/low power). Most designs use primarily high power devices.
- Devices that must run in S3
- Amount of $V_{CC-SUSPEND}$ current available, i.e., minimizing load of $V_{CC-SUSPEND}$.

11.9.1.2 General Design Issues/Notes

Regardless of the architecture used, there are some general considerations.

- The pull-up resistor size for the SMBus data and clock signals is dependent on the bus load (this includes all device leakage currents). Generally the SMBus device that may sink the least amount of current is the limiting agent on how small the resistor may be. The pull-up resistor

cannot be made so large that the bus time constant (Resistance X Capacitance) does not meet the SMBus rise and fall time specification.

- The maximum bus capacitance that a physical segment may reach is 400 pF.
- The ICH4 does not run SMBus cycles while in S3.
- SMBus devices that may operate in S3 must be powered by the $V_{CC_SUSPEND}$ supply.
- When SMBus is to be connected to PCI, it must be connected to all PCI slots.

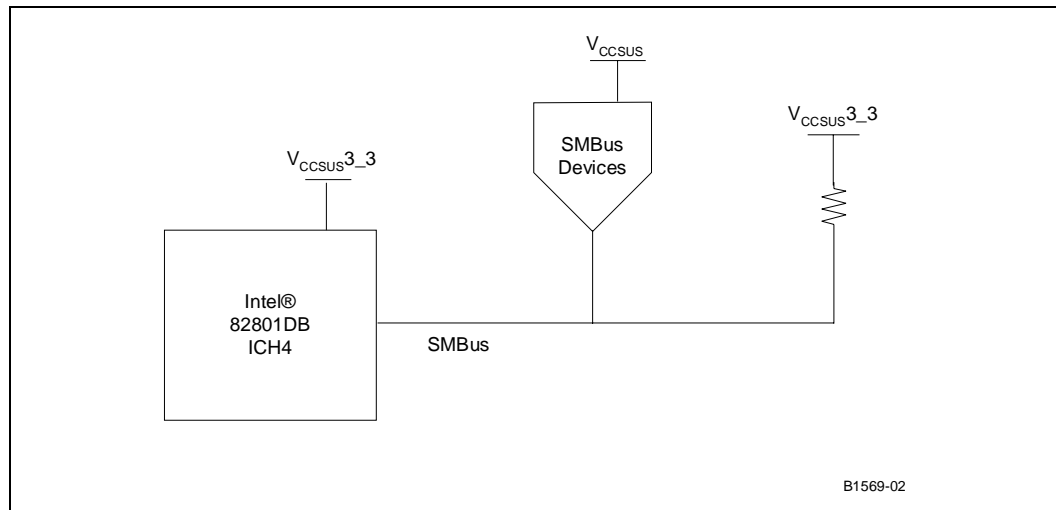
11.9.1.3 Power Supply Considerations

11.9.1.3.1 Unified $V_{CC_SUSPEND}$ Architecture

In this design all SMBus devices are powered by the $V_{CC_SUSPEND}$ supply. Consideration must be made to provide enough $V_{CC_SUSPEND}$ current while in S3.

Figure 144 illustrates the unified $V_{CC_SUSPEND}$ architecture.

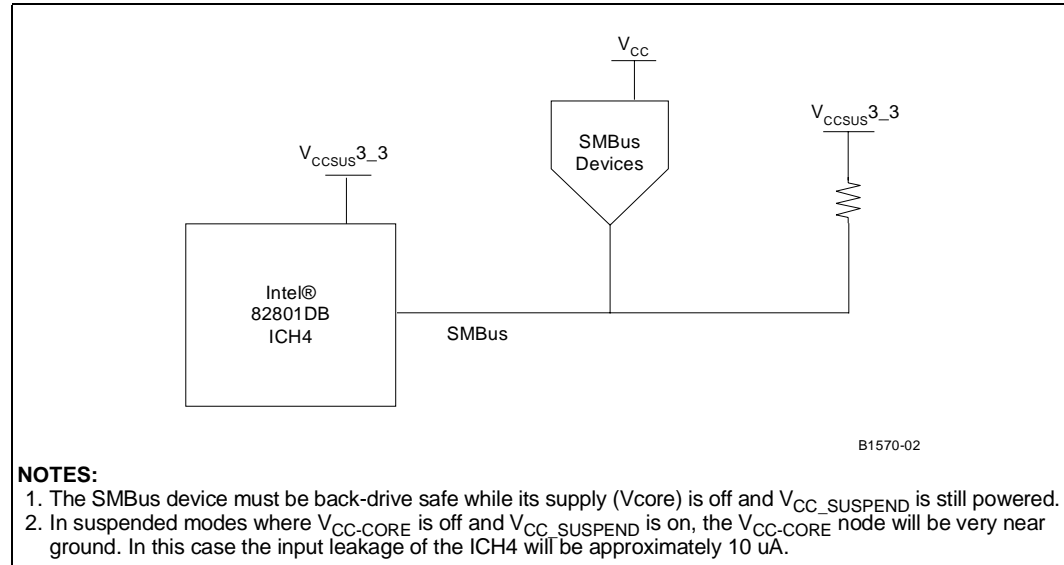
Figure 144. Unified $V_{CC_SUSPEND}$ Architecture



11.9.1.3.2 Unified $V_{CC-CORE}$ Architecture

In this design, all SMBus devices are powered by the $V_{CC-CORE}$ supply. This architecture allows none of the devices to operate in S3, but minimizes the load on $V_{CC_SUSPEND}$. Figure 145 illustrates the unified $V_{CC-CORE}$ architecture.

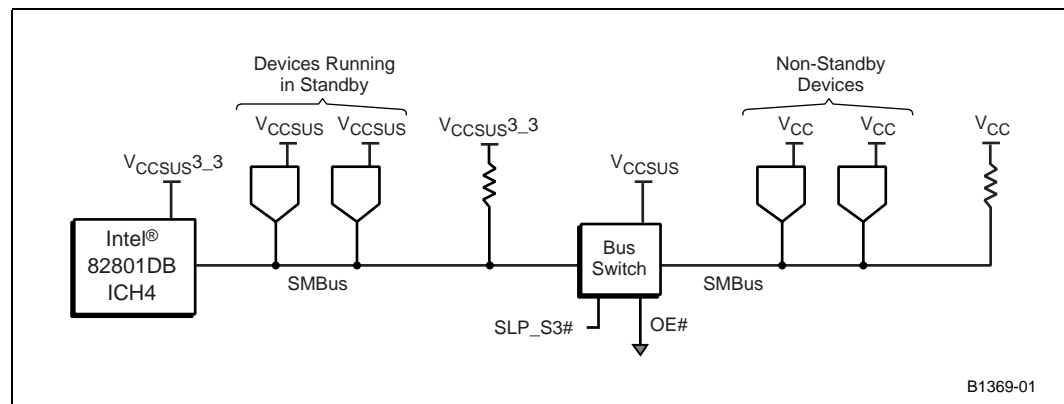
Figure 145. Unified $V_{CC-CORE}$ Architecture



11.9.1.3.3 Mixed Power Supply Architecture

This design allows for SMBus devices to communicate while in S3, yet minimizes $V_{CC_SUSPEND}$ leakage by keeping non-essential devices on the core supply. This is accomplished by the use of a bus switch to isolate the devices powered by the core and suspend supplies. Figure 146 illustrates the mixed $V_{CC_SUSPEND}/V_{CC-CORE}$ architecture.

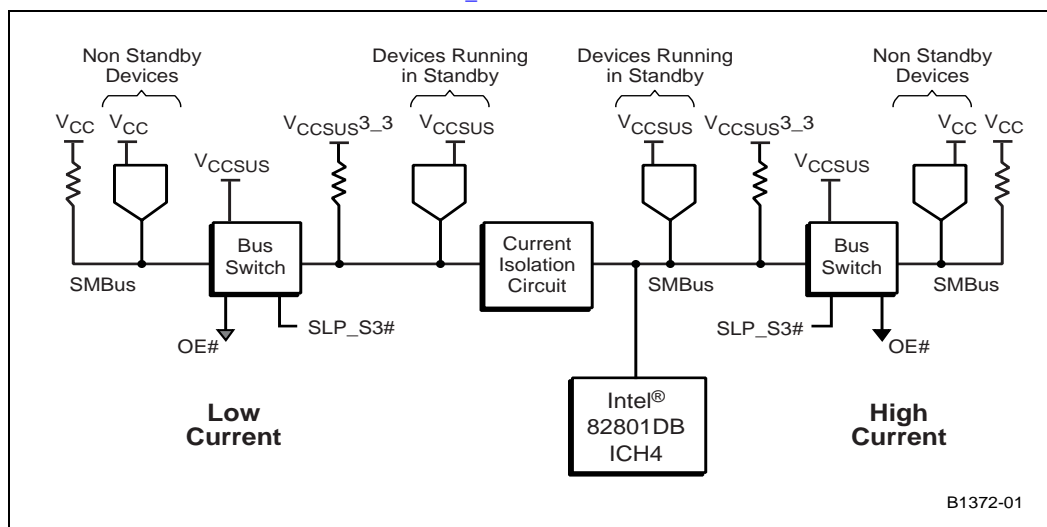
Figure 146. Mixed $V_{CC_SUSPEND}/V_{CC-CORE}$ Architecture



11.9.1.4 Device Class Considerations

In addition to the power supply considerations described above, system designers should take into consideration the SMBus device class (high power/low power) used on the bus. When the design supports both high- power and low-power devices on the bus, current isolation of high-power segment and low-power segment of the bus is needed as shown in Figure 147.

Figure 147. High Power/Low Power Mixed $V_{CC_SUSPEND}/V_{CC_CORE}$ Architecture



11.10 FWH

The following sections provide general guidelines for compatibility and design recommendations for supporting the FWH device. The majority of the changes may be incorporated in the BIOS. Refer to the *FWH BIOS Specification* or equivalent.

11.10.1 FWH Decoupling

A 0.1 μ F capacitor should be placed between the V_{CC} supply pins and the V_{SS} ground pins to decouple high-frequency noise, which may affect the programmability of the device. Additionally, a 4.7 μ F capacitor should be placed between the V_{CC} supply pins and the V_{SS} ground pins to decouple low-frequency noise. The capacitors should be placed no further than 390 mils from the V_{CC} supply pins.

11.10.2 In-Circuit FWH Programming

All cycles destined for the FWH appear on PCI. The ICH4 hub interface to PCI bridge puts all CPU boot cycles out on PCI (before sending them out on the FWH interface). When the ICH4 is set for subtractive decode, these boot cycles may be accepted by a positive decode agent on the PCI bus. This enables the ability to boot from a PCI card that positively decodes these memory cycles. To boot from a PCI card, it is necessary to keep the ICH4 in subtractive decode mode. When a PCI boot card is inserted and the ICH4 is programmed for positive decode, there are two devices positively decoding the same cycle.

11.10.3 FWH INIT# Voltage Compatibility

The FWH INIT# signal trip points need to be considered because they are NOT consistent among different FWH manufacturers. The INIT# signal is active low. Therefore, the inactive state of the ICH4 INIT# signal needs to be at a value slightly higher than the V_{IH} min FWH INIT# pin specification. The inactive state of this signal is typically governed by the formula $V_{CPU_IO(min)} - \text{noise margin}$. Therefore, if the $V_{CPU_IO(min)}$ of the processor is 1.60 V, the noise margin is 200 mV and the V_{IH} min spec of the FWH INIT# input signal is 1.35 V, there would be no compatibility issue because $1.60\text{ V} - 0.2\text{ V} = 1.40\text{ V}$, which is greater than the 1.35 V minimum of the FWH. If the V_{IH} min of the FWH was 1.45 V, there would be an incompatibility and logic translation would need to be used. The examples above do not take into account any noise that may be encountered on the INIT# signal. Ensure that the V_{IH} min specification is met with ample noise margin. In applications where it is necessary, use translation logic.

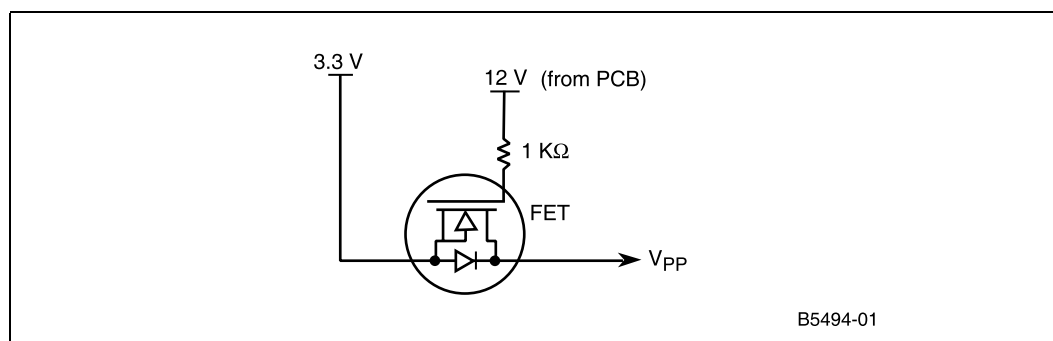
The solution assumes that level translation is necessary. It is strongly recommended that any system that implements a FWH should have its INIT# input connected to the ICH4.

11.10.4 FWH V_{PP} Design Guidelines

The V_{PP} pin on the FWH is used for programming the flash cells. The FWH supports V_{PP} of 3.3 V or 12 V. When V_{PP} is 12 V, the flash cells program about 50% faster than at 3.3 V. However, the FWH only supports 12 V V_{PP} for 80 hours (3.3 V on V_{PP} does not affect the life of the device). The 12 V V_{PP} would be useful in a programmer environment, which is typically an event that occurs very infrequently (much less than 80 hours). The V_{PP} pin MUST be tied to 3.3 V on the PCB.

In some cases, it is desirable to program the FWH during assembly with the device soldered on the board. To decrease programming time, it becomes necessary to apply 12 V to the V_{PP} pin. The following circuit allows testers to put 12 V on the V_{PP} pin while keeping the voltage separate from the 3.3 V plane to which the rest of the power pins are connected. This circuit also allows the board to operate with 3.3 V on the pin during normal operation. Figure 148 shows the FWH V_{PP} isolation circuitry.

Figure 148. FWH V_{PP} Isolation Circuitry

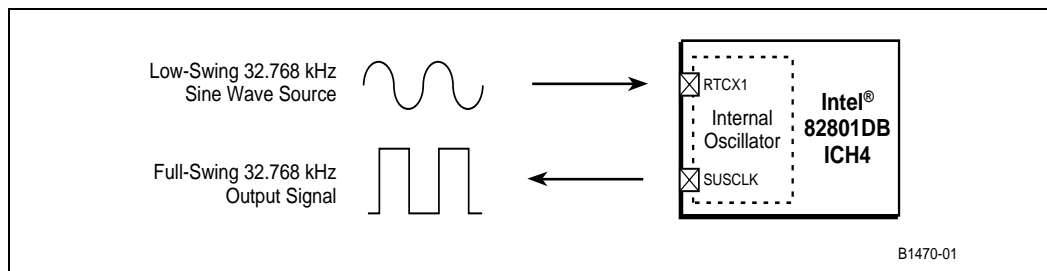


11.11 RTC

The ICH4 contains a real time clock (RTC) with 256 bytes of battery backed SRAM. The internal RTC module provides two key functions: keeping date and time and storing system data in its RAM when the system is powered down.

The ICH4 uses a crystal circuit to generate a low-swing, 32 KHz input sine wave. This input is amplified and driven back to the crystal circuit via the RTCX2 signal. Internal to the ICH4, the RTCX1 signal is amplified to drive internal logic as well as generate a free-running, full-swing clock output for system use. The ICH4 output ball is labeled SUSCLK, as shown in Figure 149.

Figure 149. RTCX1 and SUSCLK Relationship in the Intel® 82801DB ICH4



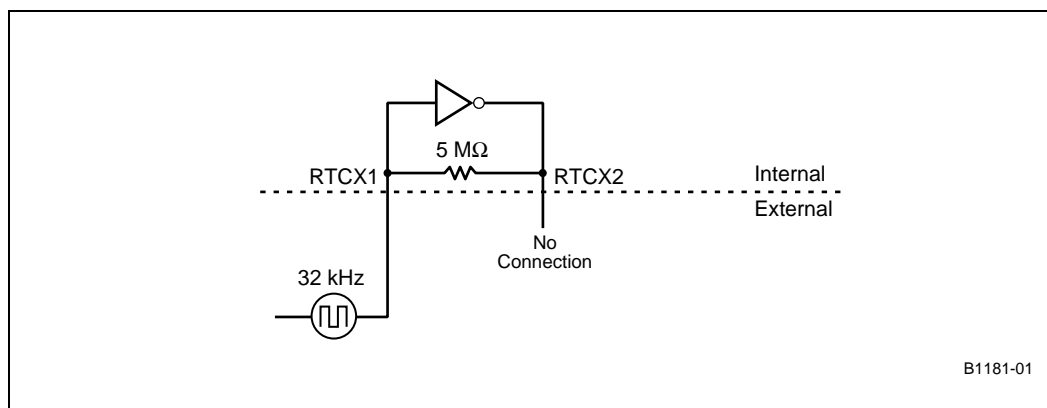
For further information on the RTC, consult *AP-728 Intel ICH Family Real Time Clock (RTC) Accuracy and Considerations under Test Conditions* at <http://www.intel.com/design/chipsets/aplnots/292276.htm>. This application note is valid for the ICH4.

Even if the ICH4 internal RTC is not used, it is still necessary to supply a clock input to RTCX1 of the ICH4 because other signals are gated off that clock in suspend modes. However, in this case the frequency accuracy (32.768 KHz) of the clock inputs is not critical; a crystal may be used or a single clock input may be driven into RTCX1 with RTCX2 left as no connect (Figure 150 shows this connection).

Note: This is not a validated feature on the ICH4. The peak-to-peak swing on RTCX1 cannot exceed 1.0 V.

Figure 150 shows the external circuitry for the ICH4 where the internal RTC is not used.

Figure 150. External Circuitry for the Intel® 82801DB ICH4 Where the Internal RTC is Not Used



11.11.1 RTC Crystal

The ICH4 RTC module requires an external oscillating source of 32.768 KHz connected on the RTCX1 and RTCX2 balls. Figure 151 shows the external circuitry that comprises the oscillator of the ICH4 RTC.

Figure 151. External Circuitry for the Intel® 82801DB ICH4 RTC

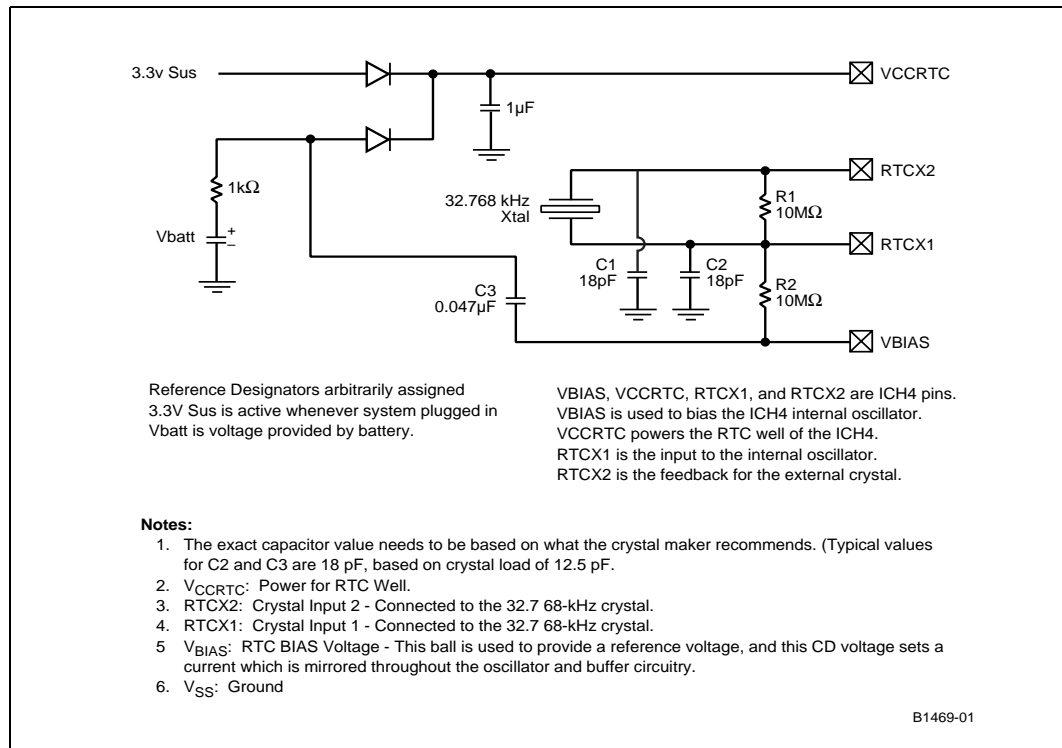


Table 105 presents the RTC routing summary.

Table 105. RTC Routing Summary

RTC Routing Requirements	Maximum Trace Length To Crystal	Signal Length Matching	R1, R2, C1, and C2 Tolerances	Signal Referencing
5 mil trace width (results in ~2 pF per inch)	1 inch	N/A	R1 = R2 = 10 MΩ ± 5% C1 = C2 = (NPO class) See Section 11.11.2 for calculating a specific capacitance value for C1 and C2.	Ground

11.11.2 External Capacitors

To maintain the RTC accuracy, the external capacitor C_3 needs to be 0.047 μF and capacitor values C_1 and C_2 should be chosen to provide the manufacturer's specified load capacitance (C_{load}) for the crystal when combined with the parasitic capacitance of the trace, socket (if used), and package.

[Equation 3](#) may be used to choose the external capacitance values:

Equation 3. External Capacitance Values

$$C_{load} = [(C_1 + C_{in1} + C_{trace1})] \times [(C_2 + C_{in2} + C_{trace2})] / [(C_1 + C_{in1} + C_{trace1} + C_2 + C_{in2} + C_{trace2})] + C_{parasitic}$$

Where:

- C_{load} = Crystal's load capacitance. This value may be obtained from Crystal's specification.
- C_{in1} , C_{in2} = input capacitances at RTCX1, RTCX2 balls of the ICH4. These values may be obtained in the ICH4's Datasheet.
- C_{trace1} , C_{trace2} = Trace length capacitances measured from Crystal terminals to RTCX1, RTCX2 balls. These values depend on the characteristics of board material, the width of signal traces and the length of the traces. A typical value, based on a 5 mil wide trace and a ½ ounce copper pour, is approximately equal to:

$$C_{trace} = \text{trace length} * 2 \text{ pF/inch}$$
- $C_{parasitic}$ = Crystal's parasitic capacitance. This capacitance is created by the existence of two electrode plates and the dielectric constant of the crystal blank inside the Crystal part. Refer to the crystal's specification to obtain this value.

Ideally, C_1 , C_2 may be chosen such that $C_1 = C_2$. Using the equation of C_{load} above, the value of C_1 , C_2 may be calculated to give the best accuracy (closest to 32.768 KHz) of the RTC circuit at room temperature. However, C_2 may be chosen such that $C_2 > C_1$. Then C_1 may be trimmed to obtain the 32.768 KHz.

In certain conditions, both C_1 , C_2 values may be shifted away from the **theoretical values** (calculated values from the above equation) to obtain the closest oscillation frequency to 32.768 KHz. When C_1 , C_2 values are smaller than the theoretical values, the RTC oscillation frequency are higher.

The following example illustrates the use of the practical values C_1 , C_2 in the case that theoretical values cannot ensure the accuracy of the RTC in low temperature condition.

Example 2. Use of Practical Values C_1 and C_2 when Theoretical Values Cannot Ensure the Accuracy of the RTC in Low Temperatures

According to a required 12 pF load capacitance of a typical crystal that is used with the ICH4, the calculated values of $C_1 = C_2$ is 10 pF at room temperature (25 °C) to yield a 32.768 KHz oscillation.

At 0 °C, the frequency stability of crystal gives – 23 ppm (assumed that the circuit has 0 ppm at 25 °C). This makes the RTC circuit oscillate at 32.767246 KHz instead of 32.768 KHz.

When the values of C_1 , C_2 are chosen to be 6.8 pF instead of 10 pF, the RTC oscillates at a higher frequency at room temperature (+23 ppm). However, this configuration of C_1 / C_2 makes the circuit oscillate closer to 32.768 KHz at 0 °C. The 6.8 pF value of C_1 and 2 is the **practical value**.

Note: The temperature dependency of crystal frequency is a parabolic relationship (ppm/degree square). The effect of changing the crystal's frequency when operating at 0 °C (25 °C below room temperature) is the same when operating at 50 °C (25 °C above room temperature).

11.11.3 RTC Layout Considerations

Since the RTC circuit is very sensitive and requires high accuracy oscillation, reasonable care must be taken during layout and routing of the RTC circuit. Some recommendations are:

1. Reduce trace capacitance by minimizing the RTC trace length. The ICH4 requires a trace length less than one inch on each branch (from crystal's terminal to RTCXn ball). Routing the RTC circuit should be kept simple to simplify the trace length measurement and increase accuracy on calculating trace capacitances. Trace capacitance depends on the trace width and dielectric constant of the board's material. On FR-4, a 5 mil trace has approximately 2 pF per inch.
2. Trace signal coupling must be limited as much as possible by avoiding the routing of adjacent PCI signals close to RTCX1 and RTCX2, and VBIAS.
3. Intel recommends a ground guard plane.
4. The oscillator V_{CC} should be clean; use a filter, such as an RC low-pass, or a ferrite inductor.

11.11.4 RTC External Battery Connections

The RTC requires an external battery connection to maintain its functionality and its RAM while the ICH4 is not powered by the system.

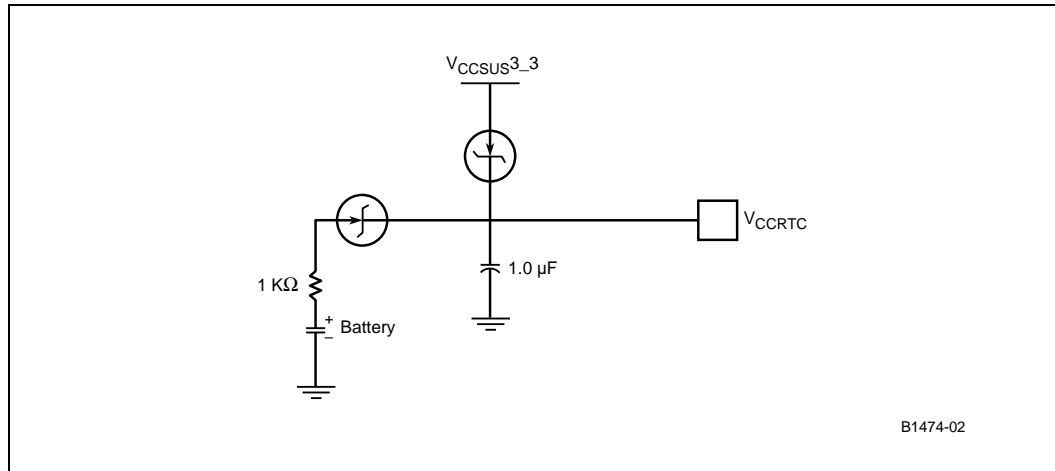
Example batteries are: Duracell® 2032, 2025, or 2016 (or equivalent) that may give many years of operation. Batteries are rated by storage capacity. The battery life may be calculated by dividing the capacity by the average current required. For example, if the battery storage capacity is 170 mAh (assumed usable) and the average current required is 5 µA, the battery life is at least:

$$170,000 \mu\text{Ah} / 5 \mu\text{A} = 34,000 \text{ h} = 3.9 \text{ years}$$

The voltage of the battery may affect the RTC accuracy. In general, when the battery voltage decays, the RTC accuracy also decreases. High accuracy may be obtained when the RTC voltage is in the range of 3.0 V to 3.3 V.

The battery must be connected to the ICH4 through a Schottky diode circuit for isolation. The Schottky diode circuit allows the ICH4 RTC-well to be powered by the battery when the system power is not available, but by the system power when it is available. To do this, the diodes are set to be reverse biased when the system power is not available. [Figure 152](#) is an example of a diode circuit that is used.

Figure 152. Diode Circuit to Connect RTC External Battery

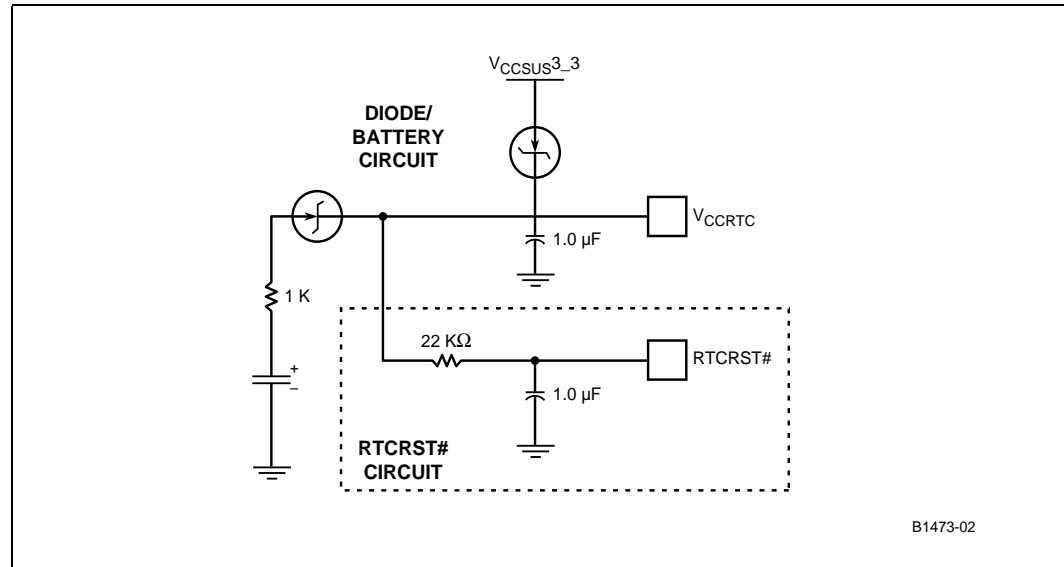


A standby power supply should be used in a mobile system to provide continuous power to the RTC when available, which significantly increases the RTC battery life and thereby the RTC accuracy.

11.11.5 RTC External RTCRST# Circuit

Figure 153 shows an RTCRST# external circuit for the ICH4 RTC.

Figure 153. RTCRST# External Circuit for the Intel® 82801DB ICH4 RTC



The ICH4 RTC requires some additional external circuitry. The RTCRST# signal is used to reset the RTC well. The external capacitor and the external resistor between RTCRST# and the RTC battery (VBAT) were selected to create an RC time delay, such that RTCRST# goes high some time after the battery voltage is valid. The RC time delay should be in the range of 10 ms to 20 ms. When RTCRST# is asserted, bit 2 (RTC_PWR_STS) in the GEN_PMCON_3 (General PM Configuration 3) register is set to 1, and remains set until software clears it. As a result of this, when the system boots, the BIOS knows that the RTC battery has been removed.

This RTCRST# circuit is combined with the diode circuit (shown in Figure 152) whose purpose is to allow the RTC well to be powered by the battery when the system power is not available. Figure 153 is an example of this circuitry that is used in conjunction with the external diode circuit.

11.11.6 VBIAS DC Voltage and Noise Measurements

VBIAS is a DC voltage level that is necessary for biasing the RTC oscillator circuit. This DC voltage level is filtered out from the RTC oscillation signal by the RC network of R2 and C3 (see Figure 151). Therefore, it is a self-adjusting voltage. Board designers should not manually bias the voltage level on VBIAS. Checking VBIAS level is used for testing purposes only to determine the right bias condition of the RTC circuit.

VBIAS should be at least 200 mV DC. The RC network of R2 and C3 will filter out most of AC signal noise that exists on this ball. However, keep the noise on this ball to a minimum in order to ensure the stability of the RTC oscillation.

Probing VBIAS requires the same technique as probing the RTCX1, RTCX2 signals (using Op-Amp). See Application Note AP-728 for further details on measuring techniques.

Note: VBIAS is also very sensitive to environmental conditions.

11.11.7 SUSCLK

SUSCLK is a square waveform signal output from the RTC oscillation circuit. Depending on the quality of the oscillation signal on RTCX1 (largest voltage swing), SUSCLK duty cycle may be between 30-70 percent. When the SUSCLK duty cycle is beyond 30-70% range, it indicates a poor oscillation signal on RTCX1 and RTCX2.

SUSCLK may be probed directly using normal probe (50 Ω input impedance probe) and it is an appropriated signal to check the RTC frequency to determine the accuracy of the ICH4's RTC Clock (see Application Note AP-728 for further details).

11.11.8 RTC-Well Input Strap Requirements

All RTC-well inputs (RSMRST#, RTCRST#, INTRUDER#) must be either pulled up to V_{CCRTC} or pulled-down to ground while in the G3 state. RTCRST# meets this requirement when configured as shown in [Figure 153](#). Provide RSMRST# with a weak external pull-down to ground and INTRUDER# with a weak external pull-up to V_{CCRTC} . This prevents these nodes from floating in G3, and correspondingly prevents I_{CCRTC} leakage that causes excessive coin-cell drain. Configure the PWROK input signal with an external weak pull-down.

11.12 Internal LAN Layout Guidelines

The ICH4 provides several options for LAN capability. The platform supports several components depending upon the target market. Available LAN components include the Intel® 82562ET, and Intel® 82562EM Platform LAN Connect components. [Table 106](#) presents the LAN component connections and features.

Table 106. LAN Component Connections and Features

LAN Component	Interface to Intel® 82801DB ICH4	Connection	Features
Intel® 82562EM (48 Pin SSOP)	LCI	Advanced 10/100 Ethernet	Ethernet 10/100 connection, Alert on LAN* (AoL)
Intel® 82562ET (48 Pin SSOP)	LCI	Basic 10/100 Ethernet	Ethernet 10/100 connection

Design guidelines are provided for each required interface and connection.

Figure 154 shows the ICH4/Platform LAN connect section.

Figure 154. Intel® 82801DB ICH4/Intel® 82562EM and Intel 82562ET Platform LAN Connect Section

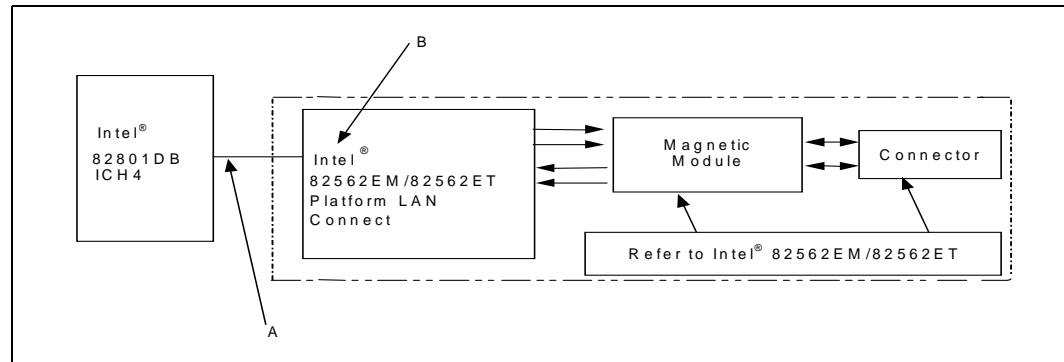


Table 107 presents the LAN design guide section reference.

Table 107. LAN Design Guide Section Reference

Layout Section	Figure 154 Reference	Design Guide Section
Intel® 82801DB ICH4 – LAN Connect Interface (LCI)	A	Section 11.12.1
Intel® 82562EM/Intel® 82562ET Platform LAN Connect Component	B	Section 11.12.2

11.12.1 Intel® 82801DB ICH4 – LAN Connect Interface Guidelines

This section contains guidelines on how to implement a Platform LAN Connect device on a system PCB. The system designer must ensure through simulations or other techniques that the system meets the specified timings. Special care must be given to matching the LAN_CLK traces to those of the other signals, as shown below. The following are guidelines for the ICH4 to LAN Connect Interface. The following signal lines are used on this interface:

- LAN_CLK
- LAN_RSTSYNC
- LAN_RXD[2:0]
- LAN_TXD[2:0]

This interface supports the Intel 82562EM/Intel 82562ET Platform LAN Connect components. Signal lines LAN_CLK, LAN_RSTSYNC, LAN_RXD[0], and LAN_TXD[0] are shared by all components. The AC characteristics for this interface are found in the *Intel® I/O Controller Hub (ICH4) Datasheet*.

11.12.1.1 Bus Topologies

The Platform LAN Connect Interface may be configured in several topologies:

- Direct point-to-point connection between the ICH4 and the LAN component
- LOM/CNR Implementation
- LOM (LAN On PCB) Point-To-Point Interconnect

The following are guidelines for a single solution PCB. The Intel® 82562EM Platform LAN Connect, Intel® 82562ET Platform LAN Connect, or CNR are uniquely installed.

Figure 155 shows the single solution interconnect.

Figure 155. Single Solution Interconnect

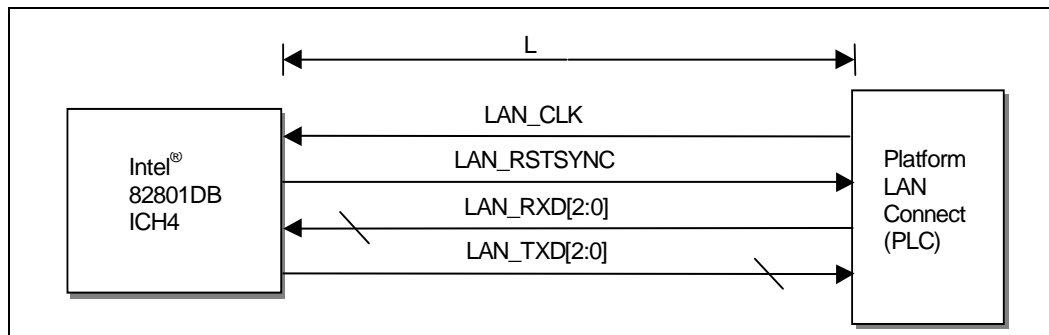


Table 108 presents the LAN LOM routing summary.

Table 108. LAN LOM Routing Summary

LAN Routing Requirements	Maximum Trace Length		Signal Referencing	LAN Signal Length Matching
5 on 10	Intel® 82562ET/ Intel® 82562EM Platform LAN Connect component	4.5 to 12 inches	Ground	Data signals must be equal to no more than 0.5 inches (500 mils) shorter than the LAN dock trace.
	Intel® 82562ET/ Intel® 82562EM Platform LAN Connect component on CNR	2.0 to 9.5 inches		

11.12.1.1.1 LOM (LAN on PCB) and CNR Interconnect

The following guidelines apply to an all-inclusive configuration of PLC design. This layout combines LAN on PCB and the CNR solutions. The resistor pack ensures that either a CNR option or a LAN on PCB option may be implemented at one time. Figure 156 shows the LOM/CNR interconnect.

Figure 156. LOM/CNR Interconnect

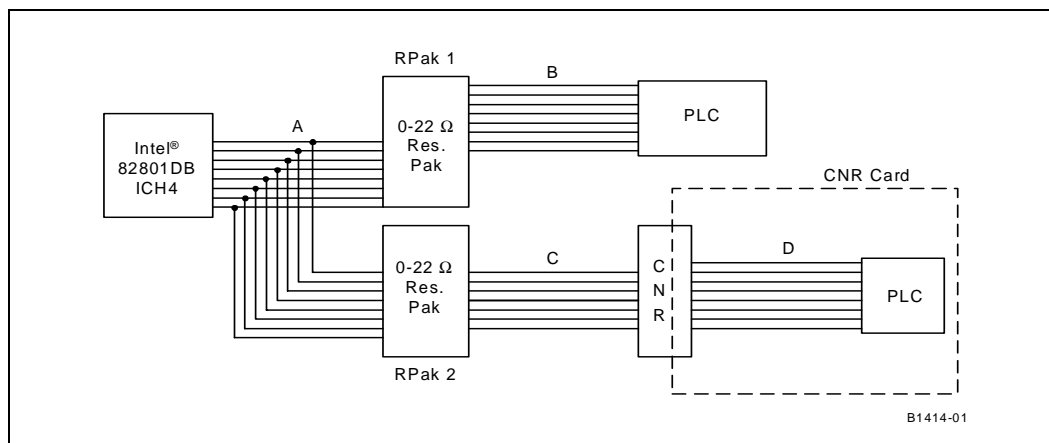


Table 109 presents the LAN LOM/CNR dual routing summary.

Table 109. LAN LOM/CNR Dual Routing Summary

LAN Routing Requirements	Maximum Trace Length					Signal Reference	LAN Signal Length Matching
5 on 10		A	B	C	D	Ground	Data signals must be equal to, or no more than, 0.5 inch (500 mils) shorter than the LAN clock trace.
	82562ET/EM	0.5" to 7.5"	4" to (11.5 – A)"	N/A	N/A		
	82562ET/EM on CNR [†]	0.5" to 7.5"	N/A	1.5" to (9 – A)"	0.5" to 3.0"		

[†] Total trace length should not exceed 9.5 inches.

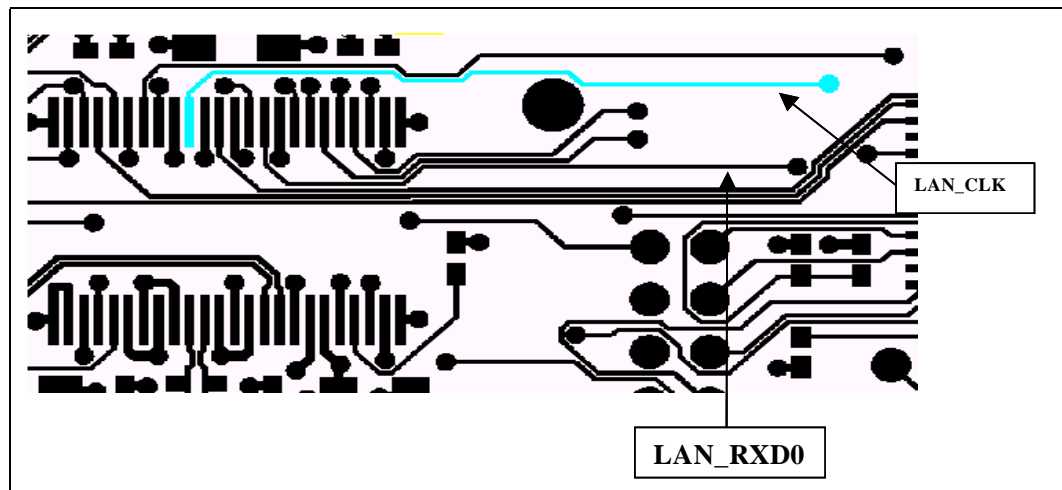
The following are additional guidelines for this configuration:

- Stubs due to the resistor pack should not be present on the surface.
- The resistor pack value may be 0 Ω to 22 Ω

11.12.1.2 Signal Routing and Layout

Platform LAN Connect Interface signals must be carefully routed on the PCB to meet the timing and signal quality requirements of this interface specification. Intel recommends that the board designer simulate the board routing to verify that the specifications are met for flight times and skews due to trace mismatch and crosstalk. On the PCB, the length of each data trace is either equal in length to the LAN_CLK trace or up to 0.5 inch shorter than the LAN_CLK trace. (LAN_CLK should always be the longest PCB trace in each group.) Figure 157 shows the LAN_CLK routing example.

Figure 157. LAN_CLK Routing Example



11.12.1.3 Crosstalk Consideration

Noise due to crosstalk must be carefully controlled to a minimum. Crosstalk is the key cause of timing skews and is the largest part of the t_{RMATCH} skew parameter; t_{RMATCH} is the sum of the trace length mismatch between LAN_CLK and the LAN data signals. To meet this requirement on the board, the length of each data trace is either equal to or up to 0.5 inches shorter than the LAN_CLK trace. Minimize noise due to crosstalk from non-PLC signals by maintaining at least 100 mils of spacing.

11.12.1.4 Impedances

The PCB impedances should be controlled to minimize the impact of any mismatch between the PCB. An impedance of $55\ \Omega \pm 15\%$ is strongly recommended, otherwise signal integrity requirements may be violated.

11.12.1.5 Line Termination

Line termination mechanisms are not specified for the LAN Connect Interface. Slew rate controlled output buffers achieve acceptable signal integrity by controlling signal reflection, over/undershoot, and ringback. A $0\ \Omega$ to $33\ \Omega$ series resistor may be installed at the driver side of the interface if the developer have concerns about over/undershoot.

Note: The receiver must allow for any drive strength and board impedance characteristic within the specified ranges.

11.12.1.6 Disabling the Intel® 82801DB ICH4 Integrated LAN

The LAN Connect Interface on the ICH4 may be left as a no-connect if it is not used.

11.12.2 Intel® 82562EM/Intel® 82562ET Platform LAN Connect Component Guidelines

For correct LAN performance, designers must follow the general guidelines outlined in [Section 11.12.1](#). Additional guidelines for implementing an Intel® 82562EM or Intel® 82562ET Platform LAN Connect component are provided below.

11.12.2.1 Guidelines for Intel® 82562EM/Intel® 82562ET Platform LAN Connect Component Placement

Component placement may affect signal quality, emissions, and temperature of a board design. This section provides the guidelines for component placement.

Careful component placement may:

- Decrease potential problems directly related to electromagnetic interference (EMI) that may cause failure to meet FCC and IEEE test specifications.
- Simplify the task of routing traces. To some extent, component orientation affects the complexity of trace routing. The overall objective is to minimize turns and crossovers between traces.

Minimizing the amount of space needed for the Ethernet LAN interface is important because all other interfaces compete for physical space on a PCB near the connector edge. As with most subsystems, the Ethernet LAN circuits need to be as close as possible to the connector. Thus, it is imperative that all designs be optimized to fit in a very small space.

11.12.2.2 Crystals and Oscillators

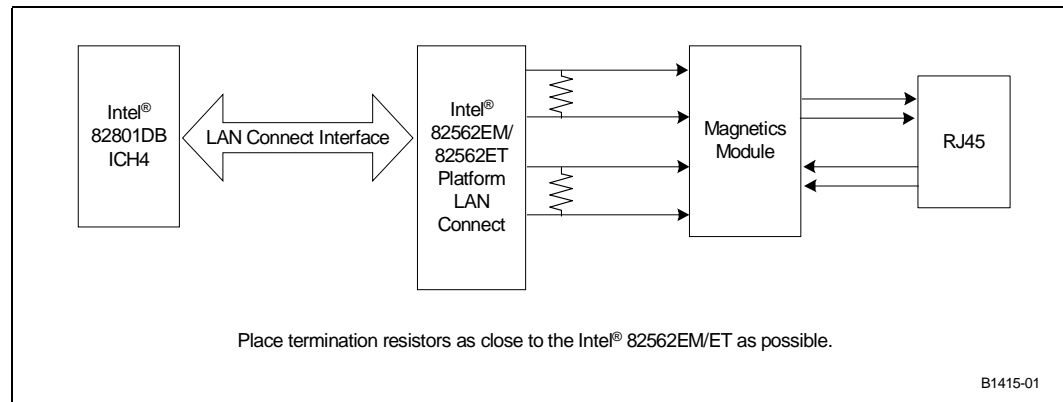
To minimize the effects of EMI, do not place clock sources near I/O ports or board edges. Radiation from these devices may be coupled onto the I/O ports or out of the system chassis. Keep crystals away from the ethernet magnetics module to prevent interference of communication. The retaining straps of the crystal (if they exist) should be grounded to prevent the possibility radiation from the crystal case and the crystal should lay flat against the PC board to provide better coupling of the electromagnetic fields to the board.

For a noise free and stable operation, place the crystal and associated discrete components as close as possible to the Intel® 82562EM/ Intel® 82562 ET Platform LAN Connect component, keeping the trace length as short as possible and do not route any noisy signals in this area.

11.12.2.3 Intel® 82562ET/Intel® 82562EM Platform LAN Connect Component Termination Resistors

Place the $100\ \Omega \pm 1\%$ resistor used to terminate the differential transmit pairs (TDP/TDN) and the $121\ \Omega \pm 1\%$ resistor used to terminate the receive differential pairs (RDP/RDN) as close to the Platform LAN connect component (Intel 82562EM or Intel 82562ET) as possible. This is due to the fact these resistors are terminating the entire impedance that is seen at the termination source (that is, Intel 82562ET), including the wire impedance reflected through the transformer. [Figure 158](#) shows the Intel 82562EM / Intel 82562ET Platform LAN Connect component termination.

Figure 158. Intel® 82562EM/Intel 82562ET Component Termination



11.12.2.4 Critical Dimensions

There are two dimensions to consider during layout. Distance 'A' from the line RJ-45 connector to the magnetics module and distance 'B' from the Intel® 82562EM or Intel® 82562ET Platform LAN Connect component to the magnetics module. The combined total distances A and B must not exceed four inches (preferably, less than two inches).

Figure 159 shows the critical dimension for component placement.

Figure 159. Critical Dimensions for Component Placement

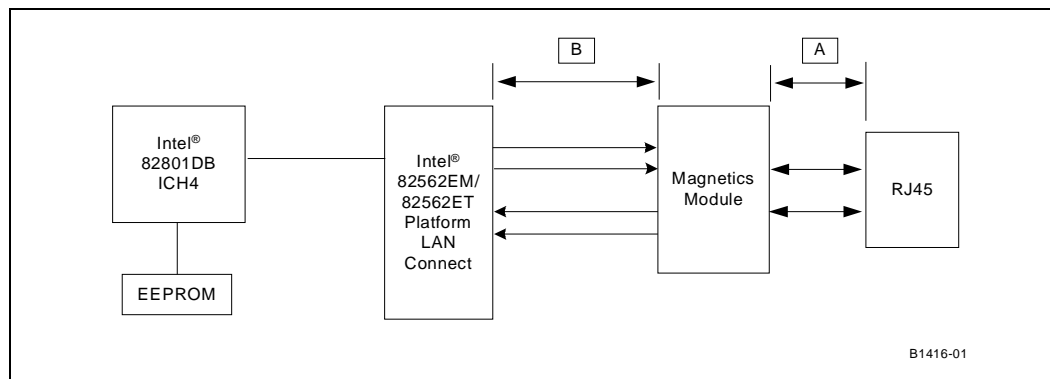


Table 110 presents the guidelines for Figure 159.

Table 110. Guidelines for Figure 159

Distance	Priority	Guideline
A	1	< 1 inch
B	2	< 1 inch

11.12.2.4.1 Distance from Magnetics Module to RJ-45 (Distance A)

Distance A in Figure 159 should be given the highest priority in board layout. Keep the distance between the magnetics module and the RJ-45 connector to less than one inch of separation. Observe the following important trace characteristics:

- **Differential Impedance:** The differential impedance should be 100 Ω . The single ended trace impedance will be approximately 55 Ω ; however, the differential impedance may also be affected by the spacing between the traces.
- **Trace Symmetry:** Route the differential pairs (such as TDP and TDN) with consistent separation and with exactly the same lengths and physical dimensions (for example, width).

Caution: Asymmetric and unequal length traces in the differential pairs contribute to common mode noise. This may degrade the receive circuit's performance and contribute to radiated emissions from the transmit circuit. When the Intel 82562ET Platform LAN Connect component must be placed further than a couple of inches from the RJ-45 connector, distance B may be sacrificed. Keeping the total distance between the Intel 82562ET and RJ-45 as short as possible is a priority.

- **Measured trace impedance** for layout designs targeting 100 Ω often result in lower actual impedance. OEMs need to verify actual trace impedance and adjust their layout accordingly. When the actual impedance is consistently low, a target of 105 Ω to 110 Ω may compensate for second order effects.

11.12.2.4.2 Distance from the Intel® 82562ET Platform LAN Connect Component to Magnetics Module (Distance B)

Design Distance B to be designed to be less than one inch between devices. The high-speed nature of the signals propagating through these traces requires that the distance between these components be closely observed. In general, any section of traces that is intended for use with high-speed signals should observe proper termination practices. Proper termination of signals may reduce reflections caused by impedance mismatches between device and traces. The reflections of a signal may have a high frequency component that may contribute more EMI than the original signal itself. For this reason, these traces should be designed to a 100 Ω differential value. Ensure that these traces are symmetric and equal length within each differential pair.

11.12.2.5 Reducing Circuit Inductance

The following guidelines show how to reduce circuit inductance in both backplanes and PCBs.

- Route traces over a continuous ground plane with no interruptions. When there are vacant areas on a ground or power plane, the signal conductors should not cross the vacant area as this increases inductance and associated radiated noise levels.
- Separate noisy logic grounds from analog signal grounds to reduce coupling. Noisy logic grounds may sometimes affect sensitive DC subsystems such as analog to digital conversion, operational amplifiers, etc.
- Connect all ground vias to every ground plane, and similarly, every power via to all power planes at equal potential. This helps reduce circuit inductance.
- Physically locate grounds to minimize the loop area between a signal path and its return path.
- Keep rise and fall times as slow as possible because signals with fast rise and fall times contain many high frequency harmonics that may radiate significantly.
- The most sensitive signal returns closest to the chassis ground should be connected together. This results in a smaller loop area and reduces the likelihood of crosstalk. The effect of different configurations on the amount of crosstalk may be studied using electronics modeling software.

11.12.2.5.1 Terminating Unused Connections

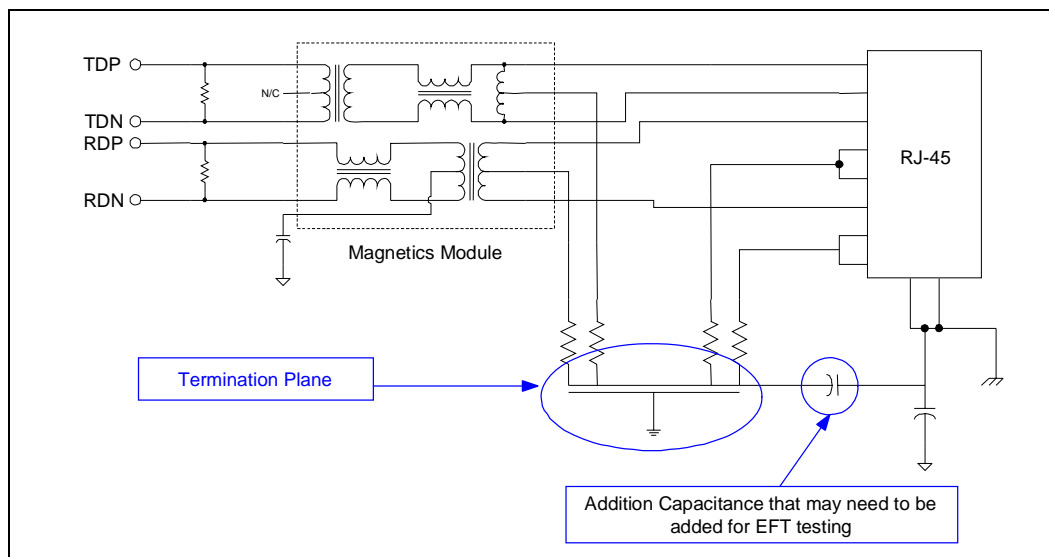
In Ethernet designs, it is common practice to terminate unused connections on the RJ-45 connector and the magnetics module to ground. Depending on overall shielding and grounding design, this may be done to the chassis ground, signal ground, or a termination plane. Care must be taken when using various grounding methods to insure that emission requirements are met. The method most often implemented is called the ‘Bob Smith’ Termination. In this method, a floating termination plane is cut out of a power plane layer. This floating plane acts as a plate of a capacitor with an adjacent ground plane. The signals may be routed through 75 Ω resistors to the plane. Stray energy on unused pins is then carried to the plane.

11.12.2.5.2 Termination Plane Capacitance

Intel recommends that the termination plane capacitance equal a minimum value of 1500 pF. This helps reduce the amount of crosstalk on the differential pairs (TDP/TDN and RDP/RDN) from the unused pairs of the RJ-45. Pads may be placed for an additional capacitance to chassis ground, which may be required if the termination plane capacitance is not large enough to pass EFT (Electrical Fast Transient) testing. When a discrete capacitor is used, to meet the EFT requirements it should be rated for at least 1000 Vac.

Figure 160 shows the termination plane.

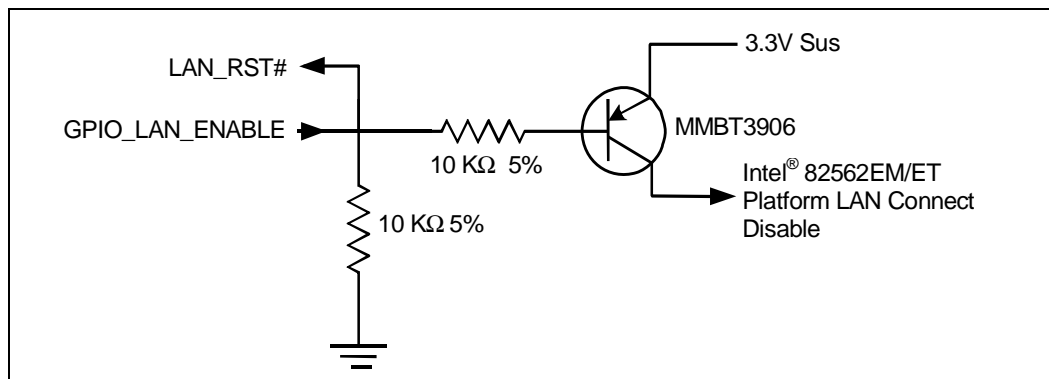
Figure 160. Termination Plane



11.12.3 Intel® 82562EM/Intel® ET Platform LAN Connect Component Disable Guidelines

To disable the Intel® 82562EM/Intel® 82562ET Platform LAN Connect component, the device must be isolated (disabled) prior to reset (RSM_PWROK) asserting. Using a GPIO, such as GPO28 to be LAN_Enable (enabled high), the LAN defaults to enabled on initial power-up and after an AC power loss. This circuit shown in Figure 161 allows this behavior. The BIOS controlling the GPIO may disable the LAN micro-controller.

Figure 161. Intel® 82562EM/Intel® 82562ET Component Disable Circuitry



There are four pins that are used to put the Intel 82562EM/Intel 82562ET Platform LAN Connect component controller in different operating states: Test_En, Isol_Tck, Isol_Ti, and Isol_Tex. Table 111 presents the operational/disable features for this design.

The four control signals presented in [Table 111](#) should be configured as follows: Test_En should be pulled-down through a 100 Ω resistor. The remaining three control signals should each be connected through 100 Ω series resistors to the common node 'Intel 82562ET/EM _Disable' of the disable circuit.

[Table 111](#) presents the Intel® 82562EM/ Intel® 82562ET Platform LAN Connect component control signals.

Table 111. Intel® 82562EM/ Intel® 82562ET Platform LAN Connect Component Control Signals

Test_En	Isol_Tck	Isol_Ti	Isol_Tex	State
0	0	0	0	Enabled
0	1	1	1	Disabled w/ clock (low power)
1	1	1	1	Disabled w/out clock (lowest power)

11.12.4 General Intel® 82562EM/Intel® 82562ET Differential Pair Trace Routing Considerations

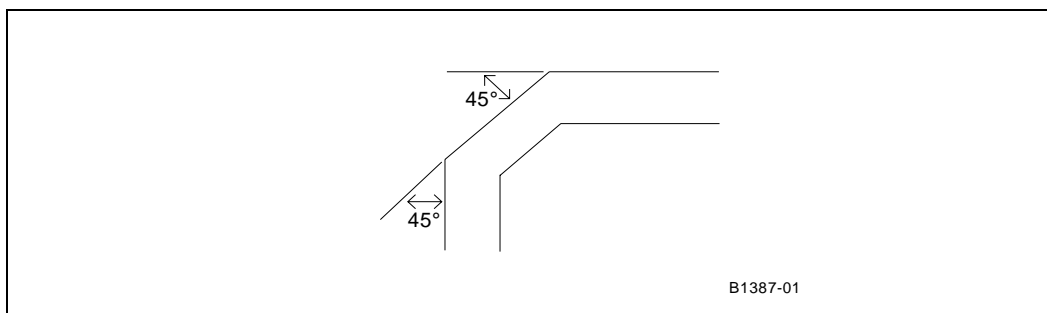
Trace routing considerations are important to minimize the effects of crosstalk and propagation delays on sections of the board where high-speed signals exist. Signal traces should be kept as short as possible to decrease interference from other signals, including those propagated through power and ground planes.

Observe the following suggestions to help optimize board performance. Some suggestions are specific to a 4.3 mil stack-up.

- Maintain constant symmetry and spacing between the traces within a differential pair.
- Keep the signal trace lengths of a differential pair equal to each other.
- Keep the total length of each differential pair under four inches. Many customer designs with differential traces longer than five inches have had one or more of the following issues: IEEE phy conformance failures, excessive EMI (Electro Magnetic Interference), and/or degraded receive BER (Bit Error Rate).
- Do not route the transmit differential traces closer than 100 mils to the receive differential traces.
- Do not route any other signal traces both parallel to the differential traces, and closer than 100 mils to the differential traces (300 mils is recommended).
- Keep maximum separation between differential pairs to 7 mils.
- For high-speed signals, the number of corners and vias should be kept to a minimum. When a 90° bend is required, it is recommended to use two 45° bends instead. Refer to [Figure 162](#).
- Traces should be routed away from board edges by a distance greater than the trace height above the ground plane. This allows the field around the trace to couple more easily to the ground plane rather than to adjacent wires or boards.
- Do not route traces and vias under crystals or oscillators. This prevents coupling to, or from, the clock. And as a general rule, place traces from clocks and drives at a minimum distance from apertures by a distance that is greater than the largest aperture dimension.

Figure 162 shows trace routing.

Figure 162. Trace Routing



11.12.4.1 Trace Geometry and Length

The key factors in controlling trace EMI radiation are the trace length and the ratio of trace-width to trace-height above the ground plane. To minimize trace inductance, high-speed signals and signal layers that are close to a ground or power plane should be as short and wide as practical. Ideally, this trace width to height above the ground plane ratio is between 1:1 and 3:1. To maintain trace impedance, the width of the trace should be modified when changing from one board layer to another if the two layers are not equidistant from the power or ground plane. Differential trace impedances should be controlled to be $\sim 100 \Omega$. It is necessary to compensate for trace-to-trace edge coupling that may lower the differential impedance by up to 10Ω when the traces within a pair are closer than 30 mils (edge to edge).

Traces between decoupling and I/O filter capacitors should be as short and wide as practical. Long and thin traces are more inductive and would reduce the intended effect of decoupling capacitors. Also for similar reasons, traces to I/O signals and signal terminations should be as short as possible. Vias to the decoupling capacitors should be sufficiently large in diameter to decrease series inductance. Additionally, the PLC should not be closer than one inch to the connector/magnetics/edge of the board.

11.12.4.2 Signal Isolation

Some rules to follow for signal isolation:

- Separate and group signals by function on separate layers if possible. Maintain a gap of 100 mils between all differential pairs (Ethernet) and other nets, but group associated differential pairs together.

Note: Over the length of the trace run, each differential pair should be at least 0.3 inch away from any parallel signal traces.

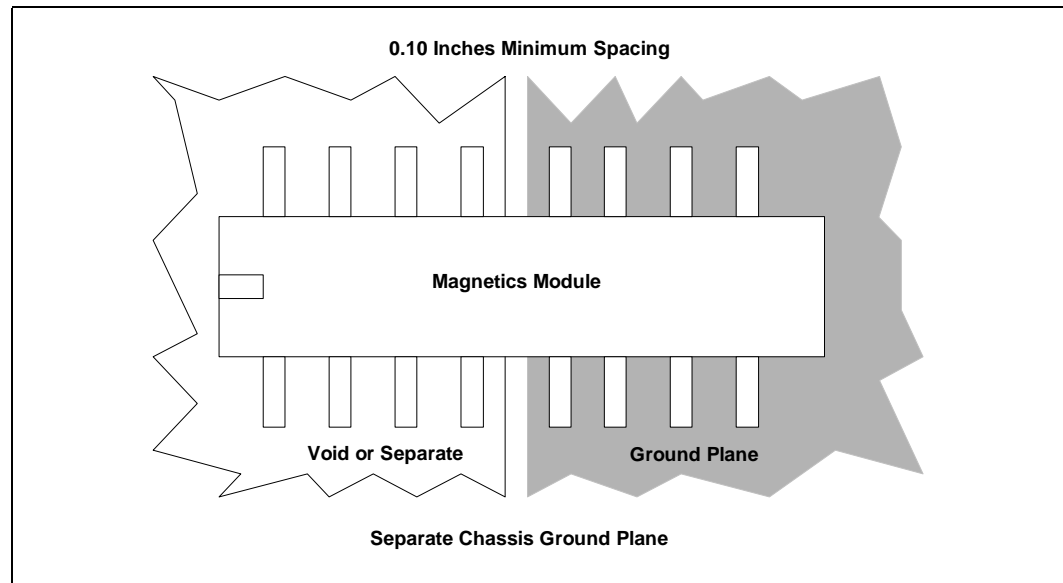
- Physically group together all components associated with one clock trace to reduce trace length and radiation.
- Isolate I/O signals from high speed signals to minimize crosstalk that may increase EMI emission and susceptibility to EMI from other signals.
- Avoid routing high-speed LAN traces near other high-frequency signals associated with a video controller, cache controller, CPU, or other similar devices.

11.12.4.3 Magnetics Module General Power and Ground Plane Considerations

To properly implement the common mode choke functionality of the magnetics module the chassis or output ground (secondary side of transformer) should be separated from the digital or input ground (primary side) by a physical separation of 100 mils minimum.

Figure 163 shows the ground plane separation.

Figure 163. Ground Plane Separation



Good grounding requires minimizing inductance levels in the interconnections and keeping ground returns short, signal loop areas small, and power inputs bypassed to signal return, significantly reduces EMI radiation.

Some rules to follow that help reduce circuit inductance in both backplanes and PCBs include the following:

- Route traces over a continuous plane with no interruptions (do not route over a split plane). When there are vacant areas on a ground or power plane, avoid routing signals over the vacant area. This increases inductance and EMI radiation levels.
- Separate noisy digital grounds from analog grounds to reduce coupling. Noisy digital grounds may affect sensitive DC subsystems.
- Connect all ground vias to every ground plane and connect every power via to all power planes at equal potential. This helps reduce circuit inductance.
- Physically locate grounds between a signal path and its return. This minimizes the loop area.
- Avoid fast rise/fall times as much as possible. Signals with fast rise and fall times contain many high frequency harmonics that may radiate EMI.
- The ground plane beneath the filter/transformer module should be split. The RJ-45 connector side of the transformer module should have chassis ground beneath it. By splitting ground planes beneath transformer, noise coupling between the primary and secondary sides of the transformer and between the adjacent coils in the transformer is minimized. Verify that a power plane is not placed under the magnetics module.

11.12.4.4 Common Physical Layout Issues

Here is a list of common physical layer design and layout mistakes in LAN on PCB designs.

1. Unequal length of the two traces within a differential pair. Inequalities create common-mode noise and distort the transmit or receive waveforms.
2. Lack of symmetry between the two traces within a differential pair. (Each component and/or via that one trace encounters, the other trace must encounter the same component or a via at the same distance from the PLC.) Asymmetry may create common-mode noise and distort the waveforms.
3. Excessive distance between the PLC and the magnetics or between the magnetics and the RJ-45 connector. Beyond a total distance of about four inches, it may become extremely difficult to design a spec-compliant LAN product. Long traces on FR4 (fiberglass epoxy substrate) attenuate the analog signals. In addition, any impedance mismatch in the traces will be aggravated if they are longer (see #9 below). Keep the magnetics as close to the connector as possible (= one inch).
4. Routing any other trace parallel to and close to one of the differential traces. Crosstalk getting onto the receive channel causes degraded long cable BER. Crosstalk getting onto the transmit channel may cause excessive emissions (failing FCC) and may cause poor transmit BER on long cables. At a minimum, keep other signals 0.3 inch from the differential traces.
5. Routing the transmit differential traces next to the receive differential traces. The transmit trace that is closest to one of the receive traces puts more crosstalk onto the closest receive trace and may greatly degrade the receiver's BER over long cables. After exiting the PLC, keep the transmit traces 0.3 inch or more away from the nearest receive trace. The only possible exceptions are in the vicinities where the traces enter or exit the magnetics, the RJ-45, and the PLC.
6. Use of an inferior magnetics module. The magnetics modules that Intel uses have been fully tested for IEEE PLC conformance, long cable BER, and for emissions and immunity. (Inferior magnetics modules often have less common-mode rejection and/or no auto transformer in the transmit channel.)
7. Use of an 82555 or 82558 physical layer schematic in a PLC design. The transmit terminations and decoupling are different. There are also differences in the receive circuit. Refer to the appropriate reference schematic or Application Note.
8. Not using (or incorrectly using) the termination circuits for the unused pins at the RJ-45 and for the wire-side center-taps of the magnetics modules. These unused RJ pins and wire-side center-taps must be correctly referenced to chassis ground via the proper value resistor and a capacitance or term plane. When these are not terminated properly, there may be emissions (FCC) problems, IEEE conformance issues, and long cable noise (BER) problems. The Application Notes have schematics that illustrate the proper termination for these unused RJ pins and the magnetics center-taps.
9. Incorrect differential trace impedances. It is important to have ~100 Ω impedance between the two traces within a differential pair. This becomes even more important as the differential traces become longer. It is very common to see customer designs that have differential trace impedances between 75 Ω and 85 Ω , even when the designers think they've designed for 100 Ω . (To calculate differential impedance, many impedance calculators only multiply the single-ended impedance by two. This does not take into account edge-to-edge capacitive coupling between the two traces. When the two traces within a differential pair are kept close to each other, the edge coupling may lower the effective differential impedance by 5 Ω to 20 Ω . A 10 Ω to 15 Ω drop in impedance is common. Short traces have fewer problems if the differential impedance is a little off.

10. Use of capacitor that is too large between the transmit traces and/or too much capacitance from the magnetic's transmit center-tap (on the Intel® 82562ET side of the magnetics) to ground. Using capacitors more than a few pF in either of these locations may slow the 100 Mbps rise and fall time so much that they fail the IEEE rise time and fall time specs. This also causes the return loss to fail at higher frequencies and degrades the transmit BER performance. Caution must be exercised if a cap is put in either of these locations. When a cap is used, it may be less than 22 pF (6 pF to 12 pF values have been used on past designs with reasonably good success). These caps are not necessary, unless there is some overshoot in 100 Mbps mode.

It is important to keep the two traces within a differential pair close† to each other. Close is considered to be less than 0.030 inch between the two traces within a differential pair; 0.007 inch trace-to-trace spacing is recommended. Keeping them close helps to make them more immune to crosstalk and other sources of common-mode noise. This also means lower emissions (that is, FCC compliance) from the transmit traces, and better receive BER for the receive traces.

11.13 GPIO

The ICH4 has 12 general purpose inputs, eight general purpose outputs, and 16 general purpose inputs/outputs as shown in [Table 112](#).

Table 112. Intel® 82562EM/Intel® 82562ET Platform LAN Connect Component Control Signals (Sheet 1 of 2)

GPIO No.	Power Well	Input, Output, I/O	Tolerance	Note
0	Core	Input	5V	2
1	Core	Input	5 V	2
2	Core	Input	5 V	2
3	Core	Input	5 V	2
4	Core	Input	5V	2
5	Core	Input	5 V	2
6	Core	Input	5 V	
7	Core	Input	5 V	
8	Resume	Input	3.3 V	
11	Resume	Input	3.3 V	2
12	Resume	Input	3.3 V	
13	Resume	Input	3.3 V	
16	Core	Output	3.3 V	2
17	Core	Output	3.3 V	2
18	Core	Output	3.3 V	
19	Core	Output	3.3 V	
20	Core	Output	3.3 V	
21	Core	Output	3.3 V	

NOTES:

- Defaults as an output.
- May be used as a GPIO if the native function is not needed. The Intel ICH4 defaults these signals to native functionality.

**Table 112. Intel® 82562EM/Intel® 82562ET Platform LAN Connect Component
Control Signals (Sheet 2 of 2)**

GPIO No.	Power Well	Input, Output, I/O	Tolerance	Note
22	Core	Output (Open Drain)	3.3 V	
23	Core	Output	3.3 V	
24	Resume	I/O	3.3 V	1
25	Resume	I/O	3.3 V	1
27	Resume	I/O	3.3 V	1
28	Resume	I/O	3.3 V	1
32	Core	I/O	3.3 V	1
33	Core	I/O	3.3 V	1
34	Core	I/O	3.3 V	1
35	Core	I/O	3.3 V	1
36	Core	I/O	3.3 V	1
37	Core	I/O	3.3 V	1
38	Core	I/O	3.3 V	1
39	Core	I/O	3.3 V	1
40	Core	I/O	3.3 V	1
41	Core	I/O	3.3 V	1
42	Core	I/O	3.3 V	1
43	Core	I/O	3.3 V	1

NOTES:

1. Defaults as an output.
2. May be used as a GPIO if the native function is not needed. The Intel ICH4 defaults these signals to native functionality.

Miscellaneous Logic

12

The Intel® 82801DB I/O Controller Hub 4 (ICH4) requires additional external circuitry to function properly. Some of these functionalities include meeting timing specifications, buffering signals, and switching between power wells. This logic may be implemented through the use of the Glue Chip or discrete logic.

12.1 Glue Chip 4

To reduce the component count and BOM (Bill of Materials) cost of the ICH4 platform, Intel has developed an ASIC component that integrates miscellaneous platform logic into a single chip. The ICH4 Glue Chip is designed to integrate some or all of the following functions into a single device. By integrating much of the required glue logic into a single device, overall board cost may be reduced.

Features include:

- Dual, strapping, selectable feature sets
- Audio-disable circuit
- Mute audio circuit
- 5 V reference generation
- 5 V standby reference generation
- HD single color LED driver
- IDE reset signal generation/PCIRST# buffers
- PWROK (PWRGD_3V) signal generation
- Power sequencing/ BACKFEED_CUT
- Power supply turn on circuitry
- RSMRST# generation
- Voltage translation from DDC to VGA monitor
- HSYNC/VSYNC voltage translation to VGA monitor
- Tri-state buffers for test
- Extra GP logic gates
- Power LED drivers
- Flash FLUSH#/INIT# circuit

More information regarding this component is available from the vendors presented in [Table 113](#) on the next page.

Table 113. Glue Chip 4 Vendor Information

Vendor	Contact Information	Vendor Part Number
Philips Semiconductor	http://www.semiconductors.philips.com	PCA9504A
Fujitsu Microelectronics	http://www.fujitsumicro.com	MB87B302ABPD-G-ER

12.2 Discrete Logic

As an alternative solution, discrete circuitry may be implemented into a design instead of using the Glue Chip.

Platform Clock Routing Guidelines 13

13.1 System Clock Groups

The system clocks are considered as a subsystem in themselves. At the center of this subsystem is the Clock Synthesizer/Driver component. Several vendors offer suitable products, as defined in the *Intel CK408 Synthesizer/Driver Specification*. This device provides the set of clocks required to implement a platform level PCB solution.

Table 114 presents a breakdown of the various individual clocks.

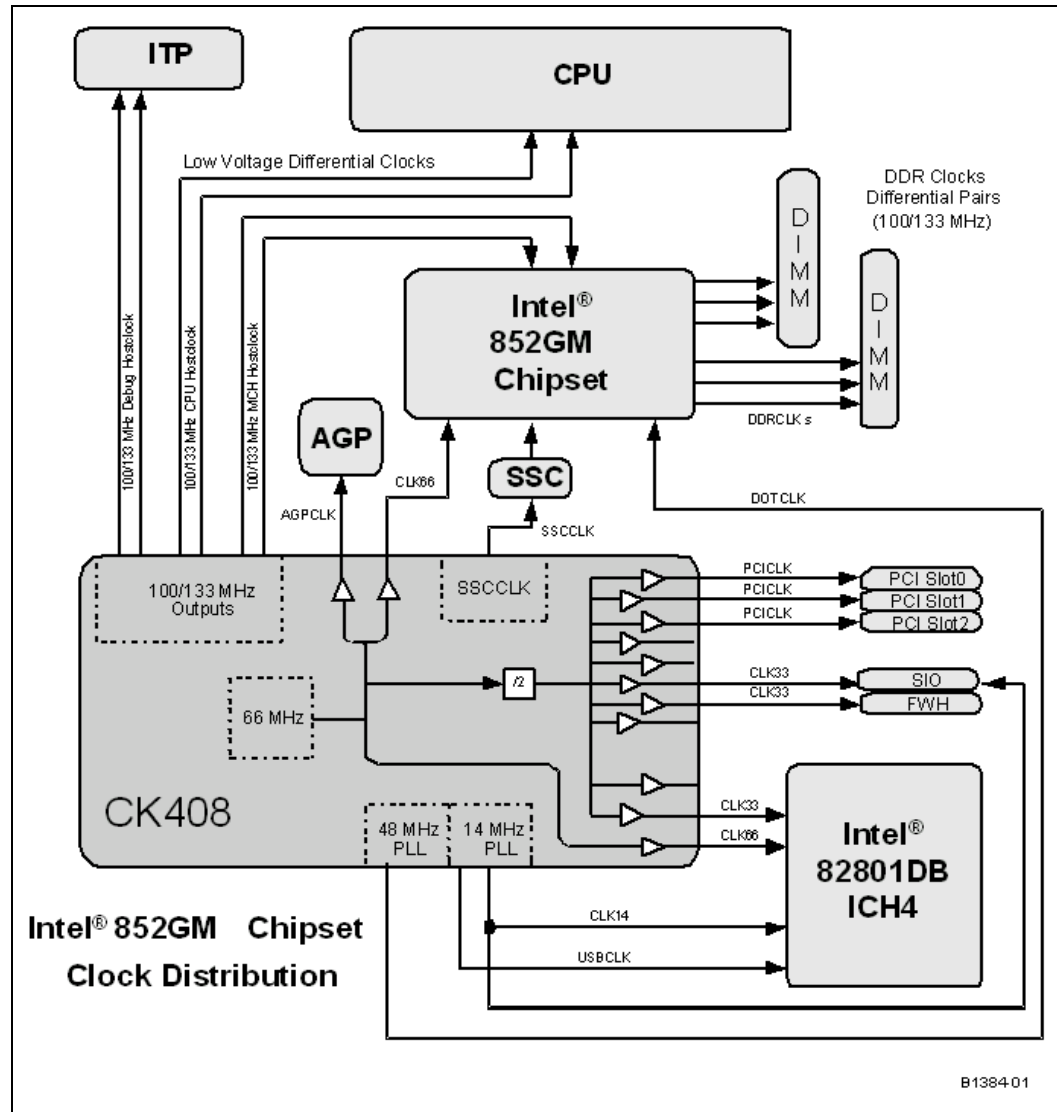
Note: When used in Intel® 852GM chipset platforms, the CK408 is configured in the unbuffered mode and a host clock swing of 710 mV.

Table 114. Individual Clock Breakdown

Clock Group	Frequency	Driver/Pin	Receiver/s	Comments
HOST_CLK	100 MHz	CK408 CPU[2:0]	CPU GMCH Debug Port	Length matched Differential signaling
CLK66	66 MHz	CK408 3V66[5:0]	GMCH Intel® 82801DB I/O Controller Hub 4 (ICH4)	Length matched
CLK33	33 MHz	CK408 PCIF[2:0] PCI[6:0]	ICH4 SIO FWH	Length matched to CLK66 Synchronous but not edge aligned with CLK66 Phase delay of 1.5 ns to 3.5 ns
PCICLK (Expansion)	33 MHz	CK408 PCI[6:0]	PCI Conn #1 PCI Conn #2 PCI Conn #3	Length matched to CLK33 CLK33 length minus 2.5 inches
CLK14	14 MHz	CK408 REF0	ICH4 SIO	Independent clock
DOTCLK	48 MHz	CK408 48 MHz	GMCH	Independent clock
SSCCLK	48/66 MHz	CK408 VCH	GMCH	Independent clock
USBCLK	48 MHz	CK408 48 MHz	ICH4	Independent clock

Figure 164 illustrates the system clock subsystem including the clock generator, major platform components, and all the related clock interconnects.

Figure 164. Clock Distribution Diagram



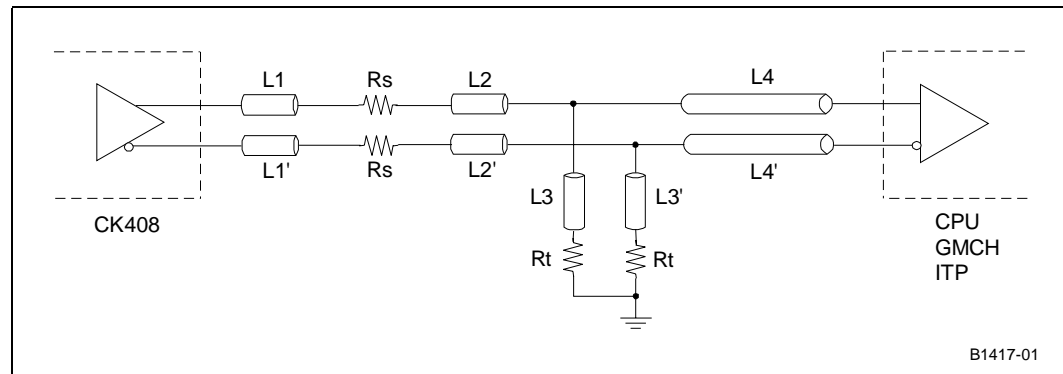
13.2 Clock Group Topologies and Routing Constraints

The topology diagrams and routing constraint tables provided on the following pages define Intel's recommended topology and routing rules for each of the platform level clocks. These topologies and rules have been simulated and verified to produce the required waveform integrity and timing characteristics for reliable platform operation.

13.2.1 Host Clock Group

The host clocks are routed point-to-point as closely coupled differential pairs on the PCB, with dedicated buffers for each of the three loads. These clocks utilize a source shunt termination scheme as shown below in Figure 165.

Figure 165. Source Shunt Termination Topology



The clock driver differential bus output structure is a 'Current Mode Current Steering' output which develops a clock signal by alternately steering a programmable constant current to the external termination resistors R_t . The resulting amplitude is determined by multiplying I_{OUT} by the value of R_t . The current I_{OUT} is programmable by a resistor and an internal multiplication factor so the amplitude of the clock signal can be adjusted for different values of R_t to match impedances or to accommodate future load requirements.

Intel's recommended termination for the differential bus clock is a 'Source Shunt termination.' Parallel R_t resistors perform a dual function, converting the current output of the clock driver to a voltage and matching the driver output impedance to the transmission line. The series resistors R_s provide isolation from the clock driver's output parasitics, which would otherwise appear in parallel with the termination resistor R_t .

Intel's recommended value for R_t is a $49.9 \Omega \pm 1\%$ resistor. The tight tolerance is required to minimize crossing voltage variance. The recommended value for R_s is $33 \Omega \pm 5\%$. Simulations have shown that R_s values above 33Ω provide no benefit to signal integrity but only degrade the edge rate.

The MULT0 pin (CK408 pin #43) should be pulled up through a $10 \text{ k}\Omega$ to V_{CC} – setting the multiplication factor to six.

The IREF pin (CK408 pin #42) should be tied to ground through a $475 \Omega \pm 1\%$ resistor – making the IREF 2.32 mA.

Table 115 presents the host clock group routing constraints.

Table 115. Host Clock Group Routing Constraints

Parameter	Definition
Class Name	HOST_CLK
Class Type	Individual Differential Pairs
Topology	Differential Source Shunt Terminated
Reference Plane	Ground Referenced (contiguous over length)
Single Ended Trace Impedance (Z_0)	55 $\Omega \pm 15\%$
Differential Mode Impedance (Z_{diff})	100 $\Omega \pm 15\%$
Nominal Inner Layer Trace Width	4.0 mils
Nominal Inner Layer Pair Spacing (edge to edge) (except as allowed below)	7.0 mils
Nominal Outer Layer Trace Width	5.0 mils (pin escapes only)
Nominal Outer Layer Pair Spacing (edge to edge) (except as allowed below)	5.0 mils
Minimum Spacing to Other Signals	25 mils
Serpentine Spacing	25 mils
Maximum Via Count	5 (per side)
Series Termination Resistor Value	33 $\Omega \pm 5\%$
Shunt Termination Resistor Value	49.9 $\Omega \pm 1\%$
Trace Length Limits – L1 & L1'	Up to 500 mils
Trace Length Limits – L2 & L2'	Up to 200 mils
Trace Length Limits – L3 & L3'	Up to 500 mils
Trace Length Limits – L4 & L4'	2 to 8 inches
Total Length Range– L1 + L2 + L4	2 to 8.5 inches
Length Matching Required	Yes (Pin to Pad)
HCLK to HCLK# Length Matching	± 10 mils (per segment) ± 10 mils (overall)
Clock to Clock Length Matching	CPU HCLK = ITP HCLK = (MCH HCLK – 0.25 inch) Tolerance = ± 20 mils
Breakout Region Exceptions	No breakout exceptions allowed.

NOTES:

1. Route differential pairs as a closely coupled side-by-side pair on a single layer over their entire length.
2. To minimize skew it is recommended that all clocks be routed on a single layer. When clock pairs are to be routed on multiple layers, the routed length on each layer should be equalized across all clock pairs.
3. As specified in the table above, the nominal length of the clock pair terminating at the Intel® 82852GM GMCH should be routed 0.25 inch shorter than the other two clock pairs. This is to compensate for a difference in package length between the CPU and the GMCH.

13.2.1.1 Host Clock Group General Routing Guidelines

When routing the 100 MHz differential clocks, do not split up the two halves of a differential clock pair between layers, and route to all agents on the same physical routing layer referenced to ground.

If a layer transition is required, make sure that the skew induced by the vias used to transition between routing layers is compensated in the traces to other agents.

Do not place vias between adjacent complementary clock traces. Vias placed in one half of a differential pair must be matched by a via in the other half. Differential vias can be placed within length L1, between clock driver and Rs, if needed to shorten length L1.

13.2.1.2 Clock-to-Clock Length Matching and Compensation

The HCLK pairs to the CPU and GMCH should be matched as close as possible in total length from CK408 pin to the die-pad of the receiving device. In addition, the L1/L1' segments of all three clock pairs should be length matched to within ± 10 mils. Pair-to-pair overall length matching requires knowledge of the package lengths of various CPUs, and the GMCH, as well as the effective length of the CPU socket/interposer if used.

Once routing lengths are defined for the CPU and GMCH, match the PCB length of the ITP clock pair to the PCB length of the CPU clock pair.

Table 116 presents the clock package length.

Table 116. Clock Package Length

Parameter	Length
Mobile Intel Celeron Processor Package Length	596 mils
Intel® 852GM chipset GMCH Package Length	1142 mils
CPU Socket Equivalent Length	157 mils

13.2.1.3 EMI Constraints

Clocks are a significant contributor to EMI and should be treated with care. The following recommendations can aid in EMI reduction:

- Maintain uniform spacing between the two halves of differential clocks.
- Route clocks on physical layer adjacent to the VSS reference plane only.

13.2.2 CLK66 Clock Group

The 66 MHz clocks are series terminated and routed point-to-point on the PCB, with dedicated buffers for each of the loads. These clocks are all length tuned to match each other and the CLK33 clocks.

Figure 166 illustrates the CLK66 clock group topology.

Figure 166. CLK66 Clock Group Topology

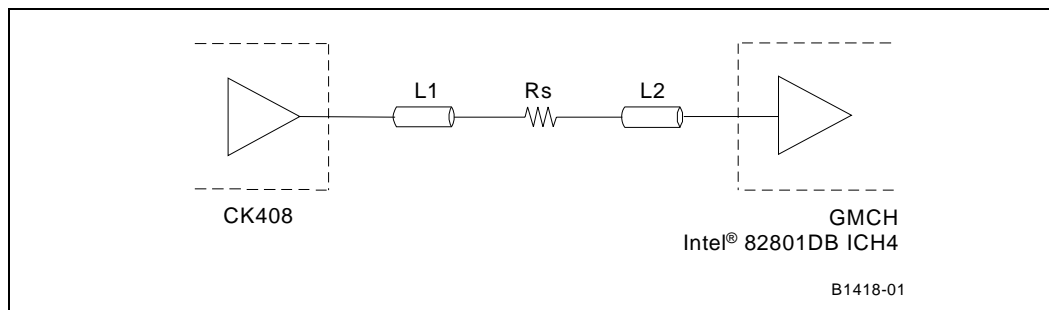


Table 117 presents the CLK66 clock group routing constraints.

Table 117. CLK66 Clock Group Routing Constraints (Sheet 1 of 2)

Parameter	Definition
Class Name	CLK66
Class Type	Individual Nets
Topology	Series Terminated Point to Point
Reference Plane	Ground Referenced
Single Ended Trace Impedance (Z_0)	$55 \Omega \pm 15\%$
Nominal Inner Layer Trace Width	4.0 mils
Nominal Outer Layer Trace Width	5.0 mils (pin escapes only)
Minimum Spacing (See exceptions below.)	20 mils
Serpentine Spacing	20 mils
Maximum Via Count	4 (per side)
Series Termination Resistor Value	$33 \Omega \pm 5\%$
Trace Length Limits – L1	Up to 500 mils (breakout segment)
Trace Length Limits – L2	4.0 inches to 8.5 inches
Total Length Range – L1 + L2	4.0 inches to 9.0 inches
Length Matching Required	Yes (Pin to Pin)
Clock to Clock Length Matching	± 100 mils CLK66 to CLK66

NOTE: The overall length of CLK66 is considered the reference length for all other clocks, except USBCLK and CLK14. The length of this clock should be set within the range and then used as the basis for defining the length of all other length matched clocks.

Table 117. CLK66 Clock Group Routing Constraints (Sheet 2 of 2)

Parameter	Definition
Breakout Region Exceptions. (Reduced spacing for GMCH & ICH breakout region)	5 mil trace with 5 mil space on outers 4 mil trace with 4 mil space in inners Maximum breakout length is 0.3 inch.

NOTE: The overall length of CLK66 is considered the reference length for all other clocks, except USBCLK and CLK14. The length of this clock should be set within the range and then used as the basis for defining the length of all other length matched clocks.

13.2.3 CLK33 Clock Group

The 33 MHz clocks are series terminated and routed point-to-point on the PCB with dedicated buffers for each of the loads. These clocks are length tuned to match the CLK66 clocks, however, they are out of phase due to an internal phase delay in the CK408.

Figure 167 illustrates the CLK33 group topology.

Figure 167. CLK33 Group Topology

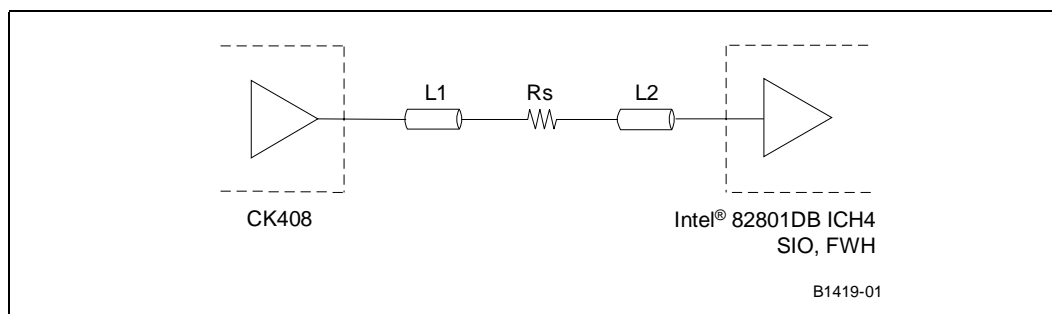


Table 118 presents the CLK33 clock group routing constraints.

Table 118. CLK33 Clock Group Routing Constraints (Sheet 1 of 2)

Parameter	Definition
Class Name	CLK33
Class Type	Individual Nets
Topology	Series Terminated Point-to-Point
Reference Plane	Ground Referenced
Single Ended Trace Impedance (Z_0)	$55 \Omega \pm 15\%$
Nominal Inner Layer Trace Width	4.0 mils
Nominal Outer Layer Trace Width	5.0 mils (pin escapes only)
Minimum Spacing (See exceptions below.)	20 mils
Serpentine Spacing	20 mils
Maximum Via Count	4
Series Termination Resistor Value	$33 \Omega \pm 5\%$
Trace Length Limits – L1	Up to 500 mils
Trace Length Limits – L2	4 to 8.5 inches

Table 118. CLK33 Clock Group Routing Constraints (Sheet 2 of 2)

Parameter	Definition
Total Length Range – L1 + L2	CLK66 Length
Length Matching Required	Yes (Pin to Pin)
Clock to Clock Matching	± 100 mils CLK33 to CLK33 to CLK66
Breakout Region Exceptions	5 mil trace with 5 mil space on outers 4 mil trace with 4 mil space in inners Maximum breakout length is 0.3 inch

13.2.4 PCI Clock Group

The PCI clocks are series terminated and routed point-to-point as on the PCB between the CK408 and the PCI connectors with dedicated buffers for of the three slots. These clocks are synchronous to the CLK33 clocks and are length tuned to compensate for the segment on the PCI daughtercard. Figure 168 illustrates the PCI clock group topology.

Figure 168. PCI Clock Group Topology

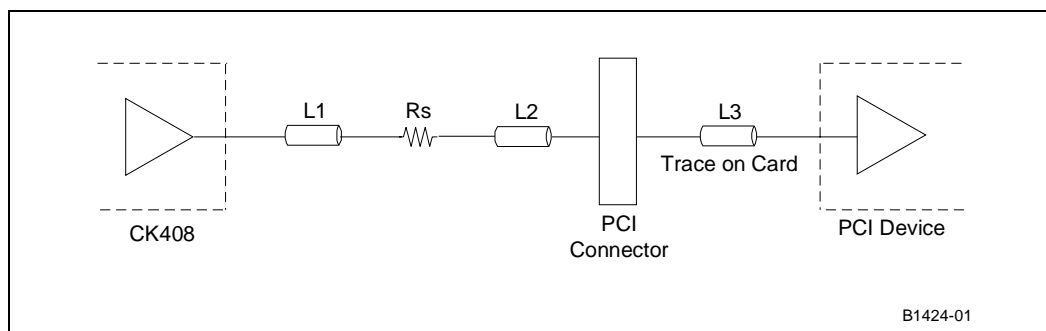


Table 119 presents the PCICLK clock group routing constraints.

Table 119. PCICLK Clock Group Routing Constraints (Sheet 1 of 2)

Parameter	Definition
Class Name	PCICLK
Class Type	Individual Nets
Topology	Series Terminated Point to Point
Reference Plane	Ground Referenced
Single Ended Trace Impedance (Z_0)	55 Ω ± 15%
Nominal Inner Layer Trace Width	4.0 mils
Nominal Outer Layer Trace Width	5.0 mils (pin escapes only)
Minimum Spacing (See exceptions below.)	20 mils
Serpentine Spacing	20 mils
Maximum Via Count	4
Series Termination Resistor Value	33 Ω ± 5%

Table 119. PCICLK Clock Group Routing Constraints (Sheet 2 of 2)

Parameter	Definition
Trace Length Limits – L1	Up to 500 mils (breakout segment)
Trace Length Limits – L2	1.5 to 8 inches
Trace Length Limits – L3	2.5 inches (as per PCI specification)
Total Length Range – L1 + L2 + L3	CLK33 – 2.5 inches (for nominal matching)
Length Matching Required	Yes (Pin to Pin)
Clock to Clock Length Matching	± 2 inches PCICLK to (CLK33 – 2.5 inches)
Breakout Region Exceptions	5 mil trace with 5 mil space on outers 4 mil trace with 4 mil space in inners Maximum breakout length is 0.3 inch

13.2.5 CLK14 Clock Group

The 14 MHz clocks are series terminated and routed point-to-point on the PCB. A single clock output is shared between the two loads. These clocks are length tuned to each other but are not synchronous with any other clocks.

Figure 169 illustrates the CLK14 clock group topology.

Figure 169. CLK14 Clock Group Topology

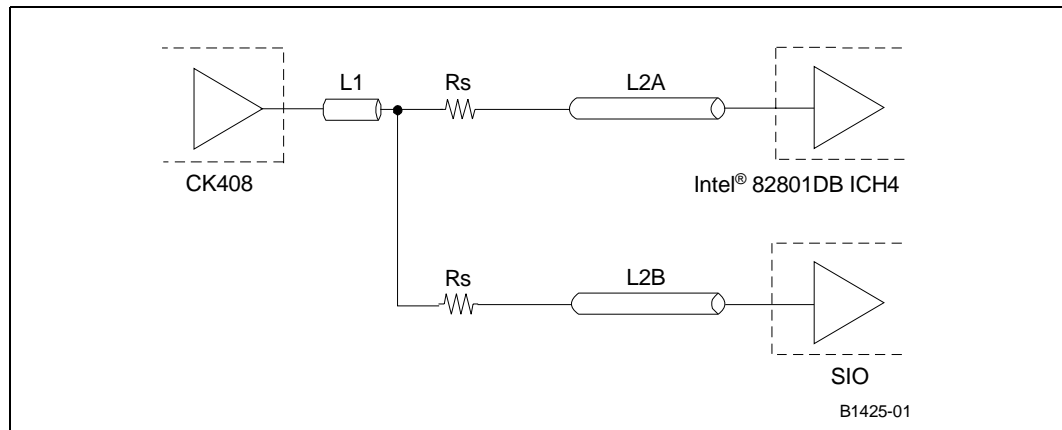


Table 120 presents the CLK14 clock group routing constraints.

Table 120. CLK14 Clock Group Routing Constraints (Sheet 1 of 2)

Parameter	Definition
Class Name	CLK14
Class Type	Individual Nets
Topology	Dual Series Terminated Point to Point
Reference Plane	Ground Referenced
Single Ended Trace Impedance (Zo)	55 Ω ± 15%

Table 120. CLK14 Clock Group Routing Constraints (Sheet 2 of 2)

Parameter	Definition
Nominal Inner Layer Trace Width	4.0 mils
Nominal Outer Layer Trace Width	5.0 mils (pin escapes only)
Minimum Spacing (See exceptions below.)	20 mils
Serpentine Spacing	20 mils
Maximum Via Count	4 (per driver/receiver path)
Series Termination Resistor Value	$33\ \Omega \pm 5\%$
Trace Length Limits – L1	Up to 500 mils
Trace Length Limits – L2A, L2B	2 to 8.5 inches
Total Length Range – L1 + L2A & L1 + L2B	2 to 9 inches
Length Matching Required	Yes (Pin to Pin)
Clock to Clock Length Matching	± 500 mils CLK14A to CLK14B
Breakout Region Exceptions	5 mil trace with 5 mil space on outers 4 mil trace with 4 mil space in inners Maximum breakout length is 0.3 inch

13.2.6 DOTCLK Clock Group

The 48 MHz DOTCLK is series terminated and routed point-to-point on the PCB. This clock operates independently and is not length-tuned to any other clock.

Figure 170 illustrates the DOTCLK clock topology.

Figure 170. DOTCLK Clock Topology

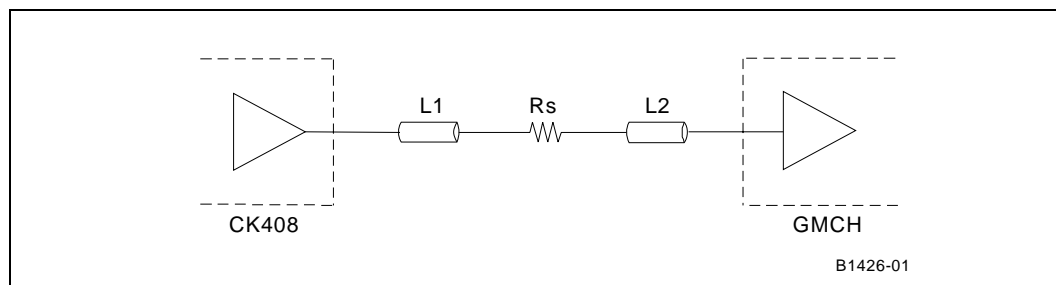


Table 121 presents the DOTCLK clock routing constraints.

Table 121. DOTCLK Clock Routing Constraints

Parameter	Definition
Class Name	DOTCLK
Class Type	Individual Net
Topology	Series Terminated Point to Point
Reference Plane	Ground Referenced
Single Ended Trace Impedance (Z_0)	$55 \Omega \pm 15\%$
Nominal Inner Layer Trace Width	4.0 mils
Nominal Outer Layer Trace Width	5.0 mils (pin escapes only)
Minimum Spacing (See exceptions below.)	25 mils
Maximum Via Count	4
Series Termination Resistor Value	$33 \Omega \pm 5\%$
Trace Length Limits – L1	Up to 500 mils
Trace Length Limits – L2	2 to 8 inches
Total Length Range – L1 + L2	2 to 8.5 inches
Length Matching Required	No
Breakout Exceptions	5 mil trace with 5 mil space on outers 4 mil trace with 4 mil space in inners Maximum breakout length is 0.3 inch

NOTE: The DOTCLK is used internally by the GMCH to generate the pixel clock and must exhibit very low jitter. Care should be taken to avoid routing through noisy areas and spacing rules should be observed. Guard traces may be employed if necessary with ground stake vias on no less than 0.5 inch intervals.

13.2.7 SSCCLK Clock Group

The 48/66 MHz SSCCLK operates independently and is not length tuned to any other clock. This clock employs a spread-spectrum device in its path to reduce EMI. The overall clock path is divided into two segments as shown in [Figure 171](#), with each segment series terminated and routed point-to-point.

Figure 171. SSCCLK Clock Topology

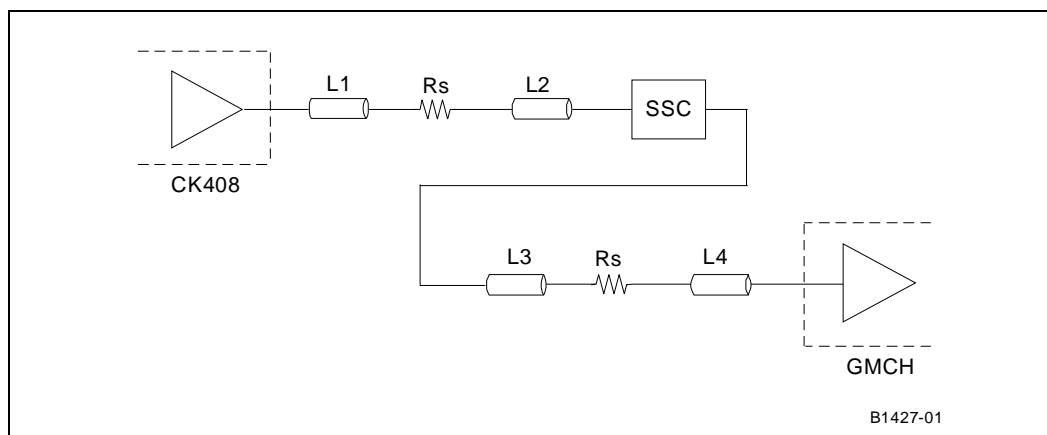


Table 122 presents the SSCCLK clock routing constraints.

Table 122. SSCCLK Clock Routing Constraints

Parameter	Definition
Class Name	SSCCLK
Class Type	Individual Net
Topology	Series Terminated Point to Point
Reference Plane	Ground Referenced
Single Ended Trace Impedance (Z_0)	$55 \Omega \pm 15\%$
Nominal Inner Layer Trace Width	4.0 mils
Nominal Outer Layer Trace Width	5.0 mils (pin escapes only)
Minimum Spacing (See exceptions below.)	20 mils
Maximum Via Count	4 (per driver/receiver path)
Series Termination Resistor Value	$33 \Omega \pm 5\%$
Trace Length Limits – L1	Up to 500 mils
Trace Length Limits – L2	1 to 4 inches
Trace Length Limits – L3	Up to 500 mils
Trace Length Limits – L4	1 to 7 inches
Total Length Range – $L1 + L2 + L3 + L4$	3 to 8.5 inches
Length Matching Required	No
Breakout Exceptions	5 mil trace with 5 mil space on outers 4 mil trace with 4 mil space in inners Maximum breakout length is 0.3 inch

13.2.8 USBCLK Clock Group

The 48 MHz USBCLK is series terminated and routed point-to-point on the PCB. This clock operates independently and is not length tuned to any other clock.

Figure 172 illustrates the USBCLK clock topology.

Figure 172. USBCLK Clock Topology

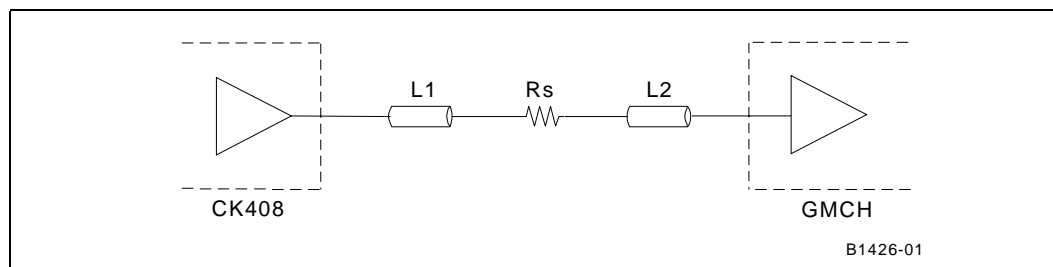


Table 123 presents the USBCLK clock routing constraints.

Table 123. USBCLK Clock Routing Constraints

Parameter	Definition
Class Name	USBCLK
Class Type	Individual Net
Topology	Series Terminated Point to Point
Reference Plane	Ground Referenced
Single Ended Trace Impedance (Z_0)	55 $\Omega \pm 15\%$
Nominal Inner Layer Trace Width	4.0 mils
Nominal Outer Layer Trace Width	5.0 mils (pin escapes only)
Minimum Spacing (See exceptions below.)	20 mils
Maximum Via Count	4
Series Termination Resistor Value	33 $\Omega \pm 5\%$
Trace Length Limits – L1	Up to 500 mils
Trace Length Limits – L2	3 to 12 inches
Total Length Range – L1 + L2	3 to 12.5 inches
Length Matching Required	No
Breakout Exceptions	5 mil trace with 5 mil space on outers 4 mil trace with 4 mil space in inners Maximum breakout length is 0.3 inch

13.3 CK-408 PWRDWN# Signal Connections

For systems that do not support S1M but do support the S3 state, the PWRDWN# input of the CK-408 clock chip should be connected to the SLP_S3# output of the ICH4. Intel **does not** recommend that PWRDWN# be pulled-up to the CK-408's 3.3 V power supply if the S3 state is the second highest, power consuming state supported by the platform (i.e., S1M and S2 not supported). The advantage of using SLP_S3# rather than the 3.3 V supply to qualify PWRDWN# is that it reduces the likelihood of the CK-408 clocks driving into unpowered components and potentially damaging the clock input buffers. SLP_S3# can help reduce power consumption because it is asserted before the 3.3 V supply is shut off, thus minimizing the amount of time that the clocks are left toggling.



Reserved, NC, and Test Signals

14

The processor and Intel 852GM GMCH may have signals listed as "RSVD", "NC", or other name whose functionality is Intel reserved. The following section contains recommendations on how these Intel reserved signals on the processor or GMCH should be handled.

14.1 Intel 852GM GMCH, NC, RSVD and Test Signals

The 852GM has a total of twelve NC and thirty two RSVD signals that are Intel reserved in the pin-map. The location of the Intel reserved signals in the pin-map for the 852GM are listed in [Table 124](#).

Table 124. Intel® 852GM RSVD and NC Signal Pin-Map Locations (Sheet 1 of 2)

Signal Name	Ball Name
NC	AJ29
NC	AH29
NC	B29
NC	A29
NC	AJ28
NC	A28
NC	AA9
NC	AJ4
NC	AJ2
NC	A2
NC	AH1
NC	B1
RSVD	AA22
RSVD	L2
RSVD	P3
RSVD	P4
RSVD	R3
RSVD	R5
RSVD	M1
RSVD	M5
RSVD	R6
RSVD	R4
RSVD	P6
RSVD	P5

Table 124. Intel® 852GM RSVD and NC Signal Pin-Map Locations (Sheet 2 of 2)

Signal Name	Ball Name
RSVD	N5
RSVD	P2
RSVD	N2
RSVD	N3
RSVD	M2
RSVD	T6
RSVD	T5
RSVD	F12
RSVD	D12
RSVD	B12
RSVD	AA5
RSVD	L4
RSVD	F3
RSVD	D3
RSVD	B3
RSVD	F2
RSVD	D2
RSVD	C2
RSVD	B2
RSVD	D7

14.2 Mobile Intel® Celeron® Processor NC, RSVD, and Test Signals

The Mobile Intel Celeron Processor has a total of eight NC and ten TESTHI signals that are Intel reserved in the pin-map. For connection recommendations on the TESTHI signals, refer to the latest Mobile Intel Celeron Processor Datasheet. All NC signals must remain unconnected. The location of the Intel reserved signals in the pin-map for the Mobile Intel Celeron Processor are listed in [Table 125](#).

Table 125. Mobile Intel® Celeron® Processor RSVD and NC Signal Pin-Map Locations (Sheet 1 of 2)

Signal Name	Ball Name
NC	A22
NC	A7
NC	AD2
NC	AD3

Table 125. Mobile Intel® Celeron® Processor RSVD and NC Signal Pin-Map Locations (Sheet 2 of 2)

Signal Name	Ball Name
NC	AE21
NC	AF3
NC	AF24
NC	AF25
TESTHI0	AD24
TESTHI1	AA2
TESTHI2	AC21
TESTHI3	AC20
TESTHI4	AC24
TESTHI5	AC23
TESTHI8	U6
TESTHI9	W4
TESTHI10	Y3
TESTHI11	A6

14.3 Intel® Celeron® Processor NC, RSVD, and Test Signals

The Intel Celeron Processor has a total of eight NC and eleven TESTHI signals that are Intel reserved in the pin-map. For connection recommendations on the TESTHI signals, refer to the latest Intel® Celeron Processor Datasheet. All NC signals must remain unconnected. The location of the Intel reserved signals in the pin-map for the Intel Celeron Processor are listed in [Table 126](#).

Table 126. Intel® Celeron® Processor RSVD and NC Signal Pin-Map Locations (Sheet 1 of 2)

Signal Name	Ball Name
NC	A22
NC	A7
NC	AD2
NC	AD3
NC	AE21
NC	AF3
NC	AF24
NC	AF25
TESTHI0	AD24
TESTHI1	AA2
TESTHI2	AC21

Table 126. Intel® Celeron® Processor RSVD and NC Signal Pin-Map Locations (Sheet 2 of 2)

Signal Name	Ball Name
TESTHI3	AC20
TESTHI4	AC24
TESTHI5	AC23
TESTHI8	U6
TESTHI9	W4
TESTHI10	Y3
TESTHI11	A6
TESTHI12	AD25

14.4 Intel® Celeron® M Processor NC, RSVD, and Test Signals

The Celeron M Processor has a total of six RSVD and three TESTHI signals that are Intel reserved in the pin-map. For connection recommendations on the TESTHI signals, refer to the latest Intel® Celeron® M Processor Datasheet. All other RSVD signals must remain unconnected but should have access to open routing channels for possible future use. The location of the Intel reserved signals in the pin-map for the Celeron M Processor are listed in [Table 127](#).

Table 127. Intel® Celeron M Processor RSVD and NC Signal Pin-Map Locations

Signal Name	Ball Name
RSVD	AF7
RSVD	B2
RSVD	C3
RSVD	E26
RSVD	G1
RSVD	AC1
TESTHI1	C5
TESTHI2	F23
TESTHI3	C16

Layout Checklist

15

This checklist selectively highlights some of the design considerations that should be reviewed prior to manufacturing Intel Celeron processor systems that implement the Intel® 852GM chipset. Items contained within the checklist attempt to address important connections to these devices and any critical supporting circuitry. **This is not a complete list, and it does not ensure that a design will function properly.** Refer to details in this document and the appended board schematics for complete design recommendations. The recommendations and considerations in this guide are subject to change.

The following recommendations are a summary of the information presented in this design guide. They are based on the example 8-layer stackup detailed in [Chapter 3](#). Deviation from the example stackup will require thorough signal integrity and timing simulations.

15.1 Processor Checklist for Intel Celeron Processor

Table 128. Intel Celeron Processor Layout Checklist (Sheet 1 of 4)

Checklist Items	Recommendations	Notes
Intel Celeron Processor Front Side Bus Interface Signals		
A[31:3]# ¹ ADSTB[1:0]# ² DSTBN[3:0]# ³ DSTBP[3:0]# ⁴ DBI[3:0]# D[63:0]# ⁵ REQ[4:0]# ⁶	<ul style="list-style-type: none"> Trace impedance = $55\ \Omega \pm 15\%$. Use strip-line routing, referencing ground planes above and below the signal layer. Route data strobes and data signals 4.5/11.5 with board trace length between 1.0 and 6.0 inches. Use GMCH die-pad to processor pin length for all length matching operations. Length match data strobes of the same group to within ± 25 mils of each other and to the average length of their associated data signal group. Route all data signals as groups, on the same layer, and balance within group ± 100 mils with respect to the associated strobes. Route address strobes 4.5/9 and address signals 4.5/9 with board trace length between 1.0 and 6.0 inches. The address signals within each group must be routed to within ± 200 mils of its associated strobe. 	<ul style="list-style-type: none"> AGTL+ Source Synchronous Signals. Refer to Section 4.4.2 for more information.
ADS# BNR# BR0# DBSY# DRDY# HIT# HITM# LOCK# BPRI# DEFER# RS[2:0]# TRDY# ⁸	<ul style="list-style-type: none"> Trace impedance = $55\ \Omega \pm 15\%$. Use strip-line routing, referencing solid ground planes. Route traces using 4.5/11.5 mils spacing with board trace length between 2.0 and 6.0 inches. Trace length matching is not required for common clock signals. Package length compensation is necessary in determining minimum board trace length. 	<ul style="list-style-type: none"> AGTL+ Common Clock Signals. Refer to Section 4.4.3 for more information.

NOTES:

1. A[31:3]# pins on the processor correspond to HA[31:3]# pins on the GMCH.
2. ADSTB[1:0]# pins on the processor correspond to HADSTB[1:0]# pins on the GMCH.
3. DSTBN[3:0]# pins on the processor correspond to HDSTBN[3:0]# pins on the GMCH.
4. DSTBP[3:0]# pins on the processor correspond to HDSTBP[3:0]# pins on the GMCH.
5. D[63:0]# pins on the processor correspond to HD[63:0]# pins on the GMCH.
6. REQ[4:0]# pins on the processor correspond to HREQ[4:0]# pins on the GMCH.
7. The RESET# pin on the processor corresponds to the CPURST# pin on the GMCH.
8. The TRDY# pin on the processor corresponds to the HTRDY# pin on the GMCH.

Table 128. Intel Celeron Processor Layout Checklist (Sheet 2 of 4)

Checklist Items	Recommendations	Notes
RESET# ⁷	When ITP Is Not Used <ul style="list-style-type: none"> Trace impedance = $55\ \Omega \pm 15\%$. Use strip-line routing, referencing solid ground planes. Route traces using 4.5/11.5 mils spacing with board trace length between 2.0 and 6.0 inches. Trace length matching is not required for common clock signals. Package length compensation is necessary in determining minimum board trace length. 	<ul style="list-style-type: none"> Refer to http://developer.intel.com/design/Xeon/guides/249679.htm for treatment of RESET# signal when implementing ITP700FLEX debug port. AGTL+ Common Clock Signal. Refer to Section 4.4.3 for more information.
IERR# FERR#	<ul style="list-style-type: none"> May be routed as a test point or to any optional system receiver. May be routed as strip-line or micro-strip with trace impedance = $55\ \Omega \pm 15\%$. Place pull-up resistor Rpu within three inches of the Intel® 82801DB I/O Controller Hub 4 (ICH4). Pull-up voltage for termination resistor Rpu is VCC_CPU. 	<ul style="list-style-type: none"> Asynchronous AGTL+ Output Signal. Refer to Topology 1A in Section 4.4.4.1 for resistor values and trace length recommendations.
PROCHOT#	<ul style="list-style-type: none"> May be routed as strip-line or micro-strip with trace impedance = $55\ \Omega \pm 15\%$. Use recommended voltage translation logic for an appropriate system receiver. Pull-up voltage for termination resistor Rpu is VCC_CPU 	<ul style="list-style-type: none"> Asynchronous AGTL+ Output Signal. Refer to Topology 1B in Section 4.4.4.2 for resistor values and trace length recommendations.
THERMTRIP#	<ul style="list-style-type: none"> Recommend connecting processor signal THERMTRIP# to the ICH4, but may be connected to any optional system receiver, with consideration for any voltage level translation if necessary. May be routed as strip-line or micro-strip with trace impedance = $55\ \Omega \pm 15\%$. Place pull-up resistor Rpu within three inches of ICH4. Pull-up voltage for termination resistor Rpu is VCC_CPU. 	<ul style="list-style-type: none"> Asynchronous AGTL+ Output Signals. Refer to Topology 1C in Section 4.4.4.3 for resistor values and trace length recommendations.

NOTES:

- A[31:3]# pins on the processor correspond to HA[31:3]# pins on the GMCH.
- ADSTB[1:0]# pins on the processor correspond to HADSTB[1:0]# pins on the GMCH.
- DSTBN[3:0]# pins on the processor correspond to HDSTBN[3:0]# pins on the GMCH.
- DSTBP[3:0]# pins on the processor correspond to HDSTBP[3:0]# pins on the GMCH.
- D[63:0]# pins on the processor correspond to HD[63:0]# pins on the GMCH.
- REQ[4:0]# pins on the processor correspond to HREQ[4:0]# pins on the GMCH.
- The RESET# pin on the processor corresponds to the CPURST# pin on the GMCH.
- The TRDY# pin on the processor corresponds to the HTRDY# pin on the GMCH.

Table 128. Intel Celeron Processor Layout Checklist (Sheet 3 of 4)

Checklist Items	Recommendations	Notes
PWRGOOD	<ul style="list-style-type: none"> May be routed as strip-line or micro-strip with trace impedance = $55\ \Omega \pm 15\%$. Route point-to-point between the ICH4 signal CPUPWRGD and CPU signal PWRGOOD, trace length range between 1.0 and 12 inches. Place a termination resistor Rpu within three inches of CPU pin. T-split routing should not be used. Pull-up voltage for termination resistor Rpu is VCC_CPU. 	<ul style="list-style-type: none"> Asynchronous Open Drain CMOS Input Signal. Refer to Topology 2C in Section 4.4.4.6 for resistor values and detailed routing recommendations.
IGNNE# LINT0/INTR LINT1/NMI SMI# SLP# A20M# STPCLK#	<ul style="list-style-type: none"> May be routed as strip-line or micro-strip with trace impedance = $55\ \Omega \pm 15\%$. Implement a point-to-point connection between the ICH4 and CPU, trace length range between 0.5 and 12 inches. No additional components are necessary for this topology. 	<ul style="list-style-type: none"> Asynchronous GTL+ Input Signals. Refer to Topology 2A in Section 4.4.4.4.
INIT#	<ul style="list-style-type: none"> May be routed as strip-line or micro-strip with trace impedance = $55\ \Omega \pm 15\%$. Route signal point-to-point between the ICH4 and CPU, trace length range max 17 inches. Voltage level translation is required from the ICH4 INIT# pin to FWH. 	<ul style="list-style-type: none"> Asynchronous GTL+ Input Signal. Refer to Topology 2B in Section 4.4.4.5 for resistor values and trace length recommendations. The Intel board makes use of an optional alternative circuit for FWH voltage translation. Refer to schematic appendix.
Other Signals		
BCLK, BCLK#	CPU BCLK, BCLK# from CK-408 should be routed as differential pairs and length matched to the GMCH BCLK, BCLK# signals.	<ul style="list-style-type: none"> Refer to host clock group routing guidelines detailed in Section 13.2.1. Refer to Chapter 13 for detailed breakdown of all system clock routing recommendations.
COMP[0,1]	Terminate each signal to ground with $51.1\ \Omega \pm 1\%$ resistors.	<ul style="list-style-type: none"> Refer to Section 4.4.4.9 for detailed layout recommendations.
Processor Decoupling, VREF and Filtering		

NOTES:

- A[31:3]# pins on the processor correspond to HA[31:3]# pins on the GMCH.
- ADSTB[1:0]# pins on the processor correspond to HADSTB[1:0]# pins on the GMCH.
- DSTBN[3:0]# pins on the processor correspond to HDSTBN[3:0]# pins on the GMCH.
- DSTBP[3:0]# pins on the processor correspond to HDSTBP[3:0]# pins on the GMCH.
- D[63:0]# pins on the processor correspond to HD[63:0]# pins on the GMCH.
- REQ[4:0]# pins on the processor correspond to HREQ[4:0]# pins on the GMCH.
- The RESET# pin on the processor corresponds to the CPURST# pin on the GMCH.
- The TRDY# pin on the processor corresponds to the HTRDY# pin on the GMCH.

Table 128. Intel Celeron Processor Layout Checklist (Sheet 4 of 4)

Checklist Items	Recommendations	Notes
GTLREF	<ul style="list-style-type: none"> Connect CPU GTLREF pin to a $49.9\ \Omega \pm 1\%$ and $100\ \Omega \pm 1\%$ resistive divider to VCC_CPU. Connect voltage divider node to CPU GTLREF pin with a $Z_0 = 55\ \Omega$ trace that is shorter than 1.5 inch. Minimum separation from other switching signals should be 10 mils. 	Refer to Section 4.2 for more information.
VCC_CPU Decoupling	<p>Recommended bulk decoupling:</p> <ul style="list-style-type: none"> (10) 560μF Al POLYMER - ESR 5 mΩ (typ) and ESL 4.0 nH, placed one each near the CPU and the GMCH packages. (40) 22μF X5R 0603 caps - ESR 3.5 mΩ (typ) and ESL 1.4 nH, placed on the secondary side within the CPU package outline. (4) 1200μF AL Electrolytic 16V 2.1 A ripple caps - ESR 22 mΩ and ESL 30 nH (4) 1206 pkg 4.7μF - ESR 6 mΩ and ESL 1.1 nH 	Refer to Section 7.4.7 for processor VCCP decoupling recommendations.

NOTES:

- A[31:3]# pins on the processor correspond to HA[31:3]# pins on the GMCH.
- ADSTB[1:0]# pins on the processor correspond to HADSTB[1:0]# pins on the GMCH.
- DSTBN[3:0]# pins on the processor correspond to HDSTBN[3:0]# pins on the GMCH.
- DSTBP[3:0]# pins on the processor correspond to HDSTBP[3:0]# pins on the GMCH.
- D[63:0]# pins on the processor correspond to HD[63:0]# pins on the GMCH.
- REQ[4:0]# pins on the processor correspond to HREQ[4:0]# pins on the GMCH.
- The RESET# pin on the processor corresponds to the CPURST# pin on the GMCH.
- The TRDY# pin on the processor corresponds to the HTRDY# pin on the GMCH.

15.2 Processor Checklist for Mobile Intel Celeron Processor

Table 129. Mobile Intel Celeron Processor Layout Checklist (Sheet 1 of 4)

Checklist Items	Recommendations	Notes
Intel Celeron Processor Front Side Bus Interface Signals		
A[31:3]# ¹ ADSTB[1:0]# ² DSTBN[3:0]# ³ DSTBP[3:0]# ⁴ DBI[3:0]# D[63:0]# ⁵ REQ[4:0]# ⁶	<ul style="list-style-type: none"> Trace impedance = $55 \Omega \pm 15\%$. Use strip-line routing, referencing ground planes above and below the signal layer. Route data strobes and data signals 4/12 with board trace length between 0.5 and 5.5 inches. Use GMCH die-pad to processor pin length for all length matching operations. Length match data strobes of the same group to within ± 25 mils of each other and to the average length of their associated data signal group. Route all data signals as groups, on the same layer, and balance within group ± 100 mils with respect to the associated strobes. Route address strobes 4/8 and address signals 4/8 with board trace length between 0.5 and 6.5 inches. The address signals within each group must be routed to within ± 200 mils of its associated strobe. 	<ul style="list-style-type: none"> AGTL+ Source Synchronous Signals. Refer to Section 5.3.1 for more information.
ADS# BNR# BR0# DBSY# DRDY# HIT# HITM# LOCK# BPRI# DEFER# RS[2:0]# TRDY# ⁸	<ul style="list-style-type: none"> Trace impedance = $55 \Omega \pm 15\%$. Use strip-line routing, referencing solid ground planes. Route traces using 4/8 mils spacing with board trace length between 0.5 and 6.5 inches. Trace length matching is not required for common clock signals. Package length compensation is necessary in determining minimum board trace length. 	<ul style="list-style-type: none"> AGTL+ Common Clock Signals. Refer to Section 5.3.3 for more information.

NOTES:

1. A[31:3]# pins on the processor correspond to HA[31:3]# pins on the GMCH.
2. ADSTB[1:0]# pins on the processor correspond to HADSTB[1:0]# pins on the GMCH.
3. DSTBN[3:0]# pins on the processor correspond to HDSTBN[3:0]# pins on the GMCH.
4. DSTBP[3:0]# pins on the processor correspond to HDSTBP[3:0]# pins on the GMCH.
5. D[63:0]# pins on the processor correspond to HD[63:0]# pins on the GMCH.
6. REQ[4:0]# pins on the processor correspond to HREQ[4:0]# pins on the GMCH.
7. The RESET# pin on the processor corresponds to the CPURST# pin on the GMCH.
8. The TRDY# pin on the processor corresponds to the HTRDY# pin on the GMCH.

Table 129. Mobile Intel Celeron Processor Layout Checklist (Sheet 2 of 4)

Checklist Items	Recommendations	Notes
RESET# ⁷	When ITP Is Not Used <ul style="list-style-type: none"> Trace impedance = $55\ \Omega \pm 15\%$. Use strip-line routing, referencing solid ground planes. Route traces using 4/8 mils spacing with board trace length between 0.5 and 6.5 inches. Trace length matching is not required for common clock signals. Package length compensation is necessary in determining minimum board trace length. 	<ul style="list-style-type: none"> Refer to http://developer.intel.com/design/Xeon/guides/249679.htm for treatment of RESET# signal when implementing ITP700FLEX debug port. AGTL+ Common Clock Signal. Refer to Section 5.3.3 for more information.
IERR# FERR#	<ul style="list-style-type: none"> May be routed as a test point or to any optional system receiver. May be routed as strip-line or micro-strip with trace impedance = $55\ \Omega \pm 15\%$. Place pull-up resistor Rpu within three inches of the Intel® 82801DB I/O Controller Hub 4 (ICH4). Pull-up voltage for termination resistor Rpu is VCCP. 	<ul style="list-style-type: none"> Asynchronous AGTL+ Output Signal. Refer to Topology 1A in Section 5.3.4.1 for resistor values and trace length recommendations.
PROCHOT#	<ul style="list-style-type: none"> May be routed as strip-line or micro-strip with trace impedance = $55\ \Omega \pm 15\%$. Use recommended voltage translation logic for an appropriate system receiver. Pull-up voltage for termination resistor Rpu is VCCP. 	<ul style="list-style-type: none"> Asynchronous AGTL+ Output Signal. Refer to Topology 1C in Section 5.3.4.3 for resistor values and trace length recommendations.
THERMTRIP#	<ul style="list-style-type: none"> Recommend connecting processor signal THERMTRIP# to the ICH4, but may be connected to any optional system receiver, with consideration for any voltage level translation if necessary. May be routed as strip-line or micro-strip with trace impedance = $55\ \Omega \pm 15\%$. Place pull-up resistor Rpu within three inches of ICH4. Pull-up voltage for termination resistor Rpu is VCCP. 	<ul style="list-style-type: none"> Asynchronous AGTL+ Output Signals. Refer to Topology 1B in Section 5.3.4.2 for resistor values and trace length recommendations.

NOTES:

- A[31:3]# pins on the processor correspond to HA[31:3]# pins on the GMCH.
- ADSTB[1:0]# pins on the processor correspond to HADSTB[1:0]# pins on the GMCH.
- DSTBN[3:0]# pins on the processor correspond to HDSTBN[3:0]# pins on the GMCH.
- DSTBP[3:0]# pins on the processor correspond to HDSTBP[3:0]# pins on the GMCH.
- D[63:0]# pins on the processor correspond to HD[63:0]# pins on the GMCH.
- REQ[4:0]# pins on the processor correspond to HREQ[4:0]# pins on the GMCH.
- The RESET# pin on the processor corresponds to the CPURST# pin on the GMCH.
- The TRDY# pin on the processor corresponds to the HTRDY# pin on the GMCH.

Table 129. Mobile Intel Celeron Processor Layout Checklist (Sheet 3 of 4)

Checklist Items	Recommendations	Notes
PWRGOOD	<ul style="list-style-type: none"> May be routed as strip-line or micro-strip with trace impedance = $55\ \Omega \pm 15\%$. Route point-to-point between the ICH4 signal CPUPWRGD and CPU signal PWRGOOD, trace length range between 0.5 and 12 inches. Place a termination resistor Rpu within three inches of CPU pin. T-split routing should not be used. Pull-up voltage for termination resistor Rpu is VCC_CPU. 	<ul style="list-style-type: none"> Asynchronous Open Drain CMOS Input Signal. Refer to Topology 2A in Section 5.3.4.4 for resistor values and detailed routing recommendations.
IGNNE# LINT0/INTR LINT1/NMI SMI# SLP# A20M# STPCLK#	<ul style="list-style-type: none"> May be routed as strip-line or micro-strip with trace impedance = $55\ \Omega \pm 15\%$. Implement a point-to-point connection between the ICH4 and CPU, trace length range between 0.5 and 12 inches. No additional components are necessary for this topology. 	<ul style="list-style-type: none"> Asynchronous GTL+ Input Signals. Refer to Topology 2B in Section 5.3.4.5.
INIT#	<ul style="list-style-type: none"> May be routed as strip-line or micro-strip with trace impedance = $55\ \Omega \pm 15\%$. Route signal point-to-point between the ICH4 and CPU, trace length range max 12 inches. Voltage level translation is required from the ICH4 INIT# pin to FWH. 	<ul style="list-style-type: none"> Asynchronous CMOS Input Signal. Refer to Topology 2C in Section 5.3.4.6 for resistor values and trace length recommendations. The Intel board makes use of an optional alternative circuit for FWH voltage translation. Refer to schematic appendix.
Other Signals		
BCLK, BCLK#	CPU BCLK, BCLK# from CK-408 should be routed as differential pairs and length matched to the GMCH BCLK, BCLK# signals.	<ul style="list-style-type: none"> Refer to host clock group routing guidelines detailed in Section 13.2.1. Refer to Chapter 13 for detailed breakdown of all system clock routing recommendations.
COMP[0,1]	Terminate each signal to ground with $51\ \Omega \pm 1\%$ resistors.	<ul style="list-style-type: none"> Refer to Section 5.3.4.7 for detailed layout recommendations.
Processor Decoupling, VREF and Filtering		

NOTES:

- A[31:3]# pins on the processor correspond to HA[31:3]# pins on the GMCH.
- ADSTB[1:0]# pins on the processor correspond to HADSTB[1:0]# pins on the GMCH.
- DSTBN[3:0]# pins on the processor correspond to HDSTBN[3:0]# pins on the GMCH.
- DSTBP[3:0]# pins on the processor correspond to HDSTBP[3:0]# pins on the GMCH.
- D[63:0]# pins on the processor correspond to HD[63:0]# pins on the GMCH.
- REQ[4:0]# pins on the processor correspond to HREQ[4:0]# pins on the GMCH.
- The RESET# pin on the processor corresponds to the CPURST# pin on the GMCH.
- The TRDY# pin on the processor corresponds to the HTRDY# pin on the GMCH.

Table 129. Mobile Intel Celeron Processor Layout Checklist (Sheet 4 of 4)

Checklist Items	Recommendations	Notes
GTLREF	<ul style="list-style-type: none"> Connect CPU GTLREF pin to a $49.9\ \Omega \pm 1\%$ and $100\ \Omega \pm 1\%$ resistive divider to VCC_CPU. Connect voltage divider node to CPU GTLREF pin with a $Z_0 = 55\ \Omega$ trace that is shorter than 1.5 inch. Minimum separation from other switching signals should be 10 mils. 	Refer to Section 5.5.1 for more information.
VCC_CPU Decoupling	<p>Recommended bulk decoupling:</p> <ul style="list-style-type: none"> (10) 560μF AI POLYMER - ESR 5 mΩ (typ) and ESL 4.0 nH, placed one each near the CPU and the GMCH packages. (40) 22μF X5R 0603 caps - ESR 3.5 mΩ (typ) and ESL 1.4 nH, placed on the secondary side within the CPU package outline. (4) 1200μF AL Electrolytic 16V 2.1 A ripple caps - ESR 22 mΩ and ESL 30 nH (4) 1206 pkg 4.7μF - ESR 6 mΩ and ESL 1.1 nH 	Refer to Section 7.4.7 for processor VCCP decoupling recommendations.

NOTES:

- A[31:3]# pins on the processor correspond to HA[31:3]# pins on the GMCH.
- ADSTB[1:0]# pins on the processor correspond to HADSTB[1:0]# pins on the GMCH.
- DSTBN[3:0]# pins on the processor correspond to HDSTBN[3:0]# pins on the GMCH.
- DSTBP[3:0]# pins on the processor correspond to HDSTBP[3:0]# pins on the GMCH.
- D[63:0]# pins on the processor correspond to HD[63:0]# pins on the GMCH.
- REQ[4:0]# pins on the processor correspond to HREQ[4:0]# pins on the GMCH.
- The RESET# pin on the processor corresponds to the CPURST# pin on the GMCH.
- The TRDY# pin on the processor corresponds to the HTRDY# pin on the GMCH.

15.3 Checklist for the Intel® Celeron® M Processor

Table 130. Processor Layout Checklist for the Intel® Celeron® M Processor (Sheet 1 of 5)

Checklist Items	Recommendations	Comments
Intel Celeron M FSB Interface Signals		
A[31:3]# ¹ ADSTB[1:0]# ² DSTBN[3:0]# ³ DSTBP[3:0]# ⁴ DINV[3:0]# D[63:0]# ⁵ REQ[4:0]# ⁶	<ul style="list-style-type: none"> Trace impedance = $55 \Omega \pm 15\%$. Use stripline routing, referencing ground planes above and below the signal layer. Route data strobes and data signals 3:1 with board trace length between 0.5 and 5.5 inches total trace length including package compensation. Use GMCH die-pad to processor pin length for all length matching operations. Length match data strobes of the same group to within ± 25 mils of each other and to the average length of their associated data signal group. Route all data signals as groups, on the same layer, and balance within group ± 100 mils with respect to the associated strobes. Route address strobes 4/12 and address signals 4/8 with board trace length between 0.5 and 6.5 inches total trace length including package compensation. Trace length match address strobes to ± 200 mils of average length of their associated address signals group. 	<ul style="list-style-type: none"> AGTL+ Source Synchronous Signals. Refer to Section 6.1.3 for more information.
ADS# BNR# BR0# DBSY# DRDY# HIT# HITM# LOCK# DPWR# BPR# DEFER# RS[2:0]# TRDY# ⁸	<ul style="list-style-type: none"> Trace impedance = $55 \Omega \pm 15\%$. Use stripline routing, referencing solid ground planes. Route traces using 2:1 mils spacing with maximum board trace length of 6.5 inches. Trace length matching is not required for common clock signals. Package length compensation is necessary in determining minimum board trace length. 	<ul style="list-style-type: none"> AGTL+ Common Clock Signals. Refer to Section 6.1.2 for more information.

NOTES:

- A[31:3]# pins on the processor correspond to HA[31:3]# pins on the GMCH.
- ADSTB[1:0]# pins on the processor correspond to HADSTB[1:0]# pins on the GMCH.
- DSTBN[3:0]# pins on the processor correspond to HDSTBN[3:0]# pins on the GMCH.
- DSTBP[3:0]# pins on the processor correspond to HDSTBP[3:0]# pins on the GMCH.
- D[63:0]# pins on the processor correspond to HD[63:0]# pins on the GMCH.
- REQ[4:0]# pins on the processor correspond to HREQ[4:0]# pins on the GMCH.
- The RESET# pin on the processor corresponds to the CPURST# pin on the GMCH. Refer to the ITP portion of this checklist, [Section 6.1.5](#) for treatment of RESET# when using ITP700FLEX debug port.
- The TRDY# pin on the processor corresponds to the HTRDY# pin on the GMCH.

Table 130. Processor Layout Checklist for the Intel® Celeron® M Processor (Sheet 2 of 5)

Checklist Items	Recommendations	Comments
RESET# ⁷	<ul style="list-style-type: none"> • When ITP700 Is Not Used: • Trace impedance = $55\ \Omega \pm 15\%$. • Use stripline routing, referencing solid ground planes. • Route traces using 2:1 mils spacing with board trace length between 1101 mils and 6.5 inches. • Trace length matching is not required for common clock signals. • Package length compensation is necessary in determining minimum board trace length. 	<ul style="list-style-type: none"> • Refer to http://developer.intel.com/design/Xeon/guides/249679.htm for treatment of RESET# signal when implementing ITP700FLEX debug port. • AGTL+ Common Clock Signal. • Refer to Section 6.1.5 for more information.
Intel® 82801DB I/O Controller Hub (ICH4) Interface Signals		
IERR#	<ul style="list-style-type: none"> • May be routed as a test point or to any optional system receiver. • May be routed as stripline or microstrip with trace impedance = $55\ \Omega \pm 15\%$. • Place series resistor R1 within three inches of system receiver. • Place pull-up resistor Rtt within three inches of series resistor R1. • Pull-up voltage for termination resistor Rtt is V_{CCP} (1.05). 	<ul style="list-style-type: none"> • Asynchronous AGTL+ Output Signal. • Refer to Topology 1A in Section 6.1.4.1 for resistor values and trace length recommendations.
PROCHOT#	<ul style="list-style-type: none"> • May be routed as stripline or microstrip with trace impedance = $55\ \Omega \pm 15\%$. • Use Intel's recommended voltage translation logic for an appropriate system receiver. • Pull-up voltage for termination resistor Rtt is V_{CCP} (1.05) • Place series resistor Rs at the beginning of trace T-split and within three inches from Q1. 	<ul style="list-style-type: none"> • Asynchronous AGTL+ Output Signal. • Refer to Topology 1C in Section 6.1.4.3 for resistor values and trace length recommendations.

NOTES:

1. A[31:3]# pins on the processor correspond to HA[31:3]# pins on the GMCH.
2. ADSTB[1:0]# pins on the processor correspond to HADSTB[1:0]# pins on the GMCH.
3. DSTBN[3:0]# pins on the processor correspond to HDSTBN[3:0]# pins on the GMCH.
4. DSTBP[3:0]# pins on the processor correspond to HDSTBP[3:0]# pins on the GMCH.
5. D[63:0]# pins on the processor correspond to HD[63:0]# pins on the GMCH.
6. REQ[4:0]# pins on the processor correspond to HREQ[4:0]# pins on the GMCH.
7. The RESET# pin on the processor corresponds to the CPURST# pin on the GMCH. Refer to the ITP portion of this checklist, [Section 6.1.5](#) for treatment of RESET# when using ITP700FLEX debug port.
8. The TRDY# pin on the processor corresponds to the HTRDY# pin on the GMCH.

Table 130. Processor Layout Checklist for the Intel® Celeron® M Processor (Sheet 3 of 5)

Checklist Items	Recommendations	Comments
FERR# THERMTRIP#	<ul style="list-style-type: none"> Connect FERR# to the processor and the Intel® 82801DB I/O Controller Hub 4 (ICH4). Recommend connecting processor signal THERMTRIP# to the ICH4, but may be connected to any optional system receiver, with consideration for any voltage level translation if necessary. May be routed as stripline or microstrip with trace impedance = $55\ \Omega \pm 15\%$. Place series resistor R1 within three inches of system receiver. Place pull-up resistor Rtt within three inches of series resistor R1. Pull-up voltage for termination resistor Rtt is V_{CCP} (1.05). 	<ul style="list-style-type: none"> Asynchronous AGTL+ Output Signals. Refer to Topology 1B in Section 6.1.4.2 for resistor values and trace length recommendations. Refer to Section 6.1.4.7 for voltage translation recommendations.
PWRGOOD	<ul style="list-style-type: none"> May be routed as stripline or microstrip with trace impedance = $55\ \Omega \pm 15\%$ Route point-to-point between the ICH4 signal CPUPWRGD and CPU signal PWRGOOD, trace length range between 0.5 and 12 inches. Place a termination resistor Rtt within three inches of CPU pin. T-split routing should not be used. Pull-up voltage for termination resistor Rtt is V_{CCP} (1.05) 	<ul style="list-style-type: none"> Asynchronous Open Drain CMOS Input Signal. Refer to Topology 2A in Section 6.1.4.4 for resistor values and detailed routing recommendations.
IGNNE# LINT0/INTR LINT1/NMI SMI# SLP# A20M# STPCLK#	<ul style="list-style-type: none"> May be routed as stripline or microstrip with trace impedance = $55\ \Omega \pm 15\%$. Implement a point-to-point connection between the ICH4 and CPU, trace length range between 0.5 and 12 inches. No additional components are necessary for this topology. 	<ul style="list-style-type: none"> Asynchronous CMOS Input Signals. Refer to Topology 2B in Section 6.1.4.5.

NOTES:

1. A[31:3]# pins on the processor correspond to HA[31:3]# pins on the GMCH.
2. ADSTB[1:0]# pins on the processor correspond to HADSTB[1:0]# pins on the GMCH.
3. DSTBN[3:0]# pins on the processor correspond to HDSTBN[3:0]# pins on the GMCH.
4. DSTBP[3:0]# pins on the processor correspond to HDSTBP[3:0]# pins on the GMCH.
5. D[63:0]# pins on the processor correspond to HD[63:0]# pins on the GMCH.
6. REQ[4:0]# pins on the processor correspond to HREQ[4:0]# pins on the GMCH.
7. The RESET# pin on the processor corresponds to the CPURST# pin on the GMCH. Refer to the ITP portion of this checklist, [Section 6.1.5](#) for treatment of RESET# when using ITP700FLEX debug port.
8. The TRDY# pin on the processor corresponds to the HTRDY# pin on the GMCH.

Table 130. Processor Layout Checklist for the Intel® Celeron® M Processor (Sheet 4 of 5)

Checklist Items	Recommendations	Comments
INIT#	<ul style="list-style-type: none"> May be routed as stripline or microstrip with trace impedance = $55\ \Omega \pm 15\%$. Route signal point-to-point between the ICH4 and CPU, trace length range between 0.5 and 12 inches. Voltage level translation is required from the ICH4 INIT# pin to FWH. Place series resistor R_s at the beginning of trace T-split and within three inches from Q1. 	<ul style="list-style-type: none"> Asynchronous CMOS Input Signal. Refer to Topology 3 in Section 6.1.4.6 for resistor values and trace length recommendations. Refer also to Section 6.1.4.7 for more details on voltage translation recommendations. The Intel customer reference board makes use of an optional alternative circuit for FWH voltage translation. Refer to schematic appendix.
Other Signals		
BCLK, BCLK#	<ul style="list-style-type: none"> CPU BCLK, BCLK# from CK-408 should be routed as differential pairs and length matched to the GMCH BCLK, BCLK# signals. 	<ul style="list-style-type: none"> Refer to host clock group routing guidelines detailed in Section 13.2.1. Refer to Chapter 13 for detailed breakdown of all system clock routing recommendations.
COMP[0,2]	<ul style="list-style-type: none"> Terminate each signal to ground with $27.4\ \Omega \pm 1\%$ resistors. Connect each to CPU with a $Z_o = 27.4\ \Omega$ trace that is less than 0.5 inch from the pin. Spacing from other switching signal traces should be a minimum of 25 mils. 	<ul style="list-style-type: none"> Refer to Section 6.1.8.1 for detailed layout recommendations.
COMP[1,3]	<ul style="list-style-type: none"> Terminate each signal to ground with $54.9\ \Omega \pm 1\%$ resistors. Connect each to CPU with a $Z_o = 55\ \Omega$ trace that is less than 0.5 inch from the pin. Spacing from other switching signal traces should be a minimum of 25 mils. 	Refer to Section 6.1.8.1 for detailed layout recommendations.
Processor Power and GND Measurement/Sense Signals		
V _{CCSENSE} V _{SSSENSE}	<ul style="list-style-type: none"> Route traces of equal length using 3:1 spacing, $Z_o = 55\ \Omega \pm 15\%$. Place via next to the processor socket's pin for measurement of CPU_VCC/V_{SS}. Place a ground via 100 mils from each test point via. 	Refer to Section 6.1.10 for more information.
Processor Decoupling, VREF, and Filtering		

NOTES:

- A[31:3]# pins on the processor correspond to HA[31:3]# pins on the GMCH.
- ADSTB[1:0]# pins on the processor correspond to HADSTB[1:0]# pins on the GMCH.
- DSTBN[3:0]# pins on the processor correspond to HDSTBN[3:0]# pins on the GMCH.
- DSTBP[3:0]# pins on the processor correspond to HDSTBP[3:0]# pins on the GMCH.
- D[63:0]# pins on the processor correspond to HD[63:0]# pins on the GMCH.
- REQ[4:0]# pins on the processor correspond to HREQ[4:0]# pins on the GMCH.
- The RESET# pin on the processor corresponds to the CPURST# pin on the GMCH. Refer to the ITP portion of this checklist, [Section 6.1.5](#) for treatment of RESET# when using ITP700FLEX debug port.
- The TRDY# pin on the processor corresponds to the HTRDY# pin on the GMCH.

Table 130. Processor Layout Checklist for the Intel® Celeron® M Processor (Sheet 5 of 5)

Checklist Items	Recommendations	Comments
GTLREF	<ul style="list-style-type: none"> Connect CPU GTLREF pin to a 1 K $\Omega \pm 1\%$ and 2 K $\Omega \pm 1\%$ resistive divider to V_{CCP}. No decoupling on this signal. Connect voltage divider node to CPU GTLREF pin with a $Z_0 = 55 \Omega$ trace that is shorter than 0.5 inch. Minimum separation from other switching signals should be 25 mils. 	Refer to Section 6.1.7 for more information.
V_{CC} (CORE) Decoupling	<p>Intel recommends bulk decoupling:</p> <ul style="list-style-type: none"> (4) 220 μF SP caps - ESR 12 mΩ (max) and ESL 3.5 μH, placed near CPU north power corridor (pin map row AF). <p>Intel recommends mid-frequency decoupling:</p> <ul style="list-style-type: none"> (35) 10 μF 0805 caps - ESR 5 mΩ (typ) and ESL 0.6 nH placed in and near package outline. 	Refer to the <i>Intel® Celeron® M Processor Datasheet</i> for more information.
V_{CCP} Decoupling	<p>Intel recommends bulk decoupling:</p> <ul style="list-style-type: none"> (2) 150 μF POSCAP - ESR 42 mΩ (typ) and ESL 2.5 nH, placed one each near the CPU and the GMCH packages. (10) 0.1 μF X7R 0603 caps - ESR 16 mΩ (typ) and ESL 0.6 nH, placed on the secondary side within the CPU package outline. 	Refer to the <i>Intel® Celeron® M Processor Datasheet</i> for more information.

NOTES:

- A[31:3]# pins on the processor correspond to HA[31:3]# pins on the GMCH.
- ADSTB[1:0]# pins on the processor correspond to HADSTB[1:0]# pins on the GMCH.
- DSTBN[3:0]# pins on the processor correspond to HDSTBN[3:0]# pins on the GMCH.
- DSTBP[3:0]# pins on the processor correspond to HDSTBP[3:0]# pins on the GMCH.
- D[63:0]# pins on the processor correspond to HD[63:0]# pins on the GMCH.
- REQ[4:0]# pins on the processor correspond to HREQ[4:0]# pins on the GMCH.
- The RESET# pin on the processor corresponds to the CPURST# pin on the GMCH. Refer to the ITP portion of this checklist, [Section 6.1.5](#) for treatment of RESET# when using ITP700FLEX debug port.
- The TRDY# pin on the processor corresponds to the HTRDY# pin on the GMCH.

15.4 Intel® 852GM Chipset GMCH Layout Checklist

Table 131. Intel® 852GM Chipset GMCH Layout Checklist (Sheet 1 of 5)

Checklist Items	Recommendations	Comments
Host Interface Signals		
ADS# BNR# BPRI# BREQ0# ¹ CPURST# ² DBSY# DEFER# HA[31:3]# ³ HD[63:0]# ⁴ HADSTB[1:0]# ⁵ HDSTBN[3:0]# ⁶ HDSTBP[3:0]# ⁷ HIT# HITM# HLOCK# ¹⁰ HREQ[4:0]# ⁸ HTRDY# ⁹ DRDY# RS[2:0]# DINV[3:0]#	Refer to the Processor section of this checklist.	
DDR System Memory Interface		
SDQS[8] SDM[8] SDQ[71:64]	<ul style="list-style-type: none"> ECC error detection is not supported on the 825GM CGMCH. Leave these signals as no connect. 	Refer to Section 9 .
SCK[5:0] SCK[5:0]#	<ul style="list-style-type: none"> Route as closely-coupled differential pairs, three clock pairs to each DIMM. Spacing to other DDR signals should not be less than 20 mils. Isolation from non-DDR signals should be 25 mils. Route on internal layers, except for pin escapes. Nominal internal trace width 7 mils and nominal internal spacing 4 mils. Routed trace length limits are 3.5 to 6.5 inches. Length match clock pairs to ± 10 mils. Match all DIMM0 clock lengths and match all DIMM1 clock lengths. Use GMCH package lengths for pad-to-pin length tuning. 	Refer to the detailed routing guidelines in Section 9.4.3 .

Table 131. Intel® 852GM Chipset GMCH Layout Checklist (Sheet 2 of 5)

Checklist Items	Recommendations	Comments
SDQ[63:0] SDM[7:0] SDQS[7:0]	<ul style="list-style-type: none"> Route SDQ/SDM with trace impedance $55 \Omega \pm 15\%$ using 2:1 spacing. Route SDQS strobes similarly with 3:1 spacing. Isolation from non-DDR signals should be 20 mils. Overall min/max length to the DIMM must comply with clock length matching requirements. 	Refer to the detailed routing guidelines in Section 9.4.4 .
SCKE[3:0] SCS[3:0]#	<ul style="list-style-type: none"> Route with trace impedance $55 \Omega \pm 15\%$ using 2:1 spacing. Isolation from non-DDR signals should be 20 mils. GMCH pad to DIMM trace length limits are 2.0 to 6.0 inches. Place parallel termination resistor within 2.0 inches of DIMM pad. Overall min/max length to the DIMM must comply with clock length matching requirements. 	Refer to the detailed routing guidelines in Section 9.4.5 .
SRAS# SCAS# SWE# SMA[12:6,3,0] SBA[1:0]	<ul style="list-style-type: none"> Route with trace impedance $55 \Omega \pm 15\%$ using 2:1 spacing. Isolation from non-DDR signals should be 20 mils. GMCH pad to first DIMM trace length limits are 2.0 to 5.5 inches. Total DIMM to DIMM spacing should be less than two inches. Place parallel termination resistor within 1.5 inches of the second DIMM pad. Overall min/max length to the DIMM must comply with clock length matching requirements. 	Refer to the detailed routing guidelines in Section 9.4.6 .
SMA[5,4,2,1] SMAB[5,4,2,1]	<ul style="list-style-type: none"> Route with trace impedance $55 \Omega \pm 15\%$ using 2:1 spacing. Isolation from non-DDR signals should be 20 mils. GMCH pad to DIMM trace length limits are 2.0 to 6.0 inches. Place parallel termination resistor within 2.0 inches of the DIMM pad. Overall min/max length to the DIMM must comply with clock length matching requirements. 	Refer to the detailed routing guidelines in Section 9.4.7 .
RCVENIN# RCVENOUT#	<ul style="list-style-type: none"> Internally shunted on Intel® 852GM chipset - no external connection necessary. Recommendation is that both signals be transitioned to the secondary side with vias next to the package balls to facilitate probing. 	Refer to the detailed routing guidelines in Section 9.4.8 .

Table 131. Intel® 852GM Chipset GMCH Layout Checklist (Sheet 3 of 5)

Checklist Items	Recommendations	Comments
DDR System Memory Decoupling		
GMCH VCCSM Decoupling	<ul style="list-style-type: none"> Requires a minimum of eleven 0603, 0.1µF caps placed within 150 mils of the GMCH package. Distribute evenly along the DDR memory interface, placed perpendicular to the GMCH with the power side of the caps facing the GMCH. Each GMCH ground and VCCSM power ball should have its own via. Each via should be as close to the associated cap pad as possible, within 25 mils and with as thick a trace as possible. 	Refer to Section 7.7.3 for more information.
DDR Bypass Caps	<ul style="list-style-type: none"> Place nine evenly spaced 0.1µF 0603 caps between the DIMMs. A wide trace from each cap should connect to a via that transitions to the ground plane layer. A wide trace should connect the 2.5 V side of each cap to a via that transitions to the 2.5 V plane, each via placed as close to the cap pad as possible. Each cap should also connect to the closest 2.5 V DIMM pin on either DIMM connector with a wide trace. 	<ul style="list-style-type: none"> Helps minimize return path discontinuities. Refer to Section 7.7.4 for more information.
DDR VTT Decoupling	<ul style="list-style-type: none"> Decouple VTT termination rail using one 0603 0.1µF capacitor per four DDR signals and one 0603 0.01µF capacitor per four DDR signals. Spread out placement across the VTT termination rail, connecting directly to the rail, so that each parallel termination resistor is within 100 mils of one of these high-frequency capacitors. Each ground via should be as close to the associated cap pad as possible, within 25 mils and with as thick a trace as possible. 	Refer to Section 7.7.5 for more information.

Hub Interface		
General Guidelines	<ul style="list-style-type: none"> Route hub interface data and strobes with trace impedance $55 \Omega \pm 15\%$ using 4/8 spacing and VSS reference. Route hub interface strobe and its complement as a differential pair, length matched within ± 10 mils. Maximum length for both data and strobe signals is 6.0 inches. Hub interface data and strobe signals are routed on the same layer, transitioning together when a layer change is required. Keep layer changes to a minimum, using only two vias per net. 	<ul style="list-style-type: none"> Refer to Section 10.2.1 for detailed routing recommendations. The platform design guide example references routing guidelines for the 8-bit Hub Interface using enhanced (parallel) termination.

Table 131. Intel® 852GM Chipset GMCH Layout Checklist (Sheet 4 of 5)

Checklist Items	Recommendations	Comments
Clocks and Reset Signals		
BCLK BCLK#	<ul style="list-style-type: none"> The differential host clock pair should be length matched to ± 10 mils and to the processor BCLK/BCLK# pair within ± 20 mils overall (match L1 segments to ± 10 mils across all pairs). Route as strip-line traces 4/7 mils spacing (except as allowed for pin escapes). Total length range is 2.0 to 8.5 inches. 	<ul style="list-style-type: none"> Refer to host clock group routing guidelines detailed in Section 13.2.1. Refer to Chapter 10 for detailed breakdown of all system clock routing recommendations.
GCLKIN	<ul style="list-style-type: none"> Place series resistor close to CK408, within 500 mils. Total trace length range is 4.0 to 9.0 inches. Minimum spacing 20 mils. Overall length of CLK66 is considered the reference length for all other clocks, except USBCLK and CLK14. The length of CLK66 traces should be matched within ± 100 mils and then used as the basis for defining the length of all other length matched clocks. 	Refer to CLK66 clock group routing guidelines detailed in Section 13.2.2 .
RSTIN#	Connect to PCIRST# output of the Intel® 82801DB ICH4.	
GMCH Decoupling, VREF, and Filtering		
HLRCOMP HLVREF PSWING	<ul style="list-style-type: none"> GMCH HLRCOMP signal should be strapped to 1.2 V via $27.4 \Omega \pm 1\%$ HLRCOMP resistor with trace impedance $55 \Omega \pm 15\%$. HLVREF and PSWING voltage requirements must be set appropriately for proper hub interface operation. The case is similar for HIREF and HIVSWING signals on ICH4. 	Refer to Section 10.3 for HI specific voltage requirements and several options for voltage divider circuits.
HXRCOMP HYRCOMP	<ul style="list-style-type: none"> Each signal should be pulled to ground with a $27.4 \Omega \pm 1\%$ resistor. Max trace length to the resistor should be less than 0.5 inches and should be 18 mils wide to achieve the characteristic impedance target of 27.4Ω. Maintain 25 mil separation from any switching signals. 	<ul style="list-style-type: none"> This signal is used to calibrate the Host AGTL+ I/O buffers characteristics to specific board characteristics. Refer to Section 7.7.7.2 for more information.
HDVREF[2:0] HAVREF HCCVREF	<ul style="list-style-type: none"> Max length from pin to voltage divider for each reference voltage should be less than 0.5 inch. 10 mil traces are recommended. 	<ul style="list-style-type: none"> To provide constant and clean power delivery to the data, address, and common clock signals of the host AGTL+ interface. Refer to Section 7.7.7.1 for recommended individual voltage divider circuits.

Table 131. Intel® 852GM Chipset GMCH Layout Checklist (Sheet 5 of 5)

Checklist Items	Recommendations	Comments
HXSWING HYSWING	<ul style="list-style-type: none"> Voltage divider components for each input should be placed within 0.5 inch of their respective pins. Use a 15 mil wide trace maintaining a minimum of 25 mils separation to other signals. 	<ul style="list-style-type: none"> The HXSWING and HYSWING inputs of GMCH are used to provide reference voltage for the compensation logic. Refer to Section 7.7.7.3 for more information.
Analog Power Filtering	There are eight analog circuits that require filtered supplies on the Intel® 852GM chipset.	Refer to Section 7.7.7.4 for detailed filter requirements.

NOTES:

1. The BREQ0# pin on the GMCH corresponds to the BR0# pin on the processor.
2. The CPURST# pin on the GMCH corresponds to the RESET# pin on the processor.
3. HA[35:3]# pins on the GMCH correspond to A[31:3]# pins on the processor.
4. HD[63:0]# pins on the GMCH correspond to D[63:0]# pins on the processor.
5. HADSTB[1:0]# pins on the GMCH correspond to ADSTB[1:0]# pins on the processor.
6. HADSTBN[3:0]# pins on the GMCH correspond to DSTBN[3:0]# pins on the processor.
7. HADSTBP[3:0]# pins on the GMCH correspond to DSTBP[3:0]# pins on the processor.
8. HREQ[4:0]# pins on the GMCH correspond to REQ[4:0]# pins on the processor.
9. The HTRDY# pin on the GMCH corresponds to the TRDY# pin on the processor.
10. The HLOCK# pin on the GMCH correspond to LOCK# pin on the processor.

15.5 Intel® 82801DB I/O Control Hub 4 (ICH4) Layout Checklist

Table 132. Intel® 82801DB I/O Controller Hub 4 (ICH4) Layout Checklist (Sheet 1 of 5)

Checklist Items	Recommendations	Comments
Processor Signals		
A20M# CPUSLP# FERR# IGNNE# INIT# LINT[1:0] SMI# STPCLK#	Refer to the Processor section of this checklist.	
FWH Interface		
Decoupling	<ul style="list-style-type: none"> 0.1 μF capacitors should be placed between the V_{CC} supply balls and the VSS ground balls, and no less than 390 mils from the V_{CC} supply balls. 4.7 μF capacitors should be placed between the V_{CC} supply balls and the VSS ground balls, and no less than 390 mils from the V_{CC} supply balls. 	
Hub Interface - Refer to General Guidelines in the GMCH section of this checklist.		
IDE Checklist		
General Guidelines	<ul style="list-style-type: none"> Traces are routed 5 mils wide with 7 mils spacing. Max trace length is eight inches long. The maximum length difference between the shortest data signal and the longest strobe signal of a channel is 0.5 inch. 	<ul style="list-style-type: none"> Refer to Section 11.3 for primary/secondary IDE details. Refer to ATA/ATAPI-6 specification.
LAN Interface		
General Guidelines	Maintain board trace impedance $55 \Omega \pm 15\%$ per example 8-layer stack-up to avoid violation of signal integrity requirements.	Refer to Section 3.1 for more information.
	Traces: 5 mils wide, 10 mils spacing.	Refer to Section 11.12.1.1 .

Table 132. Intel® 82801DB I/O Controller Hub 4 (ICH4) Layout Checklist (Sheet 2 of 5)

Checklist Items	Recommendations	Comments
General Guidelines	<ul style="list-style-type: none"> Point-to-Point Single Solution - trace length range, Intel® 82801DB I/O Controller Hub 4 (ICH4) to Intel® 82562ET/ Intel® 82562EM Platform LAN Connect component should be 4.5 to 12 inches. Range for CNR is 2 to 9.5 inches. LOM and CNR Solution - trace length range ICH4 to RPAK should be L1 = 0.5 to 7.5 inches. Range for RPAK to PLC is L2 = 4 to (11.5 - L1) inches. Range for RPAK to CNR is L2 = 1.5 to (9.0 - L1) inches. CNR card trace length range is 0.5 to 3 inches. Total trace length is not to exceed 9.5 inches. 	<ul style="list-style-type: none"> To meet timing requirements. Refer to Section 11.12.1.1 for more information.
	Stubs due to RPAK CNR/LOM stuffing option should not be present on the surface.	To minimize inductance.
	All routing should reference V_{SS} .	
	Maximum mismatch between the length of LAN_CLK and the length of any data trace is 0.5 inch (clock must be the longest trace).	To meet timing and signal quality requirements.
	Maintain constant symmetry and spacing between the traces within a differential pair out of the LAN phy.	To meet timing and signal quality requirements.
	Keep the total length of each differential pair under four inches.	Issues found with traces longer than four inches. <ul style="list-style-type: none"> IEEE phy conformance failures Excessive EMI and or degraded receive BER.
	Do not route the transmit differential traces closer than 100 mils to the receive differential traces.	To minimize crosstalk.
	Distance between differential traces and any other signal line must be at least 100 mils. (Intel recommends 300 mils.)	To minimize crosstalk.
	Differential trace impedance should be controlled to be ~100 Ω .	To meet timing and signal quality requirements.
	For high-speed signals, the number of corners and vias should be minimized. When a 90-degree bend is required, use two 45-degree bends.	To meet timing and signal quality requirements.
	Traces should be routed away from board edges by a distance greater than the trace height above the ground plane.	This allows the field around the trace to couple more easily to the ground plane rather than to adjacent wires or boards.
	Do not route traces and vias under crystals or oscillators.	This prevents coupling to or from the clock.

Table 132. Intel® 82801DB I/O Controller Hub 4 (ICH4) Layout Checklist (Sheet 3 of 5)

Checklist Items	Recommendations	Comments
General Guidelines	Trace width to height ratio above the ground plane should be between 1:1 and 3:1.	To control trace EMI radiation.
	Traces between decoupling and I/O filter capacitors should be as short and wide as practical.	Long and thin lines are more inductive and would reduce the intended effect of decoupling capacitors.
	Vias to decoupling capacitors should be sufficiently large in diameter.	To decrease series inductance.
	Isolate I/O signals from high speed signals.	To minimize crosstalk.
	Avoid routing high-speed LAN or Phone line traces near other high-frequency signals associated with a video controller, cache controller, processor, or other similar device.	To minimize crosstalk.
	Place the Intel® 82562ET/ Intel® 82562EM Platform LAN Connect component more than 1.5 inches away from any board edge.	This minimizes the potential for EMI radiation problems.
	Place at least one bulk capacitor (4.7 μ F or greater OK) on each side of the Intel® 82562ET/ Intel® 82562EM Platform LAN Connect component.	Research and development has shown that this is a robust design recommendation.
	Place decoupling capacitors (0.1 μ F) as close to the Intel 82562ET/ Intel 82562EM Platform LAN Connect component as possible.	
ICH4 Power Decoupling		
V_CPU_IO[2:0]	Use one 0.1 μ F decoupling capacitor. Locate within 100 mils of the ICH4 package near ball AA23.	Refer to Section 7.7.8.1 for more information.
V _{CC3_3}	Requires six 0.1 μ F decoupling capacitors. Place caps within 100 mils of the ICH4 package near balls A4, A1, H1, T1, AC10, and AC18.	
V _{CCSUS3_3}	Requires two 0.1 μ F decoupling capacitors. Place within 100 mils of the ICH4 package near balls A22 and AC5.	
V _{CC1_5}	Requires two 0.1 μ F decoupling capacitors. Place within 100 mils of the ICH4 package near balls K23 and C23.	
V _{CCSUS1_5}	Requires two 0.1 μ F decoupling capacitors. Place within 100 mils of the ICH4 package near balls A16 and AC1.	
V _{5REF_SUS}	Requires one 0.1 μ F decoupling capacitor. V _{5REF_SUS} affects only 5 V tolerance for USB OC[5:0]# balls, and may be connected to V _{CCSUS3_3} when 5 V tolerance on these signal is not required.	

Table 132. Intel® 82801DB I/O Controller Hub 4 (ICH4) Layout Checklist (Sheet 4 of 5)

Checklist Items	Recommendations	Comments
V _{5REF}	Requires one 0.1 µF decoupling capacitor placed near ball E7. V _{5REF} is the reference voltage for 5 V tolerant inputs in the ICH4. Tie to balls V _{5REF} [2:1]. V _{5REF} must power up before or simultaneous to V _{CC3_3} . It must power down after or simultaneous to V _{CC3_3} .	
V _{CCRTC}	Requires one 0.1 µF decoupling capacitor placed near ball AB5.	
V _{CCHI}	Requires two 0.1 µF decoupling capacitors placed near balls T23 and N23.	
V _{CCPLL}	Requires one 0.1 µF and one 0.01 µF decoupling capacitor placed near ball C22.	
RTC		
General Guidelines	<ul style="list-style-type: none"> • RTC ball to crystal termination trace length should be less than one inch. • Use five mil trace width (results in approximately 2 pF per inch). • Minimize capacitance between RTCX1 and RTCX2. • Put ground plane underneath crystal components. • Do not route switching signals under the external components (unless on other side of board). 	Refer to Section 11.11.1 for more information.
USB		
General Guidelines	<ul style="list-style-type: none"> • Route all traces over continuous planes (ground) with no interruptions. Avoid crossing over anti-etch when possible. Crossing over anti-etch (plane splits) increases inductance and radiation levels by forcing a greater loop area. Likewise, avoid changing layers with high-speed traces. (Applies to USB signals, high-speed clocks, as well as slower signals that might be coupling to them.) • Keep traces at least 50 mils away from the edge of the reference ground plane. This helps prevent the coupling of the signal onto adjacent wires, and helps prevent free radiation of the signal from the edge of the PCB. 	<ul style="list-style-type: none"> • Refer to Section 11.7.1 for detailed USB guidelines. • Refer to Section 11.7.1.1 for termination recommendations.

Table 132. Intel® 82801DB I/O Controller Hub 4 (ICH4) Layout Checklist (Sheet 5 of 5)

Checklist Items	Recommendations	Comments
General Guidelines	<ul style="list-style-type: none"> Maintain parallelism between USB differential signals with the trace spacing needed to achieve 90 Ω differential impedance. (Recommended: Use of impedance calculator to determine the trace width and spacing required for the specific board stack-up being used. Using 4 mil traces with 4.5 mil spacing results in approximately 90 Ω differential trace impedance. Minimize the length of high-speed clock and periodic signal traces that run parallel to USB signal lines to minimize crosstalk. The minimum recommended spacing to clock signals is 50 mils. Use 20 mils minimum spacing between USB signal pairs and other signal traces. This helps to prevent crosstalk. USB signal pair traces should be trace length matched. Max trace length mismatch between USB signal pairs should be no greater than 150 mils. No termination resistors needed for USB. 	<ul style="list-style-type: none"> Refer to Section 11.7.1 for detailed USB guidelines. Refer to Section 11.7.1.4 for termination recommendations.

Schematic Checklist Summary

16

The following checklist provides design recommendations and guidance for the Intel Celeron Processor, Intel Celeron M Processor, or the Mobile Intel Celeron Processors with the Intel® 852GM chipset.

The schematic checklist is a tool used to ensure that design recommendations detailed in this Platform Design Guide have been followed prior to schematic reviews. The items contained in this checklist attempt to address important connections and critical supporting circuitry; however, **it is not a complete list**. For complete design recommendations, refer to the main content of this document (referred to as the Platform Design Guide) and the appended board schematics. The information in this guide is subject to change.

Note: Unless otherwise specified the default tolerance on resistors is $\pm 5\%$.

16.1 Intel® Celeron® Processor Checklists

16.1.1 Resistor Recommendations Checklist

Table 133. Resistor Recommendations Checklist (Sheet 1 of 5)

Pin Name	System Pull-up/Pull-down	Series Termination	Voltage Translation	Notes	✓
A[31:3]#				Connect to HA[31:3]# pins on 852GM.	
A[35:32]#				No connect.	
A20M#				Connect to A20M# pin on ICH4	
ADS#				Connect to ADS# pin on 852GM.	
ADSTB[1:0]#				Connect to HADSTB[1:0]# pins on 852GM.	
AP[1:0]#				No connect.	
BINIT#				No Connect.	
BNR#				Connect to BNR# pin on the 852GM.	
BPM[5:0]#				Refer to the <i>ITP700 Debug Port Design Guide</i> for further information.	
BPRI#				Connect to BPRI# pin on 852GM.	
BR0#	220 Ω \pm 5% pull-up to VCC_CPU.			Connect to BREQ0# pin to 852GM.	
BSEL[1:0]				No Connect.	
COMP[1:0]	Terminate to GND through a 51.1 Ω \pm 1% resistor.			Minimize the distance from termination resistor and processor pin.	
D[63:0]#				Connect to HD[63:0]# pins on 852GM.	
DBI[3:0]#				Connect to DINV[3:0]# pins on 852GM.	
DBR#				Refer to the <i>ITP700 Debug Port Design Guide</i> for further information.	
DBSY#				Connect to DBSY# pin on the 852GM.	
DEFER#				Connect to DEFER# pin on the 852GM.	
DP[3:0]#				No connect.	

NOTE: Default tolerance for resistors is \pm 5% unless otherwise specified.

Table 133. Resistor Recommendations Checklist (Sheet 2 of 5)

Pin Name	System Pull-up/Pull-down	Series Termination	Voltage Translation	Notes	✓
DRDY#				Connect to DRDY# pin on the 852GM.	
DSTBN[3:0]#				Connect to HDSTBN[3:0]# pins on 852GM.	
DSTBP[3:0]#				Connect to HDSTBP[3:0]# pins on 852GM.	
FERR#	62 Ω \pm 5% pull-up to VCC_CPU			Connect to FERR# pin on ICH4, with resistor placed by ICH4.	
GTLREF[3:0]	Terminate to VCC_CPU through a 49.9 Ω \pm 1% resistor. Terminate to GND through a 100 Ω \pm 1% resistor. Should be 2/3 VCC_CPU.			Voltage divider should be placed within 1.5 inches of the processor pin. Place 1 μ F cap by the resistor divider, 220 pF by the processor pin. Minimum one GTLREF pin require to be connected as recommended above.	
HIT#				Connect to HIT# pin on 852GM.	
HITM#				Connect to HITM# pin on 852GM.	
IERR#	62 Ω \pm 5% pull-up to VCC_CPU			IERR# may also be routed to a test point or to any optional system receiver.	
IGNNE#				Connect to IGNNE# pin on ICH4.	
INIT#			See Figure 173	Connect to INIT# pin on ICH4. Voltage transition circuit is required if connecting to FWH. See Figure 173 for more information.	
ITP_CLK0				Refer to the <i>ITP700 Debug Port Design Guide</i> for further information.	
ITP_CLK1				Refer to the <i>ITP700 Debug Port Design Guide</i> for further information.	
LINT0/INTR				Connect to INTR# pin on ICH4.	

NOTE: Default tolerance for resistors is \pm 5% unless otherwise specified.

Table 133. Resistor Recommendations Checklist (Sheet 3 of 5)

Pin Name	System Pull-up/Pull-down	Series Termination	Voltage Translation	Notes	✓
LINT1/NMI				Connect to NMI pin on ICH4.	
LOCK#				Connect to HLOCK# pin on 852GM.	
MCERR#				No Connect.	
PROCHOT#	62 Ω \pm 5% pull up to VCC_CPU			Refer to board schematic and Figure 175 for more details. When PROCHOT# is routed to external logic, voltage translation may be required. The receiver at the output of the voltage translation circuit may be any receiver that functions properly with the PROCHOT# signal.	
PWRGOOD	300 Ω \pm 5% pull-up to VCC_CPU			Connect to CPUPWRGD signal on ICH4, with resistor placed by the processor.	
REQ[4:0]#				Connect to HREQ[4:0]# pins on MCH.	
RESET#	51 Ω \pm 5% pull-up to VCC_CPU.			Connect to CPURST# pin on 852GM. If ITP is implemented, refer to the <i>ITP700 Debug Port Design Guide</i> for further information.	
RS[2:0]#				Connect to RS[2:0]# pin on 852GM.	
RSP#				No connect.	
SKTOCC#				Connect to Glue Chip / Discrete Logic (if pin is used).	
SLP#				Connect to CPUSLP# pin on ICH4.	
SMI#				Connect to SMI# pin on ICH4.	
STPCLK#				Connect to STPCLK# pin on ICH4.	
TCK				Refer to the <i>ITP700 Debug Port Design Guide</i> for further information.	

NOTE: Default tolerance for resistors is \pm 5% unless otherwise specified.

Table 133. Resistor Recommendations Checklist (Sheet 4 of 5)

Pin Name	System Pull-up/Pull-down	Series Termination	Voltage Translation	Notes	✓
TDI				Refer to the <i>ITP700 Debug Port Design Guide</i> for further information.	
TDO				Refer to the <i>ITP700 Debug Port Design Guide</i> for further information.	
TESTHI[1:0], TESTHI[5:2] TESTHI[10:8] TESTHI[12:11]	Matched resistors pull up to VCC_CPU with value $\pm 20\%$ of trace impedance.			TESTHI pins may use individual pull-up resistors too.	
THERMDA				If used, connect to thermal monitor circuitry.	
THERMDC				If used, connect to thermal monitor circuitry.	
THERMTRIP#	62 $\Omega \pm 5\%$ pull-up to VCC_CPU.			Connect to THRMTRIP# pin on ICH4 ICH4, with resistor placed by ICH4. If connecting to other device, voltage translation logic may be required.	
TMS				Refer to the <i>ITP700 Debug Port Design Guide</i> for further information.	
TRDY#				Connect to HTRDY# pin on MCH.	
TRST#				Refer to the <i>ITP700 Debug Port Design Guide</i> for further information.	
VCC[85:0]	Connect to VCC_CPU.				
VCCA, VSSA, VCCIOPLL	Connect to VCC_CPU via filter.			C1 = 22 μ F - 33 μ F with a 20% tolerance. The ESL is ≤ 2.5 nH and the ESR $\leq 0.225 \Omega$. L1, L2 = 10 μ H $\pm 25\%$. Rdc = 0.4 $\pm 30\%$. See Figure 174 for more information.	
VCCSENSE, VSSSENSE				If used, connect to VR control silicon.	
VCCVID				Connect to 1.2 V linear regulator.	

NOTE: Default tolerance for resistors is $\pm 5\%$ unless otherwise specified.



Table 133. Resistor Recommendations Checklist (Sheet 5 of 5)

Pin Name	System Pull-up/Pull-down	Series Termination	Voltage Translation	Notes	✓
VID[4:0]	These signals must be pulled up to 3.3 V through either 1 kΩ pull-ups on the PCB or with internal pull-ups in the VR or VRM.			Connect to VR or VRM.	
VSS[182:0]	Connect to GND.				

NOTE: Default tolerance for resistors is ± 5% unless otherwise specified.

Figure 173. Routing Illustration for INIT#

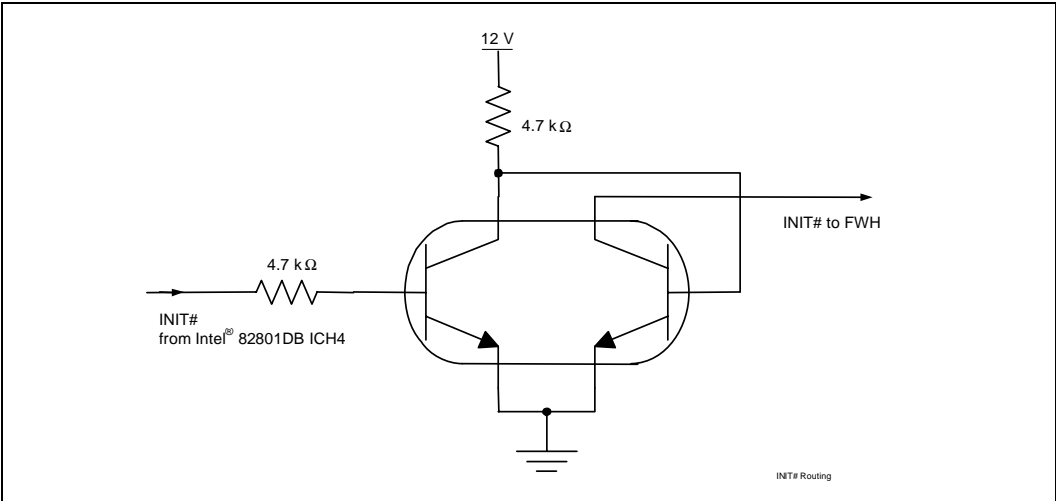


Figure 174. VCCIOPLL, VCCA, and VSSA Power Distribution

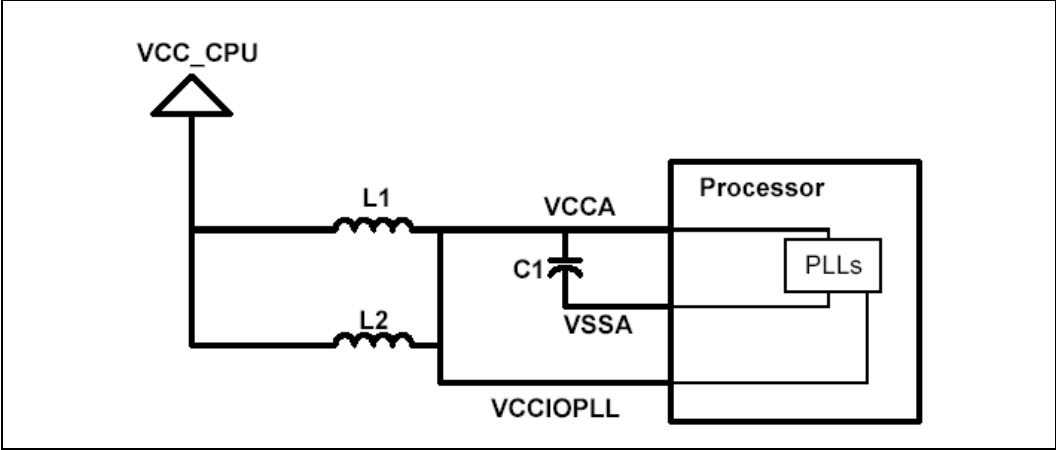
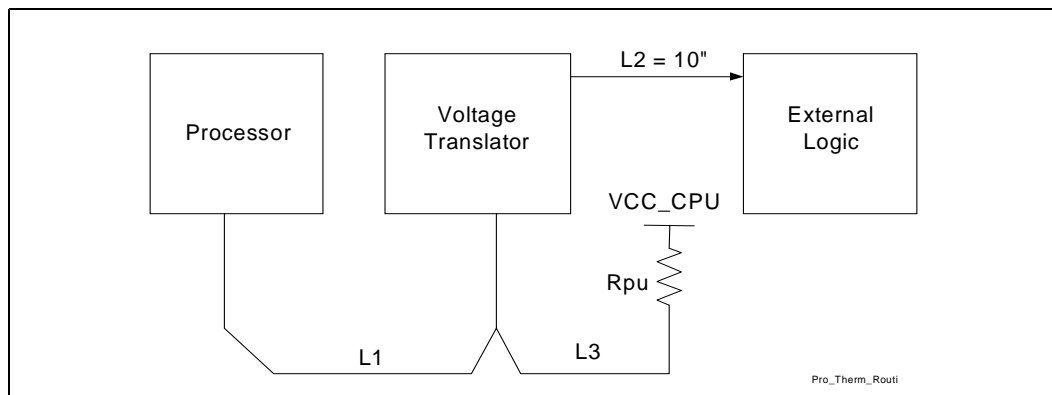


Figure 175. Voltage Translation Circuit for PROCHOT#



16.1.2 In Target Probe (ITP) Checklist

Refer to the latest revision of the *ITP700 Debug Port Design Guide* for details on the implementation of the debug port. The document can be found from <http://developer.intel.com/design/Xeon/guides/249679.htm>.

16.1.3 Decoupling Recommendations Checklist

Table 134. Decoupling Recommendations Checklist

Signal	Configuration	Value	Qty	Notes	✓
VCC[Vcc_CPU]	Connect to VCC	560µF 22µF 1200µF 4.7µF	10 40 4 4	22µF caps in X5R, 1206 package for high frequency decoupling.	

NOTE: Decoupling guidelines are recommendations based on our reference board design. Customers will need to take layout & PCB board design into consideration when deciding on overall decoupling solution.

16.2 Mobile Intel® Celeron® Processor Checklists

16.2.1 Resistor Recommendations Checklist

Table 135. Resistor Recommendations Checklist (Sheet 1 of 5)

Pin Name	System Pull-up/Pull-down	Series Termination	Voltage Translation	Notes	✓
A[31:3]#				Connect to HA[31:3]# pins on 852GM.	
A[35:32]#				No connect.	
A20M#				Connect to A20M# pin on ICH4	
ADS#				Connect to ADS# pin on 852GM.	
ADSTB[1:0]#				Connect to HADSTB[1:0]# pins on 852GM.	
AP[1:0]#				No connect.	
BINIT#				No Connect.	
BNR#				Connect to BNR# pin on the 852GM.	
BPM[5:0]#				Refer to the <i>ITP700 Debug Port Design Guide</i> for further information.	
BPRI#				Connect to BPRI# pin on 852GM.	
BR0#	220 Ω \pm 5% pull-up to VCC_CPU.			Connect to BREQ0# pin to 852GM.	
BSEL[1:0]				No Connect.	
COMP[1:0]	Terminate to GND through a 51.1 Ω \pm 1% resistor.			Minimize the distance from termination resistor and processor pin.	
D[63:0]#				Connect to HD[63:0]# pins on 852GM.	
DBI[3:0]#				Connect to DINV[3:0]# pins on 852GM.	
DBR#				Refer to the <i>ITP700 Debug Port Design Guide</i> for further information.	
DBSY#				Connect to DBSY# pin on the 852GM.	
DEFER#				Connect to DEFER# pin on the 852GM.	
DP[3:0]#				No connect.	

NOTE: Default tolerance for resistors is \pm 5% unless otherwise specified.

Table 135. Resistor Recommendations Checklist (Sheet 2 of 5)

Pin Name	System Pull-up/Pull-down	Series Termination	Voltage Translation	Notes	✓
DPSLP#	4.7 K Ω pull-up to VCC_CPU at CPU, 1 K Ω pull-up to VCC_CPU at GMCH			Used only with the ICH4-M. The ICH4 does not provide this signal.	
DRDY#				Connect to DRDY# pin on the 852GM.	
DSTBN[3:0]#				Connect to HDSTBN[3:0]# pins on 852GM.	
DSTBP[3:0]#				Connect to HDSTBP[3:0]# pins on 852GM.	
FERR#	56 Ω \pm 5% pull-up to VCC_CPU			Connect to FERR# pin on ICH4, with resistor placed by ICH4.	
GTLREF[3:0]	Terminate to VCC_CPU through a 49.9 Ω \pm 1% resistor. Terminate to GND through a 100 Ω \pm 1% resistor. Should be 2/3 VCC_CPU.			Voltage divider should be placed within 1.5 inches of the processor pin. Place 1 μ F cap by the resistor divider, 220 pF by the processor pin. Minimum one GTLREF pin require to be connected as recommended above.	
HIT#				Connect to HIT# pin on 852GM.	
HITM#				Connect to HITM# pin on 852GM.	
IERR#	56 Ω \pm 5% pull-up to VCC_CPU			IERR# may also be routed to a test point or to any optional system receiver.	
IGNNE#				Connect to IGNNE# pin on ICH4.	
INIT#			See Figure 176	Connect to INIT# pin on ICH4. Voltage transition circuit is required if connecting to FWH. See Figure 176 for more information.	
ITP_CLK0				Refer to the <i>ITP700 Debug Port Design Guide</i> for further information.	

NOTE: Default tolerance for resistors is \pm 5% unless otherwise specified.

Table 135. Resistor Recommendations Checklist (Sheet 3 of 5)

Pin Name	System Pull-up/Pull-down	Series Termination	Voltage Translation	Notes	✓
ITP_CLK1				Refer to the <i>ITP700 Debug Port Design Guide</i> for further information.	
LINT0/INTR				Connect to INTR# pin on ICH4.	
LINT1/NMI				Connect to NMI pin on ICH4.	
LOCK#				Connect to HLOCK# pin on 852GM.	
MCERR#				No Connect.	
PROCHOT#	56 Ω \pm 5% pull up to VCC_CPU			Refer to board schematic and Figure 178 for more details. When PROCHOT# is routed to external logic, voltage translation may be required. The receiver at the output of the voltage translation circuit may be any receiver that functions properly with the PROCHOT# signal.	
PWRGOOD	300 Ω \pm 5% pull-up to VCC_CPU			Connect to CPUPWRGD signal on ICH4, with resistor placed by the processor.	
REQ[4:0]#				Connect to HREQ[4:0]# pins on MCH.	
RESET#	51 Ω \pm 5% pull-up to VCC_CPU.			Connect to CPURST# pin on 852GM. If ITP is implemented, refer to the <i>ITP700 Debug Port Design Guide</i> for further information.	
RS[2:0]#				Connect to RS[2:0]# pin on 852GM.	
RSP#				No connect.	
SKTOCC#				Connect to Glue Chip / Discrete Logic (if pin is used).	
SLP#				Connect to CPUSLP# pin on ICH4.	
SMI#				Connect to SMI# pin on ICH4.	

NOTE: Default tolerance for resistors is \pm 5% unless otherwise specified.

Table 135. Resistor Recommendations Checklist (Sheet 4 of 5)

Pin Name	System Pull-up/Pull-down	Series Termination	Voltage Translation	Notes	✓
STPCLK#				Connect to STPCLK# pin on ICH4.	
TCK				Refer to the <i>ITP700 Debug Port Design Guide</i> for further information.	
TDI				Refer to the <i>ITP700 Debug Port Design Guide</i> for further information.	
TDO				Refer to the <i>ITP700 Debug Port Design Guide</i> for further information.	
TESTHI[1:0], TESTHI[5:2] TESTHI[10:8] TESTHI[12:11]	Matched resistors pull up to VCC_CPU with value $\pm 20\%$ of trace impedance.			TESTHI pins may use individual pull-up resistors too.	
THERMDA				If used, connect to thermal monitor circuitry.	
THERMDC				If used, connect to thermal monitor circuitry.	
THERMTRIP#	56 $\Omega \pm 5\%$ pull-up to VCC_CPU.			Connect to THRMTRIP# pin on ICH4 ICH4, with resistor placed by ICH4. If connecting to other device, voltage translation logic may be required.	
TMS				Refer to the <i>ITP700 Debug Port Design Guide</i> for further information.	
TRDY#				Connect to HTRDY# pin on MCH.	
TRST#				Refer to the <i>ITP700 Debug Port Design Guide</i> for further information.	
VCC[85:0]	Connect to VCC_CPU.				

NOTE: Default tolerance for resistors is $\pm 5\%$ unless otherwise specified.

Table 135. Resistor Recommendations Checklist (Sheet 5 of 5)

Pin Name	System Pull-up/Pull-down	Series Termination	Voltage Translation	Notes	✓
VCCA, VSSA, VCCIOPLL	Connect to VCC_CPU via filter.			C1 = 22μF - 33μF with a 20% tolerance. The ESL is ≤ 2.5 nH and the ESR $\leq 0.225 \Omega$. L1, L2 = 10μH $\pm 25\%$. Rdc = 0.4 $\pm 30\%$. See Figure 177 for more information.	
VCCSENSE, VSSSENSE				If used, connect to VR control silicon.	
VCCVID				Connect to 1.2 V linear regulator.	
VID[4:0]	These signals must be pulled up to 3.3 V through either 1 kΩ pull-ups on the PCB or with internal pull-ups in the VR or VRM.			Connect to VR or VRM.	
VSS[182:0]	Connect to GND.				

NOTE: Default tolerance for resistors is $\pm 5\%$ unless otherwise specified.

Figure 176. Routing Illustration for INIT#

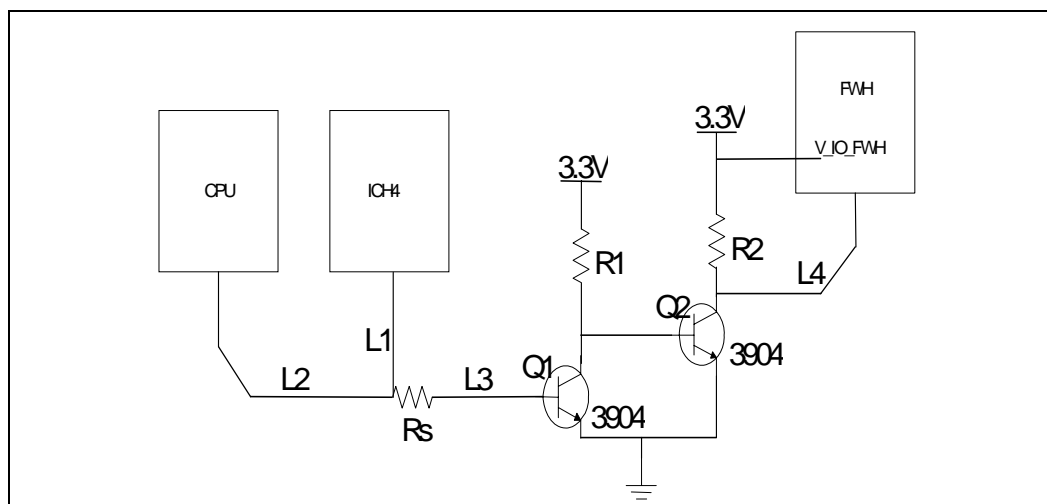


Figure 177. VCCIOPLL, VCCA, and VSSA Power Distribution

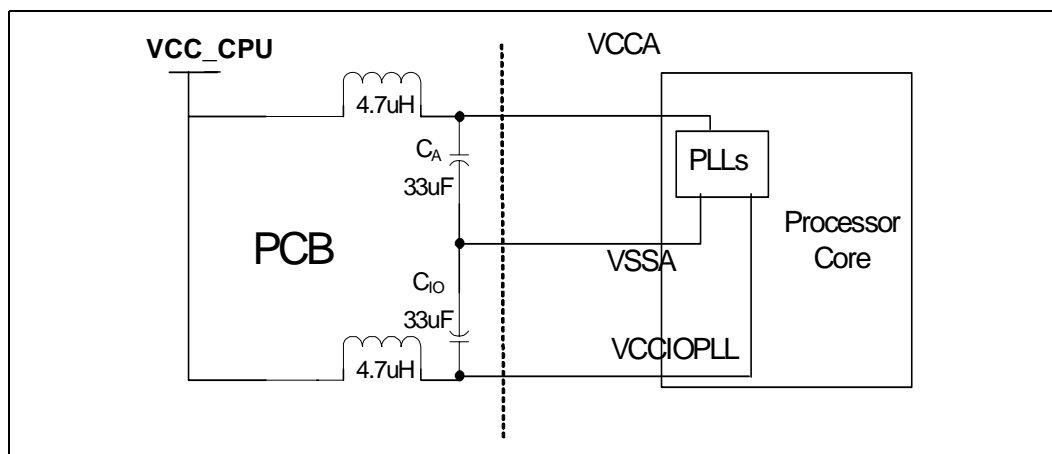
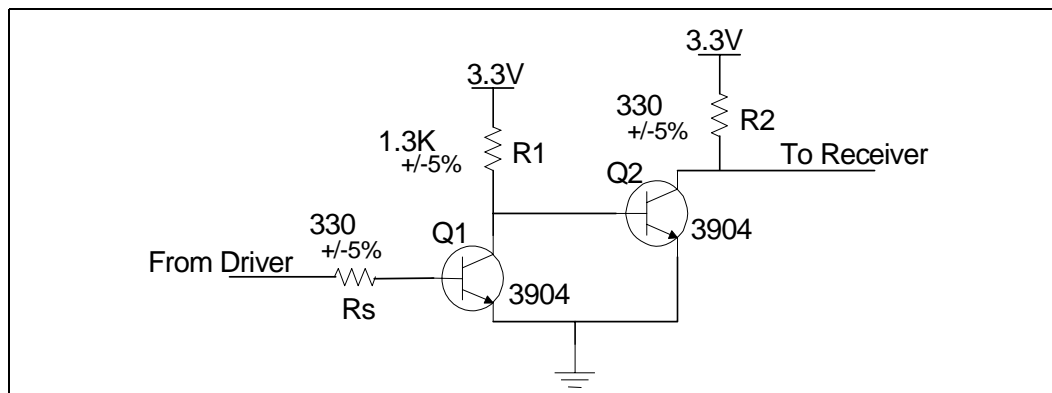


Figure 178. Voltage Translation Circuit for PROCHOT#



16.2.2 In Target Probe (ITP) Checklist

Refer to the latest revision of the *ITP700 Debug Port Design Guide* for details on the implementation of the debug port. The document can be found from <http://developer.intel.com/design/Xeon/guides/249679.htm>

16.2.3 Decoupling Recommendations Checklist

Table 136. Decoupling Recommendations Checklist

Signal	Configuration	Value	Qty	Notes	✓
VCC[Vcc_CPU]	Connect to VCC	10 μ F	38	X5R/X7R, 1206 package. Use for high frequency decoupling. Bulk decoupling will depend on the VR solution. The maximum Equivalent Series Resistance should be equal to or less than 2.5 m Ω	

NOTE: Decoupling guidelines are recommendations based on our reference board design. Customers will need to take layout & PCB board design into consideration when deciding on overall decoupling solution.

16.3 Intel® Celeron® M Processor Checklist

16.3.1 Connection Recommendations

Table 137 presents the connection recommendations.

Table 137. Connection Recommendations (Sheet 1 of 3)

Pin Name	System Pull-up/Pull-down	Series Termination	Voltage Translation	Notes	✓
A20M#				Point-to-point connection to the Intel® 82801DB I/O Controller Hub 4 (ICH4), (A20M# signal).	
BR0#				Point-to-point connection to GMCH (BREQ0# signal).	
COMP0, COMP2	27.4 Ω \pm 1% pull-down to GND			Resistor placed within 0.5 inch of processor pin. Trace should be 27.4 Ω \pm 15%.	
COMP1, COMP3	54.9 Ω \pm 1% pull-down to GND			Resistor placed within 0.5 inch of processor pin. Trace should be 55 Ω \pm 15%.	
FERR#	56 Ω pull-up to V _{CCP}	56 Ω from pull-up to ICH4 pin		Point-to-point connection to ICH4 (FERR# signal), with pull-up resistor and series resistor placed by the ICH4.	

Table 137. Connection Recommendations (Sheet 2 of 3)

Pin Name	System Pull-up/Pull-down	Series Termination	Voltage Translation	Notes	✓
GTLREF	1 K Ω \pm 1% pull-up to V _{CCP} 2 K Ω \pm 1% pull-down to GND			Voltage divider should be placed within 0.5 inch of processor pin.	
IERR#	56 Ω pull-up to V _{CCP}			IERR# is a 1.05 V signal. Voltage translation logic and/or series resistor may be required if used.	
INIT#			R1 = 1.3 K Ω R2 = 330 Ω Rs = 330 Ω	Point-to-point connection to the ICH4 (INIT# signal). Voltage translation circuit is required if connecting to FWH. Signal is T-split from the ICH4 to FWH. Refer to Figure 179.	
IGNNE#				Point-to-point connection to the ICH4 (IGNNE# signal).	
LINT0				Point-to-point connection to the ICH4 (INTR signal).	
LINT1				Point-to-point connection to the ICH4 (NMI signal).	
PROCHOT#	56 Ω pull up to V _{CCP}		R1 = 1.3 K Ω R2 = 330 Ω Rs = 330 Ω	PROCHOT# is a V _{CCP} signal. Voltage translation logic may be required if used. When Voltage Translation is Required: Driver isolation resistor (Rs) should be placed at the beginning of the T-split to the system receiver. Refer to Figure 180.	
PSI#				May be left as not connected (NC) if not used for Intel® IMVP.	
PWRGOOD	330 Ω pull-up to V _{CCP}			Point-to-point connection to the ICH4, with resistor placed by the processor.	
RESET#	220 Ω \pm 5% pull-up to V _{CCP} WHEN USING ITP700FLEX	22.6 Ω \pm 1% from pull-up to ITP700FLEX		Connect to CPURST# pin on 852GM. If ITP is implemented, refer to the <i>ITP700 Debug Port Design Guide</i> for further information.	
SLP#				Point-to-point connection to the ICH4 (CPUSLP# signal).	
SMI#				Point-to-point connection to the ICH4 (SMI# signal).	
STPCLK#				Point-to-point connection to the ICH4 (STPCLK# signal).	
TEST[3:1]	1 K Ω pull-down to GND (default: no stuff)			For each signal, stuffing option for pull-down should be provided for testing purposes. For normal operation, leave the resistors unpopulated.	

Table 137. Connection Recommendations (Sheet 3 of 3)

Pin Name	System Pull-up/Pull-down	Series Termination	Voltage Translation	Notes	✓
THERMTRIP#	56 Ω pull-up to V_{CCP}	56 Ω from pull-up to the ICH4 pin		Point-to-point connection to an ICH4 (THERMTRIP# signal), with pull-up and series resistors placed by ICH4. THERMTRIP# is a V_{CCP} signal. When connecting to device other than an ICH4, voltage translation logic may be required.	
$V_{CC}[72:1]$	Connect to CPU_CORE			From Intel® IMVP-IV specification power supply.	
$V_{CCA}[3:0]$	Connect to V_{1P8}				
$V_{CC1_05}[25:1]$	Connect to V_{CCP}				
$V_{CCSENSE}$, $V_{SSSENSE}$	54.9 $\Omega \pm 1\%$ pull-down to GND (Default: no stuff)			For each signal, stuffing option for pull-down should be provided for testing purposes. Also, a test point for differential probe ground should be placed between the two resistors. For normal operation, leave the resistors unpopulated.	
GND[192:1]	Connect to GND				

Figure 179 illustrates the routing illustration for INIT# for the Celeron M processor.

Figure 179. Routing Illustration for INIT# for the Intel® Celeron® M Processor

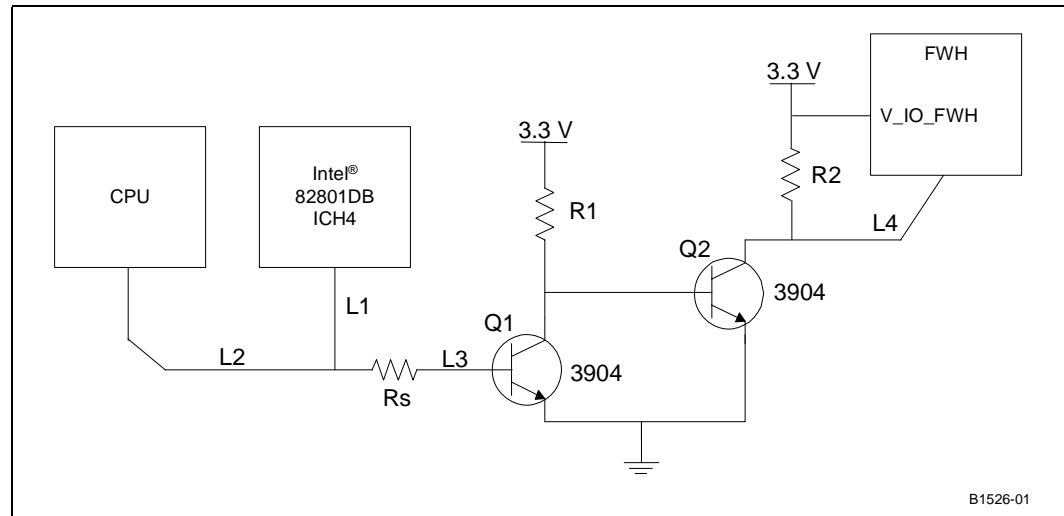
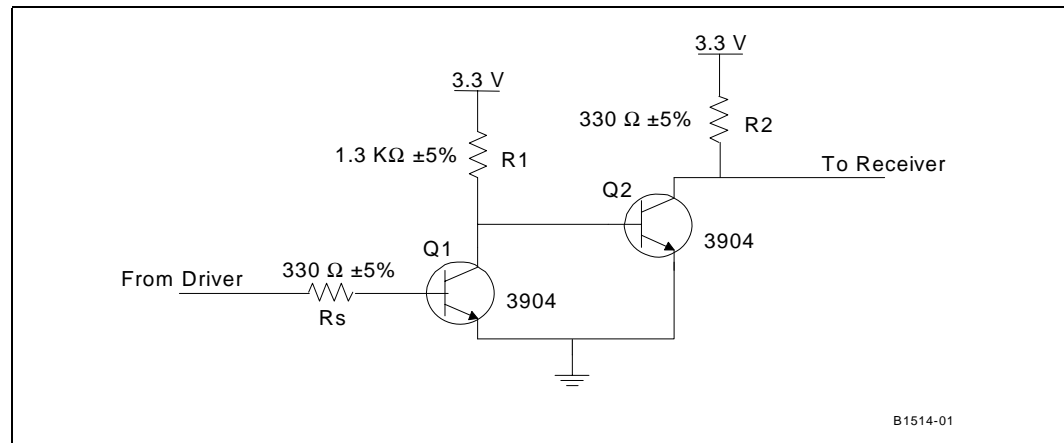


Figure 180 illustrates the voltage translation circuit for PROCHOT# for the Celeron M Processor.

Figure 180. Voltage Translation Circuit for PROCHOT# for the Intel® Celeron® M Processor



16.3.2 In Target Probe (ITP) Checklist

Refer to the latest revision of the *ITP700 Debug Port Design Guide* for details on the implementation of the debug port. The document can be found from <http://developer.intel.com/design/Xeon/guides/249679.htm>

16.3.3 Decoupling Recommendations

16.3.3.1 V_{CCP} (I/O)

Table 138 presents the V_{CCP} (I/O) decoupling recommendations.

Table 138. V_{CCP} (I/O) Decoupling Recommendations

Description	C, μ F	ESR, m Ω	ESL, nH	Notes	✓
Low Frequency Decoupling (Polymer Covered Tantalum - POSCAP, Neocap, KO Cap)	2 x 150 μ F	42 m Ω (typ)/2	2.5 nH/2	Refer to the Intel® Celeron® M Processor Datasheet for more information.	
High Frequency Decoupling (0603 MLCC, >= X7R)	10 x 0.1 μ F	16 m Ω (typ)/10	0.6 nH/10		

16.3.3.2 V_{CCA} (PLL)

Table 139 presents the V_{CCA} (PLL) decoupling recommendations.

Table 139. V_{CCA} (PLL) Decoupling Recommendations

Description	C, μ F	Notes	✓
Mid Frequency Decoupling (Polymer Covered Tantalum - POSCAP, Neocap, KO Cap)	4 x 10 μ F	Place one 10 μ F and one 0.01 μ F for each V_{CCA} pin.	
High Frequency Decoupling (0603 MLCC, >= X7R). Place next to the Celeron M.	4 x 0.01 μ F	Place one 10 μ F and one 0.01 μ F for each V_{CCA} pin.	

16.3.3.3 V_{CC} (CORE)

Table 140 presents the V_{CC} (CORE) decoupling recommendations.

Table 140. V_{CC} (CORE) Decoupling Recommendations (Sheet 1 of 2)

Option	Description	C, μ F	ESR, m Ω	ESL, nH	✓
#1	Low-Frequency Decoupling (Polymer Covered Tantalum – POSCAP, Neocap, KO Cap)	12 x 150 μ F	36 m Ω (typ)/12	2.5 nH/12	

NOTES:

- Decoupling guidelines are recommendations based on Intel reference board design. The Intel Customer Reference Board uses option #4. This is the preferred recommendation for decoupling.
- When deciding on overall decoupling solution, customers may need to take layout and PCB board design into consideration.
- Option #4 is to be used with small footprint (100 mm² or less) 0.36 μ H \pm 20% inductors.

Table 140. V_{CC} (CORE) Decoupling Recommendations (Sheet 2 of 2)

Option	Description	C, μ F	ESR, m Ω	ESL, nH	✓
	Mid-Frequency Decoupling (0612 MLCC, X5R or better)	15 x 2.2 μ F	5 m Ω (typ)/15	0.2 nH/15	
#2	Low-Frequency Decoupling (1206 MLCC, X5R or better)	40x10 μ F	5 m Ω (typ)/40	1.2 nH/40	
	Mid-Frequency Decoupling (0612 MLCC, X5R or better)	15 x 2.2 μ F	5 m Ω (typ)/15	0.2 nH/15	
#3	Low Frequency Decoupling (Polymer Covered Aluminum – SP Cap, AO Cap)	5 x 330 μ F	15 m Ω (max)/5	3.5 nH/5	
	Low Frequency Decoupling (1206 MLCC, >= X5R)	25 x 10 μ F	5 m Ω (typ)/25	1.2 nH/25	
	Mid Frequency Decoupling (0612 MLCC, >= X5R)	15 x 2.2 μ F	5 m Ω (typ)/15	0.2 nH/15	
#4 (Note 1)	Low-Frequency Decoupling (Polymer Covered Aluminum – SP CAP, AO Cap)	4 x 220 μ F	12 m Ω (max)/4	3.5 nH/4	
	Mid-Frequency Decoupling (0805 MLCC>= X5R)	35 x 10 μ F	5 m Ω (typ)/35	0.6 nH/35	

NOTES:

- Decoupling guidelines are recommendations based on Intel reference board design. The Intel Customer Reference Board uses option #4. This is the preferred recommendation for decoupling.
- When deciding on overall decoupling solution, customers may need to take layout and PCB board design into consideration.
- Option #4 is to be used with small footprint (100 mm² or less) 0.36 μ H \pm 20% inductors.

16.4 CK-408 Clock Checklist

16.4.1 Connection Recommendations

Table 141. CK-408 Resistor Recommendations Checklist (Sheet 1 of 2)

Pin Name	System Pull-up/Pull-down	Series Resistor	Notes	✓
3V66[0] 3V66[1]		33 Ω	If the signal is NOT used, it should be left as NC (Not Connected) or connected to a test point. Two possible topologies for 3V66_1: Use directly for GMCH's DREFSSCLK Use as input to an SSC device with SSC output to GMCH's DREFSSCLK.	
3V66_[5:2]		33 Ω	The Intel board routes 3V66[2] (pin 21) to GCLKIN on GMCH. The other two signals route to ICH4 (CLK66) and AGP connector (AGPCLK)	

Table 141. CK-408 Resistor Recommendations Checklist (Sheet 2 of 2)

Pin Name	System Pull-up/Pull-down	Series Resistor	Notes	✓
BCLK[1:0]	Connect a $49.9\ \Omega \pm 1\%$ shunt source termination (R_t) resistor to GND for each signal on the processor side of the series resistor.	Connect 20-33 Ω series resistors to each clock signal.	Connect to CK_408.	
CPU[0], CPU[0]# CPU[1], CPU[1]# CPU[2], CPU[2]#	49.9 $\Omega \pm 1\%$ pull-down to gnd	33 Ω	Connect one pair to BCLK[1:0] pins on processor. Connect one pair to BCLK/CBCLK# pins on 852GM. If on-board ITP is implemented connect the third pair of clock signals for the ITP connector. Otherwise, it may be connected to ITP_CLK[1:0] pins on processor.	
DOT_48MHz		33 Ω	Connect to DREFCLK pin on 852GM.	
IREF	475 $\Omega \pm 1\%$ pull-down to gnd		Adjusts IREF to 2.32 mA	
MULT[0]	10 K Ω pull-up to Vcc3_3CLK			
PCI[6:0]		33 Ω	Connect to various PCI devices.	
PCIF[2], PCIF[1], PCIF[0]		33 Ω	Use one clock for Intel® 82801DB ICH4. Unused clock pins should be left as NC or connected to a test point.	
PWRDWN#	Terminate to Vcc3_3CLK through 1 k Ω resistor		ICH4 does not support S1M state.	
REF0		33 Ω	This is the 14.318 MHz clock reference signal for ICH4, SIO and LPC. Each receiver requires one 33 Ω series resistor.	
SEL[2]	1 k Ω - 20 k Ω pull-down to GND.		Configured for unbuffered mode.	
SEL[1:0]	<ul style="list-style-type: none"> SEL[0]: 1 kΩ - 20 kΩ pull up to VCC3_3CLK SEL[1]: 1 kΩ - 20 kΩ pull down to GND. 			
USB_48MHz		33 Ω	Connect to CLK48 on ICH4.	
XTAL_IN, XTAL_OUT	Terminate each pin to GND through a 10 pF $\pm 5\%$ capacitor		Connect to a 14.318 MHz crystal, placed within 500 mils of CK-408.	
VDD[7:0], VDDA	Connect to Vcc3_3		Refer to clock vendor datasheet for decoupling info.	
VSS[5:0], VSSA	Connect to GND			
VSSIREF	Connect to GND			

16.5 Intel® 852GM Chipset GMCH (82852GM) Checklist

16.5.1 System Memory

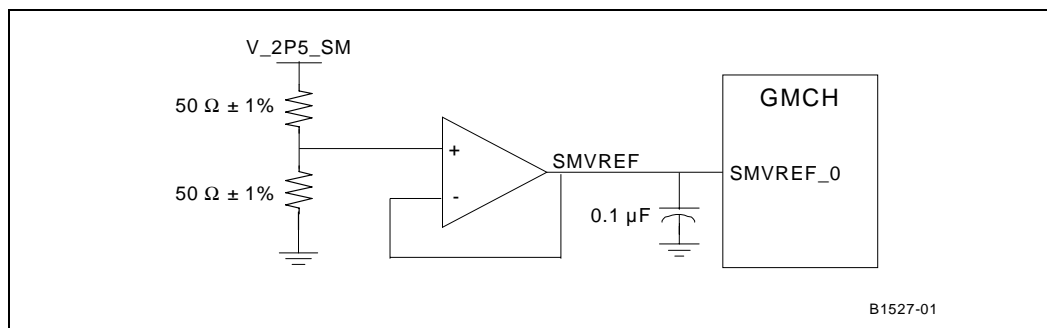
16.5.1.1 GMCH System Memory Interface Checklist

Table 142. GMCH System Memory Interface Checklist

Pin Name	System Pull-up/Pull-down	Series Resistor	Notes	✓
RCVENIN#			This signal should be routed to a via next to ball and left as a NC (No Connect).	
RCVENOUT#			This signal should be routed to via next to ball and left as a NC (No Connect).	
SBA[1:0], SCAS#, SRAS#, SWE#	56 Ω pull-up to Vcc1_25		Connect to DIMM0 and DIMM1.	
SCKE[1:0], SCS#[1:0]	56 Ω pull-up to Vcc1_25		Connect to DIMM 0	
SCKE[3:2], SCS#[3:2]	56 Ω pull-up to Vcc1_25		Connect to DIMM1	
SDQ[63:0], SDM[7:0], SDQS[7:0]	56 Ω pull-up to Vcc1_25	10 Ω	Connect to DIMM0 and DIMM1	
SDQ[71:64], SDM8, SDQS8			ECC detection is not supported. These signals should be left as NC	
SMA[12:6,3,0]	56 Ω pull-up to Vcc1_25		Connect to DIMM0 and DIMM1.	
SMA[5,4,2,1] SMAB[5,4,2,1]	56 Ω pull-up to Vcc1_25		Use SMA[5,4,2,1] for DIMM0; use SMAB[5,4,2,1] for the DIMM1.	
SCK0, SCK0# SCK1, SCK1# SCK2, SCK2#			These clock signals connect differentially to DIMM 0.	
SCK3, SCK3# SCK4, SCK4# SCK5, SCK5#			These clock signals connect to DIMM 1.	
SMVREF_0	Resistor Divider to VccSus2_5 consists of two identical resistors (50 Ω -150 $\Omega \pm 1\%$) Intel board uses 49.9 Ω .		Signal voltage level = VccSus2_5/2. A buffer is used to provide the necessary current and reference voltage to SMVREF. Place a 0.1 μ F cap by GMCH, DIMM0 and DIMM1 pins. Power must be provided during S3. Refer to Figure 181	
SMVSWINGL	604 Ω 1% pull-up to VccSus2_5 150 Ω 1% pull-down to gnd		Signal voltage level = 1/5 * VccSus2_5. Need 0.1 μ F cap at GMCH pin.	
SMVSWINGH	150 Ω 1% pull-up to VccSus2_5 604 Ω 1% pull-down to gnd		Signal voltage level = 4/5 * VccSus2_5. Need 0.1 μ F cap at GMCH pin.	
SMRCOMP	60.4 Ω 1% pull-up to VccSus2_5 60.4 Ω 1% pull-down to gnd		Signal voltage level = 1/2 * VccSus2_5 Need 0.1 μ F cap by the voltage divider.	

Figure 181 illustrates the reference voltage level for SMVREF.

Figure 181. Reference Voltage Level for SMVREF



16.5.1.2 DDR DIMM Interface Checklist

Table 143. DDR DIMM Interface Checklist

Pin Name	Configuration	Notes	✓
VREF[pin 1]		Signal voltage level = $V_{ccSus2_5} / 2$. Place a 0.1 uF cap by GMCH, DIMM0 and DIMM1	
VDD[9:1]	Connect to VccSus2_5.	Power must be provided during S3.	
VDDSPD	Connect to Vcc2_5.		
VDDQ[16:1]	Connect to VccSus2_5.		
SA[2:1]	Connect to GND.	These lines are used for strapping the SPD address for each DIMM.	
SA0	DIMM 0: Connect to GND. DIMM 1: Connect to VccSus2_5.		
VSS[22:1]	Connect to GND.		
RESET(DU)		Signal may be left as NC (Not Connected).	
SDA/SCL	Connect to Intel® 82801DB ICH4 SMBUS and SMLINK through isolation circuitry.		
VDDID		Signal may be left as NC (Not Connected).	
DU[4:1]		Signal may be left as NC (Not Connected).	
GND[1:0]		Signal may be left as NC (Not Connected).	
A13, CS[3:2]#, BA2, WP, FETEN		Signal may be left as NC (Not Connected).	
NC [4:1]		Signal may be left as NC (Not Connected).	

16.5.1.3 DIMM Decoupling Recommendation Checklist

Table 144. DIMM Decoupling Recommendation Checklist

Pin Name	F	Qty	Notes	✓
V_1P25_MEMVTT	0.1μF 4.7μF 470μF	55 3 4	Place one 0.1μF cap close to every two pull up resistors terminated to V_1P25_MEMVTT (VTT for DDR signal termination. Place two 4.7μF caps at either end of the VTT island and one near the center. Four 470μF caps may be placed as bulk decoupling	
VccSus2_5	0.1μF 220μF 100μF	15 3 1	A minimum of nine high frequency caps are recommended to be placed between the DIMMS. A minimum of four low frequency caps are required.	

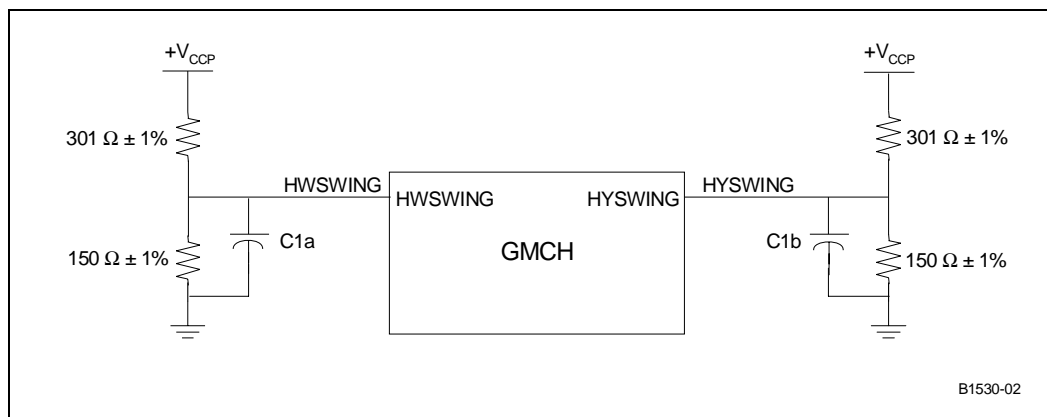
16.5.2 Front Side Bus (FSB) Checklist

Table 145. Front Side Bus (FSB) Checklist

Pin Name	System Pull-up/Pull-down	Notes	✓
HXSWING, HYSWING	301 Ω 1% pull-up to VCCP 150 Ω 1% pull-down to GND	Signal voltage level = 1/3 of VCCP. C1a = 0.1μF C1b=0.1μF Trace should be 10-mil wide with 20-mil spacing. See Figure 182 for more information.	
HXRCOMP, HYRCOMP	27.4 Ω 1% pull down to GND	One pulled-down resistor per pin. Trace should be 10-mil wide with 20-mil spacing.	
HDVREF[2:0]	49.9 Ω 1% pull-up to VCCP 100 Ω 1% pull-down to GND	Signal voltage level = 2/3 of VCCP. Need one 0.1μF cap and one 1μF cap for voltage divider.	
HAVREF	49.9 Ω 1% pull-up to VCCP 100 Ω 1% pull-down to GND	Signal voltage level = 2/3 of VCCP. Need one 0.1μF cap and one 1μF cap for voltage divider.	
HCCVREF	49.9 Ω 1% pull-up to VCCP 100 Ω 1% pull-down to GND	Signal voltage level = 2/3 of VCCP. Need one 0.1μF cap and one 1μF cap for voltage divider.	

Figure 182 illustrates the Intel 852GM Chipset HXSWING and HYSWING reference voltage generation circuit.

Figure 182. Intel® 852GM Chipset HXSWING and HYSWING Reference Voltage Generation Circuit



16.5.3 Hub Interface Checklist

Table 146. Hub Interface Checklist

Pin Name	System Pull-up/Pull-down	Notes	✓
HL[10:0]		Connect to HI[10:0] pins on ICH4.	
HLSTB		Connect to HI_STB pin on ICH4.	
HLSTB#		Connect to HI_STB# pin on ICH4.	
HLVREF	Refer to Section 10.3 .	Signal voltage level = 0.35 V ± 8%.	
PSWING	Refer to Section 10.3 .	Signal voltage level = 2/3 of VCC1_2 or 0.8 V ± 8%.	
HLRCOMP	27.4 Ω ± 1% pull-up to Vcc1_2	Refer to Section 10.1 for more information.	

16.5.4 Graphics Interfaces Checklist

16.5.4.1 Low Voltage Digital Signalling (LVDS) Checklist

Table 147. LVDS Checklist

Pin Name	System Pull-up/Pull-down	Notes	✓
LIBG	1.5 k Ω 1% pull-down to GND		
IYAP[2:0]/ IYAM[2:0] IYBP[2:0]/ IYBM[2:0]		If any of these LVDS data pairs are unused, they may be left as "no connect."	
ICLKAP/ICLKAM ICLKBP/ICLKBM		If any of these LVDS clock pairs are not used, they may be left as "no connect."	
DDCPCLK,DDCPD ATA	2.2 k Ω to 10 k Ω pull up to 3.3 V if not used	LVDS Panel DDC Clock/Data pair to collect digital display EDID information.	
PANELVDDEN	100 k Ω pull down to GND	Used for LVDS Panel Power Control.	
PANELBKLTEN	100 k Ω pull down to GND	Used for LVDS Panel Backlight Enable.	
PANELBKLTCTL	100 k Ω pull down GND	Used for LVDS Panel Backlight Brightness Control.	

16.5.4.2 Digital Video Out (DVO) Checklist

Table 148. DVO Checklist (Sheet 1 of 2)

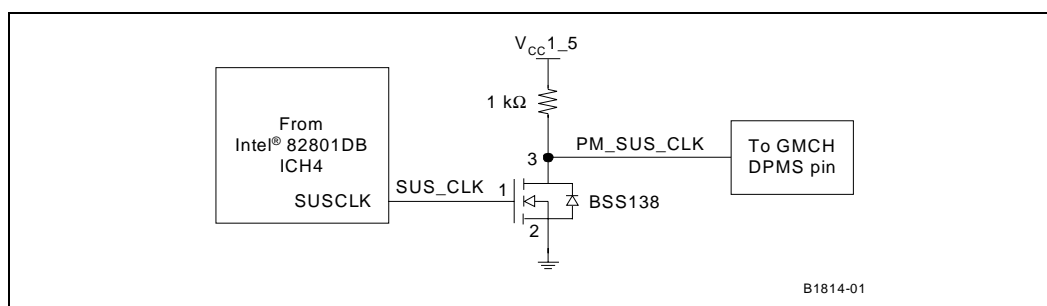
Pin Name	System Pull-up/Pull-down	Notes	✓
DVORCOMP	40.2 Ω 1% pull-down to GND	Trace should be 10-mil wide with 20-mil spacing.	
GVREF	1 K Ω 1% pull-up to Vcc1_5 1 K Ω 1% pull-down to GND	Signal voltage level = 1/2 of Vcc1_5. Need 0.1 μ F cap at GMCH pin.	
DVOC[11:0]		When unused, these signals may be left as NC.	
DVOCCLK, DVOCCLK#		When unused, these signals may be left as NC.	
DVOCHSYNC		When unused, these signals may be left as NC.	
DVOCVSYNC		When unused, these signals may be left as NC.	
DVOCBLANK#		When unused, these signals may be left as NC.	
DVOCFLDSTL	100 K Ω pull-down to GND	Pull-down resistor required only if signal is unused (10 K-100 K). It is up to DVO device to drive this signal.	
DVOBCINTR#	100 K Ω pull-up to Vcc1_5	Pull-up resistor required only if signal is unused (10 K-100 K). It is up to the DVO device to drive this signal.	
DVOBCCLKINT	100 K Ω pull-down to GND	Pull-down resistor required only if signal is unused (10 K-100 K). It is up to the DVO device to drive this signal.	

Table 148. DVO Checklist (Sheet 2 of 2)

Pin Name	System Pull-up/Pull-down	Notes	✓
MI2CCLK, MI2CDATA	2.2 K Ω pull-up to Vcc1_5	Pull-up resistor required on each signal even if they are unused (2.2 K-100 K). This signal is 1.5 V tolerant. It may require voltage translation circuit.	
MDVICLK, MDVIDATA	2.2 K Ω pull-up to Vcc1_5	Pull-up resistor required on each signal even if they are unused (2.2 K-100 K). This signal is 1.5 V tolerant. It may require voltage translation circuit.	
MDDCCLK, MDDCDATA	2.2 K Ω pull-up to Vcc1_5	Pull-up resistor required on each signal even if they are unused (2.2 K-100 K). This signal is 1.5 V tolerant. It may require voltage translation circuit.	
ADDID[6:0]		Connect to ADD slot if implemented. Otherwise, leave as NC.	
ADDID7	1 K Ω pull-down to GND if DVO device is onboard	Connect to ADD slot if implemented. When DVO device is onboard then implement pull-down. Other wise leave as NC.	
GCLKIN	33 Ω series at CK408	Connect to CK408, 66 MHz clock.	
DVODETECT		Leave as NC.	
DPMS		Connect to 1.5 V version of the ICH4's SUSCLK or a clock that runs during S1.	

Figure 183 illustrates the DPMS clock implementation.

Figure 183. DPMS Clock Implementation



16.5.4.3 Digital-to-Audio Converter (DAC) Checklist

Table 149. DAC Checklist (Sheet 1 of 2)

Pin Name	System Pull-up/Pull-down	In Series	Notes	✓
REFSET	124-137 Ω 1% pull-down to GND			
RED #	Connect to GND.		Need to connect to RED's return path.	
BLUE #	Connect to GND.		Need to connect to BLUE's return path.	
GREEN#	Connect to GND.		Need to connect to GREEN's return path.	

† Value used on Intel board.

Table 149. DAC Checklist (Sheet 2 of 2)

Pin Name	System Pull-up/Pull-down	In Series	Notes	✓
RED	On GMCH side of ferrite bead: 75 Ω 1% pull-down to GND, 3.3 pF cap to GND, ESD diode protection for Vcc1_5 On VGA side of ferrite bead: 3.3 pF cap to GND	Ferrite bead: 75 Ω at 100 MHz	Ferrite bead for EMI suppression between GMCH and VGA connector.	
BLUE	On GMCH side of ferrite bead: 75 Ω 1% pull-down to GND, 3.3 pF cap to GND, ESD diode protection for Vcc1_5. On VGA side of ferrite bead: 3.3 pF cap to GND	Ferrite bead: 75 Ω at 100 MHz	Ferrite bead for EMI suppression between GMCH and VGA connector.	
GREEN	On GMCH side of ferrite bead: 75 Ω 1% pull-down to GND, 3.3 pF cap to GND, ESD diode protection for Vcc1_5 On VGA side of ferrite bead: 3.3 pF cap to GND	Ferrite bead: 75 Ω at 100 MHz	Ferrite bead for EMI suppression between GMCH and VGA connector.	
HSYNC	33 pF cap to GND at connector (33 pF)	39 Ω	Unidirectional buffer is required. Refer to Section 8.1.6 for more information.	
VSYNC	33 pF cap to GND at connector (33 pF)	39 Ω	Unidirectional buffer is required. Refer to Section 8.1.6 for more information.	

† Value used on Intel board.

16.5.5 Miscellaneous Signal Checklist

Table 150. Miscellaneous Signals Checklist

Pin Name	System Pull-up/Pull-down	Notes	✓
EXTTS	10 kΩ 1% pull-up to Vcc3_3		
DPWR# (pin AA22)		Connect to DPWR# pin of Intel Celeron M Processor. Leave as NC for all other processors.	
LCLKCTLB	1 kΩ pull-up to Vcc3_3 for Intel 852GM GMCH.	Strap option for Mobile Intel Celeron Processor and Intel Celeron Processor. No strapping option should be used for Intel Celeron M processor. Used for SSC chip data control on Intel board. Leave as NC if not used.	
LCLKCTLA		Used for SSC chip data control on Intel board. Leave as NC if not used	
GST1, GST0	Leave as NC or 1 kΩ pull-up to Vcc1_5.	These pins have internal pull-down. See Table 151 for configuration options.	

Table 151. GST[2:0] Configurations

Straps Read Through HPLLCC[2:0]	FSB	DDR	GFx Core Clock Low	GFx Core Clock - High
00	400 MHz	266 MHz	n/a	133 MHz
10	400 MHz	200 MHz	n/a	133 MHz

16.5.6 GMCH Decoupling Recommendations Checklist

Table 152. GMCH Decoupling Recommendations Checklist (Sheet 1 of 2)

Pin Name	Configuration	F	Qty	Notes	✓
VCC[17:0]	Connect to VCC1_2S	0.1μF 150μF 10μF	4 2 1	Bulk decoupling is based on VR solutions used on board design.	
VTTLF[20:0]	Connect to VCC_CPU	0.1μF 150μF 10μF	2 1 1	Bulk decoupling is based on VR solutions used on board design.	
VTTHF[4:0]		0.1μF	5	Connect pins directly to caps.	
VCCHL[7:0]	Connect to VCC1_2S	0.1μF 10μF	2 1	Bulk decoupling is based on VR solutions used on board design.	
VCCSM[36:0]	Connect to VccSus2_5	0.1μF 150μF	11 2	Bulk decoupling is based on VR solutions used on board design.	

NOTE: Decoupling guidelines are recommendations based on our reference board design. Customers will need to take layout and PCB board design into consideration when deciding on overall decoupling solution.

Table 152. GMCH Decoupling Recommendations Checklist (Sheet 2 of 2)

Pin Name	Configuration	F	Qty	Notes	✓
VCCQSM[1:0]	Connect VccSus2_5 with filter network	0.1µF 4.7µF + 1 Ω	1 1 each	0.68 µH from power supply to GMCH pins. On GMCH side of inductor: one 0.1µF to GND, 4.7µF + 1 Ω to GND	
VCCASM[1:0]	Connect to VCC1_2S with filter network	0.1µF 100µF	1 1	1µH from power supply to GMCH pins, with caps on GMCH side of inductor.	
VCCDVO[15:0]	Connect to Vcc1_5	0.1µF 10µF 150µF	2 1 1	Bulk decoupling is based on VR solutions used on board design.	
VCCADAC[1:0]	Connect to Vcc1_5	0.01µF 0.1µF 220µF (no stuff)	1 1 1	Route VSSADAC to other side of the caps, then to ground. One 0 Ω 0805 resistor is recommended between the caps and Vcc1_5. This and the 220µF cap footprints are there in case there is noise issue with the VGA supply.	
VCCALVDS	Connect to Vcc1_5	0.1µF 0.01µF	1 1	Route VSSALVDS to other side of the caps, then to ground.	
VCCDLVDS[3:0]	Connect to Vcc1_5	0.1µF 22µF 47µF	1 1 1	Bulk decoupling is based on VR solutions used on board design.	
VCCTXLVDS[3:0]	Connect to Vcc2_5	0.1µF 22µF 47µF	3 1 1	Bulk decoupling is based on VR solutions used on board design. This power signal may be optionally connected to Vcc2_5 and powered off in S3.	
VCCGPIO	Connect to Vcc3	0.1µF 10µF	1 1	Bulk decoupling is based on VR solutions used on board design.	
VCCAHPLL	Connect to VCC1_2S	0.1µF	1		
VCCAGPLL	Connect to VCC1_2S	0.1µF	1		
VCCADPLLA	Connect to VCC1_2S with filter network	0.1µF 220µF	1 1	0.1µH from power supply to GMCH pins, with caps on GMCH side of inductor.	
VCCADPLLB	Connect to VCC1_2S with filter network	0.1µF 220µF	1 1	0.1µH from power supply to GMCH pins, with caps on GMCH side of inductor.	

NOTE: Decoupling guidelines are recommendations based on our reference board design. Customers will need to take layout and PCB board design into consideration when deciding on overall decoupling solution.

16.6 Intel® 82801DB I/O Controller Hub 4 (ICH4) Checklist

Note: Inputs to the ICH4 must not be left floating. Many GPIO signals are fixed inputs that must be pulled up to different sources.

16.6.1 PCI Interface and Interrupts

Table 153. PCI Interface and Interrupts Checklist

Pin Name	System Pull-up /Pull-down	Notes	✓
DEVSEL#	2.7 k Ω pull-up to V _{CC5} or 8.2 k Ω pull-up to V _{CC3_3}		
FRAME#	2.7 k Ω pull-up to V _{CC5} or 8.2 k Ω pull-up to V _{CC3_3}		
REQ[4:0]#, REQ[5]#/REQ[B]#/GPIO[1]	2.7 k Ω pull-up to V _{CC5} or 8.2 k Ω pull-up to V _{CC3_3}	Each signal requires a pull-up resistor.	
GPIO16 / GNTA#		GNTA is also used as a strap for top block swap. It is sampled on the rising edge of PWROK. By default, this signal is HIGH (strap function DISABLED). It may be enabled by a pull-down to gnd through a 1 k Ω resistor.	
IRDY#	2.7 k Ω pull-up to V _{CC5} or 8.2 k Ω pull-up to V _{CC3_3}		
PLOCK#	2.7 k Ω pull-up to V _{CC5} or 8.2 k Ω pull-up to V _{CC3_3}		
PERR#	2.7 k Ω pull-up to V _{CC5} or 8.2 k Ω pull-up to V _{CC3_3}		
SERR#	2.7 k Ω pull-up to V _{CC5} or 8.2 k Ω pull-up to V _{CC3_3}		
STOP#	2.7 k Ω pull-up to V _{CC5} or 8.2 k Ω pull-up to V _{CC3_3}		
TRDY#	2.7 k Ω pull-up to V _{CC5} or 8.2 k Ω pull-up to V _{CC3_3}		
PME#		Intel® 82801DB ICH4 has internal pull-up	
PCIRST#		47 Ω series at FWH	
APICCLK	Pull down to GND (if NOT Used).		
APICD[1:0]	10 k Ω pull-down to gnd (if NOT Used)	If XOR chain testing is NOT used: Pull down the signals through a shared 10 K Ω resistor. If XOR chain testing is used: Each signal requires a separate 10 k Ω pull-down resistor.	
IRQ[15:14]	8.2 k Ω pull-up to V _{CC3}	Each signal requires a pull-up resistor.	



Table 153. PCI Interface and Interrupts Checklist

Pin Name	System Pull-up /Pull-down	Notes	✓
PIRQ#[A:D] PIRQE#/GPIO2 PIRQF#/GPIO3 PIRQG#/GPIO4 PIRQH#/GPIO5	2.7 k Ω pull-up to V _{CC5} or 8.2 k Ω pull-up to V _{CC3_3}	External pull up is required for P_INT[A:D]#. External pull up is required when muxed signal (P_INT[E:H]#/ GPIO[2:5]) is implemented as PIRQ or GPIO.	
SER IRQ	10 k Ω pull-up to V _{CC3}		

16.6.2 General Purpose I/O (GPIO) Recommendations Checklist

Note: Ensure that ALL unconnected signals are OUTPUTS ONLY. GPIO[7:0] are 5 V tolerant.

Table 154. GPIO Checklist

Recommendations	✓
<p>GPIO[7:0]:</p> <ul style="list-style-type: none"> These pins are in the Main Power Well. Pull-ups must use the V_{CC3_3} plane. These pins are inputs only. They must not be allowed to float. Unused GPI must be pulled up to V_{CC3_3}. GPIO[1:0] may be used as REQ[B:A]#. GPIO[1] may be used as PCI REQ[5]#. GPIO[5:2] may be used as PIRQ[H:E]#. These signals are 5 V tolerant. 	
<p>GPIO[8] and [13:11]:</p> <ul style="list-style-type: none"> These pins are in the Resume Power Well. Pull-ups must use the V_{CCSUS3_3} plane. These pins are inputs only. They must not be allowed to float. Unused GPI must be pulled up to V_{3P3_STBY} These are the only GPIs that may be used as ACPI compliant wake events. GPIO[11] may be used as SMBALERT#. These signals are not 5V tolerant. 	
<p>GPIO[23:16]:</p> <ul style="list-style-type: none"> These pins are in the Main Power Well. Pull-ups, if required, must use the V_{CC3_3} plane. These pins are outputs only. Unused GPO may be left as NC. GPIO[17:16] may be used as GNT[B:A]#. GPIO[17] may be used as PCI GNT[5]#. These signals are not 5V tolerant. 	
<p>GPIO[28, 27, 25, 24]:</p> <ul style="list-style-type: none"> These pins are in the Resume Power Well. Pull-ups, if required, must use the V_{CCSUS3_3} plane. I/O pins. Default as outputs. Unused GPIO may be left as NC. These signals are not 5V tolerant. 	
<p>GPIO[43:32]:</p> <ul style="list-style-type: none"> These pins are in the Main Power Well. Pull-ups, if required, must use the V_{CC3_3} plane. I/O pins. Default as outputs These signals are not 5V tolerant. 	

16.6.3 SMBus System Management Interface Checklist

Table 155. SMBus Interface Checklist

Pin Name	System Pull-up/Pull-down	Notes	✓
INTRUDER#	100 kΩ pull-up to V _{CCRTC}	RTC well input requires pull-up (10 kΩ -100 kΩ) to reduce leakage from coin cell battery in G3.	

Table 155. SMBus Interface Checklist

Pin Name	System Pull-up/Pull-down	Notes	✓
SMBALERT#/GPIO[11]	10 k Ω pull-up to V _{CC} SUS3_3		
SMBCLK, SMBDATA, SMLINK[1:0]	Pull-up to V _{CC} SUS3_3	Require external pull-up resistors. Pull up value is determined by bus characteristics. board schematics use 10 k Ω pull-up resistors. The SMBus and SMLink signals must be connected together externally in S0 for SMBus 2.0 compliance: SMBCLK connected to SMLink[0] and SMBDATA connected to SMLink[1].	

16.6.4 AC'97 Interface Checklist

Table 156. AC'97 Interface Checklist

Pin Name	System Pull-up/Pull-down	Series Termination Resistor	Notes	✓
AC_BIT_CLK	None	33-47 Ω	The internal pull-down resistor is controlled by the AC'97 Global Control Register, ACLINK Shut Off bit: 1 = Enabled; 0 = Disabled When no AC'97 devices are connected to the link, BIOS must set the ACLINK Shut Off bit for the internal keeper resistors to be ENABLED. At that point, pull-ups/pull-downs are NOT needed on ANY of the link signals.	
AC_SDIN[2:0]	None	33-47 Ω	A series termination resistor is required for the PRIMARY CODEC. A series termination resistor is required for the SECONDARY and TERTIARY CODEC if the resistor is not found on CODEC.	
AC_SDOUT	None	33-47 Ω	A series termination resistor is required for the PRIMARY CODEC. One series termination resistor is required for the SECONDARY/ TERTIARY CODEC connector card if the resistor is not found on the connector card.	
AC_SYNC	None	33-47 Ω	A series termination resistor is required for the PRIMARY CODEC. One series termination resistor is required for the SECONDARY/ TERTIARY CODEC connector card if the resistor is not found on the connector card.	

16.6.5 Intel® 82801DB ICH4 Power Management Interface Checklist

Table 157. Intel® 82801DB ICH4 Power Management Interface Checklist

Pin Name	System Pull-up/Pull-down	Notes	✓
SLP_S3#, SLP_S4#, SLP_S5#		Signals driven by ICH4.	
PWRBTN#		Has integrated pull-up of 18 kΩ – 42 kΩ.	
PWROK	Weak pull-down to GND.	This signal should be connected to power monitoring logic and should go high no sooner than 10 ms after both Vcc3_3 and Vcc1_5 have reached their nominal voltages.	
RI#	8.2 kΩ pull-up to Vccsus3_3	If this signal is enabled as a wake event, it needs to be powered during a power loss event. If this signal goes low (active), when power returns the RI_STS bit will be set and the system will interpret that as a wake event.	
RSMRST#	Weak pull-down to GND.	RSMRST# is a RTC well input and requires pull-down to reduce leakage from coin cell battery in G3. Input must not float in G3. This signal should be connected to power monitoring logic and should go high no sooner than 10 ms after both Vcc3_3 and Vcc1_5 have reached their nominal voltages.	
THRM#	4.7 kΩ Pull-up to Vcc3_3 if TEMP SENSOR not used	External pull-up not required if connecting to temperature sensor.	
SYS_RESET#	22 kΩ pull-up to Vccsus3_3 if not actively driven.	This signal to ICH4 should not float. It needs to be at valid level all the time.	

16.6.6 FWH/LPC Interface Checklist

Table 158. FWH/LPC Interface Checklist

Pin Name	System Pull-up/Pull-down	Notes	✓
LAD[3:0]/FWH[3:0]/LDRQ[1:0]		No extra pull-ups required. Connect straight to FWH/LPC.	

16.6.7 USB Interface Checklist

Table 159. USB Interface Checklist

Pin Name	System Pull-up/Pull-down	Notes	✓
OC[5:0]#	10 k Ω pull-up to V3.3ALWAYS if not driven	No pull-up is required if signals are driven. Signals must NOT float if they are not being used.	
USBRBIAS, USBRBIAS#	22.6 Ω \pm 1% pull-down to GND	Connect signals together and pull down through a common resistor, placed within 500 mils of the Intel® 82801DB ICH4. Avoid routing next to clock pin.	

16.6.8 Intel® 82801DB ICH4 Hub Interface Checklist

Table 160. Intel® 82801DB ICH4 Hub Interface Checklist

Pin Name	System Pull-up/Pull-down	Notes	✓
HICOMP	48.7 Ω 1% pull-up to Vcc1_5	Place resistor within 0.5 inch of the Intel® 82801DB ICH4 pad using a thick trace.	
HIREF, HI_VSWING		HIREF signal voltage level = 0.35 V \pm 8%. HI_VSWING signal voltage level = 0.80 V \pm 8%. Three options are available for generating these references. Refer to Figure 10.3	
HI[11]	56 Ω pull-down to GND	HI[11] is not available on the GMCH.	

16.6.9 RTC Circuitry Checklist

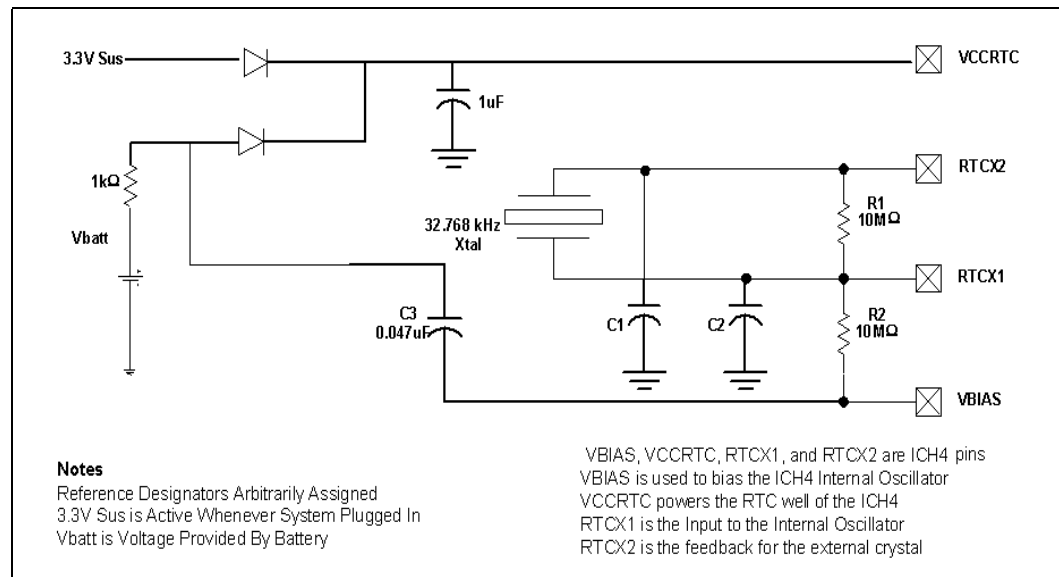
Table 161. RTC Circuitry Checklist

Pin Name	System Pull-up/Pull-down	In Series	Notes	✓
RTCRST#	22 k Ω pull-up to VccRTC and 1 μ F cap to GND		RTCRST# requires 18-25 ms delay. Use a 0.1 μ F cap to ground pull up with 22 K Ω resistor. Any resistor or capacitor combination that yields a time constant is acceptable.	
RTCX1, RTCX2			Connect a 32.768 KHZ crystal oscillator across these pins with a 10 M Ω resistor and a decoupling cap at each signal. Values for C1 and C2 are dependent on crystal. See http://www.intel.com/design/chipsets/applnnts/292276.htm , Note 1, and Figure 184 for more information.	
VBIAS		1 K Ω 0.047 μ F	Connect to RTCX1 through a 10 M Ω resistor. Connect to VBATT through a 1 k Ω in series with a 0.047 μ F capacitor. See Note 2 for more information.	

NOTES:

1. Voltage swing on RTCX1 pin should not exceed 1.0 V.
2. Recommendation for VBIAS 200 mV - 350 mV.

Figure 184. External Circuitry for the RTC



16.6.10 LAN Interface Checklist

Table 162. LAN Interface Checklist

Pin Name	System Pull-up/Pull-down	Notes	✓
LAN_CLK		Connect to LAN_CLK on the platform LAN Connect Device. If LAN interface is not used, leave the signal unconnected (NC).	
LAN_RST#	10 kΩ pull-down to GND if Intel® 82801DB ICH4 LAN not used	Timing Requirement: Signal should be connected to power monitoring logic, and should go high no sooner than 10 ms after both VccSus3_3 and VccSus1_5 have reached their nominal voltages. If the Intel® 82801DB ICH4 LAN controller is NOT used, pull LAN_RST# down through a 10 KΩ resistor. Refer to Figure 11.12.3	
LAN_RXD[2:0], LAN_TXD[2:0]		Connect to corresponding pins on platform LAN Connect Device. If LAN interface is not used, leave the signal unconnected (NC)	
LAN_RSTYSC		Connect to LAN_RSTSYNC on Platform LAN Connect Device. If LAN interface is not used, leave the signal unconnected (NC).	

16.6.11 Primary IDE Interface Checklist

Table 163. Primary IDE Interface Checklist

Pin Name	System Pull-up/Pull-down	Series Damping	Notes	✓
PDD[15:0]			These signals have integrated series resistors.	
PDA[2:0], PDCS1#, PDCS3#, PDDACK#, PDIOW#, PDIOR#			These signals have integrated series resistors. Pads for series resistors may be implemented should the system designer have signal integrity concerns.	
PDDREQ			These signals have integrated series resistors and pull-down resistors in Intel® 82801DB ICH4.	
PIORDY	4.7 kΩ pull-up to Vcc3_3		This signal has integrated series resistor in ICH4.	

16.6.12 Secondary IDE Interface Checklist

Table 164. Secondary IDE Interface Checklist

Pin Name	System Pull-up/Pull-down	Series Damping	Notes	✓
SDD[15:0]			These signals have integrated series resistors.	
SDA[2:0], SDCS1#, SDCS3#, SDDACK#, SDIOW#, SDIOR#			These signals have integrated series resistors. Pads for series resistors may be implemented should the system designer have signal integrity concerns.	
SDDREQ			These signals have integrated series resistors and pull-down resistors in Intel® 82801DB ICH4.	
SIORDY	4.7 kΩ pull-up to Vcc3_3		This signal has integrated series resistor in ICH4.	

16.6.13 Miscellaneous Signals Checklist

Table 165. Miscellaneous Signals Checklist

Pin Name	System Pull-up/Pull-down	Notes	✓
SPKR		SPKR is a strapping option for the TCO Timer Reboot function and is sampled on the rising edge of PWROK. An integrated weak pull-down is enabled only at boot/reset. Status of strap is readable via the NO_REBOOT bit (D31:F0, Offset D4h, bit 1): 1 = Disabled 0 = Enabled (normal operation) To disable, a jumper may be populated to pull SPCR high. Value of pull-up must be such that the voltage divider output caused by the pull-up, effective impedance of speaker and codec circuit, and internal pull-down will be read as logic high ($0.5 * V_{cc3_3}$ to $V_{cc3_3} + 0.5$)	
TP0	10 kΩ pull up to V _{CC} SUS3_3		

16.6.14 Intel® 82801DB ICH4 Decoupling Recommendations

Table 166. Intel® 82801DB ICH4 Decoupling Recommendations

Pin Name	Configuration	Value	Q	Notes	✓
VCC1_5	Connect to Vcc1_5.	0.1µF	2	Low frequency decoupling is dependent on layout and power supply design.	
VCCHI[3:0]	Connect to Vcc1_5.	0.1µF	2	Low frequency decoupling is dependent on layout and power supply design.	
VCC3_3	Connect to Vcc3_3.	0.1µF	6	Low frequency decoupling is dependent on layout and power supply design.	
V _{CC} SUS1_5	Connect to VccSUS1_5.	0.1µF	2	Low frequency decoupling is dependent on layout and power supply design.	
V _{CC} SUS3_3	Connect to VccSUS3_3	0.1µF	2	Low frequency decoupling is dependent on layout and power supply design.	
V5REF	Connect to V _{CC} through 1 KΩ.	0.1µF	1	Caps from V _{CC} 5REF to ground. Also connect diode from V _{CC} 5REF to Vcc3_3.	
V5REFSUS	Connect to VccSUS5_0 through 1 kΩ.	0.1µF	1	Caps from VCC5REFSUS to ground. Also connect diode from VCC5REFSUS to VccSus3_3	
V_CPU_IO	Connect to VCCP.	0.1µF 1µF	1 1		
VccPLL	Connect to Vcc1_5.	0.1µF 0.01µF	1 1		
VCCRTC	Connect to V_3P0_BAT_VREG.	0.1µF	1		

NOTE: All decoupling guidelines are recommendations based on our reference board design. Customers will need to take their layout, and PCB board design into consideration when deciding on their overall decoupling solution. Capacitors should be place less than 100 mils from the package.

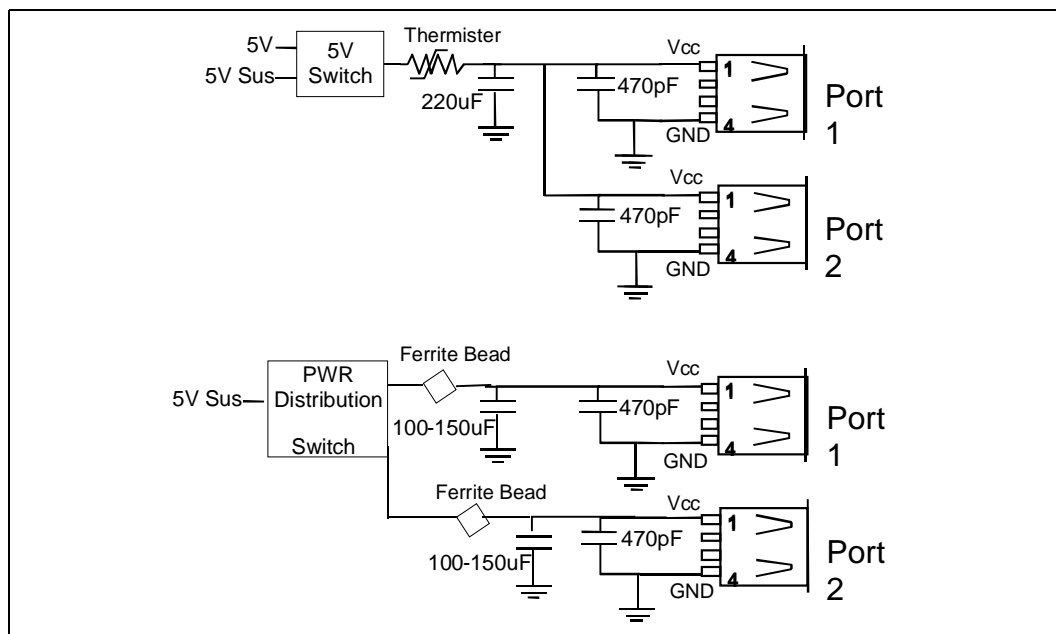
16.7 USB Power Checklist

16.7.1 Downstream Power Connection Checklist

Table 167. Downstream Power Connection Checklist

Pin Name	Notes	✓
USB_VCC[E:A]	One 220µF and two 470 pF are recommended for every two power lines. Either a thermistor or a power distribution switch (with short circuit and thermal protection) is required. See Figure 185 for more information.	

Figure 185. Good Downstream Power Connection



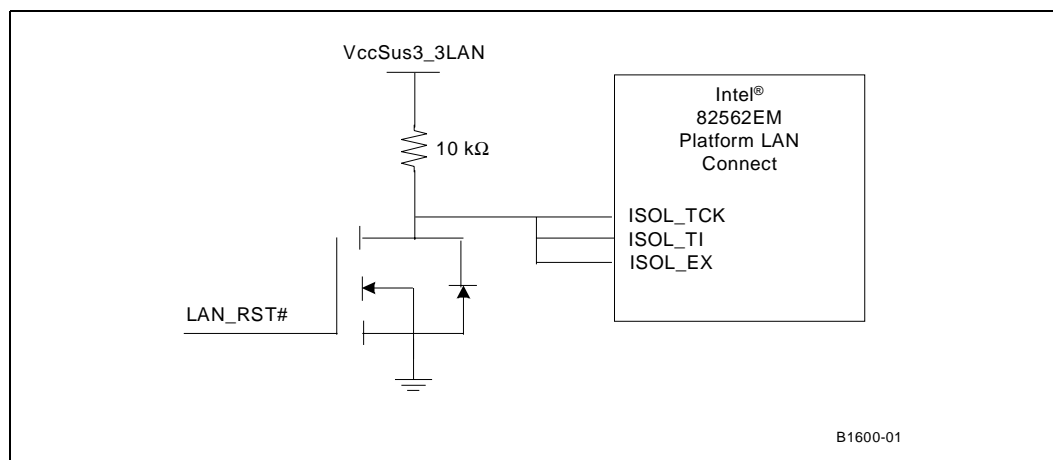
16.8 LAN Checklist

16.8.1 Resistor Recommendations Checklist for Intel® 82856ET/ Intel® 82562EM Platform LAN Connect Components

Table 168. Resistor Recommendations Checklist for Intel® 82856ET/Intel® 82562EM Platform LAN Connect Components

Pin Name	System Pull-up/Pull-down	Term Resistor	Notes	✓
ISOL_EX, ISOL_TCK, ISOL_TI	10 k Ω pull-up to VccSus3_3		If LAN is enabled, all three signals needs to be pulled up to VccSus3_3LAN through a common 10 K Ω pull-up resistor. See Figure 186 for more information.	
RBIAS10	562 $\Omega \pm 1\%$ pull-down to GND		The RBIAS values previously listed should be considered starting values. Intel recommends that board designers measure each of their PCB's output amplitude and then adjust the RBIAS values as required.	
RBIAS100	619 $\Omega \pm 1\%$ pull-down to GND		The RBIAS values previously listed should be considered starting values. Intel recommends that board designers measure each of their PCB's output amplitude and then adjust the RBIAS values as required.	
RDP, RDN		124 $\Omega \pm 1\%$	Connect 124 Ω resistor between RDP and RDN.	
TDP, TDN		100 $\Omega \pm 1\%$	Connect 100 Ω resistor between TDP and TDN.	
TESTEN	100 Ω pull-down to GND			
X1, X2			Connect a 25 MHz crystal across these two pins. 33 pF on each pin to ground.	
LAN_RST#			On board, the power monitoring logic waits for PM_PWROK to go high before deasserting this signal to enable the LAN device. It also keeps this signal high during S3. See Figure 186 for more information.	

Figure 186. LAN_RST# Design Recommendation



16.8.2 LAN Decoupling Recommendations Checklist

Table 169. LAN Decoupling Recommendations Checklist

Signal Name	Configuration	F	Qty	Notes	✓
VCC[2:1], VCCP[2:1], VCCA[2:1], VCCT[4:1]	Connect to VccSus3_3	0.1µF 4.7µF	8 2		
VCCR[2:1]	Connect to VccSus3_3 via filter	0.1µF 4.7µF 1000 pF	1 1 1	4.7µH from power supply to VCCR pins. Caps on VCCR side of the inductor.	