



Intel® 82870P2 PCI/PCI-X 64-bit Hub 2 (P64H2)

Thermal Design Guide

Intel® 82870P2 (P64H2) Thermal and Mechanical Design Guidelines

December 2002



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Revision History

Revision Number	Description	Date
-001	Initial Release	December 2002

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1 *Introduction*

As the complexity of computer systems increases, so do the power dissipation requirements. Care must be taken to ensure that the additional power is properly dissipated. Typical methods to improve heat dissipation include selective use of ducting, and/or passive heatsinks.

The goals of this document are to:

- Specify the operating limits of the Intel® 82870P2 PCI/PCI-X 64-bit Hub 2 (P64H2) components.
- Describe two reference thermal solutions that meet the thermal specifications of the Intel® 82870P2 PCI/PCI-X 64-bit Hub 2 (P64H2) component.

Properly designed solutions provide adequate cooling to maintain the P64H2 component die temperatures at or below thermal specifications. This is accomplished by providing a low local-ambient temperature, ensuring adequate local airflow, and minimizing the die to local-ambient thermal resistance. By maintaining the P64H2 component die temperature at or below the specified limits, a system designer can ensure the proper functionality, performance, and reliability of the chipset. Operation outside the functional limits can degrade system performance and may cause permanent changes in the operating characteristics of the component.

The simplest and most cost effective method is to improve the inherent system cooling characteristics through careful design and placement of fans, vents, and ducts. When additional cooling is required, component thermal solutions may be implemented in conjunction with system thermal solutions. The size of the fan or heatsink can be varied to balance size and space constraints with acoustic noise.

This document addresses thermal design and specifications for the P64H2 components only. For thermal design information on other chipset components, refer to the respective component datasheets. For the ICH3-S, refer to the *Intel® 82801CA I/O Controller Hub 3 (ICH3-S) Datasheet*. For the ICH4, refer to the *Intel® 82801DB I/O Controller Hub 4 (ICH4) Datasheet*.

The information on the thermal solutions design provided in this document is for reference only, and suggests good thermal design practices. All responsibility for determining the adequacy of any thermal or system design remains solely with the reader. Intel makes no warranties or representations that merely following all of the instructions presented in this document will result in a system with adequate thermal performance.

1.1 Definition of Terms

Term	Definition
BGA	Ball Grid Array. A package type, defined by a resin-fiber substrate, onto which a die is mounted, bonded and encapsulated in molding compound. The primary electrical interface is an array of solder balls attached to the substrate opposite the die and molding compound.
FC-BGA	Flip Chip Ball Grid Array. A packaging type defined by a resin-fiber substrate where a die is mounted using an underfilled C4 (controlled collapse chipset connection) attach style. The primary electrical interface is an array of solder balls attached to the substrate opposite the die. The device arrives at the customer with solder balls attached. This is the package technology used for the P64H2.
Intel® ICH3-S / Intel® ICH4	I/O Controller Hub. The chipset component that contains the primary PCI interface, LPC interface, USB, ATA-100, and other legacy functions.
MCH	Memory Controller Hub. The chipset component that contains the processor interface, the memory interface, and the hub interfaces.
Intel® P64H2	Bus Controller Hub. The chipset component that interfaces the PCI-X buses.
T_{case}	Maximum die temperature allowed. This temperature is measured at the geometric center of the top of the package die.
TDP	Thermal Design Power. Thermal solutions should be designed to dissipate this target power level.

1.2 Reference Documents

Document	Document Number / Location
<i>Intel® Xeon™ Processor Thermal Design Guidelines</i>	http://www.intel.com/design/Xeon/guides/298348.htm
<i>Intel® E7500/E7505 Chipset Thermal Design Guide</i>	http://developer.intel.com/design/chipsets/e7505/guides/298647.htm
<i>Intel® Xeon™ Processor with 512-KB L2 Cache and Intel® E7500 Chipset Platform Design Guide</i>	http://developer.intel.com/design/chipsets/e7500/guides/298649.htm
<i>Intel® E7500 Chipset: E7500 Memory Controller Hub (MCH) Datasheet</i>	http://developer.intel.com/design/chipsets/e7500/datashts/290730.htm
<i>Intel® Xeon™ Processor and Intel® E7505 Chipset: For use with Intel® Xeon™ Processors with 512-KB L2 Cache and Intel® Xeon™ Processors with 533 MHz System Bus Platform Design Guide</i>	http://developer.intel.com/design/chipsets/e7505/guides/251934.htm
<i>Intel® E7505 Chipset Memory Controller Hub (MCH) Datasheet</i>	http://developer.intel.com/design/chipsets/e7505/datashts/251932.htm
<i>Intel® 82801CA I/O Controller Hub 3 (ICH3-S) Datasheet</i>	http://developer.intel.com/design/chipsets/e7500/datashts/290733.htm
<i>Intel® 82801DB I/O Controller Hub 4 (ICH4) Datasheet</i>	http://developer.intel.com/design/chipsets/datashts/290744.htm
<i>Intel® 82870P2 PCI/PCI-X 64-bit Hub 2 (P64H2) Datasheet</i>	http://developer.intel.com/design/chipsets/e7500/datashts/290732.htm
Thermal Design Suggestions for various form factors	http://www.formfactors.org

NOTE: Contact your Intel Field Sales representative for further reference information.



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2 Packaging Technology

The P64H2 component uses a 31 mm, 6-layer FC-BGA package (see Figure 1, Figure 2, and Figure 3). For information on the ICH3-S package, refer to the *Intel® 82801CA I/O Controller Hub 3 (ICH3-S) Datasheet*. For information on the ICH4 package, refer to the *Intel® 82801DB I/O Controller Hub 4 (ICH4) Datasheet*.

Figure 1. Intel® P64H2 Package Dimensions (Top View)

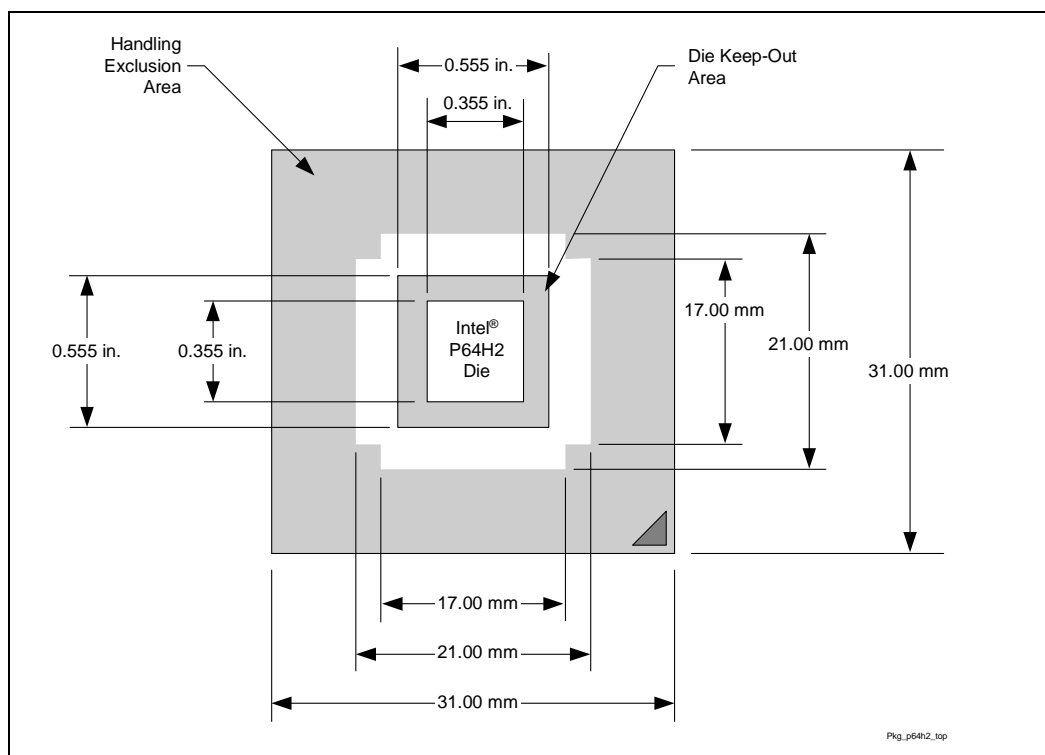
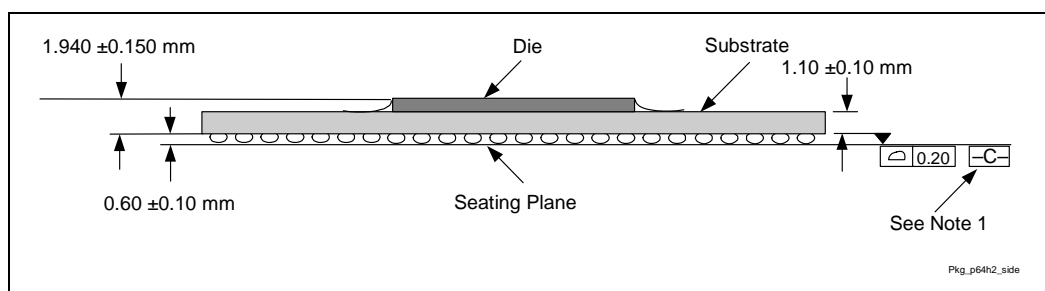


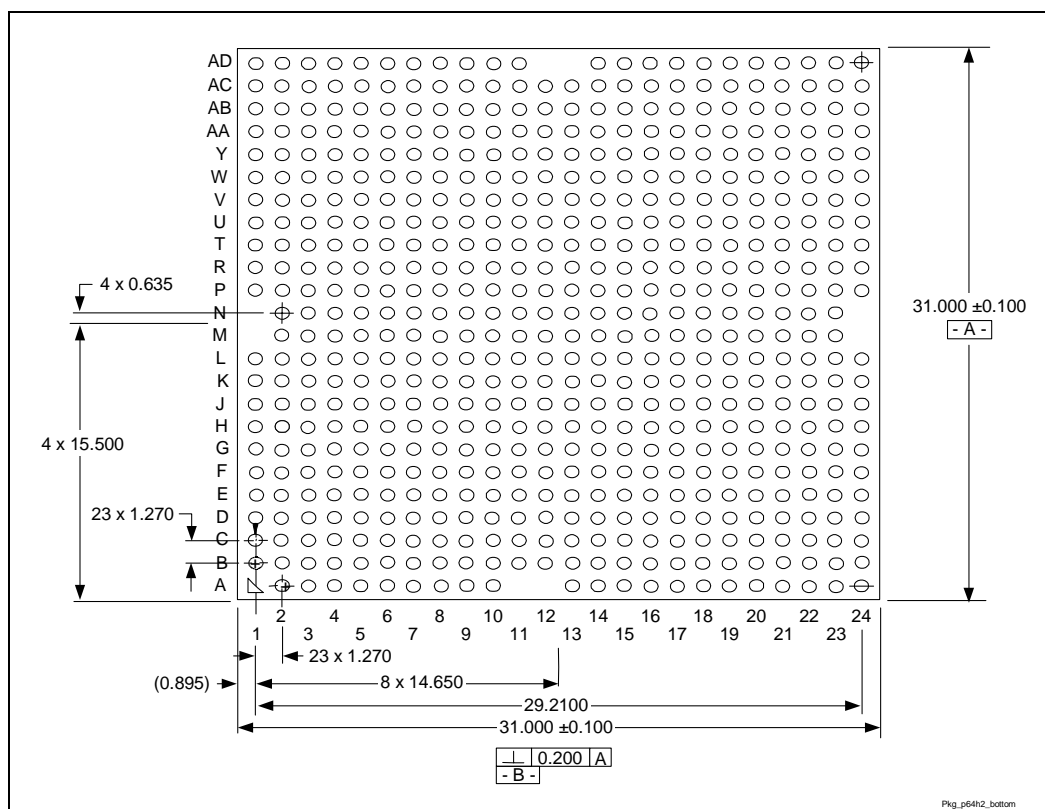
Figure 2. Intel® P64H2 Package Dimensions (Side View)



NOTES:

1. Primary datum –C– and seating plane are defined by the spherical crowns of the solder balls.
2. All dimensions and tolerances conform to ANSI Y14.5M–1982.

Figure 3. Intel® P62H2 Package Dimensions (Bottom View)



NOTES:

1. All dimensions are in millimeters.
2. All dimensions and tolerances conform to ANSI Y14.5M-1982.

3 Thermal Specifications

3.1 Case Temperature and Thermal Design Power

The P64H2 TDP specification is provided in Table 1 for the P64H2 component. FC-BGA packages have poor heat transfer capability into the board and have minimal thermal capability without thermal solutions. Intel recommends that system designers refer to Figure 4 to determine whether or not their systems' boundary conditions require a thermal solution on the P64H2.

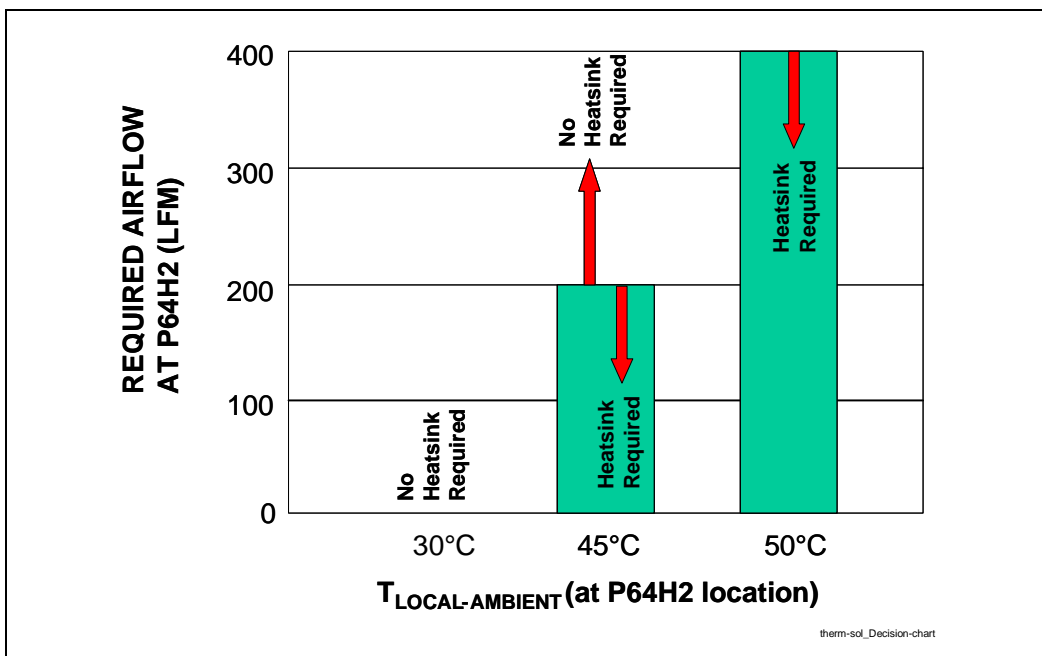
3.2 Die Temperature

To ensure proper operation and reliability of the P64H2 component, the die temperatures must be at or below the values specified in Table 1. System and/or component level thermal solutions are required to maintain die temperatures below the maximum temperature specification. Refer to Chapter 4 for guidelines on accurately measuring package die temperatures.

Table 1. Intel® P64H2 Thermal Specifications

Parameter	Maximum
T_{case}	105 °C
TDP	4.6 W

Figure 4. Intel® P64H2 Thermal Solution Decision Chart





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4 Thermal Metrology

The system designer must make temperature measurements to accurately determine the thermal performance of the system. To determine whether an attached thermal solution is required for the P64H2 component, the system integrator must measure the air temperature local to the component and compare corresponding airflow velocity to minimum airflow requirements. Intel has established guidelines for proper techniques to measure the P64H2 package die temperature described in Section 4.1.

4.1 Die Temperature Measurements

To ensure functionality and reliability, the T_{case} of the P64H2 must be maintained at or below the maximum temperature specifications as noted in Table 1. The surface temperature at the geometric center of the die corresponds to T_{case} . Measuring T_{case} requires special care to ensure an accurate temperature measurement.

Temperature differences between the temperature of a surface and the surrounding local ambient air can introduce errors in the measurements. The measurement errors could be due to a poor thermal contact between the thermocouple junction and the surface of the package, heat loss by radiation and/or convection, conduction through thermocouple leads, or contact between the thermocouple cement and the heatsink base (if a heatsink is used). To maximize measurement accuracy, only the 0° degree thermocouple attach approach is recommended.

4.1.1 Die Temperature Measurement without Attached Heatsink

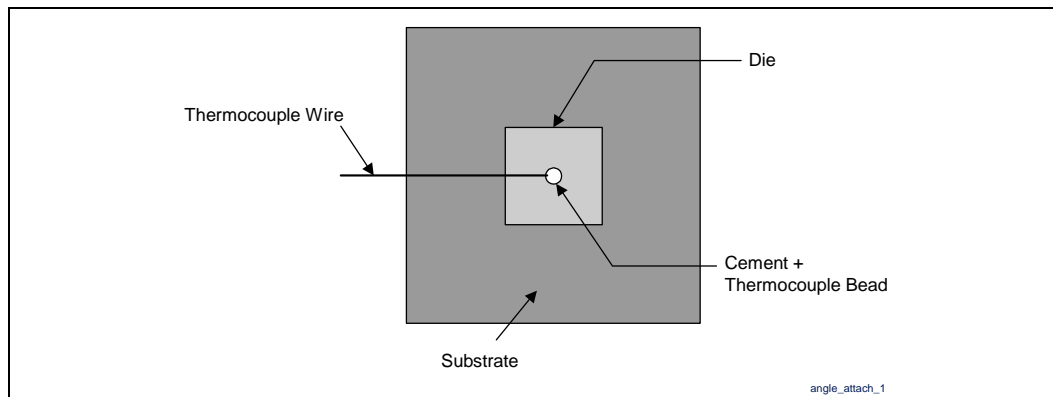
The following methodology is recommended to determine if system boundary conditions require a thermal solution as mentioned in Section 3.1.

Attach a 36 gauge or smaller calibrated K-type thermocouple bead or junction to the geometric center of the top surface of the die using a high thermal conductivity cement. *It is critical that the thermocouple bead makes contact with the die.*

4.1.2 Die Temperature Measurement with Attached Heatsink

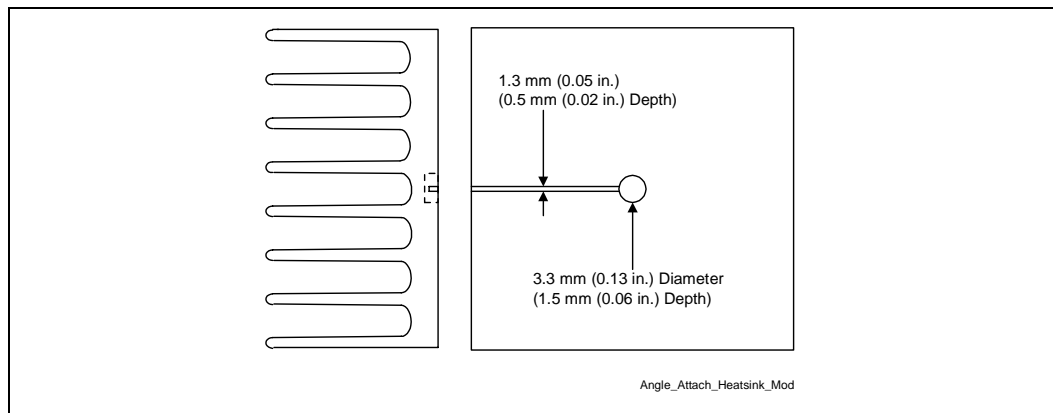
1. Mill a 3.3 mm (0.13 in.) diameter and 1.5 mm (0.06 in.) deep hole centered on the bottom of the heatsink base.
2. Mill a 1.3 mm (0.05 in.) wide and 0.5 mm (0.02 in.) deep slot from the centered hole to one edge of the heatsink. The slot should be parallel to the heatsink fins (see Figure 6).
3. Attach thermal interface material (TIM) to the bottom of the heatsink base.
4. Cut out portions of the TIM to make room for the thermocouple wire and bead. The cutouts should match the slot and hole milled into the heatsink base.
5. Attach a 36 gauge or smaller calibrated K-type thermocouple bead or junction to the center of the top surface of the die using high thermal conductivity cement. During this step, make sure no contact is present between the thermocouple cement and the heatsink base because any contact will affect the thermocouple reading. **It is critical that the thermocouple bead makes contact with the die** (see Figure 5).
6. Attach heatsink assembly to the P64H2 and route thermocouple wire out through the milled slot.

Figure 5. 0° Angle Attach Methodology (Top View)



NOTE: Not to scale.

Figure 6. 0° Angle Attach Heatsink Modifications



NOTE: Not to scale.

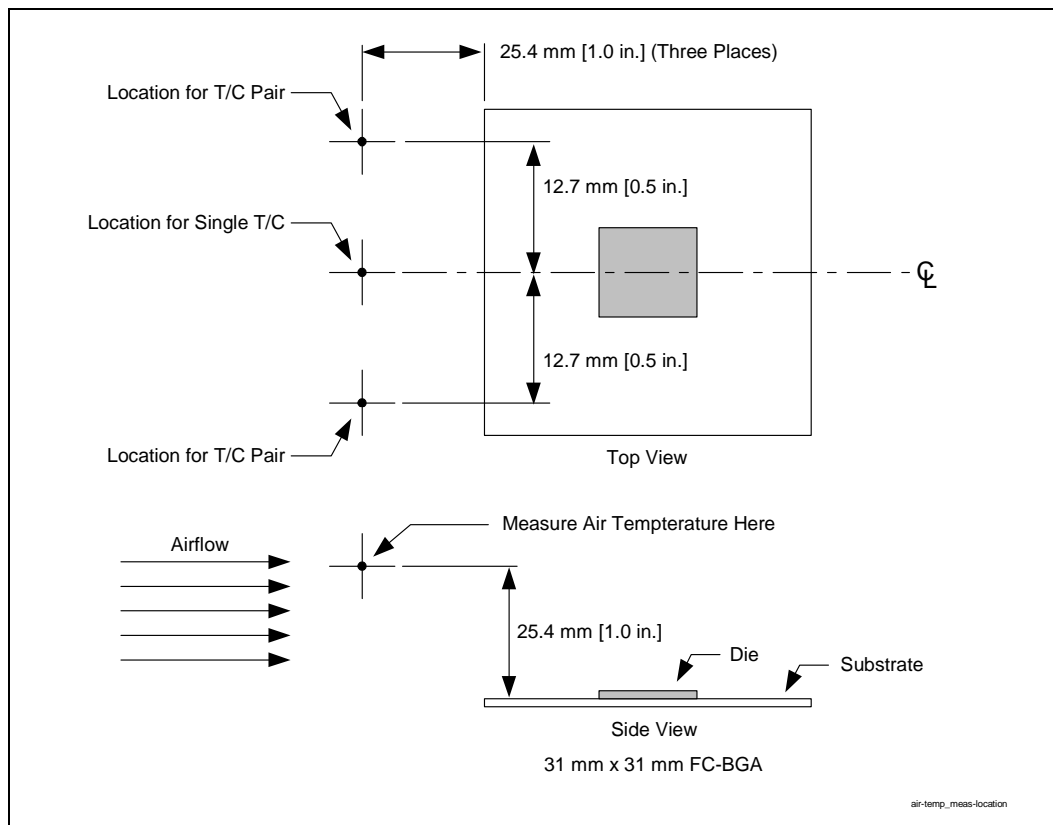
4.2 Air Temperature Measurements

Figure 7 describes the recommended location for air temperature measurements measured relative to the component. For a more accurate measurement of the average approach air temperature, Intel recommends averaging temperatures recorded from two thermocouples spaced about 25.4 mm (1.0 in.) apart. Locations for both a single thermocouple and a pair of thermocouples are presented.

4.3 Airflow Velocity Measurements

Airflow velocity should be measured using industry standard air velocity sensors. Typical airflow sensor technology may include hot wire anemometers. Airflow velocity measurement locations should correspond to the temperature measurement locations in Figure 7. Measurements should be taken with the chassis fully assembled in its operational configuration to achieve a representative airflow profile within the chassis.

Figure 7. Recommended Air Temperature Measurement Locations



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5 Reference Thermal Solutions

Intel has developed two reference thermal solutions designed to meet the cooling needs of the P64H2 under worst-case conditions. They are as follows:

1. A clip based thermal solution by attaching the reference heatsink to the P64H2 with the use of a strap clip to the motherboard (refer to Section 5.2)
2. A non-clip based thermal solution by attaching the reference heatsink to the P64H2 with the use of thermal adhesive tape on the back of the heatsink (refer to Section 5.3)

This chapter describes the overall requirements for the reference thermal solution including critical-to-function dimensions, operating environment, and validation criteria. Other chipset components may or may not need thermal solutions, depending on specific system local-ambient operating conditions. For the ICH3-S, refer to thermal specifications in the *Intel® 82801CA I/O Controller Hub 3 (ICH3-S) Datasheet*. For the ICH4, refer to thermal specifications in the *Intel® 82801DB I/O Controller Hub 4 (ICH4) Datasheet*.

5.1 Operating Environment

In certain system environments, the P64H2 component requires the use of an attached heatsink to meet thermal specifications. Table 2 lists the minimum local component airflow versus local-ambient temperature (T_a) for the P64H2 component without any attached thermal solution. For instances where the airflow falls below the minimum value, Intel recommends the use of an attached heatsink to extend the thermal capability of the component. Airflow velocity corresponding to T_a values that fall between the temperatures listed in Table 2 should not be interpolated by this table. Use the higher value of T_a for these cases. For example, a measured T_a of 48 °C corresponds to a minimum airflow of 400 LFM.

The data presented is based on thermal analysis and test of the Intel reference thermal solution, and actual data may vary depending on system configuration and thermal solution used. The user should always measure the package die temperature to ensure temperature specifications are met for a specific application.

Refer to Section 4, “Thermal Metrology”, for guidelines on measuring the component local-ambient temperature and airflow velocity.

Table 2. Minimum Airflow Requirements without Requiring Thermal Solution

Local-Ambient Temperature (T_a)	Minimum Airflow Velocity
30 °C	0 LFM
45 °C	200 LFM
50 °C	400 LFM

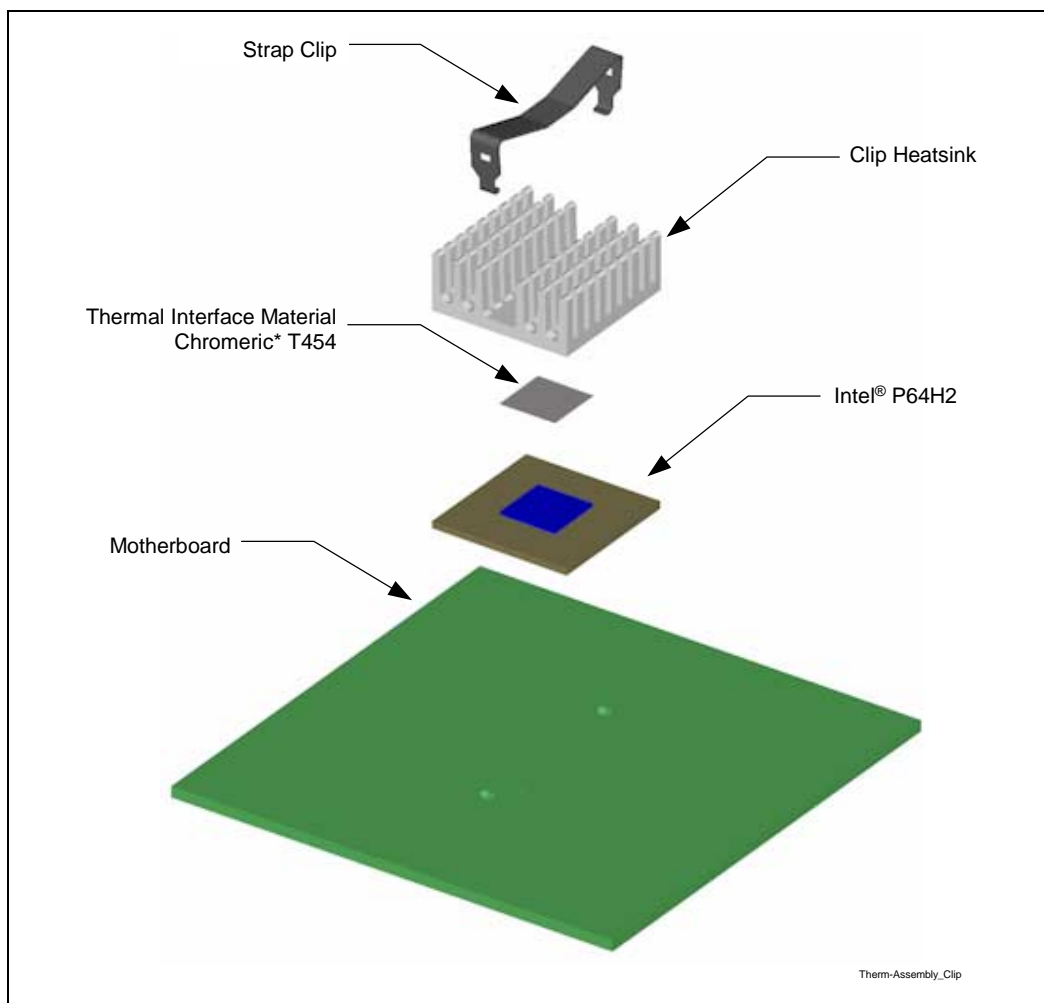
Note: Do Not Interpolate

5.2 Clip Heatsink Thermal Solution Assembly

This reference thermal solution is a passive extruded heatsink with thermal interfaces. It is attached using a strap clip designed to hook into holes on the motherboard. Figure 8 shows the reference thermal solution assembly and associated components.

Full mechanical drawings of this thermal solution assembly and the heatsink clip are provided in Appendix B. Appendix A contains vendor information for each thermal solution component.

Figure 8. Clip-Based Reference Thermal Solution Assembly

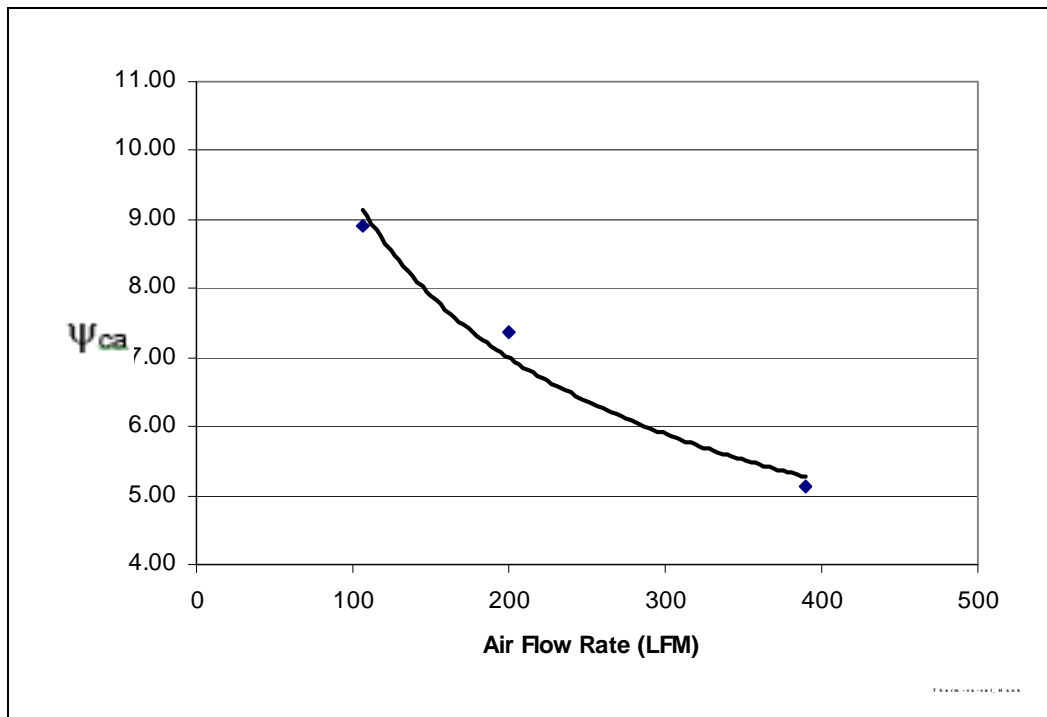


NOTE: Not to scale.

5.2.1 Heatsink Performance

Figure 9 shows the measured thermal performance of the clip heatsink solution versus airflow rate corrected to 5000' altitude.

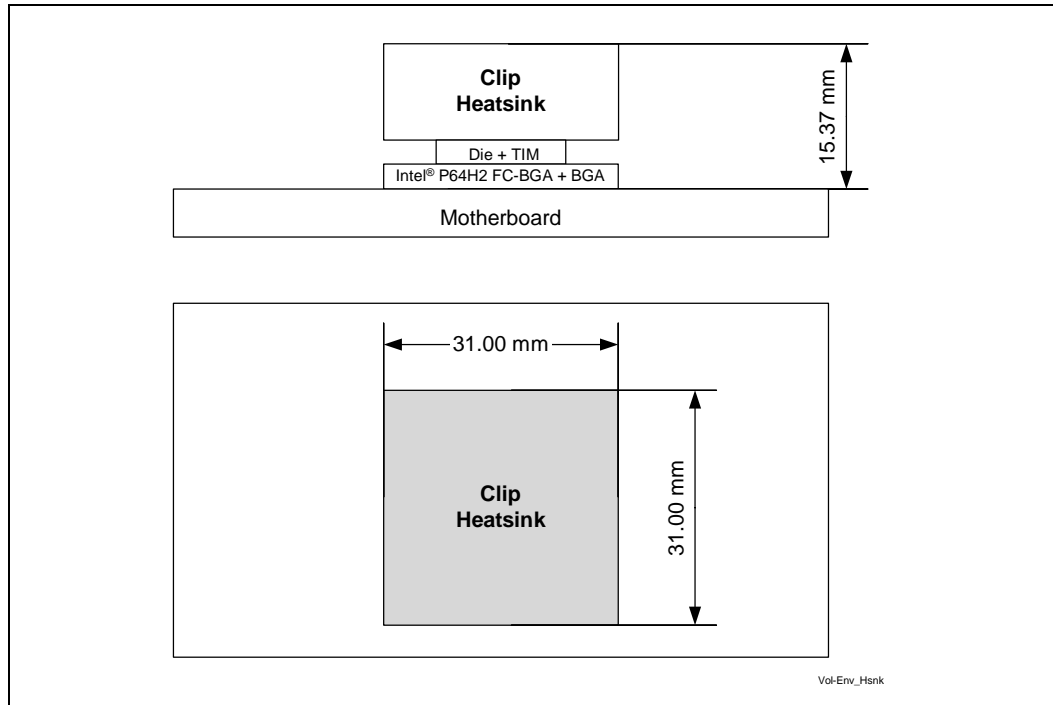
Figure 9. Intel® P64H2 Reference Clip Heatsink Measured Thermal Performance Versus Approach Velocity



5.2.2 Mechanical Design Envelope

Though each design may have unique mechanical volume and height restrictions or implementation requirements, the height, width, and depth constraints typically placed on the P64H2 thermal solution are shown in Figure 10.

Figure 10. Clip Heatsink Volumetric Envelope for the Intel® P64H2



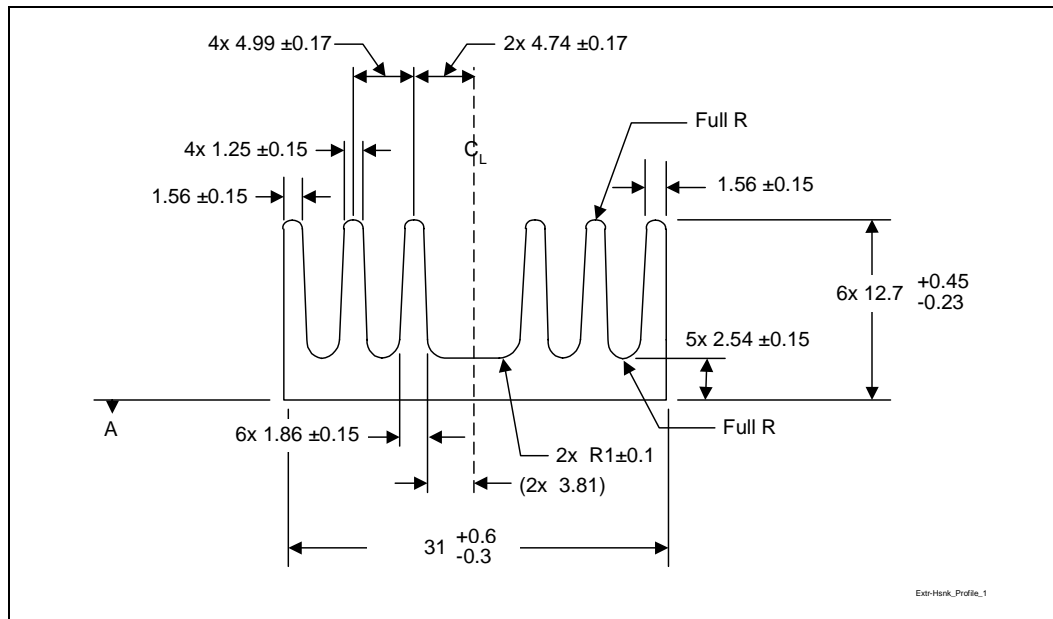
5.2.3 Heatsink Orientation

To enhance the efficiency of the reference thermal solution, it is important for the designer to orient the fins properly with respect to the mean airflow direction. Simulation and experimental evidence have shown that the P64H2 clip heatsink thermal performance is enhanced when the fins are aligned with the mean airflow direction (see Figure 12 and Figure 13). Aligning the heatsink 45° relative to the airflow is acceptable but delivers reduced thermal performance.

5.2.4 Extruded Heatsink Profile

The reference clip heatsink thermal solution uses an extruded heatsink for cooling the P64H2 component. Figure 11 shows the heatsink profile. Appendix A lists a supplier for this extruded heatsink. Other heatsinks with similar dimensions and increased thermal performance may be available.

Figure 11. Extruded Heatsink Profile



5.2.5 Thermal Interface Material

A thermal interface material provides improved conductivity between the die and heatsink. The clip heatsink reference thermal solution uses Chromerics' T454, 0.127 mm (0.005 in.) thick, 12.7 mm x 12.7 mm (0.5 in. x 0.5 in.) square.

5.2.6 Heatsink Clip

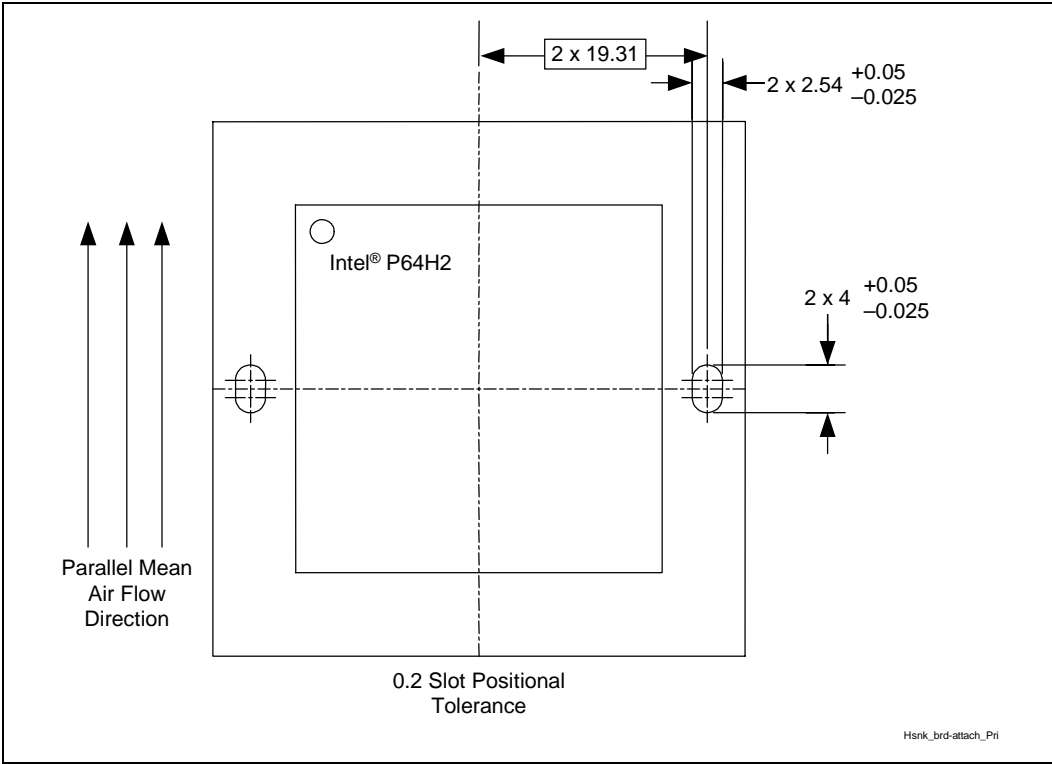
The clip heatsink reference solution uses a strap clip that is latched to two through holes on the motherboard. See Figure 21 in Appendix B for mechanical drawings of the clip.

5.2.7 Board-Level Components Keep-Out Dimensions

The locations of hole patterns and keep-out zones for the clip heatsink reference thermal solution are shown in Figure 12 and Figure 13.

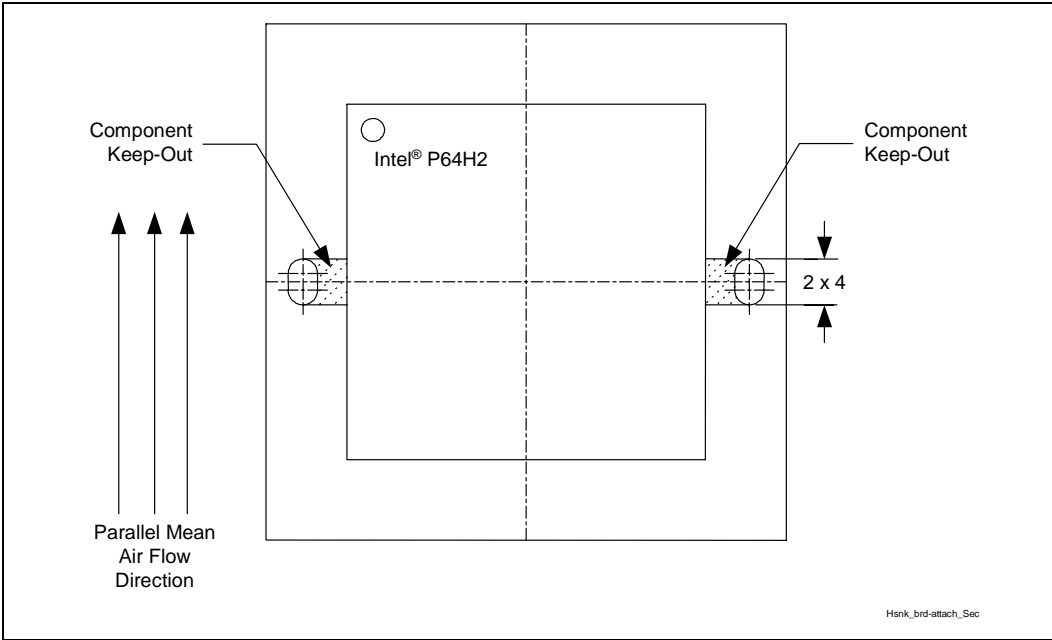


Figure 12. Clip Heatsink Board Attach Location and Keep-Outs (Primary Side)



NOTE: Dimensions are in millimeters.

Figure 13. Clip Heatsink Board Attach Location and Keep-Outs (Secondary Side)



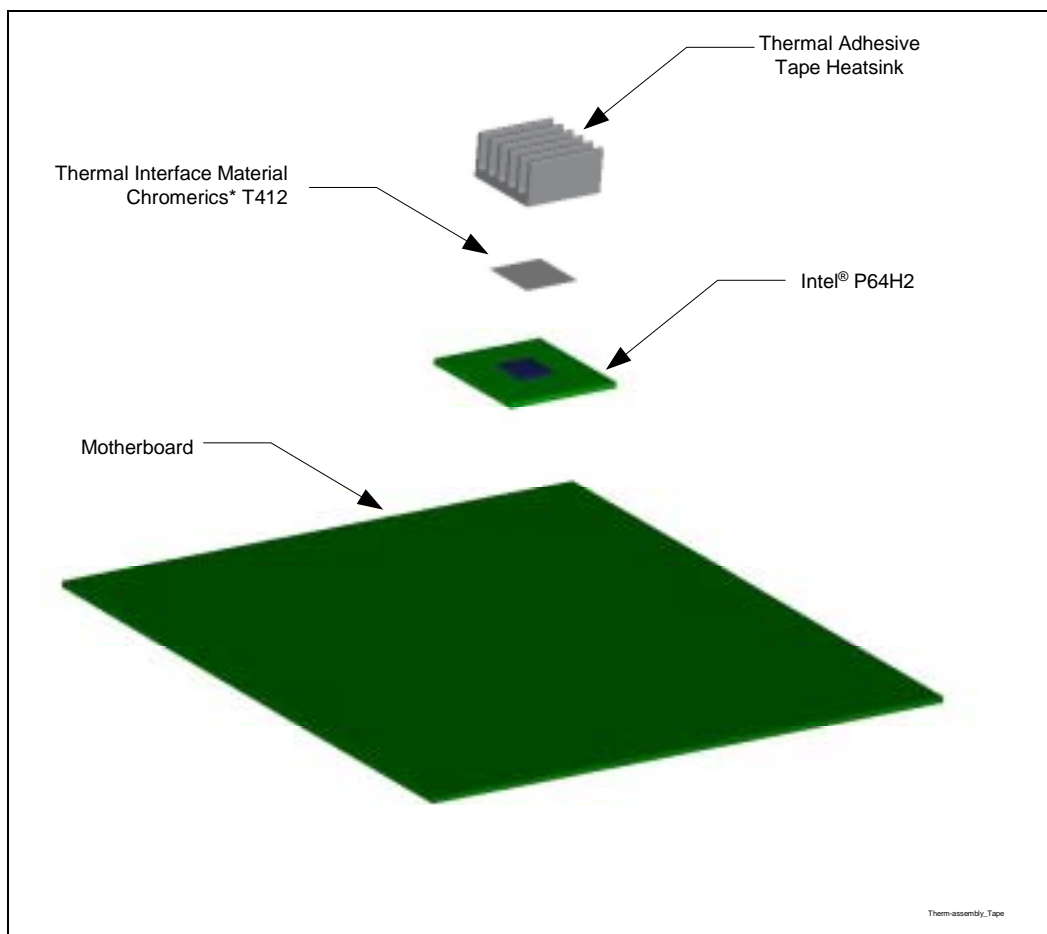
NOTE: Dimensions are in millimeters.

5.3 Thermal Adhesive Tape Heatsink Thermal Solution Assembly

This reference thermal solution is a passive extruded unidirectional heatsink with thermal interfaces. It is attached to the die of the P64H2 package. Figure 14 shows the reference thermal solution assembly and associated components.

Full mechanical drawings of this thermal solution assembly are provided in Appendix B. Appendix A contains vendor information for each thermal solution component.

Figure 14. Thermal Adhesive Tape-Based Reference Thermal Solution Assembly

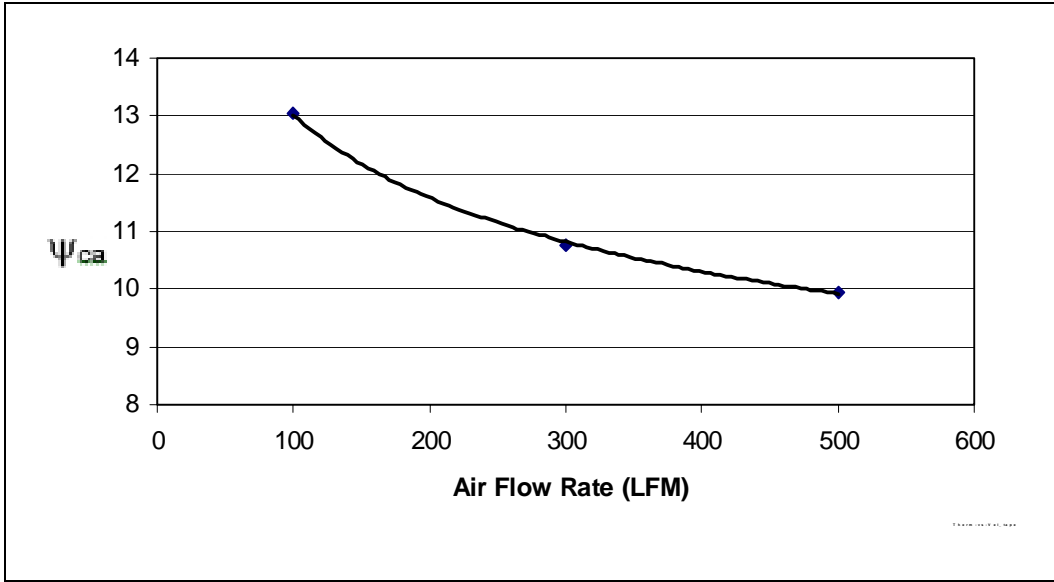




5.3.1 Heatsink Performance

Figure 15 shows the measured thermal performance of the thermal adhesive tape heatsink thermal solution versus airflow rate corrected to 5000’ altitude.

Figure 15. Intel® P64H2 Reference Thermal Adhesive Tape Heatsink Measured Thermal Performance Versus Approach Velocity

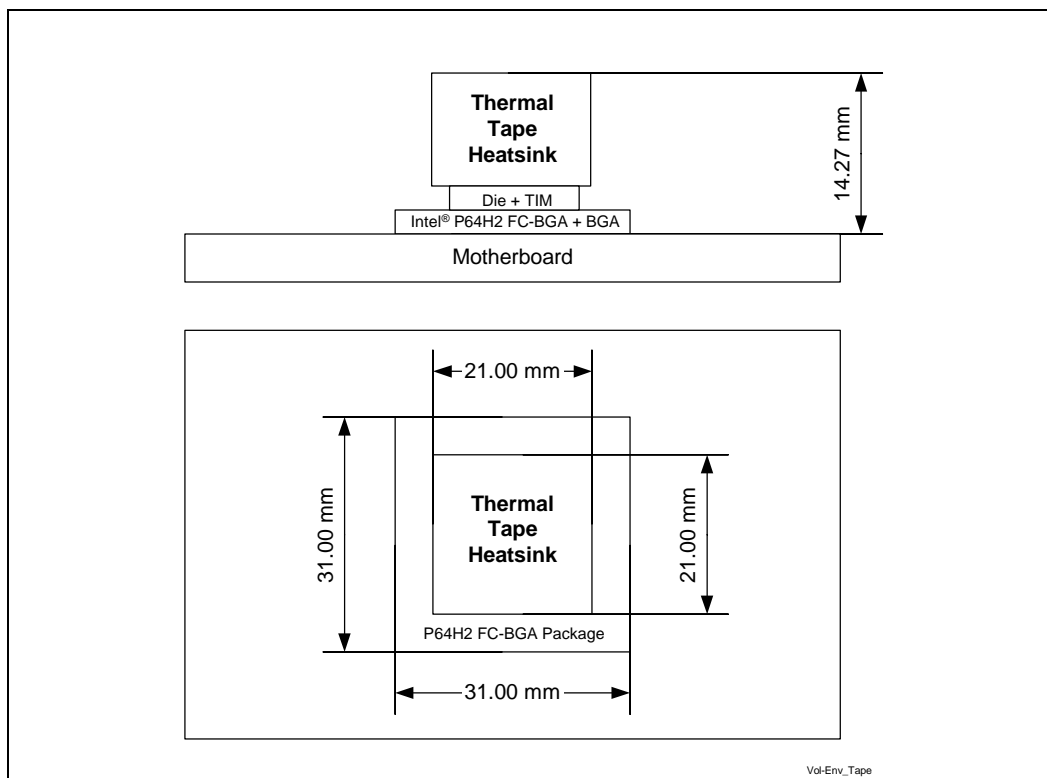


NOTE: Not to scale.

5.3.2 Mechanical Design Envelope

Though each design may have unique mechanical volume and height restrictions or implementation requirements, the height, width, and depth constraints typically placed on the P64H2 thermal adhesive tape heatsink thermal solution are shown in Figure 16.

Figure 16. Thermal Adhesive Tape Heatsink Volumetric Envelope for the Intel® P64H2



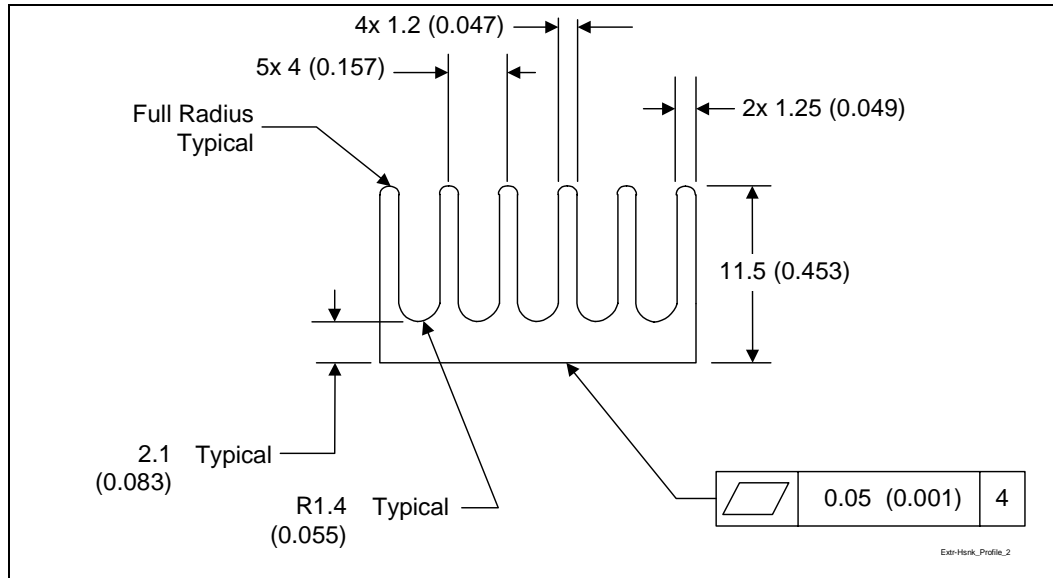
5.3.3 Heatsink Orientation

Since this solution is based on a unidirectional heatsink, mean airflow direction must be aligned with the direction of the fins of the heatsink.

5.3.4 Extruded Heatsink Profile

The reference thermal adhesive tape heatsink uses an extruded heatsink for cooling the P64H2. Figure 17 shows the heatsink profile. Appendix A lists a supplier for this extruded heatsink. Other heatsinks with similar dimensions and increased thermal performance may be available.

Figure 17. Extruded Heatsink Profile



5.3.5 Thermal Interface Material

A thermal interface material provides improved conductivity between the die and the heatsink. The thermal adhesive tape heatsink reference solution uses Chromerics' T412 0.23 mm (0.009 in.) thick, 15 mm x 15 mm (0.59 in. x 0.59 in.) square.

5.3.6 Heatsink Clip

There is no heatsink clip associated with this reference solution.

5.3.7 Board-Level Components Keep-Out Dimensions

There are no board-level component keep-out areas associated with this reference solution.

5.4 Reliability Guidelines

Each motherboard, heatsink and attach combination may vary the mechanical loading of the component. Based on the end user environment, the user should define the appropriate reliability test criteria and carefully evaluate the completed assembly prior to use in high volume. Some general recommendations are shown in Table 3.

Table 3. Reliability Guidelines

Test ¹	Test Profile	Pass/Fail Criteria ²
Mechanical Shock	50 g, board level, 11 msec, 3 shocks/axis	Visual Check and Electrical Functional Test
Random Vibration	7.3 g, board level, 45 min/axis, 50 Hz to 2000 Hz	Visual Check and Electrical Functional Test
Temperature Life	85 °C, 2000 hours total, checkpoints at 168, 500, 1000, and 2000 hours	Visual Check
Thermal Cycling	-5 °C to +70 °C, 500 cycles	Visual Check
Humidity	85% relative humidity, 55 °C, 1000 hours	Visual Check

NOTES:

1. It is recommended that the above tests be performed on a sample size of at least 12 assemblies from 3 lots of material.
2. Additional Pass/Fail Criteria may be added at the discretion of the user.



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Appendix A: Thermal Solution Component Suppliers

Table 4. Thermal Solution Component Suppliers

Part	Intel Part Number	Supplier	Contact Information
Clip Heatsink + TIM Assembly	a16412-001	CCI/ACK	Harry Lin 714-739-5797 hlinack@aol.com Monica Chih 866-2-29952666x131 monica_chih@ccic.com.tw
Clip Heatsink Attach Clip	729342-001	CCI/ACK	Harry Lin 714-739-5797 hlinack@aol.com Monica Chih 866-2-29952666x131 monica_chih@ccic.com.tw
Thermal Adhesive Tape Heatsink + TIM Assembly	a80409-002	Foxconn	Bob Hall 503-693-3509 x235 bhall@foxconn.com

Note: The enabled components may not be currently available from all suppliers. Contact the supplier directly to verify time of component availability.

Note: These vendors/devices/ are listed by Intel as a convenience to Intel's general customer base, but Intel does not make any representations or warranties whatsoever regarding quality, reliability, functionality, or compatibility of these devices. This list and/or these devices may be subject to change without notice.



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Appendix B: Mechanical Drawings

This appendix contains the following drawings:

- Clip Heatsink + TIM Assembly Drawing (Sheet 1 of 2)
- Clip Heatsink + TIM Assembly Drawing (Sheet 2 of 2)
- Clip Heatsink Drawing
- Clip Heatsink Attach Clip Drawing
- Thermal Adhesive Tape Heatsink Assembly Drawing
- Thermal Adhesive Tape Heatsink Drawing



Figure 18. Clip Heatsink + TIM Assembly Drawing (Sheet 1 of 2)

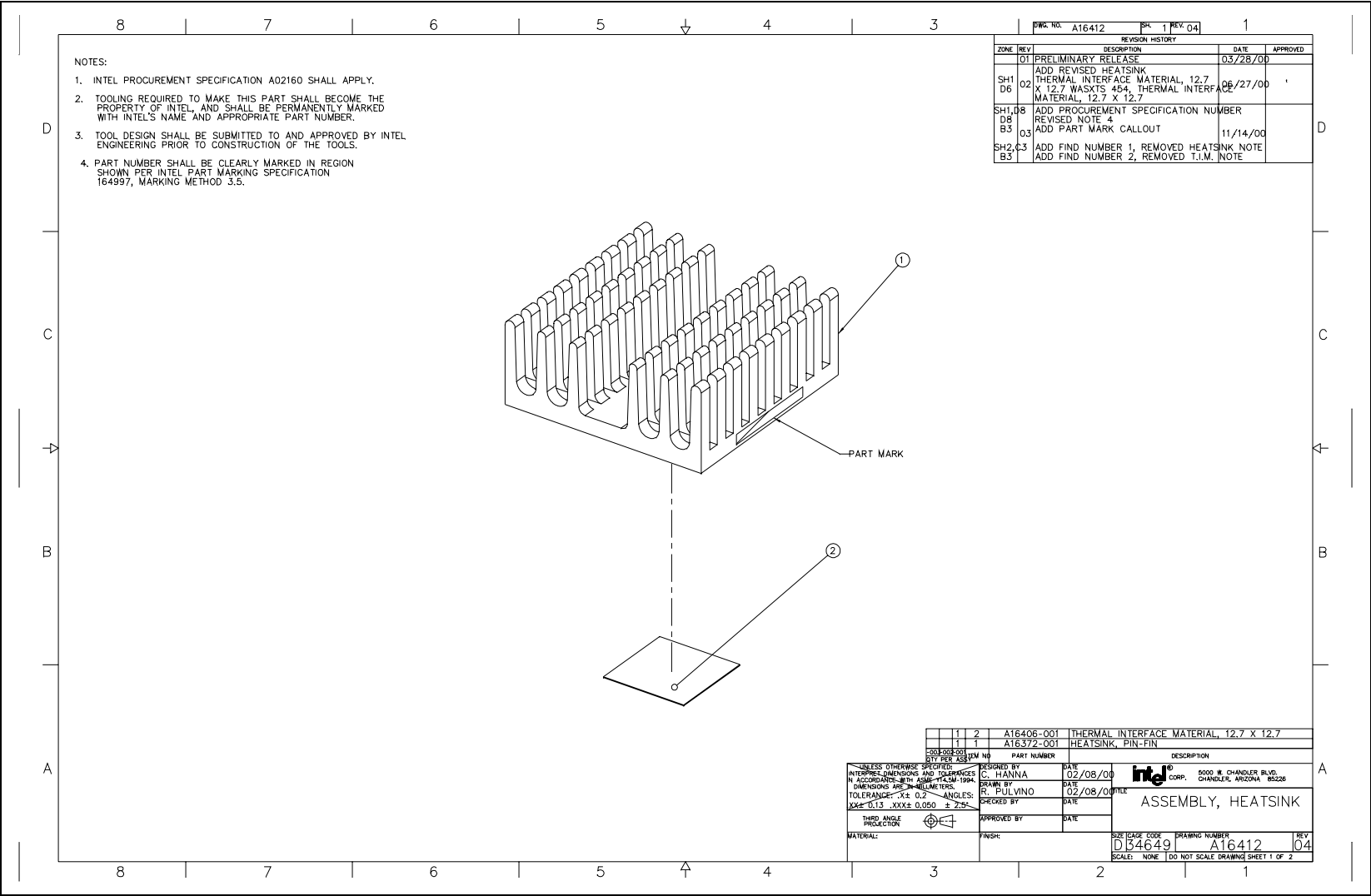
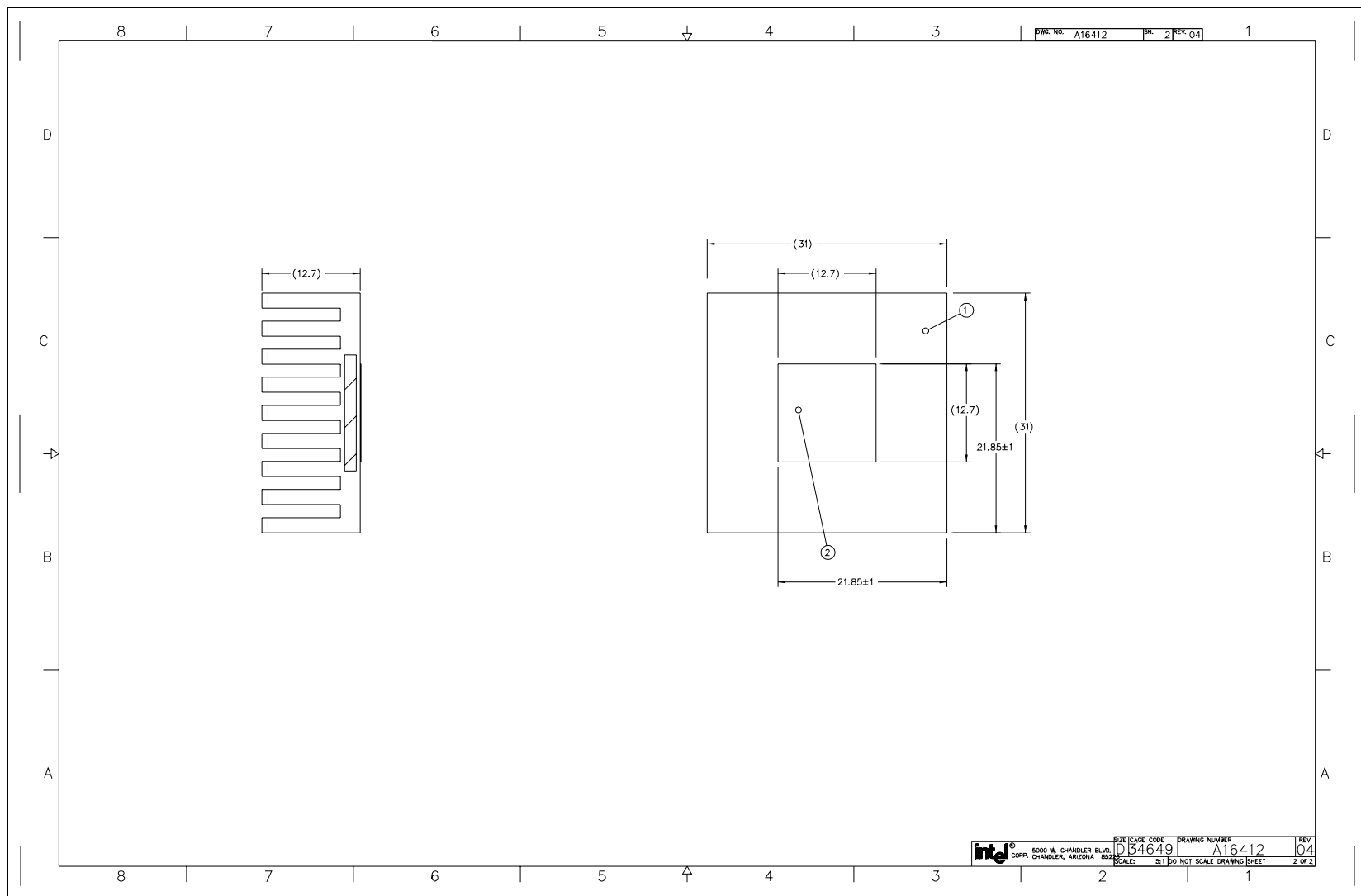


Figure 19. Clip Heatsink + TIM Assembly Drawing (Sheet 2 of 2)



NOTES:

- BREAK ALL SHARP EDGES 0.13 MAX.
- TOOLING REQUIRED TO MAKE THIS PART SHALL BECOME THE PROPERTY OF INTEL AND SHALL BE PERMANENTLY MARKED WITH INTEL'S NAME AND APPROPRIATE PART NUMBER.
- TOOL DESIGN SHALL BE SUBMITTED TO AND APPROVED BY INTEL ENGINEERING PRIOR TO CONSTRUCTION OF THE TOOLS.
- ALL SURFACES ASSOCIATED WITH DATUM "A" SHALL BE FREE OF BURRS.
- ⌘ INDICATES CRITICAL TO FUNCTION DIMENSION.

REVISION HISTORY

ZONE	REV	DESCRIPTION	DATE	APPROVED
	01	PRELIMINARY RELEASE		
C4	02	(9X 1.94) WAS (8X 1.86) 8X 1.6g ^{+0.15} _{-0.02} WAS 8X 1.7g ^{+0.18} _{-0.02}	06/23/00	*
TC8		REMOVED NOTES 1, 6, 7		
TC4	03	8X 2.54 ^{+0.15} _{-0.02} WAS 8X 2.54 ^{+0.15} _{-0.02} ADD ANGULAR TOL OF ±2.5°	11/15/00	
TA3		REMOVED SHEETS 2,3		
B6		2X 4.74 ^{+0.17} WAS 2X 4.74		
B6		1.56 ^{+0.15} WAS 1.56		
A5	04	6X 12.7 ^{+0.45} _{-0.23} WAS 12.7 ^{+0.45} _{-0.23}	12/19/00	
A5		5X 2.54 ^{+0.15} WAS 2X 2.54 ^{+0.15}		
1A2	05	REMOVED NOTE 6 FLAG	01/29/01	

Dimensions and Features:

- Overall width: 31^{+0.6}_{-0.3}
- Pin height: 31^{±0.25}
- Pin pitch: 1.94
- Pin width: 1.6g^{+0.15}_{-0.02}
- Pin spacing: 2.54^{+0.15}_{-0.53}
- Pin angle: 12.7^{+0.45}_{-0.23}
- Pin base width: 1.56^{+0.15}
- Pin base spacing: 4.99^{+0.17}
- Pin base width: 4.74^{+0.17}
- Pin base spacing: 1.25^{+0.15}
- Pin base width: 1.86^{+0.15}
- Pin base spacing: 2.54^{+0.15}
- Pin base width: 1.56^{+0.15}
- Pin base spacing: 4.74^{+0.17}
- Pin base width: 1.25^{+0.15}
- Pin base spacing: 1.94
- Pin base width: 1.6g^{+0.15}_{-0.02}
- Pin base spacing: 2.54^{+0.15}_{-0.53}
- Pin base width: 1.56^{+0.15}
- Pin base spacing: 4.99^{+0.17}
- Pin base width: 4.74^{+0.17}
- Pin base spacing: 1.25^{+0.15}
- Pin base width: 1.86^{+0.15}
- Pin base spacing: 2.54^{+0.15}
- Pin base width: 1.56^{+0.15}
- Pin base spacing: 4.74^{+0.17}
- Pin base width: 1.25^{+0.15}
- Pin base spacing: 1.94
- Pin base width: 1.6g^{+0.15}_{-0.02}
- Pin base spacing: 2.54^{+0.15}_{-0.53}
- Pin base width: 1.56^{+0.15}
- Pin base spacing: 4.99^{+0.17}
- Pin base width: 4.74^{+0.17}
- Pin base spacing: 1.25^{+0.15}
- Pin base width: 1.86^{+0.15}
- Pin base spacing: 2.54^{+0.15}
- Pin base width: 1.56^{+0.15}
- Pin base spacing: 4.74^{+0.17}
- Pin base width: 1.25^{+0.15}
- Pin base spacing: 1.94
- Pin base width: 1.6g^{+0.15}_{-0.02}
- Pin base spacing: 2.54^{+0.15}_{-0.53}
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- Pin base width: 4.74^{+0.17}
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- Pin base width: 1.86^{+0.15}
- Pin base spacing: 2.54^{+0.15}
- Pin base width: 1.56^{+0.15}
- Pin base spacing: 4.74^{+0.17}
- Pin base width: 1.25^{+0.15}
- Pin base spacing: 1.94
- Pin base width: 1.6g^{+0.15}_{-0.02}
- Pin base spacing: 2.54^{+0.15}_{-0.53}
- Pin base width: 1.56^{+0.15}
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- Pin base width: 4.74^{+0.17}
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- Pin base width: 1.56^{+0.15}
- Pin base spacing: 4.74^{+0.17}
- Pin base width: 1.25^{+0.15}
- Pin base spacing: 1.94
- Pin base width: 1.6g^{+0.15}_{-0.02}
- Pin base spacing: 2.54^{+0.15}_{-0.53}
- Pin base width: 1.56^{+0.15}
- Pin base spacing: 4.99^{+0.17}
- Pin base width: 4.74^{+0.17}
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- Pin base spacing: 2.54^{+0.15}
- Pin base width: 1.56^{+0.15}
- Pin base spacing: 4.74^{+0.17}
- Pin base width: 1.25^{+0.15}
- Pin base spacing: 1.94
- Pin base width: 1.6g^{+0.15}_{-0.02}
- Pin base spacing: 2.54^{+0.15}_{-0.53}
- Pin base width: 1.56^{+0.15}
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- Pin base width: 1.56^{+0.15}
- Pin base spacing: 4.74^{+0.17}
- Pin base width: 1.25^{+0.15}
- Pin base spacing: 1.94
- Pin base width: 1.6g^{+0.15}_{-0.02}
- Pin base spacing: 2.54^{+0.15}_{-0.53}
- Pin base width: 1.56^{+0.15}
- Pin base spacing: 4.99^{+0.17}
- Pin base width: 4.74^{+0.17}
- Pin base spacing: 1.25^{+0.15}
- Pin base width: 1.86^{+0.15}
- Pin base spacing: 2.54^{+0.15}
- Pin base width: 1.56^{+0.15}
- Pin base spacing: 4.74^{+0.17}
- Pin base width: 1.25^{+0.15}
- Pin base spacing: 1.94
- Pin base width: 1.6g^{+0.15}_{-0.02}
- Pin base spacing: 2.54^{+0.15}_{-0.53}
- Pin base width: 1.56^{+0.15}
- Pin base spacing: 4.99^{+0.17}
- Pin base width: 4.74^{+0.17}
- Pin base spacing: 1.25^{+0.15}
- Pin base width: 1.86^{+0.15}
- Pin base spacing: 2.54^{+0.15}
- Pin base width: 1.56^{+0.15}
- Pin base spacing: 4.74^{+0.17}
- Pin base width: 1.25^{+0.15}
- Pin base spacing: 1.94
- Pin base width: 1.6g^{+0.15}_{-0.02}
- Pin base spacing: 2.54^{+0.15}_{-0.53}
- Pin base width: 1.56^{+0.15}
- Pin base spacing: 4.99^{+0.17}
- Pin base width: 4.74^{+0.17}
- Pin base spacing: 1.25^{+0.15}
- Pin base width: 1.86^{+0.15}
- Pin base spacing: 2.54^{+0.15}
- Pin base width: 1.56^{+0.15}
- Pin base spacing: 4.74^{+0.17}
- Pin base width: 1.25^{+0.15}
- Pin base spacing: 1.94
- Pin base width: 1.6g

Figure 21. Clip Heatsink Attach Clip Drawing

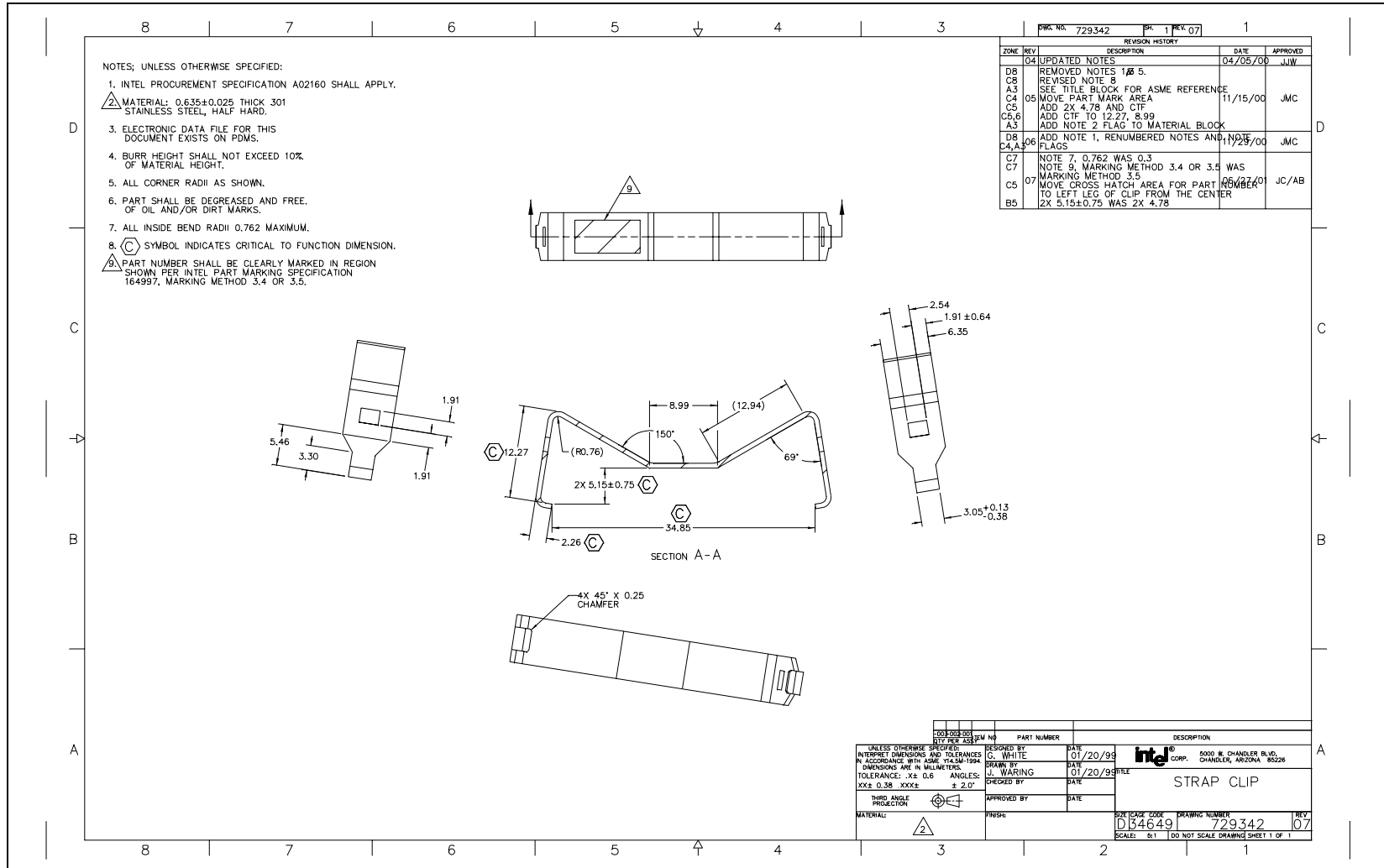




Figure 22. Thermal Adhesive Tape Heatsink Assembly Drawing

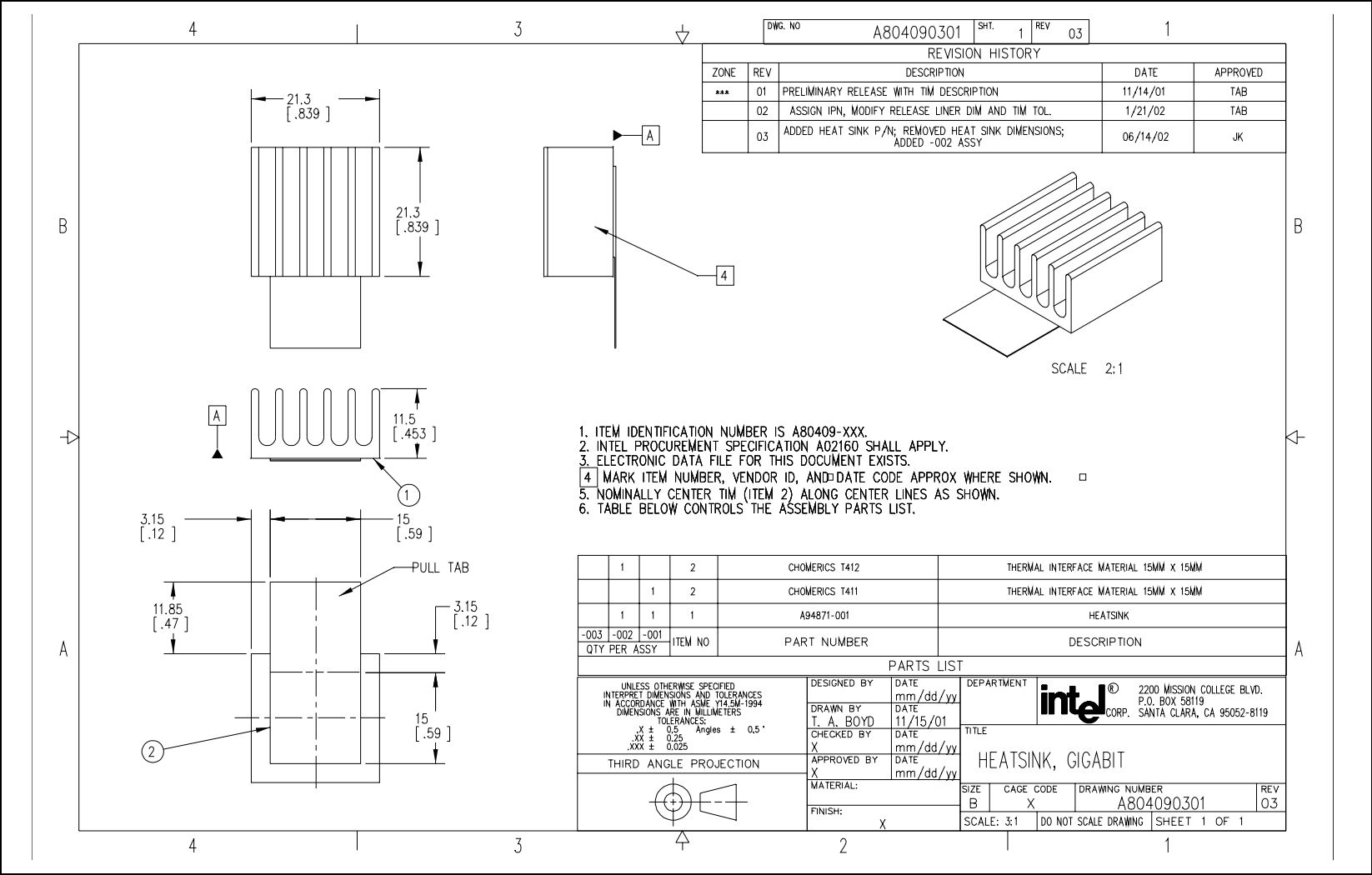


Figure 23. Thermal Adhesive Tape Heatsink Drawing

