Intel® 82599 10 GbE Controller Checklists

LAN Access Division

Project Name	
Fab Revision	
Date	
Schematic Designer	
Layout Designer	
Intel Contact(s)	
Reviewer(s)	

REVISION	DATE	CHANGES
0.10	1/28/2008	Initial draft.
0.2	2/6/2008	Started adding updated layout rules.
0.5	10/22/2008	Should be AC coupling caps "Simmyetry" Symmetry "AC cupling caps" Should be AC coupling cap
0.75	2/3/2009	Schematic Checklist -many changes to update format and ensure consistency with the reference design schematic. Layout Checklist -many grammatical and spelling error fixes
0.76	3/6/2009	Removed design guide references (now a part of the datasheet). Removed XFI reference in layout and placement checklist. Fixed grammatical and spelling errors. Corrected consistency of terms.

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REVISION	DATE	CHANGES
1.5	5/11/2009	Added "For additional design comments, position the mouse cursor over the red symbol at the top-right of these cells: F30, F73, B104, B108, B144, and B148 under General. Added additional design comments to cells: F30, F73, B104, B108, B144, and B148. Corrected typos and symbols.
1.9	5/28/2009	Removed EEPROM-less information. Updated BX, KX, KR and SFI connection information (both MAUI ports). Included additional high-speed decoupling and bulk capacitors for 3.3V and 1.2V supply.
1.91	6/19/2009	Added "Flash clock (FLSH_SCK) should also be pulled to ground using an 8.2 KΩ resistor." at C35 on schematic sheet
		Added "EEPROM clock (EE_SK) should also be pulled to ground using an 8.2 KΩ resistor." at C44 on schematic sheet
		Added SDP connections for SFI designs at 116 and 170
		Updated value of JTDO pull up resistor to 3.3 K ohm
		Added item for pulling up MAIN_PWR_OK with 8.2 K ohm resistor to 3.3 V
		Added details that decoupling for VCC3P3 is 2x22uF and 6x 22uF

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1.91	6/19/2009	Updated antipad dimensions to be of a diameter of via pad diameter + 20 mils
		Added new item "Special layout considerations for SFI"
		Made sure every dimension was in mils or inches Added legal disclaimer. Reformatted for Developer posting. Added Hibberd#.
2.00	7/15/2009	Initial Public Release.
2.10	11/6/2009	Minor edits. No technical changes.
2.11	11/17/2010	Changed the load capacitance value to 20 pF. Changed A21 to AA21 in the PCIe interface.

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SECTION	CHECK ITEM	DETAIL	BALL	Done	COMMENTS AND FEEDBACK
General					
	Have up to date documentation	Documents are subject to frequent change. Make sure to download the latest collateral release.			
	Observe instructions for special pins needing pull- up or pull-down resistors.	Do not connect pull-up or pull-down resistors to any pins marked No Connect (RSVDxxxx_NC/NC_xxxx).			
	Optional interfaces are labeled and should be treated appropriately.	There are many optional interfaces for this silicon that might require a unique configuration.			
PCIe Interface	Connect PCI-Express* PCIe* transmit signals to PCIe host.	PCIe TX Lane 0 differential signals (**PET_0_P** and **PET_0_N**) should be connected to PCIe RX Lane 0 of host interface through **0.1 µF** AC coupling capacitors. NOTE: Place the AC coupling caps close to the transmitter.	Y23 and Y24		

SECTION	CHECK ITEM	DETAIL	BALL	Done	COMMENTS AND FEEDBACK
PCIe Interface	Connect PCI-Express* PCIe* transmit signals to PCIe host.	PCIe Tx lane 1 differential signals (**PET_1_P** and **PET_1_N**) should be connected to PCIe RX Lane 1 of host interface through **0.1 µF** AC coupling capacitors. NOTE: Place the AC coupling caps close to the transmitter.	V23 and V24		
		PCIe Tx lane 2 differential signals (**PET_2_P** and **PET_2_N**) should be connected to PCIe RX Lane 2 of host interface through **0.1 µF** AC coupling capacitors. NOTE: Place the AC coupling caps close to the transmitter.	T23 and T24		
		PCIe Tx lane 3 differential signals (**PET_3_P** and **PET_3_N**) should be connected to PCIe RX Lane 3 of host interface through **0.1 µF** AC coupling capacitors. NOTE: Place the AC coupling caps close to the transmitter.	P23 and P24		

SECTION	CHECK ITEM	DETAIL	BALL	Done	COMMENTS AND FEEDBACK
PCIe Interface	Connect PCI-Express* PCIe* transmit signals to PCIe host.	PCIe Tx lane 4 differential signals (**PET_4_P** and **PET_4_N**) should be connected to PCIe RX Lane 4 of host interface through **0.1 µF** AC coupling capacitors. NOTE: Place the AC coupling caps close to the transmitter.	J23 and J24		
		PCIe Tx lane 5 differential signals (**PET_5_P** and **PET_5_N**) should be connected to PCIe RX Lane 5 of host interface through **0.1 µF** AC coupling capacitors. NOTE: Place the AC coupling caps close to the transmitter.	G23 and G24		
		PCIe Tx lane 6 differential signals (**PET_6_P** and **PET_6_N**) should be connected to PCIe RX Lane 6 of host interface through **0.1 µF** AC coupling capacitors. NOTE: Place the AC coupling caps close to the transmitter.	E23 and E24		

SECTION	CHECK ITEM	DETAIL	BALL	Done	COMMENTS AND FEEDBACK
PCIe Interface	Connect PCI-Express* PCIe* transmit signals to PCIe host.	PCIe Tx lane 7 differential signals (**PET_7_P** and **PET_7_**N) should be connected to PCIe RX Lane 7 of host interface through **0.1 µF** AC coupling capacitors. NOTE: Place the AC coupling caps close to the transmitter.	C23 and C24		
	Connect PCIe receive signals to PCIe host.	PCIe Rx lane 0 differential signals (**PER_0_P** and **PER_0_N**) should be connected to PCIe TX Lane 0 of host interface through **0.1 µF** AC coupling capacitors. NOTE: Place the AC coupling caps close to the transmitter.	AC20 and AC21		
		PCIe Rx lane 1 differential signals (**PER_1_P** and **PER_1_N**) should be connected to PCIe TX Lane 1 of host interface through **0.1 µF** AC coupling capacitors. NOTE: Place the AC coupling caps close to the transmitter.	AA20 and AA21		

SECTION	CHECK ITEM	DETAIL	BALL	Done	COMMENTS AND FEEDBACK
PCIe Interface	Connect PCIe receive signals to PCIe host.	PCIe Rx lane 2 differential signals (**PER_2_P** and **PER_2_N**) should be connected to PCIe TX Lane 2 of host interface through **0.1 µF** AC coupling capacitors. NOTE: Place the AC coupling caps close to the transmitter.	U20 and U21		
		PCIe Rx lane 3 differential signals (**PER_3_P** and **PER_3_N**) should be connected to PCIe TX Lane 3 of host interface through **0.1 µF** AC coupling capacitors. NOTE: Place the AC coupling caps close to the transmitter.	R20 and R21		
		PCIe Rx lane 4 differential signals (**PER_4_P** and **PER_4_N**) should be connected to PCIe TX Lane 4 of host interface through **0.1 µF** AC coupling capacitors. NOTE: Place the AC coupling caps close to the transmitter.	K20 and K21		

SECTION	CHECK ITEM	DETAIL	BALL	Done	COMMENTS AND FEEDBACK
PCIe Interface	Connect PCIe receive signals to PCIe host.	PCIe Rx lane 5 differential signals (**PER_5_P** and **PER_5_N**) should be connected to PCIe TX Lane 5 of host interface through **0.1 µF** AC coupling capacitors. NOTE: Place the AC coupling caps close to the transmitter.	H20 and H21		
		PCIe Rx lane 6 differential signals (**PER_6_P** and **PER_6_N**) should be connected to PCIe TX Lane 6 of host interface through **0.1 µF** AC coupling capacitors. NOTE: Place the AC coupling caps close to the transmitter.	D20 and D21		
		PCIe Rx lane 7 differential signals (**PER_7_P** and **PER_7_N**) should be connected to PCIe TX Lane 7 of host interface through **0.1 µF** AC coupling capacitors. NOTE: Place the AC coupling caps close to the transmitter.	B20 and B21		

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SECTION	CHECK ITEM	DETAIL	BALL	Done	COMMENTS AND FEEDBACK
PCIe Interface	Connect PCIe differential clock signals to PCIe host clock.	PCIe differential clock signals (**PE_CLK_P** and **PE_CLK_N**) should be connected to PCIe differential clock of host interface.	AB23 and AB24		
	Connect PCIe reset to host system.	PCIe reset signal (**PE_RST_N**) should be connected to PCIe reset signal of host interface.	AD18		
	Connect PCIe wake signal to host.	PCIe wake signal (**PE_WAKE_N**) should be connected to PCIe wake signal of host interface.	AA18		
		PCIe wake signal (**PE_WAKE_N**) should be connected to external 100 KΩ pull-up resistor to the **3.3V** supply.	AA18		
		If not used leave unconnected.	AA18		

SECTION	CHECK ITEM	DETAIL	BALL	Done	COMMENTS AND FEEDBACK
PCIe Interface	Connect PCIe compensation resistor	A **24.9 Ω 0.5%** PCIe compensation resistor should be connected between **PE_RBIAS** and the **1.2V** supply. NOTE: Using less expensive 1% resistors instead of 0.5% adds risk to the stability of the 82599. COMMENT: These resistors control the stability and accuracy of internal circuits used on the analog interfaces to establish and maintain link between the LAN controller and the far end device. Failure to install the Intel specified tolerance will result in a product that will not conform to the IEEE, PCIe, or PICMG specification requirements for transmitter and receiver performance across process, temperature, and voltage variations. This may or may not include failure to obtain a reliable PCIe or MAUI link.	M24		
		Connect the **PE_RBIAS** and **PE_RSENSE** pins together..	M24 and N24		

SECTION	CHECK ITEM	DETAIL	BALL	Done	COMMENTS AND FEEDBACK
Serial Flash Interface	Connect serial Flash interface.	Flash chip enable (**FLSH_CE_N**) should be connected to chip select of Flash device.	B7		
		Flash chip enable (**FLSH_CE_N**) should be connected to external **8.2 KΩ** pull-up resistor to **3.3V** supply. **Note:** 10 KΩ - 100 KΩ	B7		
		Flash clock (**FLSH_SCK**) should be connected to Flash clock port of external Flash device. **Note:** Optional 22 Ω serial resistor can be added.	A8		
		Flash clock (FLSH_SCK) should also be pulled to ground using an 8.2 KΩ resistor.	A8		
		Flash data input signal (**FLSH_SI**), an output signal, should be connected to Flash data input (**SI**) of external Flash device.	B6		

SECTION	CHECK ITEM	DETAIL	BALL	Done	COMMENTS AND FEEDBACK
Serial Flash Interface	Connect serial Flash interface.	Flash data output signal (**FLSH_SO**), an input signal, should be connected to Flash data output (**SO**) of external Flash device.	A7		
		Add a **8.2 KΩ** pull-up resistor on the Flash's **WP_N** and **HOLD_N** pins.			
		Add a **0.1 µF** decoupling capacitor close to the SPI Flash chip's power pin			
	If a Flash is not used.	Leave **FLSH_CE_N**, **FLSH_SCK**, **FLSH_SI**, **FLSH_SO** unconnected.			
Serial EEPROM Interface	Connect serial EEPROM interface.	EEPROM chip enable **(EE_CS_N)** should be connected to chip select of EEPROM device.	C19		
		EEPROM chip enable (**EE_CS_N**) should be connected to external **8.2 KΩ** pull-up resistor to **3.3V** supply. NOTE: 10 KΩ - 100 KΩ	C19		

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SECTION	CHECK ITEM	DETAIL	BALL	Done	COMMENTS AND FEEDBACK
Serial EEPROM Interface	Connect serial EEPROM interface.	EEPROM clock (**EE_SK**) should be connected to EEPROM clock port of external EEPROM device.	B19		
		EEPROM clock (**EE_SK**) should also be pulled to ground using an 8.2 KΩ resistor.	B19		
		EEPROM data input signal (**EE_DI**), an output signal, should be connected to EEPROM data input (**SI**) of external EEPROM device.	B18		
		EEPROM data output signal (**EE_DO**), an input signal, should be connected to EEPROM data output (**SO**) of external EEPROM device.	A18		
		Add a **8.2 KΩ** pull-up resistor on the EEPROM's **WP_N** and **HOLD_N** pins.			
		Add a **0.1 µF** decoupling capacitor close to the EEPROM's power pin.			

SECTION	CHECK ITEM	DETAIL	BALL	Done	COMMENTS AND FEEDBACK
SMBus Interface	Connect SMBus management interface.	SMB bidirectional data signal (**SMBD**) should be connected to SMBus data signal.	AB19		
		SMB bidirectional data signal (**SMBD**) should be connected to an external **8.2 KΩ** pull-up resistor to **3.3V**. For valid pull-up value range please consult the datasheet.	AB19		
		SMB clock signal (**SMBCLK**) should be connected to SMBus clock signal on the platform.	AC19		
		SMB clock signal (**SMBCLK**) should be connected to an external **8.2 KΩ** pull-up resistor to **3.3V**. For valid pull-up value range please consult the datasheet.	AC19		
		SMB alert signal (**SMBALRT_N**) should be connected to SMBus alert signal on the platform. NOTE: Thi an optional signal. If not used, it is typically pulled up to 3.3V with a 8.2 KΩ	AA19		

SECTION	CHECK ITEM	DETAIL	BALL	Done	COMMENTS AND FEEDBACK
SMBus Interface	Connect SMBus management interface.	SMB alert signal (**SMBALRT_N**) should be connected to an external **8.2 KΩ** pull-up resistor to **3.3V**. For valid pull-up value range please consult the datasheet.	AA19		
	If SMBus is not used.	SMB bidirectional data signal (**SMBD**) should be connected to an external **8.2 KΩ** pull-up resistor to **3.3V**. For valid pull-up value range please consult the datasheet.	AB19		
		SMB clock signal (**SMBCLK**) should be connected to an external **8.2 KΩ** pull-up resistor to **3.3V**. For valid pull-up value range please consult the datasheet.	AC19		
		SMB alert signal (**SMBALRT_N**) should be connected to an external **8.2 KΩ** pull-up resistor to **3.3V**. For valid pull-up value range please consult the datasheet.	AA19		

SECTION	CHECK ITEM	DETAIL	BALL	Done	COMMENTS AND FEEDBACK
NC-SI interface	Connect NC-SI management interface.	The NC-SI clock input (NCSI_CLK_IN) should be connected to a specification-compliant 50 MHz clock generated on the platform (50 ppm).	AC11		
		The NC-SI clock input (NCSI_CLK_IN) should be connected to 100 Ω pull-down resistor to VSS.	AC11		
		The NC-SI receive data output signals (NCSI_RXD_1 and NCSI_RXD_0) should be connected to the NC-SI data inputs of the external Manageability Controller (MC).	AA11 and AC10		
		The NC-SI receive data output signals (NCSI_RXD_1 and NCSI_RXD_0) should be connected to 8.2 KΩ pull-up resistors to 3.3V.	AA11 and AC10		

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SECTION	CHECK ITEM	DETAIL	BALL	Done	COMMENTS AND FEEDBACK
NC-SI interface	Connect NC-SI management interface.	The NC-SI carrier sense/receive data valid signal output (NCSI_CRS_DV) should be connected to the CRS/DV input port on the external MC.	AB11		
		The NC-SI carrier sense/receive data valid signal output (NCSI_CRS_DV) should be connected to a 100 Ω pull-down resistor. For valid pull-down value range please consult the datasheet.	AB11		
		The NC-SI transmit data input signals (NCSI_TXD_1 and NCSI_TXD_0) should be connected to the NC-SI data outputs of the external MC.	AA10 and AD11		
		The NC-SI transmit data input signals (NCSI_TXD_1 and NCSI_TXD_0) should be connected to 8.2 KΩ pull-up resistor to 3.3V.	AA10 and AD11		

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SECTION	CHECK ITEM	DETAIL	BALL	Done	COMMENTS AND FEEDBACK
NC-SI interface	Connect NC-SI management interface.	The NC-SI transmit enable input signal (NCSI_TX_EN) should be connected to the transmit enable output of the external MC.	AB11		
		The NC-SI transmit enable input signal (NCSI_TX_EN) should be connected to 100 Ω pull-down resistor to VSS.	AB11		
	If NC-SI interface is not used.	The NC-SI clock input (NCSI_CLK_IN) should be connected to external 100 Ω pull-down resistor. For valid pull-down value range please consult the datasheet.	AC11		
		The NC-SI receive data output signals (NCSI_RXD_1 and NCSI_RXD_0) should be connected to an external 8.2 KΩ pull-up resistor to 3.3V supply. For valid pull-down value range please consult the datasheet.	AA11 and AC10		

SECTION	CHECK ITEM	DETAIL	BALL	Done	COMMENTS AND FEEDBACK
NC-SI interface	Connect NC-SI interface.	The NC-SI carrier sense/receive data valid signal output (NCSI_CRS_DV) should be connected to a 100 Ω pull-down resistor. For valid pull-down value range please consult the datasheet.	AB11		
		The NC-SI transmit data input signals (NCSI_TXD_1 and NCSI_TXD_0) should be connected to external 8.2 KΩ pull-up resistor to 3.3V supply. For valid pull-down value range please consult the datasheet.	AA10 and AD11		
		The NC-SI transmit enable input signal (NCSI_TX_EN) should be connected to an external 100 Ω pull-down resistor. For valid pull-down value range please consult the datasheet.	AB10		

SECTION	CHECK ITEM	DETAIL	BALL	Done	COMMENTS AND FEEDBACK
MAUI		Connect a **1 KΩ 0.5%** bias resistor between **XA_RBIAS_p** and **XA_RBIAS_n.** For valid pull-down value range please consult the datasheet. NOTE: Using less expensive 1% resistors instead of 0.5% adds risk to the stability of the 82599. COMMENT: These resistors control the stability and accuracy of internal circuits used on the analog interfaces to establish and maintain link between the LAN controller and the far end device. Failure to install the Intel specified tolerance will result in a product that will not conform to the IEEE, PCIe, or PICMG spec requirements for transmitter and receiver performance across process, temperature, and voltage variations. This may or may not include failure to obtain a reliable PCIe or MAUI link.	L2 and L1		

SECTION	CHECK ITEM	DETAIL	BALL	Done	COMMENTS AND FEEDBACK
MAUI		Each of the MAUI ports can individually be configured to operate in one of the following modes: XAUI, BX, KX/KX4/KR, CX4 or SFI			
		Based on the chosen interface setup there might be unused differential pairs. These should be left unconnected.			
MAUI Port 0	BX, KX, KR and SFI connection.	Port 0 - lane 0 transmit differential signals (**TX0_L0_N** and **TX0_L0_P**) should be connected to the receive port of the link partner or to the corresponding connector.	J1 and J2		

SECTION	CHECK ITEM	DETAIL	BALL	Done	COMMENTS AND FEEDBACK
MAUI Port 0	BX, KX, KR and SFI connection.	Port 0 - lane 0 receive differential signals (**RX0_L0_N** and **RX0_L0_P**) should be connected to the transmit port of the link partner or to the corresponding connector through **0.01 µF** AC coupling capacitors. Place the AC coupling capacitors close to the receiver of the 82599. If designing an SFI interface, then AC coupling capacitors are not required if they are internal to SFP+ module.	H4 and H5		
	KX4 connection.	Port 0 - lane 0 transmit differential signals (**TX0_L0_N** and **TX0_L0_P**) should be connected to the receive port of the link partner or to the corresponding pins of the backplane connector.	J1 and J2		

SECTION	CHECK ITEM	DETAIL	BALL	Done	COMMENTS AND FEEDBACK
MAUI Port 0	KX4 connection.	Port 0 - lane 1 transmit differential signals (**TX0_L1_N** and **TX0_L1_P**) should be connected to the receive port of the link partner or to the corresponding pins of the backplane connector.	G1 and G2		
		Port 0 - lane 2 transmit differential signals (**TX0_L2_N** and **TX0_L2_P**) should be connected to the receive port of the link partner or to the corresponding pins of the backplane connector.	E1 and E2		
		Port 0 - lane 3 transmit differential signals (**TX0_L3_N** and **TX0_L3_P**) should be connected to the receive port of the link partner or to the corresponding pins of the backplane connector.	C1 and C2		

SECTION	CHECK ITEM	DETAIL	BALL	Done	COMMENTS AND FEEDBACK
MAUI Port 0	KX4 connection.	Port 0 - lane 0 receive differential signals (**RX0_L0_N** and **RX0_L0_P**) should be connected to the transmit port of the link partner or to the corresponding pins of the backplane connector, through **0.01 µF** AC coupling capacitors. Place the AC coupling capacitors close to the receiver of the 82599.	H4 and H5		
		Port 0 - lane 1 receive differential signals (**RX0_L1_N** and **RX0_L1_P**) should be connected to the transmit port of the link partner or to the corresponding pins of the backplane connector, through **0.01 µF** AC coupling capacitors. Place the AC coupling capacitors close to the receiver of the 82599.	F4 and F5		

SECTION	CHECK ITEM	DETAIL	BALL	Done	COMMENTS AND FEEDBACK
MAUI Port 0	KX4 connection.	Port 0 - lane 2 receive differential signals (**RX0_L2_N** and **RX0_L2_P**) should be connected to the transmit port of the link partner or to the corresponding pins of the backplane connector, through **0.01 µF** AC coupling capacitors. Place the AC coupling capacitors close to the receiver of the 82599.	D4 and D5		
		Port 0 - lane 3 receive differential signals (**RX0_L3_N** and **RX0_L3_P**) should be connected to the transmit port of the link partner or to the corresponding pins of the backplane connector, through **0.01 µF** AC coupling capacitors. Place the AC coupling capacitors close to the receiver of the 82599.	B4 and A4		
	CX4 connection.	Port 0 - lane 0 transmit differential signals (**TX0_L0_N** and **TX0_L0_P**) should be connected to pin **S15** and **S16,** respectively, of the CX4 connector.	J1 and J2		

SECTION	CHECK ITEM	DETAIL	BALL	Done	COMMENTS AND FEEDBACK
MAUI Port 0	CX4 connection.	Port 0 - lane 1 transmit differential signals (**TX0_L1_N** and **TX0_L1_P**) should be connected to pin **S13** and **S14,** respectively, of the CX4 connector.	G1 and G2		
		Port 0 - lane 2 transmit differential signals (**TX0_L2_N** and **TX0_L2_P**) should be connected to pin **S11** and **S12,** respectively, of the CX4 connector.	E1 and E2		
		Port 0 - lane 3 transmit differential signals (**TX0_L3_N** and **TX0_L3_P**) should be connected to pin **S9** and **S10,** respectively, of the CX4 connector.	C1 and C2		
		Port 0 - lane 0 receive differential signals (**RX0_L0_P** and **RX0_L0_N**) should be connected to pin **S1** and **S2,** respectively, of the CX4 connector., through **470 pF** AC coupling caps. Place the AC coupling caps close to the receiver of the 82599	H4 and H5		

SECTION	CHECK ITEM	DETAIL	BALL	Done	COMMENTS AND FEEDBACK
MAUI Port 0	CX4 connection.	Port 0 - lane 1 receive differential signals (**RX0_L1_P** and **RX0_L1_N**) should be connected to pin **S3** and **S4,** respectively, of the CX4 connector through **470 pF** AC coupling capacitors. Place the AC coupling caps close to the receiver of the 82599	F4 and F5		
		Port 0 - lane 2 receive differential signals (**RX0_L2_P** and **RX0_L2_N**) should be connected to pin **S5** and **S6,** respectively, of the CX4 connector through **470 pF** AC coupling capacitors. Place the AC coupling caps close to the receiver of the 82599	D4 and D5		

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SECTION	CHECK ITEM	DETAIL	BALL	Done	COMMENTS AND FEEDBACK
MAUI Port 0	CX4 connection.	Port 0 - lane 3 receive differential signals (**RX0_L3_P** and **RX0_L3_N**) should be connected to pin **S7** and **S8,** respectively, of the CX4 connector through **470 pF** AC coupling capacitors. Place the AC coupling capacitors close to the receiver of the 82599	B4 and A4		.
	XAUI connection.	Port 0 - lane 0 transmit differential signals (**TX0_L0_N** and **TX0_L0_P**) should be connected to the receive port lane 0 of the XAUI link partner. The link partner should have caps located near the receiver on its PHY. Some optical modules like XENPAK, XPAK include these AC coupling caps.	J1 and J2		

SECTION	CHECK ITEM	DETAIL	BALL	Done	COMMENTS AND FEEDBACK
MAUI Port 0	XAUI connection.	Port 0 - lane 1 transmit differential signals (**TX0_L1_N** and **TX0_L1_P**) should be connected to the receive port lane 1 of the XAUI link partner. The link partner should have caps located near the receiver on its PHY. Some optical modules like XENPAK, XPAK include these AC coupling caps.	G1 and G2		
		Port 0 - lane 2 transmit differential signals (**TX0_L2_N** and **TX0_L2_P**) should be connected to the receive port lane 2 of the XAUI link partner. The link partner should have caps located near the receiver on its PHY. Some optical modules like XENPAK, XPAK include these AC coupling caps.	E1 and E2		

SECTION	CHECK ITEM	DETAIL	BALL	Done	COMMENTS AND FEEDBACK
MAUI Port 0	XAUI connection.	Port 0 - lane 3 transmit differential signals (**TX0_L3_N** and **TX0_L3_P**) should be connected to the receive port lane 3 of the XAUI link partner. The link partner should have caps located near the receiver on its PHY. Some optical modules like XENPAK, XPAK include these AC coupling caps.	C1 and C2		
		Port 0 - lane 0 receive differential signals (**RX0_L0_N** and **RX0_L0_P**) should be connected to the transmit port lane 0 of the XAUI link partner through **0.01 µF** AC coupling capacitors. Place the AC coupling capacitors close to the receiver of the 82599. Some optical modules like XENPAK, XPAK include these AC coupling capacitors.	H4 and H5		

SECTION	CHECK ITEM	DETAIL	BALL	Done	COMMENTS AND FEEDBACK
MAUI Port 0	XAUI connection.	Port 0 - lane 1 receive differential signals (**RX0_L1_N** and **RX0_L1_P**) should be connected to the transmit port lane 1 of the XAUI link partner through **0.01 µF** AC coupling capacitors. Place the AC coupling capacitors close to the receiver of the 82599. Some optical modules like XENPAK, XPAK include these AC coupling capacitors.	F4 and F5		
		Port 0 - lane 2 receive differential signals (**RX0_L2_N** and **RX0_L2_P**) should be connected to the transmit port lane 2 of the XAUI link partner through **0.01 µF** AC coupling capacitors. Place the AC coupling capacitors close to the receiver of the 82599. Some optical modules like XENPAK, XPAK include these AC coupling capacitors.	D4 and D5		

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SECTION	CHECK ITEM	DETAIL	BALL	Done	COMMENTS AND FEEDBACK
MAUI Port 0	XAUI connection.	Port 0 - lane 3 receive differential signals (**RX0_L3_N** and **RX0_L3_P**) should be connected to the transmit port lane 3 of the XAUI link partner through **0.01 µF** AC coupling capacitors. Place the AC coupling capacitors close to the receiver of the 82599. Some optical modules like XENPAK, XPAK include these AC coupling capacitors.	B4 and A4		
	Connect the LED signals	The LED outputs can be configured in many different ways. Make sure to provide a current limiting resistor and, it is recommended to also provide a place for an EMI filter capacitor (for example: **470 pF**). For more information see the datasheet and reference schematics.	AD14, AC14, AB14, and AA14		
		If LEDs are not needed leave the pins unconnected.			

SECTION	CHECK ITEM	DETAIL	BALL	Done	COMMENTS AND FEEDBACK
MAUI Port 0	Connect MDIO interface. NOTE: The Intel device driver is coded for I^2C and not MDIO.	If used, connect the MDIO signals (**MDC0** and **MDIO0**) to the MDIO port of the PHY used. For valid pull-up value range please consult the datasheet. NOTE: Intel device driver implements I^2C when applicable	AC12 and AD12		
		Pull up the MDIO line to **3.3V** via a **3.3 KΩ** resistor. For valid pull-up value range please consult the datasheet.	AD12		
		Please note that these pins use **3.3V** signaling. If necessary use **bi-directional level shifters**.			
		If MDIO not used: leave the **MDC0** signal unconnected and pull-up the **MDIO0** signal to **3.3V** with a **3.3 KΩ** resistor. For valid pull-up value range please consult the datasheet.	AC12 and AD12		

SECTION	CHECK ITEM	DETAIL	BALL	Done	COMMENTS AND FEEDBACK
MAUI Port 0	Connect I^2C interface NOTE: The Intel device driver is coded for I^2C and not MDIO.	If used, connect the **SCL0** signal to the SFP+ interface's corresponding pin. NOTE: Intel device driver implements I^2C when applicable	AB12		
		Connect **SCL0** to a **3.3 KΩ** pull-up resistor to **3.3V.** For valid pull-up value range please consult the datasheet.	AB12		
		If used, connect the **SDA0** signal to the SFP+ interface's corresponding pin.	AA12		
		Connect **SDA0** to a **3.3 KΩ** pull-up resistor to **3.3V.** For valid pull-up value range please consult the datasheet.	AA12		
		If the I^2C interface is not used, an external **3.3 KΩ** pull up resistor to **3.3V** should be used for both: **SCL0** and the **SDA0** pins. For valid pull-up value range please consult the datasheet.	AB12 and AA12		

SECTION	CHECK ITEM	DETAIL	BALL	Done	COMMENTS AND FEEDBACK
MAUI Port 0	Connect Software Defined Pins (SDPs).	Use these signals as needed for miscellaneous PHY control signals like reset, signal detect, transmit disable, module detect and others. These pins can be configured to operate in native (hardware-determined function) mode or as a GPIO controlled by software. For more information on function, default value and I/O direction consult the datasheet			
		Please note that these pins use **3.3V** signaling. If necessary use level shifters.			
		SDPs that are not used should be left unconnected.			
	SDP connections for SFI designs.	**SDP0_0** connects to the **RX_LOS pin (8)** on the SFP cage.	AD8		
		SDP0_0 is also pulled up to **3.3V** with a **10KΩ** resistor.	AD8		

SECTION	CHECK ITEM	DETAIL	BALL	Done	COMMENTS AND FEEDBACK
MAUI Port 0	SDP connections for SFI designs.	**SDP0_1** connects to **RX_LOS pin (8)** on the SFP cage using an inverter. The inverter input is connected to RX_LOS pin (8) from the SFP cage, and the output is connected to the 82599	AC8		
		SDP0_2 connects to **MOD_ABS pin (6)** using an inverter. The inverter input is connected to MOD_ABS pin on the SFP cage, and the output is connected to the 82599.	AB8		
		SDP0_3 connects to **TX_DISABLE pin (3)** on the SFP cage.	AA8		
		SDP0_3 should have a stuffing option to pull down to **ground** through **100 Ω** resistor.	AA8		

SECTION	CHECK ITEM	DETAIL	BALL	Done	COMMENTS AND FEEDBACK
MAUI Port 0	SDP connections for SFI designs.	**SDP0_4** is used to strap SEC_ENA for both ports. To **enable,** pull SDP0_4 to **3.3V** using **10 KΩ** resistor. To **disable,** pull SDP0_4 to **ground** using **100 Ω** resistor.	AD7		
		Connect **RS1 pin (9)** and **RS0 pin (7)** on the SFP+ cage to form **RS0/RS1_SENSE**	AC7		
		SDP0_5 connects to **RS0/RS1_SENSE** through a **1.5 KΩ** resistor.	AC7		
		SDP0_5 is also pulled up to **3.3V** with a **1.5 KΩ** resistor.	AC7		
		SDP0_6 connects to **RS0/RS1_SENSE**	AB7		
		SDP0_7 connects to TX_FAULT pin (2) on the SFP cage.	AA7		
		SDP0_7 is also pulled up to **3.3V** with a **10 KΩ** resistor.	AA7		

SECTION	CHECK ITEM	DETAIL	BALL	Done	COMMENTS AND FEEDBACK
MAUI Port 0	SDP connections for SFI designs.	**MOD_ABS pin (6)** on the SFP connector is pulled to **3.3V** using a **10 KΩ** resistor.	AB8		
MAUI Port 1	BX, KX, KR and SFI connection.	Port 1 - lane 0 transmit differential signals (**TX1_L0_N** and **TX1_L0_P**) should be connected to the receive port of the link partner or to the corresponding connector.	AB1 and AB2		
		Port 1 - lane 0 receive differential signals (**RX1_L0_N** and **RX1_L0_P**) should be connected to the transmit port of the link partner or to the corresponding connector through **0.01 µF** AC coupling capacitors. Place the AC coupling capacitors close to the receiver of the 82599. If designing an SFI interface, then AC coupling capacitors are not required if they are internal to SFP+ module.	AD4 and AC4		

SECTION	CHECK ITEM	DETAIL	BALL	Done	COMMENTS AND FEEDBACK
MAUI Port 1	KX4 connection.	Port 1 - lane 0 transmit differential signals (**TX1_L0_N** and **TX1_L0_P**) should be connected to the receive port of the link partner or to the corresponding pins of the backplane connector.	AB1 and AB2		
		Port 1 - lane 1 transmit differential signals (**TX1_L1_N** and **TX1_L1_P**) should be connected to the receive port of the link partner or to the corresponding pins of the backplane connector.	Y1 and Y2		
		Port 1 - lane 2 transmit differential signals (**TX1_L2_N** and **TX1_L2_P**) should be connected to the receive port of the link partner or to the corresponding pins of the backplane connector.	V1 and V2		

SECTION	CHECK ITEM	DETAIL	BALL	Done	COMMENTS AND FEEDBACK
MAUI Port 1	KX4 connection.	Port 1 - lane 3 transmit differential signals (**TX1_L3_N** and **TX1_L3_P**) should be connected to the receive port of the link partner or to the corresponding pins of the backplane connector.	T1 and T2		
		Port 1 - lane 0 receive differential signals (**RX1_L0_N** and **RX1_L0_P**) should be connected to the transmit port of the link partner or to the corresponding pins of the backplane connector, through **0.01 µF** AC coupling capacitors. Place the AC coupling capacitors close to the receiver of the 82599.	AD4 and AC4		

SECTION	CHECK ITEM	DETAIL	BALL	Done	COMMENTS AND FEEDBACK
MAUI Port 1	KX4 connection.	Port 1 - lane 1 receive differential signals (**RX1_L1_N** and **RX1_L1_P**) should be connected to the transmit port of the link partner or to the corresponding pins of the backplane connector, through **0.01 µF** AC coupling capacitors. Place the AC coupling capacitors close to the receiver of the 82599.	AA4 and AA5		
		Port 1 - lane 2 receive differential signals (**RX1_L2_N** and **RX1_L2_P**) should be connected to the transmit port of the link partner or to the corresponding pins of the backplane connector, through **0.01 µF** AC coupling capacitors.	W4 and W5		

SECTION	CHECK ITEM	DETAIL	BALL	Done	COMMENTS AND FEEDBACK
MAUI Port 1	KX4 connection.	Port 1 - lane 3 receive differential signals (**RX1_L3_N** and **RX1_L3_P**) should be connected to the transmit port of the link partner or to the corresponding pins of the backplane connector, through **0.01 µF** AC coupling capacitors. Place the AC coupling capacitors close to the receiver of the 82599.	U4 and U5		
	CX4 connection.	Port 1 - lane 0 transmit differential signals (**TX1_L0_N** and **TX1_L0_P**) should be connected to pin **S15** and **S16,** respectively, of the CX4 connector.	AB1 and AB2		
		Port 1 - lane 1 transmit differential signals (**TX1_L1_N** and **TX1_L1_P**) should be connected to pin **S13** and **S14,** respectively, of the CX4 connector.	Y1 and Y2		
		Port 1 - lane 2 transmit differential signals (**TX1_L2_N** and **TX1_L2_P**) should be connected to pin **S11** and **S12,** respectively, of the CX4 connector.	V1 and V2		

SECTION	CHECK ITEM	DETAIL	BALL	Done	COMMENTS AND FEEDBACK
MAUI Port 1	CX4 connection.	Port 1 - lane 3 transmit differential signals (**TX1_L3_N** and **TX1_L3_P**) should be connected to pin **S9** and **S10,** respectively, of the CX4 connector.	T1 and T2		
		Port 1 - lane 0 receive differential signals (**RX1_L0_P** and **RX1_L0_N**) should be connected to pin **S1** and **S2,** respectively, of the CX4 connector., through **470 pF** AC coupling capacitors. Place the AC coupling capacitors close to the receiver of the 82599.	AD4 and AC4		
		Port 1 - lane 1 receive differential signals (**RX1_L1_P** and **RX1_L1_N**) should be connected to pin **S3** and **S4,** respectively, of the CX4 connector through **470 pF** AC coupling capacitors. Place the AC coupling capacitors close to the receiver of the 82599.	AA4 and AA5		

SECTION	CHECK ITEM	DETAIL	BALL	Done	COMMENTS AND FEEDBACK
MAUI Port 1	CX4 connection.	Port 1 - lane 2 receive differential signals (**RX1_L2_P** and **RX1_L2_N**) should be connected to pin **S5** and **S6,** respectively, of the CX4 connector through **470 pF** AC coupling capacitors. Place the AC coupling capacitors close to the receiver of the 82599.	W4 and W5		
		Port 1 - lane 3 receive differential signals (**RX1_L3_P** and **RX1_L3_N**) should be connected to pin **S7** and **S8,** respectively, of the CX4 connector through **470 pF** AC coupling capacitors. Place the AC coupling capacitors close to the receiver of the 82599.	U4 and U5		
	XAUI connection.	Port 1 - lane 0 transmit differential signals (**TX1_L0_N** and **TX1_L0_P**) should be connected to the receive port lane 0 of the XAUI link partner.	AB1 and AB2		

SECTION	CHECK ITEM	DETAIL	BALL	Done	COMMENTS AND FEEDBACK
MAUI Port 1	XAUI connection.	Port 1 - lane 1 transmit differential signals (**TX1_L1_N** and **TX1_L1_P**) should be connected to the receive port lane 1 of the XAUI link partner. Place the AC coupling capacitors close to the receiver. Some optical modules like XENPAK, XPAK include these AC coupling capacitors.	Y1 and Y2		
		Port 1 - lane 2 transmit differential signals (**TX1_L2_N** and **TX1_L2_P**) should be connected to the receive port lane 2 of the XAUI link partner. Place the AC coupling capacitors close to the receiver. Some optical modules like XENPAK, XPAK include these AC coupling capacitors.	V1 and V2		

SECTION	CHECK ITEM	DETAIL	BALL	Done	COMMENTS AND FEEDBACK
MAUI Port 1	XAUI connection.	Port 1 - lane 3 transmit differential signals (**TX1_L3_N** and **TX1_L3_P**) should be connected to the receive port lane 3 of the XAUI link partner. Place the AC coupling capacitors close to the receiver. Some optical modules like XENPAK, XPAK include these AC coupling capacitors.	T1 and T2		
		Port 1 - lane 0 receive differential signals (**RX1_L0_N** and **RX1_L0_P**) should be connected to the transmit port lane 0 of the XAUI link partner through **0.01 µF** AC coupling capacitors. Place the AC coupling capacitors close to the receiver. Some optical modules like XENPAK, XPAK include these AC coupling capacitors.	AD4 and AC4		

SECTION	CHECK ITEM	DETAIL	BALL	Done	COMMENTS AND FEEDBACK
MAUI Port 1	XAUI connection.	Port 1- lane 1 receive differential signals (**RX1_L1_N** and **RX1_L1_P**) should be connected to the transmit port lane 1 of the XAUI link partner through **0.01 µF** AC coupling capacitors.	AA4 and AA5		
		Port 1 - lane 2 receive differential signals (**RX1_L2_N** and **RX1_L2_P**) should be connected to the transmit port lane 2 of the XAUI link partner through **0.01 µF** AC coupling capacitors. Place the AC coupling capacitors close to the receiver. Some optical modules like XENPAK, XPAK include these AC coupling capacitors.	W4 and W5		

SECTION	CHECK ITEM	DETAIL	BALL	Done	COMMENTS AND FEEDBACK
MAUI Port 1	XAUI connection.	Port 1 - lane 3 receive differential signals (**RX1_L3_N** and **RX1_L3_P**) should be connected to the transmit port lane 3 of the XAUI link partner through **0.01 µF** AC coupling capacitors. Place the AC coupling capacitors close to the receiver. Some optical modules like XENPAK, XPAK include these AC coupling capacitors.	U4 and U5		
	Connect the LED signals.	The LED outputs can be configured in many different ways. Make sure to provide a current limiting resistor and, it is also recommended to provide a place for an EMI filter capacitor (for example: **470 pF**). For more information see the datasheet and reference schematics.	AD13, AC13, AB13, and AA13		
		If LEDs are not needed leave the pins unconnected.			

SECTION	CHECK ITEM	DETAIL	BALL	Done	COMMENTS AND FEEDBACK
MAUI Port 1	Connect MDIO interface.	If used, connect the MDIO signals (**MDC1** and **MDIO1**) to the MDIO port of the PHY used.	AB18 and AC17		
		Pull up the MDIO line to **3.3V** via a **3.3 KΩ** resistor. For more information see the datasheet and reference schematics.	AC17		
		Please note that these pins use **3.3V** signaling. If necessary use **bi-directional level shifters**.			
		If MDIO not used: leave the **MDC1** signal unconnected and pull up the **MDIO1** signal to **3.3V** with a **3.3 KΩ** resistor. For more information see the datasheet and reference schematics.	AB18 and AC17		
	Connect I^2C B4interface. NOTE: The Intel device driver is coded for I^2C and not MDIO.	If used, connect the **SCL1** signal to the SFP+ interface's corresponding pin.	AD17		

SECTION	CHECK ITEM	DETAIL	BALL	Done	COMMENTS AND FEEDBACK
MAUI Port 1	Connect I^2C interface. NOTE: The Intel device driver is coded for I^2C and not MDIO.	Connect **SCL1** to a **3.3 KΩ** pull-up resistor to **3.3V.** For more information see the datasheet and reference schematics.	AD17		
		If used, connect the **SDA1** signal to the SFP+ interface's corresponding pin.	AC18		
		Connect **SDA1** to a **3.3 KΩ** pull-up resistor to **3.3V.** For valid pull-up value range please consult the datasheet.	AC18		
		If the I^2C interface is not used an external **3.3 KΩ** pull-up resistor to **3.3V** should be used for both: **SCL1** and the **SDA1** pins. For valid pull-up value range please consult the datasheet.	AD17 and AC18		

SECTION	CHECK ITEM	DETAIL	BALL	Done	COMMENTS AND FEEDBACK
MAUI Port 1	Connect SDPs.	Use these signals as needed for miscellaneous PHY control signals like reset, signal detect, transmit disable, module detect and others. These pins can be configured to operate in native (hardware-determined function) mode or as a GPIO controlled by software. For more information on function, default value and I/O direction consult the datasheet.			
		Please note that these pins use **3.3V** signaling. If necessary use level shifters.			
		SDPs that are not used should be left unconnected.			
	SDP connections for SFI designs.	**SDP1_0** connects to the **RX_LOS pin (8)** on the SFP cage.	AC16		
		SDP1_0 is also pulled up to **3.3V** with a **10 KΩ** resistor.	AC16		

SECTION	CHECK ITEM	DETAIL	BALL	Done	COMMENTS AND FEEDBACK
MAUI Port 1	SDP connections for SFI designs.	**SDP1_1** connects to **RX_LOS pin (8)** on the SFP cage using an inverter. The inverter input is connected to RX_LOS pin (8) from the SFP cage, and the output is connected to the 82599	AB16		
		SDP1_2 connects to **MOD_ABS pin (6)** using an inverter. The inverter input is connected to MOD_ABS pin on the SFP cage, and the output is connected to the 82599.	AB17		
		SDP1_3 connects to **TX_DISABLE pin (3)** on the SFP cage.	AA17		
		SDP1_3 should have a stuffing option to pull down to **ground** through **100 Ω** resistor.	AA17		
		SDP1_4 is available for use as a GPIO if desired. If not used, leave unconnected.	AA16		

SECTION	CHECK ITEM	DETAIL	BALL	Done	COMMENTS AND FEEDBACK
MAUI Port 1	SDP connections for SFI designs.	Connect **RS1 pin (9)** and **RS0 pin (7)** on the SFP+ cage to form **RS0/RS1_SENSE**	AC15		
		SDP1_5 connects to **RS0/RS1_SENSE** through a **1.5 KΩ** resistor.	AC15		
		SDP1_5 is also pulled up to **3.3V** with a **1.5 KΩ** resistor.	AC15		
		SDP1_6 connects to **RS0/RS1_SENSE**	AB15		
		SDP1_7 connects to TX_FAULT pin (2) on the SFP cage.	AA15		
		SDP1_7 is also pulled up to **3.3V** with a **10 KΩ** resistor.	AA15		
		MOD_ABS pin (6) on the SFP connector is pulled to **3.3V** using a **10 KΩ** resistor.	AB17		

SECTION	CHECK ITEM	DETAIL	BALL	Done	COMMENTS AND FEEDBACK
Clock Source	Choose an appropriate clocking option for your design.	There are two options to choose from: - connect a 25 MHz crystal. - use an external 25 MHz differential reference clock. For more details please consult the datasheet.			
	Crystal oscillator mode.	To configure the chip for crystal oscillator mode pull the **OSC_SEL** pin low with a **100 Ω** resistor. For valid pull-down value range please consult the datasheet.	AA9		
		Configure for a 25 MHz reference clock frequency by pulling **OSC_FREQ_SEL** up to **3.3V** using an **8.2 KΩ** resistor. For valid pull-up value range please consult the datasheet.	AC6		

82599 Schematic Checklist

SECTION	CHECK ITEM	DETAIL	BALL	Done	COMMENTS AND FEEDBACK
Clock Source	Crystal oscillator mode.	Choose a 25 MHz crystal that meets the specifications in the datasheet and connect it between **REFCLKIN_p** and **REFCLKIN_n**.	P1 and P2		
		Connect a **20 pF** load capacitor to from both **REFCLKIN_p** and **REFCLKIN_n** to ground.	P1 and P2		
	External reference clock.	To configure the chip to accept an external differential reference clock pull the **OSC_SEL** pin up to **3.3V** using an **8.2 KΩ** resistor. For valid pull-up value range please consult the datasheet.	AA9		
		Configure for **25 MHz** reference clock pull **OSC_FREQ_SEL** up to **3.3V** using an **8.2 KΩ** resistor to configure the multipliers accordingly. For valid pull-up value range please consult the datasheet.	AC6		

SECTION	CHECK ITEM	DETAIL	BALL	Done	COMMENTS AND FEEDBACK
Clock Source	External reference clock.	Please choose an oscillator with an LVPECL or CML output buffer that meets the AC/DC requirements described in the datasheet. A fixed crystal oscillator is preferred over the programmable crystal oscillators because of the smaller resulting jitter . For valid pull-up value range please consult the datasheet.			
		If the clock generator has an **LVPECL** output, terminate the **P** and **N** clock signals to ground via **147** Ω resistors near the driver, and also use two **26** Ω serial resistors after the termination but before connecting to the AC coupling. For valid pull-up value range please consult the datasheet.			
		If the clock generator has a **CML** output, use **26** Ω serial resistors near the driver on both the **P** and **N** clock signals.			

82599 Schematic Checklist

SECTION	CHECK ITEM	DETAIL	BALL	Done	COMMENTS AND FEEDBACK
Clock Source	External reference clock.	Connect the differential clock input (**RCLEXTP** and **RCLKEXTN**) to the external differential clock source through **0.1 µF** AC coupling capacitors.	P1 and P2		
		Add a **0.1 µF** decoupling capacitor close to the clock generator's power pin. Optionally, a ferrite bead could be used to filter the oscillator's supply.			
JTAG Interface	Connect JTAG signals to system JTAG chain.	JTAG clock signal (**JTCK**) should be connected to JTAG clock signal of the platform.	B16		
		JTAG clock signal (**JTCK**) should be connected to an external **470 Ω** pull-down resistor. This prevents unwanted toggling when the interface is not active. For valid pull-down value range please consult the datasheet.	B16		

SECTION	CHECK ITEM	DETAIL	BALL	Done	COMMENTS AND FEEDBACK
JTAG Interface	Connect JTAG signals to system JTAG chain.	JTAG data input signal (**JTDI**) should be connected to JTAG data output of the platform.	A13		
		JTAG data input signal (**JTDI**) should be connected to an external **8.2 KΩ** pull-up resistor to **3.3V**. For valid pull-up value range please consult the datasheet.	A13		
		JTAG data output signal (**JTDO**) should be connected to JTAG data input signal of the platform.	B15		
		JTAG data output signal (**JTDO**) should be connected to an external 3.3 **KΩ** pull-up resistor to **3.3V**. Previous to 6/25/09, Datasheet, checklist & reference schematics all used 8.2 KΩ as recommended value.	B15		
		JTAG mode select signal (**JTMS**) should be connected to JTAG TMS signal of the platform.	B13		

SECTION	CHECK ITEM	DETAIL	BALL	Done	COMMENTS AND FEEDBACK
JTAG Interface	Connect JTAG signals to system JTAG chain.	JTAG mode select signal (**JTMS**) should be connected to an external **8.2 KΩ** pull-up resistor to **3.3V**. For valid pull-up value range please consult the datasheet.	B13		
		JTAG reset (**JRST_N**) signal has to be connected to an external **470 Ω** pull-down resistor. For valid pull-up value range please consult the datasheet.	B14		
	If the JTAG interface is not connected to the system the following resistors should still be in place.	JTAG clock signal (**JTCK**) should be connected to an external **470 Ω** pull-down resistor. For valid pull-up value range please consult the datasheet.	B16		
		JTAG data input signal (**JTDI**) should be connected to an external **8.2 KΩ** pull-up resistor to **3.3V**. For valid pull-up value range please consult the datasheet.	A13		

SECTION	CHECK ITEM	DETAIL	BALL	Done	COMMENTS AND FEEDBACK
JTAG Interface	If the JTAG interface is not connected to the system the following resistors should still be in place.	JTAG mode select signal (**JTMS**) should be connected to an external **8.2 KΩ** pull-up resistor to **3.3V**. For valid pull-up value range please consult the datasheet.	B13		
		JTAG data output signal (**JTDO**) should be left unconnected.	B15		
		JTAG reset (**JRST_N**) signal has to be connected to an external **470 Ω** pull-down resistor. For valid pull-down value range please consult the datasheet.	B14		
Power Good and Reset	If internal Power On Reset (POR) is used.	**POR_BYPASS** signal should be connected to **GND** through a **100 Ω** pull-down resistor.	D19		

SECTION	CHECK ITEM	DETAIL	BALL	Done	COMMENTS AND FEEDBACK
Power Good and Reset	If internal Power On Reset (POR) is used.	**LAN_PWR_GOOD** should be left unconnected. This enables the internal POR. For valid pull-down value range please consult datasheet.	A14		
	If internal POR is not used. (Recommend using external LAN_POWER_GOOD if power rails can't meet the start-up timings detailed in the datasheet).	**POR_BYPASS** signal should be pulled up to the **3.3V** supply through a **8.2 KΩ** resistor. This disables internal POR. For valid pull-up value range please consult the datasheet.	D19		
		LAN_PWR_GOOD should be connected to an external power monitoring solution. This serves as a reset signal. For more details see the datasheet.	A14		

SECTION	CHECK ITEM	DETAIL	BALL	Done	COMMENTS AND FEEDBACK
Misc Signals	Connect main power OK signal.	Main power OK signal (**MAIN_PWR_OK**) should be connected externally to a signal indicating the power supplied to the 82599 is derived from the MAIN supply. This is typically achieved by connecting this pin to a 8.2KΩ pull up resistor to 3.3V. For more detail please see the datasheet.	AC9		
	Connect auxiliary power indicator.	When **present**: auxiliary power indicator signal (**AUX_PWR**) should be connected to **3.3V AUX** through an external **3.3 KΩ** resistor, if AUX power is available. For valid pull-up value range please consult the datasheet.	AB9		

SECTION	CHECK ITEM	DETAIL	BALL	Done	COMMENTS AND FEEDBACK
Misc Signals	Connect auxiliary power indicator.	When **not present**: auxiliary power indicator signal (**AUX_PWR**) should be connected ground through an external **100 Ω** resistor. For valid pull-down value range please consult the datasheet.	AB9		
	Connect LAN disable signals.	LAN disable port 0 signal (**LAN0_DIS_N**) should be connected to an external I/O C4dedicated to this function. If LAN disable is not used, pull up or pull down resistors can be used to statically enable or disable the LAN ports. For valid pull-up/pull-down value range please consult the datasheet.	AD21		
		LAN disable port 1signal (**LAN1_DIS_N**) should be connected to an external I/O dedicated to this function.	AD20		

SECTION	CHECK ITEM	DETAIL	BALL	Done	COMMENTS AND FEEDBACK
Reserved Signals	RSVDxxx_NC signals.	Reserved signals (RSVDA11_NC, RSVDA12_NC, RSVDA17_NC, RSVDA20_NC, RSVDA21_NC, RSVDB10_NC, RSVDB11_NC, RSVDB12_NC, RSVDB17_NC, RSVDB8_NC, RSVDB9_NC, RSVDC10_NC, RSVDC11_NC, RSVDC12_NC, RSVDC13_NC, RSVDC14_NC, RSVDC15_NC, RSVDC16_NC, RSVDC17_NC, RSVDC18_NC, RSVDC7_NC, RSVDC8_NC, RSVDC9_NC, RSVDD10_NC, RSVDD11_NC, RSVDD12_NC, RSVDD13_NC, RSVDD14_NC, RSVDD15_NC, RSVDD16_NC, RSVDD17_NC, RSVDD18_NC, RSVDD7_NC, RSVDD8_NC, RSVDD9_NC, RSVDE11_NC, RSVDE13_NC, RSVDE15_NC, RSVDE9_NC, RSVDJ6_NC, RSVDJ7_NC, RSVDL23_NC, RSVDL24_NC, RSVDM1_NC, RSVDM2_NC, RSVDM20_NC, RSVDM21_NC, RSVDN1_NC, RSVDN2_NC, RSVDN20_NC, RSVDN21_NC, RSVDN4_NC, RSVDN5_NC, RSVDT6_NC, RSVDT7_NC, RSVDW20_NC, RSVDW21_NC, RSVDY11_NC, RSVDY13_NC, RSVDY15_NC, RSVDY17_NC and RSVDY18_NC) should NOT be connected on the board.			

SECTION	CHECK ITEM	DETAIL	BALL	Done	COMMENTS AND FEEDBACK
Reserved Signals	Connect RSVDxxx_VSS pins.	Reserved signals (**RSVDF21_VSS**, **RSVDV16_VSS**, **RSVDW16_VSS**, **RSVDE17_VSS** and **RSVDY9_VSS**) should each be connected to **GND** through **100 Ω** pull-down resistors (one for each pin). For valid pull-down value range please consult the datasheet.			
No Connect Signals	NC_xxx signals.	No connect signals (**NC_Y16 , NC_Y14 , NC_Y12 , NC_Y10 , NC_Y8 , NC_U7, NC_E10**, **NC_E12**, **NC_E14**, **NC_E16**, **NC_E18**, **NC_E8**, **NC_F20**, **NC_H7**, **NC_L4**, and **NC_P4**) should **NOT** be connected on the board.			
Power Supply Connections	Connect 3.3V supply.	3.3V voltage supply signals (**VCC3P3**) should be connected to **3.3V** supply voltage.			

SECTION	CHECK ITEM	DETAIL	BALL	Done	COMMENTS AND FEEDBACK
Power Supply Connections	Connect 3.3V supply.	3.3V voltage supply signals (**VCC3P3**) should be connected to decoupling capacitors as specified in the datasheet.			
	High-speed decoupling and bulk capacitors for 3.3V supply.	The minimum acceptable decoupling by power supply is as follows (including decoupling only for the LAN silicon):			
		VCC3P3 decoupling: **44 µF** bulk **(2x 22 µF)** **8x 0.1 µF** high speed			
	Connect 1.2V supply.	1.2V voltage supply signals (**VCC1P2**) should be connected to **1.2V** supply voltage.			
		1.2V voltage supply signals (**VCC1P2**) should be connected to decoupling capacitors as specified in the datasheet.			

SECTION	CHECK ITEM	DETAIL	BALL	Done	COMMENTS AND FEEDBACK
Power Supply Connections	High-speed decoupling and bulk capacitors for 1.2V supply.	The minimum acceptable decoupling by power supply is as follows (including decoupling only for the LAN silicon):			
		VCC1P2 decoupling: **132 µF** bulk (**6x 22 µF**) **6x 1 µF** distributed bulk under the BGA **36x 0.1 µF** high speed 1**2x 1 nF** high speed			
	Power sequencing.	Make sure the design follows the power sequencing requirements detailed in the datasheet.			

SECTION	CHECK ITEM	DETAIL	BALL	Done	COMMENTS AND FEEDBACK
Power Supply Connections	Connect ground	Ground signals (VSS) should be connected to the ground of the board. Refer to the datasheet for pin numbers.			

82599 Layout and Placement Checklist

SECTION	CHECK ITEM	DETAIL	BALL	Done	COMMENTS AND FEEDBACK
General					
	Have up to date documentation and specification updates.	Documents are subject to frequent change. Make sure to download the latest collateral release			
	Provide board stack up information	Please include details such as dielectric constant, thickness, loss tangent, etc.			
	Observe special instructions for some of the interfaces that need special attention.				

82599 Layout and Placement Checklist

SECTION	CHECK ITEM	DETAIL	BALL	Done	COMMENTS AND FEEDBACK
Component Placement	82599 controller.	Place the 82599 controller silicon at least one inch from the edge of the board. If the 82599 controller is closer to the board edge, the strongest fields do not have path to GND and might cause EMI problems.			
	PCIe bias resistor.	Place the **PE_RBIAS** resistor close to the 82599 controller such that total etch length connecting it to the BGA balls is less than 1 inch.			

82599 Layout and Placement Checklist

SECTION	CHECK ITEM	DETAIL	BALL	Done	COMMENTS AND FEEDBACK
Component Placement	MAUI bias resistor.	Place the **XA_RBIAS** resistor close to the 82599 controller such that total etch length connecting it to the BGA balls is less than 1 inch.			
	25 MHz crystal.	Place the crystal close to the 82599 controller such that total etch length connecting it to the BGA balls is less than 1.5 inches. Apply either the crystal or the oscillator checklist items based on your reference clock choice.			
		Place the load capacitors less than 200 mils from the crystal pads.			

82599 Layout and Placement Checklist

SECTION	CHECK ITEM	DETAIL	BALL	Done	COMMENTS AND FEEDBACK
Component Placement	25 MHz oscillator.	Place oscillator as close to the 82599 controller as possible.			
		Use appropriate decoupling and place the cap close to the power pins of the oscillator chip.			
		Place the clock termination (2x 147 Ω & 2x 26 Ω) close to the oscillator's output (<250 mils)			
		Place the AC coupling capacitors as close to the 82599 controller as possible (<250 mil)			
	High-speed AC coupling capacitor.	See details broken out by interface further down.			

82599 Layout and Placement Checklist

SECTION	CHECK ITEM	DETAIL	BALL	Done	COMMENTS AND FEEDBACK
Component Placement	Decoupling capacitors.	Distribute the big bulk capacitors evenly on all four sides of the BGA package.			
		Distribute the small (0402) 1 µF bulk capacitors evenly under the BGA package. It is likely that use of "via in pad" is required to achieve the required density.			
		Distribute the rest of the high-speed decoupling capacitors evenly on the back side of the board, right under the BGA package.			

82599 Layout and Placement Checklist

SECTION	CHECK ITEM	DETAIL	BALL	Done	COMMENTS AND FEEDBACK
Component Placement	EEPROM and Flash.	Placement of the EEPROM and Flash devices is not critical but they should be kept as close as possible.			
		The decoupling caps for these devices should be placed close to their power pin.			

82599 Layout and Placement Checklist

SECTION	CHECK ITEM	DETAIL	BALL	Done	COMMENTS AND FEEDBACK
Component Placement	Manageability Controller (MC).	If there's a MC connected to the 82599 controller over the NC-SI interface, make sure to place the two chips close enough such that the maximum trace lengths detailed in the datasheet are not exceeded. For more detail please consult the datasheet.			
General Routing	Choose the stackup carefully.	Take in consideration that most of the high-speed interfaces are preferred to be routed on stripline rather than microstrip.			

82599 Layout and Placement Checklist

SECTION	CHECK ITEM	DETAIL	BALL	Done	COMMENTS AND FEEDBACK
General Routing	Choose the stackup carefully.	Due to high signal density, a minimum of an 8 layer board is necessary. For some possible stackup examples, please consult the datasheet.			
	Route the high-speed interfaces first.	Routing the PCI-Express* (PCIe*) and KX/KX4/KR/CX4/XAUI differential traces should be done prior the rest of the digital interfaces. Consult the datasheet for more detail.			

82599 Layout and Placement Checklist

SECTION	CHECK ITEM	DETAIL	BALL	Done	COMMENTS AND FEEDBACK
General Routing	Route the high-speed interfaces first.	Routing of power rails should have the second highest priority, followed by the sideband and miscellaneous signals.			
	Separate analog and digital domains.	To maintain best signal integrity, keep digital signals far away from the analog traces.			
		No digital signal should be within 7 to 10 times the dielectric height of the differential pairs.			

82599 Layout and Placement Checklist

SECTION	CHECK ITEM	DETAIL	BALL	Done	COMMENTS AND FEEDBACK
General Routing	Separate analog and digital domains.	If digital signals on other board layers cannot be separated from the high-speed differential signals by a ground plane, they should be routed at a right angle (90 degrees) to the differential pairs.			
	Avoid EMI issues.	Keep high-speed traces greater than **100 mils** from the board edge. This includes both: high-speed analog signals and sideband signals with high frequency content (fast rising/falling edges).			

82599 Layout and Placement Checklist

SECTION	CHECK ITEM	DETAIL	BALL	Done	COMMENTS AND FEEDBACK
General Routing	Avoid EMI issues.	Provide short return path for each signal.			
		Avoid slots in the return path that can act as slot antennas.			
Reference Clock Routing	General.	Keep the clock traces at least 15 mils away from other signals. This includes spacing to other digital traces, I/O ports, or any other differential pairs.			
		Also keep clock sources away from board edge.			
	25 MHz crystal.	Route the clock signals as a 100 Ω differential pair.			

82599 Layout and Placement Checklist

SECTION	CHECK ITEM	DETAIL	BALL	Done	COMMENTS AND FEEDBACK
Reference Clock Routing	25 MHz crystal.	The clock traces should be the shortest possible, less than 1.5 inches.			
		Connect the grounded side of the load capacitors to the ground plane through a short trace to a via.			
	25 MHz oscillator.	Route the clock signals as a 100 Ω differential pair with the shortest possible length.			
		The clock traces should be the shortest possible.			

82599 Layout and Placement Checklist

SECTION	CHECK ITEM	DETAIL	BALL	Done	COMMENTS AND FEEDBACK
PCIe Interface	AC coupling capacitors.	Recommended AC coupling capacitor package size is **0402** or **0201.** X7R or X5R (or better) type capacitors.			
		Place AC coupling capacitors close to the transmitter (within **1 inch**).			
		Grouping discontinuities can help reduce reflections. If the signal needs to change routing layers it is to do that within 100 mils from the AC coupling capacitors.			

82599 Layout and Placement Checklist

SECTION	CHECK ITEM	DETAIL	BALL	Done	COMMENTS AND FEEDBACK
PCIe Interface	Reduce parasitic capacitance.	Place the AC coupling capacitors in a staggered formation, to reduce the package-to-package parasitic capacitance. For more detail please consult the datasheet.			
		An alternate solution would be to increase the distance between them to at least **30 mils.** For more detail please consult the datasheet.			

82599 Layout and Placement Checklist

SECTION	CHECK ITEM	DETAIL	BALL	Done	COMMENTS AND FEEDBACK
PCIe Interface	Reduce parasitic capacitance.	Void the reference plane right under the AC coupling capacitors to reduce the parasitic capacitance to the reference plane. For more detail please consult the datasheet.			
	Trace geometry and orientation.	The preferred trace geometry is stripline, but microstrip topologies can be used successfully as well.			
		Design traces for **85 Ω** differential impedance (**± 10%**).			

82599 Layout and Placement Checklist

SECTION	CHECK ITEM	DETAIL	BALL	Done	COMMENTS AND FEEDBACK
PCIe Interface	Trace geometry and orientation.	If 1 oz copper is used, minimum trace spacing within each differential pair must be >= 8 mils.			
		Keep traces relatively close together within differential pairs (6 to 10 mils edge to edge within a differential pair).			
		For long distances, thick traces are preferred over wide traces. Modify board stackup if necessary to avoid highly resistive traces.			

82599 Layout and Placement Checklist

SECTION	CHECK ITEM	DETAIL	BALL	Done	COMMENTS AND FEEDBACK
PCIe Interface	Trace geometry and orientation.	Long traces from the 82599 controller to the root complex are allowed to be up to **50 cm** or **20 inches** on **FR4** material, but avoid highly resistive traces. Take into consideration the entire channel length (chip-to-chip).			
		Choosing a dielectric material with lower loss tangent and using wider traces might enable longer PCIe traces.			

82599 Layout and Placement Checklist

SECTION	CHECK ITEM	DETAIL	BALL	Done	COMMENTS AND FEEDBACK
PCIe Interface	Trace geometry and orientation.	As much as possible, traces should be routed at an angle of 11º to 45º to the FR4 weave to maintain consistent impedance. For more detail please consult the datasheet.			
		If differential traces must be straight and orthogonal to the outline of the circuit board for most of their routed lengths, then rotate the CAD artwork by ~15°.			

82599 Layout and Placement Checklist

SECTION	CHECK ITEM	DETAIL	BALL	Done	COMMENTS AND FEEDBACK
PCIe Interface	Reference planes.	Use a quiet reference plane, preferably ground. If the differential traces are sandwiched between a power and ground plane, use an offset stripline structure (**H, 3H**), keeping the pairs closer to the ground plane. For more information, consult the datasheet.			
		When differential signals transition from one board layer to another, place stitching vias within **40 mils** of the signal vias to connect the reference planes.			

82599 Layout and Placement Checklist

SECTION	CHECK ITEM	DETAIL	BALL	Done	COMMENTS AND FEEDBACK
PCIe Interface	Reference planes.	If the differential signals transition from a ground referenced layer to a power referenced layer, place a decoupling capacitor on the power and ground within **40 mils** of the signal vias.			
		Differential traces should not cross plane splits. If this is not possible, AC coupling capacitors must be added to connect the two different reference planes.			

82599 Layout and Placement Checklist

SECTION	CHECK ITEM	DETAIL	BALL	Done	COMMENTS AND FEEDBACK
PCIe Interface	Reference planes.	Differential traces should be kept away from plane splits, voids, or the reference plane edge by 6 times the dielectric height.			
	Vias.	Use smallest possible vias on board.			
		Use ground vias adjacent to any signal via.			
		Remove via pads on inner layers with no connections.			

SECTION	CHECK ITEM	DETAIL	BALL	Done	COMMENTS AND FEEDBACK
PCIe Interface	Vias.	Anti-pad must be at least 20 mils larger than the pad diameter. Anti-pad diameter = via pad diameter + 20 mils. Implication on internal layers – no signal or plane should be within this region; external layers – you are only limited by the spacing guidelines.			
		There should be no copper separating the signal vias on any metal layer (including GND and power layers). When differential signals cross metal planes, use appropriate keep-outs to prevent separation.			

82599 Layout and Placement Checklist

SECTION	CHECK ITEM	DETAIL	BALL	Done	COMMENTS AND FEEDBACK
PCIe Interface	Vias.	Minimize through holes (vias): If using vias, the maximum plated through hole budget from chip to chip is **6** per trace. This can be a combination of 10 mil finished hole size vias and through holes for connector pins.			
	Stubs.	Avoid unused pads and stubs along the differential traces. The vias should carry the signal to the opposite side of the circuit board.			

82599 Layout and Placement Checklist

SECTION	CHECK ITEM	DETAIL	BALL	Done	COMMENTS AND FEEDBACK
PCIe Interface	Stubs.	When transitioning to a different routing layer try to minimize the stubs resulting from the extra length of the via by choosing the routing layers carefully.			
		Length of via stubs should be kept under **35 mils**.			
	Breakout area.	Keep its length under **200 mils**. Use this area to get the signals out from under the BGA package.			
	Symmetry.	The traces within a differential pair have to be symmetric.			

82599 Layout and Placement Checklist

SECTION	CHECK ITEM	DETAIL	BALL	Done	COMMENTS AND FEEDBACK
PCIe Interface	Symmetry.	Adjacent ground vias must be symmetric with respect to the differential traces. Helps reduce the imbalance that can occur in the different return current paths.			
	Do not make 90° bends.	Bevel corners with turns based on **45°** angles.			
		Radius bends can also be used.			
	Differential skew.	Trace lengths should be equal within **5 mils** in each differential pair.			

82599 Layout and Placement Checklist

SECTION	CHECK ITEM	DETAIL	BALL	Done	COMMENTS AND FEEDBACK
PCIe Interface	Differential skew.	Try to match the pairs at pads, vias and turns. Establish routing rules carefully. Asymmetry contributes to impedance mismatch.			
	Pair-to-pair skew.	Pair-to-pair skew should be less than **1 inch**. This applies to the Tx of one port and to the Rx of the same port independently.			
	Differential trace spacing.	In case of **Microstrip,** routing the minimum distance between the differential pairs is **7 times** the dielectric height.			

82599 Layout and Placement Checklist

SECTION	CHECK ITEM	DETAIL	BALL	Done	COMMENTS AND FEEDBACK
PCIe Interface	Differential trace spacing.	In case of **Stripline,** routing the minimum distance between the differential pairs is **6 times** the dielectric height.			
		Avoid broadside coupling to traces on other layers. The broadside effect significantly increases the insertion loss and reduces signal quality.			

82599 Layout and Placement Checklist

SECTION	CHECK ITEM	DETAIL	BALL	Done	COMMENTS AND FEEDBACK
PCIe Interface	Differential trace spacing.	Do not guard the differential traces with adjacent ground fill or ground traces. It's acceptable to put ground fill or thieving on the trace layers, but not closer than 50 mils to the differential traces and connector pins.			
		The differential pair should be kept away from ground fills or ground traces by at least the minimum pair-to-pair distance (**6 times** the dielectric height).			

82599 Layout and Placement Checklist

SECTION	CHECK ITEM	DETAIL	BALL	Done	COMMENTS AND FEEDBACK
PCIe Interface	Differential trace spacing.	The differential pair should be kept away from the edge of the reference plane by at least the minimum pair-to-pair distance (**6/7 times** the dielectric height depending on trace topology).			
	Differential trace grouping.	Tx and Rx differential traces should be kept separate. Helps to minimize crosstalk effects.			
XAUI / BX / KX / KX4 / CX4 Interface	AC coupling capacitors.	Recommended AC coupling capacitor package size is **0402** or **0201.** NOTE: X7R or X5R (or better) type capacitors.			

82599 Layout and Placement Checklist

SECTION	CHECK ITEM	DETAIL	BALL	Done	COMMENTS AND FEEDBACK
XAUI / BX / KX / KX4 / CX4 Interface	AC coupling capacitors.	Place AC coupling capacitors close to the receiver (within **1 inch**).			
	Trace geometry and orientation.	The preferred trace geometry is stripline, but microstrip topologies can be used successfully as well.			
		Design traces for **100 Ω** differential impedance (**± 10%**).			
		For long distances, thick traces are preferred over wide traces. Modify board stackup if necessary to avoid highly resistive traces.			

82599 Layout and Placement Checklist

SECTION	CHECK ITEM	DETAIL	BALL	Done	COMMENTS AND FEEDBACK
XAUI / BX / KX / KX4 / CX4 Interface	Trace geometry and orientation.	Long traces from the 82599 controller to the link partner are allowed to be up to **50 cm** or **20 inches** on **FR4** material, but avoid highly resistive traces. Take into consideration the entire channel length. That includes the backplane and the traces on the link partner side.			

82599 Layout and Placement Checklist

SECTION	CHECK ITEM	DETAIL	BALL	Done	COMMENTS AND FEEDBACK
XAUI / BX / KX / KX4 / CX4 Interface	Trace geometry and orientation.	As much as possible, traces should be routed at an angle of 11º to 45º to the FR4 weave to maintain consistent impedance. For more information consult the datasheet.			
		If differential traces must be straight and orthogonal to the outline of the circuit board for most of their routed lengths, then rotate the CAD artwork by ~15°.			

82599 Layout and Placement Checklist

SECTION	CHECK ITEM	DETAIL	BALL	Done	COMMENTS AND FEEDBACK
XAUI / BX / KX / KX4 / CX4 Interface	Reference planes.	Use a quiet reference plane, preferably ground. If the differential traces are sandwiched between a power and ground plane, use an offset stripline structure (**H, 3H**), keeping the pairs closer to the ground plane. For more information consult the datasheet.			
		When differential signals transition from one board layer to another, place stitching vias within **40 mils** of the signal vias to connect the reference planes.			

82599 Layout and Placement Checklist

SECTION	CHECK ITEM	DETAIL	BALL	Done	COMMENTS AND FEEDBACK
XAUI / BX / KX / KX4 / CX4 Interface	Reference planes.	If the differential signals transition from a ground referenced layer to a power referenced layer, place a decoupling cap on the power and ground within **40 mils** of the signal vias.			
		Differential traces should not cross plane splits. If this is not possible, AC coupling caps must be added to connect the two different reference planes.			

82599 Layout and Placement Checklist

SECTION	CHECK ITEM	DETAIL	BALL	Done	COMMENTS AND FEEDBACK
XAUI / BX / KX / KX4 / CX4 Interface	Reference planes.	Differential traces should be kept away from plane splits, voids, or the reference plane edge by 6 times the dielectric height.			
	Vias.	Use smallest possible vias on board.			
		Use ground vias adjacent to any signal via.			
		Remove via pads on inner layers with no connections.			

SECTION	CHECK ITEM	DETAIL	BALL	Done	COMMENTS AND FEEDBACK
XAUI / BX / KX / KX4 / CX4 Interface	Vias.	Anti-pad must be at least 20 mils larger than the pad diameter. Anti-pad diameter = via pad diameter + 20 mils. Implication on internal layers – no signal or plane should be within this region; external layers – you are only limited by the spacing guidelines.			
		There should be no copper separating the signal vias on any metal layer (including GND and power layers). When differential signals cross metal planes, use appropriate keep-outs to prevent separation.			

82599 Layout and Placement Checklist

SECTION	CHECK ITEM	DETAIL	BALL	Done	COMMENTS AND FEEDBACK
XAUI / BX / KX / KX4 / CX4 Interface	Vias.	Minimize through holes (vias): If using vias, the maximum plated through hole budget from chip to chip is **6** per trace. This can be a combination of 10 mil finished hole size vias and through holes for connector pins.			
	Stubs.	Avoid unused pads and stubs along the differential traces.			

82599 Layout and Placement Checklist

SECTION	CHECK ITEM	DETAIL	BALL	Done	COMMENTS AND FEEDBACK
XAUI / BX / KX / KX4 / CX4 Interface	Stubs.	When transitioning to a different routing layer try to minimize the stubs resulting from the extra length of the via by choosing the routing layers carefully. The vias should carry the signal to the opposite side of the circuit board.			
		Length of via stubs should be kept under **35 mils**.			
	Breakout area.	Keep its length under **200 mils**. Use this area to get the signals out from under the BGA package.			

82599 Layout and Placement Checklist

SECTION	CHECK ITEM	DETAIL	BALL	Done	COMMENTS AND FEEDBACK
XAUI / BX / KX / KX4 / CX4 Interface	Symmetry.	The traces within a differential pair have to be symmetric.			
		Adjacent ground vias must be symmetric with respect to the differential traces. Helps reduce the imbalance that can occur in the different return current paths.			
	Do not make 90° bends.	Bevel corners with turns based on **45°** angles.			
		Radius bends can also be used.			

82599 Layout and Placement Checklist

SECTION	CHECK ITEM	DETAIL	BALL	Done	COMMENTS AND FEEDBACK
XAUI / BX / KX / KX4 / CX4 Interface	Differential skew.	Trace lengths should be equal within **5 mils** in each differential pair.			
		Try to match the pairs at pads, vias and turns. Establish routing rules carefully. Asymmetry contributes to impedance mismatch.			
	Pair-to-pair skew.	Pair-to-pair skew should be less than **100 mils**. This applies to the Tx of one port and to the Rx of the same port separately.			

SECTION	CHECK ITEM	DETAIL	BALL	Done	COMMENTS AND FEEDBACK
XAUI / BX / KX / KX4 / CX4 Interface	Differential trace spacing.	In case of **Microstrip** routing the minimum distance between the differential pairs is **7 times** the dielectric height.			
		In case of **Stripline** routing the minimum distance between the differential pairs is **6 times** the dielectric height.			
		Avoid broadside coupling to traces on other layers. The broadside effect will significantly increase the insertion loss and reduce signal quality.		.	

82599 Layout and Placement Checklist

SECTION	CHECK ITEM	DETAIL	BALL	Done	COMMENTS AND FEEDBACK
XAUI / BX / KX / KX4 / CX4 Interface	Differential trace spacing.	Do not guard the differential traces with adjacent ground fill or ground traces. It's acceptable to put ground fill or thieving on the trace layers, but not closer than 50 mils to the differential traces and connector pins.			
		The differential pair should be kept away from ground fills or ground traces by at least the minimum pair-to-pair distance (**6 times** dielectric height).			

82599 Layout and Placement Checklist

SECTION	CHECK ITEM	DETAIL	BALL	Done	COMMENTS AND FEEDBACK
XAUI / BX / KX / KX4 / CX4 Interface	Differential trace spacing.	The differential pair should be kept away from the edge of the reference plane by at least the minimum pair-to-pair distance (**6/7 times** the dielectric height depending on trace topology).			
	Differential trace grouping.	Tx and Rx differential traces should be kept separate.C4 Helps to minimize crosstalk effects.			
	Silk screen.	Make sure that there is no silk screen (text or other symbols) on top of the differential pairs.			

SECTION	CHECK ITEM	DETAIL	BALL	Done	COMMENTS AND FEEDBACK
KR / SFI Interface	AC coupling capacitors.	Recommended AC coupling capacitor package size is **0402** or **0201.** X7R or X5R (or better) type capacitors.			
		Place AC coupling capacitors close to the receiver (within **1 inch**).			
		Grouping discontinuities can help reduce reflections. If the signal needs to change routing layers it is best to do that within 100 mils from the AC coupling capacitors.			

SECTION	CHECK ITEM	DETAIL	BALL	Done	COMMENTS AND FEEDBACK
KR / SFI Interface	Reduce parasitic capacitance.	Place the AC coupling capacitors in a staggered formation, to reduce the package-to-package parasitic capacitance.			
		An alternate solution would be to increase the distance between them to at least **30 mils.**			
		Void the reference plane right under the AC coupling capacitors to reduce the parasitic capacitance to the reference plane. For more detail please consult the datasheet.			

82599 Layout and Placement Checklist

SECTION	CHECK ITEM	DETAIL	BALL	Done	COMMENTS AND FEEDBACK
KR / SFI Interface	Trace geometry and orientation.	The preferred trace geometry is stripline, but microstrip topologies can be used successfully as well.			
		Design traces for **100 Ω** differential impedance (**± 10%**).C120 Loosely coupled differential pairs can help avoid the influence of the fiberglass weave on the impedance.			
		For long distances, thick traces are preferred over wide traces. Modify board stackup if necessary to avoid highly resistive traces.			

82599 Layout and Placement Checklist

SECTION	CHECK ITEM	DETAIL	BALL	Done	COMMENTS AND FEEDBACK
KR / SFI Interface	Trace geometry and orientation.	Long traces from the 82599 controller to the link partner are allowed to be up to: **50 cm or 19 inches** on **FR4** material (KR) **2 cm** or **0.8 inches** (SFI) Avoid highly resistive traces. Take into consideration the entire channel length. This includes the backplane and the traces on the link partner side.			

82599 Layout and Placement Checklist

SECTION	CHECK ITEM	DETAIL	BALL	Done	COMMENTS AND FEEDBACK
KR / SFI Interface	Trace geometry and orientation.	Choosing a dielectric material with lower loss tangent and using wider traces might enable longer KR traces. It is highly recommended to used improved materials for SFI implementations			
		Traces should be routed at an angle of 11º to 45º to the FR4 weave to maintain consistent impedance.			

82599 Layout and Placement Checklist

SECTION	CHECK ITEM	DETAIL	BALL	Done	COMMENTS AND FEEDBACK
KR / SFI Interface	Trace geometry and orientation.	If differential traces must be straight and orthogonal to the outline of the circuit board for most of their routed lengths, then rotate the CAD artwork by ~15°.			
		Use a quiet reference plane, preferably ground. If the differential traces are sandwiched between a power and ground plane, use an offset stripline structure (**H, 3H**), keeping the pairs closer to the ground plane. +C109For more information consult the datasheet.			

SECTION	CHECK ITEM	DETAIL	BALL	Done	COMMENTS AND FEEDBACK
KR / SFI Interface	Reference planes.	When differential signals transition from one board layer to another, place stitching vias within **40 mils** of the signal vias to connect the reference planes.			
		If the differential signals transition from a ground referenced layer to a power referenced layer, place a decoupling capacitor on the power and ground within **40 mils** of the signal vias.			

82599 Layout and Placement Checklist

SECTION	CHECK ITEM	DETAIL	BALL	Done	COMMENTS AND FEEDBACK
KR / SFI Interface	Reference planes.	Differential traces should not cross plane splits. If this is not possible, AC coupling capacitors must be added to connect the two different reference planes.			
		Differential traces should be kept away from plane splits, voids, or the reference plane edge by 6 times the dielectric height.			
	Vias.	Use smallest possible vias on board.			
		No vias on SFI TX traces			

82599 Layout and Placement Checklist

SECTION	CHECK ITEM	DETAIL	BALL	Done	COMMENTS AND FEEDBACK
KR / SFI Interface	Vias.	Use ground vias adjacent to any signal via.			
		Remove via pads on inner layers with no connections.			
		Anti-pad must be at least 20 mils larger than the pad diameter. Anti-pad diameter = via pad diameter + 20 mils. Implication on internal layers – no signal or plane should be within this region; external layers – you are only limited by the spacing guidelines.			

82599 Layout and Placement Checklist

SECTION	CHECK ITEM	DETAIL	BALL	Done	COMMENTS AND FEEDBACK
KR / SFI Interface	Vias.	There should be no copper separating the signal vias on any metal layer (including GND and power layers). When differential signals cross metal planes, use appropriate keep-outs to prevent separation.			
KR / SFI Interface	Vias.	Minimize through holes (vias): If using vias, the maximum plated through hole budget from chip-to-chip is **4** per trace. This can be a combination of 10 mil finished hole size vias and through holes for connector pins.			

82599 Layout and Placement Checklist

SECTION	CHECK ITEM	DETAIL	BALL	Done	COMMENTS AND FEEDBACK
KR / SFI Interface	Stubs.	There must be no unused pads, test points and stubs along the differential traces.			
		When transitioning to a different routing layer try to minimize the stubs resulting from the extra length of the via by choosing the routing layers carefully. The vias should carry the signal to the opposite side of the circuit board.			
		Length of via stubs has to be kept under **35 mils**, preferably **20 mils**.			

82599 Layout and Placement Checklist

SECTION	CHECK ITEM	DETAIL	BALL	Done	COMMENTS AND FEEDBACK
KR / SFI Interface	Breakout area.	Keep its length under **200 mils**. Use this area to get the signals out from under the BGA package.			
		Making sure the single-ended impedance is 50 Ω in the breakout region helps reduce reflections.			
	Symmetry.	The traces within a differential pair have to be symmetric.			

82599 Layout and Placement Checklist

SECTION	CHECK ITEM	DETAIL	BALL	Done	COMMENTS AND FEEDBACK
KR / SFI Interface	Symmetry.	Adjacent ground vias must be symmetric with respect to the differential traces. Helps reduce the imbalance that can occur in the different return current paths.			
		Using two return path vias per each signal via results in a lower reflection.			
	Do not make 90° bends.	Bevel corners with turns based on **45°** angles.			
		Radius bends can also be used.			

82599 Layout and Placement Checklist

SECTION	CHECK ITEM	DETAIL	BALL	Done	COMMENTS AND FEEDBACK
KR / SFI Interface	Differential skew.	Trace lengths should be equal within **2 mils** in each differential pair.			
		Try to match the pairs at pads, vias and turns. Establish routing rules carefully. Asymmetry contributes to impedance mismatch.			
	Pair-to-pair skew.	Pair-to-pair skew should be less than **100 mils**. C170 This applies to the Tx of one port and to the Rx of the same port independently.			

SECTION	CHECK ITEM	DETAIL	BALL	Done	COMMENTS AND FEEDBACK
KR / SFI Interface	Differential trace spacing.	In case of **Microstrip,** routing the minimum distance between the differential pairs is **7 times** the dielectric height.			
		In case of **Stripline,** routing the minimum distance between the differential pairs is **6 times** the dielectric height.			
		Avoid broadside coupling to traces on other layers. The broadside effect significantly increases the insertion loss and reduces signal quality.			

82599 Layout and Placement Checklist

SECTION	CHECK ITEM	DETAIL	BALL	Done	COMMENTS AND FEEDBACK
KR / SFI Interface	Differential trace spacing.	Do not guard the differential traces with adjacent ground fill or ground traces. It's acceptable to put ground fill or thieving on the trace layers, but not closer than 50 mils to the differential traces and connector pins.			
		The differential pair should be kept away from ground fills or ground traces by at least the minimum pair-to-pair distance (**6 times** dielectric height).			

82599 Layout and Placement Checklist

SECTION	CHECK ITEM	DETAIL	BALL	Done	COMMENTS AND FEEDBACK
KR / SFI Interface	Differential trace spacing.	The differential pair should be kept away from the edge of the reference plane by at least the minimum pair-to-pair distance (**6/7 times** dielectric height depending on trace topology).			
	Differential trace grouping.	Tx and Rx differential traces should be kept separate.			
	Silk screen.	Make sure that there is no silk screen (text or other symbols) on top of the differential pairs.C148 Helps to minimize crosstalk effects.			

82599 Layout and Placement Checklist

SECTION	CHECK ITEM	DETAIL	BALL	Done	COMMENTS AND FEEDBACK
KR / SFI Interface	Special layout considerations for SFI	Stripline is not recommended for SFI.			
		The reference plane areas directly under each pair of SFP module connector pads must be voided.C160 Avoid reference place sharp corners. Consult datasheet for more details and illustration.			
		Traces width should be approximately 12 mils .			
		Keep trace length < 20 mm or 0.8 inches.			

82599 Layout and Placement Checklist

SECTION	CHECK ITEM	DETAIL	BALL	Done	COMMENTS AND FEEDBACK
KR / SFI Interface	Special layout considerations for SFI	Use dielectric materials with low Er (lower dk) and low dissipation factor (df), as the ones recommended on the datasheet. This allows wider SFI traces and reduces SFI traces' insertion loss.			
NC-SI	Make sure to follow the delay recommendations detailed in the datasheet.	This is necessary as a workaround for a minor timing specification violation.			
		Trace-to-trace space should be kept around 3 times the dielectric height to avoid crosstalk issues.			

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SECTION	CHECK ITEM	DETAIL	BALL	Done	COMMENTS AND FEEDBACK
NC-SI	Make sure to follow the delay recommendations detailed in the datasheet.	Clock traces from the clock source to the MC and from the source to the 82599 should be length matched within 5 mils.			
		Total skew between clocks less than 1ns			
	Trace geometry and orientation.	Trace impedance of 50 Ω plus 20% and minus 10%.			
		For direct connect application maximum trace length should be about 8 inches			

82599 Layout and Placement Checklist

SECTION	CHECK ITEM	DETAIL	BALL	Done	COMMENTS AND FEEDBACK
NC-SI	Trace geometry and orientation.	For multidrop applications maximum trace length should be 4 inches between the two packages connected to the same MC.			
Power Supply and Signal Ground	Use planes to deliver power.	Planes have lower inductance and lower resistance than traces.			
		When power planes have to be stitched together use an array of vias. The via size should also be bigger than the one used for high speed signals.			

82599 Layout and Placement Checklist

SECTION	CHECK ITEM	DETAIL	BALL	Done	COMMENTS AND FEEDBACK
Power Supply and Signal Ground	Use planes to deliver power.	Make sure to avoid power planes that resemble swiss cheese due to the huge number of vias piercing through it.			
	Use decoupling and bulk capacitors generously.	Connect the each of the bypass capacitors with traces as wide as possible.			
		For connecting bypass capacitors to the power planes use bigger via size than the via used for high speed signals.			

82599 Layout and Placement Checklist

SECTION	CHECK ITEM	DETAIL	BALL	Done	COMMENTS AND FEEDBACK
LEDs	Keep LED traces away from high speed digital traces running in parallel.	Since LEDs are usually placed so they are easily viewable, these traces can carry noise out to the edge of the board, increasing EMI.			
	If using decoupling capacitors on LED lines, place them carefully.	Capacitors on LED lines should be placed near the LEDs.			