Intel® 82598 10 GbE Controller Checklists

LAN Access Division

Project Name	
Fab Revision	
Date	
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REVISION	DATE	NOTES
0.10	6/10/2006	Initial Draft. Put together based Revision 0.25 of the Reference Schematic.
0.15	7/18/2006	Included Layout and placement checklist.
0.50	2/3/2007	Updated Clock Source Recommendations
0.75	4/2/2007	Following the DMTF spec notations renamed RMII to NCSI; added titles to each section for better print outs, added entries for how-to terminate unused buses; cleaned up many items making sure that the datasheet and the checklist are in sync
0.76	6/11/2007	Added requirement for JRST (ball C2) pull down.
1.00	8/19/2007	Added clarification to JTDO connections when interface is not used, same for PE_WAKE, and updated clock termination.
1.01	10/22/2007	Added checkpoints for LAN_PWR_GOOD and POR_BYPASS
2.1	11/16/2007	Updated, released in support of SDM rev. 2.
2.2	1/18/2008	Corrected typo in the reserved pin list and a typo in the MDIO section for Port0
2.7	3/23/2009	Updated format to add PDF notation functionality. Made corrections.
2.8	7/2/2009	Changed JTDO pull up resistor from 8.2K to 3.3K ohms. Updated format.
2.9	7/7/2009	Created PDF version of checklist Developer posting. Updated XLS is also posted on CDI.
2.91	9/2/2009	Corrected PDF. The FORM version now permits data entry using Acrobat Reader. If you have data entry issues with the form, check and make sure you have a recent edition of the Reader loaded. Several typos also corrected.

9/2/2009

Rev 2.91; 242480-003EN

Schematic Checklist

SECTION	CHECK ITEMS	DETAIL	√ Done or Not done	NOTES AND COMMENTS
General	Have up to date documentation.	Documents are subject to frequent change. Make sure to download the latest collateral release.		
	Observe instructions for special pins needing pull- up or pull-down resistors.	Do not connect pull-up or pull-down resistors to any pins marked No Connect.		
	Optional interfaces are labeled and should be treated appropriately.	There are many optional interfaces for the 82598 that might require unique configurations.		
PCIe Interface	Connect the PCI Express* (PCIe*) transmit signals to the PCIe host.	PCIe Tx lane 0 differential signals (PET_0_P and PET_0_N) should be connected to the PCIe Rx lane 0 of the host interface through 0.1 mF AC coupling capacitors.		
		PCIe Tx lane 1 differential signals (PET_1_P and PET_1_N) should be connected to the PCIe Rx lane 1 of the host interface through 0.1mF AC coupling capacitors.		

SECTION	CHECK ITEMS	DETAIL	√ Done or Not done	NOTES AND COMMENTS
		PCIe Tx lane 2 differential signals (PET_2_P and PET_2_N) should be connected to the PCIe Rx lane 2 of the host interface through 0.1 mF AC coupling capacitors.		
		PCIe Tx lane 3 differential signals (PET_3_P and PET_3_N) should be connected to the PCIe Rx lane 3 of the host interface through 0.1 mF AC coupling capacitors.		
		PCIe Tx lane 4 differential signals (PET_4_P and PET_4_N) should be connected to the PCIe Rx lane 4 of the host interface through 0.1 mF AC coupling capacitors.		

SECTION	CHECK ITEMS	DETAIL	√ Done or Not done	NOTES AND COMMENTS
		PCIe Tx lane 5 differential signals (PET_5_P and PET_5_N) should be connected to the PCIe Rx lane 5 of the host interface through 01 mF AC coupling capacitors.		
		PCIe Tx lane 6 differential signals (PET_6_P and PET_6_N) should be connected to the PCIe Rx lane 6 of the host interface through 01 mF AC coupling capacitors.		
		PCIe Tx lane 7 differential signals (PET_7_P and PET_7_N) should be connected to the PCIe Rx lane 7 of the host interface through 0.1 mF AC coupling capacitors.		

SECTION	CHECK ITEMS	DETAIL	√ Done or Not done	NOTES AND COMMENTS
	Connect the PCIe receive signals to the PCIe host.	PCIe Rx lane 0 differential signals (PER_0_P and PER_0_N) should be connected to the PCIe Tx lane 0 of the host interface through 0.1 mF AC coupling capacitors.		
		PCIe RX Lane 1 differential signals (PER_1_P and PER_1_N) should be connected to PCIe TX Lane 1 of host interface through 0.1uF AC coupling capacitors.		
		PCIe Rx lane 2 differential signals (PER_2_P and PER_2_N) should be connected to the PCIe Tx lane 2 of the host interface through 0.1 mF AC coupling capacitors.		

SECTION	CHECK ITEMS	DETAIL	√ Done or Not done	NOTES AND COMMENTS
		PCIe Rx lane 3 differential signals (PER_3_P and PER_3_N) should be connected to the PCIe Tx lane 3 of the host interface through 0.1 mF AC coupling capacitors.		
		PCIe Rx lane 4 differential signals (PER_4_P and PER_4_N) should be connected to the PCIe Tx lane 4 of the host interface through 0.1 mF AC coupling capacitors.		
		PCIe Rx lane 5 differential signals (PER_5_P and PER_5_N) should be connected to the PCIe Tx lane 5 of the host interface through 0.1 mF AC coupling capacitors.		

SECTION	CHECK ITEMS	DETAIL	√ Done or Not done	NOTES AND COMMENTS
		PCIe Rx lane 6 differential signals (PER_6_P and PER_6_N) should be connected to the PCIe Tx lane 6 of host interface through 0.1 mF AC coupling capacitors.		
		PCIe Rx lane 7 differential signals (PER_7_P and PER_7_N) should be connected to the PCIe Tx lane 7 of the host interface through 0.1 mF AC coupling capacitors.		
	Connect the PCIe differential clock signals to the PCIe host clock.	PCIe differential clock signals (PE_CLK_P and PE_CLK_N) should be connected to PCIe differential clock of the host interface.		
	Connect the PCIe reset to the host system.	PCIe reset signal (PE_RST_N) should be connected to the PCIe reset signal of the host interface.		

SECTION	CHECK ITEMS	DETAIL	√ Done or Not done	NOTES AND COMMENTS
	Connect the PCIe reset to the host system.	PCIe reset signal (PE_RST_N) should be connected to the PCIe reset signal of the host interface.		
	Connect the PCIe wake signal to the PCIe host.	PCIe wake signal (PE_WAKE_N) should be connected to the PCIe wake signal of the host interface.		
		PCIe wake signal (PE_WAKE_N) should be connected to and external 10 KW pull-up resistor to the 3.3 V dc supply.		
		If not used, leave unconnected.		
	Connect the PCIe compensation resistor.	PCIe compensation signal (PE_RCOMP_N and PE_RCOMP_P) should be connected together through a 1.4 KW 1% tolerance resistor.		

SECTION	CHECK ITEMS	DETAIL	√ Done or Not done	NOTES AND COMMENTS
Serial Flash Interface	Connect the serial Flash interface.	Flash chip enable (FLSH_CE_N) should be connected to chip select of the Flash device.		
		Flash chip enable (FLSH_CE_N) should be connected to an external 10 KW pull-up resistor to the 3.3 V dc supply. 10 KW - 100 KW		
		Flash clock (FLSH_SCK) should be connected to the Flash clock port of the external Flash device. Optional 22 W serial resistor can be added.		
		Flash data input signal (FLSH_SI), an output signal, should be connected to the Flash data input of the external Flash device.		
		Flash data output signal (FLSH_SO), an input signal, should be connected to the Flash data output of the external Flash device.		

SECTION	CHECK ITEMS	DETAIL	√ Done or Not done	NOTES AND COMMENTS
		Add a 3.3 KW pull-up resistor on the Flash's WP_N and HOLD_N pins.		
		Add a 0.1 mF decoupling capacitor close to the SPI Flash chip's power pin.		
	If a Flash is not used.	Leave FLSH_CE_N, FLSH_SCK, FLSH_SI, FLSH_SO unconnected.		
Serial EEPROM Interface	Connect the serial EEPROM interface.	EEPROM chip enable (EE_CS_N) should be connected to the chip select of the EEPROM device.		
		EEPROM chip enable (EE_CS_N) should be connected to an external 10 KW pull-up resistor to the 3.3 V dc supply. 10 KW - 100 KW		

SECTION	CHECK ITEMS	DETAIL	√ Done or Not done	NOTES AND COMMENTS
		EEPROM clock (EE_SK) should be connected to the EEPROM clock port of external the EEPROM device. Optional 22 W serial resistor can be added.		
		EEPROM data input signal (EE_DI), an output signal, should be connected to the EEPROM data input of the external EEPROM device.		
		EEPROM data output signal (EE_DO), an input signal, should be connected to the EEPROM data output of the external EEPROM device.		
		Add a 3.3 KW pull-up resistor on the EEPROM's WP_N and HOLD_N pins.		

SECTION	CHECK ITEMS	DETAIL	√ Done or Not done	NOTES AND COMMENTS
		Add a 0.1 mF decoupling capacitor close to the serial EEPROM chip's power pin.		
		Add a 0.1 mF decoupling capacitor close to the EEPROM's power pin.		
	If EEPROM is not used	Leave EE_CE_N, EE_SCK, EE_SI, EE_SO unconnected.		
SMBus Interface	Connect the SMBus management interface	SMBus bidirection data signal (SMBD) should be connected to the SMBus data signal.		
		SMBus bidirection data signal (SMBD) should be connected to an external 8.2 KW pull-up resistor to the 3.3 V dc supply. For a valid pull-up resistor value range, refer to the Datasheet.		
		SMBus clock signal (SMBCLK) should be connected to the SMBus clock signal on the platform.		

SECTION	CHECK ITEMS	DETAIL	√ Done or Not done	NOTES AND COMMENTS
		SMBus clock signal (SMBCLK) should be connected to an external 8.2 KW pull-up resistor to the+C4 3.3 V dc. For a valid pull-up resistor value range, refer to the Datasheet.		
		SMBus alert signal (SMBALRT_N) should be connected to the SMBus alert signal on the platform. For a valid pull-up resistor value range, refer to the Datasheet.		
		SMBus alert signal (SMBALRT_N) should be connected to an external 8.2 KW pull-up resistor to the 3.3 V dc supply. For a valid pull-up resistor value range, refer to the Datasheet.		

SECTION	CHECK ITEMS	DETAIL	√ Done or Not done	NOTES AND COMMENTS
	If SMBus is not used	SMBus bidirection data signal (SMBD) should be connected to an external 8.2 KW pull-up resistor to the 3.3 V dc supply. For a valid pull-up resistor value range, refer to the Datasheet.		
		SMBus clock signal (SMBCLK) should be connected to an external 8.2 KW pull-up resistor to the 3.3 V dc supply. For a valid pull-up resistor value range, refer to the Datasheet.		
		SMBus alert signal (SMBALRT_N) should be connected to an external 8.2 KW pull-up resistor to the 3.3 V dc supply.		
NC-SI interface	Connect the NC-SI management interface	The NC-SI clock input (NC-SI_CLK_IN) should be connected to a specification-compliant 50 MHz clock generated on the platform (50 ppm).		

SECTION	CHECK ITEMS	DETAIL	√ Done or Not done	NOTES AND COMMENTS
		The NCSI clock input (NCSI_CLK_IN) should be connected to an external 100 W pull-down resistor. For a valid pull-down resistor value range, refer to the Datasheet		.
		The NC-SI receive data output signals (NC-SI_RXD_1 and NC-SI_RXD_0) should be connected to the NC-SI data inputs of the external BMC.		
		The NCSI receive data output signals (NCSI_RXD_1 and NCSI_RXD_0) should be connected to an external 8.2 KW pull-up resistor to the 3. 3 Vdc supply. For a valid pull-up resistor value range, refer to the Datasheet.		

SECTION	CHECK ITEMS	DETAIL	√ Done or Not done	NOTES AND COMMENTS
		The NC-SI carrier sense/receive data valid signal output (NC-SI_CRS_DV) should be connected to the CRS/DV input port on the external BMC.		
		The NC-SI carrier sense/receive data valid signal output (NC-SI_CRS_DV) should be connected to a 100 W pull-down resistor. For a valid pull-down resistor value range, refer to the Datasheet.		
		The NC-SI transmit data input signals (NC-SI_TXD_1 and NC-SI_TXD_0) should be connected to the NC-SI data outputs of the external BMC. For a valid pull-down resistor value range, refer to the Datasheet.		

SECTION	CHECK ITEMS	DETAIL	√ Done or Not done	NOTES AND COMMENTS
		The NCSI transmit data input signals (NCSI_TXD_1 and NCSI_TXD_0) should be connected to external 8.2 KW pull-up resistor to 3.3 V dc supply. For a valid pull-up resistor value range, refer to the Datasheet.		
		The NCSI transmit enable input signal (NCSI_TX_EN) should be connected to an external 100 W pull-down resistor. For a valid pull-down resistor value range, refer to the Datasheet.		
		The NC-SI transmit enable input signal (NC-SI_TX_EN) should be connected to the transmit enable output of the external BMC.		

SECTION	CHECK ITEMS	DETAIL	√ Done or Not done	NOTES AND COMMENTS
	If NC-SI interface is not used	The NC-SI clock input (NC-SI_CLK_IN) should be connected to external 100 W pull-down resistor. For a valid pull-down resistor value range, refer to the Datasheet.		
		The NC-SI receive data output signals (NC-SI_RXD_1 and NC-SI_RXD_0) should be connected to an external 8.2 KW pull-up resistor to the 3.3 V dc supply. For a valid pull-up resistor value range, refer to the Datasheet.		
		The NC-SI carrier sense/receive data valid signal output (NC-SI_CRS_DV) should be connected to a 100 W pull-down resistor. For a valid pull-down resistor value range, refer to the Datasheet.		

SECTION	CHECK ITEMS	DETAIL	√ Done or Not done	NOTES AND COMMENTS
		The NC-SI transmit data input signals (NC-SI_TXD_1 and NC-SI_TXD_0) should be connected to an external 8.2 KW pull-up resistor to the 3.3 V dc supply. For a valid pull-up resistor value range, refer to the Datasheet.		
		The NC-SI transmit enable input signal (NC-SI_TX_EN) should be connected to an external 100 W pull down resistor. For a valid pull-down resistor value range, refer to the Datasheet.D73		
MAUI		Connect a 6.49 KW 1% bias resistor between RBIAS and ground.		
		Connect VSSAF1 to ground.		

SECTION	CHECK ITEMS	DETAIL	√ Done or Not done	NOTES AND COMMENTS
		Each of the MAUI ports can idividually be configured to operate in one of the following modes: KX, BX, KX4, CX4 or XAUI.		
		Based on the chosen interface setup there might be unused differential pairs. These should be left unconnected.		
MAUI Port 0	KX or BX connection.	Port 0 - lane 0 transmit differential signals (TX0_L0_N and TX0_L0_P) should be connected to the receive port of the link partner or to the corresponding connector.		

SECTION	CHECK ITEMS	DETAIL	√ Done or Not done	NOTES AND COMMENTS
		Port 0 - lane 0 receive differential signals (RX0_L0_N and RX0_L0_P) should be connected to the transmit port of the link partner or to the coresponding connector through 0.01 mF AC coupling capacitors. Place the AC coupling capacitors close to the receiver.		
	KX4 connection.	Port 0 - lane 0 transmit differential signals (TX0_L0_N and TX0_L0_P) should be connected to the receive port of the link partner or to the corresponding pins of the backplane connector.		

SECTION	CHECK ITEMS	DETAIL	√ Done or Not done	NOTES AND COMMENTS
		Port 0 - lane 0 receive differential signals (RX0_L0_N and RX0_L0_P) should be connected to the transmit port of the link partner or to the corresponding pins of the backplane connector through 0.01 mF AC coupling capacitors. Place the AC coupling capacitors close to the receiver.		
		Port 0 - lane 1 transmit differential signals (TX0_L1_N and TX0_L1_P) should be connected to the receive port of the link partner or to the corresponding pins of the backplane connector.		

SECTION	CHECK ITEMS	DETAIL	√ Done or Not done	NOTES AND COMMENTS
		Port 0 - lane 1 receive differential signals (RX0_L1_N and RX0_L1_P) should be connected to the transmit port of the link partner or to the corresponding pins of the backplane connector through 0.01 mF AC coupling capacitors. Place the AC coupling capacitors close to the receiver.		
		Port 0 - lane 2 transmit differential signals (TX0_L2_N and TX0_L2_P) should be connected to the receive port of the link partner or to the corresponding pins of the backplane connector.		

SECTION	CHECK ITEMS	DETAIL	√ Done or Not done	NOTES AND COMMENTS
		Port 0 - lane 2 receive differential signals (RX0_L2_N and RX0_L2_P) should be connected to the transmit port of the link partner or to the corresponding pins of the backplane connector through 0.01 mF AC coupling capacitors. Place the AC coupling capacitors close to the receiver.		
		Port 0 - lane 3 transmit differential signals (TX0_L3_N and TX0_L3_P) should be connected to the receive port of the link partner or to the corresponding pins of the backplane connector.		

SECTION	CHECK ITEMS	DETAIL	√ Done or Not done	NOTES AND COMMENTS
		Port 0 - lane 3 receive differential signals (RX0_L3_N and RX0_L3_P) should be connected to the transmit port of the link partner or to the corresponding pins of the backplane connector through 0.01 mF AC coupling capacitors. Place the AC coupling capacitors close to the receiver.		
	CX4 connection.	Port 0 - lane 0 transmit differential signals (TX0_L0_N and TX0_L0_P) should be connected to pin S15 and S16 (respectively) of the CX4 connector.		

SECTION	CHECK ITEMS	DETAIL	√ Done or Not done	NOTES AND COMMENTS
		Port 0 - lane 0 receive differential signals (RX0_L0_P and RX0_L0_N) should be connected to pin S1 and S2 (respectively) of the CX4 connector through 470 pF AC coupling capacitors. Place the AC coupling capacitors close to the receiver.		
		Port 0 - lane 1 transmit differential signals (TX0_L1_N and TX0_L1_P) should be connected to pin S13 and S14 (respectively) of the CX4 connector.		

SECTION	CHECK ITEMS	DETAIL	√ Done or Not done	NOTES AND COMMENTS
		Port 0 - lane 1 receive differential signals (RX0_L1_P and RX0_L1_N) should be connected to pin S3 and S4 (respectively) of the CX4 connector through 470 pF AC coupling capacitors. Place the AC coupling capacitors close to the receiver.		
		Port 0 - lane 2 transmit differential signals (TX0_L2_N and TX0_L2_P) should be connected to pin S11 and S12 (respectively) of the CX4 connector.		

SECTION	CHECK ITEMS	DETAIL	√ Done or Not done	NOTES AND COMMENTS
		Port 0 - lane 2 receive differential signals (RX0_L2_P and RX0_L2_N) should be connected to pin S5 and S6 (respectively) of the CX4 connector through 470 pF AC coupling capacitors. Place the AC coupling capacitors close to the receiver.		
		Port 0 - lane 3 transmit differential signals (TX0_L3_N and TX0_L3_P) should be connected to pin S9 and S10 (respectively) of the CX4 connector.		

SECTION	CHECK ITEMS	DETAIL	√ Done or Not done	NOTES AND COMMENTS
		Port 0 - lane 3 receive differential signals (RX0_L3_P and RX0_L3_N) should be connected to pin S7 and S8 (respectively) of the CX4 connector through 470 pF AC coupling capacitors. Place the AC coupling capacitors close to the receiver.		
	XAUI connection. NOTE: 82598 TX (output) connects to the PHY's RX (input), but some PHY vendors may label the corresponding PHY input as TX (not RX).	Port 0 - lane 0 transmit (output) differential signals (TX0_L0_N and TX0_L0_P) should be connected to the receive (input) port lane 0 of the XAUI PHY.		

SECTION	CHECK ITEMS	DETAIL	√ Done or Not done	NOTES AND COMMENTS
		Port 0 - lane 0 receive (input) differential signals (RX0_L0_N and RX0_L0_P) should be connected to the transmit (output) port lane 0 of the XAUI PHY through 0.01 mF AC coupling capacitors. Place the AC coupling capacitors close to the receiver. Some optical modules like XENPAK, XPAK include these AC coupling capacitors.		
		Port 0 - lane 1 transmit (output) differential signals (TX0_L1_N and TX0_L1_P) should be connected to the receive (input) port lane 1 of the XAUI PHY.		

SECTION	CHECK ITEMS	DETAIL	√ Done or Not done	NOTES AND COMMENTS
		Port 0 - lane 1 receive (input) differential signals (RX0_L1_N and RX0_L1_P) should be connected to the transmit (output) port lane 1 of the XAUI PHY through 0.01 mF AC coupling capacitors. Place the AC coupling capacitors close to the receiver. Some optical modules like XENPAK, XPAK include these AC coupling capacitors.		
		Port 0 - lane 2 transmit (output) differential signals (TX0_L2_N and TX0_L2_P) should be connected to the receive (input) port lane 2 of the XAUI PHY.		

SECTION	CHECK ITEMS	DETAIL	√ Done or Not done	NOTES AND COMMENTS
		Port 0 - lane 2 receive (input) differential signals (RX0_L2_N and RX0_L2_P) should be connected to the transmit (output) port lane 2 of the XAUI PHY through 0.01 mF AC coupling capacitors. Place the AC coupling capacitors close to the receiver. Some optical modules like XENPAK, XPAK include these AC coupling capacitors.		
		Port 0 - lane 3 transmit (output) differential signals (TX0_L3_N and TX0_L3_P) should be connected to the receive (input) port lane 3 of the XAUI PHY.		

SECTION	CHECK ITEMS	DETAIL	√ Done or Not done	NOTES AND COMMENTS
		Port 0 - lane 3 receive (input) differential signals (RX0_L3_N and RX0_L3_P) should be connected to the transmit (output) port lane 3 of the XAUI PHY through 0.01 mF AC coupling capacitors. Place the AC coupling capacitors close to the receiver. Some optical modules like XENPAK, XPAK include these AC coupling capacitors.		

SECTION	CHECK ITEMS	DETAIL	√ Done or Not done	NOTES AND COMMENTS
	Connect the LED signals.	The LED outputs can be configured in many different ways. Make sure to provide a current limiting resistor. It is recommended to provide a place for an EMI filter capacitor also (for example: 470 pF). For more information, refer to the Datasheet and reference schematic.		
		If LEDs are not needed, leave the pins unconnected.		
	Connect MDIO.	If used, connect the MDIO signals (MDC0 and MDIO0) to the MDIO port of the PHY used.		

SECTION	CHECK ITEMS	DETAIL	√ Done or Not done	NOTES AND COMMENTS
		Pull-up the MDIO line to 3.3 V dc via an 8.2 KW resistor For a valid pull-up value range, refer to the Datasheet.		
		Please note that these pins use 3.3 V dc signaling. If necessary use bidirectional level shifters.		
		If MDIO is not used, leave the MDC signal unconnected and then pull up the MDIO signal to 3.3 V dc with an 8.2 KW resistor. For a valid pull-up value range, refer to the Datasheet.		

SECTION	CHECK ITEMS	DETAIL	√ Done or Not done	NOTES AND COMMENTS
	Connect the Software Defined Pins (SDPs).	Use these signals as needed for miscellaneous PHY control signals like reset, signal detect, transmit disable, module detect, and others. Caution should be used when connecting these signals because these pins default as outputs.		
		Please note that these pins use 3.3 V dc signaling. If necessary use level shifters.		
		Please note that SDP 6 and 7 have open drain output buffers.		
		SDPs that are not used should be left unconnected.		

SECTION	CHECK ITEMS	DETAIL	√ Done or Not done	NOTES AND COMMENTS
MAUI Port 1	KX connection.	Port 1 - lane 0 transmit differential signals (TX1_L0_N and TX1_L0_P) should be connected to the receive port of the link partner or to the corresponding connector.		
		Port 1 - lane 0 receive differential signals (RX1_L0_N and RX1_L0_P) should be connected to the transmit port of the link partner or to the corresponding connector through 0.01 mF AC coupling capacitors. Place the AC coupling capacitors close to the receiver.		

SECTION	CHECK ITEMS	DETAIL	√ Done or Not done	NOTES AND COMMENTS
	KX4 connection	Port 1 - lane 0 transmit differential signals (TX1_L0_N and TX1_L0_P) should be connected to the receive port of the link partner or to the corresponding pins of the backplane connector.		
		Port 1 - lane 0 receive differential signals (RX1_L0_N and RX1_L0_P) should be connected to the transmit port of the link partner or to the corresponding pins of the backplane connector through 0.01 mF AC coupling capacitors. Place the AC coupling capacitors close to the receiver.		

SECTION	CHECK ITEMS	DETAIL	√ Done or Not done	NOTES AND COMMENTS
		Port 1 - lane 1 transmit differential signals (TX1_L1_N and TX1_L1_P) should be connected to the receive port of the link partner or to the corresponding pins of the backplane connector.		
		Port 1 - lane 1 receive differential signals (RX1_L1_N and RX1_L1_P) should be connected to the transmit port of the link partner or to the corresponding pins of the backplane connector through 0.01 mF AC coupling capacitors. Place the AC coupling capacitors close to the receiver.		

SECTION	CHECK ITEMS	DETAIL	√ Done or Not done	NOTES AND COMMENTS
		Port 1 - lane 2 transmit differential signals (TX1_L2_N and TX1_L2_P) should be connected to the receive port of the link partner or to the corresponding pins of the backplane connector.		
		Port 1 - lane 2 receive differential signals (RX1_L2_N and RX1_L2_P) should be connected to the transmit port of the link partner or to the corresponding pins of the backplane connector through 0.01 mF AC coupling capacitors. Place the AC coupling capacitors close to the receiver.		

SECTION	CHECK ITEMS	DETAIL	√ Done or Not done	NOTES AND COMMENTS
		Port 1 - lane 3 transmit differential signals (TX1_L3_N and TX1_L3_P) should be connected to the receive port of the link partner or to the corresponding pins of the backplane connector.		
		Port 1 - lane 3 receive differential signals (RX1_L3_N and RX1_L3_P) should be connected to the transmit port of the link partner or to the corresponding pins of the backplane connector through 0.01 mF AC coupling capacitors. Place the AC coupling capacitors close to the receiver.		

SECTION	CHECK ITEMS	DETAIL	√ Done or Not done	NOTES AND COMMENTS
	CX4 connection	Port 1 - lane 0 transmit differential signals (TX1_L0_N and TX1_L0_P) should be connected to pin S15 and S16 (respectively) of the CX4 connector.		
		Port 1 - lane 0 receive differential signals (RX1_L0_P and RX1_L0_N) should be connected to pin S1 and S2 (respectively) of the CX4 connector, through 470 pF AC coupling capacitors. Place the AC coupling capacitors close to the receiver.		
		Port 1 - lane 1 transmit differential signals (TX1_L1_N and TX1_L1_P) should be connected to pin S13 and S14 (respectively) of the CX4 connector.		

SECTION	CHECK ITEMS	DETAIL	√ Done or Not done	NOTES AND COMMENTS
		Port 1 - lane 1 receive diferential signals (RX1_L1_P and RX1_L1_N) should be connected to pin S3 and S4 (respectively) of the CX4 connector through 470 pF AC coupling capacitors. Place the AC coupling capacitors close to the receiver.		
		Port 1 - lane 2 transmit differential signals (TX1_L2_N and TX1_L2_P) should be connected to pin S11 and S12 (respectively) of the CX4 connector.		

SECTION	CHECK ITEMS	DETAIL	√ Done or Not done	NOTES AND COMMENTS
		Port 1 - lane 2 receive differential signals (RX1_L2_P and RX1_L2_N) should be connected to pin S5 and S6 (respectively) of the CX4 connector through 470 pF AC coupling capacitors. Place the AC coupling capacitors close to the receiver.		
		Port 1 - lane 3 transmit differential signals (TX1_L3_N and TX1_L3_P) should be connected to pin S9 and S10 (respectively) of the CX4 connector.		

SECTION	CHECK ITEMS	DETAIL	√ Done or Not done	NOTES AND COMMENTS
		Port 1 - lane 3 receive differential signals (RX1_L3_P and RX1_L3_N) should be connected to pin S7 and S8 (respectively) of the CX4 connector through 470 pF AC coupling capacitors. Place the AC coupling capacitors close to the receiver.		
	XAUI connection. NOTE: 82598 TX (output) connects to the PHY's RX (input), but some PHY vendors may label the corresponding PHY input as TX (not RX).	Port 1 - lane 0 transmit (output) differential signals (TX0_L0_N and TX0_L0_P) should be connected to the receive (input) port lane 0 of the XAUI PHY.		

SECTION	CHECK ITEMS	DETAIL	√ Done or Not done	NOTES AND COMMENTS
		Port 1 - lane 0 receive (input) differential signals (RX0_L0_N and RX0_L0_P) should be connected to the transmit (output) port lane 0 of the XAUI PHY through 0.01 mF AC coupling capacitors. Place the AC coupling capacitors close to the receiver. Some optical modules like XENPAK, XPAK include these AC coupling capacitors.		
		Port 1 - lane 1 transmit (output) differential signals (TX0_L1_N and TX0_L1_P) should be connected to the receive (input) port lane 1 of the XAUI PHY.		

SECTION	CHECK ITEMS	DETAIL	√ Done or Not done	NOTES AND COMMENTS
		Port 1 - lane 1 receive (input) differential signals (RX0_L1_N and RX0_L1_P) should be connected to the transmit (output) port lane 1 of the XAUI PHY through 0.01 mF AC coupling capacitors. Place the AC coupling capacitors close to the receiver. Some optical modules like XENPAK, XPAK include these AC coupling capacitors.		
		Port 1 - lane 2 transmit (output) differential signals (TX0_L2_N and TX0_L2_P) should be connected to the receive (input) port lane 2 of the XAUI PHY.		

SECTION	CHECK ITEMS	DETAIL	√ Done or Not done	NOTES AND COMMENTS
		Port 1 - lane 2 receive (input) differential signals (RX0_L2_N and RX0_L2_P) should be connected to the transmit (output) port lane 2 of the XAUI PHY through 0.01 mF AC coupling capacitors. Place the AC coupling capacitors close to the receiver. Some optical modules like XENPAK, XPAK include these AC coupling capacitors.		
		Port 1 - lane 3 transmit (output) differential signals (TX0_L3_N and TX0_L3_P) should be connected to the receive (input) port lane 3 of the XAUI PHY.		

SECTION	CHECK ITEMS	DETAIL	√ Done or Not done	NOTES AND COMMENTS
		Port 1 - lane 3 receive (input) differential signals (RX0_L3_N and RX0_L3_P) should be connected to the transmit (output) port lane 3 of the XAUI PHY through 0.01 mF AC coupling capacitors. Place the AC coupling capacitors close to the receiver. Some optical modules like XENPAK, XPAK include these AC coupling capacitors.		
	Connect the LED signals.	The LED outputs can be configured in many different ways. Make sure to provide a current limiting resistor. It is also recommended to provide a place for an EMI filter capacitor (for example: 470 pF). For more information, refer to the Datasheet and reference schematic.		

SECTION	CHECK ITEMS	DETAIL	√ Done or Not done	NOTES AND COMMENTS
		If LEDs are not needed, leave the pins unconnected.		
	Connect MDIO.	If used, connect the MDIO signals (MDC1 and MDIO1) to the MDIO port of the PHY used.		
		Pull up the MDIO line to 3.3 V dc via a 8.2 KW resistor. For a valid pull-up value range, refer to the Datasheet.		
		Please note that these pins use 3.3 V dc signaling. If necessary use bidirectional level shifters.		
		If MDIO is not used, leave the MDC signal unconnected and then pull up the MDIO signal to 3.3 V dc with a 8.2 KW resistor. For a valid pull-up value range, refer to the Datasheet.		

SECTION	CHECK ITEMS	DETAIL	√ Done or Not done	NOTES AND COMMENTS
	Connect the SDPs.	Use these signals as needed for miscellaneous PHY control signals like reset, signal detect, transmit disable, module detect, and others. Caution should be used when connecting these signals because these pins default as outputs.		
		Please note that these pins use 3.3 V dc signaling. If necessary use level shifters.		
		Please note that SDP 6 and 7 have open drain output buffers.		
		SDPs that are not used should be left unconnected.		
Clock Source	Choose an appropiate oscillator.	A fixed crystal oscillator is preferred over the programable crystal oscillators becauese of the smaller resulting jitter. For more details, refer to the Datasheet.		

SECTION	CHECK ITEMS	DETAIL	√ Done or Not done	NOTES AND COMMENTS
		Please choose an oscillator with an LVPECL output buffer that meets the AC/DC requirements described in the Datasheet. Oscillators with CML output are not recommended due to the fast rise time. The oscillator's duty cycle should be between 45% and 55% and the frequency tolerance should be lower than ±50 ppm; the rise and fall times have to be between 500 ps and 1 ns.		
		Connect the differential clock input (REFCLKIN_P and REFCLKIN_N) to an external 156.25 MHz differential clock source through 0.1 mF AC coupling capacitors.		

SECTION	CHECK ITEMS	DETAIL	√ Done or Not done	NOTES AND COMMENTS
	Use appropiate termination for the clock lines.	Place the termination between the clock source and the AC coupling capacitors. For more details, refer to the Datasheet and Reference schematics.		
		Connect both the + and - lines of the clock signal to a 127 W pull-up resistor and to the 3.3 V dc supply.		
		Connect both the + and - lines of the clock signal to an 82.5 W pull-down resistor.		
		Use two 27 W serial resistors between the previously mentioned termination and the AC coupling capacitors (one on each line: + and -).		
JTAG interface	Connect JTAG signals to system JTAG chain.	JTAG clock signal (JTCK) should be connected to JTAG clock signal on the platform.		

SECTION	CHECK ITEMS	DETAIL	√ Done or Not done	NOTES AND COMMENTS
		JTAG clock signal (JTCK) should be connected to an external 470 W pull-down resistor. For a valid pull-down value range, refer to the Datasheet.		
		JTAG data input signal (JTDI) should be connected to JTAG data output on the platform.		
		JTAG data input signal (JTDI) should be connected to an external 8.2 KW pull-up resistor to the 3.3 V dc. For a valid pull-up value range, refer to the Datasheet.		
		JTAG data output signal (JTDO) should be connected to JTAG data input signal on the platform.		
		JTAG data output signal (JTDO) should be connected to an external 3.3K ohm pull up resistor to the 3.3 V dc supply.		

SECTION	CHECK ITEMS	DETAIL	√ Done or Not done	NOTES AND COMMENTS
		JTAG mode select signal (JTMS) should be connected to JTAG TMS signal on the platform.		
		JTAG mode select signal (JTMS) should be connected to an external 8.2 KW pull-up resistor to the 3.3 V dc supply. For a valid pull-up value range, refer to the Datasheet.		
		JTAG reset (JRST_N) signal has to be connected to an external 470 W pull-down resistor. For a valid pull-up value range, refer to the Datasheet.		
	If the JTAG interface is not connected to the system, the following pull-up/pull-down resistors should still be in place.	JTAG clock signal (JTCK) should be connected to an external 470 W pull-down resistor. For a valid pull-down value range, refer to the Datasheet.		

SECTION	CHECK ITEMS	DETAIL	√ Done or Not done	NOTES AND COMMENTS
		JTAG data input signal (JTDI) should be connected to an external 8.2 KW pull-up resistor to the 3.3 V dc.		
		JTAG mode select signal (JTMS) should be connected to an external 8.2 KW pull-up resistor to the 3.3 V dc supply.		
		JTAG data output signal (JTDO) should be connected to an external 3.3K ohm pull up resistor to the 3.3 V dc supply.		
		JTAG reset (JRST_N) signal must be connected to an external 470 W pull-down resistor. For a valid pull-down value range, refer to the Datasheet.		

SECTION	CHECK ITEMS	DETAIL	√ Done or Not done	NOTES AND COMMENTS
Power Good and Reset	If internal Power On Reset (POR) is used.	POR_BYPASS signal should be connected to ground through a 470 W pull-down resistor. Formerly RSVDAC3_VSS. This enables the internal POR. An optional test point might be placed to support ICT board tests. For a valid pull-down value range, refer to the Datasheet.		
		LAN_PWR_GOOD should be left unconnected. Formally RSVDB17_NC. An optional test point might be placed to support ICT board tests.		

SECTION	CHECK ITEMS	DETAIL	√ Done or Not done	NOTES AND COMMENTS
	If internal POR is not used. (Recommend using external LAN_POWER_GOOD if the power rails can't meet the start-up timings described in the Datasheet)	POR_BYPASS signal should be pulled up to the 3.3 V dc supply through a 8.2 KW resistor. Formally RSVDAC3_VSS. This disables the internal POR. An optional test point might be placed to support ICT board tests. For a valid pull-up value range, refer to the Datasheet.		
		LAN_PWR_GOOD should be connected to an external power monitoring solution. Formally RSVDB17_NC. An optional test point might be placed to support ICT board tests. Serves as a reset signal. Refer to the Datasheet for more details.		

SECTION	CHECK ITEMS	DETAIL	√ Done or Not done	NOTES AND COMMENTS
Misc Signals	Connect the main power OK signal.	Main power OK signal (MAIN_PWR_OK) should be connected externally to a signal indicating that the main power is present for the 82598. Refer to the Datasheet.		
	Connect the auxiliary power indicator.	When present, the auxiliary power indicator signal (AUX_PWR) should be connected to 3.3 V dc AUX through an external 3.3 KW pull-up resistor if AUX power is available. Refer to the Datasheet.		
		When not present, the auxiliary power indicator signal (AUX_PWR) should be connected to ground through an external 100 W pull-down resistor if AUX power is NOT available. Refer to the Datasheet.		

SECTION	CHECK ITEMS	DETAIL	√ Done or Not done	NOTES AND COMMENTS
	Connect LAN disable signals.	LAN disable port 0 signal (LAN0_DIS_N) should be connected to an external I/O dedicated to this function.*		
		LAN disable port 1signal (LAN1_DIS_N) should be connected to an external I/O dedicated to this function.* *NOTE: If dynamic disable is not used, pull-up or pull-down resistors can be used to statically enable or disable the LAN ports. For a valid pull-up/pull-down value range, refer to the Datasheet.		
	Connect the DEV_PWRDN_N signal.	Device power down output should be connected to the power supply circuit shut down/standby input. Optional. If not used, should be left unconnected.		

SECTION	CHECK ITEMS	DETAIL	√ Done or Not done	NOTES AND COMMENTS
	Connect the PHY power-down signals.	PHY power-down signal (PHY0_PWRDN_N) should be connected to power-down input of the external PHY device. Optional. If not used, should be left unconnected.		
		PHY power-down signal (PHY1_PWRDN_N) should be connected to power-down input of the external PHY device. Optional. If not used, should be left unconnected.		

SECTION	CHECK ITEMS	DETAIL	√ Done or Not done	NOTES AND COMMENTS
Reserved Signals	Reserved NC signals.	Reserved signals (RSVDD3_NC, RSVDG1_NC, RSVDAC13_NC, RSVDAC14_NC, RSVDAB3_NC, RSVDAA3_NC, RSVDY3_NC, RSVDW3_NC, RSVDV4_NC, RSVDU4_NC, RSVDG1_NC, RSVDAD24_NC, RSVDAE25_NC, RSVDF20_NC, RSVDD20_NC, RSVDT28_NC, RSVDT29_NC, RSVDA9_NC, RSVDB11_NC, RSVDA10_NC, RSVDB10_NC, RSVDD1_NC, RSVDA3_NC, RSVDA4_NC, RSVDB4_NC, RSVDB5_NC, RSVDN4_NC, RSVDM4_NC, RSVDL4_NC, RSVDK2_NC, RSVDK3_NC,		

SECTION	CHECK ITEMS	DETAIL	√ Done or Not done	NOTES AND COMMENTS
	Connect reserved 1.2 V dc pins.	Reserved signals (RSVDY10_1P2 and RSVDY11_1P2) should be connected or pulled up to the 1.2 V dc supply on the board.		
	Connect reserved VSS pins.	Reserved signals (RSVDJ1_VSS and RSVDE1_VSS) should be connected to ground through 470 W pull-down resistors.		
No Connect Signals	No connect signals.	No_Connect signals (NCJ19, NCJ20, NCK11, NCL11, NCN28, NCP28, NCP29, NCR17, NCT17, NCU28, NCU29, NCV11, NCW11, NCV28, NCT4, NCR4, NCP4, NCN3, NCM3, NCL3 and NCK1) should NOT be connected on the board.		
Power Supply Connections	Connect the 3.3 V dc supply.	3.3 V dc voltage supply signals (VCC3P3) should be connected to the 3.3 V dc supply voltage.		

SECTION	CHECK ITEMS	DETAIL	√ Done or Not done	NOTES AND COMMENTS
		3.3 V dc voltage supply signals (VCC3P3) should be connected to decoupling capacitors as specified in the Datasheet.		
	High speed decoupling and bulk capacitors for the 3.3 V dc supply.	The minimum acceptable decoupling by power supply is as follows (including decoupling only for the 82598):		
		VCC3P3 decoupling 22 mF bulk 5 x 0.1 mF high speed		
	Connect the 1.8 V dc supply.	1.8 V dc voltage supply signals (VCC1P8) should be connected to the 1.8 V dc supply voltage.		
		1.8 V dc voltage supply signals (VCC1P8) should be connected to decoupling capacitors as specified in the Datasheet.		
	High speed decoupling and bulk capacitors for the 1.8 V dc supply.	The minimum acceptable decoupling by power supply is as follows (including decoupling only for the 82598):		

SECTION	CHECK ITEMS	DETAIL	√ Done or Not done	NOTES AND COMMENTS
		VCC1P8 decoupling 66 mF bulk 8 x 0.1 mF high speed		
	Connect the 1.2 V dc supply.	1.2 V dc voltage supply signals (VCC1P2) should be connected to the 1.2 V dc supply voltage.		
		1.2 V dc voltage supply signals (VCC1P2) should be connected to decoupling capacitors as specified in the Datasheet.		
	High speed decoupling and bulk capacitors for the 1.2 V dc supply.	The minimum acceptable decoupling by power supply is as follows (including decoupling only for the 82598):		
		VCC1P2 decoupling 160 mF bulk 40 - 0.1 mF high speed 6 - 1 nF high speed		
	Power sequencing.	Make sure the design follows the power sequencing requirements detailed in the Datasheet.		

SECTION	CHECK ITEMS	DETAIL	√ Done or Not done	NOTES AND COMMENTS
	Connect ground signals.	Ground signals (VSS) should be connected to the ground of the board. For the signal list, see the Datasheet.		

Layout and Placement Checklist

SECTION	CHECK ITEMS	DETAIL	√ Done or Not done	NOTES AND COMMENTS
General	Have up to date documentation and specification updates.	Documents are subject to frequent change. Make sure to download the latest collateral release.		
	Observe special instructions for some of the interfaces that need special attention.			
	Choose the board stack up carefully.	Take in consideration that most of the high speed interfaces are preferred to be routed on stripline rather than microstrip.		
		Due to high signal density, use an 8-layer board at a minimum.		
	Route the high speed interfaces before routing the digital traces.	Layout of differential traces is critical.		
		Routing the PCI Express* (PCIe*) and KX/KX4/CX4/XAUI differential traces should be routed before the remaining digital interfaces.		
		Refer to the Datasheet for detailed routing requirements.		
Component placement	Place the 82598 at least one inch from the edge of the board.	If the 82598 is closer to the board edge, the strongest fields do not have path to ground and might cause EMI problems.		

SECTION	CHECK ITEMS	DETAIL	√ Done or Not done	NOTES AND COMMENTS
	MAUI bias resistor: RBIAS.	Place the RBIAS bias resistor less than one inch from the 82598.		
	PCIe bias resistor: PE_RCOM	Place the PE_RCOMP bias resistor less than one inch from the 82598.		
	EEPROM and Flash.	Placement of the EEPROM and Flash devices is not critical but they should be kept as close as possible to the 82598.		
		The decoupling capacitors for these devices should be placed close to the power pin.		
Clock Source	Oscillator placement.	Place the oscillator as close to the 82598 as possible.		
		Use appropriate decoupling for the oscillator and place the capacitor close to the power pins.		
		Place the clock termination (two 127 W, two 82.5 W, and two 27 W) and AC coupling as close to the 82598 as possible (<250mil).		
	Reference clock routing	Route the clock signals as a 100 W differential pair with the shortest possible length.		
		Keep the clock traces at least 15 mils away from other signals. This includes spacing to other digital traces, I/O ports, or any other differential pairs.		

SECTION	CHECK ITEMS	DETAIL	√ Done or Not done	NOTES AND COMMENTS
		Also keep clock sources away from board edge		
XAUI/KX/ KX4/CX4	Use small footprint AC coupling capacitors.	Recommended package size is 0402 or smaller		
		Place AC coupling caps close to the receiver (within 1 inch)		
	Design traces for 100 W differential impedance (± 10%)	For long distances, thick traces are preferred over wide traces. Modify board stack up if necessary to avoid highly resistive traces.		
	Reference planes	Use a quiet reference plane, preferably ground. If the differential traces are placed between a power and ground plane, use an offset stripline structure (H, 3H), keeping the pairs closer to the ground plane. For more information, refer to the Datasheet.		
		When differential signals transition from one board layer to another, place ground vias within 40 mils of the signal vias.		
		Differential traces should not cross plane splits. If this is not possible, AC		

SECTION	CHECK ITEMS	DETAIL	√ Done or Not done	NOTES AND COMMENTS
		If the differential signals transition from a ground referenced layer to a power referenced layer, place a decoupling capacitor on the power and ground within 40 mils of the signal vias.		
		Differential traces should be kept away from plane splits, voids, or the reference plane edge by six times the dielectric height.		
	Possible routing topologies are the microstrip or stripline.	Preferred topology is stripline.		
	Long traces from the 82598 to the link partner are allowed to be up to 50 cm on FR4 material, but avoid highly resistive traces.	As much as possible, traces should be routed diagonally to the FR4 weave to maintain consistent impedance. Take into consideration the entire channel length. That includes the backplane and the traces on the link partner side.		
		Avoid broadside coupling to traces on other layers. The broadside effect significantly increases the insertion loss and reduces signal quality.		

SECTION	CHECK ITEMS	DETAIL	√ Done or Not done	NOTES AND COMMENTS
	Do not make 90° bends	Bevel corners with turns based on 45° angles.		
		Radiused bends can also be used.		
	Symmetry	The traces within a differential pair have to be symmetric.		
		Adjacent ground vias must be		
		Try to match the pairs at pads, vias and turns. Establish routing rules carefully. Asymmetry contributes to impedance mismatch.		
	Differential trace grouping	Tx and Rx differential traces should be kept separate.		
	Keep the differential pairs away from each other.	In case of microstrip routing the minimum distance between the differential pairs is seven times the dielectric height.		
		If using stripline routing, the minimum distance between the differential pairs is six times the dielectric height.		
	Keep the break-out area within 200 mils.	Use this area to get the signals out from under the BGA package.		

SECTION	CHECK ITEMS	DETAIL	√ Done or Not done	NOTES AND COMMENTS
	Do not guard the differential traces with adjacent ground fill or ground traces.	Guarding ground traces or copper areas around the differential pairs should not be used. The differential pair should be kept away from ground fills or ground traces by at least the minimum pair-to-pair distance (six times the dielectric height).		
	Vias	Use smallest possible vias on the board.		
		Use ground Vias adjacent to any signal via.		
		Remove via pads on inner layers with no connections.		
		Diameter of anti-pad/signal keep out must be at least 20 mils larger than the pad diameter.		
		There should be no copper separating the signal vias on any routing layer. When differential signals cross metal planes, use appropriate keepouts to prevent separation.		
		Add anti-pad diameter requirement to the via to ground and power clearance of at least 10 mils.		

SECTION	CHECK ITEMS	DETAIL	√ Done or Not done	NOTES AND COMMENTS
		Minimize through holes (vias): If using vias, the maximum plated through hole budget from chip-to-chip is six per trace. This can be a combination of 10 mil finished hole size vias and through holes for connector pins.		
PCIe Interface	For the PCIe interface, place AC coupling capacitors close to the transmitters.	The AC coupling is always on the transmit lines on the PCIe interface		
		Reduces oscillation and ripple in the power supply.		
	Design traces for 100 W differential impedance (microstrip ± 20%; stripline ± 10%).	For long distances, thick traces are preferred over wide traces. Modify board stack up if necessary to avoid highly resistive traces.		
	Route traces on appropriate layers always referenced to a quiet power plane.	Run pairs on different layers as needed to improve routing. Use layers adjacent to ground layers. There must be no splits in the reference planes.		
		When differential signals transition from one board layer to another, place ground vias within 40 mils of the signal vias.		

SECTION	CHECK ITEMS	DETAIL	√ Done or Not done	NOTES AND COMMENTS
		If the differential signals transition from a ground referenced layer to a power referenced layer, place a decoupling capacitor on the power and ground within 40 mils of the signal vias.		
	Long traces are allowed up to 14 inches, but avoid highly resistive traces. Maximum distance from the 82598 to the PCIe chipset is about 20 inches.	Traces should be routed diagonally to the FR4 weave to maintain consistent impedance.		
		If one ounce copper is used, minimum trace spacing within each differential pair must be >= 8 mils.		
		Avoid broadside coupling to traces on other layers. The broadside effect significantly increases the insertion loss and reduces signal quality.		
		Make sure digital signals on adjacent layers cross at 90° angles.		
	Do not make 90° bends.	Bevel corners with turns based on 45° angles.		
	Make traces symmetrical.			

SECTION	CHECK ITEMS	DETAIL	√ Done or Not done	NOTES AND COMMENTS
	Check the skew within a pair and pair-to-pair as well.	The trace lengths within a differential pair have to be matched within 5 mils in each segment.		
		The length of the different PCIe lanes have to be matched within one inch .		
		Try to match the pairs at pads, vias and turns. Establish routing rules carefully. Asymmetry contributes to impedance mismatch.		
	Keep traces relatively close together within differential pairs (6 to 10 mils edge-to-edge within a differential pair).	If spacing is less than 6 mils, it is almost impossible to achieve >90 W differential impedance.		
		Minimizes signal skew and reduces common mode conversion.		
	Keep PCIe differential pairs approximately 15 mils or more from other PCIe differential pairs.	The minimum separation is 15 mils for designs with a dielectric thickness of 2.8 mils, nominal. Minimizes crosstalk and noise injection. This includes spacing to other digital traces, I/O ports, board edge, transformers and differential pairs.		
		If using a larger dielectric thickness, keep adjacent traces away by at least six times the dielectric thickness. For example, 4.5 mil thick FR4; spacing >= 27 mils.		

SECTION	CHECK ITEMS	DETAIL	√ Done or Not done	NOTES AND COMMENTS
	Keep traces greater than 0.1 inch from the board edge.	Reduces EMI.		
	Avoid unused pads and stubs along the traces.	Use zero W resistors sparingly if needed.		
	Minimize through holes (vias)	If using vias, the maximum plated through hole budget from chip-to-chip is six per trace. This can be a combination of 10 mil finished hole size vias and through holes for connector pins.		
NC-SI	Make sure to follow the delay recommendations detailed in the Datasheet.	This helps the design to meet the necessary NC-SI timing specifications.		
Power Supply and Signal Ground	Use planes to deliver power.	Planes have lower inductance and lower resistance than traces.		
		When power planes have to be stitched together use an array of vias. The via size should also be bigger than the one used for high speed signals.		
	Use decoupling and bulk capacitors generously.	Use at least the indicated amount of decoupling on each power rail.		
		Place bulk capacitors close to Ethernet device. If power is distributed on traces, bulk capacitors should be used at both ends.		

SECTION	CHECK ITEMS	DETAIL	√ Done or Not done	NOTES AND COMMENTS
		Place most of the high speed bypass capacitors on the back side of the board , right under the BGA package.		
		Connect the each of the bypass capacitors with traces as wide as possible.		
		For connecting bypass capacitors to the power planes use bigger via size than the via used for high speed signals.		
LEDs	Keep LED traces away from high speed digital traces running in parallel.	Since LEDs are usually placed so they are easily viewable, these traces can carry noise out to the edge of the board, increasing EMI.		
	If using decoupling capacitors on LED lines, place them carefully.	Capacitors on LED lines should be placed near the LEDs.		