Intel® 82580 Quad/Dual GbE Controller Checklists

LAN Access Division

Project Name	
Fab Revision	
Date	
Designer	
Intel Contact	
Reviewer	

Revision	Date	Notes
0.5	3/1/2009	Initial Release
1.0	6/29/2009	Add Guidance For RSVD_TP_* and LED Pins. Clarify Trace Length.
1.1	7/30/2009	Correct inversion in LED Guidance.
1.2	9/3/2009	Add Guidance For RSVD_JRST_3P3
1.3	9/11/2009	Improve 1000BASE-KX layout details.
1.4	11/30/2009	Added Ball numbers. Added range information on component values.
2.0	1/22/2010	SE_RSET value changed to 2.37k, Update SERDES layout to include all interfaces.
2.1	2/26/2010	Added PCIe guidelines and No connect information on SERDES interface.
2.2	4/22/2010	Add information about LAN Disable requirement for series resister. Made LAN_PWR_GOOD and MAIN_PWR_OK consistant with reference schmatic.
2.3	5/7/2010	Tighten ranage of resister values for LAN Disable and AUX Power pins Add information for JTDO.
2.4	8/18/2010	Major improvement of Layout Checklist Guidelines. Fixed Typographic issues.
2.5	10/5/2010	Updated some pictures for clarity in the layout guidelines. Fixed DEV_OFF_N

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Schematic Checklist

SECTION	CHECK ITEMS	Detail	√ Done or Not Done	NOTES
General	Obtain the most recent documentation and specification updates.	Documents are subject to frequent change.		
SKU	The 82580 has a Dual Port SKU and a Quad Port SKU. The SKU's are pin compatable. On the Dual Port SKU all balls relating to ports 0 and 1 can be used while ports 2 and 3 can be left unconnected.			
PCIe Interface	Connect PCIe interface pins to corresponding pins on an upstream PCIe device. The 82580 supports x4, x2, and x1 configurations at 2.5 GT/s and 5GT/s.			
	Place AC coupling capacitors (0.1 µF) should be near the PCIe transmitter.	Size 0402, X7R is recommended.		
	Connect PE_CLK_n (A15) and PE_CLK_p (A16) to the 100 MHz PCIe system clock.	This is required by the PCIe interface.		
	Connect PE_RST_N (B1) to PLTRST# on an upstream PCIe device.	This signal is defined by the PCIe specification and is required for proper device initialization.		
	Connect PE_WAKE_N (D16) to PE_WAKE# on an upstream PCIe device.	This is required to enable Wake on LAN functionality required for advanced power management.		

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SECTION	CHECK ITEMS	Detail	√ Done or Not Done	NOTES
Support Pins	Connect DEV_OFF_N (C4), to an IO pin that retains it value during PCIe reset. or Pull-up DEV_OFF_N (C4) to with a 3.3 KΩ resistor to 3.3 V.	Connect to a super I/O pin that retains its value during PCIe reset, is driven from aux power and defaults to one on power-up. If device off functionality is not needed, then DEV_OFF_N should be connected with an external pull-up resistor. Ensure pull-ups are connected to aux power. The exact 3.3k value of the pull-up resister is not critical. 100 Ohms to 10k is ok.		
	Connect LAN0_DIS_N(F14), LAN1_DIS_N(E14), LAN2_DIS_N(D14), and LAN3_DIS_N(C14) through a 3.3 KΩ series resister to an IO pin that retains it value during PCIe reset. or Pull-up with LAN0_DIS_N(F14), LAN1_DIS_N(E14), LAN2_DIS_N(D14), and LAN3_DIS_N(C14) with 3.3 KΩ resistors to 3.3 V.	Connect to a super I/O pin that retains its value during PCIe reset, is driven from aux power and defaults to one on power-up. The LAN disable pin must be driven through a series resister because it becomes an output after intialization is complete. If there is no series resister there will be contention on this signal. In the case of a hot PCIe reset there is a 40 ns setup time on this signal between when it stop driving and when it samples. If lan disable functionality is not needed, then the LANn_DIS_N ports should be connected with an external pull-up resistor. Ensure pull-ups are connected to aux power. The 3.3 KΩ must be placed near the 82580 less than a 1 inch trace to ensure the 40ns setup can be met. (less than ~4 pF of trace.) If the resister must be further from the device use a value smalller than 3.3k. The exact 3.3kΩ value of the pull-up resister is not critical. 1kΩ to 3.3kΩ is ok.		

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	Connect MAIN_PWR_OK(B2) to the Main 3.3 V power source with a 3.3 KΩ resistor.	When MAIN_PWR_OK is high, the 82580 is allowed to enter any power state and can consume it's max power. When MAIN_PWR_OK is low, the 82580 is not allowed to enter it's fully powered state and will stay in a low power mode used for managbility and Wake-on-LAN. The exact 3.3k value of the pull-up resister is not critical. 0Ω to 10kΩ is ok.		
	Pull-up LAN_PWR_GOOD(D4) to with a 3.3 KΩ resistor to the 3.3 V.	Add Guidance For RSVD_JRST_3P3		
	Connect PE_TRIM1(A2) to PE_TRIM2(A1) with a 1.5kΩ 1% resister.	This is required to trim the PCIe interface. The exact 1.5kΩ 1% value is critical to the function of the device.		

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	Pull-down SE_RSET(K13), with a 2.37 KΩ 1% resistor.	This is required to trim the SerDes interface. The exact 2.37kΩ 1% value is critical to the function of the device. An incorrect value will impact the TX return loss on the SERDES SET* interface.		
	Pull-down GE_REXT3K(T2), with a 3.01 KΩ 1% resistor.	This is required to trim the 1000BASE-T MDI interface. The exact 3.01kΩ 1% value is critical to the function of the device. This pin should be connected even when the 1000BASE-T interface is not used.		
	Pull-up AUX_PWR(D15), with a 3.3 KΩ resistor if the power supplies are derived from always on auxiliary power rails. Pull down AUX_PWR(D15) if the part only has main power available. If this is an Add-in card design where AUX_PWR may or may not be available AUX_PWR should be driven through a 3.3k series resister.	This pin impacts if the 82580 advertises D3 cold wakeup support on the PCIe bus. Ensure pull-ups are connected to auxiliary power. The AUX_PWR pin must be driven through a series resister because it becomes an output after intialization is complete. If there is no series resister there will be contention on this signal. In the case of a hot PCIe reset there is a 40 ns setup time on this signal between when it stop driving and when it samples. The 3.3 KΩ must be placed near the 82580 with less than a 1 inch trace to ensure the 40ns setup can be met. (less than ~ 4 pF of trace.) If the resister must be further from the device use a value smalller than 3.3kΩ. The exact 3.3kΩ value of the pull-up resister is not critical. 1kΩ to 3.3kΩ is ok.		
	RSVD_TP_5(C13), RSVD_TP_6(D12), RSVD_TP_7(G14), and RSVD_TP_8(G15) can be left unconnected or can be pulled up with a 3.3kΩ resister.	These are testpoints used to put the device into a test mode. The exact 3.3kΩ value of the pull-up resister is not critical. 100 Ohms or to 10kΩ is ok.		

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	Pull-down RSVD_TE_VSS (C12) with a 3.3 KΩ resistor.	This is required to prevent the device from going into test mode during normal operation. The exact 3.3kΩ value of the pull-up resister is not critical. 100 Ohms to 10kΩ is ok.		
Clock Source (Oscillator Option)	Connect 3.3V, 25.000MHz ± 50ppm oscillator to XTAL_CLK_I (P1).	The oscillator needs to maintain 50 ppm under all applicable temperature and voltage conditions. Avoid PLL clock buffers. Clock buffers introduce additional jitter. Broadband peak-to-peak jitter must be less than 200 ps. If the packet time stamping features of the I350 are used as a critical element of a precision time syncronization system using a protocol like IEEE 1588, consider using a temperture controled timing device with 1 ppm or less. The XTAL_CLK_I (P1) signal is the basis for the system clock associated with each port.		
	Use a local 0.1 µF decoupling capacitor on the oscillator power supply.	The exact 0.1 µF value is not critical.		

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Clock Source (Crystal Option)	Use a 25 MHz 30 ppm accuracy @ 25 °C crystal. Avoid components that introduce jitter.	Parallel resonant crystals are required. The calibration load should be 18 pF. Specify Equivalent Series Resistance (ESR) to be 50Ω or less. If the packet time stamping features of the 82580 are used as a critical element of a precision time syncronization system using a protocol like IEEE 1588, some applications may require using a temperture controled timing device with less than 1 ppm. The XTAL_CLK_I (P1) signal is the basis for the system clock associated with each port.		
	Place a 10 pF series capacitor on the XTAL_CLK_O (P2).	This is to attenuate the signal from the 82580 to prevent overdriving the crystal.		
	Connect two load capacitors to crystal; one on XTAL_CLK_I (P1) and one on XTAL_CLK_O (P2). Use 27 pF capacitors as a starting point, but be prepared to change the value based on testing.	Capacitance affects accuracy of the frequency. The load capacitors must be matched to crystal specifications and the estimated trace capacitance. Use capacitors with low ESR (types C0G or NPO, for example). Refer to the design considerations section of the datasheet and the Intel Ethernet Controllers Timing Device Selection Guide for more information.		

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Flash	Use 0.1 µF decoupling capacitor on the power supplies for the flash device.	The exact 0.1 µF value is not critical. 1 µF to 0.01 µF is ok.		
	The Flash must be powered from auxiliary power.	The Flash could be read when the system is powered on even before main power is available.		
	Check connections to FLSH_CS_N(C16), FLSH_SK(B16), FLSH_SI(B15), FLSH_SO(C15).	Pins on 82580 are connected to same named pin on the flash device. (FLSH_SI(B15) connects to SI(5) on the Flash device. FLSH_SO(C15) connects to SO(2) on the Flash Device.)		
	If a Flash is not used add a 3.3 KΩ pull-up to FLSH_SO(C15).	In order to use iSCSI Boot and PXE without a flash device, these features must be integrated into the BIOS.		

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SECTION	**CHECK ITEMS**	**Detail**	**√ Done or Not Done**	**NOTES**
EEPROM	Use 0.1 µF decoupling capacitor on the power supplies for the EEPROM device.	The exact 0.1 µF value is not critical. 1 µF to 0.01 µF is ok.		
	The EEPROM must be powered from auxiliary power.	The EEPROM is read when the system is powered even before main power is available.		
	Check connections to EE_CS_N(F16), EE_SK(E16), EE_DI(E15), EE_DO(F15).	Pins on 82580 are connected to same named pin on the NVM. (EE_SI(E15) connects to SI(5) on the EEPROM. EE_SO(E16) connects to SO(2) on the EEPROM.)		
	An EEPROM is required for a fully compatable PCIe interface.	Configurations without an EEPROM always require fully custom software. In addition, configurations without an EEPROM cannot support any features which require configuration before software initialization including PXE/iSCSI Boot, managability and Wake-On-LAN functionality.		

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SECTION	**CHECK ITEMS**	**Detail**	**√ Done or Not Done**	**NOTES**
SMBus	For best performance, each 82580 should have it's own dedicated SMBus link to the SMBus master device.	The 82580 allows for multiple devices but the SMBus has a very limited throughput. Using multiple devices further limits the throughput.		
	If SMBus is not used, connect pull-up resistors to SMB_CLK(E5), SMB_DAT(G3), and SMB_ALRT_N(G4).	10 KΩ pull-ups are reasonable values. Ensure pull-ups are connected to auxiliary power. This prevents noise on these pins from causing problems with device operation. The exact value of the pullup may need to be need to adjusted to deal with other specific platform requirements.		
	If SMBus is used, there should be pull-up resistors on SMB_DAT(G3), SMB_ALRT_N(G4) and SMB_CLK(E5) somewhere on the board.	SMBus signals are open-drain. Ensure pull-ups are connected to auxiliary power.		

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NC-SI	Use a 10 KΩ pull-up resistors on the NC_SI_TXD0 (J3), NC_SI_TXD1 (J4), NC_SI_RXD0(H4), and NC_SI_RXD1(J1) interfaces.			
	Use a 10 KΩ pull-down resistors on the NC_SI_TX_EN(J2), and NC_SI_CRS_DV(H3) interfaces.	Refer to the design considerations section of the datasheet for more details.		
	Use a 33 Ω series resister on the NC_SI_CLK_IN(H1) interface near the clock source.	This improves signal integrity by preventing reflections. The value may need to be tuned for a specific design.		
	Use a 22 Ω series back-termination resistor near the BMC NC_SI_TXD0(J3) and NC_SI_TXD1(J4) interface.	This improves reflections on the trace. The value may need to be tuned for a specific design.		
	If the NC-SI interface is not used tie NC_SI_CLK_IN(H1), NC_SI_CRS_DV(H3), and NC_SI_TX_EN(J2) each to ground with a 10 KΩ resistor.	This is required so that noise on these pins does not cause problems with device operation.		
	If the NC-SI interface is not used tie NC_SI_TXD0, NC_SI_TXD1, NC_SI_RXD0, and NC_SI_RXD1 each to 3.3 V dc with a 10 KΩ resistor.	This is required so that noise on these pins does not cause problems with device operation.		

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SECTION	**CHECK ITEMS**	**Detail**	**√ Done or Not Done**	**NOTES**
10Base-T 100Base-TX 1000Base-T Traces	If any of the MDI* pins are not used they can be left disconnected.			
	The System Side Center tap should not be connected to a power supply.	The 82580's output buffers are internally biased.		
	Ensure there are no termination resistors in the path between the 82580 and the magnetic module.	The 82580 has an internal termination network.		

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SECTION	**CHECK ITEMS**	**Detail**	**√ Done or Not Done**	**NOTES**
10Base-T 100Base-TX 1000Base-T Interface Magnetics Module (Only for Discrete Magnetics with separate RJ-45 Connector)	Bob Smith termination: use 4 x 75 Ω resistors connected to each cable-side center tap.	Terminate pair-to-pair common mode impedance of the CAT5 cable.		
	Bob Smith termination: use an EFT capacitor attached to the chassis ground. Suggested values are 1500 pF/2 KV or 1000 pF/3 KV.	These capacitors provide high voltage isolation.		
	Use 0.1 µF bypass capacitors on system Side Center Tap.	Capacitors with low ESR should be used. The exact value of 0.1 µF is not critical. 0.1 µF to 1000 pF is ok.		
	The System Side Center tap should not be connected to a power supply.	The 82580's output buffers are internally biased.		
	Ensure there are no termination resistors in the path between the 82580 and the magnetics.	The 82580 has an internal termination network.		

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10Base-T 100Base-TX 1000Base-T Interface Chassis Ground	Provide a separate chassis ground to connect the shroud of the RJ-45 connector and to terminate the line side of the magnetic module.	This design improves EMI behavior.		
	Place pads for approximately 4-6 stitching capacitors to bridge the gap from chassis ground to signal ground.	Typical values range from 0.1µF to 4.8µF. The correct value should be determined experimentally to improve EMI. Past experiments have shown they are not required in some designs.		
1000Base-KX Backplane Interface	Connect the respective SER and SET signals to the link partner using 4.7 nF 0402 capacitors series capacitors near the recievers.	The specification for IEEE 1000BASE-KX states that the capacitors shall be less than 4.7 nF.		
	If any SET* and SER* pins are not used they can be left disconnected.			
1000Base-BX Backplane Interface	Connect the respective SER and SET signals to the link partner using 4.7 nF 0402 capacitors series capacitors near the recievers.	The specification for PICMG 1000BASE-BX states that the capacitors shall be less than 10 nF.		
	If any SET* and SER* pins are not used they can be left disconnected.			

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1000Base-SR, 1000Base-LR, or SFP Interface	If any SET*, SER*, SIG_DET*, SFP, and SDP* pins are not used they can be left disconnected.			
	Connect the SER and SET signals to the optical module.			
	Connect the SIG_DET_*_N Signal to the SIG_DET or LOS signal on the optical transciever. Use an 8.2k pull-up resister.	The ILOS bit in the EEPROM controls the polarity of this signal.		
	Connect SDP_*_0 to MOD_ABS on a removeable SFP optical module. Use an 8.2k pullup resister.			
	Connect SDP_*_1 to TX_DISABLE on an optical module.			
	Connect SDP_*_2 to TX_FAULT on an optical module.			
	Connect SDP_*_3 to shutdown the power on the optical module.	This can be used in to save power if the port is not needed when the driver is not loaded. The default state can be controlled from the EEPROM.		
	Connect SFP_*_I2C_CLK and SFP_*_I2C_DATA signals to the physical interface device if applicable.			

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SGMII Interface	When using SGMII, standard Intel software is setup to work with the Marvell 88E1111. Custom software is required for operation with other SGMII devices.			
	Connect SFP_*_I2C_CLK and SFP_*_I2C_DATA to the SGMII device.			

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External Power supply	Derive all three power supplies from auxiliary power supplies.	Auxiliary power is necessary to support wake up and managability during power down states.		
	The TXVTERM and Analog power supplies should be seperated and filtered with a ferrite bead. The refernce design shows an example of how to do this. The reference design example shows a 330 Ohm TDK MPZ2012S331AT or a Murata BLM21PG331SN1 Ferrite Bead in parellel with a 0.39 Ohm resister on each isolated supply.	Noise from digital supplies and internal oscilators can impact the performance of analog circuits. The exact example shown in the schmatic has been sucessful. However, the exact component values are not critical could change by 40%.		
	All voltages should ramp to within their control bands in 100 ms or less. In addition the 1.8V dc must ramp in 80 ms or less. Voltages must ramp in sequence (3.3 V should always be greater that 1.8 V. The 1.8V supply should always be greater than the 1.0 V supply). The voltage rise must be monotonic. The minimum rise time on the 3.3 V dc power is 1 ms.	The 82580 has a power on reset circuit that requires a 1-100 ms ramp time. The rise must be montonic to so the power on reset triggers only once. The sequence is required protect the ESD diodes connected to the power supplies from being forward biased		
LED Circuits	The LED's Use 3.3V dc The Default Behaviours are: LED0->Link Up is Low, Link Down is High. Connect LED0 to Cathode of Green Link/Activity LED. LED1->Normally High, Blinks Low for Filtered Activity. Connect LED1 to Anode of Green Link/Activity LED LED2->If Linked at 100BASE-TX then low. Connect LED2 to Cathode of Green Speed LED and the anode of the orange speed LED. LED3->If Linked at 1000BASE-T then low. Connect LED3 to Cathode of Orange Speed LED and the anode of the green speed LED.	For externally powered LED's use AUX power. Consider adding one or two filtering capacitors per LED for extremely noisy situations. A suggested starting value is 470 pF. The LED behaviors are programmable in the EEPROM and via registers.		
	Add current limiting resistors to LED paths.	Typical current limiting resistors are 250 Ω to 330Ω when using a 3.3 V dc supply. Current limiting resistors are occationally included with integrated magnetic modules.		

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SECTION	**CHECK ITEMS**	**Detail**	**√ Done or Not Done**	**NOTES**
JTAG Circuits	On Rev A0 of the 82580 Pull-down RSVD_JRST_3P3(E13) to Ground with a 10k resister. This will disable JTAG. If JTAG is used RSVD_JRST_3P3(E13) can be driven high after the power up sequence is complete. In later revisions of the 82580 Pull-up RSVD_JRST_3P3(E13) to enable the JTAG interface.	Rev A0 of the 82580 does not reset the JTAG interface as a part of the Power on Reset sequence. This can cause problems with the operation of the 82580. This is fixed in later revisions of the 82580.		
	JTDO (D13) should be pulled up with a 1kΩ resister.	The exact 1kΩ value of the pull-up resister is not critical to the function of the device. 400Ω to 10kΩ is ok. In order to achive 10 MHz high speed jtag access a value of 1kΩ or less is required.		

Layout and Placement Checklist				
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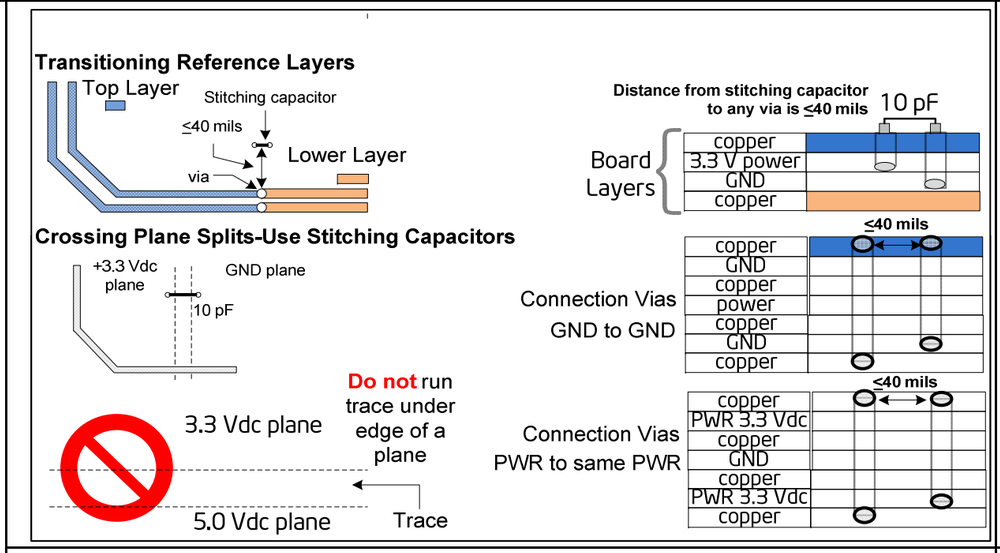
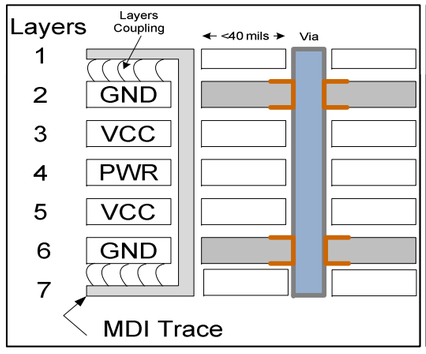
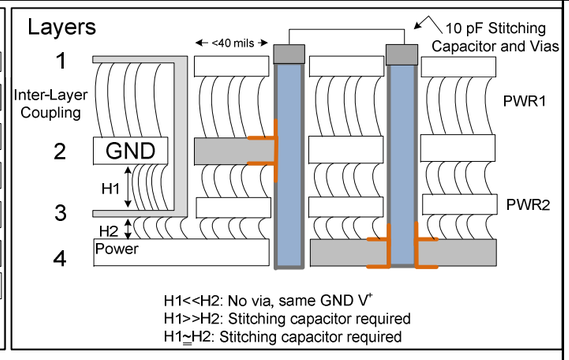
General	Obtain the most recent documentation and specification updates.	Documents are subject to frequent change.		
	Route the transmit and receive differential traces before routing the digital traces. Following the design guide, route the differential PCIe and MDI traces first relative to other traces on the board. Then route the clock traces.			
	IMPORTANT: All impedance controlled signals should be routed in reference to a solid plane. If there are plane splits on a reference layer and the signal traces cross those splits then stitching caps should be used within 40 mils of where the crossing occurs. If signals transition from one reference layer to another reference layer then stitching caps or connecting vias should be used based on the following. If the transition is from power referenced layer to ground referenced layer or from one voltage power referenced layer to a different voltage power referenced layer then stitching caps should be used within 40 mils of the transition. If the transition is from one ground referenced layer to another ground referenced layer or is from a power referenced layer to the same net power referenced layer then connecting vias should be used within 40 mils of the transition.	These are especially important on single ended signaling such as the crystal/oscillator clocking. It is also very important for the MDI differential signaling. If stitching caps or connecting vias are not used then it will increase the probability of having EMI issues, ESD immunity, and may have some IEEE test conformance issues. If this is not followed for single ended signaling (such as the crystal/oscillator trace) then the 25Mhz crystal may broadcast as EMI as well as pick up noise potentially causing jitter and BER issues with longer Ethernet cables. If the bus has several signals or differential pairs it may not be possible to place a single stitching cap or connecting via within 40 mils of all of the signals. In this case multiple stitching caps or connecting vias should be used.		

Layout and Placement Checklist

SECTION	CHECK ITEMS	REMARKS	Done? (Yes/No)	NOTES
			
				
	Obtain the most recent stack-up information including the dielectric constant (dk) within the 1 to 100Mhz range and the dk at 1Ghz or higher from your Printed Circuit Board (PCB) vendor.	This is needed to calculate the transmission line impedance. See below.		
	Refer to the Platform Design Guide (PDG) for detailed routing requirements.			
Placement	The Lan Device must be placed greater than 1" away from any hole to the outside of the chassis bigger than 0.125 inches (125 mils)	The larger the hole the higher the probability the EMI and ESD immunity will be negatively affected.		
	The Lan Device should be placed greater than 250mils from the board edge.	Make sure that the Lan Device is at least 1" from any chassis openings.		

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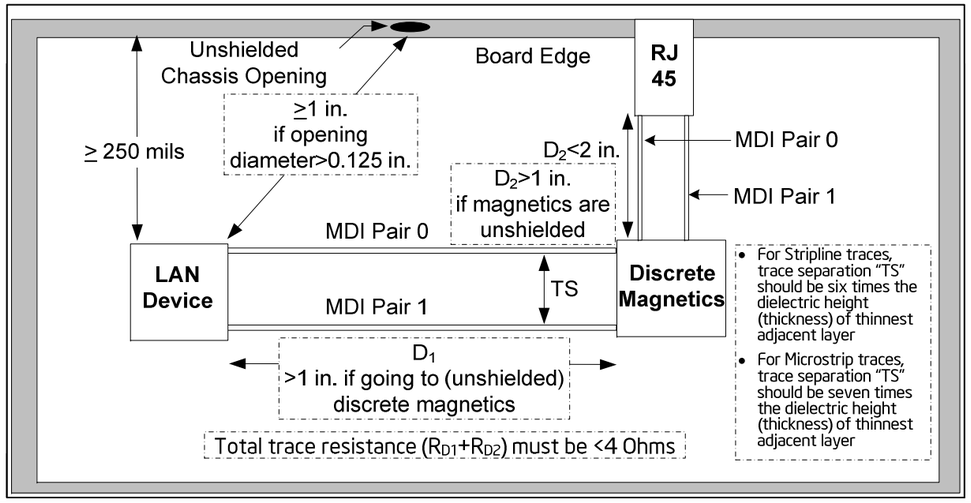
	If the connector or integrated magnetics module is not shielded, the Lan Device should be placed at least one inch from the magnetics (if a LAN switch is not used).	Placing the Lan Device closer than one inch to unshielded magnetics or connectors will increase probability of failed EMI and common mode noise.		
	If there is a LAN switch, the LAN device should be placed within 2 inches	Add Guidance For RSVD_JRST_3P3		
				
	The SE_RSET, GE_REXT3K, PE_TRIM1, and PE_TRIM2 individual trace lengths should be less than 0.5"	The RBIAS is used to set internal current sources. It is more sensitive to noise that can come from the board which could lead to issues with BER, common mode noise, etc..		
Clock Source (Crystal Option)	The crystal trace lengths should be less than 1 inch.	This reduces EMI. This can also affect the IEEE BER, Jitter, and crystal PPM.		
	The crystal load caps should be placed less than 1" from the crystal.			
	The clock lines must be at least 5 times the height of the thinnest adjacent dielectric layer away from other from other digital traces (especially reset signals), I/O ports, board edge, transformers and differential pairs.	This helps reduce EMI. Do not route the crystal traces as differential pairs		
	The clock lines must not cross any plane cuts on adjacent power or ground reference layers unless there are decoupling caps or connecting vias near the transition.	It is best that the clock signals reference a ground plane. If they reference a power plane it is possible they might pick up noise from power sources. Refer to the guidance on impedance controlled signals in the "general" section above on when and where stitching caps or ground vias are needed when crossing plane splits or transitioning between layers.		

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	The clock lines should not cross or run in parallel (within 3x the dielectric thickness of the closest dielectric layer) with any trace (100Mhz signal or higher) on an adjacent layer.			
Clock Source (Oscillator Option)	The oscillator clock trace should be less than 2 inches from the LAN device.	If it is greater than 2 inches then verify the signal quality, jitter, and clock frequency measurements at the LAN Device. The clock lines should also target 50 Ω +/- 15% and should have 33 Ω series back termination placed close to the series oscillator. See the platform design guide.		
	The clock lines must be at least 5 times the height of the thinnest adjacent dielectric layer away from other from other digital traces (especially reset signals), I/O ports, board edge, transformers and differential pairs.	This helps reduce EMI. Do not route the crystal traces as differential pairs		
	The clock lines must not cross any plane cuts on adjacent power or ground reference layers unless there are decoupling caps or connecting vias near the transition.	It is best that the clock signals reference a ground plane. If they reference a power plane it is possible they might pick up noise from power sources. Refer to the guidance on impedance controlled signals in the "general" section above on when and where stitching caps or ground vias are needed when crossing plane splits or transitioning between layers.		
	The clock lines should not cross or run in parallel with any trace (100Mhz signal or higher) on an adjacent layer.			
	The oscillator must have it's own decoupling caps and they must be placed within 0.25 inches.	If a power trace is used (not power plane) the trace from the cap to the oscillator must not exceed 0.25 inches in length. The decoupling caps help to improve the oscillator stability.		
	There should be a ferrite bead within 250 mils of the oscillator power pin	The ferrite bead filters noise off the power supply which translates to less jitter on the transmit and receiver. If the ferrite bead is placed too far away then it becomes ineffective.		
	If there is a ferrite bead on the power trace for the oscillator (see above rule), there must be a 1uF or greater capacitor within 250 mils of the oscillator and connected to the power trace between the oscillator input and ferrite bead.	The bulk decoupling cap reduces the power supply ripple.		

Layout and Placement Checklist				
SECTION	**CHECK ITEMS**	**REMARKS**	**Done? (Yes/No)**	**NOTES**
	If there is a ferrite bead on the power trace for the oscillator there should be a power pour (or fat trace) to supply power to the oscillator.	This will provide a lower series impedance path to the bulk decoupling and power input to the inductor which avoids voltage drops that would cause ringing and jitter.		
General Power Supply Guidance	The user should use planes to deliver power for all DC power rails	Not using planes can cause resistive voltage drop, inductive voltage drop (due to transient or static currents). Some of the symptoms of these voltage drops can include higher EMI, radiated immunity, radiated emissions, IEEE conformance issues, and register corruption. Use the copper loss calculator as an aid to determine the power loss due to trace width.		
	The decoupling capacitors (0.1uF and smaller) should be placed within 250 mils of the LAN silicon			
	The decoupling capacitors (0.1uF and smaller) should be distributed around the Lan Device and some should be in close proximity to the power pins.			
	The bulk capacitors (1uF or greater) should be placed within 1 inch if using a trace (50 mils wide or wider) and within 1.5 inches if using a plane.	The trace does not have to be the full width within the first 50 mils of the C6 pins due to the pin placement.		
PCIe interface	All impedance controlled signals should be routed in reference to a solid plane	Refer to the guidance on impedance controlled signals in the "general" section above on when and where stitching caps or ground vias are needed when crossing plane splits or transitioning between layers.		
	The AC coupling capacitors should be placed within 1" of the transmit or receiver side.	Size 0402, X7R is recommended. The AC coupling capacitors should be placed reasonably close to the transmitter for the PCIe interface for test purposes. This rule is based on the PCIe spec but it typically does not matter where the capacitors are placed. Placing them near the transmitter gives a convenient point to measure the transmitter output.		
	The nominal target differential trace impedance for the PCIe interface data pairs (transmit/receive) should be 85 Ω with ±15% manufacturing tolerance.	Intel recommends that board designers use a 85 Ω differential trace impedance for PCIe I/O with the expectation that the center of the impedance is always targeted at 85 Ω. The ±15% tolerance is provided to allow for board manufacturing process variations and not lower target impedances.		
	The nominal target differential trace impedance for the PCIe interface clock pair should be within the range 90 Ω to 100 Ω with ±15% manufacturing tolerance.	Intel recommends that board designers use a 90 Ω to 100 Ω differential trace impedance for PCIe clock with the expectation that the center of the impedance is always targeted at somewhere between 90 and 100 Ω. The ±15% tolerance is provided to allow for board manufacturing process variations and not lower target impedances.		

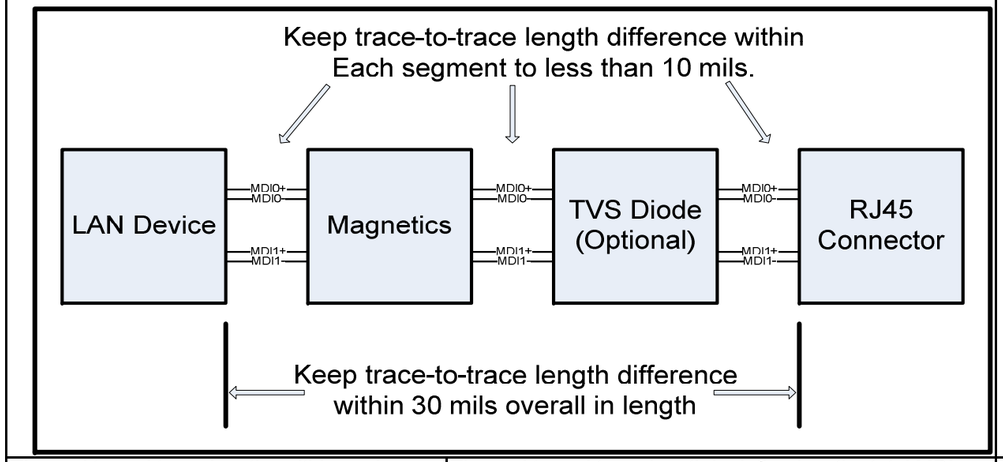
Layout and Placement Checklist				
SECTION	**CHECK ITEMS**	**REMARKS**	**Done? (Yes/No)**	**NOTES**
	The in-pair trace length matching on the PCIe differential pairs should be within 5 mils on a segment by segment basis.	A PCIe segment is defined as any trace within the same layer. For example, transitioning from one layer to another through a via is considered as two separate PCIe segments. The differential pairs within each segment needs to be matched to 5 mils. The PCIe clock runs at a lower frequency and is more tolerant to in-pair length skew mismatch. We recommend less than 20 mils of in-pair skew mismatch on each segment for the clock pair. However, if the clock is within 4x the thinnest adjacent dielectric height of a high speed parallel signal trace then keep the in-pair mismatch within 5 mils.		
	The end to end trace lengths within each PCIe differential pair should match within 5 mils.	The end to end trace length is defined as the total PCIe length from one component to another regardless of layer transitions. For the PCIe clock we recommend less than 20 mils of in-pair end to end length mismatch. However, if the clock is within 4x the thinnest adjacent dielectric height of a high speed parallel signal trace then keep the in-pair mismatch within 5 mils.		
	Whenever the accumulated in-pair skew on the PCIe data pairs exceeds 25 mils then it should be corrected within 600 mils.	The running in-pair skew is the mismatch of each trace within a differential pair on a segment. This mismatch is often caused by bends or staggered pins. The general guidelines is that two bends in the same direction are roughly equivalent to 25mils of skew. The skew can be corrected by adding serpentine routes on the shorter trace to increase its length to match it to its pair. It is acceptable to do this for PCIe. If adding the serpentine route this is a good opportunity to correct the segment by segment in-pair matching to within 5 mils (see rule above).		
	The PCIe spacing between differential pairs and to any other high speed signals (transmit/receive and PCIe clock) should be at least 3x the thinnest adjacent dielectric thickness for stripline and at least 4x for microstrip.	This is to reduce the amount of crosstalk between adjacent pairs. Some platforms might use 5x or greater the distance between pairs if they are using Gen 2 or higher PCIe. Example for 3 mil thick dielectric: For stripline Use a minimum of 9 mil pair-to-pair spacing. For microstrip a minimum of 12 mil pair-to-pair spacing would need to be used. This minimizes crosstalk and noise injection. Tighter spacing is allowed within 200 mils of the components pins.		

Layout and Placement Checklist				
SECTION	**CHECK ITEMS**	**REMARKS**	**Done? (Yes/No)**	**NOTES**
	The distance from the edge of any PCIe trace to the edge of any adjacent reference plane should be at least 3x the thinnest adjacent dielectric thickness for stripline and at least 4x for microstrip	This is to prevent causing an impedance imbalance within a differential pair. This could lead to EMI and reflections.		
SERDES Interface including SGMII, 1000BASE-KX, 1000BASE-BX	All impedance controlled signals should be routed in reference to a solid plane	Refer to the guidance on impedance controlled signals in the "general" section above on when and where stitching caps or ground vias are needed when crossing plane splits or transitioning between layers. For the SERDES interface, the stitching caps and return path vias only need to be within 100 mils instead of 40 mils.		
	The AC coupling capacitors should be placed within 1" of the transmit or receiver side of each device.	Size 0402, X7R is recommended. The AC coupling capacitors should be placed near the transmitter for the SERDES interface. If you are designing for conformance to the PICMG spec then the AC coupling capacitors should be placed near the receiver. If the connection is to an SFP module, then the AC coupling capacitors are not required because they are built into the module.		
	The nominal target differential trace impedance for the SERDES interface data pairs (transmit/receive) should be 100 Ω with ±12% manufacturing tolerance.	Intel recommends that board designers use a 100 Ω differential trace impedance for SERDES I/O with the expectation that the center of the impedance is always targeted at 100 Ω. The ±12% tolerance is provided to allow for board manufacturing process variations and not lower target impedances. We do not recommend traces shorter than 2" due to the risk of a combination of reflections and low insertion loss degrading the signal.		
	For most applications the SERDES trace length should be more than 2" and less than 28".	Longer trace lengths up to 39" can be achieved with thicker dielectrics and wider traces. Ex: 5 mil dielectrics with 5 mil wide traces. We do not recommend traces shorter than 2" due to the risk of a combination of reflections and low insertion loss degrading the signal. There is an APP note and SIM kits are available for verification of specific channel routing parameters.		
	The in-pair trace length matching for each SERDES differential pair should be within 5 mils on a segment by segment basis.	A SERDES segment is defined as any trace within the same layer. For example, transitioning from one layer to another through a via is considered as two separate SERDES segments. The differential pairs within each segment needs to be matched to 5 mils.		

Layout and Placement Checklist				
SECTION	**CHECK ITEMS**	**REMARKS**	**Done? (Yes/No)**	**NOTES**
	The in-pair trace length matching for the total SERDES differential pair channel path from silicon to silicon should match within 50 mils.	The channel path could span across multiple boards. For example, if you had 3 boards in the SERDES path then the in-pair length matching should not deviate more than ~16.5 mils per board.		
	Whenever the accumulated in-pair skew on the PCIe data pairs exceeds 50 mils then it should be corrected within 1 inch.	The running in-pair skew is the mismatch of each trace within a differential pair on a segment. This mismatch is often caused by bends or staggered pins. For 4 mil wide traces, two bends in the same direction could cause about 25 mils of in-pair skew. The skew can be corrected by adding serpentine routes on the shorter trace to increase its length to match it to its pair. It is acceptable to do this for SERDES. If adding the serpentine route this is a good opportunity to correct the segment by segment in-pair matching to within 5 mils (see rule above).		
	The separation from the outside edge of any SERDES trace to any other signal trace on the same layer and any adjacent signal layer (including other SERDES trace pairs) should be at least 6x the thinnest adjacent dielectric thickness for stripline and at least 7x for microstrip. This rule does not apply to the separation within a differential pair.	This is to reduce the amount of crosstalk between adjacent pairs. Example for 3 mil thick dielectric: For stripline Use a minimum of 18 mil pair-to-pair spacing. For microstrip a minimum of 21 mil pair-to-pair spacing would need to be used. This minimizes crosstalk and noise injection. Tighter spacing is allowed within 200 mils of the components pins.		
	The distance from the edge of any SERDES trace to the edge of any adjacent reference plane should be at least 6x the thinnest adjacent dielectric thickness for stripline and at least 7x for microstrip.	This is to prevent causing an impedance imbalance within a differential pair. This could lead to EMI and reflections.		
NC-SI	Traces should be designed for a single ended impedance of 50Ω +20% -10%	The internal buffer of the Manageability Controller is matched to 50Ω with a back terminator so the optimal transmission line is matched to 50Ω		
	The total NC-SI trace length of all connections on a single net should be less than 5.5" when using 4 point multi-drop connections or should be less than 8.5" when using a point to point connection to the Manageability Controller.	To stay conformant to the spec the transmission line needs to be <30pF. Connectors in the transmission path could shorten the allowed length. These length values are the values necessary to be conformant to the spec. Functional designs are possible with traces up to 18" (4 point multi-drop) and 21" (point to point) if spec conformance is not required.		

Layout and Placement Checklist				
SECTION	**CHECK ITEMS**	**REMARKS**	**Done? (Yes/No)**	**NOTES**
EEPROM or Flash Memory	NVM traces should be placed at least 3x the dielectric height from sources of noise (ex: signaling traces or switching power supplies) on the same layer or adjacent layers.	Extremely high levels of switching currents could cause errors reading/writing to the NVM. This separation rule does not apply to low noise or low speed signals (ex: control lines) that don't switch very often.		
	The decoupling capacitors (0.1uF and smaller) should be placed within 250 mils of the NVM.			
SMBus	**System LOM:** The traces should be less than 70 inches for stripline and less than 100 inches for microstrip	These numbers depend on the stackup, dielectric layer thickness, and trace width. The total capacitance on the trace and input buffers should be under 400pF.		
	Add in card: The traces should be less than 7 inches for stripline and less than 10 inches for microstrip	These numbers are conservative and depend on the stackup, dielectric layer thickness, and trace width. Longer traces could be used as long as long as the total capacitance on the trace and input buffers is under 30pF.		
MDI Interface	All impedance controlled signals should be routed in reference to a solid plane	Refer to the guidance on impedance controlled signals in the "general" section above on when and where stitching caps or ground vias are needed when crossing plane splits or transitioning between layers.		
	The MDI traces must not have 90° bends	Bevel corners with turns based on 45° angles or use rounded trace corners.		
	The in-pair trace length matching for each differential pair must be within 10 mils on a segment by segment basis.	An MDI segment is defined as any trace within the same layer. For example, transitioning from one layer to another through a via is considered as two separate MDI segments. The differential pairs within each segment needs to be matched to 10 mils. Do not use serpentine routing (zig zag of shorter trace) to match the trace lengths. Serpentine routing to the RJ-45 connector which connects to long out-of-system unshielded cables can contribute to radiated EMI and can decrease immunity to ESD.		

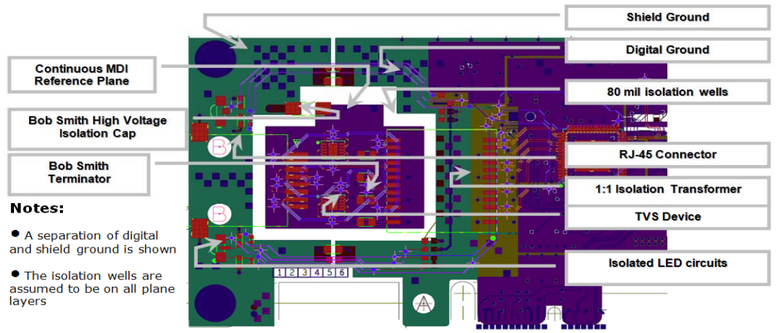
Layout and Placement Checklist

SECTION	CHECK ITEMS	REMARKS	Done? (Yes/No)	NOTES
				
	The end to end trace lengths within each differential pair must match within 30 mils. Make sure to include each segment before and after the AC decoupling caps.	The end to end trace length is defined as the total MDI length from one component to another regardless of layer transitions. The pair to pair length matching is not as critical as the in-pair length matching but it should be within 2 inches. Do not use serpentine routing (zig zag of shorter trace) to match the trace lengths. Serpentine routing to the RJ-45 connector which connects to long out-of-system unshielded cables can contribute to radiated EMI and can decrease immunity to ESD.		
	Aside from vias and their stubs covered in prior rules, there should not be more than two stubs longer than 300 mils per MDI trace.	Stubs cause discontinuities. Stubs could come from vias, MDI termination, TVS stuffing, and test points.		

Layout and Placement Checklist				
SECTION	**CHECK ITEMS**	**REMARKS**	**Done? (Yes/No)**	**NOTES**
	The nominal target differential impedance for the MDI traces should be 100 Ω with ±15% manufacturing tolerance. For MDI traces longer than 3.5" refer to the platform design guide table "design guide for the maximum trace lengths based on trace geometry and board stack-up" to determine maximum recommended traces.	This is a primary requirement for 10/100/1000 Mb/s Ethernet. Paired 50 Ω traces do not make 100 Ω differential. An impedance calculator can be used to verify this. Use a good differential impedance calculator and make sure to work with the fab vendor. If a trusted commercial differential impedance calculator is not available then use the Intel MDI trace calculator. When using impedance calculators and when working with the fab vendor for microstrip traces make sure that the post plating thickness is taken into account. The post plated thickness is typically 1.9 to 2.0 mils. Optimal Trace width and separation of the MDI pairs is influenced by the board stack up in order to achieve the correct impedance. For applications that require a longer MDI trace lengths, Intel recommends that thicker dielectric or lower Er materials be used. This permits higher differential trace impedance and wider, lower loss traces. Target differential impedance is 100 Ω +/- 15% or 95 Ω +/- 10% to stay within the IEEE spec tolerances. Violating these tolerances can lead to issues with return loss, common mode noise, and Bit Error Rate. Complying with this rule is important for longer traces.		
	There should be no more than 2 vias per segment (Lan Device to magnetics or magnetics to RJ45) and there should not be more than 4 vias total.	Every via adds lumped capacitance to the traces at the point it is located. Each reference plane layer that a via passes through typically adds ~0.2pF to the via capacitance. For example, a 6 layer board with 2 reference layers where a via goes from the top layer to the bottom would be ~0.4pF of lump capacitance at that via. This lump capacitance causes a discontinuity in the MDI transmission lines. It is preferable that the vias be located closest to the pins and pads of devices on the MDI path (ex: magnetics, Lan Device, RJ45). Placing the vias farther than an inch from the end points may have a greater adverse impact on return loss and rise/fall times.		

Layout and Placement Checklist				
SECTION	**CHECK ITEMS**	**REMARKS**	**Done? (Yes/No)**	**NOTES**
	The separation from the outside edge of any MDI trace to any other signal trace on the same layer and any adjacent signal layer (including other MDI trace pairs) should be at least 6x the thinnest adjacent dielectric thickness for stripline and at least 7x for microstrip. This rule does not apply to the other trace within the same differential pair.	This is to reduce the amount of crosstalk between adjacent pairs. Example for 3 mil thick dielectric: For stripline Use a minimum of 18 mil pair-to-pair spacing. For microstrip a minimum of 21 mil pair-to-pair spacing would need to be used. This minimizes crosstalk and noise injection. Tighter spacing is allowed within 200 mils of the components' MDI pins.		
	The distance from the edge of any MDI trace to the edge of any adjacent reference plane should be at least 7x the adjacent dielectric.	It keeps the differential signals impedance balanced which enables IEEE conformance and reduces EMI caused by differential to common mode conversion. The 7x distance from the edge of an adjacent reference plane is not the same as 7x from the edge of a board. If the trace is routed near any holes or connectors in the chassis then this rule must be followed.		
	If using an integrated magnetics module without USB, provide a separate chassis ground “island” to ground around the RJ-45 connector. The split in the ground plane should be at least 20 mils wide. If using an integrated magnetics module with USB, do not use a separate chassis ground.	This split is mainly intended for EMI tuning so it does not have to be 80 mils as required for high voltage isolation. It is expected that the high voltage isolation requirements are already built into the integrated+C85 magnetics. The split may not be necessary but can limit EMI performance by 1 to 2 dB. Because integrated magnetics with USB have (Digital) DC power and DC ground there is no way to isolate the chassis ground from the digital ground which limits the ability to tune for potentially 1 to 2 dB better EMI. If the split is used, there should be stuffing options for AC coupling caps across the split on both sides of the magnetic modules. The values of the caps and whether to stuff the caps is determined during EMI testing. A good starting value is 0.1uF.		
	DISCRETE MAGNETICS: In order to meet IEEE high voltage isolation requirements the MDI traces and Bob Smith termination on the RJ45 side (between discrete magnetics and RJ45) must be at least 80 mils from all other traces and plane fills including adjacent layers.	This is to reduce the risk of shock hazard to the end user. Refer to the PDG for routing and placement guidelines. It can also be helpful for ESD and EFT immunity. Solder mask is not sufficient to ensure high voltage isolation. Air bubbles can cause pin holes and therefore it can not be relied upon. Internally routed traces also need to follow this rule because they could potentially arc through air filled pinholes in the glass epoxy dielectric to planes/traces above/below.		

Layout and Placement Checklist

SECTION	CHECK ITEMS	REMARKS	Done? (Yes/No)	NOTES
			
	DISCRETE MAGNETICS: In order to meet IEEE high voltage isolation requirements there must be a separate chassis ground for the LAN connector.	If using a discrete magnetics module, provide a separate chassis ground "island" to ground the shroud of the RJ-45 connector and to terminate the line side of the magnetics module. The physical separation between the ground planes (Chassis and digital) and the reference plane (aka termplane) should be at least 80 mils wide. This separation should run under the center of magnetics module. Differential pairs must never cross the split. Refer to the PDG for more details.		
	USING LAN SWITCH: The total resistance from the LAN device to the LAN magnetics center tap (including LAN switch resistance) must not exceed 10 Ω. **NO LAN SWICH:** The total MDI path resistance from the LAN device to the LAN magnetics center tap must not exceed 4 Ω.	The trace resistance includes the series resistance of any components that might be present such as LAN switches, inductors, or resistors. Desktop designs and some mobile designs do not use a LAN switch. Some embedded designs and many mobile designs use a LAN switch to accommodate alternate MDI paths such as docking stations on mobile designs. Use the copper loss trace length calculator available from Intel to help with the calculation.		
Magnetics Module	ALL MAGNETICS: 1uF caps should be connected within 1" of each magnetics center-tap pin	This decoupling cap helps improve BER. It filters out some of the power supply noise and other noise on the platforms. It can also help reduce conductive EMI.		
	DISCRETE MAGNETICS: 0.1uf caps should be connected within 100 mils of each magnetics center-tap pin	This can decrease radiated emissions and can improve BER. NOTE: Some integrated magnetics do not include this cap internally and need the 0.1uF caps placed. Please check the datasheet to confirm this.		

Layout and Placement Checklist				
SECTION	**CHECK ITEMS**	**REMARKS**	**Done? (Yes/No)**	**NOTES**
	DISCRETE MAGNETICS: The discrete magnetics MDI traces should be less than 2" length from the RJ-45 connector.	Keep as short as possible.		
	DISCRETE MAGNETICS: If the connector is not shielded, the discrete magnetics should be placed at least one inch from the RJ-45 connector.	Placing the discrete magnetics closer than one inch to an unshielded connector will increase probability of failed EMI and common mode noise.		
LED Circuits	Decoupling capacitors should be placed within 250 mils of the LED pins to mitigate potential EMI and ESD issues. If decoupling capacitors are not used then there should be empty pads for placing caps to prevent a potential board redesign.	If the decoupling capacitors are used in conjunction with LED current limiting resistors then a filter could be implemented that will separate the digital ground noise from the chassis noise creating a more robust EMI solution. The preferred package size for the caps are 0402.		
	LAN LED traces should be placed at least 6x (side by side separation) the dielectric height from sources of noise (ex: signaling traces) and susceptible signal traces (ex: reset signals) on the same layer. LAN LED traces should be placed at least 7x (broadside coupling) the dielectric height from sources of noise (ex: signaling traces) and susceptible signal traces (ex: reset signals) on adjacent layers.	LED traces can carry noise into integrated magnetics modules, RJ-45 connectors, or out to the edge of the board, increasing EMI. LED traces can also carry outside ESD/EMP onto adjacent internal signals which can cause issues to other signals. For example: an ESD event can be coupled onto a device reset trace and cause the device or system to reset.		