Intel® 82576 GbE Controller Checklists

LAN Access Division

Project Name	
Fab Revision	
Date	
Schematic Designer	
Layout Designer	
Intel Contact(s)	
Reviewer(s)	

Revision	Date	Changes
0.5	7/9/2007	Initial release.
0.9	4/29/2008	Updated.
0.95	5/26/2008	Add not use signals comment.
2.0	7/3/2008	Updated and released for SRA.
2.1	4/1/2009	Format udpated.
2.2	7/6/2009	PDF'd for Developer. Added project data area on title page.
2.3	9/2/2009	Updated commentable PDF so that it accept comments when used with Reader. If you still have issue with data input in this mode, try upgrading your Acrobat Reader. Consider http://get.adobe.com/reader/. Made some format corrections.
2.4	12/4/2009	Line 21 of the Schematic checklist: Added "NOTE: Even if Wake on LAN is not used a 10K ohm pull-up is still recommended on PE_WAKE_N." Line 107 of the Schematic checklist: "0.1uf" changed to "0.01uF."

12/4/2009

Rev 2.4; 321746-004EN

Schematic Checklist

SECTION	CHECK ITEMS	DETAILS	BALL	Done or Not Done	NOTES
General	Have up-to-date product documentation and specification updates				
	Observe instructions for special pins needing pull- up or pull down resistors.	Do not connect pull-up or pull-down resistors to any pins marked No Connect.			
	Optional interfaces are labeled and must be treated appropriately.	There are many optional interfaces for this silicon that may require unique configuration.			
Pin Compatibility with 82575	82576 adds 2 new pins	The 82576 is pin out compatible with the 82575. the 82576 adds 2 new pins (NCSI_ARB_OUT, NCSI_ARB_IN) that are used if the NC-SI HW Arbitration feature is supported in the design.	B3, AD3		

Schematic Checklist

SECTION	CHECK ITEMS	DETAILS	BALL	Done or Not Done	NOTES
	82575/82526 support	In order to design a board that supports both the 82575 and the 82576, it is necessary to connect both AD3 and B3 balls to optionally stuff, 0-ohm resistors that could be connected to the platform for either 82575 or 82576 implementation. If the NC-SI interface is not used in this particular application for both the 82575 and 82576, then leaving these pins as “no connects” is acceptable.	B3, AD3		
	82576 Support	To enable a 82575 board design for the 82576, stuff the 0-ohm resistors (connected to AD3 and B3) that could then be connected to the appropriate NC-SI arbitration pins of the platform. This is the only special requirement for implementing the 82576 silicon in a design to support both silicon devices and HW Arbitration is supported.	B3, AD3		
PCI-Express Interface	Connect PCI-Express Transmit signals to PCI-Express Host	PCI-Express TX Lane 0 differential signals (PET_0_p and PET_0_n) must be connected to PCI-Express RX Lane 0 of host interface through 0.1uF AC coupling capacitors.	D1 and D2		

Schematic Checklist

SECTION	CHECK ITEMS	DETAILS	BALL	Done or Not Done	NOTES
		PCI-Express TX Lane 1 differential signals (PET_1_p and PET_1_n) must be connected to PCI-Express RX Lane 1 of host interface through 0.1uF AC coupling capacitors.	H1 and H2		
		PCI-Express TX Lane 2 differential signals (PET_2_p and PET_2_n) must be connected to PCI-Express RX Lane 2 of host interface through 0.1uF AC coupling capacitors.	R1 and R2		
		PCI-Express TX Lane 3 differential signals (PET_3_p and PET_3_n) must be connected to PCI-Express RX Lane 3 of host interface through 0.1uF AC coupling capacitors.	W1 and W2		
	Connect PCI-Express Receive signals to PCI-Express Host	PCI-Express RX Lane 0 differential signals (PER_0_p and PER_0_n) must be connected to PCI-Express TX Lane 0 of host interface through 0.1uF AC coupling capacitors.	F1 and F2		
		PCI-Express RX Lane 1 differential signals (PER_1_p and PER_1_n) must be connected to PCI-Express TX Lane 1 of host interface through 0.1uF AC coupling capacitors.	K1 and K2		

Schematic Checklist

SECTION	CHECK ITEMS	DETAILS	BALL	Done or Not Done	NOTES
		PCI-Express RX Lane 2 differential signals (PER_2_p and PER_2_n) must be connected to PCI-Express TX Lane 2 of host interface through 0.1uF AC coupling capacitors.	U1 and U2		
		PCI-Express RX Lane 3 differential signals (PER_3_p and PER_3_n) must be connected to PCI-Express TX Lane 3 of host interface through 0.1uF AC coupling capacitors.	AA1 and AA2		
	Connect PCI-Express differential clock signals to PCI-Express Host clock	PCI-Express differential clock signals (PE_CLK_p and PE_CLK_n) must be connected to PCI-Express differential clock of host interface.	N1 and N2		
	Connect PCI-Express Reset to Host system	PCI-Express Reset signal (PE_RST_N) must be connected to PCI-Express reset signal of host interface.	AC9		
	Connect PCI-Express Wake signal to host	PCI-Express Wake signal (PE_WAKE_N) must be connected to PCE-Express wake signal of host interface.	AC20		

Schematic Checklist

SECTION	CHECK ITEMS	DETAILS	BALL	Done or Not Done	NOTES
		PCI-Express Wake signal (PE_WAKE_N) must be connected to external 10k ohm pull up resistor to 3.3V supply. NOTE: Even if Wake on LAN is not used a 10K ohm pull-up is still recommended on PE_WAKE_N.	AC20		
	Connect PCI-Express compensation resistor	PCI-Express compensation signal (PE_RCOMP) must be connect to ground through a 1.4kohm 1% tolerance resistor.	L1		
Serial Flash Interface	Connect serial Flash interface	Flash chip enable (FLSH_CE_N) must be connected to external 10kohm pull up resistor to 3.3V supply.	AC15		
		Flash clock (FLSH_SCK) must be connected to Flash clock port of external flash device.	AD15		
		Flash data input signal (FLSH_SI), which is actually an output signal must be connected to Flash data input of external flash device.	AC14		
		Flash data output signal (FLSH_SO), which is actually an input signal, must be connected to Flash data output of external flash device.	AD14		
	If a Flash is not used.	Leave FLSH_CE_N, FLSH_SCK, FLSH_SI, FLSH_SO unconnected.			

Schematic Checklist

SECTION	CHECK ITEMS	DETAILS	BALL	Done or Not Done	NOTES
Serial EEPROM Interface	Connect serial EEPROM interface	EEPROM chip enable (EE_CS_N) must be connected to chip select of EEPROM device.	B21		
		EEPROM chip enable (EE_CS_N) must be connected to external 10kohm pull up resistor to 3.3V supply.	B21		
		EEPROM clock (EE_SK) must be connected to EEPROM clock port of external EEPROM device.	B20		
		EEPROM data input signal (EE_DI), which is actually an output signal must be connected to EEPROM data input of external EEPROM device.	A21		
		EEPROM data output signal (EE_DO), which is actually an input signal, must be connected to EEPROM data output of external EEPROM device.	A20		
	If EEPROM is not used	Leave EE_CE_N, EE_SCK, EE_SI, EE_SO unconnected.			
SMBus Interface	Connect SMBus management interface	SMB bidirectional data signal (SMBD) must be connected to SMBus data signal.	AD21		
		SMB bidirectional data signal (SMBD) must be connected to an external 10kohm pull up resistor.	AD21		

Schematic Checklist

SECTION	CHECK ITEMS	DETAILS	BALL	Done or Not Done	NOTES
		SMB clock signal (SMBCLK) must be connected to SMBus clock signal on the platform.	AC21		
		SMB clock signal (SMBCLK) must be connected to an external 10kohm pull up resistor.	AC21		
		SMB alert signal (SMBALRT_N) must be connected to SMBus alert signal on the platform.	AD20		
		SMB alert signal (SMBALRT_N) must be connected to an external 10kohm pull up resistor.	AD20		
	If the SMBus interface is not connected to the system.	The pull-up/pull-down resistors described above should still be in place.			
NCSI interface	Connect NCSI management interface	The NCSI clock input (NCSI_CLK_IN) must be connected to a spec compliant 50MHz clock generated on the platform or to the NCSI_CLK_OUT of the 82576.	B5		
		The NCSI clock input (NCSI_CLK_IN) is recommended to have 10K ohm pull down resistor.	B5		

Schematic Checklist

SECTION	CHECK ITEMS	DETAILS	BALL	Done or Not Done	NOTES
		The NCSI clock output signal (NCSI_CLK_OUT) must be connected to external BMC 50MHz spec compliant input if CLK not implemented externally. NCSI clock output signal must be enabled by EEPROM.	B4		
		The NCSI receive data output signals (NCSI_RXD_1 and NCSI_RXD_0) must be connected to the NCSI data inputs of the external BMC. These signals must have external 10KΩ pull up resistors.	A6 and B7		
		The NCSI carrier sense/receive data valid signal output (NCSI_CRS_DV) must be connected to the CRS/DV input port on the external BMC. This signal must have 10KΩ external pull down resistor.	A4		
		The NCSI transmit data input signals (NCSI_TXD_1 and NCSI_TXD_0) must be connected to the NCSI data outputs of the external BMC. These signals must have external 10KΩ pull up resistors.	A7 and B8		

Schematic Checklist

SECTION	CHECK ITEMS	DETAILS	BALL	Done or Not Done	NOTES
		NC-SI HW_Arbitration signals should be connected if HW Arbitration is to be supported in the design. If not supported, they are recommended to be left unconnected. These are the only 2 pins that have different functionality from the 82575.	B3, AD3		
		The NCSI transmit enable input signal (NCSI_TX_EN) must be connected to the transmit enable output of the external BMC. This signal must have external 10KΩ pull down resistor.	B6		
	If not using NC-SI,	above PU/PDs are still recommended.			
SerDes Port 0/SGMII(SFP)/Optic(SFF) interface	Connect SerDes/SGMII/Optic interface port 0	SerDes port 0 transmit differential signals (SRDSO_0_p and SRDSO_0_n) must be connected to transmit port of the fiber optic transceiver/SFP connector/ Backplane connector.	K23 and K24		
		SerDes port 0 receive differential signals (SRDSI_0_p and SRDSI_0_n) must be connected to the receive port of the fiber optic transceiver/SFP connector/ Backplane connector.	J23 and J24		

Schematic Checklist

SECTION	CHECK ITEMS	DETAILS	BALL	Done or Not Done	NOTES
SerDes Port 0 to SFP	Connect SFP interface port 0	SerDes port 0 SFP interface signals (SFP0_I2C_CLK and SFP0_I2C_DATA) must be connected to I2C interface of the SFP in order to able change registers and settings within the SFP module .	AD19 and AD18		
	Connect SDP to SFP interface port 0	SerDes port 0 SFP interface signals SDP0_1 - TX FAULT SDP0_2 - TDIS SDP0_3 - LOS All pins must be connected to correct SFP interface on platform and to must be connected to external 10kohm pull up resistor to 3.3V supply.	B15, B17 B16		
SerDes Port 0 to SI	Connect SDP to SFF Optic interface port 0	SerDes port 0 SFF interface signals SDP0_2 - TDIS must be connected the TDIS pin of the fiber optic transceiver, must be connected to external 10KΩ pull up resistor to 3.3V supply SDP0_3 - Laser_PWR must be connected the power supply control of fiber optic transceiver if supported is needed to save power. If this is not connected the driver will be unable to turn off the optics to save power.	B15, B17		

Schematic Checklist

SECTION	CHECK ITEMS	DETAILS	BALL	Done or Not Done	NOTES
SerDes Port 1/SGMII(SFP)/Optic(SFF) interface	Connect SerDes/SGMII interface port 1	SerDes port 1 transmit signals (SRDSO_1_p and SRDSO_1_n) must be connected to transmit port of the fiber optic transceiver.	R23 and R24		
		SerDes port 1 receive differential signals (SRDSI_1_p and SRDSI_1_n) must be connected to the receive port of the fiber optic transceiver/SFP connector/ Backplane connector.	T23 and T24		
SerDes Port 1 to SFP	Connect SDP to SFP interface port 1	SerDes port 1 SFP interface signals SDP1_1 - TX FAULT SDP1_2 - TDIS SDP1_3 - LOS All pins must be connected to correct SFP interface on platform and must be connected to external 10kohm pull up resistor to 3.3V supply.	A12, A13, AC10		
	Connect SFP interface port 1	SerDes port 1 SFP interface signals (SFP1_I2C_CLK and SFP1_I2C_DATA) must be connected to I2C interface of the SFP in order to able change registers and settings within the SFP module .	AC19 and AC18		

Schematic Checklist

SECTION	CHECK ITEMS	DETAILS	BALL	Done or Not Done	NOTES
SerDes Port 1 to SI	Connect SDP to Optic interface port 1	SerDes port 0 SFF interface signals SDP1_2 - TDIS must be connected the TDIS pin of the fiber optic transceiver and must be connected to external 10KΩ pull up resistor to 3.3V supply SDP1_3 - Laser_PWR must be connected the power supply control of fiber optic transceiver if supported is needed to save power. If this is not connected the driver will be unable to turn off the optics to save power.	A13, AC10		
SerDes to SFF	Connect SerDes Optic signal detect pins for both port 0 and port 1	SerDes port 0 signal detect pin (SRDS0_SIG_DET) must be connected the signal detect pin of the fiber optic transceiver. If not Optic(SFF) configuration connected to external 10KΩ PU resistor to 3.3v	A9		
		SerDes port 1 signal detect pin (SRDS1_SIG_DET) must be connected the signal detect pin of the fiber optic transceiver. If not Optic(SFF) configuration connected to external 10KΩ PU resistor to 3.3v	A10		

Schematic Checklist

SECTION	CHECK ITEMS	DETAILS	BALL	Done or Not Done	NOTES
	Connect SerDes compensation resistor	SerDes compensation signal (SER_RCOMP) must be connect to ground through a 1.4kohm 1% tolerance resistor.	L22		
If Serdes not in use		Leave serdes signals unconnected.			
If Serdes not in use		Leave SDP signals unconnected.C72			
Ethernet interface	Connect MDI interface for port 0	MDI port 0 channel 0 differential signals (MDI0_p_0 and MDI0_n_0) must be connected to pin 1 and 2 of the RJ45 respectively.	C23 and C24		
		MDI port 0 channel 0 differential signals (MDI0_p_0 and MDI0_n_0) must be connected to 2 49.9 ohm 1% tolerance termination resistors forming a ~100 ohm differential termination with 0.1 uF capacitors attached between center nodes and ground.	C23 and C24		
		MDI port 0 channel 1 differential signals (MDI0_p_1 and MDI0_n_1) must be connected to pin 3 and 6 of the RJ45 respectively.	D23 and D24		

Schematic Checklist

SECTION	CHECK ITEMS	DETAILS	BALL	Done or Not Done	NOTES
		MDI port 0 channel 1 differential signals (MDI0_p_1 and MDI0_n_1) must be connected to 2 49.9 ohm 1% tolerance termination resistors forming a ~100 ohm differential termination with 0.1 uF capacitors attached between center nodes and ground.	D23 and D24		
		MDI port 0 channel 2 differential signals (MDI0_p_2 and MDI0_n_2) must be connected to pin 4 and 5 of the RJ45 respectively.	F23 and F24		
		MDI port 0 channel 2 differential signals (MDI0_p_2 and MDI0_n_2) must be connected to 2 49.9 ohm 1% tolerance termination resistors forming a ~100 ohm differential termination with 0.1 uF capacitors attached between center nodes and ground.	F23 and F24		
		MDI port 0 channel 3 differential signals (MDI0_p_3 and MDI0_n_3) must be connected to pin 7 and 8 of the RJ45 respectively.	G23 and G24		

Schematic Checklist

SECTION	CHECK ITEMS	DETAILS	BALL	Done or Not Done	NOTES
		MDI port 0 channel 3 differential signals (MDI0_p_3 and MDI0_n_3) must be connected to 2 49.9 ohm 1% tolerance termination resistors forming a ~100 ohm differential termination with 0.1 uF capacitors attached between center nodes and ground.	G23 and G24		
	Connect MDI IEEE clock output test signals for port 0	IEEE port 0 clock output differential signals (IEEE_TEST0_p and IEEE_TEST0_n) can be connected to external test header for test access.	A22 and B22		
		Use a two-pin header to access the clock required for IEEE GbE PHY conformance testing.	A22 and B22		
		Connect one pin on the header to the IEEE_TEST0_p and the other pin to IEEE_TEST0_n.	A22 and B22		
		For production applications, all test points may be deleted and signal pins may be left unconnected.	A22 and B22		
	Connect MDI bias resistor for port 0	MDI bias signals for port 0 (RBIAS0) must be connected through a 1.4 kohm 1% tolerance resistor to GND.	E22		

Schematic Checklist

SECTION	CHECK ITEMS	DETAILS	BALL	Done or Not Done	NOTES
	Connect LEDS for MDI port 0	MDI LED linkup signal for port 0 (LED0_0) must be connected to corresponding LED on RJ45.	A19		
		MDI LED activity signal for port 0 (LED0_1) must be connected to corresponding LED on RJ45.	B19		
		MDI LED link 100 signal for port 0 (LED0_2) must be connected to corresponding LED on RJ45.	B18		
		MDI LED link 1000 signal for port 0 (LED0_3) must be connected to corresponding LED on RJ45.	A18		
	Add sites for capacitors on LED lines.	Use 3.3V AUX for designs supporting wakeup. Add approximately one capacitor site per LED for EMI. Suggested starting value 470pF. Determine experimentally.	A18, A19, B18, B19		
	Add current limiting resistors to LED paths, if required.	Typical current limiting resistors are 300-330 ohm when using a 3.3V supply. Current limiting resistors are frequently included with integrated magnetics modules.	A18, A19, B18, B19		
	Connect MDI interface for port 1	MDI port 1 channel 0 differential signals (MDI1_p_0 and MDI1_n_0) must be connected to pin 1 and 2 of the RJ45 respectively.	AB23 and AB24		

Schematic Checklist

SECTION	CHECK ITEMS	DETAILS	BALL	Done or Not Done	NOTES
		MDI port 1 channel 0 differential signals (MDI1_p_0 and MDI1_n_0) must be connected to 2 49.9 ohm 1% tolerance termination resistors forming a ~100 ohm differential termination with 0.1 uF capacitors attached between center nodes and ground.	AB23 and AB24		
		MDI port 1 channel 1 differential signals (MDI1_p_1 and MDI1_n_1) must be connected to pin 3 and 6 of the RJ45 respectively.	AA23 and AA24		
		MDI port 1 channel 1 differential signals (MDI1_p_1 and MDI1_n_1) must be connected to 2 49.9 ohm 1% tolerance termination resistors forming a ~100 ohm differential termination with 0.1 uF capacitors attached between center nodes and ground.	AA23 and AA24		
		MDI port 1 channel 2 differential signals (MDI1_p_2 and MDI1_n_2) must be connected to pin 4 and 5 of the RJ45 respectively.	W23 and W24		

Schematic Checklist

SECTION	CHECK ITEMS	DETAILS	BALL	Done or Not Done	NOTES
		MDI port 1 channel 2 differential signals (MDI1_p_2 and MDI1_n_2) must be connected to 2 49.9 ohm 1% tolerance termination resistors forming a ~100 ohm differential termination with 0.1 uF capacitors attached between center nodes and ground.	W23 and W24		
		MDI port 1 channel 3 differential signals (MDI1_p_3 and MDI1_n_3) must be connected to pin 7 and 8 of the RJ45 respectively.	V23 and V24		
		MDI port 1 channel 3 differential signals (MDI1_p_3 and MDI1_n_3) must be connected to 2 49.9 ohm 1% tolerance termination resistors forming a ~100 ohm differential termination with 0.1 uF capacitors attached between center nodes and ground.	V23 and V24		
	Connect MDI IEEE clock output test signals for port 1	IEEE port 1 clock output differential signals (IEEE_TEST1_p and IEEE_TEST1_n) can be connected to external test header for test access.	AD22 and AC22		
		Use a two-pin header to access the clock required for IEEE GbE PHY conformance testing.	AD22 and AC22		

Schematic Checklist

SECTION	CHECK ITEMS	DETAILS	BALL	Done or Not Done	NOTES
		Connect one pin on the header to the IEEE_TEST1_p and the other pin to IEEE_TEST1_n.	AD22 and AC22		
		For production applications, all test points may be deleted and signal pins may be left unconnected.	AD22 and AC22		
	Connect MDI bias resistor for port 1	MDI bias signal for port 1 (RBIAS1) must be connected through a 1.4 kohm 1% tolerance resistor to GND.	Y22		
	Connect LEDS for MDI port 1	MDI LED linkup signal for port 1 (LED1_0) must be connected to corresponding LED on RJ45.	AD13		
		MDI LED activity signal for port 1 (LED1_1) must be connected to corresponding LED on RJ45.	AC11		
		MDI LED link 100 signal for port 1 (LED1_2) must be connected to corresponding LED on RJ45.	AC13		
		MDI LED link 1000 signal for port 1 (LED1_3) must be connected to corresponding LED on RJ45.	AC12		
	Add sites for capacitors on LED lines.	Use 3.3V AUX for designs supporting wakeup. Add approximately one capacitor site per LED for EMI. Suggested starting value 470pF. Determine experimentally.	AC12, AC13, AC11, AD13		

Schematic Checklist

SECTION	CHECK ITEMS	DETAILS	BALL	Done or Not Done	NOTES
	Add current limiting resistors to LED paths, if required.	Typical current limiting resistors are 300-330 ohm when using a 3.3V supply. Current limiting resistors are frequently included with integrated magnetics modules.	AC12, AC13, AC11, AD13		
Magnetics Module	Place the magnetics module between the silicon and the RJ-45	Applies to designs using discrete magnetics modules.			
	Integrated magnetics modules/RJ-45 connectors are available to minimize space requirements.	Modules with integrated USB are typical.			
	Qualify magnetics module carefully for Return Loss, Insertion Loss, Open Circuit Inductance, Common Mode Rejection, and Crosstalk Isolation	Magnetics module is critical to passing IEEE PHY conformance tests and EMI test.			

Schematic Checklist

SECTION	CHECK ITEMS	DETAILS	BALL	Done or Not Done	NOTES
	Supply 1.8V to the silicon side of the transformer center taps and use **a 0.01uF bypass capacitor** on every center tap pin (silicon side) of the magnetics module.	The 82576 requires 1.8V power on the MDI magnetic center taps for normal operation.C131			
		Magnetics with four center tap pins may have better IEEE performance than those with 1-2 center tap pins. Use capacitors with low Equivalent Series Resistance.			
Crystal Interface	Connect clock signals to external crystal	The clock signals (XTAL1 and XTAL2) must be connected to external 25MHz crystal oscillator.	N23 and N24		
		30 ohm resistor must be connected in series with N24. See reference schematic for connectivity details.	N24		
		The clock signals (XTAL1 and XTAL2) must be connected to external 27pF 5% tolerance capacitors to ground.	N23 and N24		
		If using an oscillator instead, contact Intel for important circuit modifications. Avoid PLL clock buffers.	N23 and N24		

Schematic Checklist

SECTION	CHECK ITEMS	DETAILS	BALL	Done or Not Done	NOTES
		Capacitance affects accuracy of the frequency. Must be matched to crystal specs specified in datasheet, including estimated trace and pin capacitance.	N23 and N24		
		Read Intel Technical Advisory TA-181 regarding important crystal placement and layout.			
JTAG interface	Connect JTCK signal	JTAG clock signal (JTCK) must be connected to JTAG clock signal of the platform.	AC6		
	Connect JTDI signal	JTAG data input signal (JTDI) must be connected to JTAG data input of the platform.	AD7		
		JTAG data input signal (JTDI) must be connected to an external 1 kohm pull up resistor to 3.3V.	AD7		
	Connect JTDO signal	JTAG data output signal (JTDO) must be connected to JTAG data output signal of the platform.	AC8		
		JTAG data output signal (JTDO) must be connected to an external 1 kohm pull up resistor to 3.3V.	AC8		
	Connect JTMS signal	JTAG TMS signal (JTDI) must be connected to JTAG TMS signal of the platform.	AC7		
		JTAG TMS signal (JTDI) must be connected to an external 1 kohm pull up resistor to 3.3V.	AC7		

Schematic Checklist

SECTION	CHECK ITEMS	DETAILS	BALL	Done or Not Done	NOTES
	If the JTAG interface is not connected to the system,	the above pull-up/pull-down resistors should still be in place.			
Misc Signals	Connect Main Power OK signal	Main Power OK signal (MAIN_PWR_OK) must be connected externally to a signal indicating the MAIN power is present for the LAN silicon.	AD4		
	Connect Auxiliary Power indicator	Auxiliary Power indicator signal (AUX_PWR) must be connected 3.3V AUX through an external 3.3 kohm resistor if AUX power is available.	B14		
		Auxiliary Power indicator signal (AUX_PWR) must be connected ground through an external 10 kohm resistor if AUX power is NOT available.	B14		
	Connect Device OFF signal	Device off signal (DEV_OFF_N) if used, must be connected to a super IO signal on the platform at retains its value during reset.	B9		
	Connect LAN disable signal for port 0	LAN disable port 0 signal (LAN0_DIS_N) must be connected to external IO dedicated to this function.	B13		
	Connect LAN disable signal for port 1	LAN disable port 1 signal (LAN1_DIS_N) must be connected to external IO dedicated to this function.	A15		

Schematic Checklist

SECTION	CHECK ITEMS	DETAILS	BALL	Done or Not Done	NOTES
Reserved Signals	Reserved NC signals	Reserved signals (RSVDM3_NC, RSVDM2_NC, RSVDAB19_NC, RSVDAB18_NC, RSVDM23_NC, RSVDM24_NC, RSVDAC16_NC, RSVDAC17_NC, RSVDAD16_NC and RSVDAD17_NC) should NOT be connected on the board.	M3, M2, AB19, AB18, M23, M24, AC16, AC17, AD16, AD17		
	Connect reserved 3.3V pins	Reserved signals (RSVDAD9_3P3, RSVDA8_3P3, RSVDA11_3P3, RSVDB12_3P3, RSVDB10_3P3, RSVDB11_3P3) must be connected to 3.3V on the board.	AD9, A8, A11, B10, B11, B12		
	Connect reserved 3.3V pins	RSVDAC5_3P3 must be connected to 10KΩ 3.3v PU.	AC5		
	Connect reserved 1.0V pins	Reserved signals (RSVDL14_1P0 and RSVDP14_1P0) must be connected to 1.0V on the board.	L14 and P14		
	Connect reserved VSS pins	Reserved signals (RSVDA14_VSS, RSVDAD8_VSS) must be connected to VSS on the board.	A14, AD8		
No Connect Signals	No connect signals	No connect signal (NCAC3) should not be connect on the board.	AC3		

Schematic Checklist

SECTION	CHECK ITEMS	DETAILS	BALL	Done or Not Done	NOTES
Power Supply Connections	Connect 3.3V supply	3.3V voltage supply signals (VCC3P3) must be connected to 3.3V supply voltage.	AD6, AD12, A5, A17		
		3.3V voltage supply signals (VCC3P3) must be connected to decoupling capacitors as specified in the design guide.	AD6, AD12, A5, A17		
	High speed decoupling and bulk capacitors for 3.3V supply	The minimum acceptable decoupling by power supply is as follows (not including decoupling at magnetic):	AD6, AD12, A5, A17		
		VCC3P3 Decoupling 1 - 10 uF bulk 3 - 0.1 uF high speed.	AD6, AD12, A5, A17		
	Connect 1.8V supply	1.8V voltage supply signals (VCC1P8) must be connected to 1.8V supply voltage.	P5, P4, N9, N8, N5, N4, M9, M8, M5, M4, L9, L8, L5, L4, L15, K15, J15, H15, G15, E20, E19, D20, D19, Y20, Y19, V15, U15, T15, R15, P15, AA20, AA19, N21, N15, M21, M15, P9, P8.		
		1.8V voltage supply signals (VCC1P8) must be connected to decoupling capacitors as specified in the design guide.			
	High speed decoupling and bulk capacitors for 1.8V supply	The minimum acceptable decoupling by power supply is as follows (not including decoupling at magnetic):	P5, P4, N9, N8, N5, N4, M9, M8, M5, M4, L9, L8, L5, L4, L15, K15, J15, H15, G15, E20, E19, D20, D19, Y20, Y19, V15, U15, T15, R15, P15, AA20, AA19, N21, N15, M21, M15, P9, P8.		
		VCC1P8 Decoupling 1 - 10 uF bulk 6 - 0.1 uF high speed			

Schematic Checklist

SECTION	CHECK ITEMS	DETAILS	BALL	Done or Not Done	NOTES
	Connect 1.0V supply	1.0V voltage supply signals (VCC1P0) must be connected to 1.0V supply voltage.	V5, V4, U5, U4, P11, N11, M11, L11, H5, H4, G5, G4, J21, J20, J18, J17, L21, L20, L18, L17, K21, K20, K18, K17, T21, T20, T18, T17, P21, P20, P18, P17, R21, R20, R18, R17, K11, K12, K13, K14, L12, L13, P12, P13, R11, R12, R13, R14.		
		1.0V voltage supply signals (VCC1P0) must be connected to decoupling capacitors as specified in the design guide.			
	High speed decoupling and bulk capacitors for 1.0V supply	The minimum acceptable decoupling by power supply is as follows (not including decoupling at magnetic):	V5, V4, U5, U4, P11, N11, M11, L11, H5, H4, G5, G4, J21, J20, J18, J17, L21, L20, L18, L17, K21, K20, K18, K17, T21, T20, T18, T17, P21, P20, P18, P17, R21, R20, R18, R17, K11, K12, K13, K14, L12, L13, P12, P13, R11, R12, R13, R14.		
		VCC1P0 Decoupling 1 - 10 uF bulk 8 - 0.1 uF high speed			
Chassis Ground (10/ 100/ 1000BASE-T Applications)	Connect Ground	Ground signals (VSS) must be connected to the ground of the board.			

Y9, Y8, Y7, Y6, Y15, Y14, Y13, Y12, Y11, Y10, W9, W8, W7, W14, W13, W12, W11, W10, V9, V8, V14, V13, V12, V11, V10, U9, U14, U13, U12, U11, U10, T14, T13, T12, T11, N14, N13, N12, M14, M13, M12, J14, J13, J12, J11, H9, H14, H13, H12, H11, H10, G9, G8, G14, G13, G12, G11, G10, F9, F8, F7, F14, F13, F12, F11, F10, E9, E8, E7, E6, E15, E14, E13, E12, E11, E10, D9, D8, D7, D6, D5, D16, D15, D14, D13, D12, D11, D10, C9, C8, C7, C6, C5, C4, C17, C16, C15, C14, C13, C12, C11, C10, B2, B1, AD5, AD2, AD11, AD1, AC4, AC2, AC1, AB9, AB8, AB7, AB6, AB5, AB4, AB17, AB16, AB15, AB14, AB13, AB12, AB11, AB10, AA9, AA8, AA7, AA6, AA5, AA16, AA15, AA14, AA13, AA12, AA11, AA10, A3, A2, A1, Y24, Y23, Y21, Y18, Y17, Y16, W21, W20, W19, W18, W17, W16, W15, V22, V21, V20, V19, V18, V17, V16, U24, U23, U22, U21, U20, U19, U18, U17, U16, T22, T19, T16, R22, R19, R16, P24, P23, P22, P19, P16, N22, N20, N19, N18, N17, N16, M22, M20 M19, M18, M17, M16, L24, L23, L19, L16, K22, K19, K16, J22, J19, J16, H24, H23, H22, H21, H20, H19, H18, H17, H16, G22, G21, G20, G19, G18, G17, G16, F21, F20, F19, F18, F17, F16, F15, E24, E23, E21, E18, E17, E16, D22, D21, D18, D17, C22, C21, C20, C19, C18, B24, B23, AD24, AD23, AC24, AC23, AB22, AB21, AB20, AA22, AA21, AA18, AA17, A24, A23, Y5, Y4, Y3, Y2, Y1, W6.

Schematic Checklist

SECTION	CHECK ITEMS	DETAILS	BALL	Done or Not Done	NOTES
	If possible, provide a separate chassis ground to connect the shroud of the RJ-45 connector and to terminate the line side of the magnetics module.	This design technique decreases EMI of magnetics without integrated USB. Place pads for approximately four “stitching” capacitors to bridge the gap from chassis ground to signal ground. Typical values range from 0.1uF to 4.7uF. Determined experimentally.			
	High speed decoupling and bulk capacitors for 1.0V supply	Do not use a separate chassis ground when using magnetics with integrated USB. The split ground may increase the EMI of the USB signals or cause energy to couple from the USB interface to the Ethernet cable.			

Schematic Checklist

SECTION	CHECK ITEMS	DETAILS	BALL	Done or Not Done	NOTES

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Layout and Placement Checklist

SECTION	CHECK ITEMS	DETAILS	Done or Not Done	NOTES
General	Have up-to-date product documentation and spec updates	Documents are subject to frequent change		
	Route the PCI-Express, Ethernet and SerDes differential traces before routing the digital traces.	Layout of differential traces is critical.		
		See design guide for detailed routing requirements.		
Ethernet Device	Place the silicon at least 1 inch from the edge of the board. A1	With closer spacing, the strongest fields do not have path to GND and may cause EMI problems.		
	Place the RBIAS compensation resistor for port 0 less than 1 inch from the silicon.			
	Place the RBIAS compensation resistor for port 1 less than 1 inch from the silicon.			
	Place the PE_RCOMP compensation resistor for less than 1 inch from the silicon.			
	Place the SER_RCOMP compensation resistor for less than 1 inch from the silicon.			
Clock Source	Place crystal and load capacitors less than 0.75 inches from the Ethernet device.	This includes spacing to other digital traces, I/O ports, board edge, transformers and differential pairs		
	Keep crystal lines 15 mils away from other signals	6 mil width is best for low capacitance, which is important for crystal circuit frequency accuracy.		
	Crystal traces are 6 mil width	Check trace impedance with an impedance calculator.		
	Read Intel Technical Advisory TA-181 regarding important crystal placement and layout.	Comply with TA-181 requirements.		
MDI Differential Pairs	Design traces for 100 ohm differential impedance (± 20%)	Traces will be 4 mils wide with 8 mils of separation (inside of a pair) for designs with a dielectric thickness of 2.8 mils, nominal.		

Layout and Placement Checklist

SECTION	CHECK ITEMS	DETAILS	Done or Not Done	NOTES
		With closer spacing, fields can follow the surface of the magnetics module or wrap past edge of board, increasing EMI. If the board does not have power and ground planes along the edge, the problem could be worse.		
	Place the silicon at least 1 inch from the integrated magnetics module but less than 4 inches	Larger spacing increases the insertion loss of the MDI signals and decreases amplitude which may cause IEEE failures.		
		Optimum location is approximately 1 inch behind the magnetics module.		
		If trace length is a problem, use thicker board dielectrics to allow wider traces. Thicker copper is even better than wider traces.		
	Avoid highly resistive traces, for example, 4 mil traces longer than 4 inches.	Try to match the pairs at pads, vias and turns. Establish rules carefully for the autorouter. Asymmetry contributes to impedance mismatch.		
	Make traces symmetrical	Bevel corners with turns based on 45° angles		
	Do not make 90° bends	If using through holes (vias), the budget is two 10 mil finished hole size vias per trace.		
	Minimize through holes (vias).	Minimizes signal skew and common mode noise. Improves long cable performance.		
	Keep trace-to-trace length difference within each pair to less than 50 mils.	Keep differences under approximately 2 inches. A 25% difference in length from longest pair to shortest pair is typical.		

Layout and Placement Checklist

SECTION	CHECK ITEMS	DETAILS	Done or Not Done	NOTES
	Pair-to-pair differences in length are not critical.	Minimizes crosstalk and noise injection. Guard traces are generally not recommended and will reduce the impedance if done incorrectly.		
	Keep differential pairs 30 mils or more away from each other and away from parallel digital traces.	If the component or MDI traces are near the board edge, EMI could increase.		
	Keep traces greater than 0.1 inches away from the board edge.	Run pairs on different layers as needed to improve routing. Use layers adjacent to ground layers. There must be no splits in the GND planes.		
	Route traces on appropriate layers.	When differential signals transition from one board layer to another, place ground vias within 40 mils of the signal vias.		
		If the differential signals transition from a ground referenced layer to a power referenced layer, place a decoupling cap on the power and ground within 40 mils of the signal vias.		
		Avoid broadside coupling to traces on other layers. The broadside effect will significantly increase the insertion loss and reduce signal quality.		
		Make sure digital signals on adjacent layers cross at 90° angles.		
		Improves IEEE performance by reducing reflections. Use symmetrical pads. Minimize any stubs.		
	Place MDI termination resistors and capacitors less than 0.25 inches from the Ethernet device	Placement contributes directly to IEEE performance.		

Layout and Placement Checklist

SECTION	CHECK ITEMS	DETAILS	Done or Not Done	NOTES
Magnetics Module	Capacitors connected to center taps should be placed less than 0.1 inch to magnetics module.	Narrow finger-like planes and very wide traces are allowed. If using traces, aim for 100 mils (minimum).		
	Deliver 1.8V to the magnetic center tap with a plane.	Planes are lower inductance and lower resistance than traces and provide better IEEE performance.		
		Paired 50 ohm traces do not make 100 ohm differential. Check impedance calculator.		
PCI-Express Interface	Design traces for 100 ohm differential impedance (± 20%)	Traces will be 4 mils wide with 8 mils of separation (inside of a pair) for designs with a dielectric thickness of 2.8 mils, nominal.		
		For long distances, thick traces are preferred over wide traces. Modify board stackup if necessary to avoid highly resistive traces.		
	Long traces are allowed up to 14 inches, but avoid highly resistive traces.	Traces should be routed diagonal to the FR4 weave to maintain consistent impedance.		
		If 1 oz copper is used, minimim trace spacing within each differential pair must be >= 8 mils.		
		Try to match the pairs at pads, vias and turns. Establish rules carefully for the autorouter. Asymmetry contributes to impedance mismatch.		
	Make traces symmetrical	Bevel corners with turns based on 45° angles.		
	Do not make 90° bends	If using through holes (vias), the budget is six 10 mil finished hole size vias per trace.		
	Minimize through holes (vias).	Traces will be 4 mils wide with 8 mils of separation (inside of a pair) for designs with a dielectric thickness of 2.8 mils, nominal.		

Layout and Placement Checklist

SECTION	CHECK ITEMS	DETAILS	Done or Not Done	NOTES
	Keep traces close together within differential pairs.	If spacing is less than 6 mils, it is almost impossible to achieve >90 ohm differential impedance.		
		Minimizes signal skew and reduces common mode conversion.		
	Keep trace-to-trace length difference within each pair to less than 10 mils.	The minimum separation is 15 mils for designs with a dielectric thickness of 2.8 mils, nominal. Minimizes crosstalk and noise injection. This includes spacing to other digital traces, I/O ports, board edge, transformers and differential pairs.		
	Keep PCI-Express differential pairs approximately 15 mils or greater away from each other.	If using a larger dielectric thickness, keep adjacent traces away by at least 6X the dielectric thickness. For example, 4.5 mil thick FR4; spacing >= 27 mils.		
		Reduces EMI.		
	Keep traces greater than 0.1 inch from the board edge	Use zero ohm resistors sparingly if needed.		
	Avoid unused pads and stubs along the traces	Run pairs on different layers as needed to improve routing. Use layers adjacent to ground layers. There must be no splits in the GND planes.		
	Route traces on appropriate layers always referenced to GND.	When differential signals transition from one board layer to another, place ground vias within 40 mils of the signal vias.		
		If the differential signals transition from a ground referenced layer to a power referenced layer, place a decoupling cap on the power and ground within 40 mils of the signal vias.		

Layout and Placement Checklist

SECTION	CHECK ITEMS	DETAILS	Done or Not Done	NOTES
		Avoid broadside coupling to traces on other layers. The broadside effect will significantly increase the insertion loss and reduce signal quality.		
		Make sure digital signals on adjacent layers cross at 90° angles.		
		The AC coupling is always at the receiver on the PCI-Express interface.		
	For the PCI-Express interface, place AC coupling capacitors close to the transmitters.	Reduces oscillation and ripple in the power supply.		
Power Supply and Signal Ground	Use planes to deliver power.	Planes are lower inductance and lower resistance than traces.		
	Use decoupling and bulk capacitors generously.	Place decoupling and bulk capacitors close to Ethernet device, with some along every side, using short, wide traces and large vias. If power is distributed on traces, bulk capacitors should be used at both ends.		
	Consider using a separate chassis ground for the LAN connector.	If using a discrete magnetics module, provide a separate chassis ground "island" to ground the shroud of the RJ-45 connector and to terminate the line side of the magnetics module. This design improves EMI behavior. Split in ground plane should be at least 50 mils wide. Split should run under center of magnetics module. Differential pairs never cross the split.		

Layout and Placement Checklist

SECTION	CHECK ITEMS	DETAILS	Done or Not Done	NOTES
		If using an integrated magnetics module without USB, provide a separate chassis ground "island" to ground around the RJ-45 connector. Split in ground plane should be at least 50 mils wide.		
		If using an integrated magnetics module with USB, do not use a separate chassis ground.		
		If using an integrated magnetics module without USB, place 4-6 pairs of pads for "stitching" capacitors to bridge the gap from chassis ground to signal ground. Determine exact number and values empirically based on EMI performance. Expect to populate approximately two capacitor sites.		
	Consider placing ground stitching caps.	If using an integrated magnetics module with USB, do not use stitching capacitors.		
LEDs	Keep LED traces away from sources of noise, for example, high speed digital traces running in parallel.	LED traces can carry noise into integrated magnetics modules, RJ-45 connectors, or out to the edge of the board, increasing EMI.		
	If using decoupling capacitors on LED lines, place them carefully.	Capacitors on LED lines should be placed near the LEDs (typically adjacent to integrated magnetics module).		

Layout and Placement Checklist

SECTION	CHECK ITEMS	DETAILS	Done or Not Done	NOTES

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