Intel® 82573E/V/L Layout Checklist (version 1.5)

Project Name	
Fab Revision	
Date	
Designer	
Intel Contact	

SECTION	CHECK ITEMS	REMARKS	√ DONE	COMMENTS
General	Obtain the most recent documentation and specification updates	Documents are subject to frequent change		
	Route the transmit and receive differential traces before routing the digital traces.	Layout of differential traces is critical.		
Ethernet Devices	Place the Ethernet silicon at least 1 inch from the edge of the board.	With closer spacing, fields can follow the surface of the magnetics module or wrap past edge of board. EMI may increase. Optimum location is approximately 1 inch behind the magnetics module.		
	Place the silicon at least 1 inch from the integrated magnetics module but less than 4 inches	Keep trace length under 4 inches from the Ethernet controller through the magnetics to the RJ-45 connector. Signal attenuation will cause problems for traces longer than 4 inches. However, due to EMI, the silicon should be placed at least 1 inch away from the magnetics module.		
	Place the AC coupling capacitors on the PCIe* Tx traces as close as possible to the 82573E/V/L but not further than 250 mils.	Size 0402, X7R is recommended. The AC coupling capacitors should be placed near the transmitter for PCIe*.		
	For the 82573 controller, ensure the trace impedance for the PCIe* differential pairs is 100 Ω +/- 20%.	These traces should be routed differentially.		
	Match trace lengths between PCIe* pairs to within 3 inches.			
	Match trace lengths within each PCIe* pair on a segment-by-segment basis. Match trace lengths within a pair to 5 mils.			
Clock Source	Place crystal and load capacitors within 0.75 inches of the Ethernet device.	This reduces EMI.		
	Match the length of the clock lines to within 200 mils.	A large difference in length between the clock lines leads to clock skew.		
	Keep clock lines away from other digital traces (especially RESET signals), I/O ports, board edge, transformers and differential pairs	This reduces EMI.		
Non-Volatile Memory	Ensure that traces meet the specifications of the design guide (placement is not critical). Refer to the design guide for routing specifications for particular stackups.	EEPROM and Flash can be placed a few inches away from Ethernet controller to provide better spacing of critical components.		

	Place 47Ω damping resistors on the NVM lines close to the signal driver. 0.1inches is recommended. Please refer to the design guide for all length requirements.			
	For both shared and dedicated NVM configuration options, place 0 Ω resistors to minimize the stubs on the NVM lines for each option.			
Transmit and Receive Differential Pairs	Design traces for 100 Ω differential impedance (± 20%)	Primary requirement for 10/100/1000 Mb/s Ethernet. Paired 50 Ω traces do not make 100 Ω differential. An impedance calculator can be used to verify this.		
	Avoid highly resistive traces (for example, 4 mil traces longer than 4 inches)	If trace length is a problem, use thicker board dielectrics to allow wider traces. Thicker copper is even better than wider traces.		
	Make traces symmetrical	Pairs should be matched at pads, vias and turns. Rules for the autorouter should be carefully established. Asymmetry contributes to impedance mismatch. MDI pairs must not use autorouter.		
	Do not make 90° bends	Bevel corners with turns based on 45° angles		
	Avoid through holes (vias).	If vias are used, the budget is two per trace.		
	Keep traces close together inside a differential pair.	Traces should be kept within 10 mils regardless of trace geometry.		
	Keep trace-to-trace length difference within each pair to less than 50 mils.	This minimizes signal skew and common mode noise. Improves long cable performance.		
	Pair-to-pair trace length does not have to be matched as differences are not critical.	The difference between the length of longest pair and the length of the shortest pair should be kept below 2 inches.		
	Try to keep differential pairs 50 mils or more away from each other and other traces, including NVM traces and parallel digital traces.	This minimizes crosstalk and noise injection. Pairs may be spaced as close as 30 mils as long as crosstalk isolation is 34 dB or more. Tighter spacing is allowed closer to connections.		
	Keep traces at least 0.1 inches away from the board edge.	This reduces EMI.		
	Avoid unused pads and stubs along the traces	Unused pads and stubs cause impedance discontinuities.		
	Route traces on appropriate layers.	Pairs should be run on different layers as needed to improve routing. Digital signals on adjacent layers must cross at 90° angles. Splits in power and ground planes must not cross.		
	Place termination resistors and capacitors close to Ethernet device	This prevents reflections. Symmetrical pads should be used. Termination components should not be connected to differential pairs with stub traces.		
Magnetics Module (10/100/1000 Base-T applications)	Capacitors connected to center taps should be placed very close (less than 0.1 inch recommended) to integrated magnetics module.	This improves Bit Error Rate (BER).		

Power Supply and Signal Ground	When using the internal regulator control circuits of the 82573 controller with external PNP transistors, keep the distance from the CTRL_12 and CTRL_25 output balls to the transistors very short (less 0.5 inches) and use 25 mil (minimum) wide traces.	A low inductive loop should be kept from the regulator control pin, through the PNP transistor, and back to the chip from the transistor's collector output. The power pins should connect to the collector of the transistor through a power plane to reduce the inductive path. This reduces oscillation and ripple in the power supply.		
	Use planes if possible.	Narrow finger-like planes and very wide traces are allowed. If traces are used, 100 mils is the minimum.		
	The 1.2V and 2.5V regulating circuits require 1/2 inch x 1/2 inch thermal relief pads for each PNP.	The pads should be placed on the top layer, under the PNP.		
	A 1Ω 0.5 W resistor should be placed at the emitter of the PNP for the 1.2V regulating circuit.	This resistor is used for heat dissipation.		
	Use decoupling and bulk capacitors generously. The 1.2V and 2.5V rails should have 25 μF of capacitance. Place these to minimize the inductance from each power pin to the nearest decoupling capacitor. 40 μF is recommended at the emitter (on the 3.3V rail) of each PNP used in the voltage regulating circuit.	Place decoupling and bulk capacitors close to Ethernet device, with some along every side, using short, wide traces and large vias. If power is distributed on traces, bulk capacitors should be used at both ends. If power is distributed on cards, bulk capacitors should be used at the connector.		
	If using decoupling capacitors on LED lines, place them carefully.	Capacitors on LED lines should be placed near the LEDs.		
Chassis Ground	If possible, provide a separate chassis ground "island" to ground the shroud of the RJ-45 connector and to terminate the line side of the magnetics module. This design improves EMI behavior.	The split in ground plane should be at least 50 mils. The split should run under center of magnetics module. Differential pairs never cross the split.		
	Place 4-6 pairs of pads for "stitching" capacitors to bridge the gap from chassis ground to signal ground.	Determine exact number and values empirically based on EMI performance.		
LED Circuits	Keep LED traces away from sources of noise, for example, high speed digital traces running in parallel.	LED traces can carry noise into integrated magnetics modules, RJ-45 connectors, or out to the edge of the board, increasing EMI.		