Intel® 82573 Schematic Checklist (version 1.6)

Project Name	
Fab Revision	
Date	
Designer	
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Reviewer	

SECTION	CHECK ITEMS	REMARKS	√ DONE	COMMENTS
General	Obtain the most recent documentation and specification updates	Documents are subject to frequent change		
	Observe instructions for special pins needing pull-up or pull-down resistors	Do not connect pull-up or pull-down resistors to any pins marked No Connect, Test, or Reserved.		
82573 Controller	Connect PCIe* interface pins to corresponding pins on ICH			
	Place AC coupling capacitors (0.1μF) near the PCIe* transmitter			
	Connect balls G2 PE_CLKn and G1 PE_CLKp to 100 MHz PCIe* system clock			
	Connect PE_RST# to PLTRST# on the ICH			
	Connect PE_WAKE# to PE_WAKE# on the ICH			
	Connect ball P5 LAN_PWR_GOOD to RSMRST# on the ICH	Connect to the reset supervisor for the LAN power well		
	Connect ball L7 DEVICE_OFF# to SUPER_IO_GP_DISABLE#	Connect to a super I/O pin that retains its value during PCIe* reset, is driven from the resume well and defaults to one on power-up. If not connected to a super I/O pin, then Device_Off# should be connected with an external pull-up resistor.		
	Pull-down ball D12, PHY_REF, with a 4.99 KΩ 1% resistor			
	Pull-down ball A13 TEST_EN with a 3.3 KΩ resistor			
	Leave ball C3, DOCK_IND, unconnected. This feature is not supported in the 82753.			
	82573L only: Connect ball P9, CLKREQ#, to the clock driver responsible for generating the PCIe* clock.	**82573L only:** This signal may be left unconnected if functionality is not desired but functionality must also be disabled in the NVM.		
	Ensure that ball C6, AUX_PRESENT (AUX_PWR for the 82573L), is pulled-up to the 3.3V standby power supply if the LAN Controller is powered from standby supplies. This signal should be pulled down if auxiliary power is not used.			
Clock Source	Use 25 MHz 30 ppm accuracy @ 25 °C clock source. Avoid components that introduce jitter.	Parallel resonant crystals are preferred. A clock oscillator can be used if testability rules require turning off the clock. If an oscillator is used, consider a series termination resistor of 22-33 Ω. Avoid PLL clock buffers.		
	Connect two 22 pF load capacitors to the crystal.	Capacitance affects accuracy of the frequency. Must be matched to crystal specifications, including estimated trace capacitance in calculation.		

EEPROM and FLASH Memory	Use 0.1 μF decoupling capacitor	Applies to EEPROM or FLASH devices.		
	Connect WP# and HOLD# signals to VCC through a 3.3 KΩ resistor	Applies to EEPROM or FLASH devices.		
	For shared Flash configuration, connect ball D3 NVM_SHARED to ground through a 3.3 KΩ resistor			
	If SPI Flash is used, connect ball A6 NVM_TYPE to ground through a 3.3 KΩ resistor			
	To disable SPI NVM protection, install a jumper to connect ball A5 NVM_PROT to ground			
	Connect ball B4 NVM_REQ to SPI_ARB on the ICH. This signal should be unconnected for dedicated LAN Flash configuration.	If both shared and dedicated configuration options are available please use a 0 Ω stuffing option for this signal.		
	Check EEPROM connections to NVM_CS#, NVM_SK, NVM_SI, NVM_SO			
	For dedicated LAN Flash: - Connect NVM_CS# to CS# on the Flash device - Connect NVM_SK through a 47Ω resistor to SCK on the Flash device and through a 8.2 - 10 KΩ resistor to ground - Connect NVM_SI through a 47Ω resistor to SI on the Flash device - Connect NVM_SO through a 47Ω resistor to SO on the Flash device	The 47Ω resistors should be placed closest to the outputs. A value other than 47Ω may be optimal depending on board characteristics. A simulation should be done if a different value is used.		
	For shared LAN Flash: - Connect NVM_CS# to ICH_SPI_CS and CS# on the Flash device - Connect NVM_SK to ICH_SPI_SCK and through a 47Ω resistor to SCK on the Flash device and through a 8.2-10kΩ resistor to ground - Connect NVM_SI to ICH_SPI_MOSI and through a 47Ω resistor to SI on the Flash device - Connect NVM_SO to ICH_SPI_MISO and through a 47Ω resistor to SO on the Flash device	The 47 Ω resistors should be placed closest to the outputs. A value other than 47Ω may be optimal depending on board characteristics. Please simulate if a different value is used.		
	If both shared and non-shared options are to be made available, please use 0 Ω resistors to minimize the stubs seen on the NVM lines	The reference schematics and the ICH7 layout guidelines can be consulted for further details.		
SMBus	**82573L only:** The SMBus interface is not functional for 82573L. Please leave unconnected.	**82573L only:** If these pins are connected to the SMBus it will not affect normal operation of the SMB but the 82573L will not been seen on the bus.		
	82573E/V only: If SMBus is not used, connect pull-up resistors to SMB_CLK, SMB_DATA, and SMB_ALRT#	**82573E/V only:** 3.3 KΩ pull-ups are reasonable values		
	82573E/V only: If SMBus is used, there should be pull-up resistors on SMB_DATA, SMB_ALRT# and SMB_CLK somewhere on the board	**82573E/V only:** SMBus signals are open-drain.		
	82573E/V only: For ASF and Intel® AMT applications with SMBus, connect ball N11 SMB_ALRT#/ASF_PWRGOOD to the system PWR_GOOD signal or to Vcc through a 3.3 KΩ pull-up resistor	**82573E/V only:** Use 3.3V, not 3.3V AUX. Alternatively, ball N11 can be configured as an SMB_ALRT# output		

	82573E/V only: Connect ball N11 SMB_ALRT#/ASF_PWRGOOD to SMB_INT for certain management modes	**82573E/V only:** The design guide provides further details for management modes.		
Transmit and Receive Differential Pairs	For 10/100/1000 Base-T applications, the 82573 controller uses pairs of 49.9 Ω termination resistors with 0.1 μF capacitors attached between center nodes and ground	This applies to all four differential pairs of each port.		
Magnetics Module (10/100/1000 Base-T applications)	If applicable, use integrated magnetics modules/RJ-45 connectors to minimize space requirements	Multivendor pin compatibility is possible. The design guide provides further details on recommended models and manufacturers.		
	Qualify magnetics module carefully for Return Loss, Insertion Loss, Open Circuit Inductance, Common Mode Rejection, and Crosstalk Isolation	Magnetics module is critical to passing IEEE PHY conformance tests and EMI test		
	Supply 2.5V to the transformer center taps and use 0.1μF bypass capacitors	2.5V biases the controller's output buffers. Magnetics with four center tap pins may have better characteristics than those with 1-2 center tap pins. Capacitors with low ESR should be used.		
Discrete Magnetics Module/RJ-45 Connector Option (10/100/1000 Base-T applications)	Bob Smith termination: use 4 x 75 Ω resistors for cable-side center taps and unused pins.	Terminate pair-to-pair common mode impedance of the CAT5 cable.		
	Bob Smith termination: use an EFT capacitor attached to the termination plane. Suggested values are 1500 pF/2 KV or 1000 pF/3 KV	A minimum of 50 mil spacing from capacitor to traces and components should be maintained.		
	Connect signal pairs correctly to RJ-45 connector.			
Power Supply and Signal Ground	Connect external PNP transistors to the regulator control CTRL_12 and CTRL_25 outputs to supply 1.2V and 2.5V, respectively. The connections and transistor parameters are critical.	Alternatively, provide external regulators to generate these voltages. If the internal voltage regulator control circuit is not used, the CTRL pins may be left unconnected.		
	Ball B5 EN2.5REG should be pulled up to enable the on-die 2.5V regulator or pulled down to disable the on-die regulator.			
	Place a 1Ω 0.5 W 1% resistor at the emitter of the PNP transistor for the 1.2V regulator circuit to drop some of the voltage. Two 2.0 Ω, 1%, 0.25 W resistors or any combination that yields 1.0 Ω, 0.5 W may also be used.			
	Ensure that there is adequate capacitance on the PNPs.	Please check the reference schematic. **82573L only:** Intel recommends using 20 μF of capacitance at the emitter of each PNP for the 82573L. **82573E/V only:** Intel recommends using 40 μF of capacitance at the emitter of each PNP.		
	82573E/V only: Place a 1 Ω resistor in series with a 10 μF ceramic capacitor at the collector of each PNP.	**82573E/V only:** Alternatively, a 10 μF tantalum capacitor may be used in place of the RC combination.		
	Provide a 3.3V supply. Use auxiliary power supplies.	Auxiliary power is necessary to support wake up from power down states.		

	Design with power supplies that start up properly.	A good guideline is that all voltages should ramp to within their control bands in 20 ms or less. It is desirable that voltages ramp in sequence (3.3V ramps first, 2.5V ramps second, 1.2V ramps last) and that the voltage rise be monotonic. The minimum rise time on the 3.3V power is 100 μs.		
	Use decoupling and bulk capacitors generously.	Use approximately 12 bypass capacitors for the Ethernet silicon. Add approximately 20-30 μF of bulk capacitance per voltage rail, typically using 10 μF capacitors. If power is distributed on traces, bulk capacitors should be used at both ends. If power is distributed on cards, bulk capacitors should be used at the connector.		
	If the 1.2V and 2.5V rails are externally supplied (the 82573 has no control), please ensure the following connections: - IREG2.5_IN (balls A2 and A3) should be tied to the 3.3V rail - VCC2.5_OUT (balls B1 and B2) should be connected to the 2.5V rail. Alternatively, it could be left floating. - CTRL_1.2 (ball P3) should be tied to ground through a 3.3 KW resistor. Alternatively, it could be left floating. - CTRL_2.5 (ball A4) should be tied to ground through a 3.3 KW resistor. Alternatively, it could be left floating. - EN2.5REG (ball B5) should be pulled down through a 3.3 KW resistor	Pull-down resistors do not need to be exactly 3.3kΩ; however, they must be greater than 1kΩ.		
Chassis Ground (10/100/1000 Base-T applications)	If possible, provide a separate chassis ground to connect the shroud of the RJ-45 connector and to terminate the line side of the magnetics module.	This design improves EMI behavior.		
	Place pads for approximately 4-6 "stitching" capacitors to bridge the gap from chassis ground to signal ground.	Typical values range from 0.1μF to 4.7μF. The correct value should be determined experimentally.		
LED Circuits	Basic recommendation is a single green LED for Activity and a dual (bi-color) LED for Speed. Many other configurations are possible. LEDs are configurable through the NVM.	Two LED configuration is compatible with integrated magnetics modules. For the Link/Activity LED, connect the anode to the LED1# pin and the cathode to VCC. For the bi-color speed LED pair, have the LED2# signal drive one end. The other end should be connected to LED0#.		
	Connect LEDs to 3.3V as indicated in reference schematics.	Use 3.3V AUX for designs supporting wake-up. Consider adding one or two filtering capacitors per LED for extremely noisy situations. Suggested starting value is 470 pF.		
	Add current limiting resistors to LED paths.	Typical current limiting resistors are 250 to 330 Ω when using a 3.3V supply. Current limiting resistors are typically included with integrated magnetics modules.		
Mfg Test	82573 controller allows a JTAG Test Access Port.	Connect these signals to the ICH if using system level JTAG		