82573/82562 Dual Footprint Design Guide

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Contents

Figures

Tables

Revision History

Date	Revision	Description
2.7	Oct 2009	Added crystal manufacturer information.
2.6	Dec 2007	Updated Analog Front End reference schematic (sheet 6).
2.5	Sept 2007	Updated section 3.3.2 (item number 3).
2.4	May 2007	Updated Table 21. Under "LED Circuits" in the "Remarks" column, changed anode to cathode and cathode to anode.
2.3	Jan 2007	Added magnetics model numbers to Tables 4 and 5.
2.2	Oct 2006	Major edit all sections. Updated EEPROM/Flash Configuration Size table. Updated Compatible Flash Parts table. Updated 82573L ball out definitions. Updated figure title for Figure 13 (removed "non-shared". Removed "or greater" from items 4 and 5 in section 3.3.2
2.1	June 2006	Removed all references to Dev_OFF and replaced with DEVICE_OFF, changed the Intel logo and used the new template style.
2.0	Sept 2005	Integrated information for the 82573E into this document, *82573/82562 Dual Footprint Design Guide.*
1.6	July 2005	Updated DEVICE_OFF# (ball L7) to indicate that an internal pull-up resistor does not exist.
1.5	July 2005	Initial release.

1.0 Introduction

Note: **Product features and specifications are subject to change without notice. Verify with your local Intel sales office that you have the latest information before finalizing a design.**

The Intel® 945/Intel® I/O Control Hub 7 (ICH7) 82801GB platform supports several footprint compatible Ethernet options depending upon the target application. The term “footprint compatible” means the silicon devices are all manufactured in a 15 mm by 15 mm, 196 Thin and Fine Ball Grid Array (TF-BGA) package, with the same ball pattern. Many of the critical signal pin locations are identical, allowing designers to create a single LAN on Motherboard (LOM) design that accommodates all devices. This is a flexible, cost-effective, multipurpose design technique that maximizes value while meeting performance requirements.

Note: Since some of the signal pins differ in usage, the term “pin compatible” is not applicable.

Available LAN components with the same footprint include the Intel® 82573E, 82573V and 82573L Gigabit Ethernet Controllers and Intel® 82562EZ, 82562EX, 82562GZ and 82562GX Platform LAN Connect (PLC) components. (For purposes of this document, the 82573E, 82573V and the 82573L will be referred to as the 82573; and the 82562EZ, 82562EX, 82562GZ and 82562GX will be referred to as the 82562 unless otherwise noted. Specific device data can be referenced in their respective datasheets for feature differences.) ICHx refers to ICH6 and ICH7 components.

The requirements for connection speed and manageability determine which LAN components should be used on a specific platform. As these requirements change, footprint compatibility make it possible to refocus the platform without the need for a motherboard redesign.

Table 1. LAN Component Connections/Features

LAN Component	Interface	Connection	Features
Intel® 82573E	PCI Express* (PCIe*)	GbE (1000BASE-T) with manageability	GbE, Intel® Active Management Technology (Intel® AMT), ASF 2.0 alerting
Intel® 82573V	PCIe*	GbE (1000BASE-T) with manageability	GbE, ASF 2.0 alerting
Intel® 82573L	PCIe*	GbE (1000BASE-T)	GbE, no manageability
Intel® 82562EX/GX (196 BGA)	LCI	10/100 Mb/s Ethernet with manageability	Ethernet 10/100 Mb/s connection, ASF 1.0 alerting
Intel® 82562EZ/GZ (196 BGA)	LCI	Basic 10/100 Mb/s Ethernet	Ethernet 10/100 Mb/s connection

1.1 Scope

This document contains Ethernet design guidelines applicable to LOM designs based on the Intel® 945/ICH7 82801GB chipset. The document identifies similarities and differences between the 82562 Platform LAN Connect device and the 82573 controller.

- Section 2.0 - describes the port interfaces specific to each device.
- Section 3.0 - explains requirements to connect an Ethernet device.
- Section 4.0 - describes board layout techniques applicable to these devices.
- Section 5.0 - describes the Flash interface applicable to these devices.
- Section 6.0 - describes selection criteria for crystal devices.

This document assumes the reader is acquainted with high-speed design and board layout techniques. Please see the reference document list for additional design information.

1.2 Reference Documents

- Intel® 82573 Family of GbE Controllers Datasheet. Intel Corporation.
- Intel® 82562GX 10/100 Mb/s Platform LAN Connect (PLC) Networking Silicon Datasheet. Intel Corporation.
- Intel® 82562GZ 10/100 Mb/s Platform LAN Connect (PLC) Networking Silicon Datasheet. Intel Corporation.
- 82573E Intel® Active Management Technology (Intel® AMT) Design Guide. Intel Corporation.
- Intel® 82573 NVM Map and Programming Information Guide. Intel Corporation.
- Intel® ICHx Integrated LAN Controller Function Disable and Power Control. Intel Corporation.
- Intel® Ethernet Controllers Timing Device Selection Guide. Intel Corporation.
- PCI Express Specification, Revision 1.0a. PCI Special Interest Group.
- PCI Bus Power Management Interface Specification, Revision 1.1. PCI Special Interest Group.
- IEEE Standard 802.3, 2000 Edition. Institute of Electrical and Electronics Engineers (IEEE).[1]

Note: Intel documentation is subject to frequent revision. Verify with your local Intel sales office that you have the latest information before finalizing a design.

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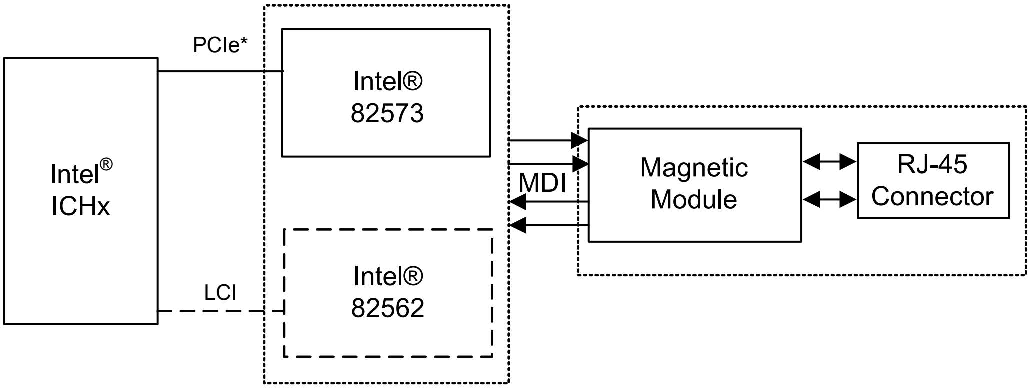
[1] This document incorporates various IEEE standards previously published separately.

2.0 System Data Port Interfaces

The 82562 PLC device and the 82573 controller use different system interfaces, as illustrated below in Figure 1.

Figure 1. ICHx Platform LAN Connect Sections



Note: Further details can be found in the reference design schematics (see Section 9.0).

2.1 LCI Connection to the 82562 Platform LAN Connect Device

The 82562 PLC device uses the LAN Connect Interface (LCI) to connect to the ICHx. LCI is a point-to-point interface optimized to support one device.

Line termination mechanisms are not specified for the LAN Connect Interface. Slew rate controlled output buffers achieve acceptable signal integrity by controlling signal reflection, undershoot and ringing.

Further details on connecting the LCI between the 82562 PLC device and ICHx can be obtained in the Intel® 945/ICH7 82801GB chipset design guide.

2.2 PCIe* Port Connection to the 82573 Device

PCIe* is a dual simplex point-to-point serial differential low-voltage interconnect. The signaling bit rate is 2.5 Gb/s per lane per direction. Each port consists of a group of transmitters and receivers located on the same chip. Each lane consists of a transmitter and a receiver pair. A link between the ports of two devices is a collection of lanes. The link between the 82573 and the ICHx device is a single lane.

Each signal is 8b/10b encoded with an embedded clock.

PCIe* topology consists of a transmitter (Tx) located on one device connected through a differential pair connected to the receiver (Rx) on a second device. The 82573 controller can be located on the motherboard or on an add-in card using a connector specified by PCIe*.

The lane is AC coupled between its corresponding transmitter and receiver. The AC coupling capacitor is located on the board close to transmitter side. Its recommended value is 0.1 μF. Each end of the link is terminated on the die into nominal 100 Ω differential DC impedance. Board termination is not required.

For more information on PCIe*, refer to the *PCI Express* Base Specification, Revision 1.0a* and *PCI Express* Card Electromechanical Specification, Revision 1.0a.*

Note: In manufacturing, vias are required for testing and troubleshooting purposes. The via size should be a 17-mil (±2 mils for manufacturing variance) Finished Hole Size (FHS).

2.2.1 PCIe* Reference Clock

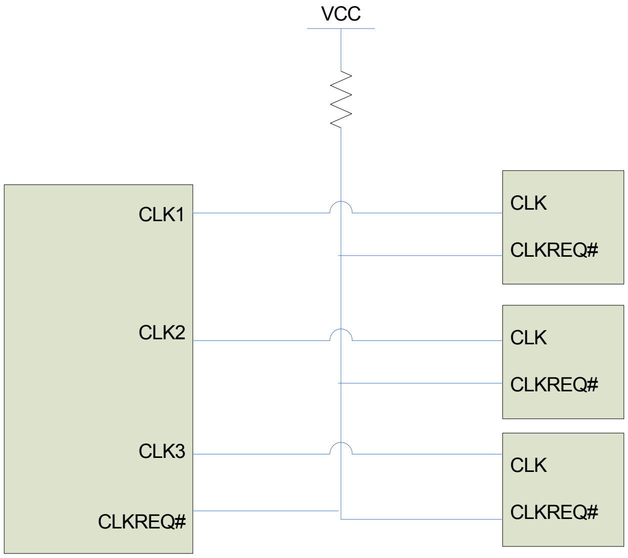
The 82573 Ethernet controller uses a 100 MHz differential reference clock, denoted PE_CLKp and PE_CLKn. This signal is typically generated on the system board and routed to the PCIe* port. For add-in cards, the clock is furnished at the PCIe* connector.

The frequency tolerance for the PCIe* reference clock is +/- 300 ppm.

2.2.2 Clock Request Signal (82573L)

The 82573L supports Clock Request. The Clock Request (CLKREQ#) signal is located at ball P9 of the 82573L. When it is sampled high, this open-drain signal alerts the system that the 82573L does not need the PCIe* differential reference clock. During normal operation, the 82573L keeps CLKREQ# asserted (low) and the system supplies this clock to the device on the PE_CLKp and PE_CLKn signals. The 82573L deasserts CLKREQ# (high) when it is in an electrical idle state (L1 or L2) and the system might choose to continue supplying the reference clock or gate it. The CLKREQ# signal should be connected to the clock driver supplying the 82573L PCIe* clock. If other devices use the same CLKREQ# signal, a pull-up resistor should be used to ensure that no device pulls this signal low when it is powered off (see Figure 2).

Figure 2. Clock Request Signal Implementation (82573L)



To enable clock management, bit 2 of word 0Fh must be set to 1b. (The *Intel® 82573 NVM Map and Programming Information Guide* provides further details.)

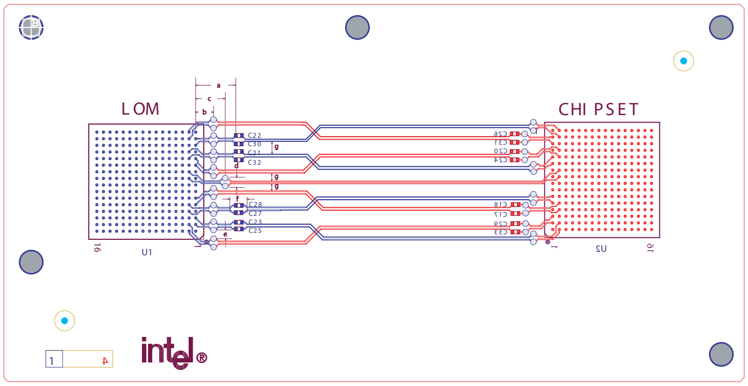
2.2.3 Other PCIe* Signals

The 82573 device also implements other signals required by the PCIe* specification. The Ethernet controller signals power management events to the system using the PE_WAKE# signal, which operates very similarly to the familiar PCI PME# signal. Finally, there is a PE_RST# signal that serves as the familiar reset function for the 82573 controller.

2.2.4 PCIe* Routing Example

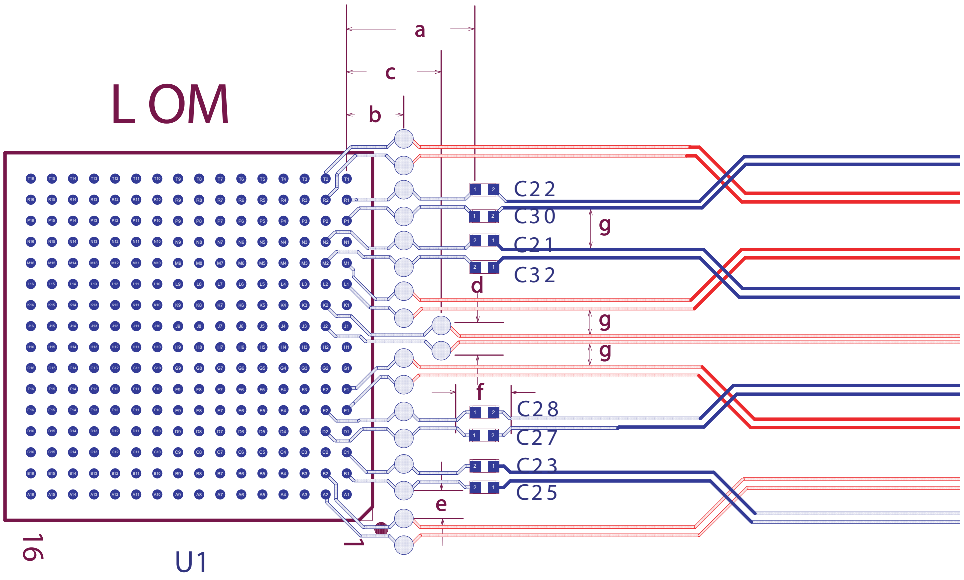
This section provides an example for routing PCIe* signals. The diagrams provided are examples only and are not specifically for the 82573.

Figure 3. PCIe* Routing Example



Dimension	Min	Max	Typical	Description
	(mils)	(mils)	(mils)	
a		500	275	Distance from BGA ball to capacitor pad
b		250	200	Trace length from BGA ball to center of 17-19 mil via on PCI-E data traces
c		1000	180	Trace length from BGA ball to center of 17-19 mil via on PCI-E clock traces
d	50	50	50	Pitch (Center-to-Center) of 17-19 mil FHS vias within a pair
e	50			Pitch (Center-to-Center) of 17-19 mil FHS vias outside the differential pair
f		50		Length of differential pair convergence from optimum intra pair conductor seperation
g	5 x h		20	Pair-to-metal differential pair seperation

FHS = Finished Hole size
h = height of this trace above the reference plane, typically the dialectric thickness



Note: The 82573 is a x1, and the drawing is for a x4 design and is shown only for reference.
Note: The second drawing is an enlargement of a section of the first drawing.

3.0 Ethernet Component Design Guidelines

These sections provide recommendations for selecting components and connecting special pins. The main design elements are the 82562 Platform LAN Connect device or the 82573, an integrated magnetics module with RJ-45 connector, and a clock source.

3.1 General Design Considerations for Ethernet Controllers

These recommendations apply to all designs, Fast Ethernet (10/100 Mb/s) or GbE (10/100/1000 Mb/s).

Follow good engineering practices with respect to unused inputs by terminating them with pull-up or pull-down resistors, unless the datasheet, design guide or reference schematic indicates otherwise. Pull-up or pull-down resistors must not be attached to any balls identified as reserved. These devices might have special test modes that could be entered unintentionally.

3.1.1 Clock Source

All designs require a 25 MHz clock source. The 82562 PLC device and the 82573 use the 25 MHz source to generate clocks up to 125 MHz for the PHY circuits. For optimum results with lowest cost, connect a 25 MHz parallel resonant crystal and appropriate load capacitors at the XTAL1 and XTAL2 leads. The frequency tolerance of the timing device should be 30 ppm or better. Refer to the *Intel Ethernet Controllers Timing Device Selection Guide* for more information on choosing crystals.

There are three steps to crystal qualification:

1. Verify that the vendor’s published specifications in the component datasheet meet the required conditions for frequency, frequency tolerance, temperature, oscillation mode and load capacitance.
2. Independently measure the component’s electrical parameters in real systems. Measure frequency at a test output to avoid test probe loading effects at XTAL2. Check that the measured behavior is consistent from sample to sample and that it meets the published specifications. For crystals, it is also important to examine startup behavior while varying system voltage and temperature.
3. Perform physical layer conformance testing and EMC (FCC and EN) testing in real systems.

Note: Section 6.0 provides guidelines for crystal selection.

3.1.2 Integrated Magnetics Module

The magnetics module has a critical effect on overall IEEE and emissions conformance. The device should meet the performance required for a design with reasonable margin to allow for manufacturing variation. Occasionally, components that meet basic specifications can cause the system to fail IEEE testing because of interactions with other components or the printed circuit board itself. Carefully qualifying new magnetics modules can help prevent this type of problem.

The steps involved in magnetics module qualification are similar to those for oscillator qualification:

1. Verify that the vendor's published specifications in the component datasheet meet the required IEEE specifications.
2. Independently measure the component's electrical parameters on the test bench, checking samples from multiple lots. Check that the measured behavior is consistent from sample to sample as well as meeting the published specifications.
3. Perform physical layer conformance testing and EMC (FCC and EN) testing in real systems. Vary temperature and voltage while performing system level tests.

Magnetics modules for 1000BASE-T Ethernet are similar to those designed solely for 10/100 Mb/s, except that there are four differential signal pairs instead of two. Section 3.3.2 contains parametric guidelines.

3.2 Designing with the 82562 Platform LAN Connect Device

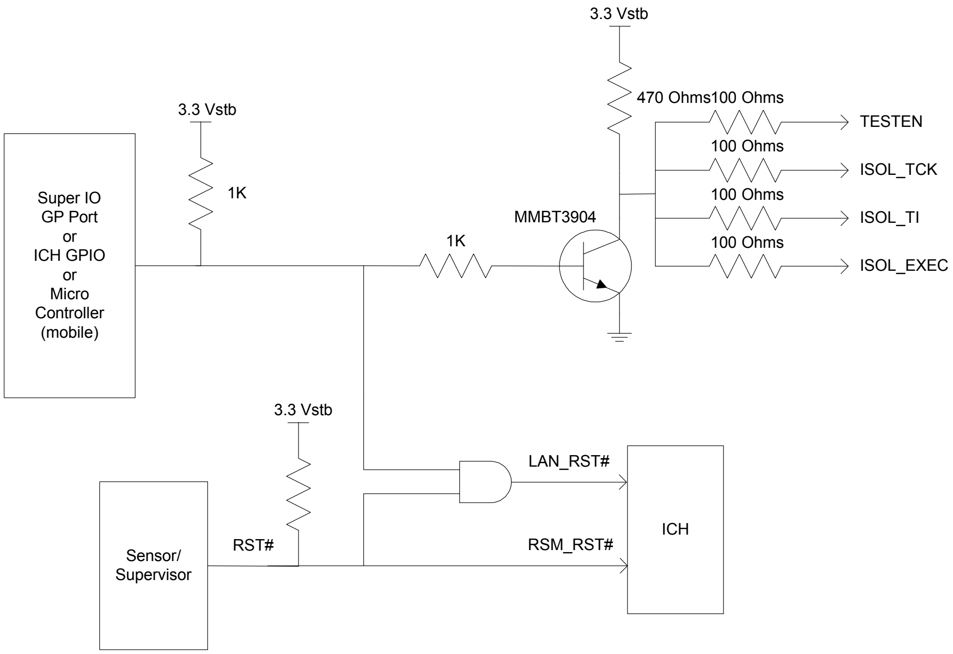
This section provides design guidelines specific to the PLC device.

3.2.1 82562EZ/EX PLC Device LAN Disable Guidelines

Note: The ICHx Integrated LAN Controller resides on the ICHx VccSus3_3 and VccSus1_8 power wells. These are typically referred to as auxiliary (aux) or standby supplies at the platform level.

The ICHx Integrated LAN_RST# is the ICHx resume-well input. It can be held low indefinitely to keep the ICHx in a reset state. The LAN reset (LAN_RST#) signal must not be de-asserted sooner than 10 ms after the resume power supply reaches its nominal voltage. This ensures that the ICHx is initialized. Figure 4 shows a possible solution for ICHx LAN disable.

Figure 4. 82562EZ/EX LAN Disable Circuitry



Notes:

1. The 100 Ω resistors for the test mode signals are required for the eXclusive OR (XOR) Tree and isolate mode.
2. The PLC device should be connected to a super I/O pin that retains its value during PCIe* reset and is driven from the resume well and defaults to a value of one on power up.

3.2.2 Serial EEPROM for 82562 PLC Implementations

The serial EEPROM for LAN implementations based on 82562 PLC devices connects to the ICHx. Depending on the size of the EEPROM, the 82562 PLC might or might not support legacy manageability. Table 2 and Table 3 list the EEPROM map for the PLC device. Details for the EEPROM can be obtained in the *I/O Control Hub 4, 5, and 6 EEPROM Map and Programming Information Guide*.

Table 2. 82562 PLC Memory Layout (128-byte EEPROM)

00h **3Fh**	Hardware/Software Reserved Area

Note: No manageability provided.

Table 3. 82562 PLC Memory Layout (512-byte EEPROM)

00h **3Fh**	HW/SW Reserved Area
40h **FFh**	ASF 1.0 Legacy Manageability

Note: Legacy manageability only.

3.2.3 Magnetics Modules for the 82562 PLC Device

Carefully select a 5-core magnetics module for your design. Table 4 lists suggested integrated magnetics modules for use with the 82562 PLC. These modules also contain integrated USB jacks.

Note: These components are pin-compatible with the magnetics modules shown in Table 5 for the 82573.

Table 4. 82562 PLC Integrated Magnetics Modules[1]

Manufacturer	Discrete Magnetics Module Part Number	Integrated Magnetics Module Part Number
Pulse	H1138 - MDI only H1338 - MDI and MDI-X only	JW0A1P01R-E JW0A1P01R - Magjack
Stewart Connector Systems	Check with manufacturer for availability.	SI70027
Foxconn	Check with manufacturer for availability.	UB11123-J51

1. These modules have been used successfully in past designs, however no particular product is recommended.

3.2.4 Power Supplies for 82562 PLC Implementations

The 82562 PLC uses a single 3.3V power supply. The 3.3V supply must provide approximately 90 mA current for full speed operation. Standby power must be furnished in order to allow wake up from a power down.

3.2.5 82562 PLC Device Test Capability

The device contains an eXclusive OR (XOR) test tree mechanism for simple board tests. Details of the XOR tree operation are available from your Intel representative.

3.3 Designing with the 82573

This section provides design guidelines specific to the 82573.

3.3.1 LAN Disable for 82573

The DEVICE_OFF# signal can be used for disabling the device from system BIOS. The DEVICE_OFF# input is completely asynchronous. It can be connected to a Super I/O pin that retains its value during the PCIe* reset, is driven from a resume well and defaults to a one on power up. The DEVICE_OFF# pin does not have an internal pull-up resistor, therefore an external pull-up resistor is recommended for normal operation.

3.3.2 Integrated Magnetics Module for 1000BASE-T

Magnetics modules for 1000BASE-T Ethernet are similar to those designed solely for 10/100 Mb/s, except that there are four differential signal pairs instead of two. The following guidelines are listed to help verify specific electrical parameters:

1. Verify that the rated return loss is 18 dB or greater from 2 MHz through 30 MHz for 100BASE-TX.
2. Verify that the rated return loss is 12 dB or greater at 80 MHz for 100BASE-TX. (The specification requires greater than or equal to 10 dB.)

3. Verify that the rated return loss is 10 dB (2 dB margin) at 100 MHz for 1000BASE-TX on the platform at 100 MHz, measured at the RJ-45 and into 85 Ω, 100 Ω, and 115 Ω references.
4. Verify that the insertion loss is less than 1.0 dB at 100 KHz through 80 MHz for 100BASE-TX.
5. Verify that the insertion loss is less than 1.4 dB at 100 KHz through 100 MHz for 1000 BASE-T.
6. Verify at least 30 dB of crosstalk isolation between adjacent channels (through 150 MHz).
7. Verify high voltage isolation to 1500 Vrms.
8. Transmitter OCL should be greater than or equal to 350 µH with 8 mA DC bias.

Table 5 lists suggested magnetics modules for use with the 82573. These modules also contain integrated USB jacks. A good quality Gigabit Ethernet magnetics module can also be used with the 82562 Platform LAN Connect device.

Table 5. 82573 Magnetics Modules[1]

Manufacturer	Discrete Magnetics Module Part Number	Integrated Magnetics Module Part Number
Pulse Engineering	H5019D (low profile) H5007	JW0A2P019D - Magjack
Bel Fuse	S558-5999–P3	Check with manufacturer for availability.

1. These modules have been used successfully in past designs, however no particular product is recommended.

Note: These components are pin-compatible with the magnetics modules shown in Table 4 for the 82562 PLC device.

3.3.3 82573 LEDs

The 82573 controller contains three programmable LED outputs. The LEDs are independently programmable to provide particular speed, link, activity and event status. The behavior of the LEDs is controlled by bits read from the Non-Volatile Memory (NVM). 82573-based designs need to ensure that the NVM is programmed correctly.

3.3.4 NVM Interface for the 82573

The 82573 provides a single Serial Peripheral Interface (SPI) that only supports SPI EEPROMs or SPI Flash devices. The 82573 is configured for either an EEPROM or Flash device based on the setting of the NVM_TYPE input pin. If the NVM_TYPE pin is pulled high, an SPI EEPROM is connected. If the NVM_TYPE pin is pulled low, an SPI Flash connection is enabled. In most cases a single physical footprint on the board can accommodate either a SPI Flash or SPI EEPROM device, which can be populated with a SPI Flash or SPI EEPROM device depending on the desired configuration. Flash is required for Intel® AMT support.

The 82573 enables the SPI Flash to be shared for access with the ICH7. In this case, the 82573 SPI Flash can be used as the single consolidated system Flash device. While the ICH7 device owns the Flash, the 82573 can request access to the Flash through the ICH7 SPI arbitration pin (NVM_REQ signal on the 82573). In this instance, the Flash contains both the firmware code used for network management and the BIOS code used by the platform to power up the system. The NVM_SHARED input pin configures the 82573 for operation in this mode. When the NVM_SHARED input pin is pulled low, the SPI Flash has shared access with the ICH.

The SPI bus is a high speed bus and requires careful design consideration. The routing recommendations are provided in Section 5.1. Since this is a high speed bus, the recommendations should be followed if possible. If there are any deviations, it is strongly recommended that they are simulated to ensure design compliance.

Table 6. EEPROM/Flash Configuration Size

Configuration	Minimum NVM Size	Memory Family
ASF or APT Manageability	64 Kb	SPI EEPROM
No Manageability (Intel® AMT, ASF or APT)	1 Kb	SPI EEPROM
Shared Flash with Intel® AMT (82573E only)	8 Mb to 16 Mb total The minimum requirement for Intel® AMT is 4 Mb	SPI Flash
Shared Flash without Intel® AMT	8 Mb to 16 Mb total mobile 4 Mb to 16 Mb total for desktop 128 Kb (minimum) is reserved for the LAN image	SPI Flash
Dedicated Flash with Intel® AMT (82573E only)	4 Mb	SPI Flash
Dedicated Flash without Intel® AMT	128 Kb	SPI Flash

Table 7. Compatible EEPROM Parts

Vendor[1]	1 Kbit
Atmel*	AT25010N-10SI-2.7
STM*	95010WMN6
Catalyst*	CAT25010S

1. The vendors listed here manufacture EEPROM parts that have been used successfully in previous designs.

Table 8. Compatible Flash Parts

Vendor	4 Mb	8 Mb	16 Mb
ST Micro*	25PE40[1], M45PE40[2]	25PE80[1], M45PE80[2]	
Chingis*	PM25LV040		
SST*	25VF040B 25LF040A	25VF080B	25VF016B

1. ST Micro* parts can only be used with Intel® non-AMT Systems.
2. These parts have been fully tested but are not pin compatible with the other Flash components listed in this table.

Note: Additional 8 Mb and 16 Mb Flash parts will become available in early 2007 and will be validated for use with the 82573 GbE controller. Consult your local Intel representative for availability information.

3.3.5 Power Supplies for the 82573 Device

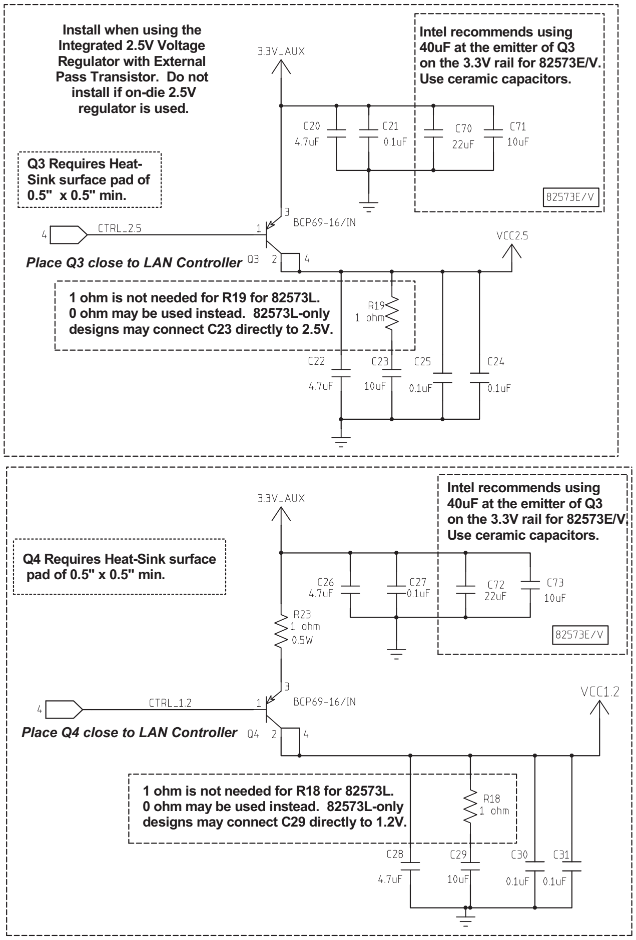
The 82573 controller requires three power supplies (3.3V, 2.5V, and 1.2V).

A central power supply can provide all the required voltage sources or the power can be derived and regulated locally by the Ethernet control circuitry. All voltage sources must remain present during power down in order to use the 82573 Ethernet controller's LAN wake up capability.

Instead of using external regulators to supply 2.5V and 1.2V, a designer can use power transistors in conjunction with on-chip regulation circuitry. The 82573 also provides the option to use the on-die voltage regulator to supply 2.5V. This option does not require the external pass transistor for 2.5V regulation. Circuit details are shown in Figure 5.

The 82573 controller has a LAN_PWR_GOOD input signal. This signal serves as an indicator that all power rails to the LAN device are stable and as an external reset. In a situation where a central power supply furnishes all the voltage sources, LAN_PWR_GOOD can possibly be tied to the POWER_GOOD output of the power supply. Designs that generate some of the voltages locally can connect LAN_PWR_GOOD to a power monitor chip. The system must drive LAN_PWR_GOOD inactive for a minimum of 50 ms, preferably 80 ms, after all three LAN power rails are stable.

Figure 5. 82573 2.5V and 1.2V LVR Schematic



Install when using the Integrated 2.5V Voltage Regulator with External Pass Transistor. Do not install if on-die 2.5V regulator is used.

Intel recommends using 40uF at the emitter of Q3 on the 3.3V rail for 82573E/V. Use ceramic capacitors.

Q3 Requires Heat-Sink surface pad of 0.5" x 0.5" min.

Place Q3 close to LAN Controller

1 ohm is not needed for R19 for 82573L. 0 ohm may be used instead. 82573L-only designs may connect C23 directly to 2.5V.

Q4 Requires Heat-Sink surface pad of 0.5" x 0.5" min.

Intel recommends using 40uF at the emitter of Q3 on the 3.3V rail for 82573E/V. Use ceramic capacitors.

Place Q4 close to LAN Controller

1 ohm is not needed for R18 for 82573L. 0 ohm may be used instead. 82573L-only designs may connect C29 directly to 1.2V.

The power sources should ramp up during a brief power-up interval (approximately 20 ms) with LAN_PWR_GOOD de-asserted. The 82573 controller must not be left in a prolonged state where some, but not all, voltages are applied. The 3.3V power source should be powered up prior to the 2.5V or 1.2V sources. The 2.5V and 1.2V supplies can be powered up simultaneously; otherwise, the 2.5V supply needs to power up before the 1.2V supply. At any time during power up, the supply voltages must be: 1.2V < 2.5V < 3.3V. In desktop systems based on ICH, LAN_PWR_GOOD is typically tied to the same signal that drives RSMRST# on the ICH.

3.3.6 82573 Controller Power Supply Filtering

Bypass capacitors, with values between 0.01 µF and 0.1 µF, are needed for each power rail. If possible, the capacitors should be placed close to the device and adjacent to power pads. Decoupling capacitors should connect to the power planes with short, thick traces of 15 mils (0.4 mm) or more and 14-mil (0.35 mm) vias. Bypass capacitance is required at the silicon.

Approximately 20 µF of bulk capacitance for each of the main 1.2V and 2.5V levels is recommended. The bulk capacitors should be placed as close as possible to the device power connections.

3.3.7 82573 Controller Power Management and Wake Up

The 82573 supports low power operation as defined in the PCI Bus Power Management Specification. There are two defined power states, D0 and D3. The D0 state provides full power operation and is divided into two sub-states: D0u (uninitialized) and D0a (active). The D3 state provides low power operation and is also divided into two sub-states: D3hot and D3cold.

To enter the low power state, the software device driver must stop data transmission and reception. Either the operating system or the software device driver must program the Power Management Control/Status Register (PMCSR) and the Wakeup Control Register (WUC). If wake up is desired, the appropriate wake up LAN address filters must also be set. The initial power management settings are specified by NVM bits.

When the 82573 transitions to either of the D3 low power states, the 1.2V, 2.5V, and 3.3V sources must continue to be supplied to the device. Otherwise, it will not be possible to use a wake up mechanism. The AUX_PRESENT signal is a logic input to the 82573 that denotes auxiliary power is available. If AUX_POWER is asserted, the 82573 device advertises that it supports wake up from a D3cold state.

The 82573 device supports both Advanced Power Management (APM) wake up and Advanced Configuration and Power Interface (ACPI) wake up. Note that APM wake up is also known as Wake on LAN (WoL).

Wake up uses the PE_WAKE# signal to wake the system up. PE_WAKE# is an active low signal typically connected to WAKE# on the ICH that goes active in response to receiving a Magic Packet*, a network wakeup packet, or link status change indication. PE_WAKE# remains asserted until it is disabled through the Power Management Control/Status Register.

3.3.8 Active State Power Management Support

The 82573L is capable of supporting Active State Power Management (ASPM) PCIe* power management.

In order to support ASPM, three items are required from the platform:

1. BIOS modifications for ASPM support. The ICH7 BIOS specification can be consulted for details on implementing ASPM specifically for the 82573.

2. EEPROM/Flash image that supports ASPM. A LAN image advertising ASPM support is required. The *82573 NVM Map and Programming Information Guide* can be consulted for details.
3. Updated LAN driver from Intel. ASPM cannot be enabled properly with a default operating system GbE driver.

3.3.9 82573 Device Test Capability

The 82573 contains a test access port conforming to the IEEE 1149.1a-1994 (JTAG) Boundary Scan specification. To use the test access port, connect these balls to pads accessible by your test equipment.

A Boundary Scan Definition Language (BSDL) file describing the 82573 device is available for use in your test environment. The 82573 also contains an eXclusive-OR (XOR) test tree mechanism for simple board tests. Details of the XOR tree operation are available from your Intel representative.

4.0 Ethernet Component Layout Guidelines

These sections provide recommendations for performing printed circuit board layouts. Good layout practices are essential to meet IEEE PHY conformance specifications and electromagnetic interference (EMI) regulatory requirements.

4.1 General Layout Considerations for Ethernet Controllers

Critical signal traces should be kept as short as possible to decrease the likelihood of being affected by high frequency noise from other signals, including noise carried on power and ground planes. Keeping the traces as short as possible can also reduce capacitive loading.

Since the transmission line medium extends onto the printed circuit board, special attention must be paid to layout and routing of the differential signal pairs.

Designing for GbE operation is very similar to designing for 10 Mb/s and 100 Mb/s. For the 82573, system level tests should be performed at all three speeds.

4.1.1 Guidelines for Component Placement

Component placement can affect signal quality, emissions, and component operating temperature. This section provides guidelines for component placement.

Careful component placement can:

- Decrease potential problems directly related to EMI, which could cause failure to meet applicable government test specifications.
- Simplify the task of routing traces. To some extent, component orientation affects the complexity of trace routing. The overall objective is to minimize turns and crossovers between traces.

Minimizing the amount of space needed for the Ethernet LAN interface is important because other interfaces compete for physical space on a motherboard near the connector. The Ethernet LAN circuits need to be as close as possible to the connector.

Figure 6. General Placement Distances

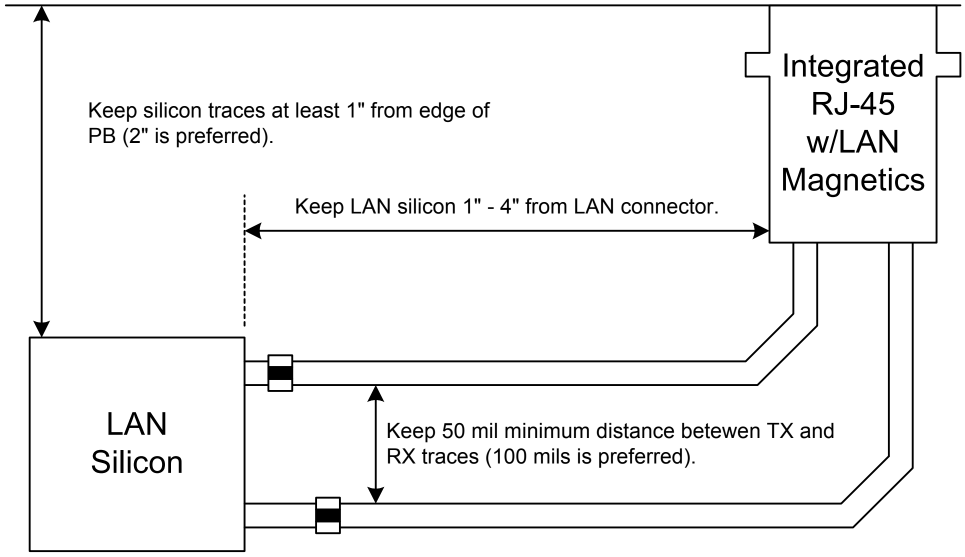


Figure 6 shows some basic placement distance guidelines. It shows two differential pairs, but it can be generalized for a GbE system with four analog pairs. The ideal placement for the Ethernet silicon would be approximately one inch behind the magnetics module.

While it is generally a good idea to minimize lengths and distances, Figure 6 also shows the need to keep the LAN silicon away from the board edge and the magnetics module for best EMI performance.

4.1.2 Crystals and Oscillators

Clock sources should not be placed near I/O ports or board edges. Radiation from these devices can be coupled onto the I/O ports or out of the system chassis. Crystals should also be kept away from the Ethernet magnetics module to prevent interference.

Place the crystal and load capacitors on the printed circuit boards as close to the Ethernet component as possible, within 0.75 inch. If an oscillator is used instead of a crystal, the clock signal should be connected with the shortest, most direct trace possible. Other potentially noisy traces should be kept away from the clock trace.

4.1.3 External Clock Oscillator

If an external oscillator is used to provide a clock to the 82573, the connection shown in Figure 7 must be used. The XTAL2 output signal of the 82573 must not be connected. The XTAL1 input signal receives the output of the oscillator directly. AC coupling is not recommended.

Figure 7. External Clock Oscillator Connectivity to the 82573

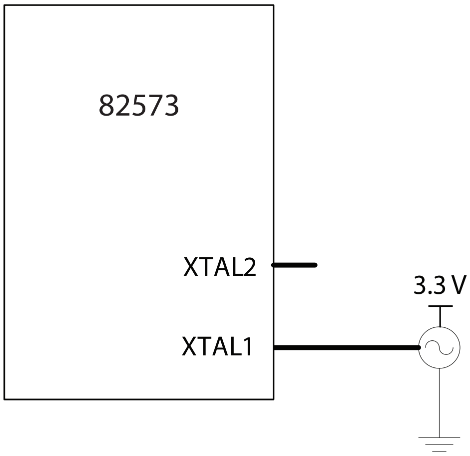


Table 9. Specification for External Clock Oscillator

Parameter Name	Symbol	Value	Conditions
Frequency	f_o	25.0 MHz	at 25 °C
Swing	V_{p-p}	3.3 ± 0.3 V	-
Frequency Tolerance	$\Delta f/f_o$	±30 ppm	0 °C to +70 °C
Operating Temperature	T_{opr}	0 °C to +70 °C	-
Aging	$\Delta f/f_o$	±5 ppm per year	-

4.1.4 Board Stack Up Recommendations

Printed circuit boards for these designs typically have four, six, eight, or more layers. Here is a description of a typical four-layer board stackup:

- Layer 1 is a signal layer. It can contain the differential analog pairs from the Ethernet device to the magnetics module.
- Layer 2 is a signal ground layer. Chassis ground can also be fabricated in Layer 2 under the connector side of the magnetics module.
- Layer 3 is used for power planes.
- Layer 4 is a signal layer. For GbE designs, it is common to route two of the differential pairs on this layer.

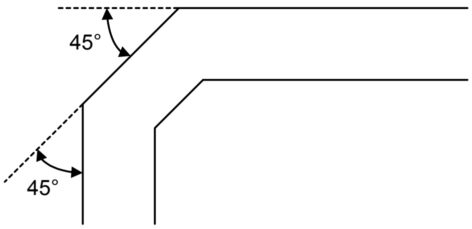
This board stack up configuration can be adjusted to conform to specific design rules.

4.1.5 Differential Pair Trace Routing

Trace routing considerations are important to minimize the effects of crosstalk and propagation delays on sections of the board where high-speed signals exist. Signal traces should be kept as short as possible to decrease interference from other signals, including those propagated through power and ground planes. The following suggestions should be observed to help optimize board performance:

- Maintain constant symmetry and spacing between the traces within a differential pair.
- Keep the signal trace lengths of a differential pair equal to each other.
- Keep the total length of each differential pair under four inches. Designs with differential traces longer than five inches are much more likely to have degraded receive Bit Error Rate (BER) performance, IEEE PHY conformance failures, and excessive EMI radiation.
- Do not route the transmit differential traces closer than 100 mils to the receive differential traces.
- Do not route any other signal traces both parallel to the differential traces and closer than 100 mils to the differential traces (300 mils is recommended).
- Keep maximum separation within differential pairs to 10 mils.
- For high-speed signals, keep the number of corners and vias to a minimum. If a 90° bend is required, it is recommended to use two 45° bends instead. (Figure 8)

Figure 8. Trace Routing



- Route traces away from board edges by a distance greater than the trace height above the ground plane. This enables the field around the trace to couple more easily to the ground plane rather than to adjacent wires or boards.
- Do not route traces and vias under crystals or oscillators. This prevents coupling to or from the clock. As a general rule, place traces from clocks and drives at a minimum distance from apertures by a distance that is greater than the largest aperture dimension.
- Ensure that the reference plane for the differential pairs is continuous and has low impedance. It is recommended that the reference plane is either ground or 1.2V (the voltage used by the PHY). This provides an adequate return path for high frequency noise currents.
- Do not route differential pairs over splits in the associated reference plane.
- Place differential termination components as close as possible to the LAN silicon.
- At most, use two vias per trace.

4.1.6 Signal Trace Geometry

The key factors in controlling trace EMI radiation are the trace length and the ratio of trace width to trace height above the ground plane. To minimize trace inductance, high-speed signals and signal layers that are close to a ground or power plane should be as short and wide as practical. Ideally, this trace width to height above the ground plane ratio is between 1:1 and 3:1. To maintain trace impedance, the width of the trace should be modified when changing from one board layer to another if the two layers are not equidistant from the power or ground plane.

Each pair of signals should have a differential impedance of 100 Ω. ±15%. If a particular tool cannot design differential traces, it is permissible to specify 55 Ω to 65 Ω single-ended traces as long as the spacing between the two traces is minimized. As an example, consider a differential trace pair on Layer 1 that is 8 mils (0.2 mm) wide and 2 mils (0.05 mm) thick, with a spacing of 8 mils (0.2 mm). If the fiberglass layer is 8 mils (0.2 mm) thick with a dielectric constant, E_R, of 4.7, the calculated single-ended impedance would be approximately 61 Ω and the calculated differential impedance would be approximately 100 Ω.

When performing a board layout, the CAD tool must not automatically route the differential pairs without intervention. In most cases, the differential pairs will have to be routed manually.

Note: Measuring trace impedance for layout designs targeting 100 Ω often results in lower actual impedance. Designers should verify actual trace impedance and adjust the layout accordingly. If the actual impedance is consistently low, a target of 105 Ω to 110 Ω should compensate for second order effects.

It is necessary to compensate for trace-to-trace edge coupling, which can lower the differential impedance by up to 10 Ω, when the traces within a pair are closer than 30 mils (edge-to-edge).

4.1.7 Trace Length and Symmetry

As indicated earlier, the overall length of differential pairs should be less than four inches measured from the Ethernet device to the magnetics.

The differential traces (within each pair) should be equal within 50 mils (1.25 mm) and as symmetrical as possible. Asymmetrical and unequal length traces in the differential pairs contribute to common mode noise. Common mode noise can degrade the receive circuit’s performance and contribute to radiated emissions.

4.1.8 Impedance Discontinuities

Impedance discontinuities cause unwanted signal reflections. Thus, vias (signal through holes) and other transmission line irregularities should be avoided. If vias must be used, a reasonable budget is two per differential trace. Unused pads and stub traces should also be avoided.

4.1.9 Reducing Circuit Inductance

Traces should be routed over a continuous ground plane with no interruptions. If there are vacant areas on a ground or power plane, the signal conductors should not cross the vacant area. This increases inductance and associated radiated noise levels. Noisy logic grounds should be separated from analog signal grounds to reduce coupling. Noisy logic grounds can also affect sensitive DC subsystems such as analog to digital conversion, operational amplifiers, etc. All ground vias should be connected to every ground plane; and similarly, every power via, to all power planes at equal potential. This helps reduce circuit inductance. Another recommendation is to physically locate grounds to minimize the loop area between a signal path and its return path. Rise and fall times should be as slow as possible since signals with fast rise and fall times contain many high frequency harmonics, which can radiate significantly. The most sensitive signal returns closest to the chassis ground should be connected together. This results in a smaller loop area and reduce the likelihood of crosstalk. The effect of different configurations on the amount of crosstalk can be studied using electronics modeling software.

4.1.10 Signal Isolation

To maintain best signal integrity, digital signals should be far away from the analog traces. A good rule to follow is no digital signal should be within 30 mils (7.5 mm) of the differential pairs. If digital signals on other board layers cannot be separated by a ground plane, they should be routed at right angles with respect to the differential pairs. If there is another LAN controller on the board, the differential pairs should be kept away from that circuit.

Some rules to follow for signal isolation:

- Separate and group signals by function on separate layers if possible. If possible, maintain a gap of 50 mils between all differential pairs (Ethernet) and other nets, but group associated differential pairs together.

Note: Over the length of the trace run, each differential pair should be at least 0.3 inches away from any parallel signal traces.

- Physically group together all components associated with one clock trace to reduce trace length and radiation.
- Isolate I/O signals from high-speed signals to minimize crosstalk, which can increase EMI emission and susceptibility to EMI from other signals.
- Avoid routing high-speed LAN traces near other high-frequency signals associated with a video controller, cache controller, processor, or other similar devices.

4.1.11 Power and Ground Planes

Good grounding requires minimizing inductance levels in the interconnections and keeping ground returns short, signal loop areas small, and power inputs bypassed to signal return. These practices significantly reduce EMI radiation.

The following guidelines help reduce circuit inductance in both backplanes and motherboards:

- Route traces over a continuous plane with no interruptions. Do not route over a split power or ground plane. If there are vacant areas on a ground or power plane, avoid routing signals over the vacant area. This increases inductance and EMI radiation levels.
- Separate noisy digital grounds from analog grounds to reduce coupling. Noisy digital grounds can affect sensitive DC subsystems.

- Connect all ground vias to every ground plane and every power via to all power planes at equal potential. This helps reduce circuit inductance.
- Physically locate grounds between a signal path and its return. This minimizes the loop area.
- Avoid fast rise and fall times as much as possible. Signals with fast rise and fall times contain many high frequency harmonics, which can radiate EMI.
- Split ground planes beneath magnetics modules. The RJ-45 connector side of the transformer module should have chassis ground beneath it.

4.1.12 Traces for Decoupling Capacitors

Traces between decoupling and I/O filter capacitors should be as short and wide as practical. Long and thin traces are more inductive and would reduce the intended effect of decoupling capacitors. For similar reasons, traces to I/O signals and signal terminations should be as short as possible. Vias to the decoupling capacitors should be sufficiently large in diameter to decrease series inductance.

4.1.13 Ground Planes Under the Magnetics Module

The magnetics module chassis or output ground (secondary side of transformer) should be separated from the digital or input ground (primary side) by a physical separation of 100 mils minimum. Splitting the ground planes beneath the transformer minimizes noise coupling between the primary and secondary sides of the transformer and between the adjacent coils in the magnetics. This arrangement also improves the common mode choke functionality of magnetics module.

Figure 9. Ground Plane Separation

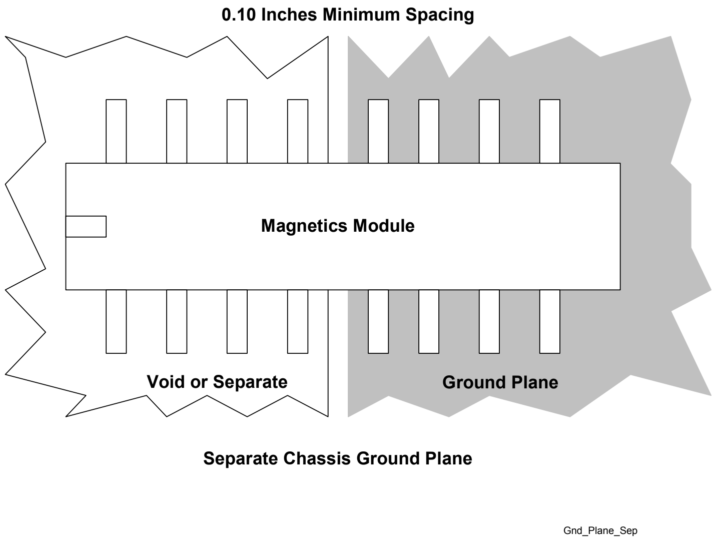
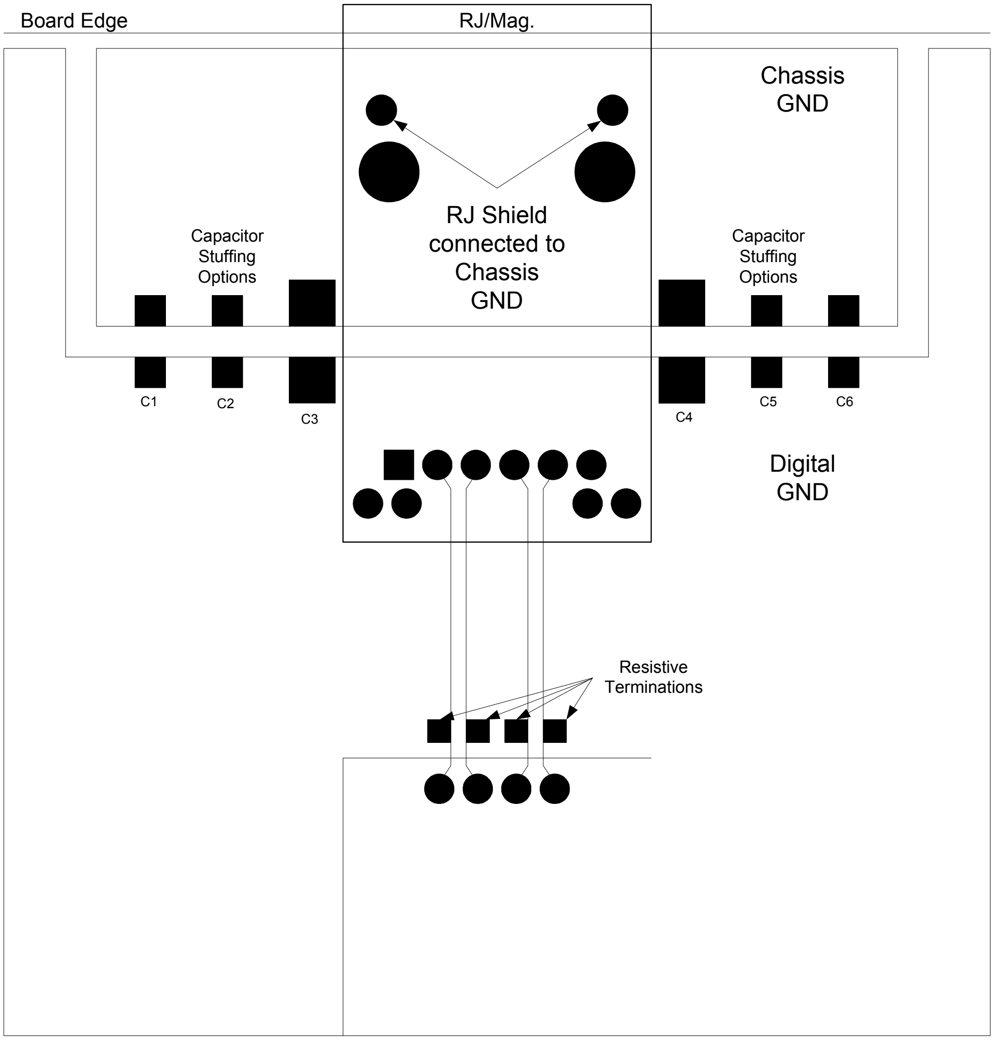


Figure 9 shows the split plane layout for a discrete magnetics module. Capacitors are used to interconnect chassis ground and signal ground.

Figure 10 shows the preferred method for implementing a ground split under an integrated magnetics module/RJ-45 connector. The capacitor stuffing options (C1 through C6) are used to reduce and filter high frequency emissions. The values of the capacitor stuffing options can be different for each board. Experiments need to be performed to determine which values provide best EMI performance.

Figure 10. Ideal Ground Split Implementation



The following table lists possible starting values for these capacitors.

Capacitors	Value
C3, C4	4.7 µF or 10 µF
C1, C2, C5, C6	470 pF to 0.1 µF

The placement of C1 through C6 can also be different for each board design (not all of the capacitors might need to be populated). Also, the capacitors might not be needed on both sides of the magnetic module.

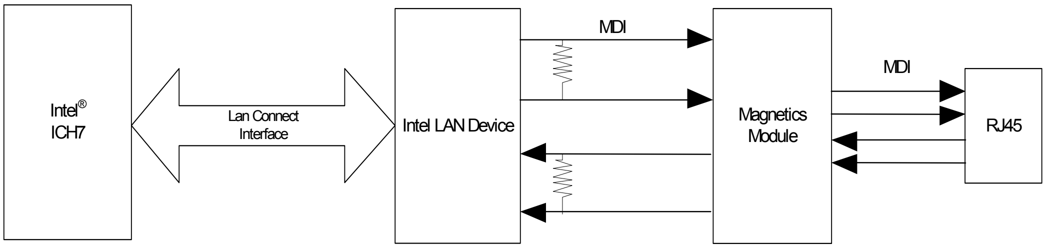
4.2 Layout for the 82562 PLC Device

This section provides layout guidelines specific to the 82562 PLC device.

4.2.1 Termination Resistors for Designs Based on 82562 PLC Device

The recommended value to terminate the transmit and receive differential pairs is 110 Ω ±1%. These termination resistors should be placed as close to the Platform LAN connect component as possible. This is due to the fact these resistors are terminating the entire impedance that is seen at the termination source, including the wire impedance reflected through the transformer.

Figure 11. 82562 PLC Device Differential Signal Termination



Place termination resistors as close to the Intel LAN device as possible.

4.2.2 Light Emitting Diodes for Designs Based on 82562EZ(EX) PLC Device

The 82562 PLC device has three high-current outputs to directly drive LEDs for link, activity and speed indication. Since LEDs are likely to be integral to a magnetics module, the LED traces need to be routed away from potential sources of EMI noise. In some cases, it might be desirable to attach filter capacitors.

4.3 Layout for the 82573

4.3.1 Termination Resistors for 82573-Based Designs

The four differential pairs are terminated with 49.9 Ω (1% tolerance) resistors, placed near the 82573. One resistor connects to the positive MDI signal trace and another resistor connects to the negative MDI signal trace. The opposite ends of the resistors connect together and to ground through a single 0.1 µF capacitor. The capacitor should be placed as close as possible to the 49.9 ohm resistors, using a wide trace.

Suggested component values should not be varied. The pads and traces for these components should be arranged with symmetrical pads and traces so that the length and symmetry of the differential pairs are not disturbed.

4.3.2 Light Emitting Diodes for 82573-Based Designs

The 82573 controller provides three programmable high-current outputs to directly drive LEDs for link activity and speed indication. Since the LEDs are likely to be integral to a magnetics module, the LED traces should be routed away from potential sources of EMI noise. In some cases, it might be desirable to attach filter capacitors.

4.4 Physical Layer Conformance Testing

Physical layer conformance testing (IEEE testing) is a fundamental requirement for all Ethernet LAN products. PHY testing is the final determination that a layout has been performed successfully. If designers do not have the resources and equipment to perform these tests, consideration should be made to have these tests contracted to an outside facility.

Crucial tests are as follows, listed in order of priority:

1. Bit Error Rate (BER). This is a good indicator of real world network performance. Perform bit error rate testing with long and short cables and many link partners.
2. Output Amplitude, Rise and Fall Time (10/100 Mb/s), Symmetry and Droop (1000 Mb/s). The appropriate PHY test waveform for the 82573 should be used.
3. Return Loss. This indicates proper impedance matching and is measured through the RJ-45 connector back toward the magnetics module.
4. Jitter Test (10/100 Mb/s) or Unfiltered Jitter Test (1000 Mb/s). This indicates clock recovery ability (master and slave for the GbE controller).
5. Harmonic Content for 10 Mb/s.
6. Duty Cycle Distortion for 100 Mb/s.

4.5 Troubleshooting Common Physical Layout Issues

The following is a list of common physical layer design and layout mistakes in LOM Designs.

1. Unequal length of the two traces within a differential pair. Inequalities create common-mode noise and will distort the transmit or receive waveforms.
2. Lack of symmetry between the two traces within a differential pair. Asymmetry can create common-mode noise and distort the waveforms. For each component and via that one trace encounters, the other trace should encounter the same component or via at the same distance from the Ethernet silicon.
3. Excessive distance between the Ethernet silicon and the magnetics. Long traces on FR4 fiberglass epoxy substrate will attenuate the analog signals. In addition, any impedance mismatch in the traces will be aggravated if they are longer than the four-inch rule.
4. Routing any other trace parallel to and close to one of the differential traces. Crosstalk getting onto the receive channel will cause degraded long cable BER. Crosstalk getting onto the transmit channel can cause excessive EMI emissions and can cause poor transmit BER on long cables. At a minimum, other signals should be kept 0.3 inches from the differential traces.
5. Routing one pair of differential traces too close to another pair of differential traces. After exiting the Ethernet silicon, the trace pairs should be kept 0.3 inches or more away from the other trace pairs. The only possible exceptions are in the vicinities where the traces enter or exit the magnetics, the RJ-45 connector, and the Ethernet silicon.
6. Use of a low quality magnetics module.
7. Re-use of an out-of-date physical layer schematic in an Ethernet silicon design. The terminations and decoupling can be different from one PHY to another.

8. Incorrect differential trace impedances. It is important to have ~100 W impedance between the two traces within a differential pair. This becomes even more important as the differential traces become longer. To calculate differential impedance, many impedance calculators only multiply the single-ended impedance by two. This does not take into account edge-to-edge capacitive coupling between the two traces. When the two traces within a differential pair are kept close to each other, the edge coupling can lower the effective differential impedance by 5 W to 20 W**.** Short traces have fewer problems if the differential impedance is slightly off target.
9. For the 82562EZ(EX) PLC design, use of a capacitor too large between the transmit traces or too much capacitance on the magnetic module's transmit center tap to ground. Using capacitors more than a few pico-Farads in either of these locations can slow the 100 Mb/s rise and fall times. This also causes return loss to fail at higher frequencies and degrades the transmit BER performance. If a capacitor is used, it should be less than 22 pF.

5.0 Flash Guidelines

General guidelines and design considerations for supporting Flash devices is discussed in this section.

5.1 Serial Peripheral Interface

The Serial Peripheral Interface (SPI) is new and is used to support a single SPI compatible Flash device. The SPI device can be used exclusively as the system BIOS device, exclusively for the Intel® 82573, or shared between system BIOS and the 82573.

Table 10. SPI Signal Description for the ICH7

ICH7 Signal Name	Description
SPI_MOSI	SPI serial output data from the Intel® ICH7 to the SPI Flash device.
SPI_MISO	SPI serial input data from the SPI Flash device to the Intel® ICH7.
SPI_CLK	SPI clock output from the Intel® ICH7.
SPI_CS#	SPI chip select.
SPI_ARB	SPI arbitration signal. This signal is used to arbitrate the SPI bus with the 82573 when shared Flash is implemented.

5.2 Serial Flash Vendors

The following vendors manufacture serial Flash devices that have been used successfully in previous designs. Additional details on the compatibility requirements for SPI devices can be obtained through the *ICH7 External Design Specification (EDS)*. Information on packaging and density on SPI devices can be obtained directly through the vendor.

SST: http://www.ssti.com/
STM: http://us.st.com/stonline/index.shtml

Note: This is not an extensive list. There might be other vendors. Your local Flash vendor can be contacted to determine if a compatible device is available.

5.3 Serial Peripheral Interface General Routing Guidelines

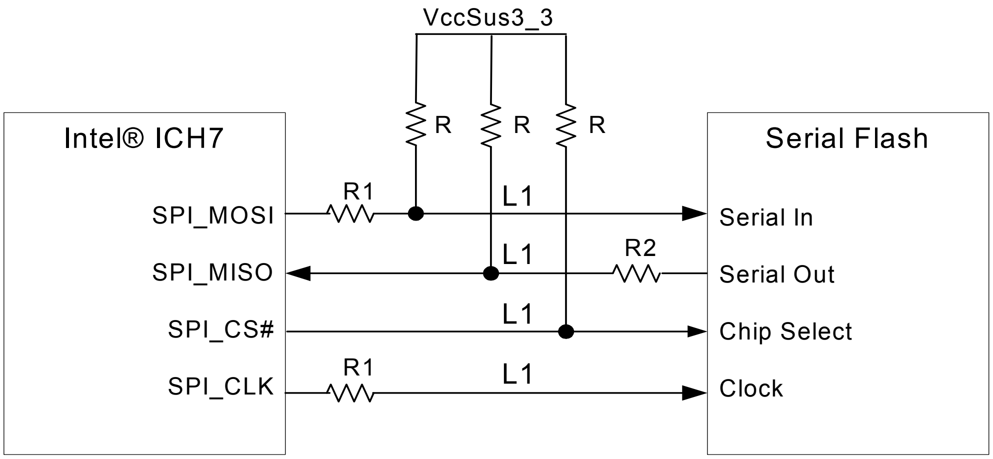
This section contains preliminary information and details for layout and routing guidelines for the ICH7 SPI. Additional serial Flash specific design considerations can be referred to the serial Flash vendor documentation.

The guidelines in this section cover three main topologies:

1. Non-shared Topology: The SPI device is used exclusively as the system BIOS. This document covers the guidelines on the SPI device used exclusively for the 82573. (Figure 12)
2. Shared Topology: The SPI device is shared between the system BIOS and the 82573.
3. Stuffing Options: This option supports a non-shared configuration for either system BIOS or for the 82573 through a single serial Flash device or shared topology through a single serial Flash device using stuffing options on the motherboard.

5.3.1 Routing Summary

Figure 12. SPI as System BIOS Topology (Non-shared Technology)



Notes:

1. R = 8.2 KΩ to 10 KΩ should be placed close to the ICH7 component.
2. R1 = 47 Ω for desktop systems or 33 Ω for mobile designs. R1 should be placed less than 100 mils from the ICH7 device.
3. R2 = 47 Ω for desktop systems or 33 Ω for mobile designs. R2 should be placed less than 100 mils from the serial Flash device.

Table 11. SPI Non-shared Routing Summary for the 2116 Stackup

Signal Name	Impedance	Width (W) / Spacing (S)	Layer	Length	Figure	Notes
SPI_MOSI SPI_MISO# SPI_CS# SPI_CLK	60 Ω ± 15%	W = 5 mils S = 7 mils	Microstrip	L1 = 0.5 – 11”	Figure 12	1

Note:

1. “W” represents the width of the signal. “S” represents spacing to any other signal.

Table 12. SPI Non-shared Routing Summary for the 1080 Stackup

Signal Name	Impedance	Width (W) / Spacing (S)	Layer	Length	Figure	Notes
SPI_MOSI SPI_MISO# SPI_CS# SPI_CLK	50 Ω ± 15%	W = 4 mils S = 5 mils	Microstrip	L1 = 0.5 – 10”	Figure 12	1

Note:

1. “W” represents the width of the signal. “S” represents spacing to any other signal.

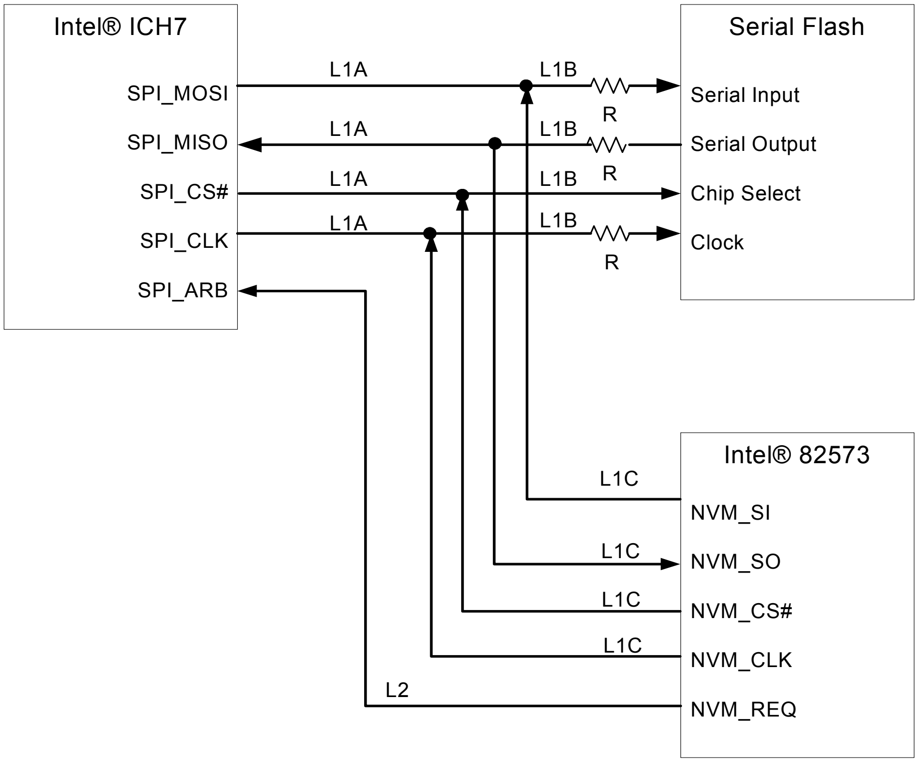
Table 13. SPI Non-shared Routing Summary for the Mobile Stackup

Signal Name	Impedance	Width (W) / Spacing (S)	Layer	Length	Figure	Notes
SPI_MOSI SPI_MISO# SPI_CS# SPI_CLK	55 Ω ± 15%	W = 4 mils S = 5 mils	Stripline	L1 = 0.5 – 10”	Figure 12	1

Note:

1. “W” represents the width of the signal. “S” represents spacing to any other signal.

Figure 13. SPI Shared Flash Exclusively Used with Intel® 82573



Note: R = 47 Ω and should be placed within 100 mils of the Flash device. (For mobile designs, R should be placed within 500 mils of the Flash device.)

Table 14. SPI Shared Topology Routing Summary for the 2116 Stackup

Signal Name	Impedance	Width (W) / Spacing (S)	Layer	Length	Figure	Notes
SPI_MOSI SPI_MISO# SPI_CS# SPI_CLK SPI_ARB	60 Ω ± 15%	W = 5 mils S = 7 mils	Microstrip	$L1_A$ = 0.5 – 8” $L1_B$ = 0.1” target $L1_C$ = 0.1 – 14” L2 = 1” – 18”	Figure 13	1

Note:
1. “W” represents the width of the signal. “S” represents spacing to any other signal.

Table 15. SPI Shared Topology Routing Summary for the 1080 Stackup

Signal Name	Impedance	Width (W) / Spacing (S)	Layer	Length	Figure	Notes
SPI_MOSI SPI_MISO# SPI_CS# SPI_CLK SPI_ARB	50 Ω ± 15%	W = 4 mils S = 5 mils	Microstrip	$L1_A$ = 0.5 – 8” $L1_B$ = 0.1” target $L1_C$ = 0.5 – 14” L2 = 1” – 18”	Figure 13	1

Note:

1. “W” represents the width of the signal. “S” represents spacing to any other signal.

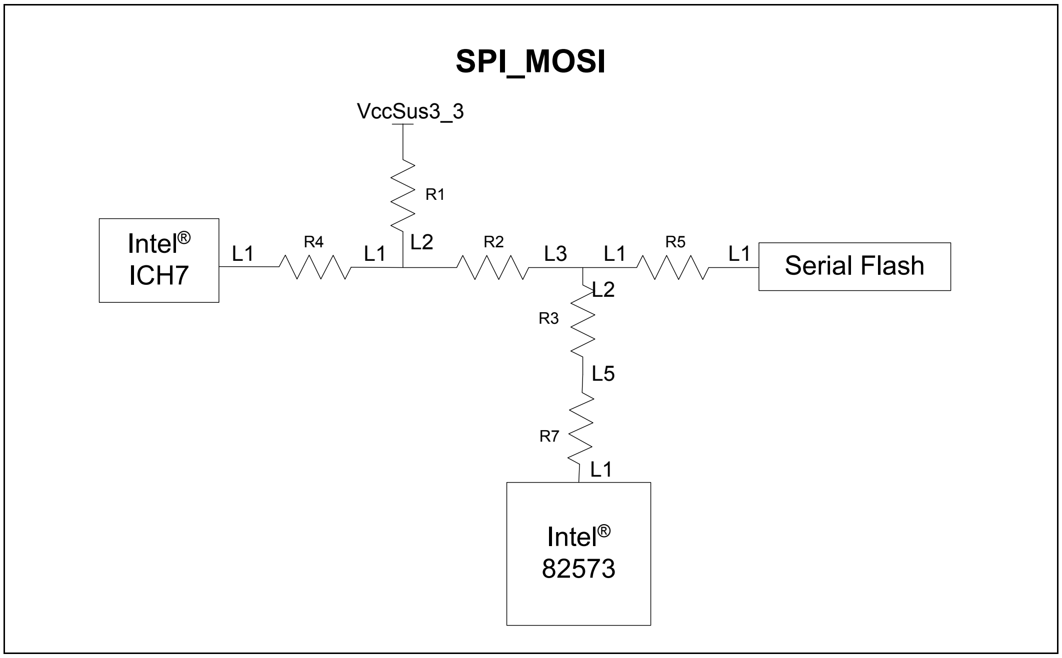
Table 16. SPI Shared Topology Routing Summary for the Mobile Stackup

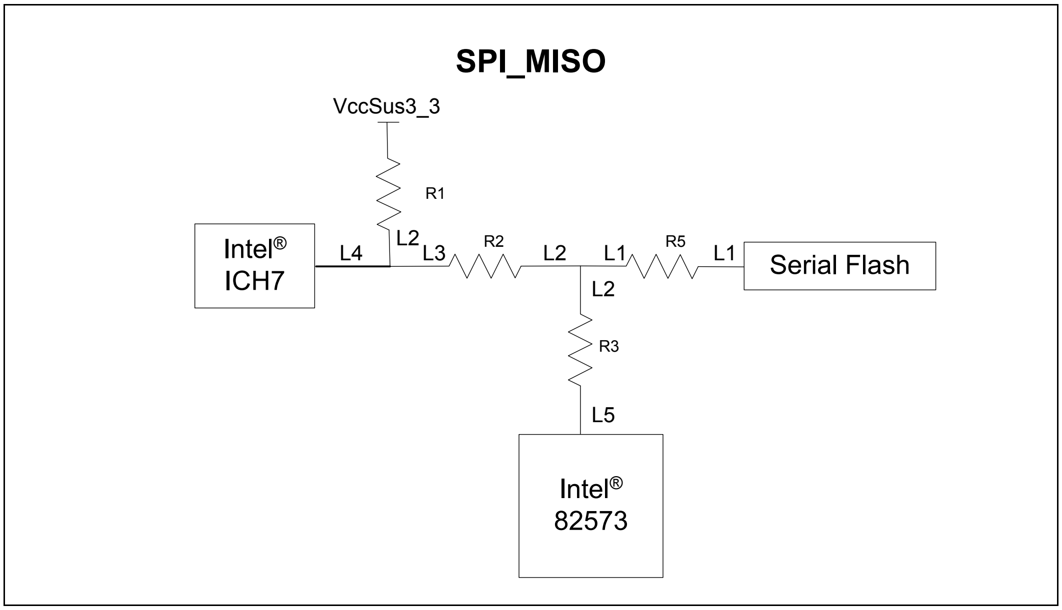
Signal Name	Impedance	Width (W) / Spacing (S)	Layer	Length	Figure	Notes
SPI_MOSI SPI_MISO# SPI_CS# SPI_CLK SPI_ARB	55 Ω ± 15%	W = 4 mils S = 7 mils	Stripline	$L1_A$ = 0.5 – 10” $L1_B$ = 0.1” target $L1_C$ = 0.5 – 6” L2 = 11”	Figure 13	1

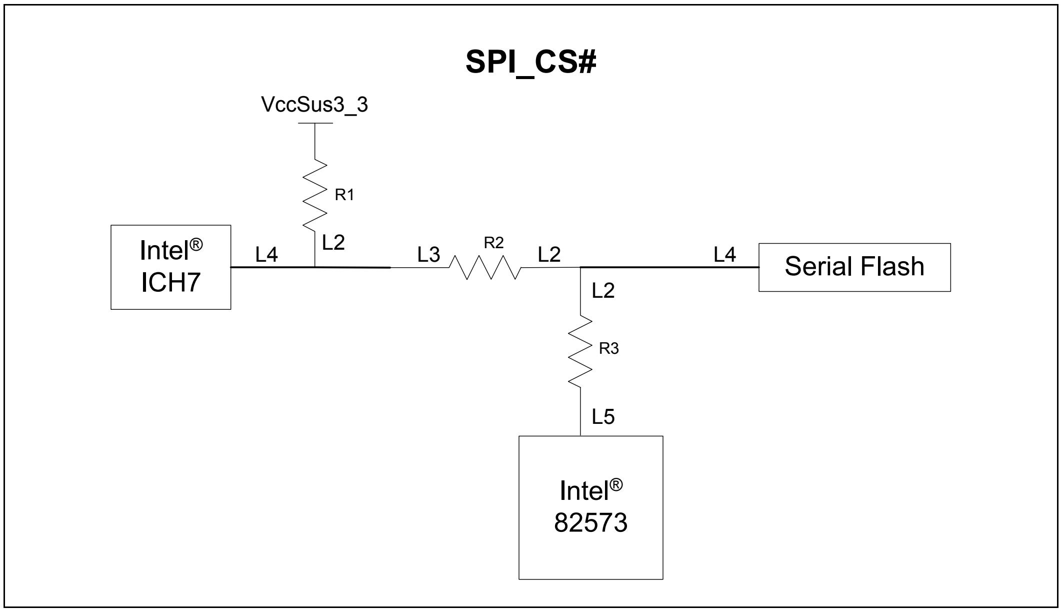
Note:

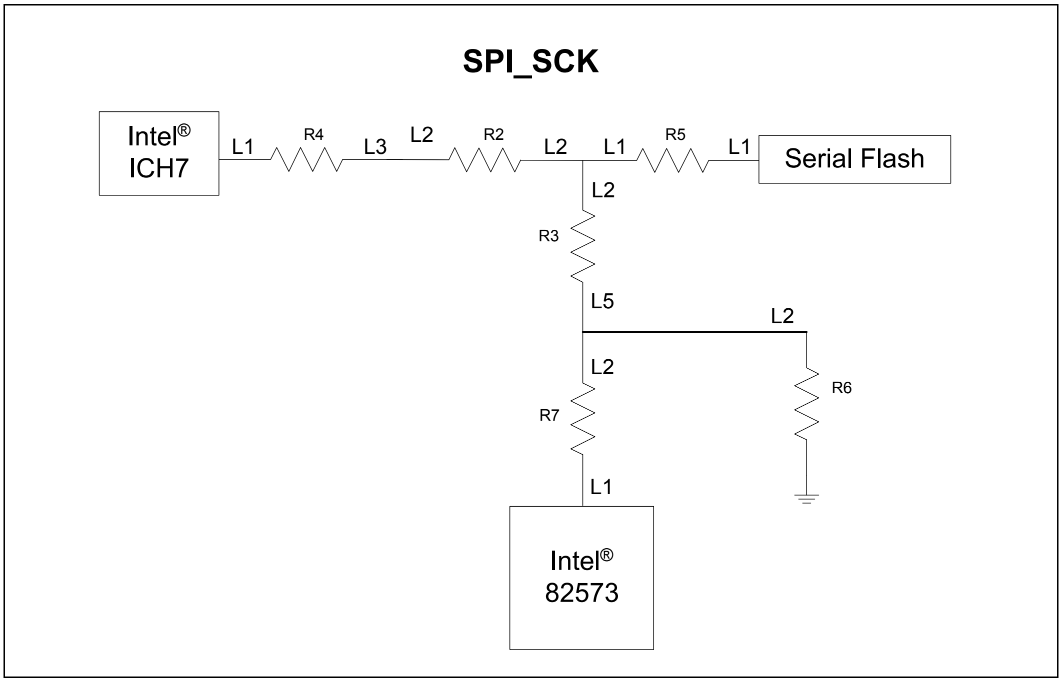
1. “W” represents the width of the signal. “S” represents spacing to any other signal.

Figure 14. Stuffing Options Supporting Shared Topology (Desktop Only)




SPI_MISO
VccSus3_3
R1
Intel®
ICH7
L4
L2
L3
R2
L2
L1
R5
L1
Serial Flash
L2
R3
L5
Intel®
82573


SPI_CS#
VccSus3_3
R1
Intel®
ICH7
L4
L2
L3
R2
L2
L4
Serial Flash
L2
R3
L5
Intel®
82573



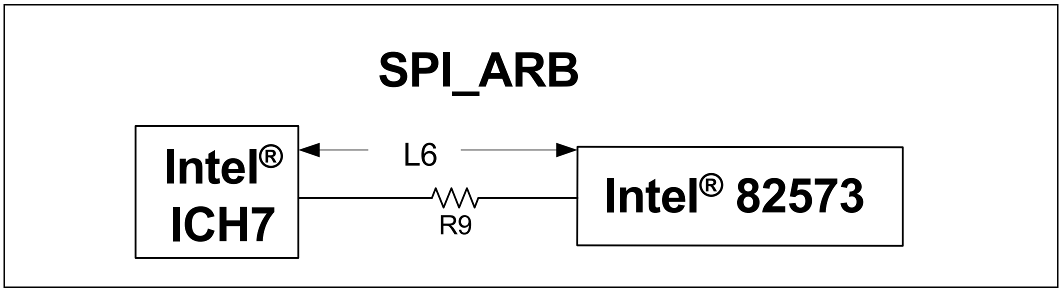


Table 17. Configurations and Stuffing Options

Configurations	Stuffing Options
SPI device as system BIOS only	R1 = 8.2 KΩ to 10 KΩ R2, R5 = 0 Ω R4, R8 = 47 Ω R3, R6, R7, R9 = Empty
SPI device used exclusively with the 82573	R1, R2, R4 = Empty R3, R5, R9 = 0 Ω R6 = 8.2 KΩ to 10 KΩ R7, R8 = 47 Ω
SPI Device shared between system BIOS and 82573	R1, R6 = Empty R2, R3, R4, R7, R9 = 0Ω R5, R8 = 47Ω

Table 18. SPI Stuffing Option Topology Routing Summary for the 2116 Stackup

Signal Name	Impedance	Width (W) / Spacing (S)	Layer	Length	Figure	Notes
SPI_MOSI SPI_MISO# SPI_CS# SPI_CLK SPI_ARB	60 Ω ± 15%	W = 5 mils S = 7 mils	Microstrip	L1 = 0.1” target L2 = 0.1 - 0.25” L3 = 0.5” - 7.5” L4 = 0.2” L5 = 1” - 14” L6 = 1”–18”	Figure 14	1

Note:
1. “W” represents the width of the signal. “S” represents spacing to any other signal.

Table 19. SPI Stuffing Option Topology Routing Summary for the 1080 Stackup

Signal Name	Impedance	Width (W) / Spacing (S)	Layer	Length	Figure	Notes
SPI_MOSI SPI_MISO# SPI_CS# SPI_CLK SPI_ARB	50 Ω ± 15%	W = 4 mils S = 5 mils	Microstrip	L1 = 0.1” target L2 = 0.1 - 0.25” L3 = 0.5” - 7.5” L4 = 0.2” L5 = 1” - 14”	Figure 14	1

Note:
1. “W” represents the width of the signal. “S” represents spacing to any other signal.

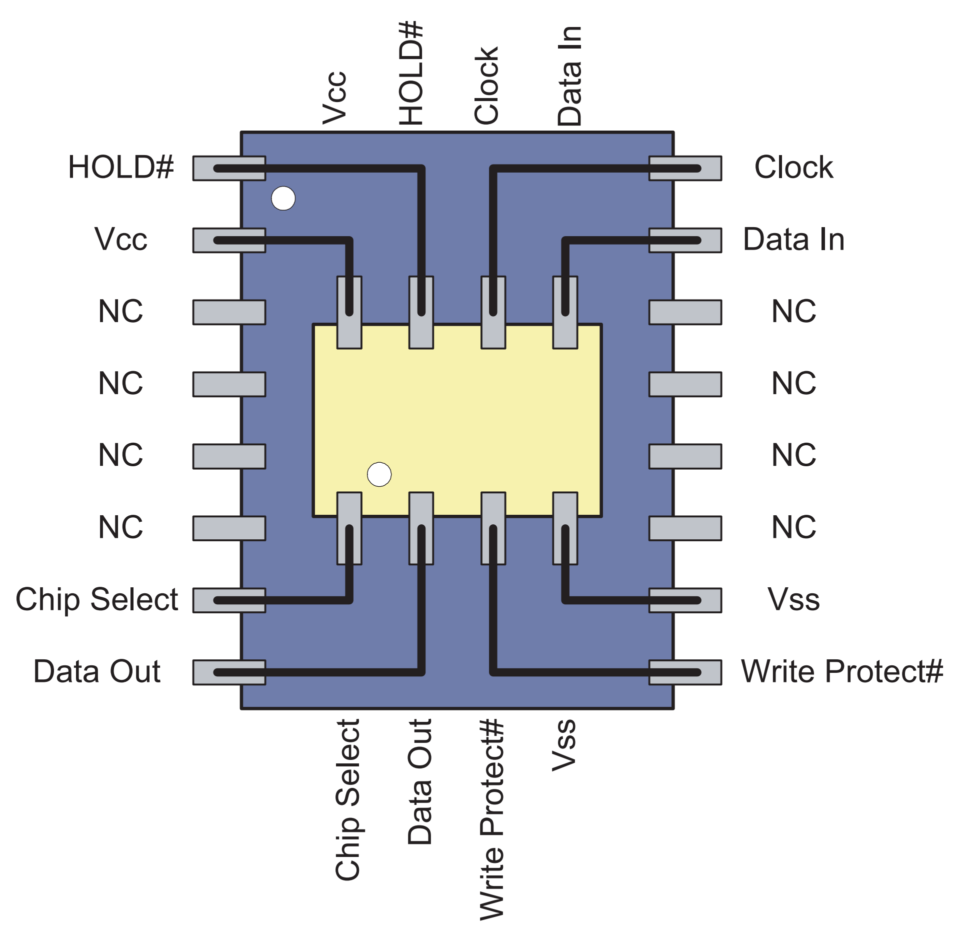
5.3.2 Terminating Unused SPI Signals

If the SPI is not implemented on the platform, all SPI signals can be left unconnected.

5.3.3 SPI Dual Footprint - SO8 and SO16 Packages

Although SPI is comprised of a 4-signal bus, SPI devices can be found in both 8-pin and 16-pin Small Outline Integrated Circuit (SOIC) packages. This section contains an example of an SO8 and SO16 dual footprint to accommodate both packages on the board. More details regarding these devices can be found in the vendors’ datasheets.

Figure 15. SPI Dual Footprint for SO8 and SO16 Packages



5.4 82573/82562 PLC Ball Outs

5.4.1 82573E/82573V Ball Out

	A	B	C	D	E	F	G	H	J	K	L	M	N	P
1	VSS	VCC25_OUT	PE_T0n	PE_TR0p	NC	PE_R0n	PE_CLKp	TEST0	TEST3	TEST6	TEST7	TEST8	VSS	TEST11
2	IREG25_IN	VCC25_OUT	VSS	VSS	VSS	PE_R0p	PE_CLKn	TEST1	TEST4	VSS	THERMn	FUSEV	TEST10	VCC33
3	IREG25_IN	VSS	NC	NVM_SHARED	TEST15	VCC33	VCC25	TEST2	TEST5	VCC12	THERMp	TEST9	TEST12	CTRL_12
4	CTRL_25	NVM_REQ	VCC12	VSS	VSS	VSS	VSS	VCC25	VCC33	VCC12	NC	VCC25	JTAG_TMS	JTAG_TDI
5	NVM_PROT	EN25REG	VCC12	VSS	VSS	VSS	VCC25	VCC25	VCC25	VCC12	VCC12	NC	JTAG_TCK	LAN_PWR_GOOD
6	NVM_TYPE	VCC25	AUX_PRESENT	VSS	VSS	VSS	VCC12	VCC12	VCC12	VCC12	NC	NC	VCC33	JTAG_TDO
7	VCC33	NC	SDP[3]	VSS	VSS	VSS	VSS	VCC12	VCC12	VCC12	DEVICE_OFF#	NC	VCC25	PE_RST#
8	SDP[0]	SDP[1]	SDP[2]	VSS	VSS	VSS	VSS	VCC12	VCC12	VCC12	NC	TEST13	VCC33	VSS
9	NVM_SI	NVM_SO	NVM_SK	VCC33	VSS	VSS	VSS	VSS	VCC12	VCC12	VCC12	NC	NC	TEST14
10	VCC12	NVM_CS#	VSS	NC	VSS	VSS	VSS	VSS	VCC12	VCC12	VCC12	VCC33	ALT_CLK125	PE_WAKE#
11	VCC25	LED0#	LED1#	NC	NC	VSS	VSS	VCC12	VCC12	VCC12	NC	SMB_DAT	SMB_ALRT#/ASF_PWR_GOOD	SMB_CLK
12	LED2#	PHY_HSDACp	VSS	PHY_REF	NC	VCC12	VCC12	VCC12	VCC25	NC	VCC25	NC	VSS	VCC33
13	TEST_EN	PHY_HSDACn	MDI0p	VSS	MDI1p	MDI2p	VCC12	MDI3p	NC	VCC25	NC	NC	NC	NC
14	TEST16	PHY_TSTPT	MDI0n	NC	MDI1n	MDI2n	VSS	MDI3n	XTAL2	XTAL1	CLK_VIEW	NC	NC	NC

5.4.2 82573L Ball Out

	A	B	C	D	E	F	G	H	J	K	L	M	N	P
1	VSS	VCC25_ OUT	PE_T0n	PE_TR0p	NC	PE_R0n	PE_CLKp	TEST0	TEST3	TEST6	TEST7	TEST8	VSS	NC
2	VCC3.3_ REG25	VCC25_ OUT	VSS	VSS	VSS	PE_R0p	PE_CLKn	TEST1	TEST4	VSS	THERMn	FUSEV	TEST10	VCC33
3	VCC3.3_ REG25	VSS	NC	NVM_ SHARED	NC	VCC33	VCC25	TEST2	TEST5	VCC12	THERMp	TEST9	NC	CTRL_12
4	CTRL_25	NVM_REQ	VCC12	VSS	VSS	VSS	VSS	VCC25	VCC33	VCC12	NC	VCC25	JTAG_TMS	JTAG_TDI
5	NVM_ PROT	EN25REG	VCC12	VSS	VSS	VSS	VCC25	VCC25	VCC25	VCC12	VCC12	NC	JTAG_ TCK	LAN_PWR_ GOOD
6	NVM_ TYPE	VCC25	AUX_PWR	VSS	VSS	VSS	VCC12	VCC12	VCC12	VCC12	NC	NC	VCC33	JTAG_TDO
7	VCC33	NC	NC	VSS	VSS	VSS	VSS	VCC12	VCC12	VCC12	DEVICE_ OFF#	NC	VCC25	PE_RST#
8	NC	NC	NC	VSS	VSS	VSS	VSS	VCC12	VCC12	VCC12	NC	NC	VCC33	VSS
9	NVM_SI	NVM_SO	NVM_SK	VCC33	VSS	VSS	VSS	VSS	VCC12	VCC12	VCC12	NC	NC	CLK_REQ#
10	VCC12	NVM_CS#	VSS	NC	VSS	VSS	VSS	VSS	VCC12	VCC12	VCC12	VCC33	ALT_CLK125	PE_WAKE#
11	VCC25	LED0#	LED1#	NC	NC	VSS	VSS	VCC12	VCC12	VCC12	NC	RSVD	RSVD	RSVD
12	LED2#	PHY_ HSDACp	VSS	PHY_REF	NC	VCC12	VCC12	VCC12	VCC25	NC	VCC25	NC	VSS	VCC33
13	TEST_EN	PHY_ HSDACn	MDI0p	VSS	MDI1p	MDI2p	VCC12	MDI3p	NC	VCC25	NC	NC	NC	NC
14	NC	PHY_ TSTPT	MDI0n	NC	MDI1n	MDI2n	VSS	MDI3n	XTAL2	XTAL1	CLK_VIEW	NC	NC	NC

5.4.3 82562EX Ball Out

	A	B	C	D	E	F	G	H	J	K	L	M	N	P
1	NC	NC	NC	NC	VCC	NC	NC	NC	NC	NC	NC	NC	VSS	NC
2	NC	NC	NC	NC	VSS	NC	NC	NC	NC	VSS	NC	NC	NC	VCC
3	VCC	VSS	NC	NC	NC	NC	NC	NC	NC	VCC	NC	NC	NC	NC
4	NC	NC	NC	VSS	VSS	VSS	NC	NC	NC	VCC	VCC	NC	NC	NC
5	NC	NC	NC	VSS	VSS	VSS	VCCR	VCCR	VCCR	VCC	VCC	NC	NC	NC
6	NC	NC	NC	VSS	VSS	VSS	VCC	VCC	VCC	VCC	VSS	VSS	VCC	NC
7	VCC	VSS	NC	VSS	VSS	VSS	VSS	VCC	VCC	VCC	ADV10	NC	NC	NC
8	NC	NC	NC	VSS	VSS	VSS	VSS	VCC	VCC	VCC	NC	NC	VCC	VSS
9	NC	NC	NC	NC	VSS	VSS	VSS	VSS	VCC	VCC	VCC	NC	NC	NC
10	NC	NC	VSS	ISOL_EXEC	VSS	VSS	VSS	VSS	VCC	VCC	VCC	NC	NC	NC
11	VCCT	SPDLED#	ACTLED#	NC	VCCT	VSS	VSS	VCC	VCC	VCC	VSS	NC	NC	NC
12	LILED#	TOUT	VSSA	ISOL_TI	VCCT	NC	NC	NC	NC	VSS	NC	JRXD[2]	VSSP	VCC
13	TESTEN	RBIAS100	TDP	VSSA	RDP	NC	NC	NC	NC	VCC	JTXD[1]	JRSTSYNC	JRXD[1]	JRXD[0]
14	NC	RBIAS10	TDN	ISOL_TCK	RDN	NC	NC	NC	X2	X1	JTXD[2]	JTXD[0]	JCLK	NC

5.4.4 82562GZ Ball Out

	A	B	C	D	E	F	G	H	J	K	L	M	N	P
1	NC	NC	NC	NC	VCC	NC	NC	NC	NC	NC	NC	NC	VSS	NC
2	NC	NC	NC	NC	VSS	NC	NC	NC	NC	VSS	NC	NC	NC	VCC
3	VCC	VSS	NC	NC	NC	NC	NC	NC	NC	VCC	NC	NC	NC	NC
4	NC	NC	NC	VSS	VSS	VSS	NC	NC	NC	VCC	3.3V	NC	NC	NC
5	NC	NC	NC	VSS	VSS	VSS	VCCR	VCCR	VCCR	3.3V	3.3V	NC	NC	NC
6	NC	NC	NC	VSS	VSS	VSS	3.3V	3.3V	3.3V	3.3V	VSS	VSS	VCC	NC
7	VCC	VSS	NC	VSS	VSS	VSS	VSS	3.3V	3.3V	3.3V	ADV10/LAN_DISABLE#	NC	NC	NC
8	NC	NC	NC	VSS	VSS	VSS	VSS	3.3V	3.3V	3.3V	NC	NC	VCC	VSS
9	NC	NC	NC	NC	VSS	VSS	VSS	VSS	3.3V	3.3V	3.3V	NC	NC	NC
10	NC	NC	VSS	ISOL_EXEC	VSS	VSS	VSS	VSS	3.3V	3.3V	3.3V	NC	NC	NC
11	VCC	SPDLED#	ACTLED#	NC	VCCT	VSS	VSS	3.3V	3.3V	3.3V	VSS	NC	NC	NC
12	LILED#	TOUT	VSS	ISOL_TI	VCCT	NC	NC	NC	NC	VSS	NC	JRXD[1]	VSS	VCC
13	TESTEN	RBIAS100	TDP	VSS	RDP	NC	3.3V	NC	NC	VCC	JTXD[1]	JRSTSYNC	JRXD[1]	JRXD[0]
14	NC	RBIAS10	TDN	ISOL_TCK	RDN	NC	VSS	NC	X2	X1	JTXD[2]	JTXD[0]	JCLK	NC

6.0 Crystal Guidelines

6.1 Crystal Selection Parameters

Quartz crystals are generally considered to be the mainstay of frequency control components due to their low cost and implementation simplicity. They are available from numerous vendors in many package types and with various specification options.

All crystals used with Intel® Ethernet controllers are described as “AT-cut”, which refers to the angle the unit is sliced with respect to the long axis of the quartz stone.

Table 20 lists the crystal electrical parameters and provides suggested values for typical designs. The parameters listed are described in the following subsections.

Table 20. Crystal Parameters

Parameter	Suggested Value
Vibration Mode	Fundamental
Nominal Frequency	25.000 MHz at 25° C (required)
Frequency Tolerance	• ±30 ppm recommended at 25 °C • ±30 ppm required for the 82573L only
Temperature Stability	±30 ppm at 0° C to 70° C required for the 82573
Calibration Mode	Parallel
Load Capacitance	20 pF
Shunt Capacitance	6 pF maximum
Equivalent Series Resistance	• For 82573: 40 Ω at 25 MHz • For 82562: 20 Ω at 25 MHz
Drive Level	0.5 mW
Aging	±5 ppm per year maximum

Recommended crystal manufacturers:

Rami Technology Asia Ltd*	AS-25.000-20-F-SMD-TR-NS5
TXC Corporation*	6C25000355

6.1.1 Vibration Mode

Crystals in the frequency range listed in Table 20 are available in both fundamental and third overtone. Unless there is a special need for third overtone, fundamental mode crystals should be used.

At any given operating frequency, third overtone crystals are thicker and more rugged than fundamental mode crystals. Third overtone crystals are more suitable for use in military or harsh industrial environments. Third overtone crystals require a trap circuit (extra capacitor and inductor) in the load circuitry to suppress fundamental mode oscillation as the circuit powers up. Selecting values for these components is beyond the scope of this document.

6.1.2 Nominal Frequency

Intel Ethernet controllers use a crystal frequency of 25.000 MHz. The 25 MHz input is used to generate a 125 MHz transmit clock for 100BASE-TX and 1000BASE-TX operation. 10 MHz and 20 MHz transmit clocks are used for 10BASE-T operation.

6.1.3 Frequency Tolerance

The frequency tolerance for an Ethernet physical layer device is dictated by the IEEE 802.3 specification as ±50 parts per million (ppm). This measurement is referenced to a standard temperature of 25° C.

Note: Intel recommends using a crystal device with a ±30 ppm frequency tolerance to ensure that the total crystal circuit tolerance does not exceed ±50 ppm. In addition to the crystal device, factors such as PCB trace capacitance, pad capacitance, and loading capacitors' tolerance add to the overall frequency variance.

6.1.4 Temperature Stability and Environmental Requirements

Temperature stability is a standard measure of how the oscillation frequency varies over the full operational temperature range (and beyond). Several optional temperature ranges are currently available, including -40° C to +85° C for industrial environments. Some vendors separate operating temperatures from temperature stability. Manufacturers may also list temperature stability as 50 ppm in their data sheets.

Note: Crystals also carry other specifications for storage temperature, shock resistance, and reflow solder conditions. Crystal vendors should be consulted early in the design cycle to discuss the application and its environmental requirements.

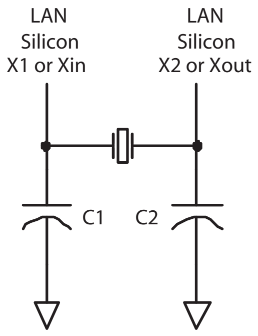
6.1.5 Calibration Mode

The terms "series-resonant" and "parallel-resonant" are often used to describe crystal circuits. Specifying parallel mode is critical to determining how the crystal frequency is calibrated at the factory.

A crystal specified and tested as series-resonant oscillates without problem in a parallel-resonant circuit, but the frequency is higher than nominal by several hundred parts per million. The purpose of adding load capacitors to a crystal circuit is to establish resonance at a frequency higher than the inherent series resonant frequency of the crystal.

Figure 16 illustrates a simplified schematic of the 82562 and the 82573 crystal circuit. The crystal and the capacitors form a feedback element for the internal inverting amplifier. This combination is called parallel-resonant because it has positive reactance at the selected frequency. In other words, the crystal behaves like an inductor in a parallel LC circuit.

Figure 16. Crystal Circuit



6.1.6 Load Capacitance

The formula for crystal load capacitance is as follows:

$$C_L = \frac{(C1 \cdot C2)}{(C1 + C2)} + C_{stray}$$

where C1 = C2 = 22 pF (as suggested in most Intel reference designs)
and C_{stray} = allowance for additional capacitance in pads, traces and the chip carrier within the Ethernet controller package

An allowance of 3 pF to 7 pF accounts for lumped stray capacitance. The calculated load capacitance is 16 pF with an estimated stray capacitance of about 5 pF.

Individual stray capacitance components can be estimated and added. For example, surface mount pads for the load capacitors add approximately 2.5 pF in parallel to each capacitor. This technique is especially useful if Y1, C1 and C2 must be placed farther than approximately one-half (0.5) inch from the controller. It is worth noting that thin circuit boards generally have higher stray capacitance than thick circuit boards.

Standard capacitor loads used by crystal manufacturers include 16 pF, 18 pF and 20 pF. Any of these values will generally operate with the controller. However, a difference of several pico-Farads between the calibrated load and the actual load will pull the oscillator slightly off frequency.

Note: C1 and C2 may vary by as much as 5% (approximately 1 pF) from their nominal values.

6.1.7 Shunt Capacitance

The shunt capacitance parameter is relatively unimportant compared to load capacitance. Shunt capacitance represents the effect of the crystal’s mechanical holder and contacts. The shunt capacitance should equal a maximum of 6 pF (7 pF is also acceptable).

6.1.8 Equivalent Series Resistance

Equivalent Series Resistance (ESR) is the real component of crystal impedance at the calibration frequency, which the inverting amplifier loop gain must overcome. ESR varies inversely with frequency for a given crystal family. The lower the ESR, the faster the crystal starts up. Crystals with an ESR value of 50 Ω or better should be used.

Note: The specific controller documentation should be verified since some devices may have tighter ESR requirements. For example, Intel recommends that 82573 devices use crystals with an ESR value of 20 Ω or less.

6.1.9 Drive Level

Drive level refers to power dissipation in use. The allowable drive level for a Surface Mounted Technology (SMT) crystal is less than its through-hole counterpart since surface mount crystals are typically made from narrow, rectangular AT strips, rather than circular AT quartz blanks.

Some crystal datasheets list crystals with a maximum drive level of 1 mW. However, Intel Ethernet controllers drive crystals to a level less than the suggested 0.5 mW value. This parameter does not have much value for on-chip oscillator use.

6.1.10 Aging

Aging is a permanent change in frequency (and resistance) occurring over time. This parameter is most important in its first year because new crystals age faster than old crystals. Crystals used should have a maximum of ±5 ppm per year aging.

6.2 Reference Crystal

The normal tolerances of the discrete crystal components can contribute to small frequency offsets with respect to the target center frequency. To minimize the risk of tolerance-caused frequency offsets causing a small percentage of production line units to be outside of the acceptable frequency range, it is important to account for those shifts while empirically determining the proper values for the discrete loading capacitors, C1 and C2.

Most crystals will oscillate slightly higher or slightly lower than the exact center of the target frequency even with a perfect support circuit. Therefore, frequency measurements (which determine the correct value for C1 and C2) should be performed with an ideal reference crystal. When the capacitive load is exactly equal to the crystal load rating, an ideal reference crystal will be perfectly centered at the desired target frequency.

There are several methods available for choosing the appropriate reference crystal:

- If a Saunders and Associates (S&A) crystal network analyzer is available, then discrete crystal components can be tested until one is found with zero or nearly zero ppm deviation (with the appropriate capacitive load). A crystal with zero or near zero ppm deviation will be a good reference crystal to use in subsequent frequency tests to determine the best values for C1 and C2.
- If a crystal analyzer is not available, then the selection of a reference crystal can be done by measuring a statistically valid sample population of crystals, which has units from multiple lots and approved vendors. The crystal, which has an oscillation frequency closest to the center of the distribution, should be the reference crystal used during testing to determine the best values for C1 and C2.
- It may also be possible to ask the approved crystal vendors or manufacturers to provide a reference crystal with zero or nearly zero deviation from the specified frequency when it has the specified C-load capacitance.

Note: For the 82562 devices, it is recommended to choose a crystal with an ESR value of 20 Ω. For the 82573 devices, it is recommended to choose a crystal with an ESR value of 40 Ω or less (for a maximum of 50 Ω).

When choosing a crystal, IEEE specifications compliance for Fast Ethernet (10/100 Mb/s) and Gigabit Ethernet (1000 Mb/s) must be considered. To ensure this, the transmitter reference frequency must be precise within ±50 ppm. Intel recommends the use of a transmitter reference frequency that is accurate to within ±30 ppm to account for variations in crystal accuracy due to crystal manufacturing tolerance.

6.3 Circuit Board

Since the dielectric layers of the circuit board are allowed some reasonable variation in thickness, the stray capacitance from the printed board (to the crystal circuit) will also vary. If the thickness tolerance for the outer layers of dielectric are controlled within ±17% of nominal value, the circuit board should not cause more than ±2 pF variation to the stray capacitance at the crystal. When tuning crystal frequency, it is recommended that at least three circuit boards are tested for frequency. These boards should differ from production lots of bare circuit boards.

Alternatively, a larger sample population of circuit boards can be used. A larger population increases the probability of obtaining the full range of possible variations in dielectric thickness and the full range of variation in stray capacitance.

Next, the exact same crystal and discrete load capacitors (C1 and C2) must be soldered onto each board, and the LAN reference frequency should be measured on each circuit board.

The circuit board, which has a LAN reference frequency closest to the center of the frequency distribution, should be used while performing the frequency measurements to select the appropriate values for C1 and C2.

6.4 Temperature Changes

Temperature changes can cause the crystal frequency to shift. Therefore, frequency measurements should be done in the final system chassis across the system rated operating temperature range.

7.0 Design and Layout Checklists

Table 21. 82573 Design Checklist

Section	Check Items	Remarks	Done	Comments
General	Obtain the most recent documentation and specification updates.	Documents are subject to frequent change.		
	Observe instructions for special pins needing pull-up or pull-down resistors.	Do not connect pull-up or pull-down resistors to any pins marked No Connect, Test, or Reserved.		
82573	Connect PCIe* interface pins to corresponding pins on ICH.			
	Place AC coupling capacitors (0.1 μF) near the PCIe* transmitter.			
	Connect balls G2 PE_CLKn and G1 PE_CLKp to 100 MHz PCIe* system clock.			
	Connect PE_RST# to PLTRST# on the ICH.			
	Connect PE_WAKE# to PE_WAKE# on the ICH.			
	Connect ball P5 LAN_PWR_GOOD to RSMRST# on the ICH.	Connect to the reset supervisor for the LAN power well.		
	Connect ball L7 DEVICE_OFF# to SUPER_IO_GP_DISABLE#.	Connect to a super I/O pin that retains its value during PCIe* reset, is driven from the resume well, and defaults to one on power-up. If not connected to Super I/O pin, then DEVICE_OFF# should be connected with an external pull-up resistor.		
	Pull down ball D12, PHY_REF, with a 4.99 KΩ 1% resistor.			
	Pull down ball A13, TEST_EN, with a 3.3 KΩ resistor			
	Leave ball C3, DOCK_IND, unconnected. This feature is not supported in the 82573.			
	82573L only: Connect ball P9, CLKREQ#, to the clock driver responsible for generating the PCIe* clock.	**82573L only**: This signal can be left unconnected if functionality is not desired; however, functionality must also be disabled in the NVM.		
	Ensure that ball C6, AUX_PRESENT (AUX_PWR for the 82573L), is pulled-up to 3.3V standby power supply if the LAN controller is powered from standby supplies. This signal should be pulled down if auxiliary power is not used.			

Table 21. (Continued) 82573 Design Checklist

Section	Check Items	Remarks	Done	Comments
Clock Source	Use a 25 MHz 30 ppm accuracy at 25° C clock source. Avoid components that introduce jitter.	Parallel resonant crystals are preferred. An oscillator can be used if testability rules require turning off the clock. If an oscillator is used, consider a series termination resistor of 22 Ω to 33 Ω. Avoid PLL clock buffers.		
	Connect two 22 pF load capacitors to the crystal.	Capacitance affects accuracy of the frequency. It must be matched to crystal specifications, including estimated trace capacitance in calculation.		
EEPROM and Flash Memory	Use 0.1 µF decoupling capacitor.	This applies to EEPROM or Flash devices.		
	Connect WP# and HOLD# signals to VCC through a 3.3 KΩ resistor.	This applies to EEPROM or Flash devices.		
	For shared Flash configuration, connect ball D3, NVM_SHARED, to ground through a 3.3 KΩ resistor.			
	If SPI Flash is used, connect ball A6, NVM_TYPE, to ground through a 3.3 KΩ resistor.			
	To disable SPI NVM protection, install a jumper to connect ball A5, NVM_PROT, to ground.			
	Connect ball B4, NVM_REQ, to SPI_ARB on the ICH device. This signal should be unconnected for dedicated LAN Flash configuration.	If both shared and dedicated configuration options are available, a 0 Ω stuffing option for this signal should be used.		
	Check EEPROM connections to NVM_CS#, NVM_SK, NVM_SI, and NVM_SO.			

Table 21. (Continued) 82573 Design Checklist

Section	Check Items	Remarks	Done	Comments
EEPROM and Flash Memory (continued)	For dedicated LAN Flash: • Connect NVM_CS# to CS# on the Flash device. • Connect NVM_SK through a 47 Ω resistor to SCK on the Flash device and through 8.2 KΩ to 10 KΩ resistor to ground. • Connect NVM_SI through a 47 Ω resistor to SI on the Flash device. • Connect NVM_SO through a 47 Ω resistor to SO on the Flash device.	The 47 Ω resistors should be placed closest to the outputs. A value other than 47 Ω can be optimal depending on board characteristics. A simulation should be done if a different value is used.		
	For shared LAN Flash: • Connect NVM_CS# to CS# on the Flash device. • Connect NVM_SK through a 47 Ω resistor to SCK on the Flash device and through 8.2 KΩ to 10 KΩ resistor to ground. • Connect NVM_SI to ICH_SPI_MOSI and through a 47 Ω resistor to SI on the Flash device. • Connect NVM_SO ICH_SPI_MISO through a 47 Ω resistor to SO on the Flash device.	The 47 Ω resistors should be placed closest to the outputs. A value other than 47 Ω can be optimal depending on board characteristics. A simulation should be done if a different value is used.		
	If both shared and non-shared options are to be made available, use 0 Ω resistors to minimize the stubs seen on the NVM lines.	The reference schematics and the ICH7 layout guidelines can be consulted for further details.		
SMBus	**82573L only**: The SMBus interface is not functional for the 82573L. Please leave it unconnected.	**82573L only**: If these pins are connected to the SMBus, it will not affect normal operation of the SMBus but the 82573L will not be seen on the bus.		
	82573E/V only: If SMBus is not used, connect pull-up resistors to SMB_CLK, SMB_DATA and SMB_ALRT#.	**82573E/V only**: 3.3 KΩ pull-up resistors are reasonable values.		
	82573E/V only: If SMBus is used, use pull-up resistors on SMB_DATA, SMB_ALRT# and SMB_CLK somewhere on the board.	**82573E/V only**: SMBus signals are open drain.		
	82573E/V only: For ASF and Intel® AMT applications with SMBus, connect ball N11, SMB_ALRT#/ASF_PWRGOOD, to the system PWR_GOOD signal or to VCC through a 3.3 KΩ pull-up resistor.	**82573E/V only**: The 3.3V rail, not 3.3V AUX should be used. Alternatively, ball N11 can be configured as an SMB_ALRT# output.		
	82573E/V only: Connect ball N11 SMB_ALRT#/ ASF_PWRGOOD to SMB_INT for certain management modes.	**82573E/V only**: The design guide provides further details for management modes.		

Table 21. (Continued) 82573 Design Checklist

Section	Check Items	Remarks	Done	Comments
Transmit and Receive Differential Pairs	For 10/100/1000BASE-T applications using the 82573E controller, use pairs of 49.9 Ω termination resistors with 0.1µF capacitors attached between center nodes and ground.	This applies to all four differential pairs of each port.		
Magnetics Module (10/100/1000BASE-T Applications)	If applicable, use integrated magnetics modules/RJ-45 connectors to minimize space requirements.	Multivendor pin compatibility is possible. The design guide provides further details on recommended models and manufacturers.		
	Qualify magnetics module carefully for Return Loss, Insertion Loss, Open Circuit Inductance, Common Mode Rejection, and Crosstalk Isolation.	Magnetics module is critical to passing IEEE PHY conformance tests and EMI test.		
	Supply 2.5V to the transformer center taps and use 0.1µF bypass capacitors.	2.5V biases the controller's output buffers. Magnetics with four center tap pins can have better characteristics than those with 1 to 2 center tap pins. Capacitors with low ESR should be used.		
Discrete Magnetics Module/RJ-45 Connector Option (10/100/1000BASE-T Applications)	Bob Smith termination: Use 4 x 75 Ω resistors for cable-side center taps and unused pins.	This method terminates pair-to-pair common mode impedance of the CAT5 cable.		
	Bob Smith termination: Use an EFT capacitor attached to the termination plane. Suggested values are 1500 pF/2KV or 1000 pF/3KV.	A minimum of 50-mil spacing from capacitor to traces and components should be maintained.		
	Connect signal pairs correctly to RJ-45 connector.			

Table 21. (Continued) 82573 Design Checklist

Section	Check Items	Remarks	Done	Comments
Power Supply and Signal Ground	Connect external PNP transistors to the regulator control CTRL_12 and CTRL_25 outputs to supply 1.2V and 2.5V, respectively. The connections and transistor parameters are critical.	Alternatively, external regulators are needed to generate these voltages. If the internal voltage regulator control circuit is not used, the CTRL pins may be left unconnected.		
	Pull ball B5, EN2.5REG, up to enable the on-die 2.5V regulator or pulled down to disable the on-die regulator.			
	Place a 1 Ω 1%, 0.5 W resistor at the emitter of the PNP transistor for the 1.2V regulator circuit to drop some of the voltage. Two 2.0 Ω 1%, 0.25 W resistors or any combination that yields 1.0 Ω, 0.5 W may also be used.			
	Ensure that there is adequate capacitance on the PNPs.	The design should be verified with the reference schematic. **82573L only**: Intel recommends using a 20 µF capacitance at the emitter of each PNP for the 82573L. **82573E/V only**: Intel recommends using 40 µF of capacitance at the emitter of each PNP.		
	82573E/V only: Place a 1 Ω resistor in series with a 10 µF ceramic capacitor at the collector of each PNP.	**82573E/V only**: Alternatively, a 10 µF tantalum capacitor can be used in place of the RC combination.		
	Provide a 3.3V supply. Use auxiliary power supplies.	Auxiliary power is necessary to support wake up from powerdown states.		
	Design with power supplies that start up properly.	A good guideline is that all voltages should ramp to within their control bands in 20 ms or less. It is desirable that voltages ramp in sequence (3.3V ramps first, 2.5V ramps second, 1.2V ramps last) and that the voltage rise be monotonic. The minimum rise time on the 3.3V power is 100 µs.		

Table 21. (Continued) 82573 Design Checklist

Section	Check Items	Remarks	Done	Comments
Power Supply and Signal Ground (continued)	Use decoupling and bulk capacitors generously.	Use approximately 12 bypass capacitors for the Ethernet silicon. Add approximately 20 µF to 30 µF of bulk capacitance per voltage rail, typically using 10 µF capacitors. If power is distributed on traces, bulk capacitors should be used at both ends. If power is distributed on cards, bulk capacitors should be used at the connector.		
	If the 1.2V and 2.5V rails are externally supplied (the 82573 has no control), ensure the following connections: • IREG2.5_IN (balls A2 and A3) should be tied to the 3.3V rail. • VCC2.5_OUT (balls B1 and B2) should be connected to the 2.5V rail. Alternatively, it could be left floating. • CTRL_1.2 (ball P3) should be tied to ground through a 3.3 KΩ resistor. Alternatively, it could be left floating. • CTRL_2.5 (ball A4) should be tied to ground through a 3.3 KΩ resistor. Alternatively, it could be left floating. • EN2.5REG (ball B5) should be pulled down through a 3.3 KΩ resistor	Pull-down resistors do not need to be exactly 3.3 KΩ; however, they must be greater than 1 KΩ.		
Chassis Ground (10/100/1000BASE-T Applications)	If possible, provide a separate chassis ground to connect the shroud of the RJ-45 connector and to terminate the line side of the magnetics module.	This design improves EMI behavior.		
	Place pads for approximately 4 to 6 "stitching" capacitors to bridge the gap from chassis ground to signal ground.	Typical values range from 0.1 µF to 4.7 µF. The correct value should be determined through experiment.		
LED Circuits	Basic recommendation is a single green LED for activity and a dual (bi-color) LED for speed. Many other configurations are possible. LEDs are configurable through the NVM.	Two-LED configuration is compatible with integrated magnetics modules. For the Link/Activity LED, connect the cathode to the LED1# pin and the anode to VCC. For the bi-color speed LED pair, one end is driven by the LED2# signal. The other end should be connected to LED0#.		

Table 21. (Continued) 82573 Design Checklist

Section	Check Items	Remarks	Done	Comments
LED Circuits (continued)	Connect LEDs to 3.3V as indicated in reference schematics.	The 3.3V AUX should be used for designs supporting wake-up. Consider adding one to two filtering capacitors per LED for extremely noisy situations. The suggested starting value is 470 pF.		
	Add current limiting resistors to LED paths.	Typical current limiting resistors are 250 Ω to 330 Ω when using a 3.3V supply. Current limiting resistors are typically included with integrated magnetics modules.		
Mfg Test	The 82573 controller supports a JTAG Test Access Port.	These signals need to be connected to the ICH if using system level JTAG.		

Table 22. 82573 Layout Checklist

Section	Check Items	Remarks	Done	Comments
General	Obtain the most recent documentation and specification updates.	Documents are subject to frequent change.		
	Route the transmit and receive differential traces before routing the digital traces.	Layout of differential traces is critical.		
Ethernet Devices	Place the Ethernet silicon at least 1 inch from the edge of the board.	With closer spacing, fields can follow the surface of the magnetics module or wrap past the edge of board. EMI may increase. Optimum location is approximately 1 inch behind the magnetics module.		
	Place the silicon at least 1 inch from the integrated magnetics module but less than 4 inches.	The trace length must be under 4 inches from the Ethernet controller through the magnetics to the RJ-45 connector. Signal attenuation will cause problems for traces longer than 4 inches. However, due to EMI, the silicon should be placed at least 1 inch away from the magnetics module.		
	Place the AC coupling capacitors on the PCIe transmit traces as close as possible to the 82573 but not further than 250 mils.	Size 0402, X7R is recommended. The AC coupling capacitors should be placed near the transmitter for PCIe*.		

Table 22. (Continued) 82573 Layout Checklist

Section	Check Items	Remarks	Done	Comments
Ethernet Devices (continued)	For the 82573 controller, ensure the trace impedance for the PCIe*differential pairs is 100 Ω +/- 20%.	These traces should be routed differentially.		
	Match trace lengths between PCIe pairs to within 3 inches.			
	Match trace lengths within each PCIe* pair on a segment-by-segment basis. Match trace lengths within a pair to 5 mils.			
Clock Source	Place crystal and load capacitors within 0.75 inches of the Ethernet device.	This reduces EMI.		
	Match the length of the clock lines to within 200 mils.	A large difference in length between the clock lines leads to clock skew.		
	Keep clock lines away from other digital traces (especially RESET signals), I/O ports, board edge, transformers and differential pairs.	This reduces EMI.		
Non-Volatile Memory	Ensure that traces meet the specifications of the design guide (placement is not critical). Refer to the design guide for routing specifications for particular stackups.	EEPROM and Flash can be placed a few inches away from the Ethernet controller to provide better spacing of critical components.		
	Place 47 Ω damping resistors on the NVM lines close to the signal driver. 0.1 inch is recommended. Refer to the design guide for all length requirements.			
	For both shared and dedicated NVM configuration options, place 0 Ω resistors to minimize the stubs on the NVM lines for each option.			
Transmit and Receive Differential Pairs	Design traces for 100 Ω differential impedance (± 20%).	This is a primary requirement for 10/100/1000 Mb/s Ethernet. Paired 50 Ω traces do not make 100 Ω differential. An impedance calculator can be used to verify this.		
	Avoid highly resistive traces (for example, 4 mil traces longer than 4 inches).	If trace length is a problem, thicker board dielectrics should be used to allow wider traces. Thicker copper is better than wider traces.		

Table 22. (Continued) 82573 Layout Checklist

Section	Check Items	Remarks	Done	Comments
Transmit and Receive Differential Pairs (continued)	Make traces symmetrical.	Pairs should be matched at pads, vias and turns. Rules for the autorouter should be carefully established. Asymmetry contributes to impedance mismatch. MDI pairs must not use autoroute.		
	Do not make 90° bends.	Corners can be beveled with turns based on 45° angles		
	Avoid through holes (vias).	If vias are used, the budget is two per trace.		
	Keep traces close together inside a differential pair.	Traces should be kept within 10 mils regardless of trace geometry.		
	Keep trace-to-trace length difference within each pair to less than 50 mils.	This will minimize signal skew and common mode noise. Improves long cable performance.		
	Pair-to-pair trace length does not have to be matched as differences are not critical.	The difference between the length of longest pair and the length of the shortest pair should be kept below 2 inches.		
	Try to keep differential pairs 50 mils or more away from each other and other traces, including NVM traces and parallel digital traces.	This minimizes crosstalk and noise injection. Pairs may be spaced as close as 30 mils as long as crosstalk isolation is 34 dB or more. Tighter spacing is allowed closer to connections.		
	Keep traces at least 0.1 inch away from the board edge.	This reduces EMI.		
	Avoid unused pads and stubs along the traces	Unused pads and stubs cause impedance discontinuities.		
	Route traces on appropriate layers.	Pairs should be run on different layers as needed to improve routing. Digital signals on adjacent layers must cross at 90° angles. Splits in power and ground planes must not cross.		
	Place termination resistors and capacitors close to the Ethernet device.	This prevents reflections. Symmetrical pads should be used. Termination components should not be connected to differential pairs with stub traces.		
Magnetics Module (10/100/1000BASE-T Applications)	Capacitors connected to center taps should be placed very close (less than 0.1 inch recommended) to integrated magnetics module.	This improves Bit Error Rate (BER).		

Table 22. (Continued) 82573 Layout Checklist

Section	Check Items	Remarks	Done	Comments
Power Supply and Signal Ground	When using the internal regulator control circuits of the 82573 controller with external PNP transistors, keep the distance from the CTRL_12 and CTRL_25 output balls to the transistors very short (less 0.5 inches) and use 25 mil (minimum) wide traces.	A low inductive loop should be kept from the regulator control pin, through the PNP transistor, and back to the chip from the transistor's collector output. The power pins should connect to the collector of the transistor through a power plane to reduce the inductive path. This reduces oscillation and ripple in the power supply.		
	Use planes if possible.	Narrow finger-like planes and very wide traces are allowed. If traces are used, 100 mils is the minimum.		
	The 1.2V and 2.5V regulating circuits require 0.5 inch x 0.5 inch thermal relief pads for each PNP.	The pads should be placed on the top layer under the PNP.		
	A 1 Ω, 0.5 W resistor should be placed at the emitter of the PNP for the 1.2V regulating circuit.	This resistor is used for heat dissipation.		
	Use decoupling and bulk capacitors generously. The 1.2V and 2.5V rails should have 25 µF of capacitance. Place these to minimize the inductance from each power pin to the nearest decoupling capacitor. 40 µF is recommended at the emitter (on the 3.3V rail) of each PNP used in the voltage regulating circuit.	Decoupling and bulk capacitors should be placed close to Ethernet device, with some along every side, using short, wide traces and large vias. If power is distributed on traces, bulk capacitors should be used at both ends. If power is distributed on cards, bulk capacitors should be used at the connector.		
	If decoupling capacitors are used on the LED lines, place them carefully.	Capacitors on LED lines should be placed near the LEDs.		
Chassis Ground (10/100/1000BASE-T Applications)	If possible, provide a separate chassis ground "island" to ground the shroud of the RJ-45 connector and to terminate the line side of the magnetics module. This design improves EMI behavior.	The split in ground plane should be at least 50 mils. The split should run under the center of magnetics module. Differential pairs never cross the split.		
	Place 4 to 6 pairs of pads for "stitching" capacitors to bridge the gap from chassis ground to signal ground.	The exact number and values empirically based on EMI performance must be determined.		
LED Circuits	Keep LED traces away from sources of noise (for example, high speed digital traces running in parallel).	LED traces can carry noise into integrated magnetics modules, RJ-45 connectors, or out to the edge of the board, increasing EMI.		

Table 23. 82562EX/GX/GZ Design Checklist

Section	Check Items	Remarks	Done	Comments
General	Have up-to-date product documentation and spec updates.	Documents are subject to frequent change		
	Observe instructions for special pins needing pull-up or pull-down resistors.	Do not connect pull-up or pull-down resistors to any pins marked No Connect, Test, or Reserved.		
Ethernet Device	Connect LCI signals to corresponding signals on ICHx device.			
	Verify LAN disable circuit.	See the related 82562 datasheet.		
	Use a 93C46 EEPROM for non-alerting applications or a 93C66 EEPROM for ASF 1.0.	EEPROM for 82562V attaches to ICH. Add decoupling capacitor. EEPROMs should be rated for at least 1 MHz.		
	Place the Ethernet silicon at least one inch from the edge of the Printed Circuit Board (PCB) and at least one inch from any integrated magnetics module. The trace impedance for the LCI port is 60 Ω.	With closer spacing, fields can follow the surface of the magnetics module or wrap past the edge of the PCB. EMI can increase. Optimum location is approximately one inch behind the magnetics module.		
	Place the transmit LCI termination carefully.	Place the transmit LCI termination close to the ICH. Place the receive LCI termination close to the silicon.		
	Connect RBIAS 10 to ground through a 619 Ω 1% resistor.			
	Connect RBIAS 100 to ground through a 649 Ω 1% resistor.			
Clock Source	Use 25 MHz 30 ppm accuracy @ 25° C clock source. Avoid components that introduce jitter.	Parallel resonant crystals are preferred.		
	Connect two 22 pF load caps to crystal.	Capacitance affects accuracy of the frequency. Must be matched to crystal specs, including estimated trace capacitance in calculation.		
	Place crystal and load capacitors within 0.75 inches from the Ethernet device.	The Ethernet clock plays a key role in EMI.		

Table 23. (Continued) 82562EX/GX/GZ Design Checklist

Section	Check Items	Remarks	Done	Comments
EEPROM and FLASH Memory	Use decoupling capacitor.	Applies to EEPROM or FLASH devices.		
	EEPROM ORG ties to 3.3 V for x16 access.	For Microwire EEPROMs. Depends on EEPROM used.		
	Placement is not critical due to slow signal speeds.	Acceptable to place a few inches away from the Ethernet controller or ICH to provide better spacing of critical components.		
Transmit and Receive Differential Pairs	82562V LCI devices use a 110 Ω +/- 1% termination resistor across Tx+/-.	110 Ω improves transmit return loss.		
	82562V LCI devices use a 110 Ω +/- 1% termination resistor across Rx+/-.	110 Ω improves receives Bit Error Rate (BER).		
	Use short traces.	Keep trace length under four inches from the Ethernet controller through the magnetics to the RJ-45 controller.		
	Avoid highly resistive traces. For example, avoid four mil traces longer than four inches.	If trace length is a problem, use thicker PCB dielectrics to allow wider traces. Thicker copper is even better than wider traces.		
	Make traces symmetric.	Try to match the pairs at pads, vias, and turns. Establish rules carefully for the auto-router. Asymmetry contributes to impedance mismatch.		
	Do not make 90 degree bends.	Bevel corners with turns based on 45 degree angles.		
	Avoid through holes (vias).	If using through holes (vias), the budget is two per trace.		
	Keep traces close together within differential pairs.	Keep within 30 mils regardless of trace geometry.		
	Keep trace-to-trace length difference within each pair to less than 50 mils.	Minimizes signal skew and common mode noise, which reduces radiated EMI. Improves long cable performance. Less than 30 mils is better; and within 10 mils is best.		
	Keep differential pairs 50 mils or more away from each other and away from parallel digital traces.	Minimizes crosstalk and noise injection. 100 mil spacing is better. Guard traces are generally not recommended and would reduce the impedance if done incorrectly.		
	Keep traces away from the PCB edge.	Controls EMI.		
	Avoid unused pads and stubs along the traces.	Use 0 Ω resistors sparingly for dual footprint designs.		

Table 23. (Continued) 82562EX/GX/GZ Design Checklist

Section	Check Items	Remarks	Done	Comments
Transmit and Receive Differential Pairs (continued)	Route traces on layers on appropriate layers.	Run pairs on different layers as needed to improve routing. Use layers adjacent to ground or power layers if possible. Make sure digital signals on adjacent layers cross at 90 degree angles.		
	Place termination resistors (and capacitors if applicable) close to Ethernet device.	Prevents reflections. Use symmetrical pads.		
Magnetics Module	Integrated magnetics modules/RJ-45 connectors are available to minimize space requirements.	Modules with pin compatibility from 10/100 to GbE are available, containing internal jumpers for the unused pairs. Multi-vendor pin compatibility is possible. Contact manufacturers.		
	Qualify magnetics module carefully for Return Loss, Insertion Loss, Open Circuit Inductance, Common Mode Rejection, and Crosstalk Isolation.	Magnetics module is critical to passing IEEE PHY conformance tests and EMI test.		
	For 82562G family LCI devices, use 5-core model.	Auto-transformer models provide better cable termination.		
	For 82562G family LCI devices, use a 0.1 µF capacitor on receive center tap.	Improves BER. DO NOT use for MDI-X mode.		
	Capacitors connected to center taps should be placed very close to Ethernet device.			
	For 82562V LCI devices, do not use capacitor on transmit center tap.	For severe EMI problems, a capacitor up to 22 pF might be used, but is generally not recommended. Larger values will diminish signal strength and fail IEEE PHY conformance.		
Discrete Magnetics Module/RJ-45 Connector Option	Bob Smith termination: use 4 x 75 Ω resistors for cable-side center taps and unused pins.	Terminates pair-to-pair common mode impedance of the CAT5 cable.		
	Bob Smith termination: use an EFT capacitor attached to the termination plane. Suggested values are 1500 pF/2 KV or 1000 pF/3 KV.	For high-voltage isolation, maintain greater than 70 mil spacing from capacitor to traces and components. Round all acute metal-fill angles to remove corners.		
	Connect signal pairs correctly to RJ-45 connector.	The differential pairs use pins 1-2 (Transmit in 10/100), 3-6 (Receive in 10/100), 4-5 (GbE only), and 7-8 (GbE only). Take care not to reverse the polarity.		

Table 23. (Continued) 82562EX/GX/GZ Design Checklist

Section	Check Items	Remarks	Done	Comments
Power Supply and Signal Ground	For 82562G family devices, provide a 3.3 V supply.	82562G family LCI components are single-voltage devices.		
	Design with power supplies that start up properly.	A good guideline is that all voltages should ramp to within their control bands in 20 ms or less. It is desirable that voltages ramp in sequence and that the voltage rise be monotonic.		
	Use planes if possible.	Narrow finger-like planes and very wide traces are allowed.		
	Use auxiliary power supplies.	Necessary to have the Ethernet device wake up from power down states.		
	If using decoupling capacitors on LED lines, place them carefully.	Capacitors on LED lines should be placed near the LEDs.		
	Use decoupling and bulk capacitors generously.	Place decoupling and bulk capacitors close to the Ethernet device, with some along every side, using short, wide traces and large vias. If power is distributed on traces, bulk capacitors should be used at both ends. If power is distributed on cards, bulk capacitors should be used at the connector.		
Chassis Ground	For discrete magnetics board designs: If possible, provide a separate chassis ground "island" to ground the shroud of the RJ-45 connector and to terminate the line side of the magnetics module. This design improves EMI behavior.	Split in ground plane should be at least 50 mils wide. Split should run under center of magnetics module. Differential pairs never cross the split.		
	Place 4-6 pairs of pads for "stitching" capacitors to bridge the gap from chassis ground to signal ground.	Determine the exact number and values empirically based on EMI performance. Expect to populate approximately two capacitor sites.		
Termination Plane	For designs with non-integrated magnetics modules, lay out Bob Smith termination plane. The termination plane floats over chassis ground.	Splits in ground plane should be at least 50 mils to prevent arcing during hi-pot tests.		

Table 23. (Continued) 82562EX/GX/GZ Design Checklist

Section	Check Items	Remarks	Done	Comments
LED Circuits	Basic recommendation is a single green LED for Activity and a dual (bi-color) LED for Speed. Many other configurations are possible.	Two LED configurations are compatible with integrated magnetics modules. For the Link/Activity LED, connect the anode to the ACTLED# pin and the cathode to the LILED# pin. For the bi-color speed LED pair, have the SPDLED# signal drive one end. The other end should be connected to 3.3 V.		
	Connect LEDs to 3.3 V as indicated in reference schematics.	Use 3.3 V AUX for designs supporting wakeup. Consider adding filtering capacitors for extremely noisy situations. Suggested starting value 470 pF.		
	Keep LED traces away from sources of noise, for example, high speed digital traces running in parallel.	LED traces can carry noise into integrated magnetics modules, RJ-45 connectors, or out to the edge of the PCB, increasing EMI.		
	Add current limiting resistors to LED paths.	Typical current limiting resistors are 250-330 ohms when using a 3.3 V supply. Current limiting resistors are typically included with integrated magnetics modules.		
Mfg Test	82562V devices use an XOR Tree Test Access Port.	See the related 82562 datasheet.		

Table 24. 82562EX/GX/GZ Layout Checklist

Section	Check Items	Remarks	Done	Comments
General	Have up-to-date product documentation and spec updates	Documents are subject to frequent change		
	Route the transmit and receive differential traces before routing the digital traces.	Layout of differential traces is critical.		
Ethernet Controller	Place the Ethernet controller at least one inch from the edge of the board (two inches is preferred) and at least one inch from any integrated magnetics module.	With closer spacing, fields can follow the surface of the magnetics module or wrap past edge of board. EMI may increase. Optimum location is approximately one inch behind the magnetics module.		
	For the 82562GZ(GX) PLC device, the trace impedance for the LCI port is 60 Ω.			

Table 24. (Continued) 82562EX/GX/GZ Layout Checklist

Section	Check Items	Remarks	Done	Comments
Ethernet Controller (continued)	For the 82562GZ(GX) PLC device, place the transmit LCI termination carefully.	For the 82562GZ(GX) PLC device, place the transmit LCI termination close to ICH, and place the receive LCI termination close to the 82562GZ(GX) PLC device.		
Clock Source	Place crystal and load capacitors within 0.75 inches from Ethernet controller.	The Ethernet clock plays a key role in EMI.		
EEPROM and FLASH Memory	Placement is not critical due to slow signal speeds.	Okay to place a few inches away from Ethernet controller or ICH to provide better spacing of critical components.		
Transmit and Receive Differential Pairs	Design traces for 110 Ω differential impedance (±20%) for the 82562GZ(GX).	Primary requirement for 10/100 Mb/s Ethernet. Paired 54.9 Ω traces do not make 110 Ω differential. Check impedance calculator.		
	Use short traces.	Keep trace length under four inches from the Ethernet controller through the magnetics to the RJ-45 connector.		
	Avoid highly resistive traces, for example, four mil traces longer than four inches.	If trace length is a problem, use thicker board dielectrics to allow wider traces. Thicker copper is even better than wider traces.		
	Make traces symmetrical.	Try to match the pairs at pads, vias and turns. Establish rules carefully for the autorouter. Asymmetry contributes to impedance mismatch.		
	Do not make 90 degree bends.	Bevel corners with turns based on 45 degree angles.		
	Avoid through holes (vias).	If using through holes (vias), the budget is two per trace.		
	Keep traces close together within differential pairs.	Keep within 30 mils regardless of trace geometry.		
	Keep trace-to-trace length difference within each pair to less than 50 mils.	Minimizes signal skew and common mode noise. Improves long cable performance.		
	Keep differential pairs 100 mils (50 mils for the 82562GZ(GX) or more away from each other and away from parallel digital traces.	Minimizes crosstalk and noise injection. 300 mil (100 mil for the 82562GZ(GX) spacing is better. Guard traces are generally not recommended and will reduce the impedance if done incorrectly.		
	Keep traces away from the board edge.	Controls EMI.		

Table 24. (Continued) 82562EX/GX/GZ Layout Checklist

Section	Check Items	Remarks	Done	Comments
Transmit and Receive Differential Pairs (continued)	Avoid unused pads and stubs along the traces	Use 0 Ω resistors sparingly for dual footprint designs.		
	Route traces on layers on appropriate layers.	Run pairs on different layers as needed to improve routing. Use layers adjacent to ground or power layers if possible. Make sure digital signals on adjacent layers cross at 90 degree angles.		
	Place termination resistors (and capacitors if applicable) close to Ethernet controller.	Prevents reflections. Use symmetrical pads.		
Magnetics Module	Capacitors connected to center taps should be placed very close to magnetics module.			
Power Supply and Signal Ground	Use of power planes is essential for optimized performance of the controller	Narrow finger-like planes and very wide traces are not recommended and a continuous plane should be used.		
	Use decoupling and bulk capacitors generously.	Place decoupling and bulk capacitors close to Ethernet controller, with some along every side, using short, wide traces and large vias. If power is distributed on traces, bulk capacitors should be used at both ends. If power is distributed on cards, bulk capacitors should be used at the connector.		
	If using decoupling capacitors on LED lines, place them carefully.	Capacitors on LED lines should be placed near the LEDs.		

Table 24. (Continued) 82562EX/GX/GZ Layout Checklist

Section	Check Items	Remarks	Done	Comments
Power Supply and Signal Ground (continued)	Bypass the emitter and collector of the external PNP transistors as closely as possible to the body of the transistors.			
	The bypass capacitor at the emitter should be at least 4.7 µF (preferably 10 to 20 µF).	Ceramic X5R or X7R type capacitors should be placed as closely as possible to the body of the transistors.		
	The larger capacitors should be concentrated near the transistor.	Do not disperse the large capacitors in a large area as this can cause instability to the circuit.		
	The high frequency bypass capacitors (0.1 µF X7R capacitors) for the controller should be placed as closely as possible to the corresponding balls.			
	Trace lengths should have around eight mils of width.			
Chassis Ground	If possible, provide a separate chassis ground "island" to ground the shroud of the RJ-45 connector and to terminate the line side of the magnetics module. This design improves EMI behavior.	Split in ground plane should be at least 50 mils. Split should run under center of magnetics module. Differential pairs never cross the split.		
	Place four to six pairs of pads for "stitching" capacitors to bridge the gap from chassis ground to signal ground.	Determine exact number and values empirically based on EMI performance. For 82562GZ(GX) controllers, expect to populate approximately two capacitor sites.		
Termination Plane	For designs with non-integrated magnetics modules, lay out Bob Smith termination plane. Term plane floats over chassis ground.	Splits in ground plane should be at least 50 mils.		
LED Circuits	Keep LED traces away from sources of noise, for example, high speed digital traces running in parallel.	LED traces can carry noise into integrated magnetics modules, RJ-45 connectors, or out to the edge of the board, increasing EMI.		

8.0 Bill of Materials

Note: Allowing for both dedicated and shared configurations in the layout will add 12 0 Ω resistors to the bill of materials.

Note: Using the internal 2.5V regulator reduces the bill of materials by one BCP69-19 PNP, three 0.1 µF capacitors, two 10 µF capacitors, and one 4.7 µF capacitor.

Table 25. Dedicated 82573 NVM

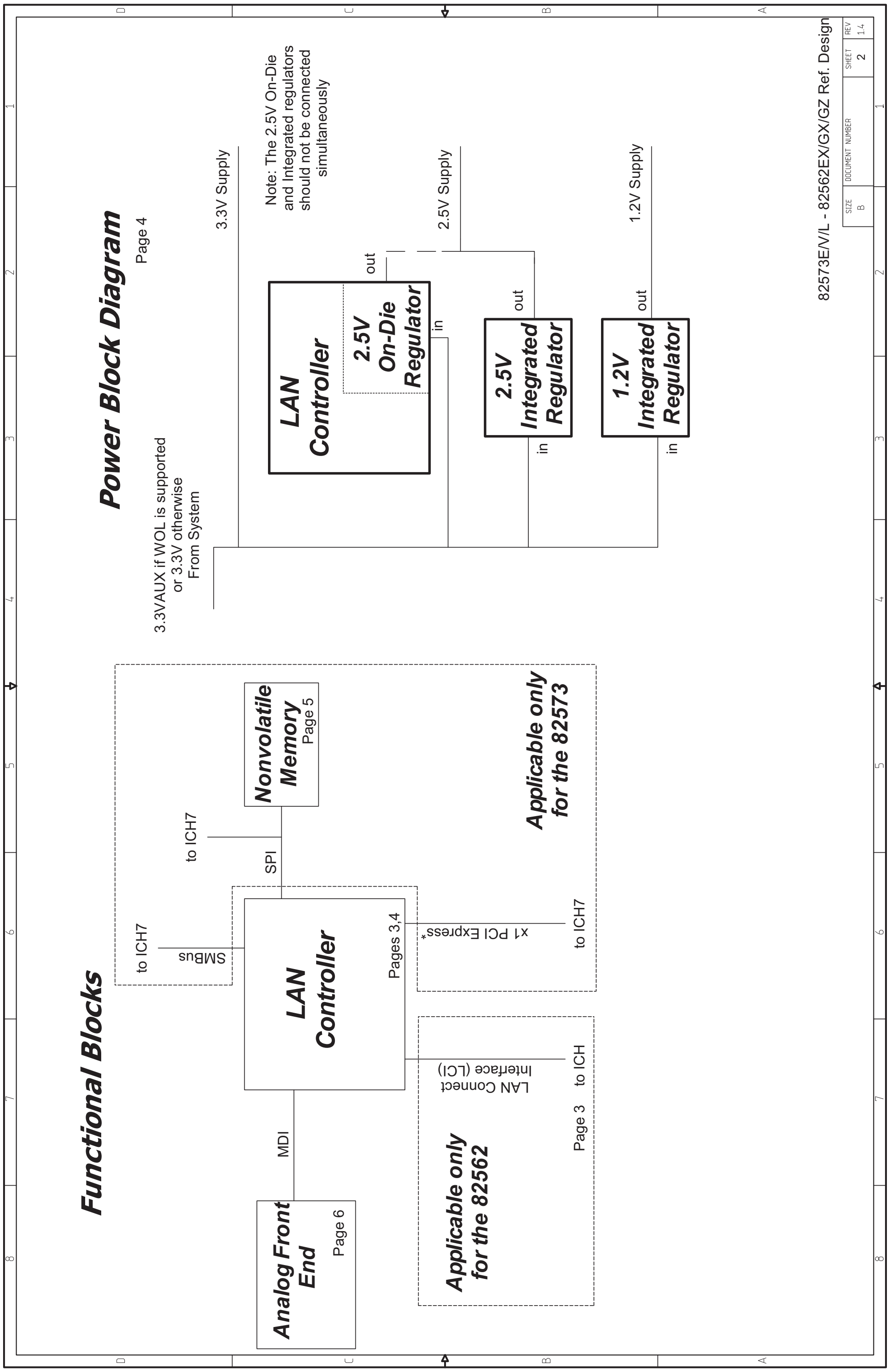
Quantity	Component	Notes
2	0.1 µF X7R 0402 Capacitor	PCIe* AC coupling
7	3.3 KΩ Resistor	Pull-up and pull-down
2	22 pF Capacitor	Crystal load
1	25 MHz, 30 ppm Crystal	
2	0 Ω 0603 Resistor	Supplies
21	0.1 µF Capacitor	Decoupling, MDI
6	4.7 µF Capacitor	Decoupling
5	10 µF Capacitor	Decoupling
2	BCP69-16 PNP	LVR
2	2.0 Ω, 1% Resistor	LVR
1	SPI EEPROM/Flash	NVM
1	10 KΩ Resistor	NVM
3	47 Ω Resistor	NVM
1	4.99 KΩ, 1% Resistor	PHYREF
4	49.9 KΩ, 1% Resistor	MDI
1	Integrated Magnetics Module	
2	470 pF EMC Capacitor	LED

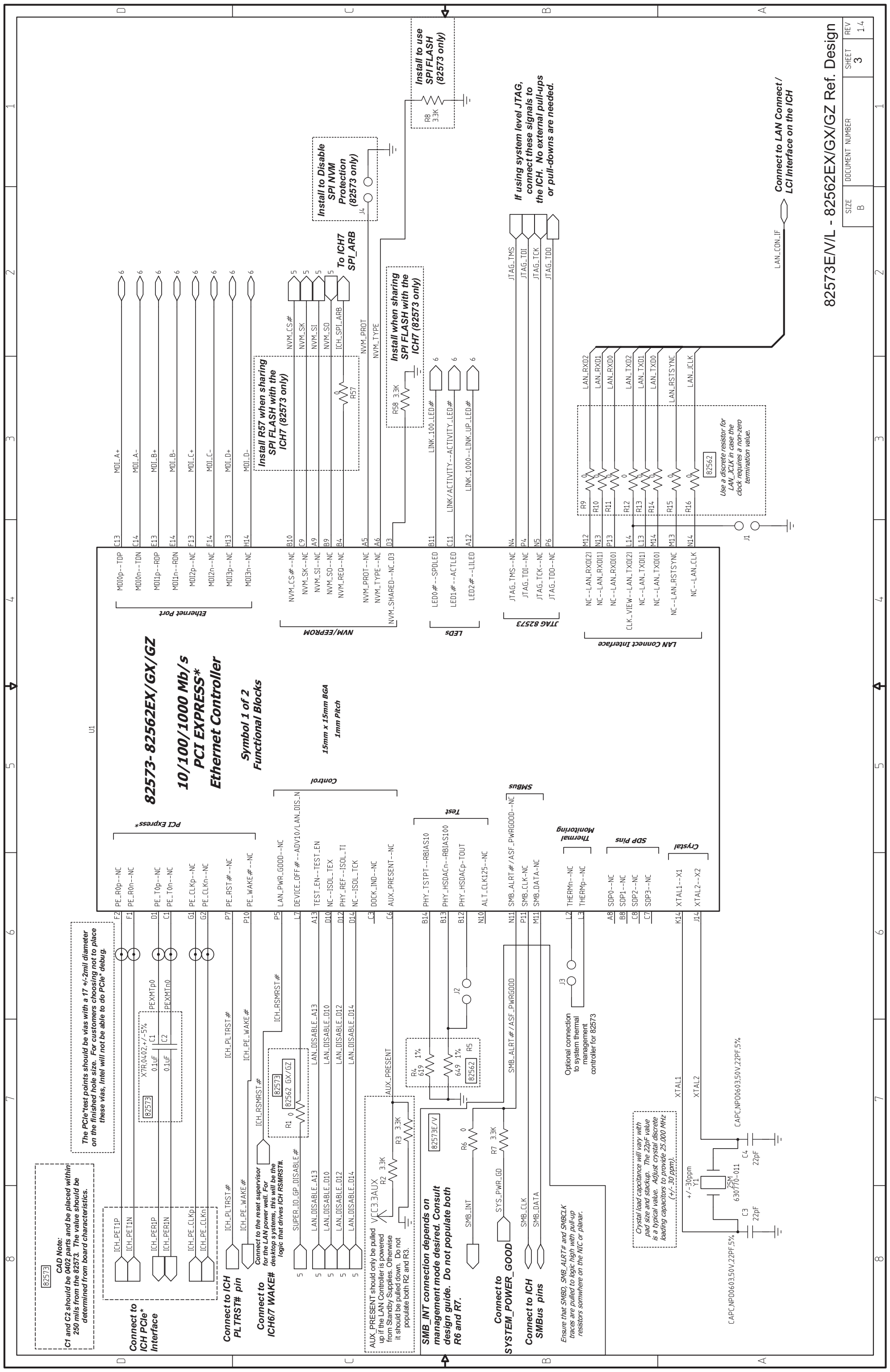
Table 26. Shared 82573 NVM

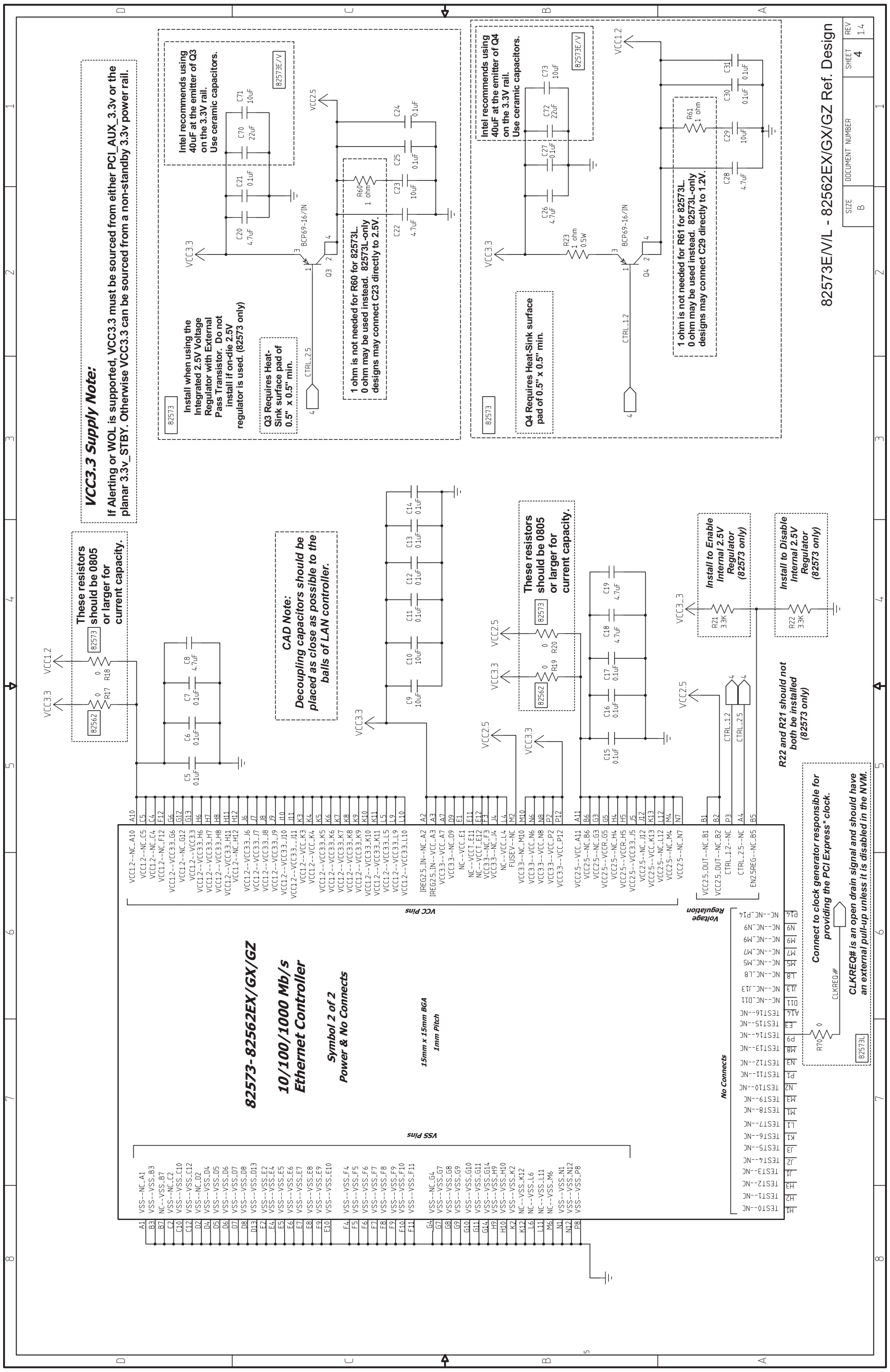
Quantity	Component	Notes
2	0.1 µF X7R 0402 Capacitor	PCIe* AC coupling
5	3.3 KΩ Resistor	Pull-up and pull-down
2	22 pF Capacitor	Crystal load
1	25 MHz, 30 ppm Crystal	
2	0 Ω 0603 Resistor	Supplies
20	0.1 µF Capacitor	Decoupling
6	4.7 µF Capacitor	Decoupling
5	10 µF Capacitor	Decoupling
2	BCP69-16 PNP	LVR
2	2.0 Ω, 1% Resistor	LVR
1	4.99 KΩ, 1% Resistor	PHYREF
4	49.9 KΩ, 1% Resistor	MDI
1	Integrated Magnetics Module	
2	470 pF EMC Capacitor	LED

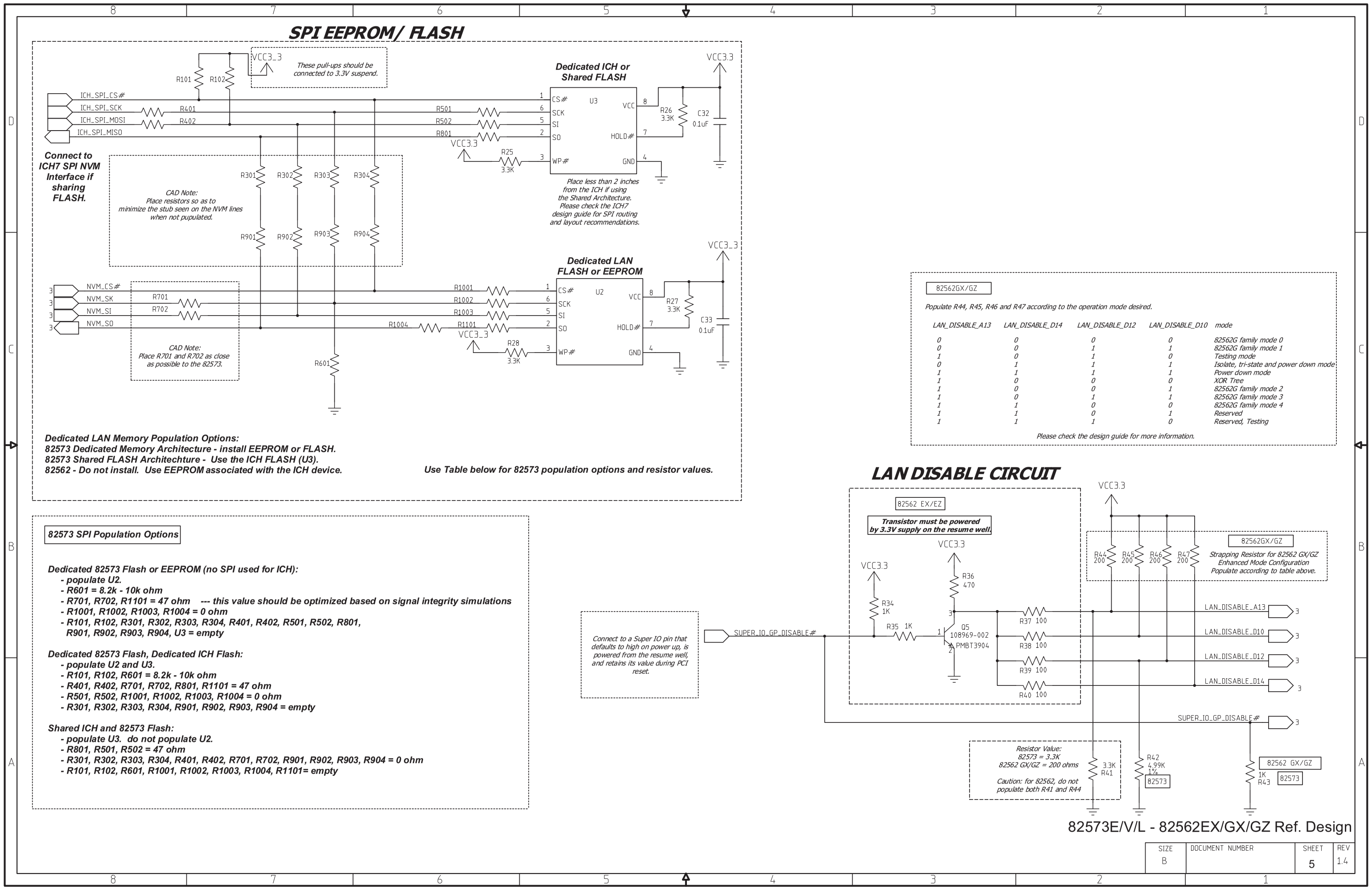
9.0 Reference Schematics

The following pages show a dual footprint design for the 82573E/82573V/82573L GbE Controller and the 82562 Platform LAN Connect device.


Functional Blocks
Analog Front End
Page 6
MDI
LAN Controller
Pages 3,4
SMBus
to ICH7
SPI
to ICH7
Nonvolatile Memory
Page 5
LAN Connect Interface (LCI)
to ICH
Page 3
Applicable only for the 82562
x1 PCI Express*
to ICH7
Applicable only for the 82573
Power Block Diagram
Page 4
3.3VAUX if WOL is supported or 3.3V otherwise From System
3.3V Supply
Note: The 2.5V On-Die and Integrated regulators should not be connected simultaneously
2.5V Supply
1.2V Supply
LAN Controller
2.5V On-Die Regulator
in
out
2.5V Integrated Regulator
in
out
1.2V Integrated Regulator
in
out
82573E/V/L - 82562EX/GX/GZ Ref. Design
SIZE
B
DOCUMENT NUMBER
SHEET
2
REV
1.4
D
C
B
A
1
2
3
4
5
6
7
8


82573E/V/L - 82562EX/GX/GZ Ref. Design
SIZE B
DOCUMENT NUMBER
SHEET 3
REV 1.4
U1
82573- 82562EX/GX/GZ
10/100/1000 Mb/s
PCI EXPRESS*
Ethernet Controller
Symbol 1 of 2
Functional Blocks
15mm x 15mm BGA
1mm Pitch
PCI Express*
Control
Test
SMBus
Thermal Monitoring
SDP Pins
Crystal
Ethernet Port
NVM/EEPROM
LEDs
JTAG 82573
LAN Connect Interface
PE_R0p--NC
PE_R0n--NC
PE_T0p--NC
PE_T0n--NC
PE_CLKp--NC
PE_CLKn--NC
PE_RST#--NC
PE_WAKE#--NC
LAN_PWR_GOOD--NC
DEVICE_OFF#--ADV10/LAN_DIS_N
TEST_EN--TEST_EN
NC--ISOL_TEX
PHY_REF--ISOL_TI
NC--ISOL_TCK
DOCK_IND--NC
AUX_PRESENT--NC
PHY_TSTPT--RBIAS10
PHY_HSDACn--RBIAS100
PHY_HSDACp--TOUT
ALT_CLK125--NC
SMB_ALRT#/ASF_PWRGOOD--NC
SMB_CLK--NC
SMB_DATA--NC
THERMn--NC
THERMp--NC
SDP0--NC
SDP1--NC
SDP2--NC
SDP3--NC
XTAL1--X1
XTAL2--X2
MDI0p--TDP
MDI0n--TDN
MDI1p--RDP
MDI1n--RDN
MDI2p--NC
MDI2n--NC
MDI3p--NC
MDI3n--NC
NVM_CS#--NC
NVM_SK--NC
NVM_SI--NC
NVM_SO--NC
NVM_REQ--NC
NVM_PROT--NC
NVM_TYPE--NC
NVM_SHARED--NC
LED0#--SPDLED
LED1#--ACTLED
LED2#--LILED
JTAG_TMS--NC
JTAG_TDI--NC
JTAG_TCK--NC
JTAG_TDO--NC
NC--LAN_RXD(2)
NC--LAN_RXD(1)
NC--LAN_RXD(0)
CLK_VIEW--LAN_TXD(2)
NC--LAN_TXD(1)
NC--LAN_TXD(0)
NC--LAN_RSTSYNC
NC--LAN_CLK
MDI_A+
MDI_A-
MDI_B+
MDI_B-
MDI_C+
MDI_C-
MDI_D+
MDI_D-
NVM_CS#
NVM_SK
NVM_SI
NVM_SO
ICH_SPI_ARB
NVM_PROT
NVM_TYPE
LINK_100_LED#
LINK/ACTIVITY--ACTIVITY_LED#
LINK_1000--LINK_UP_LED#
JTAG_TMS
JTAG_TDI
JTAG_TCK
JTAG_TDO
LAN_RXD2
LAN_RXD1
LAN_RXD0
LAN_TXD2
LAN_TXD1
LAN_TXD0
LAN_RSTSYNC
LAN_JCLK
LAN_CON_JF
Install R57 when sharing SPI FLASH with the ICH7 (82573 only)
R57
To ICH7 SPI_ARB
Install when sharing SPI FLASH with the ICH7 (82573 only)
R58 3.3K
Install to Disable SPI NVM Protection (82573 only)
J4
Install to use SPI FLASH (82573 only)
R8 3.3K
If using system level JTAG, connect these signals to the ICH. No external pull-ups or pull-downs are needed.
Connect to LAN Connect / LCI Interface on the ICH
R9 R10 R11 R12 R13 R14 R15 R16
82562
Use a discrete resistor for LAN_JCLK in case the clock requires a non-zero termination value.
J1
CAD Note:
82573
C1 and C2 should be 0402 parts and be placed within 250 mils from the 82573. The value should be determined from board characteristics.
The PCIe*test points should be vias with a 17 +/-2mil diameter on the finished hole size. For customers choosing not to place these vias, Intel will not be able to do PCIe* debug.
ICH_PETIP
ICH_PETIN
ICH_PERIP
ICH_PERIN
ICH_PE_CLKp
ICH_PE_CLKn
PEXMTp0
PEXMTn0
XTR_0402,+/-5%
C1 0.1uF
C2 0.1uF
Connect to ICH PCIe* Interface
ICH_PLTRST#
Connect to ICH PLTRST# pin
ICH_PE_WAKE#
Connect to ICH6/7 WAKE#
Connect to the reset supervisor for the LAN power well. For desktop systems, this will be the logic that drives ICH RSMRST#.
ICH_RSMRST#
R1 0
82562 GX/GZ
82573
SUPER_IO_GP_DISABLE#
LAN_DISABLE_A13
LAN_DISABLE_D10
LAN_DISABLE_D12
LAN_DISABLE_D14
VCC3_3AUX
R2 3.3K
R3 3.3K
AUX_PRESENT
AUX_PRESENT should only be pulled up if the LAN Controller is powered from Standby Supplies. Otherwise it should be pulled down. Do not populate both R2 and R3.
R4 619 1%
R5 649 1%
J2
82573E/V
R6 0
R7 3.3K
SMB_INT
SMB_INT connection depends on management mode desired. Consult design guide. Do not populate both R6 and R7.
SYS_PWR_GD
Connect to SYSTEM_POWER_GOOD
SMB_ALRT#/ASF_PWRGOOD
SMB_CLK
SMB_DATA
Connect to ICH SMBus pins
Ensure that SMBD, SMB_ALRT# and SMBCLK traces are pulled to logic high with pull-up resistors somewhere on the NIC or planar.
J3
Optional connection to system thermal management controller for 82573
XTAL1
XTAL2
Y1 25M 630770-011
+/-30ppm
C3 22pF
C4 22pF
CAPCNP0603.50V.22PF.5%
Crystal load capacitance will vary with pad size and stackup. The 22pF value is a typical value. Adjust crystal discrete loading capacitors to provide 25.000 MHz (+/- 30 ppm).
A B C D
1 2 3 4 5 6 7 8


VCC3.3 Supply Note:
If Alerting or WOL is supported, VCC3.3 must be sourced from either PCI_AUX_3.3v or the planar 3.3v_STBY. Otherwise VCC3.3 can be sourced from a non-standby 3.3v power rail.
These resistors should be 0805 or larger for current capacity.
82562
82573
VCC3.3
VCC1.2
R17 0
R18 0
C5 0.1uF
C6 0.1uF
C7 0.1uF
C8 4.7uF
CAD Note:
Decoupling capacitors should be placed as close as possible to the balls of LAN controller.
C9 10uF
C10 10uF
C11 0.1uF
C12 0.1uF
C13 0.1uF
C14 0.1uF
These resistors should be 0805 or larger for current capacity.
VCC2.5
R19 0
R20 0
C15 0.1uF
C16 0.1uF
C17 0.1uF
C18 4.7uF
C19 4.7uF
Install to Enable Internal 2.5V Regulator (82573 only)
R21 3.3K
Install to Disable Internal 2.5V Regulator (82573 only)
R22 3.3K
R22 and R21 should not both be installed (82573 only)
CTRL_12
CTRL_25
Install when using the Integrated 2.5V Voltage Regulator with External Pass Transistor. Do not install if on-die 2.5V regulator is used. (82573 only)
Q3 Requires Heat-Sink surface pad of 0.5" x 0.5" min.
Intel recommends using 40uF at the emitter of Q3 on the 3.3V rail. Use ceramic capacitors.
82573E/V
C20 4.7uF
C21 0.1uF
C70 22uF
C71 10uF
Q3 BCP69-16/INF
R60 1 ohm
1 ohm is not needed for R60 for 82573L. 0 ohm may be used instead. 82573L-only designs may connect C23 directly to 2.5V.
C22 4.7uF
C23 10uF
C24 0.1uF
C25 0.1uF
Q4 Requires Heat-Sink surface pad of 0.5" x 0.5" min.
Intel recommends using 40uF at the emitter of Q4 on the 3.3V rail. Use ceramic capacitors.
C26 4.7uF
C27 0.1uF
C72 22uF
C73 10uF
R23 1 ohm 0.5W
Q4 BCP69-16/INF
R61 1 ohm
1 ohm is not needed for R61 for 82573L. 0 ohm may be used instead. 82573L-only designs may connect C29 directly to 1.2V.
C28 4.7uF
C29 10uF
C30 0.1uF
C31 0.1uF
82573-82562EX/GX/GZ
10/100/1000 Mb/s Ethernet Controller
Symbol 2 of 2
Power & No Connects
15mm x 15mm BGA
1mm Pitch
VCC Pins
VSS Pins
Voltage Regulation
No Connects
CLKREQ#
R70 0
82573L
Connect to clock generator responsible for providing the PCI Express* clock.
CLKREQ# is an open drain signal and should have an external pull-up unless it is disabled in the NVM.
82573E/V/L - 82562EX/GX/GZ Ref. Design
SIZE B
DOCUMENT NUMBER
SHEET 4
REV 1.4
A
B
C
D
1
2
3
4
5
6
7
8



These pull-ups should be connected to 3.3V suspend.

Dedicated ICH or Shared FLASH

Place less than 2 inches from the ICH if using the Shared Architecture. Please check the ICH7 design guide for SPI routing and layout recommendations.

Connect to ICH7 SPI NVM Interface if sharing FLASH.

CAD Note:
Place resistors so as to minimize the stub seen on the NVM lines when not pupulated.

Dedicated LAN FLASH or EEPROM

CAD Note:
Place R701 and R702 as close as possible to the 82573.

Dedicated LAN Memory Population Options:
82573 Dedicated Memory Architecture - install EEPROM or FLASH.
82573 Shared FLASH Architechture - Use the ICH FLASH (U3).
82562 - Do not install. Use EEPROM associated with the ICH device.

Use Table below for 82573 population options and resistor values.

82573 SPI Population Options

Dedicated 82573 Flash or EEPROM (no SPI used for ICH):
- **populate U2.**
- **R601 = 8.2k - 10k ohm**
- **R701, R702, R1101 = 47 ohm --- this value should be optimized based on signal integrity simulations**
- **R1001, R1002, R1003, R1004 = 0 ohm**
- **R101, R102, R301, R302, R303, R304, R401, R402, R501, R502, R801, R901, R902, R903, R904, U3 = empty**

Dedicated 82573 Flash, Dedicated ICH Flash:
- **populate U2 and U3.**
- **R101, R102, R601 = 8.2k - 10k ohm**
- **R401, R402, R701, R702, R801, R1101 = 47 ohm**
- **R501, R502, R1001, R1002, R1003, R1004 = 0 ohm**
- **R301, R302, R303, R304, R901, R902, R903, R904 = empty**

Shared ICH and 82573 Flash:
- **populate U3. do not populate U2.**
- **R801, R501, R502 = 47 ohm**
- **R301, R302, R303, R304, R401, R402, R701, R702, R901, R902, R903, R904 = 0 ohm**
- **R101, R102, R601, R1001, R1002, R1003, R1004, R1101= empty**

82562GX/GZ

Populate R44, R45, R46 and R47 according to the operation mode desired.

LAN_DISABLE_A13	LAN_DISABLE_D14	LAN_DISABLE_D12	LAN_DISABLE_D10	mode
0	0	0	0	82562G family mode 0
0	0	1	1	82562G family mode 1
1	0	1	0	Testing mode
0	1	1	1	Isolate, tri-state and power down mode
1	1	1	1	Power down mode
1	0	0	0	XOR Tree
1	0	0	1	82562G family mode 2
1	0	1	1	82562G family mode 3
1	1	0	0	82562G family mode 4
1	1	0	1	Reserved
1	1	1	0	Reserved, Testing

Please check the design guide for more information.

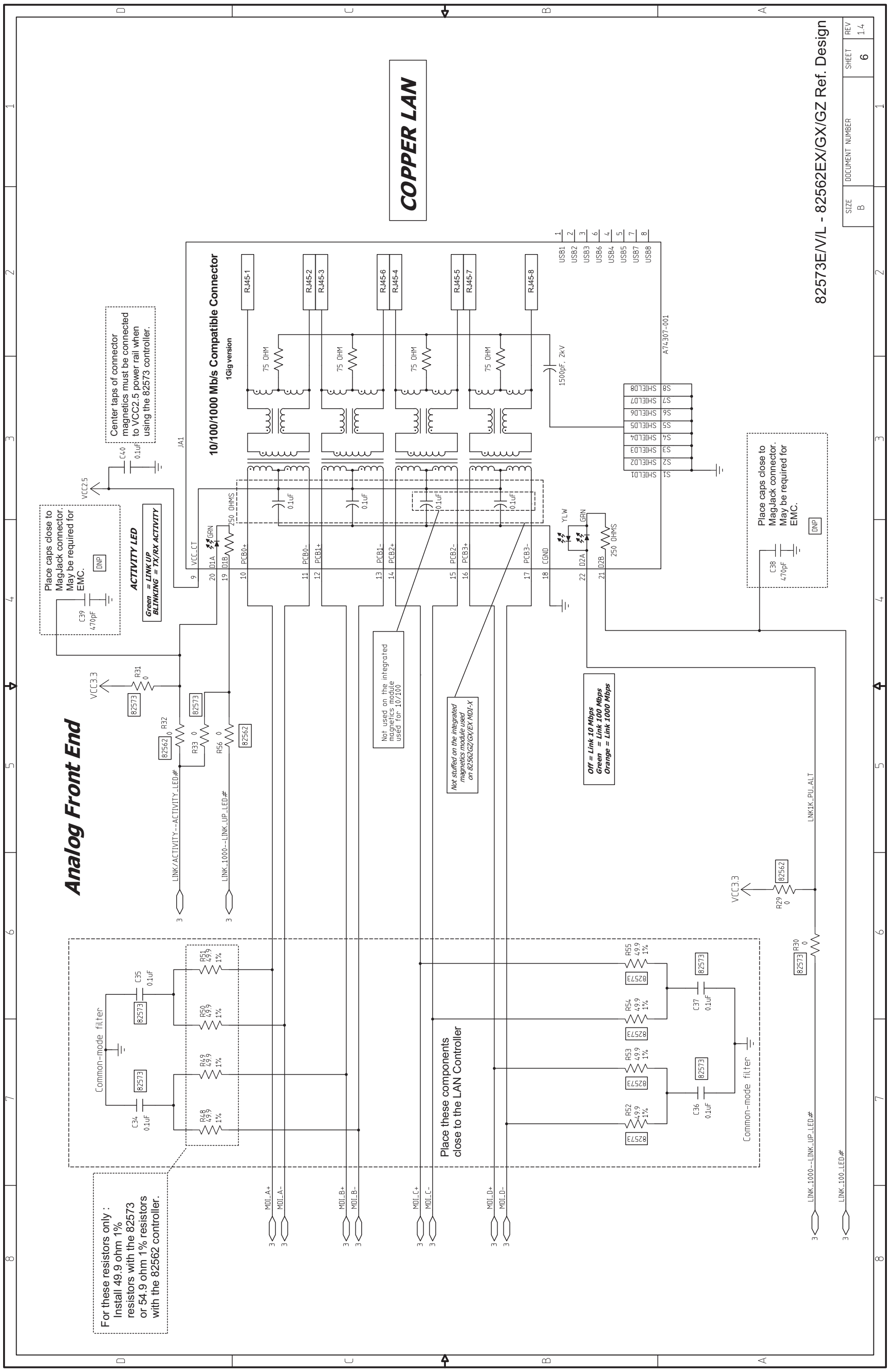
Transistor must be powered by 3.3V supply on the resume well.

Strapping Resistor for 82562 GX/GZ Enhanced Mode Configuration Populate according to table above.

Connect to a Super IO pin that defaults to high on power up, is powered from the resume well, and retains its value during PCI reset.

Resistor Value:
82573 = 3.3K
82562 GX/GZ = 200 ohms

Caution: for 82562, do not populate both R41 and R44


COPPER LAN
Analog Front End
10/100/1000 Mb/s Compatible Connector
1Gig version
JA1
Center taps of connector magnetics must be connected to VCC2.5 power rail when using the 82573 controller.
Place caps close to MagJack connector. May be required for EMC.
DNP
ACTIVITY LED
Green = LINK UP
BLINKING = TX/RX ACTIVITY
Off = Link 10 Mbps
Green = Link 100 Mbps
Orange = Link 1000 Mbps
Not used on the integrated magnetics module used for 10/100
Not stuffed on the integrated magnetics module used on 82562GZ/GX/EX MDI-X
Place these components close to the LAN Controller
For these resistors only : Install 49.9 ohm 1% resistors with the 82573 or 54.9 ohm 1% resistors with the 82562 controller.
Common-mode filter
VCC2.5
VCC3.3
C40 0.1uF
C39 470pF
C38 470pF
C34 0.1uF
C35 0.1uF
C36 0.1uF
C37 0.1uF
R31 0
R32 0
R33 0
R56 0
R29 0
R30 0
R48 49.9 1%
R49 49.9 1%
R50 49.9 1%
R51 49.9 1%
R52 49.9 1%
R53 49.9 1%
R54 49.9 1%
R55 49.9 1%
82573
82562
250 OHMS
75 OHM
1500pF, 2kV
0.1uF
GRN
YLW
9 VCC_CT
20 D1A
19 D1B
10 PCB0+
11 PCB0-
12 PCB1+
13 PCB1-
14 PCB2+
15 PCB2-
16 PCB3+
17 PCB3-
18 CGND
22 D2A
21 D2B
RJ45-1
RJ45-2
RJ45-3
RJ45-6
RJ45-4
RJ45-5
RJ45-7
RJ45-8
USB1 1
USB2 2
USB3 3
USB6 6
USB4 4
USB5 5
USB7 7
USB8 8
S1 SHIELD1
S2 SHIELD2
S3 SHIELD3
S4 SHIELD4
S5 SHIELD5
S6 SHIELD6
S7 SHIELD7
S8 SHIELD8
A74307-001
LINK/ACTIVITY~ACTIVITY_LED#
LINK_1000~LINK_UP_LED#
LNKIK_PU_ALT
LINK_1000~LINK_UP_LED#
LINK_100_LED#
MDI_A+
MDI_A-
MDI_B+
MDI_B-
MDI_C+
MDI_C-
MDI_D+
MDI_D-
3
82573E/V/L - 82562EX/GX/GZ Ref. Design
SIZE B
DOCUMENT NUMBER
SHEET 6
REV 1.4
A
B
C
D
1
2
3
4
5
6
7
8