Intel® 82566 Schematic Checklist (version 1.2)

NOTE: Do not use with dual footprint designs.

Project Name	
Fab Revision	
Date	
Designer	
Intel Contact	
Reviewer	

SECTION	CHECK ITEMS	REMARKS	√ DONE	COMMENTS
General	Obtain the most recent documentation and specification updates.	Documents are subject to frequent change.		
	Observe instructions for special pins needing pull-up or pull-down resistors.	Do not connect pull-up or pull-down resistors to any pins marked No Connect, Test, or Reserved.		
GLCI Interface	Connect GLCI interface pins to corresponding pins on the ICH8 and ICH9.			
	Connect GLAN_RXP (pin J4) to PETp6/GLAN_TXp on ICH8 (pin B27) or on ICH9 (pin E28).	Correct polarity is mandatory, the GLCI interface does not support polarity correction.		
	Connect GLAN_RXN (pin H4) to PETn6/GLAN_TXn on ICH8 (pin B28) or on ICH9 (pin E26).			
	Connect GLAN_TXP (pin H2) to PERp6/GLAN_RXp on ICH8 (pin C25) or on ICH9 (pin D30).			
	Connect GLAN_TXN (pin J2) to PERn6/GLAN_RXn on ICH8 (pin C26) or on ICH9 (pin D29).			
	All GLCI interface AC coupling capacitors are 0.1 µF, Y5V dielectric.	Use only 0.1 µF Y5V capacitors on the GLCI interface. Recommend 0402 package size; however, 0603 is acceptable.		
		There are a total of 4 coupling capacitors for the 82566.		
LCI Interface	Connect LCI interface pins to corresponding pins on the ICH8 and ICH9.			
	Connect JTXD[2:0] to LAN_TXD[2:0] on the ICH.	The 82566 JTXD pins are inputs and the ICH LAN_TXD pins are outputs.		
	Connect RTXD[2:0] to LAN_RXD[2:0] on the ICH.	The 82566 JRXD pins are inputs and the ICH LAN_RXD pins are outputs.		
Reset/Clock Signals	JKCLK connects to GLAN_CLK on the ICH through a 33 Ω, 5% series resistor.	The 33 Ω series resistor is required for all lengths of clock trace. Failure to use a series terminating resistor results in signal integrity issues such as overshoot and ringing.		
	Connect JRSTSYNC to LAN_RSTSYNC on the ICH.	Required for normal operation.		
Clock Source	Use 25 MHz 30 ppm accuracy @ 25 °C clock source. Avoid components that introduce jitter.	Parallel resonant crystals are required. The load capacitance (Cload) should be 20 pF. Specify Equivalent Series Resistance (ESR) to be 50 Ω or less.		
Clock Source (continued)		Capacitance affects accuracy of the frequency. Must be matched to crystal specifications stated in the datasheet, including estimated trace and pin capacitance.		

	Connect two load capacitors to the crystal; one on XTAL1 and one on XTAL2. Use 27 pF 0402 capacitors.	Use capacitors with low ESR. Refer to the *Intel 965 Express Chipset Family Platform Design Guide* for more details.		
		The two load capacitors, crystal component, the 82566, and the crystal circuit traces must all be located on the same side of the PCB (maximum of one via-to-ground load capacitor on each XTAL trace). Refer to Technical Advisory TA-181 for more details.		
	Connect a 30-ohm (5% tolerance) 0402 series resistor on XTAL2	The location of the resistor along the XTAL2 trace is flexible, as long as it is between the load capacitor and the 82566.		
LAN Controller	Connect TEST_EN to GND with a 100 Ω resistor.	Required for normal operation.		
	Connect RBIAS_P to GND with a 1.4 KΩ resistor.	A 1% tolerance resistor is required for IEEE compliance of the PHY.		
	Connect RBIAS_N to GND.	Required for normal operation.		
	Connect KBIAS_P to KBIAS_N with a 1.4 KΩ, 1% tolerance resistor.	Required for normal operation.		
	Verify IEEE_TEST_P and IEEE_TEST_N signals have a test header.	Use a two-pin header to access the clock required for IEEE GbE PHY conformance testing.		
		Connect one pin on the header to the IEEE_TEST_P and the other pin to IEEE_TEST_N.		
		For production applications, all test points can be deleted and signal can be left unconnected.		
	All reserved signals should not be connected on the board.	Required for normal operation.		
		RESERVED_A6, RESERVED_B5, RESERVED_C5, RESERVED_J6, and RESERVED_J7 can have test points for board manufacturing test coverage.		
MDI Transmit and Receive Differential Pairs	For 10/100/1000 Base-T applications, the 82566 controller uses pairs of 49.9 Ω termination resistors with 0.1 μF capacitors attached between center nodes and ground	This applies to all four differential pairs of each port.		
	Connect MDI signal pairs correctly to the RJ-45 connector.	The differential pairs must be mapped as follows: MDI_PLUS[0] - RJ-45 pin 1, MDI_MINUS[0] - RJ-45 pin 2, MDI_PLUS[1] - RJ-45 pin 3, MDI_MINUS[1] - RJ-45 pin 6, MDI_PLUS[2] - RJ-45 pin 4, MDI_MINUS[2] - RJ-45 pin 5, MDI_PLUS[3] - RJ-45 pin 7, MDI_MINUS[3] - RJ-45 pin 8.		
	Place the magnetics module between the silicon and the RJ-45.	Applies to designs using discrete magnetics modules.		
Magnetics Module	If applicable, use integrated magnetics modules/RJ-45 connectors to minimize space requirements	Multivendor pin compatibility is possible. The *Intel 965 Express Chipset Family Platform Design Guide* provides further details on recommended models and manufacturers.		
	Qualify magnetics module carefully for Return Loss, Insertion Loss, Open Circuit Inductance, Common Mode Rejection, and Crosstalk Isolation	Magnetics module is critical to passing IEEE PHY conformance tests and EMI test		

	Supply 1.8V to the silicon side of the transformer center taps and use a 0.1μF bypass capacitor on every center tap pin (silicon side) of the magnetics module.	The 82566 requires 1.8V power on the MDI magnetic center taps for normal operation.		
		Magnetics with four center tap pins may have better characteristics than those with 1-2 center tap pins. Capacitors with low ESR should be used.		
Power Supply and Signal Ground	Connect the base of the external PNP transistor for the VCCLAN_1P8 supply to the regulator control CTRL_18 output.	Follow the reference schematic and do not substitute components. The connections and transistor parameters are critical. Use only BCP69 bipolar transistors listed in the *Intel 965 Express Chipset Family Platform Design Guide* .		
		If the 1.8V internal voltage regulator control circuit is not used, leave the CTRL_18 pin as a no connect and provide a 1.8V supply which meets the criteria specified in the datasheet.		
		Check with your Intel representative for last minute circuit changes.		
	Connecting the CTRL_10 signal depends on the desired regulator mode.	Follow the reference schematic and do not substitute components. The connections and transistor parameters are critical. Use only BCP69 bipolar transistors listed in the *Intel 965 Express Chipset Family Platform Design Guide* .		
		Internal VR, discrete (IVRd): Connect the base of the external PNP transistor for the VCCLAN_1P0 supply to the regulator control CTRL_10 output.		
		Internal VR, on-die (IVRi): Leave the CTRL_10 signal as a no connect.		
		External VR: If the 1.0V internal voltage regulator control circuit is not used, leave the CTRL_10 pin as a no connect and provide a 1.0V supply which meets the criteria specified in the datasheet.		
		Check with your Intel representative for last minute circuit changes.		
	Connecting the emitter on the VCCLAN_1P8 supply PNP transistor depends on the desired regulator mode.	An auxiliary power supply is required to support the 82566 wake up from power down states.		
		Internal VR, discrete (IVRd): Connect the emitter of the VCCLAN_1P8 external PNP transistor to the VCCAUX3_3 supply directly. No resistor is required.		
		Internal VR, on-die (IVRi): Connect the emitter of the VCCLAN_1P8 external PNP transistor to the VCCAUX3_3 supply through a resistor. It can either be one 0.68 Ω, 5%, 1 W resistor or two 1.4 Ω, 5%, 1/2 W resistors in parallel. The resistor connection is required to meet the thermal limits of the transistor when using the on-die regulator.		
		The resistor must be in the emitter path, not the collector path for the regulator to operate normally.		

	Connecting the emitter on the VCCLAN_1P0 supply PNP transistor depends on the desired regulator mode.	An auxiliary power supply is required to support the 82566 wake up from power down states.		
		Internal VR, discrete (IVRd): Connect the emitter of the VCCLAN_1P0 external PNP transistor to the VCCAUX3_3 supply directly. No resistor is required.		
Power Supply and Signal Ground (continued)	Connecting the emitter on the VCCLAN_1P0 supply PNP transistor depends on the desired regulator mode.	**Internal VR, on-die (IVRi):** External PNP transistor is not installed.		
	Use decoupling and bulk capacitors generously.	The minimum acceptable decoupling by power supply is as follows (not including decoupling at magnetic): **VCCAUX3_3:** One 4.7 µF One 0.1 µF **VCCLAN_1P8:** One 10 mF X5R, Two 2 4.7µF Y5V, Two 0.1 µF Two 470 pF **VCCLAN_1P0:** One 10 µF X5R, Two 4.7 µF Y5V, Two 0.1 µF One 470 pF If power is distributed on traces, bulk capacitors should be used at both ends.		
	Connect VCC3P3 pin B3 and pin F2 to a 3.3V supply.	VCC3P3 pin B3 and pin F2 must be connected to a 3.3V +/-10% supply for normal operation. An auxiliary power supply is required to support the 82566 wake up from power down states.		
	Connecting V1P0_OUT depends on the desired regulator mode.	**External VR:** The V1P0_OUT signal is not used. Connect V1P0_OUT (ball B1) to the VCCLAN_1P8 supply directly for normal operation.		
		Internal VR, discrete (IVRd): The V1P0_OUT signal is not used. Connect V1P0_OUT (ball B1) to the VCCLAN_1P8 supply directly for normal operation.		
		Internal VR, on-die (IVRi): The V1P0_OUT signal is an output of the on-die regulator and provides current to the 82566 via the motherboard. Connect V1P0_OUT (ball B1) directly to the VCCLAN_1P0 supply.		
	Connect VCCFC1P0 (pin H3) to the VCCLAN_1P0 supply	Required for normal operation.		

	Connect VCCF1P0 (pin E5) to the VCCLAN_1P0 supply	Required for normal operation.		
Power Supply and Signal Ground (continued)	For the 82566 when using external LVRs: Designs must comply with power sequencing requirements to avoid latch-up and forward-biased internal diodes. Refer to the datasheet for more information. For power down, there is no requirement (the only charge that remains is stored in the decoupling capacitors).			
Stability Capacitors	Connect the stability capacitor on the CTRL_18 signal.	**Internal VR, discrete (IVRd):** Connect a 10nF X5R capacitor between the CTRL_18 output and the emitter of the PNP generating the VCCLAN_1P8 supply.		
		Internal VR, on-die (IVRi): Connect a 10nF X5R capacitor between the CTRL_18 output and the emitter of the PNP generating the VCCLAN_1P8 supply.		
	Connect the stability capacitor on the CTRL_10 signal.	**Internal VR, discrete (IVRd):** Connect a 10nF X5R capacitor between the CTRL_10 output and the emitter of the PNP generating the VCCLAN_1P0 supply.		
		Internal VR, on-die (IVRi): Leave the CTRL_10 signal as a no connect. If the 1.0V internal voltage regulator control circuit is not used, leave the CTRL_10 pin as a no connect and provide a 1.0V supply which meets the criteria specified in the datasheet.		
Chassis Ground (10/100/1000 Base-T applications)	If possible, provide a separate chassis ground to connect the shroud of the RJ-45 connector and to terminate the line side of the magnetics module.	This design technique decreases EMI of magnetics without integrated USB. Place pads for approximately four “stitching” capacitors to bridge the gap from chassis ground to signal ground. Typical values range from 0.1μF to 4.7μF. Determine experimentally. Do not use a separate chassis ground when using magnetics with integrated USB. The split ground might increase the EMI of the USB signals or cause energy to couple from the USB interface to the Ethernet cable.		
LED Circuits	Add sites for capacitors on LED lines.	Use 3.3V AUX for designs supporting wake-up. Add approximately one capacitor site per LED for EMI. Suggested starting value is 470 pF. Determine experimentally.		

	Add current limiting resistors to LED paths, if required.	Typical current limiting resistors are 250 to 330 Ω when using a 3.3V supply. Current limiting resistors are typically included with integrated magnetics modules.		
LED Circuits (continued)	Verify LED connections provide desired behavior.	By default, the LED signals on the 82566 are as follows: LED0: LINK/ACTIVITY LED1: 1000 Mb Link LED2: 100 Mb Link LED pins are active low signals by default and are typically connected to the cathode of the LED. LED behavior and polarity is configurable through the ICH8 or ICH9 NVM settings. Refer to the appropriate NVM Map and Programming Information Guide for more information.		
Mfg Test	82566 uses a 3.3V JTAG Test Access Port.	The TAP controller uses an internal reset instead of an external pin.		
	JTAG_TMS and JTAG_TDI are no connects.	JTAG_TMS and JTAG_TDI have internal pull-ups and do not require any external pull-up resistors. The JTAG pins do not require connections unless the platform is using a JTAG scan chain.		