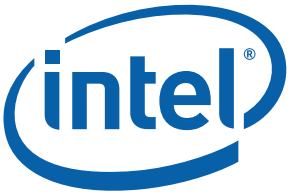

Intel® 6 Series Chipset and Intel® C200 Series Chipset

Specification Update

August 2011

Notice: Intel® 6 Series Chipsets and Intel® C200 Series Chipsets may contain design defects or errors known as errata which may cause the product to deviate from published specifications. Current characterized errata are documented in this specification update.

Document Number: 324646-008

Contents

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Revision History

Revision	Description	Date
001	• Initial Release	January 2011
002	• Updated Top Markings • Updated for B3 Rev ID • Added Errata 14: SATA Ports 2-5 Issue	February 2011
003	• Updated Top Markings • Updated PCH Device and Revision Identification	February 2011
004	• Added Intel® Q65 Chipset to Top Markings and PCH Device and Revision Identification • Added Specification Change 1: Intel Q65 SKU Addition	April 2011
005	• Removed Specification Change 1 that went into Datasheet rev 003 • Added Intel® C200 Series Chipsets to Top Markings, PCH Device and Revision Identification, and Errata.	April 2011
006	• Added Intel® Z68 Chipset to Top Markings and PCH Device and Revision Identification.	May 2011
007	• Updated: Errata 12 • Added: Errata 15: Intel® ME Clock Throttling Failure Causes Hang	July 2011
008	• Updated: PCH Device and Revision Identification • Updated: Errata 12 and USB terminology changed for consistency on various errata. • Added: Errata 16: USB Full-/low-speed Port Reset or Clear TT Buffer Request and 17: Intel® 82579 Gigabit Ethernet Controller Transmission Issue • Added: Specification Change 1: LED Locate Intel® Rapid Storage Technology Capability Removal • Added Specification Clarification: 1: Device 31 Function 6 Disable Bit, 2: LAN Disable Reset, 3: SGPIO Signal Usage, 4: RTCRST# and SRTCRST# Clarification, 5: PPM of 25 MHz Option for CLKOUTFLEX2, 6: SATA Alternate ID Enable Definition Update, 7: SATA Hot Plug Operation, 8: GPIO13 Voltage Tolerance, and 9: EHCI Configuration Programming • Added Documentation Changes: 1: Addition of LPC Capability List Pointer Register, 2: Intel® Smart Response Technology Functional Description Updates, 3: Addition of Legacy ATA Backwards Compatibility Registers, 4: DMI L1 Exit Latency Documentation Change, 5: Device 30 Function 0 Naming Consistency Change, 6: Gigabit Ethernet Capabilities and Status Registers Additions, 7: Measured ICC Corrections, and 8: Miscellaneous Documentation Corrections	August 2011

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Preface

This document is an update to the specifications contained in the Affected Documents/Related Documents table below. This document is a compilation of device and documentation errata, specification clarifications and changes. It is intended for hardware system manufacturers and software developers of applications, operating systems, or tools.

Information types defined in Nomenclature are consolidated into the specification update and are no longer published in other documents.

This document may also contain information that was not previously published.

Affected Documents/Related Documents

Title	Document Number
Intel® 6 Series Chipset and Intel® C200 Series Chipset Datasheet	324645-006

Nomenclature

Errata are design defects or errors. Errata may cause the behavior of the PCH to deviate from published specifications. Hardware and software designed to be used with any given stepping must assume that all errata documented for that stepping are present in all devices.

Specification Changes are modifications to the current published specifications. These changes will be incorporated in any new release of the specification.

Specification Clarifications describe a specification in greater detail or further highlight a specification's impact to a complex design situation. These clarifications will be incorporated in any new release of the specification.

Documentation Changes include typos, errors, or omissions from the current published specifications. These will be incorporated in any new release of the specification.

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Summary Tables of Changes

The following tables indicate the errata, specification changes, specification clarifications, or documentation changes which apply to the PCH product. Intel may fix some of the errata in a future stepping of the component, and account for the other outstanding issues through documentation or specification changes as noted. These tables uses the following notations:

Codes Used in Summary Tables

Stepping

X:	Errata exists in the stepping indicated. Specification Change or Clarification that applies to this stepping.
(No mark) or (Blank box):	This erratum is fixed in listed stepping or specification change does not apply to listed stepping.

Page

(Page):	Page location of item in this document.

Status

Doc:	Document change or update will be implemented.
Plan Fix:	This erratum may be fixed in a future stepping of the product.
Fixed:	This erratum has been previously fixed.
No Fix:	There are no plans to fix this erratum.

Row

Change bar to left of table row indicates this erratum is either new or modified from the previous version of the document.

Errata

Erratum Number	Stepping		Status	ERRATA
	B2	B3		
1	X	X	No Fix	USB Isoch In Transfer Error Issue
2	X	X	No Fix	USB Full-/low-speed Device Removal Issue
3	X	X	No Fix	USB Babble Detected with SW Overscheduling
4	X	X	No Fix	USB Full-/low-speed EOP Issue
5	X	X	No Fix	USB PLL Control FSM Not Getting Reset on Global Reset
6	X	X	No Fix	Asynchronous Retries Prioritized Over Periodic Transfers
7	X	X	No Fix	USB FS/LS Incorrect Number of Retries
8	X	X	No Fix	Incorrect Data for FS/LS USB Periodic IN Transaction
9	X	X	No Fix	HDMI 222 MHz Electrical Compliance Testing Failures
10	X	X	No Fix	SATA Signal Voltage Level Violation
11	X	X	No Fix	SATA Differential Return Loss Violations
12	X	X	No Fix	High-speed USB 2.0 Transmit Signal Amplitude
13	X	X	No Fix	Delayed Periodic Traffic Timeout Issue
14	X		Fixed	SATA Ports 2-5 Issue
15	X	X	No Fix	Intel® ME Clock Throttling Failure Causes Hang
16	X	X	No Fix	USB Full-/low-speed Port Reset or Clear TT Buffer Request
17	X	X	No Fix	Intel® 82579 Gigabit Ethernet Controller Transmission Issue

Specification Changes

Spec Change Number	Stepping		SPECIFICATION CHANGES
	B2	B3	
1	X	X	LED Locate Intel® Rapid Storage Technology Capability Removal

Specification Clarification

No.	Document Revision	SPECIFICATION CLARIFICATIONS
1	2.1	Device 31 Function 6 Disable Bit
2	2.1	LAN Disable Reset
3	2.1	SGPIO Signal Usage
4	2.1	RTCRST# and SRTCRST# Clarification
5	2.1	PPM of 25 MHz Option for CLKOUTFLEX2
6	2.1	SATA Alternate ID Enable Definition Update
7	2.1	SATA Hot Plug Operation
8	2.1	GPIO13 Voltage Tolerance
9	2.1	EHCI Configuration Programming

Documentation Changes

No.	Document Revision	DOCUMENTATION CHANGES
1	2.1	Addition of LPC Capability List Pointer Register
2	2.1	Intel® Smart Response Technology Functional Description Updates
3	2.1	Addition of Legacy ATA Backwards Compatibility Registers
4	2.1	DMI L1 Exit Latency Documentation Change
5	2.1	Device 30 Function 0 Naming Consistency Change
6	2.1	Gigabit Ethernet Capabilities and Status Registers Additions
7	2.1	Measured ICC Corrections
8	2.1	Miscellaneous Documentation Corrections

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Identification Information

Markings

PCH Stepping	S-Spec	Top Marking	Notes
B2	SLH82	BD82H67	Intel® H67 Chipset
B2	SLH84	BD82P67	Intel® P67 Chipset
B2	SLH9C	BD82HM67	Intel® HM67 Chipset
B2	SLH9D	BD82HM65	Intel® HM65 Chipset
B3	SLJ4D	BD82Q67	Intel® Q67 Chipset
B3	SLJ4E	BD82Q65	Intel® Q65 Chipset
B3	SLJ4A	BD82B65	Intel® B65 Chipset
B3	SLJ4F	BD82Z68	Intel® Z68 Chipset
B3	SLJ49	BD82H67	Intel® H67 Chipset
B3	SLJ4C	BD82P67	Intel® P67 Chipset
B3	SLJ4B	BD82H61	Intel® H61 Chipset
B3	SLJ4J	BD82C202	Intel® C202 Chipset
B3	SLJ4H	BD82C204	Intel® C204 Chipset
B3	SLJ4G	BD82C206	Intel® C206 Chipset
B3	SLJ4M	BD82QM67	Intel® QM67 Chipset
B3	SLJ4L	BD82UM67	Intel® UM67 Chipset
B3	SLJ4N	BD82HM67	Intel® HM67 Chipset
B3	SLJ4P	BD82HM65	Intel® HM65 Chipset
B3	SLJ4K	BD82QS67	Intel® QS67 Chipset

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PCH Device and Revision Identification

The Revision ID (RID) is an 8-bit register located at the offset 08h in the PCI header of every PCI device and function. The assigned value is based on the product's stepping.

PCH Device and Revision ID Table (Sheet 1 of 4)

Device Function	Description	Dev ID	B2 Rev ID	B3 Rev ID	Comments
D31:F0	LPC	1C4Eh		05h	Intel® Q67 Chipset
		1C4Ch		05h	Intel® Q65 Chipset
		1C50h		05h	Intel® B65 Chipset
		1C4Ah	04h	05h	Intel® H67 Chipset
		1C44h		05h	Intel® Z68 Chipset
		1C46h	04h	05h	Intel® P67 Chipset
		1C5Ch		05h	Intel® H61 Chipset
		1C52h		05h	Intel® C202 Chipset
		1C54h		05h	Intel® C204 Chipset
		1C56h		05h	Intel® C206 Chipset
		1C4Fh		05h	Intel® QM67 Chipset
		1C47h		05h	Intel® UM67 Chipset
		1C4Bh	04h	05h	Intel® HM67 Chipset
		1C49h	04h	05h	Intel® HM65 Chipset
		1C4Dh		05h	Intel® QS67 Chipset

PCH Device and Revision ID Table (Sheet 2 of 4)

Device Function	Description	Dev ID	B2 Rev ID	B3 Rev ID	Comments
D31:F2	SATA[1]	1C00h	04h	05h	Desktop: Non-AHCI and Non-RAID Mode (Ports 0-3)
		1C02h	04h	05h	Desktop: AHCI (Ports 0-5)
		2822h[2]	04h	05h	Desktop: Intel® Rapid Storage Technology RAID with or without Intel® Smart Response Technology (Ports 0-5) (AIE bit = 0)
		1C04h[2]	04h	05h	Desktop (all RAID-capable SKUs except Intel Z68 Chipset): RAID Capable[3] (Ports 0-5) (AIE bit = 1)
		1C06h[2]	04h	05h	Desktop (Intel Z68 Chipset only): RAID Capable[3] (Ports 0-5) (AIE bit = 1)
		1C01h	04h	05h	Mobile: Non-AHCI and Non-RAID Mode (Ports 0-3)
		1C03h	04h	05h	Mobile: AHCI (Ports 0-5)
		282Ah[2]	04h	05h	Mobile: Intel® Rapid Storage Technology RAID (Ports 0-5) (AIE bit = 0)
		1C05h[2]	04h	05h	Mobile: RAID Capable[3] (Ports 0-5) (AIE bit = 1)
D31:F5	SATA[1,4]	1C08h	04h	05h	Desktop: Non-AHCI and Non-RAID Mode (Ports 4 and 5)
		1C09h	04h	05h	Mobile: Non-AHCI and Non-RAID Mode (Ports 4 and 5)
D31:F3	SMBus	1C22h	04h	05h	
D31:F6	Thermal	1C24h	04h	05h	
D30:F0	DMI to PCI Bridge	1C25h	04h	05h	Desktop (When D30:F0:4Ch:bit 29 = 1)
		244Eh	A4h	A5h	Desktop (When D30:F0:4Ch:bit 29 = 0)
		1C25h	04h	05h	Mobile (When D30:F0:4Ch:bit 29 = 1)
		2448h	A4h	A5h	Mobile (When D30:F0:4Ch:bit 29 = 0)
D29:F0	USB EHCI #1	1C26h	04h	05h	
D26:F0	USB EHCI #2	1C2Dh	04h	05h	
D27:F0	Intel® High Definition Audio	1C20h	04h	05h	
D28:F0	PCI Express* Port 1	1C10h	B4h	B5h	Desktop and Mobile (When D28:F0/F1/F2/F3/F4/F5/ F6/F7:ECh:bit 1= 0)
		244Eh	B4h	B5h	Desktop (When D28:F0/F1/F2/F3/F4/F5/ F6/F7:ECh:bit 1 = 1)
		2448h	B4h	B5h	Mobile (When D28:F0/F1/F2/F3/F4/F5/ F6/F7:ECh:bit 1 = 1)

PCH Device and Revision ID Table (Sheet 3 of 4)

Device Function	Description	Dev ID	B2 Rev ID	B3 Rev ID	Comments
D28:F1	PCI Express Port 2	1C12h	B4h	B5h	Desktop and Mobile (When D28:F0/F1/F2/F3/F4/F5/ F6/F7:ECh:bit 1 = 0)
		244Eh	B4h	B5h	Desktop (When D28:F0/F1/F2/F3/F4/F5/ F6/F7:ECh:bit 1 = 1)
		2448h	B4h	B5h	Mobile (When D28:F0/F1/F2/F3/F4/F5/ F6/F7:ECh:bit 1 = 1)
D28:F2	PCI Express Port 3	1C14h	B4h	B5h	Desktop and Mobile (When D28:F0/F1/F2/F3/F4/F5/ F6/F7:ECh:bit 1 = 0)
		244Eh	B4h	B5h	Desktop (When D28:F0/F1/F2/F3/F4/F5/ F6/F7:ECh:bit 1 = 1)
		2448h	B4h	B5h	Mobile (When D28:F0/F1/F2/F3/F4/F5/ F6/F7:ECh:bit 1 = 1)
D28:F3	PCI Express Port 4	1C16h	B4h	B5h	Desktop and Mobile (When D28:F0/F1/F2/F3/F4/F5/ F6/F7:ECh:bit 1 = 0)
		244Eh	B4h	B5h	Desktop (When D28:F0/F1/F2/F3/F4/F5/ F6/F7:ECh:bit 1 = 1)
		2448h	B4h	B5h	Mobile (When D28:F0/F1/F2/F3/F4/F5/ F6/F7:ECh:bit 1 = 1)
D28:F4	PCI Express Port 5	1C18h	B4h	B5h	Desktop and Mobile (When D28:F0/F1/F2/F3/F4/F5/ F6/F7:ECh:bit 1 = 0)
		244Eh	B4h	B5h	Desktop (When D28:F0/F1/F2/F3/F4/F5/ F6/F7:ECh:bit 1 = 1)
		2448h	B4h	B5h	Mobile (When D28:F0/F1/F2/F3/F4/F5/ F6/F7:ECh:bit 1 = 1)
D28:F5	PCI Express Port 6	1C1Ah	B4h	B5h	Desktop and Mobile (When D28:F0/F1/F2/F3/F4/F5/ F6/F7:ECh:bit 1 = 0)
		244Eh	B4h	B5h	Desktop (When D28:F0/F1/F2/F3/F4/F5/ F6/F7:ECh:bit 1 = 1)
		2448h	B4h	B5h	Mobile (When D28:F0/F1/F2/F3/F4/F5/ F6/F7:ECh:bit 1 = 1)
D28:F6	PCI Express Port 7	1C1Ch	B4h	B5h	Desktop and Mobile (When D28:F0/F1/F2/F3/F4/F5/ F6/F7:ECh:bit 1 = 0)
		244Eh	B4h	B5h	Desktop (When D28:F0/F1/F2/F3/F4/F5/ F6/F7:ECh:bit 1 = 1)
		2448h	B4h	B5h	Mobile (When D28:F0/F1/F2/F3/F4/F5/ F6/F7:ECh:bit 1 = 1)
D28:F7	PCI Express Port 8	1C1Eh	B4h	B5h	Desktop and Mobile (When D28:F0/F1/F2/F3/F4/F5/ F6/F7:ECh:bit 1 = 0)
		244Eh	B4h	B5h	Desktop (When D28:F0/F1/F2/F3/F4/F5/ F6/F7:ECh:bit 1 = 1)
		2448h	B4h	B5h	Mobile (When D28:F0/F1/F2/F3/F4/F5/ F6/F7:ECh:bit 1 = 1)
D25:F0	LAN	1C33h[5]	04h	05h	

PCH Device and Revision ID Table (Sheet 4 of 4)

Device Function	Description	Dev ID	B2 Rev ID	B3 Rev ID	Comments
D22:F0	Intel® ME Interface #1	1C3Ah	04h	05h	
D22:F1	Intel ME Interface #2	1C3Bh	04h	05h	
D22:F2	IDE-R	1C3Ch	04h	05h	
D22:F3	KT	1C3Dh	04h	05h	

NOTES:

1. PCH contains two SATA controllers. The SATA Device ID is dependent upon which SATA mode is selected by BIOS and what RAID capabilities exist in the SKU.
2. The SATA RAID Controller Device ID is dependent upon: 1) the AIE bit setting (bit 7 of D31:F2:Offset 9Ch); and 2) (only when the AIE bit is 1) which desktop PCH SKU is in the system..
3. A third party RAID driver is required to utilize the SATA ports of the PCH for RAID functionality. Intel Rapid Storage Technology and Intel Smart Response Technology require that the AIE bit is set to 0.
4. SATA Controller 2 (D31:F5) is only visible when D31:F2 CC.SCC =01h
5. LAN Device ID is loaded from EEPROM. If EEPROM contains either 0000h or FFFFh in the Device ID location, then 1C33h is used. Refer to the appropriate Intel® GbE physical layer Transceiver (PHY) datasheet for LAN Device IDs.
6. This table shows the default PCI Express Function Number-to-Root Port mapping. Function numbers for a given root port are assignable through the “Root Port Function Number and Hide for PCI Express Root Ports” register (RCBA+0404h).

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Errata

1. USB Isoch In Transfer Error Issue

Problem: If a USB full-speed inbound isochronous transaction with a packet length 190 bytes or greater is started near the end of a microframe the PCH may see more than 189 bytes in the next microframe.

Implication: If the PCH sees more than 189 bytes for a microframe an error will be sent to software and the isochronous transfer will be lost. If a single data packet is lost no perceptible impact for the end user is expected.

Note: Intel has only observed the issue in a synthetic test environment where precise control of packet scheduling is available, and has not observed this failure in its compatibility validation testing.

- Isochronous traffic is periodic and cannot be retried thus it is considered good practice for software to schedule isochronous transactions to start at the beginning of a microframe. Known software solutions follow this practice.
- To sensitize the system to the issue additional traffic such as other isochronous transactions or retries of asynchronous transactions would be required to push the inbound isochronous transaction to the end of the microframe.

Workaround: None.

Status: No Plan to Fix.

2. USB Full-/low-speed Device Removal Issue

Problem: If two or more USB full-/low-speed devices are connected to the same USB controller, the devices are not suspended, and one device is removed, one or more of the devices remaining in the system may be affected by the disconnect.

Implication: The implication is device dependent. A device may experience a delayed transaction, stall and be recovered via software, or stall and require a reset such as a hot plug to resume normal functionality.

Workaround: None.

Status: No Plan to Fix.

3. USB Babble Detected with SW Overscheduling

Problem: If software violates USB periodic scheduling rules for full-speed isochronous traffic by overscheduling, the RMH may not handle the error condition properly and return a completion split with more data than the length expected.

Implication: If the RMH returns more data than expected, the endpoint will detect packet babble for that transaction and the packet will be dropped. Since overscheduling occurred to create the error condition, the packet would be dropped regardless of RMH behavior. If a single isochronous data packet is lost, no perceptible impact to the end user is expected.

Note: USB software overscheduling occurs when the amount of data scheduled for a microframe exceeds the maximum budget. This is an error condition that violates the USB periodic scheduling rule.

Note: This failure has only been recreated synthetically with USB software intentionally overscheduling traffic to hit the error condition.

Workaround: None.

Status: No Plan to Fix.

4. USB Full-/low-speed EOP Issue

Problem: If the EOP of the last packet in a USB Isochronous split transaction (Transaction >189 bytes) is dropped or delayed 3 ms or longer the following may occur:

- If there are no other pending low-speed or full-speed transactions the RMH will not send SOF, or Keep-Alive. Devices connected to the RMH will interpret this condition as idle and will enter suspend.
- If there is other pending low-speed or full-speed transactions, the RMH will drop the isochronous transaction and resume normal operation.

Implication:

- If there are no other transactions pending, the RMH is unaware a device entered suspend and may starting sending a transaction without waking the device. The implication is device dependent, but a device may stall and require a reset to resume functionality.
- If there are other transactions present, only the initial isochronous transaction may be lost. The loss of a single isochronous transaction may not result in end user perceptible impact.

Note: Intel has only observed this failure when using software that does not comply with the USB specification and violates the hardware isochronous scheduling threshold by terminating transactions that are already in progress

Workaround: None.

Status: No Plan to Fix.

5. USB PLL Control FSM not Getting Reset on Global Reset

Problem: Intel® 6 Series Chipsets and Intel® C200 Series Chipsets USB PLL may not lock if a Global Reset occurs early during a cold boot sequence.

Implication: USB interface would not be functional an additional cold boot would be necessary to recover.

Workaround: None.

Status: No Plan to Fix.

6. Asynchronous Retries Prioritized Over Periodic Transfers

Problem: The integrated USB RMH incorrectly prioritizes full-speed and low-speed asynchronous retries over dispatchable periodic transfers.

Implication: Periodic transfers may be delayed or aborted. If the asynchronous retry latency causes the periodic transfer to be aborted, the impact varies depending on the nature of periodic transfer:

- If a periodic interrupt transfer is aborted, the data may be recovered by the next instance of the interrupt or the data could be dropped.
- If a periodic isochronous transfer is aborted, the data will be dropped. A single dropped periodic transaction should not be noticeable by end user.

Note: This issue has only been seen in a synthetic environment. The USB spec does not consider the occasional loss of periodic traffic a violation.

Workaround: None.

Status: No Plan to Fix.

7. USB FS/LS Incorrect Number of Retries

Problem: A USB low-speed Transaction may be retried more than three times, and a USB full-speed transaction may be retried less than three times if all of the following conditions are met:

- A USB low-speed transaction with errors, or the first retry of the transaction occurs near the end of a microframe, and there is not enough time to complete another retry of the low-speed transaction in the same microframe
- There is pending USB full-speed traffic and there is enough time left in the microframe to complete one or more attempts of the full-speed transaction
- Both the low-speed and full-speed transactions must be asynchronous (Bulk/Control) and must have the same direction either in or out

Note: Note: Per the USB EHCI Specification a transaction with errors should be attempted a maximum of 3 times if it continues to fail.

Implication:

- For low-speed transactions the extra retry(s) allow a transaction additional chance(s) to recover regardless of if the full-speed transaction has errors or not.
- If the full-speed transactions also have errors, the PCH may retry the transaction fewer times than required, stalling the device prematurely. Once stalled, the implication is software dependent, but the device may be reset by software.

Workaround: None.

Status: No Plan to Fix.

8. Incorrect Data for FS/LS USB Periodic IN Transaction

Problem: The Periodic Frame list entry in DRAM for a USB FS or LS Periodic IN transaction may incorrectly get some of its data from a prior Periodic IN transaction which was initiated very late into the preceding microframe.

It is considered good practice for software to schedule Periodic Transactions at the start of a microframe. However Periodic transactions may occur late into a microframe due to the following cases outlined below:

- Asynchronous transaction starting near the end of the proceeding microframe gets Asynchronously retried

Note: Transactions getting Asynchronous retried would only occur for ill behaved USB device or USB port with a signal integrity issue

- Or Two Periodic transactions are scheduled by software to occur in the same microframe and the first needs to push the second Periodic IN transaction to the end of the microframe boundary

Implication: The implication will be device, driver or operating system specific.

Note: This issue has only been observed in a synthetic test environment

Workaround: None.

Status: No Plan to Fix.

9. HDMI 222 MHz Electrical Compliance Testing Failures

Problem: HDMI 222 MHz electrical compliance testing may show eye diagram and jitter test failures on Intel 6 Series Chipsets and Intel C200 Series Chipsets.

Implication: No functional or visual failures have been observed by Intel. HDMI electrical compliance failures may be seen at 222 MHz Deep Color Mode. This issue does not prevent HDMI with Deep Color Logo certification as no failures have been seen with 74.25 MHz Deep Color Mode (720P 60 Hz or 1080P 30 Hz) as required HDMI Compliance Test Specification.

Workaround: None.

Status: No Plan to Fix.

10. SATA Signal Voltage Level Violation

Problem: SATA transmit buffers have been designed to maximize performance and robustness over a variety of routing scenarios. As a result, the SATA transmit signaling voltage levels may exceed the maximum motherboard TX connector and device RX connector voltage specifications as defined in section 7.2.1 of the Serial ATA specification, rev 3.0. This issue applies to Gen 1 (1.5 Gb/s) and Gen 2 (3.0 Gb/s).

Implication: None known.

Workaround: None.

Status: No Plan to Fix.

11. SATA Differential Return Loss Violations

Problem: The Intel 6 Series Chipset and Intel C200 Series Chipset SATA buffer capacitance may be higher than expected.

Implication: There are no known functional failures. This may cause a violation of the SATA-IO compliance test for Receiver or Transmitter Differential Return Loss.

Workaround: None.

Note: Intel has obtained a waiver for the SATA-IO building block status.

Status: No Plan to Fix.

12. High-speed USB 2.0 Transmit Signal Amplitude

Problem: Intel 6 Series Chipset and Intel C200 Series Chipset High-speed USB 2.0 transmit signal amplitude may exceed the USB 2.0 specification.

- USB 2.0 Specification Transmit Eye template maximum boundary is +/- 525 mV following bit transitions and +/- 475 mV for non-transitional bit patterns.
- USB 2.0 Specification V_{HSOH} maximum is 440 mV.

Implication: There are no known functional failures.

Workaround: None.

Status: No Plan to Fix.

13. Delayed Periodic Traffic Timeout Issue

Problem: If a periodic interrupt transaction is pushed out to the x+4 microframe boundary, the RMH may not wait for the transaction to timeout before starting the next transaction.

Implication: If the next full-speed or low-speed transaction is intended for the same device targeted by the periodic interrupt, the successful completion of that transaction is device dependent and cannot be guaranteed. The implication may differ depending on the nature of the transaction:

- If the transaction is asynchronous and the device does not respond, it will eventually be retried with no impact.
- If the transaction is periodic and the device does not respond, the transfer may be dropped. A single dropped periodic transaction should not be noticeable by end user.

Note: This issue has only been seen in a synthetic environment.

Workaround: None.

Status: No Plan to Fix.

14. SATA Ports 2-5 Issue

Problem: Due to a circuit design issue on Intel 6 Series Chipset and Intel C200 Series Chipset, electrical lifetime wear out may affect clock distribution for SATA ports 2-5. This may manifest itself as a functional issue on SATA ports 2-5 over time.

- The electrical lifetime wear out may result in device oxide degradation which over time can cause drain to gate leakage current.
- This issue has time, temperature and voltage sensitivities.

Implication: The increased leakage current may result in an unstable clock and potentially functional issues on SATA ports 2-5 in the form of receive errors, transmit errors, and unrecognized drives.

- Data saved or stored prior to functional issues on a SATA device will be retrievable if connected to a working SATA port.
- SATA ports 0-1 are not affected by this design issue as they have separate clock generation circuitry.

Workaround: Intel has worked with board and system manufacturers to identify and implement solutions for affected systems.

- Use only SATA ports 0-1.
- Use an add-in PCIe SATA bridge solution.

Status: Fixed. For steppings affected, see the Summary Table of Changes.

- This issue has been resolved with a silicon stepping for all Intel 6 Series Chipsets and Intel C200 Series Chipsets incorporating a minor metal layer change.
- The fix does not impact the designed functionality and electrical specifications of the Intel 6 Series Chipset and Intel C200 Series Chipset.

15. Intel® ME Clock Throttling Failure Causes Hang

Problem: When the Intel® Management Engine (Intel® ME) firmware sets the internal clock frequency, the Intel ME clock may stop toggling, potentially causing the Intel® Management Engine Interface to become unresponsive.

Implication: Parts that exhibit this issue may hang during POST.

Note: No functional failures have been seen due to this issue.

An Intel® ME FW code change has been identified and may be implemented as a workaround for this erratum.

Status: No Plan to Fix.

16. USB Full-/low-speed Port Reset or Clear TT Buffer Request

Problem: One or more full-/low-speed USB devices on the same RMH controller may be affected if the devices are not suspended and either (a) software issues a Port Reset OR (b) software issues a Clear TT Buffer request to a port executing a split full-/low-speed Asynchronous Out command.

- The Small window of exposure for full-speed device is around 1.5 microseconds and around 12 microseconds for a low-speed device.

Implication: The affected port may stall or receive stale data for a newly arrived split transfer occurring at the time of the Port Reset or Clear TT Buffer request.

Note: This issue has only been observed in a synthetic test environment.

Workaround: None.

Status: No Plan to Fix.

17. Intel® 82579 Gigabit Ethernet Controller Transmission Issue

Problem: Intel® 82579 Gigabit Ethernet Controller with the Intel 6 Series Chipsets and Intel C200 Series Chipsets and Intel ME Firmware 7.x 5 MB may stop transmitting during a data transfer.

Implication: Intel 82579 Gigabit Ethernet Controller may stop transmitting packets, the link LED will blink, and a power cycle may be required to resume transmission activity.

Note: This issue has only been observed in a focused test environment where data is constantly transferred over an extended period of time (more than approximately 3 hours).

Workaround: A combination of Intel ME FW code change and Intel 82579 Gigabit Ethernet Controller LAN Driver update has been identified and may be implemented as a workaround for this erratum

Status: No Plan to Fix.

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Specification Changes

1. LED Locate Intel® Rapid Storage Technology Capability Removal

Bit 7 of 14.4.1.10 RSTF—Intel® RST Feature Capabilities Register (ABAR + C8h–C9h), previously known as the LED Locate (LEDL) bit, is changed to Reserved.

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Specification Clarification

1. Device 31 Function 6 Disable Bit

Section 10.1.45 FD—Function Disable Register bit 24 is changed as shown:

Bit	Description
24	**Thermal Sensor Registers Disable (TTD)** — R/W. Default is 0. 0 = Thermal Sensor Registers (D31:F6) are enabled. 1 = Thermal Sensor Registers (D31:F6) are disabled.

2. LAN Disable Reset

Section 10.1.44 BUC—Backed Up Control Register bit 5 is changed as shown:

Bit	Description
5	**LAN Disable** — R/W. 0 = LAN is Enabled 1 = LAN is Disabled. Changing the internal GbE controller from disabled to enabled requires a system reset (write of 0Eh to CF9h (RST_CNT Register)) immediately after clearing the LAN disable bit. A reset is not required if changing the bit from enabled to disabled. This bit is locked by the Function Disable SUS Well Lockdown register. Once locked, this bit cannot be changed by software.

3. SGPIO Signal Usage

The following note is added at the conclusion of the first paragraph of section 5.16.13:

Intel does not validate all possible usage cases of this feature. Customers should validate their specific design implementation on their own platforms.

4. RTCRST# and SRTCRST# Clarification

The following replaces section 5.13.10.6:

RTCRST# is used to reset PCH registers in the RTC Well to their default value. If a jumper is used on this pin, it should only be pulled low when system is in the G3 state and then replaced to the default jumper position. Upon booting, BIOS should recognize that RTCRST# was asserted and clear internal PCH registers accordingly. It is imperative that this signal not be pulled low in the S0 to S5 states.

SRTCRST# is used to reset portions of the Intel® Manageability Engine and should not be connected to a jumper or button on the platform. The only time this signal gets asserted (driven low in combination with RTCRST#) should be when the coin cell battery is removed or not installed and the platform is in the G3 state. Pulling this

signal low independently (without RTCRST# also being driven low) may cause the platform to enter an indeterminate state. Similar to RTCRST#, it is imperative that SRTCRST# not be pulled low in the S0 to S5 states.

See Figure 2-2 which demonstrates the proper circuit connection of these pins.

5. PPM of 25 MHz Option for CLKOUTFLEX2

The following note is added to table 4-2 and applies to CLKOUFLEX2:

The 25 MHz output option for CLKOUTFLEX2 is derived from the 25 MHz crystal input to the PCH. The PPM of the 25 MHz output is equivalent to that of the crystal.

6. SATA Alternate ID Enable Definition Update

Section 14.1.33 D31:F2:Offset 9Ch is changed as follows:

a. Name of register is changed from SCLKGC-SATA Clock General Configuration Register to SGC-SATA General Configuration Register

b. Bit 7 is redefined as shown:

<table>
<tr><th>Bit</th><th>Description</th></tr>
<tr><td>7 (non-RAID Capable SKUs Only)</td><td>Reserved</td></tr>
<tr><td>7 (RAID Capable SKUs Only)</td><td>Alternate ID Enable (AIE) — R/WO.
0 = Clearing this bit when in RAID mode, the SATA Controller located at Device 31: Function 2 will report its Device ID as 2822h for all Desktop SKUs of the PCH or 282Ah for all Mobile SKUs of the PCH. Clearing this bit is required for the Intel® Rapid Storage Technology driver (including the Microsoft* Windows Vista* OS and later in-box version of the driver) to load on the platform. Intel® Smart Response Technology also requires that the bit be cleared in order to be enabled on the platform.
1 = Setting this bit when in RAID mode, the SATA Controller located at Device 31: Function 2 will report its Device ID as called out in the table below for Desktop SKUs or 1C05h for all Mobile SKUs of the chipset. This setting will prevent the Intel Rapid Storage Technology driver (including the Microsoft Windows* OS in-box version of the driver) from loading on the platform. During the Microsoft Windows OS installation, the user will be required to "load' (formerly done by pressing the F6 button on the keyboard) the appropriate RAID storage driver that is enabled by this setting.
<table>
<tr><th colspan="3">D31:F2 Configured in RAID Mode with AIE = 1 (Desktop Only)</th></tr>
<tr><th colspan="2">Feature Vector Register 0 (FVEC0)</th><th rowspan="2">D31:F2 Dev ID</th></tr>
<tr><th>RAID Capability Bit 1</th><th>RAID Capability Bit 0</th></tr>
<tr><td>0</td><td>0</td><td>Not applicable</td></tr>
<tr><td>0</td><td>1</td><td>Not applicable</td></tr>
<tr><td>1</td><td>0</td><td>1C04h</td></tr>
<tr><td>1</td><td>1</td><td>1C06h</td></tr>
</table>
This field is reset by PLTRST#. BIOS is required to reprogram the value of this bit after resuming from S3, S4 and S5.</td></tr>
</table>

c. the following is added to the list of items describing when Intel Rapid Storage Technology is not available in section 5.16.7:

2. The SATA controller is programmed in RAID mode, but the AIE bit (D31:F2:Offset 9Ch bit 7) is set to 1.

d. The SATA D31:F2 Device ID table is updated; see PCH Device and Revision Identification section in this document.

7. SATA Hot Plug Operation

Section 5.16.5 Hot Plug Operation is modified as shown below. Section 5.16.5.1 is removed.

The PCH supports Hot Plug Surprise removal and Insertion Notification. An internal SATA port with a Mechanical Presence Switch can support PARTIAL and SLUMBER with Hot Plug Enabled. Software can take advantage of power savings in the low power states while enabling hot plug operation. Refer to chapter 7 of the AHCI specification for details.

8. GPIO13 Voltage Tolerance

GPIO13 is powered by VccSusHDA well and therefore, the voltage tolerance value varies according to the voltage connected to VccSusHDA. The following clarifications are made:

a. Table 2-24, GPIO13 Tolerance is change from “3.3 V” to “3.3 V or 1.5 V” and the following note is added to table 2-24: “GPIO13 is powered by VccSusHDA (either 3.3 V or 1.5 V). Voltage tolerance on the signal is the same as VccSusHDA.”

b. The following note is added to GPIO13 in table 3-2 as note 16: “GPIO13 is powered by VccSusHDA (either 3.3 V or 1.5 V). Pin tolerance is determined by VccSusHDA voltage.”

c. The following note is added to HDA_DOCK_RST#/GPIO13 in table 3-3 as note 24: “HDA_DOCK_RST#/GPIO13 is powered by VccSusHDA (either 3.3 V or 1.5 V). Pin tolerance is determined by VccSusHDA voltage.”

9. EHCI Configuration Programming

a. Section 16.1.31 EHCIIR1—EHCI Initialization Register 1 bits 18 and 10:9 are changed as shown:

Bit	Description
18	**EHCI Initialization Register 1 Field 2**— R/W. BIOS may write to this bit field.
10:9	**EHCI Initialization Register 1 Field 1**— R/W. BIOS may write to this bit field.

b. Section 16.1.32 EHCIIR2—EHCI Initialization Register 2 is modified as shown:

Bit	Description
31:30	Reserved
29	**EHCI Initialization Register 2 Field 6** — R/W. BIOS may write to this bit field.
28:20	Reserved
19	**EHCI Initialization Register 2 Field 5** — R/W. BIOS may write to this bit field.
18:12	Reserved

Bit	Description
11	**EHCI Initialization Register 2 Field 4** — R/W. BIOS may write to this bit field.
10	**EHCI Initialization Register 2 Field 3** — R/W. BIOS may write to this bit field.
9	Reserved
8	**EHCI Initialization Register 2 Field 2** — R/W. BIOS may write to this bit field.
7:6	Reserved
5	**EHCI Initialization Register 2 Field 1** — R/W. BIOS may write to this bit field.
4:0	Reserved

c. Section 16.1.38 EHCIIR3—EHCI Initialization Register 3 bits 32:22 are changed as shown:

Bit	Description
23:22	**EHCI Initialization Register 3 Field 1** — R/W. BIOS may write to this bit field.

d. Section 16.1.39 EHCIIR4—EHCI Initialization Register 4 bits 17 and 15 are changed as shown:

Bit	Description
17	**EHCI Initialization Register 4 Field 2** — R/W. BIOS may write to this bit field.
15	**EHCI Initialization Register 4 Field 1** — R/W. BIOS may write to this bit field.

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Documentation Changes

1. Addition of LPC Capability List Pointer Register

The following is added immediately after 13.1.11:

CAPP – Capability List Pointer Register (LPC I/F—D31:F0)

Offset Address: 34h Attribute: RO
Default Value: E0h Size: 8 bits

Bit	Description
7:0	**Capability Pointer (CP)** — RO. Indicates the offset of the first Capability Item.

2. Intel® Smart Response Technology Functional Description Updates

The following replaces section 5.16.8

Part of the Intel® RST storage class driver feature set, Intel® Smart Response Technology implements storage I/O caching to provide users with faster response times for things like system boot and application startup. On a traditional system, performance of these operations is limited by the hard drive, particularly when there may be other I/O intensive background activities running simultaneously, like system updates or virus scans. Intel Smart Response Technology accelerates the system response experience by putting frequently-used blocks of disk data on an SSD, providing dramatically faster access to user data than the hard disk alone can provide. The user sees the full capacity of the hard drive with the traditional single drive letter with overall system responsiveness similar to what an SSD-only system provides.

See Section 1.3 for SKUs enabled for Intel Smart Response Technology.

3. Addition of Legacy ATA Backwards Compatibility Registers

a. Section 14.1.22 IDE_TIM — IDE Timing Register is modified as shown:

Bit	Description
15	**IDE Decode Enable (IDE)** — R/W. Individually enable/disable the Primary or Secondary decode. 0 = Disable. 1 = Enables the PCH to decode the associated Command Block (1F0–1F7h for primary, 170–177h for secondary, or their native mode BAR equivalents) and Control Block (3F6h for primary, 376h for secondary, or their native mode BAR equivalents). This bit effects the IDE decode ranges for both legacy and native-mode decoding.

Bit	Description
14:12	**IDE_TIM Field 2** — R/W. This field is R/W to maintain software compatibility. This field has no effect on hardware.
11:10	Reserved
9:0	**IDE_TIM Field 1** — R/W. This field is R/W to maintain software compatibility. This field has no effect on hardware.

b. The following paragraph is added to the register summary of section 14.1.22 IDE_TIM — IDE Timing Register:
Bits 14:12 and 9:0 of this register are R/W to maintain software compatibility. These bits have no effect on hardware.

c. The following registers are added immediately following section 14.1.22:

SIDETIM—Slave IDE Timing Register (SATA–D31:F2)

Address Offset: 44h Attribute: R/W
Default Value: 00h Size: 8 bits

Note: This register is R/W to maintain software compatibility. These bits have no effect on hardware.

Bit	Description
7:0	**SIDETIM Field 1** — R/W. This field is R/W to maintain software compatibility. This field has no effect on hardware.

SDMA_CNT—Synchronous DMA Control Register (SATA–D31:F2)

Address Offset: 48h Attribute: R/W
Default Value: 00h Size: 8 bits

Note: This register is R/W to maintain software compatibility. These bits have no effect on hardware.

Bit	Description
7:4	Reserved
3:0	**SDMA_CNT Field 1** — R/W. This field is R/W to maintain software compatibility. This field has no effect on hardware.

SDMA_TIM—Synchronous DMA Timing Register (SATA–D31:F2)

Address Offset: 4Ah–4Bh Attribute: R/W
Default Value: 0000h Size: 16 bits

Note: This register is R/W to maintain software compatibility. These bits have no effect on hardware.

Bit	Description
15:14	Reserved
13:12	**SDMA_TIM Field 4**— R/W. This field is R/W to maintain software compatibility. This field has no effect on hardware.
11:10	Reserved

Bit	Description
9:8	**SDMA_TIM Field 3**— R/W. This field is R/W to maintain software compatibility. This field has no effect on hardware.
7:6	Reserved
5:4	**SDMA_TIM Field 2**— R/W. This field is R/W to maintain software compatibility. This field has no effect on hardware.
3:2	Reserved
1:0	**SDMA_TIM Field 1** — R/W. This field is R/W to maintain software compatibility. This field has no effect on hardware.

IDE_CONFIG—IDE I/O Configuration Register (SATA–D31:F2)

Address Offset: 54h–57h Attribute: R/W
Default Value: 00000000h Size: 32 bits

Note: This register is R/W to maintain software compatibility. These bits have no effect on hardware.

Bit	Description
31:24	Reserved
23:12	**IDE_CONFIG Field 2** — R/W. This field is R/W to maintain software compatibility. This field has no effect on hardware.
11:8	Reserved
7:0	**IDE_CONFIG Field 1** — R/W. This field is R/W to maintain software compatibility. This field has no effect on hardware.

d. Section 15.1.21 IDE_TIM — IDE Timing Register is modified as shown:

Bit	Description
15	**IDE Decode Enable (IDE)** — R/W. Individually enable/disable the Primary or Secondary decode. 0 = Disable. 1 = Enables the PCH to decode the associated Command Block and Control Block.
14:12	**IDE_TIM Field 2** — R/W. This field is R/W to maintain software compatibility. This field has no effect on hardware.
11:10	Reserved
9:0	**IDE_TIM Field 1** — R/W. This field is R/W to maintain software compatibility. This field has no effect on hardware.

e. The following paragraph is added to the register summary of section 15.1.21 IDE_TIM — IDE Timing Register:
Bits 14:12 and 9:0 of this register are R/W to maintain software compatibility. These bits have no effect on hardware.

f. The following registers are added immediately following section 15.1.21:

SDMA_CNT—Synchronous DMA Control Register (SATA–D31:F5)

Address Offset: 48h Attribute: R/W
Default Value: 00h Size: 8 bits

Note: This register is R/W to maintain software compatibility. These bits have no effect on hardware.

Bit	Description
7:4	Reserved
3:0	**SDMA_CNT Field 1** — R/W. This field is R/W to maintain software compatibility. This field has no effect on hardware.

SDMA_TIM—Synchronous DMA Timing Register (SATA–D31:F5)

Address Offset: 4Ah–4Bh Attribute: R/W
Default Value: 0000h Size: 16 bits

Note: This register is R/W to maintain software compatibility. These bits have no effect on hardware.

Bit	Description
15:10	Reserved
9:8	**SDMA_TIM Field 2**— R/W. This field is R/W to maintain software compatibility. This field has no effect on hardware.
7:2	Reserved
1:0	**SDMA_TIM Field 1** — R/W. This field is R/W to maintain software compatibility. This field has no effect on hardware.

IDE_CONFIG—IDE I/O Configuration Register (SATA–D31:F5)

Address Offset: 54h–57h Attribute: R/W
Default Value: 00000000h Size: 32 bits

Note: This register is R/W to maintain software compatibility. These bits have no effect on hardware.

Bit	Description
31:24	Reserved
23:16	**IDE_CONFIG Field 6** — R/W. This field is R/W to maintain software compatibility. This field has no effect on hardware.
15	Reserved
14	**IDE_CONFIG Field 5** — R/W. This field is R/W to maintain software compatibility. This field has no effect on hardware.
13	Reserved
12	**IDE_CONFIG Field 4** — R/W. This field is R/W to maintain software compatibility. This field has no effect on hardware.
11:8	Reserved
7:4	**IDE_CONFIG Field 3** — R/W. This field is R/W to maintain software compatibility. This field has no effect on hardware.
3	Reserved

Bit	Description
2	**IDE_CONFIG Field 2** — R/W. This field is R/W to maintain software compatibility. This field has no effect on hardware.
1	Reserved
0	**IDE_CONFIG Field 1** — R/W. This field is R/W to maintain software compatibility. This field has no effect on hardware.

4. DMI L1 Exit Latency Documentation Change

Section 10.1.14 LCAP—Link Capabilities Register bits 17:15 are changed as shown:

Bit	Description
17:15	**L1 Exit Latency (EL1)** — R/WO. 000b – Less than 1 µs 001b – 1 µs to less than 2 µs 010b – 2 µs to less than 4 µs 011b – 4 µs to less than 8 µs 100b – 8 µs to less than 16 µs 101b – 16 µs to less than 32 µs 110b – 32 µs to 64 µs 111b – More than 64 µs

5. Device 30 Function 0 Naming Consistency Change

Device 30 Function 0 is named PCI-to-PCI Bridge throughout document for consistency.

6. Gigabit Ethernet Capabilities and Status Registers Additions

a. The follow is added as section 12.2

12.2 Gigabit LAN Capabilities and Status Registers (CSR)

The internal CSR registers and memories are accessed as direct memory mapped offsets from the base address register in Section 12.1.10. Software may only access whole DWord at a time.

Note: Register address locations that are not shown in Table 12-2 should be treated as Reserved.

Table 12-2. Gigabit LAN Capabilities and Status Registers Address Map (Gigabit LAN —MBARA) (Sheet 1 of 2)

MBARA + Offset	Mnemonic	Register Name	Default	Attribute
00h-03h	GBECSR1	Gigabit Ethernet Capabilities and Status Register 1	00100241h	R/W
18h-1Bh	GBECSR2	Gigabit Ethernet Capabilities and Status Register 2	01501000h	R/W/SN
20h-23h	GBECSR3	Gigabit Ethernet Capabilities and Status Register 3	1000XXXXh	R/W/V
2Ch-2Fh	GBECSR4	Gigabit Ethernet Capabilities and Status Register 4	00000000h	R/W

Table 12-2. Gigabit LAN Capabilities and Status Registers Address Map (Gigabit LAN —MBARA) (Sheet 2 of 2)

MBARA + Offset	Mnemonic	Register Name	Default	Attribute
F00h-F03h	GBECSR5	Gigabit Ethernet Capabilities and Status Register 5	00010008h	R/W/V
F10h-F13h	GBECSR6	Gigabit Ethernet Capabilities and Status Register 6	0004000Ch	R/W/SN
5400h-5403h	GBECSR7	Gigabit Ethernet Capabilities and Status Register 7	XXXXXXXXh	R/W
5404h-5407h	GBECSR8	Gigabit Ethernet Capabilities and Status Register 8	XXXXXXXXh	R/W
5800h-5803h	GBECSR9	Gigabit Ethernet Capabilities and Status Register 9	00000008h	R/W/SN

12.2.1 GBECSR1—Gigabit Ethernet Capabilities and Status Register 1

Address Offset: MBARA + 00h Attribute: R/W
Default Value: 00100241h Size: 32 bit

Bit	Description
31:25	Reserved
24	**PHY Power Down (PHYPDN)** — R/W**.** When cleared (0b), the PHY power down setting is controlled by the internal logic of PCH.
23:0	Reserved

12.2.2 GBECSR2—Gigabit Ethernet Capabilities and Status Register 2

Address Offset: MBARA + 18h Attribute: R/W/SN
Default Value: 01501000h Size: 32 bit

Bit	Description
31:21	Reserved
20	**PHY Power Down Enable (PHYPDEN)** — R/W/SN**.** When set, this bit enables the PHY to enter a low-power state when the LAN controller is at the DMoff/D3 or with no WOL.
19:0	Reserved

12.2.3 GBECSR3—Gigabit Ethernet Capabilities and Status Register 3

Address Offset: MBARA + 20h Attribute: R/W/V
Default Value: 1000XXXXh Size: 32 bit

Bit	Description
31:29	Reserved
28	**Ready Bit (RB)** — R/W/V. Set to 1 by the Gigabit Ethernet Controller at the end of the MDI transaction. This bit should be reset to 0 by software at the same time the command is written.
27:26	**MDI Type** — R/W/V. 01 = MDI Write 10 = MDI Read All other values are reserved.
25:21	**LAN Connected Device Address (PHYADD)** — R/W/V.
20:16	**LAN Connected Device Register Address (PHYREGADD)** — R/W/V.
15:0	**DATA** — R/W/V.

12.2.4 GBECSR4—Gigabit Ethernet Capabilities and Status Register 4

Address Offset: MBARA + 2Ch Attribute: R/W
Default Value: 00000000h Size: 32 bits

Bit	Description
31	**WOL Indication Valid (WIV)** — R/W. Set to 1 by BIOS to indicate that the WOL indication setting in bit 30 of this register is valid.
30	**WOL Enable Setting by BIOS (WESB)** — R/W. 1 = WOL Enabled in BIOS. 0 = WOL Disabled in BIOS.
29:0	Reserved

12.2.5 GBECSR5—Gigabit Ethernet Capabilities and Status Register 5

Address Offset: MBARA + F00h Attribute: R/W/V
Default Value: 00010008h Size: 32 bits

Bit	Description
31:6	Reserved
5	**SW Semaphore FLAG (SWFLAG)** — R/W/V. This bit is set by the device driver to gain access permission to shared CSR registers with the firmware and hardware.
4:0	Reserved

12.2.6 GBECSR6—Gigabit Ethernet Capabilities and Status Register 6

Address Offset: MBARA + F10h Attribute: R/W/SN
Default Value: 0004000Ch Size: 32 bits

Bit	Description
31:7	Reserved
6	**Global GbE Disable (GGD)**— R/W/SN. Prevents the PHY from auto negotiating 1000Mb/s link in all power states.
5:4	Reserved
3	**GbE Disable at non D0a** — R/W/SN. Prevents the PHY from auto negotiating 1000Mb/s link in all power states except D0a. This bit must be set since GbE is not supported in Sx states.
2	**LPLU in non D0a (LPLUND)** — R/W/SN. Enables the PHY to negotiate for the slowest possible link in all power states except D0a.
1	**LPLU in D0a (LPLUD)** — R/W/SN. Enables the PHY to negotiate for the slowest possible link in all power states. This bit overrides bit 2.
0	Reserved

12.2.7 GBECSR7—Gigabit Ethernet Capabilities and Status Register 7

Address Offset: MBARA + 5400h Attribute: R/W
Default Value: XXXXXXXXh Size: 32 bits

Bit	Description
31:0	**Receive Address Low (RAL)**— R/W. The lower 32 bits of the 48 bit Ethernet Address.

12.2.8 GBECSR8—Gigabit Ethernet Capabilities and Status Register 8

Address Offset: MBARA + 5404h Attribute: R/W
Default Value: XXXXXXXXh Size: 32 bits

Bit	Description
31	**Address Valid**— R/W.
30:16	Reserved
15:0	**Receive Address High (RAH)**— R/W. The lower 16 bits of the 48 bit Ethernet Address.

12.2.9 GBECSR9—Gigabit Ethernet Capabilities and Status Register 9

Address Offset: MBARA + 5800h Attribute: R/W/SN
Default Value: 00000008h Size: 32 bits

Bit	Description
31:1	Reserved
0	**Advanced Power Management Enable (APME)** — R/W/SN. 1 = APM Wakeup is enabled 0 = APM Wakeup is disabled

b. Bit and register attributes of the type R/W/SN are defined as follows. This is added to the beginning of chapter 9:

R/W/SN Read/Write register initial value loaded from NVM

7. Measured ICC Corrections

The following updates are made in table 8-5:

Voltage Rail	Voltage (V)	S0 Iccmax Current Integrated Graphics[5] (A)	S0 Iccmax Current External Graphics[5] (A)	S0 Idle Current Integrated Graphics[4,5] (A)	S0 Idle Current External Graphics[5] (A)	Sx Iccmax Current[5] (A)	Sx Idle Current (A)	G3
VccADPLLA	1.05	0.08	0.02	0.073	0.01	0	0	—
VccDSW3_3	3.3	0.001	0.001	0.001	0.001	0.002	0.001	—

8. Miscellaneous Documentation Corrections

a. Sections 23.1.1.17 PID—PCI Power Management Capability ID Register and 23.2.1.16 PID—PCI Power Management Capability ID Register default is changed to 8C01h and the register is modified as shown:

Bit	Description
15:8	**Next Capability (NEXT)** — RO. Value of 8Ch indicates the location of the next pointer.

b. Sections 23.1.1.8 and 23.2.1.8 naming is updated to be consistent with section 23.1.2 and 23.2.2 respectively.

Section	Mnemonic	Register Name
23.1.1.8	MEI0_MBAR	Intel MEI 1 MMIO Base Address
23.2.1.8	MEI1_MBAR	Intel MEI 2 MMIO Base Address

c. In table 8-5 Measured ICC (Desktop Only) VccDMI voltage is changed from 1.05 V to 1.05 V / 1.0 V.

d. In table 4-2 CLKOUTFLEX2 is changed to reflect that it is muxed with GPIO66.

e. Section 10.1.20 D31IP—Device 31 Interrupt Pin Register (RCBA+3100) bits 27:24 are changed as shown:

Bit	Description
27:24	**Thermal Sensor Pin (TSIP)** — R/W. Indicates which pin the Thermal Sensor controller drives as its interrupt 0h = No interrupt 1h = INTA# 2h = INTB# (Default) 3h = INTC# 4h = INTD# 5h–Fh = Reserved

f. Section 17.1.2.41 is renamed to ISDFIFOS—Input Stream Descriptor FIFO Size Register and section 17.1.2.42 is renamed to OSDFIFOS—Output Stream Descriptor FIFO Size Register.

g. 82C37 is changed to 8237 throughout document.

h. 82C54 is changed to 8254 throughout document.

i. 82C59 is changed to 8259 throughout document.

j. The second paragraph of section 5.10 is changed as shown:

The PCH supports a message for 21 serial interrupts. These represent the 15 ISA interrupts (IRQ0–1, 3–15), the four PCI interrupts, and the control signals SMI# and IOCHK#. The serial IRQ protocol does not support the additional APIC interrupts (20–23).

k. Section 5.13.11 Clock Generators is removed.

l. Section 5.8.4.6 Cascade Mode is removed.

m. THERM_ALERT# is changed to TEMP_ALERT# throughout document.

n. Section 10.1.36 PRSTS—Power and Reset Status Register (RCBA+3310h) bit 4 is changed as shown:

Bit	Description
4	**PRSTS Field 1 —** R/W. BIOS may write to this bit field.

o. The following table lists changes to terms (bit names) made throughout the document to ensure consistent naming throughout the document.

Old Term	New (Correct) Term
CPUSCI_STS	DMISCI_STS
CPUSMI_STS	DMISMI_STS
USB2_STS	INTEL_USB2_STS
USB2_EN	INTEL_USB2_EN
SWGPE	SWGPE_EN
SPI_SMI_STS	SPI_STS
SMI_ON_SLP_EN_STS	SLP_SMI_STS
SMI_ON_SLP_EN	SLP_SMI_EN
OS_TCO_SMI	SW_TCO_SMI
SMI_ON_SLP_EN	SLP_SMI_EN

p. The following sentence is removed from section 5.16.7:

“By using the PCH’s built-in Intel Rapid Storage Technology, there is no loss of PCI resources (request/grant pair) or add-in card slot.”

q. Section 14.4.2.5 PxIS—Port [5:0] Interrupt Status Register (ABAR+110h, 190h, 210h, 290h, 310h, 390h) bit 23 is changed as shown:

Bit	Description
23	**Incorrect Port Multiplier Status (IPMS)** — R/WC. The PCH SATA controller does not support Port Multipliers.

r. Section 14.4.2.6 PxIE—Port [5:0] Interrupt Enable Register (ABAR+114h, 194h, 214h, 294h, 314h, 394h) bit 23 is changed as shown:

Bit	Description
23	**Incorrect Port Multiplier Enable (IPME)** — R/W. The PCH SATA controller does not support Port Multipliers. BIOS and storage software should keep this bit cleared to 0.

s. The first sentence of section 2.20 is changed to “All signals are Mobile Only, except as noted that are also available in Desktop.”

t. Table 8-17 title is changed from “HDMI Interface Timings (DDP[D:B][3:0])Timings” to “HDMI Interface Timings (DDP[D:B][3:0])”.

u. Table 3-3 is updated to show that the PMSYNCH signal is Defined in Cx States.

v. Table 3-2 SML0ALERT# / GPIO60 note in Immediately after Reset is changed from 11 to 12.

w. Tables 3-2 and 3-3 note 7 removed from GPIO8 and GPIO27.

x. In section 13.8.3.5 GPE0_STS—General Purpose Event 0 Status Register, the SMBus Wake Status (SMB_WAK_STS) bit description is updated remove “SCI” to reflect that the SMBus controller can only generate an SMI#.

y. References to the Coprocessor Error Enable bit (RCBA+31FEh bit 9) mnemonic “COPROC_ERR_EN” are changed to “CEN” to represent the actual mnemonic.

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