

# Intel® 5 Series Chipset and Intel® 3400 Series Chipset

**Thermal Mechanical Specifications and Design Guidelines**

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*April 2011*



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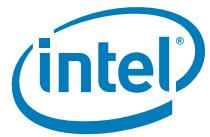


## Revision History

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Revision Number	Description	Revision Date
001	<ul style="list-style-type: none"><li>Initial release</li></ul>	September 2009
002	<ul style="list-style-type: none"><li>Added Intel® H55 Express Chipset, Intel® H57 Express Chipset, Intel® Q57 Express Chipset, and Intel® 3450 Chipset</li></ul>	January 2010
003	<ul style="list-style-type: none"><li>Added Intel® B55 Express Chipset</li></ul>	April 2011

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# 1 Introduction

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The goals of this document are to:

- Outline the thermal and mechanical operating limits and specifications for the Intel® 5 Series Chipset and Intel® 3400 Series Chipset for use in single processor Desktop, Workstation, and Server systems.
- Describe reference thermal solutions that meet the specifications of the Intel® 5 Series Chipset and Intel® 3400 Series Chipset.

The Intel® 5 Series Chipset components supported in this document are:

- Intel® P55 Express Chipset
- Intel® H55 Express Chipset
- Intel® H57 Express Chipset
- Intel® Q57 Express Chipset
- Intel® B55 Express Chipset

The Intel® 3400 Series Chipset for Server and Workstation Platform Controller Hub (PCH) components supported in this document are:

- Intel® 3400 Chipset
- Intel® 3420 Chipset
- Intel® 3450 Chipset

**Note:** Unless otherwise specified, the term "Platform Controller Hub" or "PCH" will be used to refer to any version of the Intel® 5 Series Chipset and any version of the Intel® 3400 Series Chipset for Server and Workstation Platform Controller Hub covered by this document. Only where required will a specific product code be used.

Properly designed thermal solutions provide adequate cooling to maintain the Platform Controller Hub case temperatures at or below thermal specifications. This is accomplished by providing a low local-ambient temperature, ensuring adequate local airflow, and minimizing the case to local-ambient thermal resistance. By maintaining the PCH case temperature at or below the specified limits, a system designer can ensure the proper functionality, performance, and reliability of the PCH. Operation outside the functional limits can cause data corruption or permanent damage to the component.

The simplest and most cost-effective method to improve the inherent system cooling characteristics is through careful chassis design and placement of fans, vents, and ducts. When additional cooling is required, component thermal solutions may be implemented in conjunction with system thermal solutions. The size of the fan or heatsink can be varied to balance size and space constraints with acoustic noise.

## 1.1 Related Documents

The reader of this specification should also be familiar with material and concepts presented in the following documents.

Title	Location
<i>Intel® 5 Series Chipset and Intel® 3400 Series Chipset Datasheet</i>	<a href="http://www.intel.com/Assets/PDF/datasheet/322169">www.intel.com/Assets/PDF/datasheet/322169</a>
<i>Intel® 5 Series Chipset and Intel® 3400 Series Chipset Specificaiton Update</i>	<a href="http://www.intel.com/Assets/PDF/specupdate/322170.pdf">www.intel.com/Assets/PDF/specupdate/322170.pdf</a>
<i>Intel® Core™ i7-800 and i5-700 Desktop Processor Series and LGA1156 Socket Thermal and Mechanical Specifications and Design Guidelines</i>	<a href="http://download.intel.com/design/processor/designnex/322167.pdf">http://download.intel.com/design/processor/designnex/322167.pdf</a>
<i>Intel® Xeon® Processor 3400 Series and LGA1156 Socket Thermal and Mechanical Specifications and Design Guidelines</i>	<a href="http://www.intel.com/Assets/PDF/datasheet/322374.pdf">http://www.intel.com/Assets/PDF/datasheet/322374.pdf</a>
Various system thermal design suggestions	<a href="http://www.formfactors.org">http://www.formfactors.org</a>

## 1.2 Terminology

Item	Description
BLT	Bond Line Thickness. Final settled thickness of the thermal interface material after installation of the heatsink.
CTE	Coefficient of Thermal Expansion. The relative rate a material expands during a thermal event.
FC-BGA	Flip Chip Ball Grid Array. A package type defined by a plastic substrate where a die is mounted using an underfill C4 (Controlled Collapse Chip Connection) attach style. The primary electrical interface is an array of solder balls attached to the substrate opposite the die. Note that the device arrives at the customer with solder balls attached.
PCH	Platform Controller Hub. The PCH is connected to the processor using the Direct Media Interface (DMI).
TDP	Thermal design power. Thermal solutions should be designed to dissipate this power level. TDP is not the peak power that the PCH can dissipate.
TIM	Thermal Interface Material. A conductive material used between the component and heatsink to improve thermal conduction.

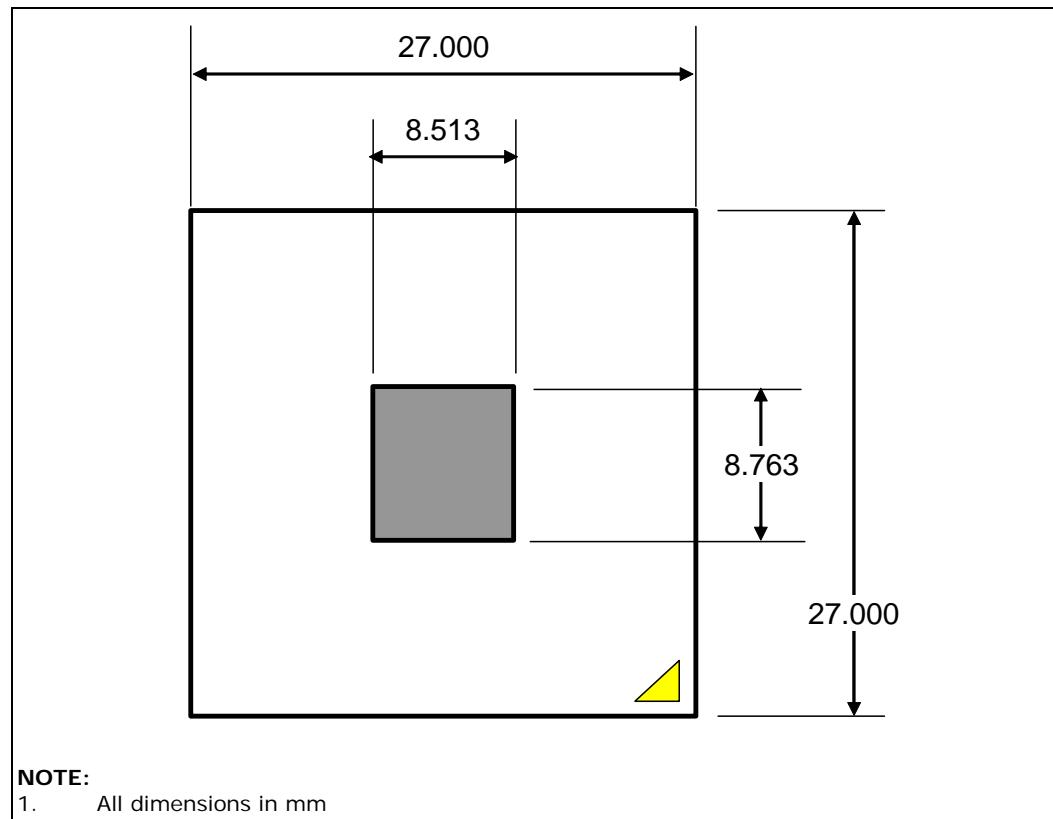
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## 2 Packaging Mechanical Specifications

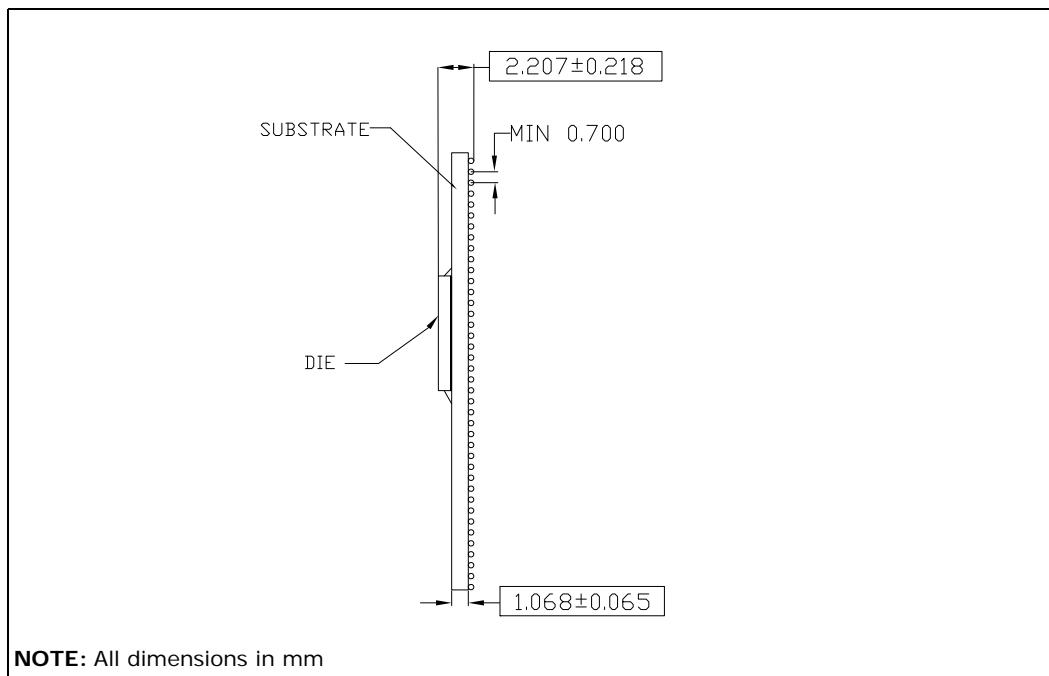
### 2.1 PCH Package for Desktop and Single Processor Server and Workstation

The Platform Controller Hub uses a 27 mm square flip chip ball grid array (FC-BGA) package (see [Figure 2-1](#) through [Figure 2-3](#)). The complete package drawing can be found in [Appendix B](#).

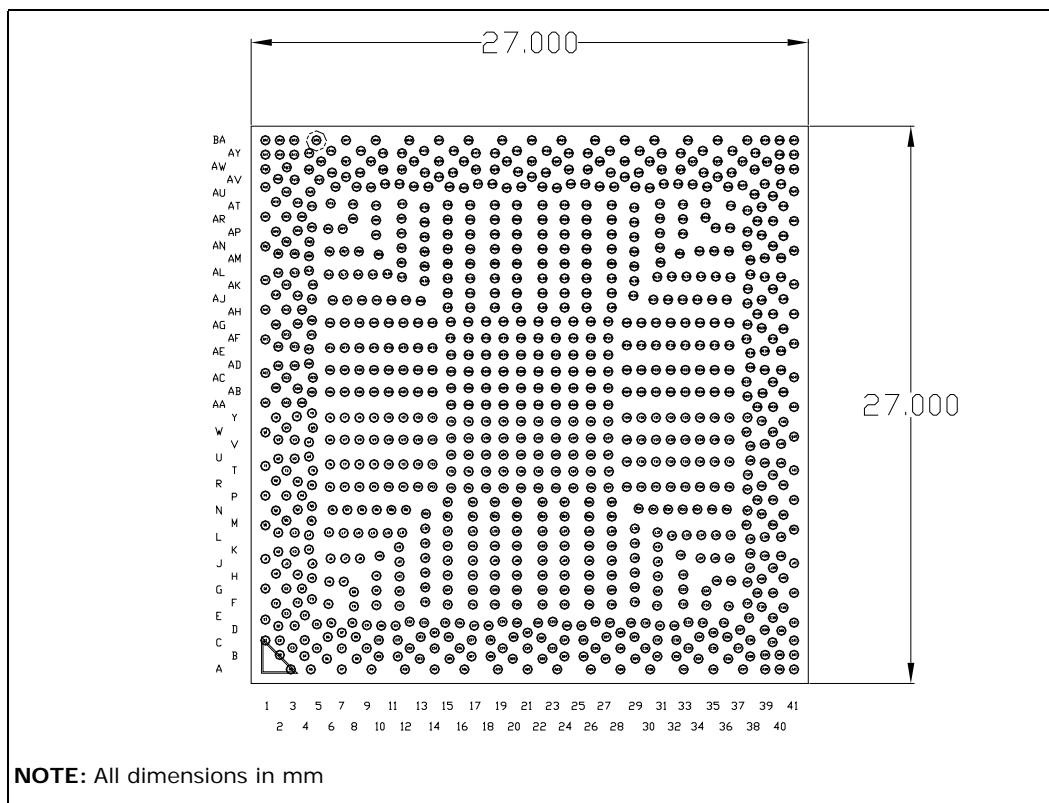
**Figure 2-1. Package Dimensions (Top View)**



**Figure 2-2. Package Dimensions (Side View)**



**Figure 2-3. Package (Land Side View)**



## 2.2 Solder Balls

A total of 951 solder balls corresponding to the lands are on the bottom of the PCH package for surface mounting with the motherboard. The package solder ball has the following characteristics:

- Lead free SAC (SnAgCu) 405 solder alloy with a silver (Ag) content between 3% and 4% and a melting temperature of approximately 217 °C. The alloy is compatible with immersion silver (ImAg) and Organic Solderability Protectant (OSP) motherboard surface finishes and a SAC alloy solder paste.
- Solder ball diameter 17 mil [0.4138 mm], before attaching to the package.

## 2.3 Package Mechanical Requirements

The package has a bare die that is capable of sustaining a maximum static normal load of 15 lbf (67N). These mechanical load limits must not be exceeded during heatsink installation, mechanical stress testing, standard shipping conditions, and/or any other use condition.

**Note:** The heatsink attach solutions must not induce continuous stress to the package with the exception of a uniform load to maintain the heatsink-to-package thermal interface.

**Note:** These specifications apply to uniform compressive loading in a direction perpendicular to the die top surface.

**Note:** These specifications are based on limited testing for design characterization. Loading limits are for the package only.

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## 3 Thermal Specifications

### 3.1 Thermal Design Power (TDP)

Real applications are unlikely to cause the PCH component to consume maximum power dissipation for sustained time periods. Therefore, in order to arrive at a more realistic power level for thermal design purposes, Intel characterizes power consumption to reach a Thermal Design Power (TDP). TDP is the target power level to which the thermal solutions should be designed. TDP is not the maximum power that the PCH can dissipate, see Table 3-1 and Table 3-2.

**Table 3-1. Intel® 5 Series Chipset Platform Controller Hub TDP and Idle Specifications**

Devices	Office <sup>1</sup>	Home <sup>1</sup>	Performance <sup>1</sup>	Notes
Intel® FDI	Yes	Yes	No	<a href="#">7</a>
PCI	0	1	1	
PCI Express*	2 - x1 (slot) Integrated GbE	3 - x1 (slot) Integrated GbE	3 - x1 (slot) 1 - x4 (slot) Integrated GbE	<a href="#">4,8</a>
SATA 1.5 Gb/s	1	2	2	<a href="#">4</a>
SATA 3.0 Gb/s	2	2	4	<a href="#">4</a>
USB (FS / HS)	2 / 5	2 / 9	2 / 9	<a href="#">5</a>
HD Audio	Ext Codec	Ext Codec	Ext Codec	
Intel® Anti-Theft Technology	Enabled	Not Used	Not Used	
Intel® QST	Enabled	Enabled	Enabled	<a href="#">6</a>
Display	2 DP	1 HDMI 1 DP	Ext Card	
TDP (W)	5.1	5.2	4.7	<a href="#">2</a>
Idle Power (W)	2.2	2.2	1.7	<a href="#">2, 3</a>

**NOTES:**

1. These specifications are based on correlated post silicon measurements and simulations.
2. The TDP and Idle estimates are based on a core voltage of 1.05 V.
3. The idle power assumes 100% Slumber for SATA devices, 100% L1 on PCI Express Links.
4. Unused PCI Express\* and SATA ports assumed to be disabled.
5. FS = Full Speed, HS = High Speed
6. Intel® Quiet System Technology
7. Intel® Flexible Display Interface
8. Integrated Gigabyte Ethernet controller uses 1 - x1 PCIe\* link

**Table 3-2. Intel® 3400 Series Chipset Platform Controller Hub TDP and Idle Specifications**

Devices	WorkStation <sup>1</sup>	Server <sup>1</sup>	Notes
Intel® FDI	Yes	No	<a href="#">7</a>
PCI	1	1	
PCI Express*	3 - x1 (slot) 1 - x4 (slot) Integrated GbE	3 - x1 (slot) 1 - x4 (slot) Integrated GbE	<a href="#">4</a> , <a href="#">8</a>
SATA 1.5 Gb/s	2	0	<a href="#">4</a>
SATA 3.0 Gb/s	4	6	<a href="#">4</a>
USB (FS / HS)	2 / 9	0 / 12	<a href="#">5</a>
HD Audio	Ext Codec	Not Used	
Intel® Anti-Theft Technology	Enabled	Not Used	
Intel® QST	Enabled	No	<a href="#">6</a>
Display	1 Analog 1 DP	External Card or VGA down chip	
TDP (W)	5.9	4.8	<a href="#">2</a>
Idle Power (W)	3.0	1.8	<a href="#">2</a> , <a href="#">3</a>

**NOTES:**

1. These specifications are based on correlated post silicon measurements and simulations.
2. The TDP and Idle estimates are based on a core voltage of 1.05 V.
3. The idle power assumes 100% Slumber for SATA devices, 100% L1 on PCI Express Links.
4. Unused PCI Express\* and SATA ports assumed to be disabled.
5. FS = Full Speed, HS = High Speed
6. Intel® Quiet System Technology
7. Intel® Flexible Display Interface
8. Integrated Gigabyte Ethernet controller uses 1 - x1 PCIe\* link

## 3.2 Case Temperature

To ensure proper operation and reliability of the component the case temperature must comply with the thermal profile as specified in [Table 3-3](#). System and/or component level thermal solutions are required to maintain these temperature specifications. Refer to [Chapter 5](#) for guidelines on accurately measuring package case temperatures.

**Table 3-3. Platform Controller Hub Thermal Specification**

Parameter	Value
Tcase-max	111 °C (Intel 5 Series Chipset) 111 °C (Intel 3400 Series Chipset)
Tcase-min	5 °C
T <sub>CONTROL</sub>	107 °C

**Note:**

The reference thermal solution is described in [Chapter 6](#).

### 3.3 Storage Specifications

Table 3-4 includes a list of the specifications for device storage in terms of maximum and minimum temperatures and relative humidity. These conditions should not be exceeded in storage or transportation.

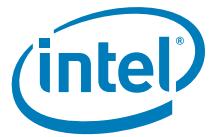
**Table 3-4. Storage Conditions**

Parameter	Description	Min	Max	Notes
$T_{ABSOLUTE\ STORAGE}$	The non-operating device storage temperature. Damage (latent or otherwise) may occur when subjected to for any length of time.	-55 °C	125 °C	<a href="#">1, 2, 3</a>
$T_{SUSTAINED\ STORAGE}$	The ambient storage temperature limit (in shipping media) for a sustained period of time.	-5 °C	40 °C	<a href="#">4, 5</a>
$RH_{SUSTAINED\ STORAGE}$	The maximum device storage relative humidity for a sustained period of time.	60% @ 24 °C		<a href="#">5, 6</a>
$TIME_{SUSTAINED\ STORAGE}$	A prolonged or extended period of time; typically associated with customer shelf life.	0 Months	6 Months	<a href="#">6</a>

**NOTE:**

1. Refers to a component device that is not assembled in a board or socket that is not to be electrically connected to a voltage reference or I/O signals.
2. Specified temperatures are based on data collected. Exceptions for surface mount reflow are specified in by applicable JEDEC standard and MAS document. Non-adherence may affect component reliability.
3.  $T_{ABSOLUTE\ STORAGE}$  applies to the unassembled component only and does not apply to the shipping media, moisture barrier bags or desiccant.
4. Intel® branded board products are certified to meet the following temperature and humidity limits that are given as an example only (Non-Operating Temperature Limit: -40 °C to 70 °C & Humidity: 50% to 90%, non-condensing with a maximum wet bulb of 28 °C) Post board attach storage temperature limits are not specified for non-Intel® branded boards.
5. The JEDEC, J-JSTD-020 moisture level rating and associated handling practices apply to all moisture sensitive devices removed from the moisture barrier bag.
6. Nominal temperature and humidity conditions and durations are given and tested within the constraints imposed by  $T_{SUSTAINED}$  and customer shelf life in applicable Intel® box and bags.

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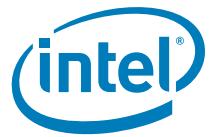


## 4 *Thermal Simulation*

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Intel provides thermal simulation models of the PCH and associated users' guides to aid system designers in simulating, analyzing, and optimizing their thermal solutions in an integrated, system-level environment. The models are for use with the commercially available Computational Fluid Dynamics (CFD)-based thermal analysis tool FLOTHERM\* (version 5.1 or higher) by Flomerics, Inc. and Icepak\* by Fluent. Contact your Intel field sales representative to order the thermal models and users' guides.

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## 5 Thermal Metrology

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The system designer must make temperature measurements to accurately determine the thermal performance of the system. Intel has established guidelines for proper techniques to measure the PCH die temperatures. [Section 5.1](#) provides guidelines on how to accurately measure the die temperatures. The flowchart in [Figure 5-1](#) offers useful guidelines for thermal performance and evaluation.

### 5.1 Die Temperature Measurements

To ensure functionality and reliability, the  $T_{case}$  of the PCH must be maintained at or between the maximum/minimum operating range of the temperature specification as noted in [Table 3-3](#). The surface temperature at the geometric center of the die corresponds to  $T_{case}$ . Measuring  $T_{case}$  requires special care to ensure an accurate temperature measurement.

Temperature differences between the surface and the surrounding local ambient air can introduce errors in the measurements. The measurement errors could be due to a poor thermal contact between the thermocouple junction and the surface of the package, heat loss by radiation and/or convection, conduction through thermocouple leads, and/or contact between the thermocouple cement and the heatsink base (if a heatsink is used). For maximum measurement accuracy, only the following thermocouple attach approach is recommended.

#### 5.1.1

#### Heatsink Thermocouple Attach Methodology

1. Mill a 3.3 mm (0.13 in.) diameter and 1.5 mm (0.06 in.) deep hole centered on the bottom of the heatsink base.
2. Mill a 1.3 mm (0.05 in.) wide and 0.5 mm (0.02 in.) deep slot from the centered hole to one edge of the heatsink. The slot should be parallel to the heatsink fins (see [Figure 5-2](#)).
3. Attach thermal interface material (TIM) to the bottom of the heatsink base.
4. Cut out portions of the TIM to make room for the thermocouple wire and bead. The cutouts should match the slot and hole milled into the heatsink base.
5. Attach a 36 gauge or smaller calibrated K-type thermocouple bead or junction to the center of the top surface of the die using a high thermal conductivity cement. During this step, ensure no contact is present between the thermocouple cement and the heatsink base because any contact will affect the thermocouple reading. It is critical that the thermocouple bead makes contact with the die (see [Figure 5-3](#)).
6. Attach heatsink assembly to the package and route thermocouple wires out through the milled slot.

Figure 5-1. Thermal Solution Decision Flow Chart

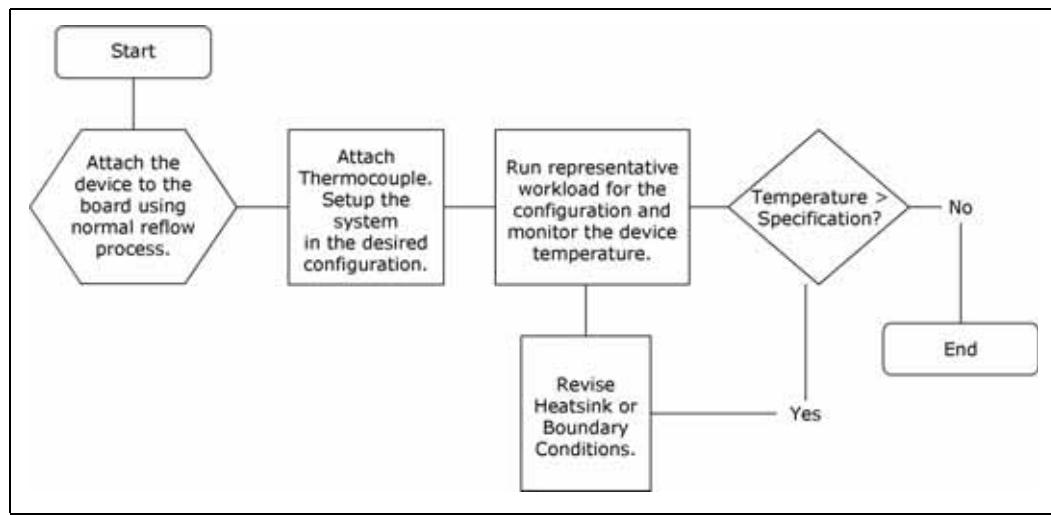
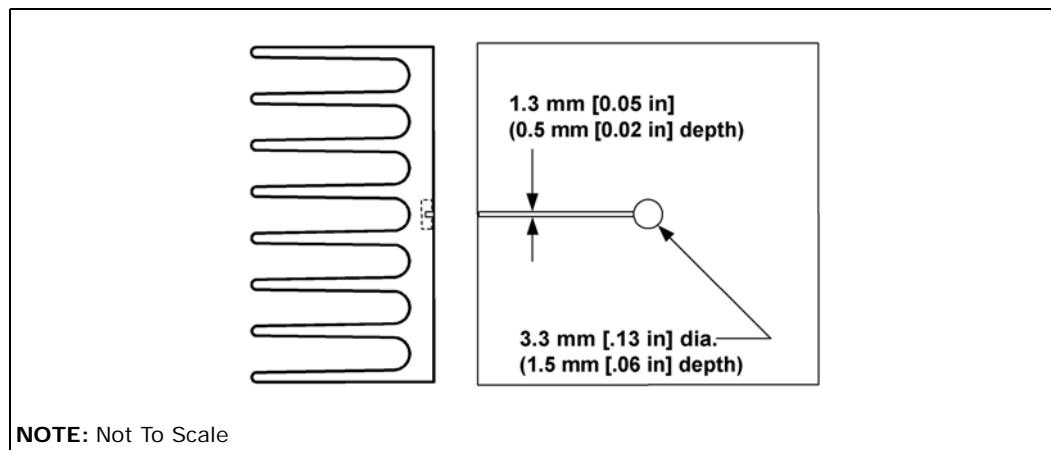
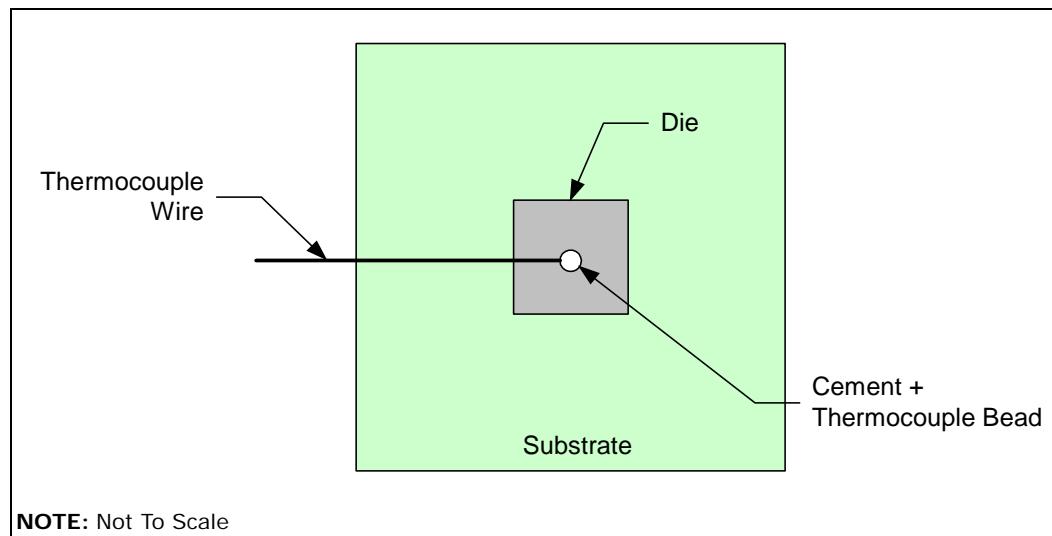


Figure 5-2. Heatsink Modifications



**Figure 5-3. Top View of Package**

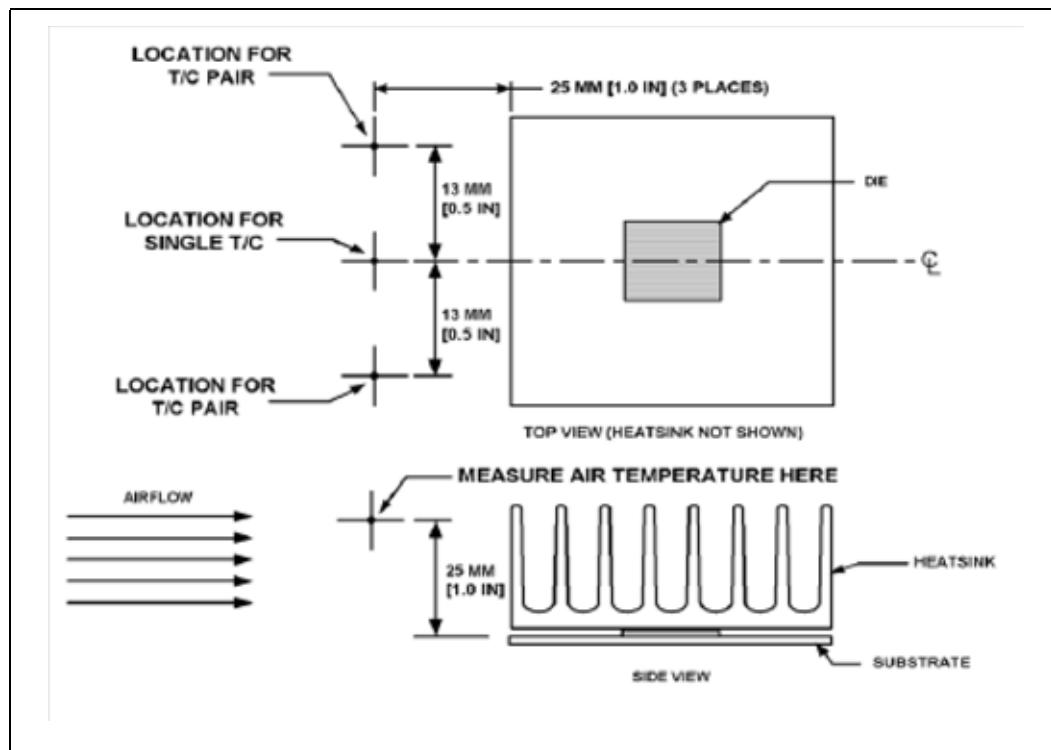
## 5.2 Ambient Temperature and Airflow Measurement

Figure 5-4 describes the recommended location for air temperature measurements measured relative to the component. For a more accurate measurement of the average approach air temperature, Intel recommends averaging temperatures recorded from two thermocouples spaced about 25 mm [1.0 in] apart. Locations for both a single thermocouple and a pair of thermocouples are presented.

Airflow velocity should be measured using industry standard air velocity sensors. Typical airflow sensor technology may include hot wire anemometers.

Figure 5-4 provides guidance for airflow velocity measurement locations. These locations are for a typical JEDEC test setup and may not be compatible with all chassis layouts due to the proximity of the, PCI and PCI Express\* add-in cards to the component. The user may have to adjust the locations for a specific chassis. Be aware that sensors may need to be aligned perpendicular to the airflow velocity vector or an inaccurate measurement may result. Measurements should be taken with the chassis fully sealed in its operational configuration to achieve a representative airflow profile within the chassis.

Figure 5-4. Airflow & Temperature Measurement Locations



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## 6 ATX Reference Thermal Solution

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**Note:** The reference thermal mechanical solution information shown in this document represents the current state of the design. The requirements review and preliminary design review have been completed. The final design reviews will occur in the 1H '09. The data is subject to modification and represents design targets, not commitments by Intel.

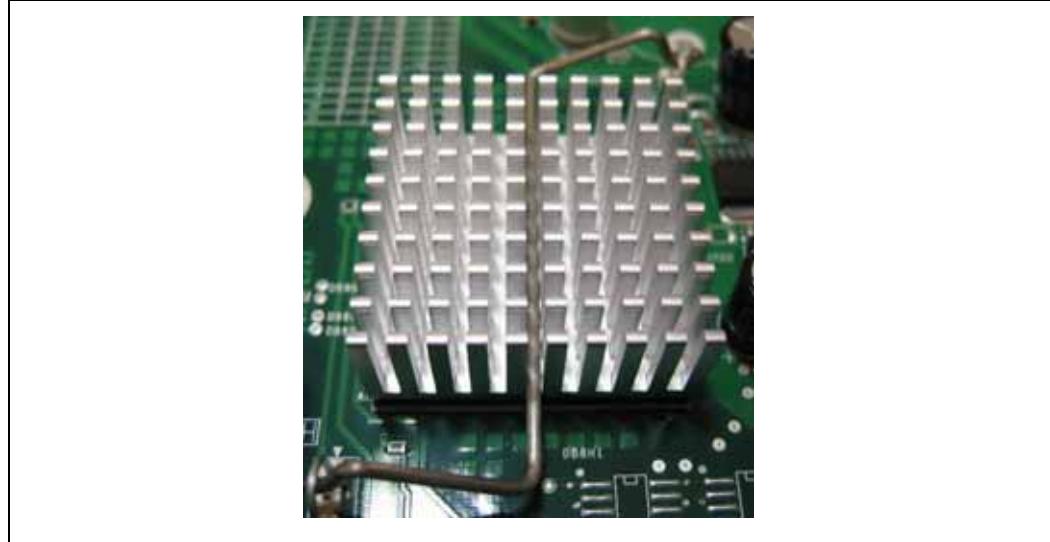
The design strategy for the PCH thermal solution is to reuse the z-clip heatsink originally designed for the I/O Controller Hub 6 (ICH6) Family and used on subsequent ICH designs through ICH10.

This section describes the overall requirements for the ATX heatsink reference thermal solution including critical-to-function dimensions, operating environment, and validation criteria. Other chipset components may or may not need attached thermal solutions depending on your specific system local-ambient operating conditions.

### 6.1 Reference Solution

The reference solution is an extruded aluminum heatsink with pre-applied phase change thermal interface material (TIM). The TIM is a Chomerics T710. The reference solution is provided as an assembly with the clip, TIM, and extrusion. See [Appendix B](#) for the complete set of mechanical drawings including the motherboard keep out zone.

**Figure 6-5. Reference Thermal Solution**



## 6.2 Environmental Reliability Requirements

The reference solution heatsink will be evaluated to the reliability requirements in [Table 6-1](#). The mechanical loading of the component may vary depending on the heatsink, and attach method used. The customer should define a validation test suite based on the anticipated use conditions and resulting reliability requirements. Thermal cycling, bake and humidity tests were performed on original design and are not being repeated. The designer should select appropriate thermal / humidity tests for the expected use conditions.

**Table 6-1. Reference Thermal Solution Environmental Reliability Requirements**

Test	Requirement	Pass / Fail Criteria
Mechanical Shock	3 drops for + and - directions in each of 3 perpendicular axes (i.e., total 18 drops). Profile: 50 G trapezoidal waveform, 170 inches/sec. minimum velocity change. Setup: Mount sample board on test fixture	Visual\Electrical Check
Random Vibration	Duration: 10 min/axis, 3 axes Frequency Range: 5 Hz to 500 Hz Power Spectral Density (PSD) Profile: 3.13 g RMS	Visual\Electrical Check

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## Appendix A Thermal Solution Component Vendors

**Note:** These vendors and devices are listed by Intel as a convenience to Intel's general customer base, but Intel does not make any representations or warranties whatsoever regarding quality, reliability, functionality, or compatibility of these devices. This list and/or these devices may be subject to change without notice.

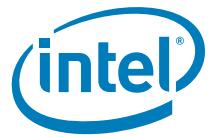
**Table A-1. Reference Heatsink Enabled Components**

Item	Intel PN	AVC	CCI	Foxconn	Wieson
Heatsink Assembly	C46655-001	S702C00001	00C855802B	2Z802-009	
Anchor	A13494-008			HB9703E-DW	G2100C888-064H

**Table A-2. Supplier Contact Information**

Supplier	Contact	Phone	
AVC (Asia Vital Corporation)	Kai Chang	+86-755-3366-8888 ext.63588	<a href="mailto:kai_chang@avc.com.tw">kai_chang@avc.com.tw</a>
CCI(Chau Choung Technology)	Monica Chih Harry Lin	+886-2-2995-2666 (714) 739-5797	<a href="mailto:monica_chih@ccic.com.tw">monica_chih@ccic.com.tw</a> <a href="mailto:hlinack@aol.com">hlinack@aol.com</a>
Foxconn	Jack Chen Wanchi Chen	(408) 919-6121 (408) 919-6135	<a href="mailto:jack.chen@foxconn.com">jack.chen@foxconn.com</a> <a href="mailto:wanchi.chen@foxconn.com">wanchi.chen@foxconn.com</a>
Wieson	Chary Lee Henry Liu	+886-2-2647-1896 ext. 6684 +886-2-2647-1896 ext.6330	<a href="mailto:chary@wieson.com">chary@wieson.com</a> <a href="mailto:henry@wieson.com">henry@wieson.com</a>

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*Thermal Solution Component Vendors*



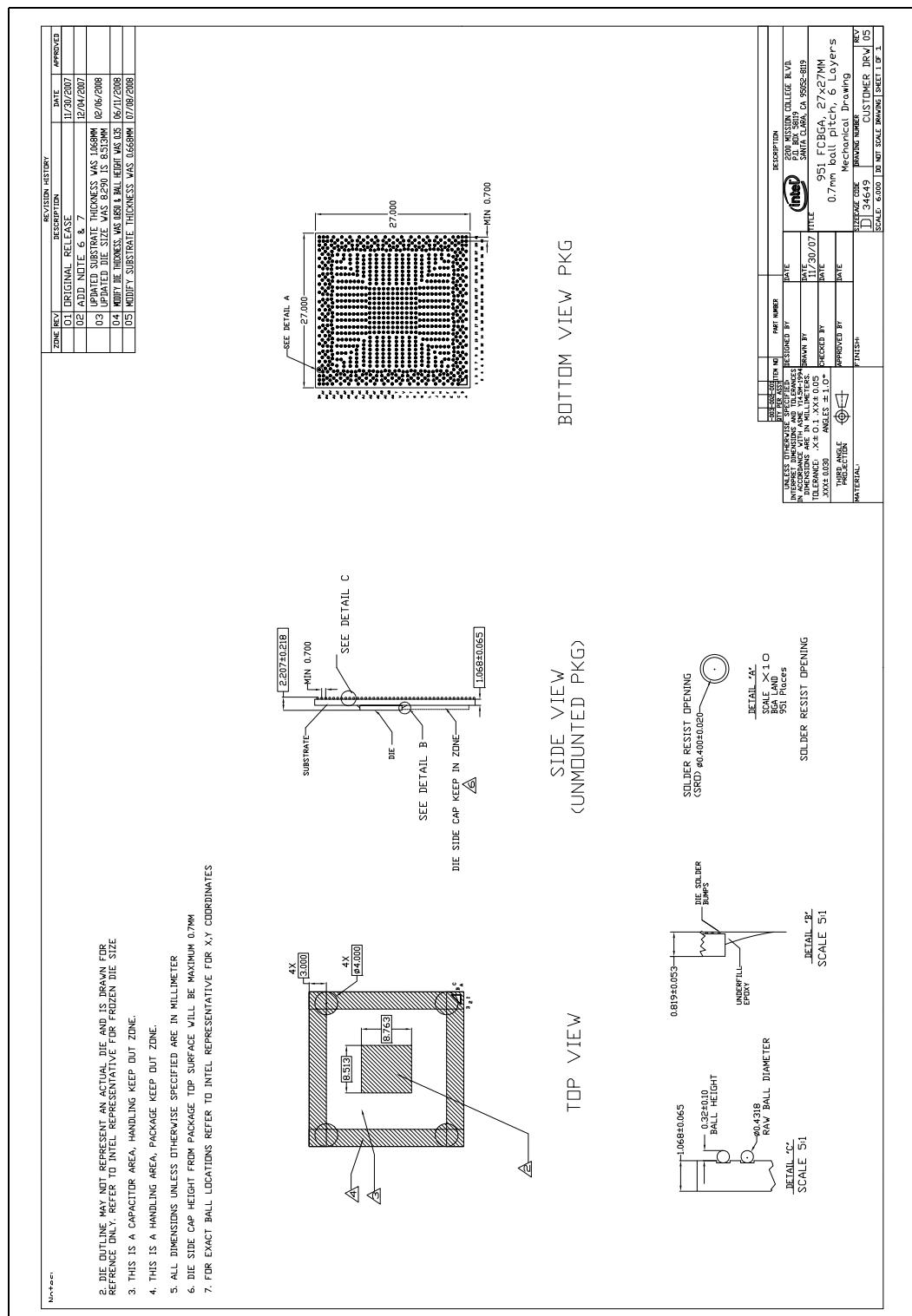
## ***Appendix B Mechanical Drawings for Package and Reference Thermal Solution***

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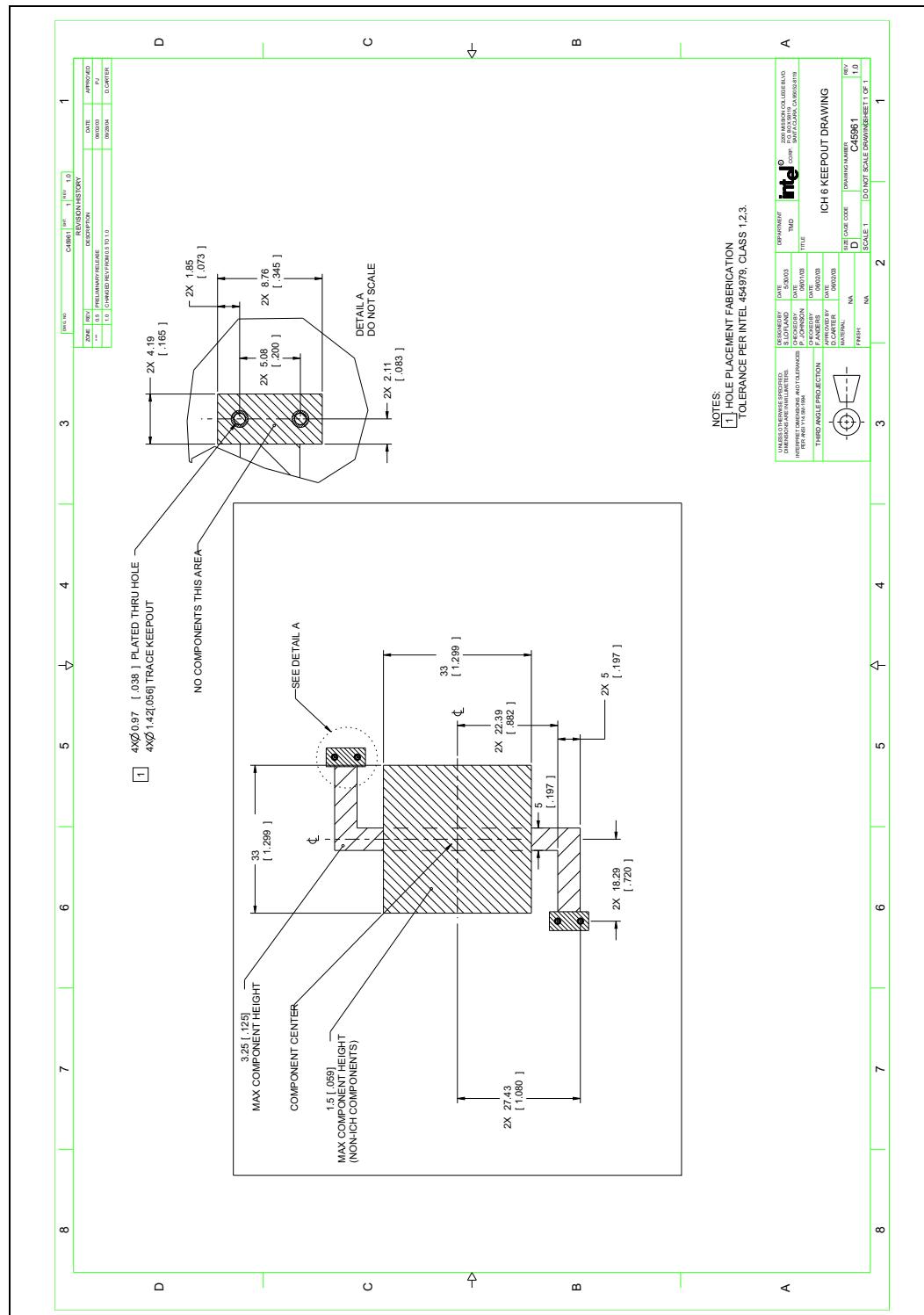
The mechanical drawings included in this appendix:

- [Figure B-1, "Desktop and Server and Workstation Platform Controller Hub Package Drawing" on page 28](#)
- [Figure B-2, "Motherboard Keep-Out for ATX Reference Heatsink" on page 29](#)
- [Figure B-3, "ATX Reference Heatsink Assembly" on page 30](#)
- [Figure B-4, "ATX Reference Heatsink Extrusion" on page 31](#)
- [Figure B-5, "ATX Reference Heatsink Clip" on page 32](#)

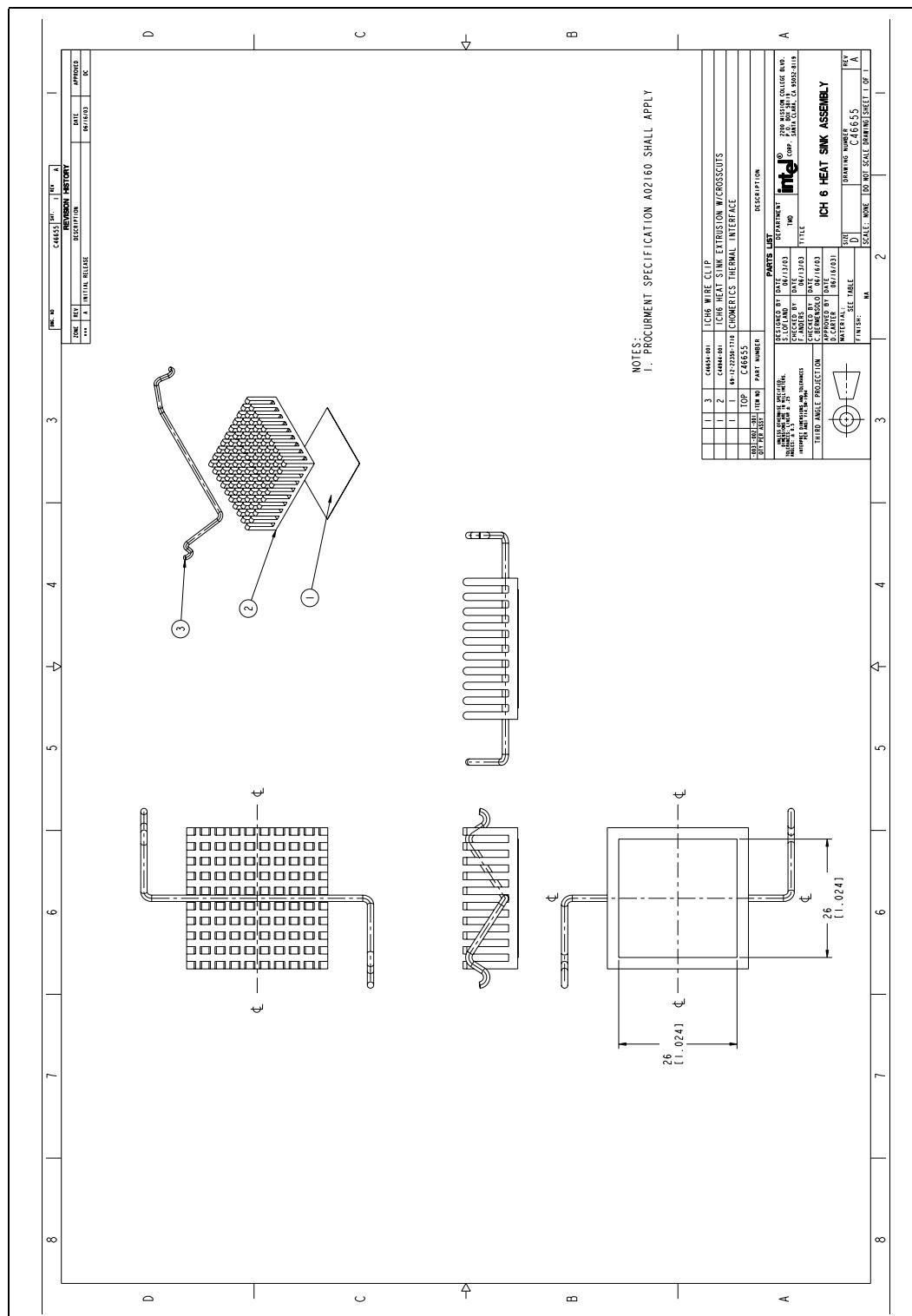
**Figure B-1. Desktop and Server and Workstation Platform Controller Hub Package Drawing**



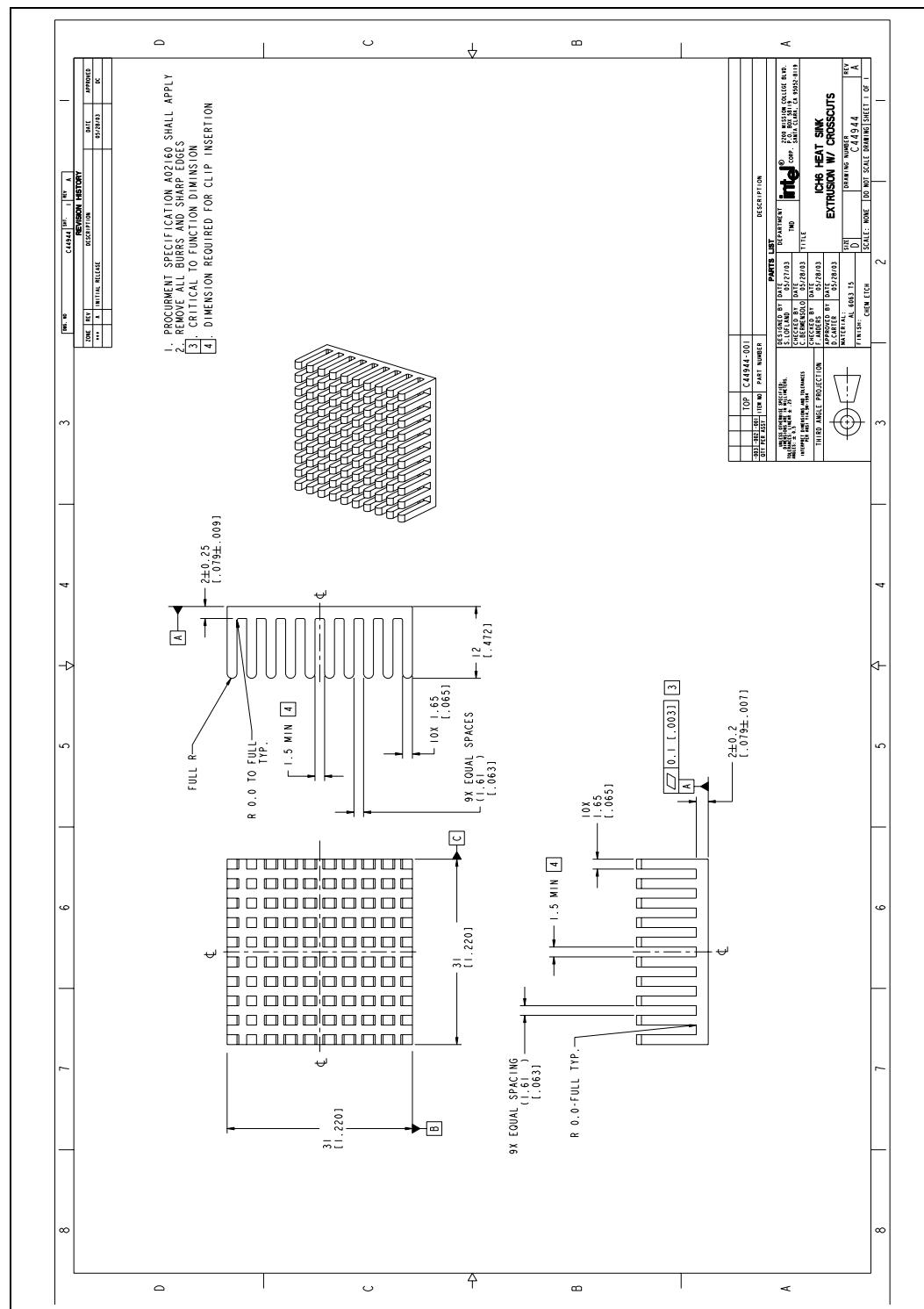
**Figure B-2. Motherboard Keep-Out for ATX Reference Heatsink**



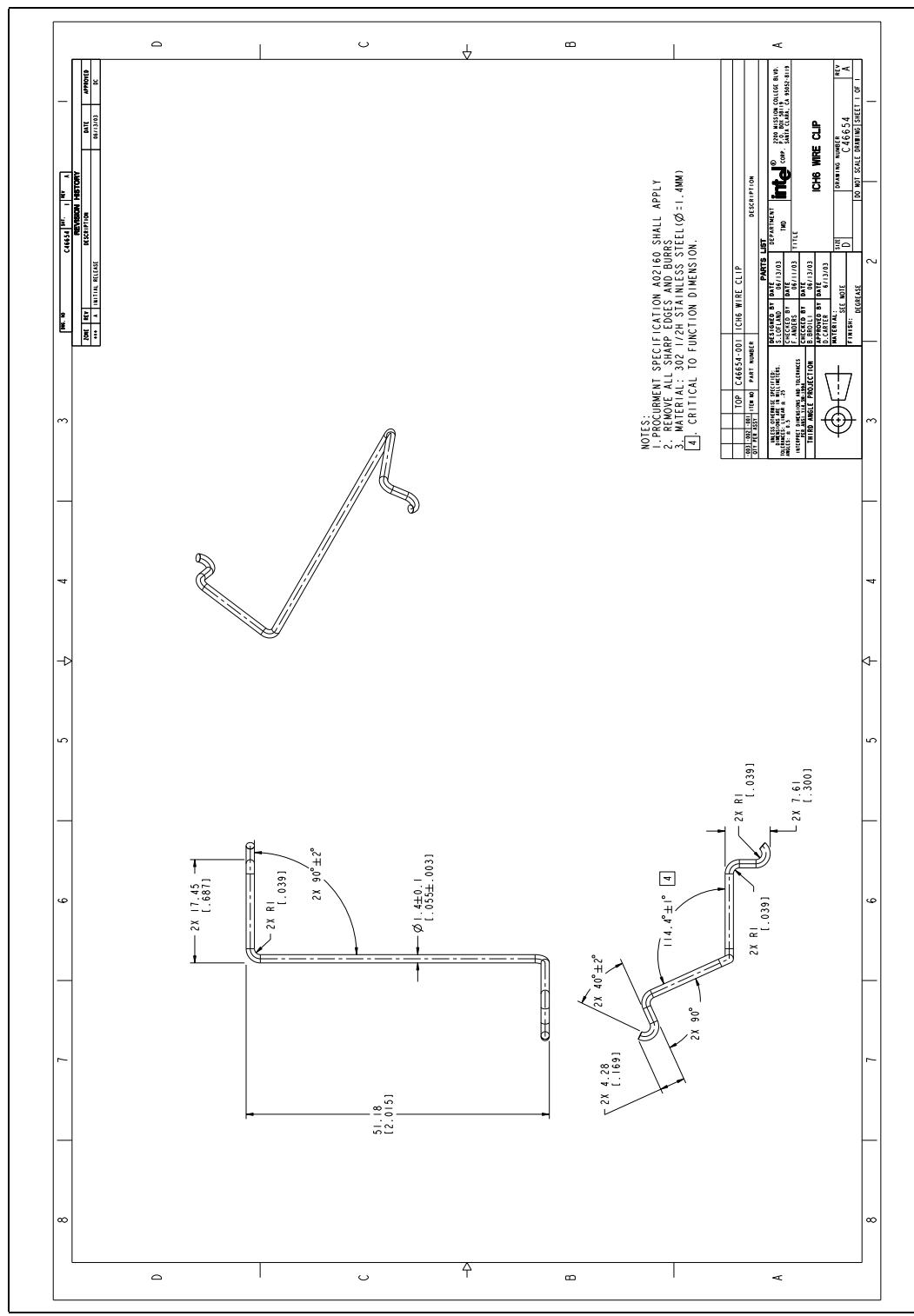
**Figure B-3. ATX Reference Heatsink Assembly**



**Figure B-4. ATX Reference Heatsink Extrusion**



**Figure B-5. ATX Reference Heatsink Clip**



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