



Mobile Intel[®] Pentium[®] 4 Processor with 533 MHz Front Side Bus

Datasheet

January 2004



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Revision History

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253028	001	Initial release of the Datasheet	June 2003
253028	002	Updates include: <ul style="list-style-type: none">• Added Intel HyperThreading Technology and 3.2-GHz specs• Updated terminology "System Bus" to "Front Side Bus (FSB)"	September 2003
253028	003	Updates include: <ul style="list-style-type: none">• Updated Figure 13, "Processor Markings"	December 2003
253028	004	Updates include: <ul style="list-style-type: none">• Updated Table 17, "Description Table for Processor Dimensions"	January 2004

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1 Introduction

The mobile Intel® Pentium® 4 processor with 533 MHz FSB is based on the Intel NetBurst™ micro-architecture. The mobile Intel Pentium 4 processor with 533-MHz FSB utilizes a 478-pin Flip-Chip Pin Grid Array (FC-PGA2) package with an integrated heat spreader, and plugs into a surface-mount, Zero Insertion Force (ZIF) socket. The mobile Intel Pentium 4 processor maintains full compatibility with IA-32 software. In this document the mobile Intel Pentium 4 processor with 533 MHz FSB will be referred to as the “mobile Intel Pentium 4 processor with 533 MHz FSB”, or “mobile Intel Pentium 4 processor”, or simply “the processor”.

The mobile Intel® Pentium® 4 processor with 533 MHz FSB supports Hyper-Threading Technology, which allows a single, physical processor to function as two logical processors. While some execution resources such as caches, execution units, and buses are shared, each logical processor has its own architecture state with its own set of general-purpose registers, control registers to provide increased system responsiveness in multitasking environments, and headroom for next generation multithreaded applications. Intel recommends enabling Hyper-Threading Technology with Microsoft Windows* XP Professional or Windows* XP Home, and disabling Hyper-Threading Technology via the BIOS for all previous versions of Windows operating systems. For more information on Hyper-Threading Technology, see www.intel.com/info/hyperthreading. Refer to [Section 7.1](#) for Hyper-Threading Technology configuration details.

The Intel NetBurst micro-architecture features include hyper-pipelined technology, a rapid execution engine, a 533-MHz FSB, and an execution trace cache. The hyper pipelined technology doubles the pipeline depth in the mobile Intel Pentium 4 processor allowing the processor to reach much higher core frequencies. The rapid execution engine allows the two integer ALUs in the processor to run at twice the core frequency, which allows many integer instructions to execute in 1/2 clock tick. The 533-MHz FSB is a quad-pumped bus running off a 133-MHz system clock making 4.3 GB/sec data transfer rates possible. The execution trace cache is a first level cache that stores approximately 12-k decoded micro-operations, which removes the instruction decoding logic from the main execution path, thereby increasing performance.

Additional features within the Intel NetBurst micro-architecture include advanced dynamic execution, advanced transfer cache, enhanced floating point and multi-media unit, and Streaming SIMD Extensions 2 (SSE2). The advanced dynamic execution improves speculative execution and branch prediction internal to the processor. The advanced transfer cache is a 512-kB, on-die level 2 (L2) cache. A newly implemented floating point and multi media unit provides superior performance for multi-media and mathematically intensive applications. Finally, SSE2 adds 144 new instructions for double-precision floating point, SIMD integer, and memory management. Power management capabilities such as AutoHALT, Stop-Grant, Sleep, Deep Sleep, and Deeper Sleep have been incorporated. The processor includes an address bus powerdown capability which removes power from the address and data pins when the FSB is not in use. This feature is always enabled on the processor.

The Streaming SIMD Extensions 2 (SSE2) enable break-through levels of performance in multimedia applications including 3-D graphics, video decoding/encoding, and speech recognition. The new packed, double-precision, floating-point instructions enhance performance for applications that require greater range and precision, including scientific and engineering applications and advanced 3-D geometry techniques, such as ray tracing.

The processor's 533 MHz Intel NetBurst micro-architecture FSB utilizes a split-transaction, deferred reply protocol like the Intel Pentium 4 processor. This FSB is not compatible with the P6 processor family bus. The 533-MHz Intel NetBurst micro-architecture FSB uses Source-Synchronous Transfer (SST) of address and data to improve performance by transferring data four times per bus clock (4X data transfer rate, as in AGP 4X). Along with the 4X data bus, the address bus can deliver addresses two times per bus clock and is referred to as a "double-clocked" or 2X address bus. Working together, the 4X data bus and 2X address bus provide a data bus bandwidth of up to 4.3 Gbytes/second.

The processor, when used in conjunction with the requisite Intel SpeedStep[®] technology applet or its equivalent, supports Enhanced Intel SpeedStep technology, which enables real-time dynamic switching of the voltage and frequency between two performance modes. This occurs by switching the bus ratios, core operating voltage, and core processor speeds without resetting the system.

The processor FSB uses GTL+ signalling technology. The mobile Intel Pentium 4 processor with 533 MHz FSB is expected to be available at the following core frequencies:

- 3.20 GHz (in Maximum Performance Mode at 1.55 V). This processor runs at 1.60 GHz (in Battery Optimized Mode at 1.20 V)
- 3.06 GHz (in Maximum Performance Mode at 1.55 V). This processor runs at 1.60 GHz (in Battery Optimized Mode at 1.20 V)
- 2.80 GHz (in Maximum Performance Mode at 1.525 V). This processor runs at 1.60 GHz (in Battery Optimized Mode at 1.20 V)
- 2.66 GHz (in Maximum Performance Mode at 1.525 V). This processor runs at 1.60 GHz (in Battery Optimized Mode at 1.20 V)
- 2.40 GHz (in Maximum Performance Mode at 1.525 V). This processor runs at 1.60 GHz (in Battery Optimized Mode at 1.20 V)

1.1 Terminology

A “#” symbol after a signal name refers to an active low signal, indicating a signal is in the active state when driven to a low level. For example, when RESET# is low, a reset has been requested. Conversely, when NMI is high, a nonmaskable interrupt has occurred. In the case of signals where the name does not imply an active state but describes part of a binary sequence (such as *address* or *data*), the “#” symbol implies that the signal is inverted. For example, D[3:0] = “HLHL” refers to a hex “A”, and D[3:0]# = “LHLH” also refers to a hex “A” (H= High logic level, L= Low logic level).

“Front Side Bus (FSB)” refers to the interface between the processor and system core logic (a.k.a. the chipset components). The FSB is a multiprocessing interface to processors, memory, and I/O.

Commonly used terms are explained here for clarification:

- **Processor** — For this document, the term processor shall mean the mobile Intel Pentium 4 processor with 533 MHz FSB in the 478-pin package.
- **Keep out zone** — The area on or near the processor that system design can not utilize.
- **Intel 852 GME/PM chipsets** — Mobile chipset that will support the mobile Intel Pentium 4 processor with 533 MHz FSB.
- **Processor core** — Mobile Intel Pentium 4 processor with 533 MHz FSB core die with integrated L2 cache.

- **FC-PGA2 package** — Flip-Chip Pin Grid Array package with 50-mil pin pitch and Integrated Heat Spreader
- **Integrated heat spreader** — The surface used to make contact between a heatsink or other thermal solution and the processor. Abbreviated IHS.

1.2 References

Material and concepts available in the following documents may be beneficial when reading this document.

Table 1. References

Document	Order Number
<i>Intel[®] 852GM/852PM Chipset Platforms Design Guide</i>	http://developer.intel.com
<i>Intel[®] Mobile Processor Micro-FCPGA Package and Socket Manufacturing and Mechanical User's Guide</i>	http://developer.intel.com
<i>Intel[®] 852GM Chipset Datasheet</i>	http://developer.intel.com
<i>Intel[®] Architecture Software Developer's Manual</i>	http://developer.intel.com
<i>Mobile Intel[®] Pentium[®] 4 Processor with 533 MHz FSB Specification Update</i>	253176
<i>Volume I: Basic Architecture</i>	
<i>Volume II: Instruction Set Reference</i>	
<i>Volume III: System Programming Guide</i>	
<i>Mobile Intel[®] Pentium[®] 4 Processor Thermal Design Guidelines for Transportable Systems</i>	
<i>Intel[®] Pentium[®] 4 Processor in the 478-pin Package Processor FloTherm models</i>	
<i>ITP700 Debug Port Design Guide</i>	http://developer.intel.com

NOTE: Contact your Intel representative for the latest revision and order number of this document.

1.3 State of Data

The data contained within this document represents the most accurate post-silicon information available by the publication date. However, all data in this document is subject to change.

2 Electrical Specifications

2.1 FSB and GTLREF

Most mobile Intel Pentium 4 processor FSB signals use Gunning Transceiver Logic (GTL+) signalling technology. As with the Intel P6 family of microprocessors, this signalling technology provides improved noise margins and reduced ringing through low-voltage swings and controlled edge rates. The termination voltage level for the mobile Intel Pentium 4 processor GTL+ signals is V_{CC} , which is the operating voltage of the processor core. Previous generations of Intel mobile processors utilize a fixed termination voltage known as V_{CCT} . The use of a termination voltage that is determined by the processor core allows better voltage scaling on the FSB for mobile Intel Pentium 4 processor. Because of the speed improvements to data and address bus, signal integrity and platform design methods have become more critical than with previous processor families. Design guidelines for the mobile Intel Pentium 4 processor FSB will be detailed in the appropriate platform design guidelines document listed in [Table 1](#).

The GTL+ inputs require a reference voltage (GTLREF), which is used by the receivers to determine if a signal is a logical 0 or a logical 1. GTLREF must be generated on the system board.

Termination resistors are provided on the processor silicon and are terminated to its core voltage (V_{CC}). Intel's 852GME/852PM chipsets will also provide on-die termination, thus eliminating the need to terminate the bus on the system board for most GTL+ signals. However, some GTL+ signals do not include on-die termination and must be terminated on the system board. For more information, refer to the appropriate platform design guidelines document listed in [Table 1](#).

The GTL+ bus depends on incident wave switching. Therefore, timing calculations for GTL+ signals are based on flight time as opposed to capacitive deratings. Analog signal simulation of the FSB, including trace lengths, is highly recommended when designing a system.

2.2 Power and Ground Pins

For clean on-chip power distribution, the mobile Intel Pentium 4 processor have 85 V_{CC} (power) and 181 V_{SS} (ground) inputs. All power pins must be connected to V_{CC} , while all V_{SS} pins must be connected to a system ground plane. The processor V_{CC} pins must be supplied with the voltage determined by the VID (Voltage ID) pins and the loadline specifications (see [Figure 3](#)).

2.3 Decoupling Guidelines

Due to its large number of transistors and high internal clock speeds, the processor is capable of generating large average current swings between low and full power states. This may cause voltages on power planes to sag below their minimum values if bulk decoupling is not adequate. Care must be taken in the board design to ensure that the voltage provided to the processor remains within the specifications listed in [Table 7](#). Failure to do so can result in timing violations and/or affect the long term reliability of the processor. For further information and design guidelines, refer to the appropriate platform design guidelines listed in [Table 1](#).

2.3.1 V_{CC} Decoupling

Regulator solutions need to provide bulk capacitance with a low Effective Series Resistance (ESR) and keep a low interconnect resistance from the regulator to the socket. Bulk decoupling for the large current swings when the part is powering on, or entering/exiting low-power states, must be provided by the voltage regulator solution. For more details on decoupling recommendations, please refer to the appropriate platform design guidelines listed in [Table 1](#).

2.3.2 FSB GTL+ Decoupling

The mobile Intel Pentium 4 processor integrates signal termination on the die and incorporates high-frequency, decoupling capacitance on the processor package. Decoupling must also be provided by the system motherboard for proper GTL+ bus operation. For more information, refer to the appropriate platform design guidelines listed in [Table 1](#).

2.4 Voltage Identification

The voltage set by the VID pins is the maximum voltage allowed by the processor. A minimum voltage is provided in [Table 7](#) and changes with frequency. This allows processors running at a higher frequency to have a relaxed minimum voltage specification. The specifications have been set such that one voltage regulator can work with all supported frequencies.

The mobile Intel Pentium 4 processor uses five voltage identification pins, VID[4:0], to support automatic selection of power supply voltages. The VID pins for the mobile Intel Pentium 4 processor are open drain outputs driven by the processor VID circuitry. The VID signals rely on pull-up resistors tied to a 3.3-V (max) supply to set the signal to a logic high level. These pull-up resistors may be either external logic on the motherboard or internal to the Voltage Regulator. [Table 3](#) specifies the voltage level corresponding to the state of VID[4:0]. A 1 in this table refers to a high-voltage level and a 0 refers to low-voltage level. If the processor socket is empty (VID[4:0] = 11111), or the voltage regulation circuit cannot supply the voltage that is requested, it must disable itself.

Power source characteristics must be stable whenever the supply to the voltage regulator is stable. Refer to the [Figure 14](#) for timing details of the power up sequence. Also refer to appropriate platform design guidelines listed in [Table 1](#) for implementation details.

Mobile Intel Pentium 4 processor's Voltage Identification circuit requires an independent 1.2-V supply. This voltage must be routed to the processor VCCVID pin. [Figure 1](#) and [Table 2](#) show the voltage and current requirements of the VCCVID pin.

Table 2. VCCVID Pin Voltage Requirements

Symbol	Parameter	Min	Typ	Max	Unit
VCCVID	Vcc for voltage identification circuit	-5%	1.2	+10%	V

NOTE: This specification applies to both static and transient components. The rising edge of VCCVID must be monotonic from 0 to 1.1 V. See [Figure 1](#) for current requirements. In this case, monotonic is defined as continuously increasing with less than 50 mV of peak to peak noise for any width greater than 2 nS superimposed on the rising edge.

Figure 1. VCCVID Pin Voltage and Current Requirements

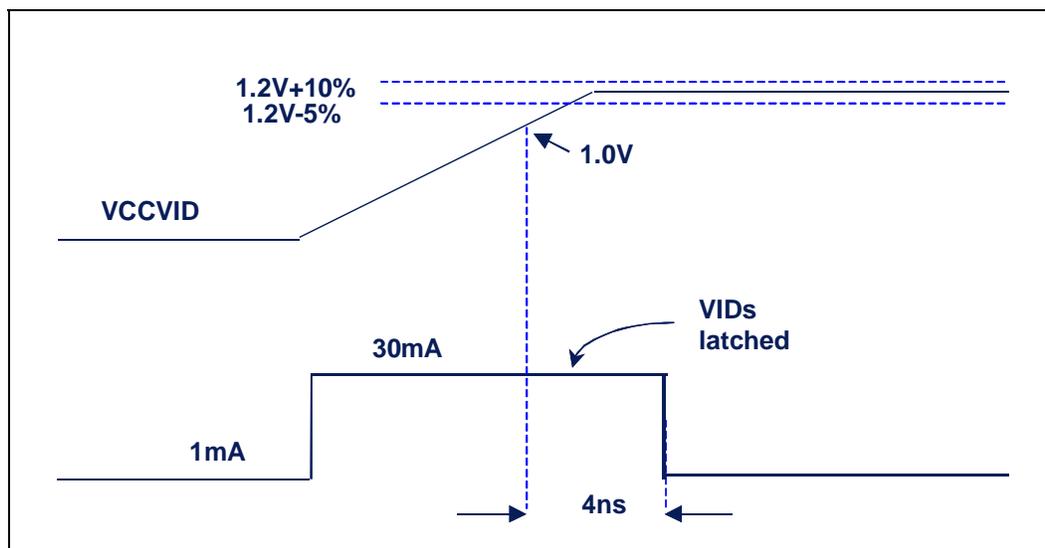


Table 3. Voltage Identification Definition (Sheet 1 of 2)

Processor Pins					
VID4	VID3	VID2	VID1	VID0	V _{CC_MAX}
1	1	1	1	1	VRM output off
1	1	1	1	0	1.100
1	1	1	0	1	1.125
1	1	1	0	0	1.150
1	1	0	1	1	1.175
1	1	0	1	0	1.200
1	1	0	0	1	1.225
1	1	0	0	0	1.250
1	0	1	1	1	1.275
1	0	1	1	0	1.300
1	0	1	0	1	1.325
1	0	1	0	0	1.350
1	0	0	1	1	1.375
1	0	0	1	0	1.400
1	0	0	0	1	1.425
1	0	0	0	0	1.450
0	1	1	1	1	1.475
0	1	1	1	0	1.500
0	1	1	0	1	1.525
0	1	1	0	0	1.550
0	1	0	1	1	1.575

Table 3. Voltage Identification Definition (Sheet 2 of 2)

0	1	0	1	0	1.600
0	1	0	0	1	1.625
0	1	0	0	0	1.650

2.4.1 Enhanced Intel SpeedStep® Technology

The mobile Intel Pentium 4 processor, when used in conjunction with the requisite Intel SpeedStep® technology applet or its equivalent, supports Enhanced Intel SpeedStep technology. Enhanced Intel SpeedStep technology allows the processor to switch between two core frequencies automatically based on CPU demand, without having to reset the processor or change the FSB frequency. The processor operates in two modes, the Maximum Performance mode or the Battery Optimized mode. Each frequency and voltage pair identifies the operating mode. The processor drives the VID[4:0] pins with the correct VID for the current operating mode. After reset, the processor will start in Battery Optimized mode. Any RESET# assertion will force the processor to the Battery Optimized mode. INIT# assertions ("soft" resets) and APIC bus INIT messages do not change the operating mode of the processor. Some electrical and thermal specifications are for a specific voltage and frequency. The mobile Intel Pentium 4 processor featuring Enhanced Intel SpeedStep technology will meet the electrical and thermal specifications specific to the current operating mode, and it is not guaranteed to meet the electrical and thermal specifications specific to the opposite operating mode. The timing specifications must be met when performing an operating mode transition.

2.4.2 Phase Lock Loop (PLL) Power and Filter

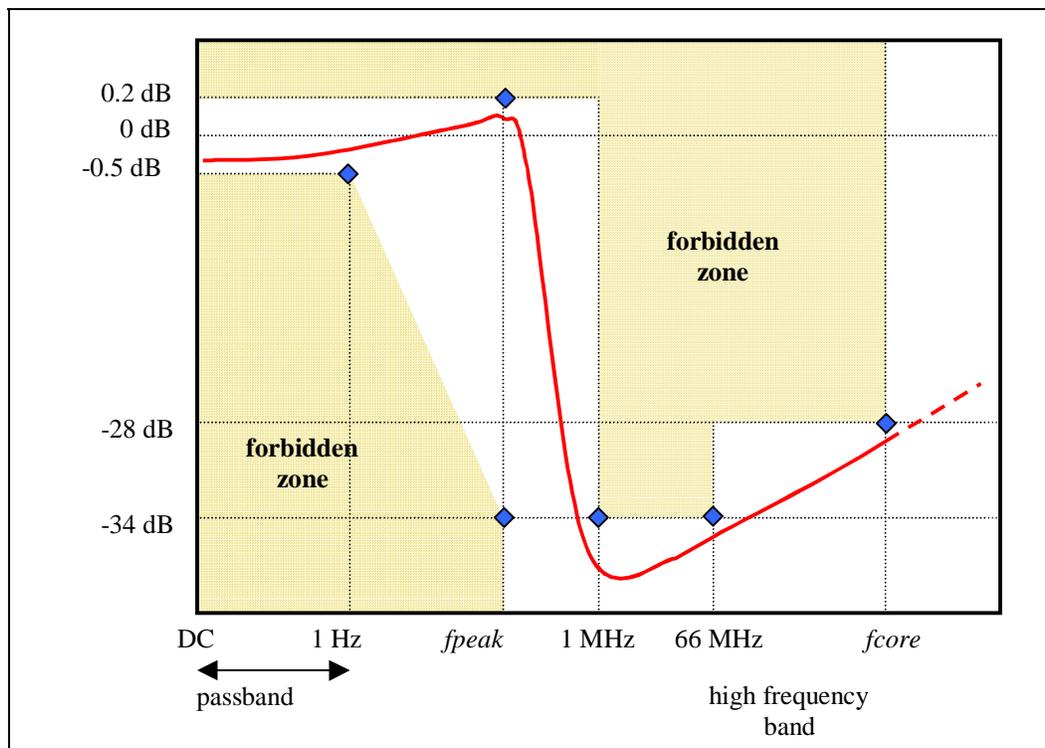
V_{CCA} and $V_{CCIOPLL}$ are power sources required by the PLL clock generators on the mobile Intel Pentium 4 processor silicon. Since these PLLs are analog in nature, they require quiet power supplies for minimum jitter. Jitter is detrimental to the system: it degrades external I/O timings as well as internal core timings (i.e. maximum frequency). To prevent this degradation, these supplies must be low pass filtered from V_{CC} .

The AC low-pass requirements, with input at V_{CCVID} is as follows:

- < 0.2 dB gain in pass band
- < 0.5 dB attenuation in pass band < 1 Hz
- > 34 dB attenuation from 1 MHz to 66 MHz
- > 28 dB attenuation from 66 MHz to core frequency

The filter requirements are illustrated in [Figure 2](#). For recommendations on implementing the filter, refer to the appropriate platform design guidelines listed in [Table 1](#).

Figure 2. Phase Lock Loop (PLL) Filter Requirements



- NOTES:**
1. Diagram not to scale.
 2. No specification for frequencies beyond f_{core} (core frequency).
 3. f_{peak} , if existent, should be less than 0.05 MHz.

2.4.3 Catastrophic Thermal Protection

The mobile Intel Pentium 4 processor supports the THERMTRIP# signal for catastrophic thermal protection. Alternatively, an external thermal sensor can be used to protect the processor and the system against excessive temperatures. Even with the activation of THERMTRIP#, which halts all processor internal clocks and activity, leakage current can be high enough such that the processor cannot be protected in all conditions without the removal of power to the processor. If the external thermal sensor detects a catastrophic processor temperature of 135°C (maximum), or if the THERMTRIP# signal is asserted, the VCC supply to the processor must be turned off within 500 ms to prevent permanent silicon damage due to thermal runaway of the processor. Refer to Section 4.2 for more details on THERMTRIP#.

2.5 Signal Terminations, Unused Pins, and TESTHI[10:0]

All NC pins must remain unconnected. Connection of these pins to V_{CC} , V_{SS} , or to any other signal (including each other) can result in component malfunction or incompatibility with future mobile Intel Pentium 4 processors. See Section 5.2 for a pin listing of the processor and the location of all NC pins.

For reliable operation, always connect unused inputs or bidirectional signals that are not terminated on the die to an appropriate signal level. Note that on-die termination has been included on the mobile Intel Pentium 4 processor to allow signals to be terminated within the processor silicon. Unused active low GTL+ inputs may be left as no connects if GTL+ termination is provided on the processor silicon. Table 4 lists details on GTL+ signals that do not include on-die termination. Unused active high inputs should be connected through a resistor to ground (V_{SS}). Refer to the platform design guidelines listed in Table 1 for the appropriate resistor values.

Unused outputs can be left unconnected, however, this may interfere with some TAP functions, complicate debug probing, and prevent boundary scan testing. A resistor must be used when tying bidirectional signals to power or ground. When tying any signal to power or ground, a resistor will also allow for system testability. For unused GTL+ input or I/O signals that don't have on-die termination, use pull-up resistors of the same value in place of the on-die termination resistors (R_{TT}). See Table 16.

The TAP, Asynchronous GTL+ inputs, and Asynchronous GTL+ outputs do not include on-die termination. Inputs and used outputs must be terminated on the system board. Unused outputs may be terminated on the system board or left unconnected. Note that leaving unused outputs unterminated may interfere with some TAP functions, complicate debug probing, and prevent boundary scan testing. Signal termination for these signal types is discussed in the appropriate platform design guidelines listed in Table 1. TAP signal termination requirements are also discussed in *ITP700 Debug Port Design Guide*.

The TESTHI pins should be tied to the processor V_{CC} using a matched resistor, where a matched resistor has a resistance value within $\pm 20\%$ of the impedance of the board transmission line traces. For example, if the trace impedance is $50\ \Omega$, then a value between $40\ \Omega$ and $60\ \Omega$ is required.

The TESTHI pins may use individual pull-up resistors or be grouped together as detailed below. A matched resistor should be used for each group:

1. TESTHI[1:0]
2. TESTHI[5:2]
3. TESTHI[10:8]

Additionally, if the ITPCLKOUT[1:0] pins are not used then they may be connected individually to V_{CC} using matched resistors or grouped with TESTHI[5:2] with a single matched resistor. If they are being used, individual termination with 1-k Ω resistors is required. Tying ITPCLKOUT[1:0] directly to V_{CC} or sharing a pull-up resistor to V_{CC} will prevent use of debug interposers. This implementation is strongly discouraged for system boards that do not implement an onboard debug port.

As an alternative, group 2 (TESTHI[5:2]), and the ITPCLKOUT[1:0] pins may be tied directly to the processor V_{CC} . This has no impact on system functionality. TESTHI[0] may also be tied directly to processor V_{CC} if resistor termination is a problem, but matched resistor termination is recommended. In the case of the ITPCLKOUT[1:0] pins, direct tie to V_{CC} is strongly discouraged for system boards that do not implement an onboard debug port.

Tying any of the TESTHI pins together will prevent the ability to perform boundary scan testing.

Pullup/down resistor requirements for the VID[4:0] and BSEL[1:0] signals are included in the signal descriptions in [Section 4](#).

2.6 FSB Signal Groups

In order to simplify the following discussion, the FSB signals have been combined into groups by buffer type. GTL+ input signals have differential input buffers, which use GTLREF as a reference level. In this document, the term "GTL+ Input" refers to the GTL+ input group as well as the GTL+ I/O group when receiving. Similarly, "GTL+ Output" refers to the GTL+ output group as well as the GTL+ I/O group when driving.

With the implementation of a source synchronous data bus comes the need to specify two sets of timing parameters. One set is for common clock signals that are dependant upon the rising edge of BCLK0 (ADS#, HIT#, HITM#, etc.) and the second set is for the source synchronous signals which are relative to their respective strobe lines (data and address) as well as the rising edge of BCLK0. Asynchronous signals are still present (A20M#, IGNNE#, etc.) and can become active at any time during the clock cycle. [Table 4](#) identifies which signals are common clock, source synchronous, and asynchronous.

Table 4. FSB Pin Groups

Signal Group	Type	Signals ¹														
GTL+ Common Clock Input	Common clock	BPRI#, DEFER#, RESET# ² , RS[2:0]#, RSP#, TRDY#														
GTL+ Common Clock I/O	Synchronous	AP[1:0]#, ADS#, BINIT#, BNR#, BPM[5:0]# ² , BR0# ² , DBSY#, DP[3:0]#, DRDY#, HIT#, HITM#, LOCK#, MCERR#														
GTL+ Source Synchronous I/O	Source Synchronous	<table border="1"> <thead> <tr> <th>Signals</th> <th>Associated Strobe</th> </tr> </thead> <tbody> <tr> <td>REQ[4:0]#, A[16:3]#⁵</td> <td>ADSTB0#</td> </tr> <tr> <td>A[35:17]#⁵</td> <td>ADSTB1#</td> </tr> <tr> <td>D[15:0]#, DBI0#</td> <td>DSTBP0#, DSTBN0#</td> </tr> <tr> <td>D[31:16]#, DBI1#</td> <td>DSTBP1#, DSTBN1#</td> </tr> <tr> <td>D[47:32]#, DBI2#</td> <td>DSTBP2#, DSTBN2#</td> </tr> <tr> <td>D[63:48]#, DBI3#</td> <td>DSTBP3#, DSTBN3#</td> </tr> </tbody> </table>	Signals	Associated Strobe	REQ[4:0]#, A[16:3]# ⁵	ADSTB0#	A[35:17]# ⁵	ADSTB1#	D[15:0]#, DBI0#	DSTBP0#, DSTBN0#	D[31:16]#, DBI1#	DSTBP1#, DSTBN1#	D[47:32]#, DBI2#	DSTBP2#, DSTBN2#	D[63:48]#, DBI3#	DSTBP3#, DSTBN3#
		Signals	Associated Strobe													
		REQ[4:0]#, A[16:3]# ⁵	ADSTB0#													
		A[35:17]# ⁵	ADSTB1#													
		D[15:0]#, DBI0#	DSTBP0#, DSTBN0#													
		D[31:16]#, DBI1#	DSTBP1#, DSTBN1#													
		D[47:32]#, DBI2#	DSTBP2#, DSTBN2#													
D[63:48]#, DBI3#	DSTBP3#, DSTBN3#															
GTL+ Strobes	Common Clock	ADSTB[1:0]#, DSTBP[3:0]#, DSTBN[3:0]#														
Asynchronous GTL+ Input ^{4,5}	Asynchronous	A20M#, DPSLP#, GHI#, IGNNE#, INIT# ⁵ , LINT0/INTR, LINT1/NMI, SMI# ⁵ , SLP#, STPCLK#														
Asynchronous GTL+ Output ⁴	Asynchronous	FERR#/PBE#, IERR# ² , THERMTRIP#														
Asynchronous GTL+ Input/Output ⁴	Asynchronous	PROCHOT#														
TAP Input ⁴	Synchronous to TCK	TCK, TDI, TMS, TRST#														
TAP Output ⁴	Synchronous to TCK	TDO														
FSB Clock	N/A	BCLK[1:0], ITP_CLK[1:0] ³														
Power/Other	N/A	V _{CC} , V _{CCA} , V _{CCIOPLL} , V _{CCVID} , VID[4:0], V _{SS} , V _{SSA} , GTLREF[3:0], COMP[1:0], NC, TESTHI[5:0], TESTHI[10:8], ITPCLKOUT[1:0], PWRGOOD, THERMDA, THERMDC, SKTOCC#, V _{CC_SENSE} , V _{SS_SENSE} , BSEL[1:0], DBR# ³														

NOTES:

1. Refer to [Section 4.2](#) for signal descriptions.
2. These GTL+ signals do not have on-die termination. Refer to [Section 2.5](#) and the *ITP700 Debug Port Design Guide* for termination requirements.
3. In processor systems where there is no debug port implemented on the system board, these signals are used to support a debug port interposer. In systems with the debug port implemented on the system board, these signals are no connects.
4. These signal groups are not terminated by the processor. Signals not driven by the ICH4-M component must be terminated on the system board. Refer to [Section 2.5](#), the *ITP700 Debug Port Design Guide*, and the appropriate platform design guidelines listed in [Table 1](#) for termination requirements and further details.
5. The value of these pins during the active-to-inactive edge of RESET# defines the processor configuration options. See [Section 6.1](#) for details.

2.7 Asynchronous GTL+ Signals

Mobile Intel Pentium 4 processor does not utilize CMOS voltage levels on any signals that connect to the processor. As a result, legacy input signals such as A20M#, IGNNE#, INIT#, LINT0/INTR, LINT1/NMI, SMI#, SLP#, and STPCLK# use GTL+ input buffers. Legacy output FERR#/PBE# and other non-GTL+ signals (THERMTRIP#) utilize GTL+ output buffers. PROCHOT# uses GTL+ input/output buffer. All of these signals follow the same DC requirements as GTL+ signals, however the outputs are not actively driven high (during a logical 0 to 1 transition) by the processor. These signals do not have setup or hold time specifications in relation to BCLK[1:0]. However, all of the Asynchronous GTL+ signals are required to be asserted for at least two BCLKs in order for the processor to recognize them. See [Section 2.11](#) for the DC and AC specifications for the Asynchronous GTL+ signal groups. See [Section 6.2](#) for additional timing requirements for entering and leaving the low power states.

2.8 Test Access Port (TAP) Connection

Due to the voltage levels supported by other components in the Test Access Port (TAP) logic, it is recommended that the mobile Intel Pentium 4 processor be first in the TAP chain and followed by any other components within the system. A translation buffer should be used to connect to the rest of the chain unless one of the other components is capable of accepting an input of the appropriate voltage level. Similar considerations must be made for TCK, TMS, and TRST#. Two copies of each signal may be required, with each driving a different voltage level. Refer to *ITP700 Debug Port Design Guide* for more detailed information.

2.9 FSB Frequency Select Signals (BSEL[1:0])

The BSEL[1:0] are output signals used to select the frequency of the processor input clock (BCLK[1:0]). [Table 5](#) defines the possible combinations of the signals and the frequency associated with each combination. The required frequency is determined by the processor, chipset, and clock synthesizer. All agents must operate at the same frequency.

The mobile Intel Pentium 4 processor with 533 MHz FSB currently operates at a 533-MHz FSB frequency (selected by a 133-MHz BCLK[1:0] frequency). Individual processors will only operate at their specified FSB frequency.

For more information about these pins refer to [Section 4.2](#) and the appropriate platform design guidelines.

Table 5. BSEL[1:0] Frequency Table for BCLK[1:0]

BSEL1	BSEL0	Function
L	L	RESERVED
L	H	133 MHz
H	L	RESERVED
H	H	RESERVED

2.10 Maximum Ratings

Table 6 lists the processor's maximum environmental stress ratings. The processor should not receive a clock while subjected to these conditions. Functional operating parameters are listed in the AC and DC tables. Extended exposure to the maximum ratings may affect device reliability. Furthermore, although the processor contains protective circuitry to resist damage from electrostatic discharge (ESD), one should always take precautions to avoid high static voltages or electric fields.

Table 6. Processor DC Absolute Maximum Ratings

Symbol	Parameter	Min	Max	Unit	Notes
T _{STORAGE}	Processor storage temperature	-40	85	°C	2
V _{CC}	Any processor supply voltage with respect to V _{SS}	-0.3	1.75	V	1
V _{inGTL+}	GTL+ buffer DC input voltage with respect to V _{SS}	-0.1	1.75	V	
V _{inAsynch_GTL+}	Asynch GTL+ buffer DC input voltage with respect to V _{SS}	-0.1	1.75	V	
I _{VID}	Max VID pin current		5	mA	

NOTES:

1. This rating applies to any processor pin.
2. Contact Intel for storage requirements in excess of one year.

2.11 Processor DC Specifications

The processor DC specifications in this section are defined at the processor core (pads) unless noted otherwise. See Chapter 5 for the pin signal definitions and signal pin assignments. Most of the signals on the processor FSB are in the GTL+ signal group. The DC specifications for these signals are listed in Table 10.

Previously, legacy signals and Test Access Port (TAP) signals to the processor used low-voltage CMOS buffer types. However, these interfaces now follow DC specifications similar to GTL+. The DC specifications for these signal groups are listed in Table 11 and Table 12.

Table 7 through Table 14 list the DC specifications for the mobile Intel Pentium 4 processor and are valid only while meeting specifications for case temperature, clock frequency, and input voltages. Care should be taken to read all notes associated with each parameter.

2.11.1 Fixed Mobile Solution (FMS)

The FMS guidelines are estimates of the maximum values the mobile Intel Pentium 4 processor will have over certain time periods. The values are only estimates and actual specifications for future processors may differ. The mobile Intel Pentium 4 processor may or may not have specifications equal to the FMS value in the foreseeable future. System designers should meet the FMS values to ensure their systems will be compatible with future releases of the mobile Intel Pentium 4 processor.

Table 7. Voltage and Current Specifications

Symbol	Parameter	Min	Typ	Max	Unit	Notes							
V _{CC}	V_{CC} for Processor at VID=1.200 V: 1.60 GHz	1.070	Refer to Table 9 and Figure 3	1.140	V	2,3,4,5,10							
	V_{CC} for Processor at VID=1.475 V: 2.40 GHz 2.66 GHz 2.80 GHz 3.06 GHz 3.20 GHz	1.300 1.295 1.290 1.265 1.260		1.380 1.370 1.370 1.345 1.350									
	V_{CC} for Processor at VID=1.500 V 2.40 GHz 2.66 GHz 2.80 GHz 3.06 GHz 3.20 GHz	1.325 1.320 1.315 1.290 1.285		1.405 1.395 1.395 1.370 1.370									
	V_{CC} for Processor at VID=1.525 V 2.40 GHz 2.66 GHz 2.80 GHz 3.06 GHz 3.20 GHz	1.355 1.345 1.340 1.315 1.310		1.430 1.420 1.420 1.395 1.395									
	V_{CC} for Processor at VID=1.550 V 3.06 GHz 3.20 GHz	1.340 1.335		1.425 1.420									
	I _{CC}	I_{CC} for Processor at VID=1.200 V: 1.60 GHz						34.1	A	4,5,7,10			
		I_{CC} for Processor with multiple VIDs: 2.40 GHz 2.66 GHz 2.80 GHz 3.06 GHz 3.20 GHz						50.7 53.9 55.9 65.4 67.4					
		V _{CCDPRSLP}		Static and Transient Deeper Sleep voltage			0.95	1.00			1.05	V	2
		I _{SGNT} I _{slp}		I _{CC} Stop-Grant at: VID = 1.200 V VID = 1.525 V VID = 1.550 V							20 23 25	A	6, 8, 10
		I _{TCC}		ICC TCC active							ICC	A	7
	I _{CC PLL}	ICC for PLL pins						60	mA	9			

NOTES:

1. Unless otherwise noted, all specifications in this table are based on the latest silicon measurements available at time of publication. Listed frequency and VID combinations are not necessarily committed production frequency and VID combinations.
2. These voltages are targets only. A variable voltage source should exist on systems in the event that a different voltage is required. See [Section 2.4](#) and [Table 3](#) for more information. The VID bits will set the maximum V_{CC} with the minimum being defined according to current consumption at that voltage.
3. The voltage specification requirements are measured across $V_{CCSENSE}$ and $V_{SSSENSE}$ pins at the socket with a 100-MHz bandwidth oscilloscope, 1.5-pF maximum probe capacitance, and 1-M Ω minimum impedance. The maximum length of ground wire on the probe should be less than 5 mm. Ensure external noise from the system is not coupled in the scope probe.
4. Refer to [Table 8](#), [Table 9](#), and [Figure 3](#) for the minimum, typical, and maximum V_{CC} allowed for a given current. The processor should not be subjected to any V_{CC} and I_{CC} combination wherein V_{CC} exceeds V_{CC_MAX} for a given current. Moreover, V_{CC} should never exceed the VID voltage. Failure to adhere to this specification can affect the long term reliability of the processor.
5. V_{CC_MIN} is defined at I_{CC_MAX} .
6. The current specified is also for AutoHALT state and applies to all frequencies.
7. The maximum instantaneous current the processor will draw while the thermal control circuit is active as indicated by the assertion of PROCHOT# is the same as the maximum I_{CC} for the processor.
8. I_{CC} Stop-Grant and I_{CC} Sleep are specified at V_{CC_MAX} .
9. The specification is defined per PLL pin.
10. The specifications for the Battery Optimized mode (1.60 GHz at 1.200 VID) are not 100% tested. These specifications are determined by characterization of the processor currents at higher voltage and frequency and extrapolating the values for the Battery Optimized mode voltage and frequency.

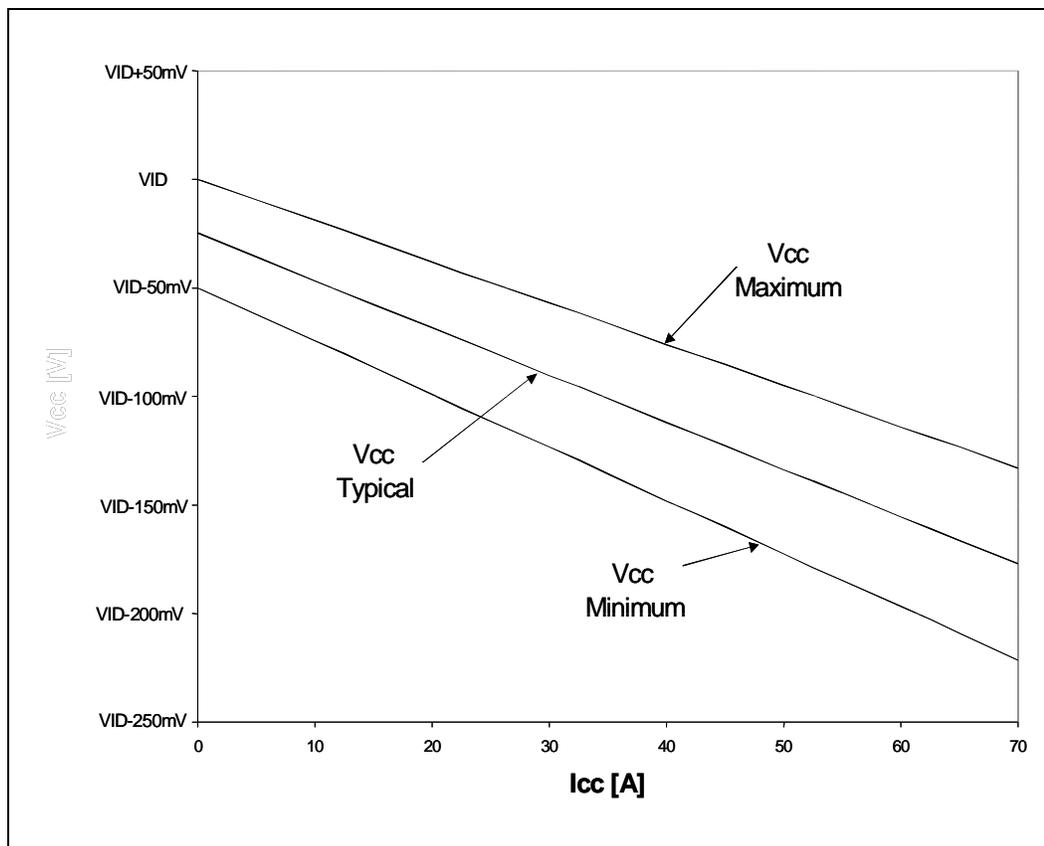
Table 8. V_{CC} Static and Transient Tolerance

I _{CC} (A)	Voltage Deviation from VID Setting (V) ^{1,2,3}		
	Maximum	Typical	Minimum
0	0.000	-0.025	-0.050
5	-0.010	-0.036	-0.062
10	-0.019	-0.047	-0.075
15	-0.029	-0.058	-0.087
20	-0.038	-0.069	-0.099
25	-0.048	-0.079	-0.111
30	-0.057	-0.090	-0.124
35	-0.067	-0.101	-0.136
40	-0.076	-0.112	-0.148
45	-0.085	-0.123	-0.160
50	-0.095	-0.134	-0.173
55	-0.105	-0.145	-0.185
60	-0.114	-0.156	-0.197
65	-0.124	-0.166	-0.209
70	-0.133	-0.177	-0.222

NOTES:

1. The loadline specifications include both static and transient limits.
2. This table is intended to aid in reading discrete points on the loadline figure below and applies to any VID setting.
3. The loadlines specify voltage limits at the die measured at V_{CCSENSE} and V_{SSSENSE} pins. Voltage regulation feedback for voltage regulator circuits must be taken from processor V_{CC} and V_{SS} pins.
4. Adherence to this loadline specification for the mobile Intel Pentium 4 processor with 533 MHz FSB is required to ensure reliable processor operation.

Figure 3. Vcc Static and Transient Tolerance



NOTES:

1. The loadline specification includes both static and transient limits.
2. Refer to [Table 8](#) for specific offsets from VID voltage which apply to all VID settings.
3. The loadlines specify voltage limits at the die measured at V_{CC_sense} and V_{SS_sense} pins. Voltage regulation feedback for voltage regulator circuits must be taken from processor V_{CC} and V_{SS} pins.
4. Adherence to this loadline specification for the mobile Intel Pentium 4 processor with 533 MHz FSB is required to ensure reliable processor operation.

Table 9. FSB Differential BCLK Specifications

Symbol	Parameter	Min	Typ	Max	Unit	Figure	Notes ¹
V_L	Input Low Voltage	-0.150	0.000	N/A	V	8	
V_H	Input High Voltage	0.660	0.700	0.850	V	8	
$V_{CROSS(abs)}$	Absolute Crossing Point	0.250	N/A	0.550	V	8, 9	2,3,8
$V_{CROSS(rel)}$	Relative Crossing Point	$0.250 + 0.5(V_{Havg} - 0.700)$	N/A	$0.550 + 0.5(V_{Havg} - 0.700)$	V	8, 9	2,3,8,9
ΔV_{CROSS}	Range of Crossing Points	N/A	N/A	0.140	V	8, 9	2,10
V_{OV}	Overshoot	N/A	N/A	$V_H + 0.3$	V	8	4
V_{US}	Undershoot	-0.300	N/A	N/A	V	8	5
V_{RBM}	Ringback Margin	0.200	N/A	N/A	V	8	6
V_{TM}	Threshold Margin	$V_{CROSS} - 0.100$	N/A	$V_{CROSS} + 0.100$	V	8	7

NOTES:

1. Unless otherwise noted, all specifications in this table apply to all processor frequencies.
2. Crossing voltage is defined as the instantaneous voltage value when the rising edge of BCLK0 equals the falling edge of BCLK1.
3. V_{Havg} is the statistical average of the V_H measured by the oscilloscope.
4. Overshoot is defined as the absolute value of the maximum voltage.
5. Undershoot is defined as the absolute value of the minimum voltage.
6. Ringback Margin is defined as the absolute voltage difference between the maximum Rising Edge Ringback and the maximum Falling Edge Ringback.
7. Threshold region is defined as a region entered around the crossing point voltage in which the differential receiver switches. It includes input threshold hysteresis.
8. The crossing point must meet the absolute and relative crossing point specifications simultaneously.
9. V_{Havg} can be measured directly using "Vtop" on Agilent* scopes and "High" on Tektronix* scopes.
10. ΔV_{CROSS} is defined as the total variation of all crossing voltages as defined in note 2.

Table 10. GTL+ Signal Group DC Specifications

Symbol	Parameter	Min	Max	Unit	Notes ¹
GTLREF	Reference Voltage	$2/3 V_{CC} - 2\%$	$2/3 V_{CC} + 2\%$	V	10
GTLREF_COMPATIBLE	Reference Voltage	$0.63 \cdot V_{CC} - 2\%$	$0.63 \cdot V_{CC} + 2\%$	V	10
V_{IH}	Input High Voltage	$1.10 \cdot \text{GTLREF}$	V_{CC}	V	2,6
V_{IL}	Input Low Voltage	0.0	$0.9 \cdot \text{GTLREF}$	V	3,4,6
V_{OH}	Output High Voltage	N/A	V_{CC}	V	7
I_{OL}	Output Low Current	N/A	50	mA	6
I_{HI}	Pin Leakage High	N/A	100	μA	8
I_{LO}	Pin Leakage Low	N/A	500	μA	9
R_{ON}	Buffer On Resistance	7	11	Ω	5, 11
$R_{ON_COMPATIBLE}$	Buffer On Resistance	8.4	13.2	Ω	5, 11

NOTES:

- Unless otherwise noted, all specifications in this table apply to all processor frequencies.
- V_{IL} is defined as the maximum voltage level at a receiving agent that will be interpreted as a logical low value.
- V_{IH} is defined as the minimum voltage level at a receiving agent that will be interpreted as a logical high value.
- V_{IH} and V_{OH} may experience excursions above V_{CC} . However, input signal drivers must comply with the signal quality specifications in Section 3.
- Refer to processor I/O Buffer Models for I/V characteristics.
- The V_{CC} referred to in these specifications is the instantaneous V_{CC} .
- V_{OL} max of 0.450 Volts is guaranteed when driving into a test load of 50 Ω as indicated in Figure 6.
- Leakage to V_{SS} with pin held at V_{CC} .
- Leakage to V_{CC} with pin held at 300 mV.
- For a platform to be forward compatible with future portable processors it must be designed to support an GTLREF value of $0.63 \cdot V_{CC} - 2\%$ (min) and $0.63 \cdot V_{CC} + 2\%$ (max). A compatible platform is one that is designed for some level of compatibility with future portable processors.
- For a platform to be forward compatible with future portable processors it must be designed to support an R_{on} value of 8.4 Ω (min) and 13.2 Ω (max). A compatible platform is one that is designed for some level of compatibility with future portable processors.

Table 11. Asynchronous GTL+ Signal Group DC Specifications

Symbol	Parameter	Min	Max	Unit	Notes ¹
V _{IH}	Input High Voltage Asynch GTL+	1.10*GTLREF	V _{CC}	V	3, 4, 5
V _{IL}	Input Low Voltage Asynch. GTL+	0	0.9*GTLREF	V	5
V _{OH}	Output High Voltage	N/A	V _{CC}	V	2, 3, 4
I _{OL}	Output Low Current	N/A	50	mA	6, 8
I _{HI}	Pin Leakage High	N/A	100	μA	9
I _{LO}	Pin Leakage Low	N/A	500	μA	10
R _{on}	Buffer On Resistance Asynch GTL+	7	11	Ω	5, 7
RON_COMPATIBLE	Buffer On Resistance Asynch GTL+	8.4	13.2	Ω	11

NOTES:

1. Unless otherwise noted, all specifications in this table apply to all processor frequencies.
2. All outputs are open-drain.
3. V_{IH} and V_{OH} may experience excursions above V_{CC}. However, input signal drivers must comply with the signal quality specifications in [Chapter 3](#).
4. The V_{CC} referred to in these specifications refers to instantaneous V_{CC}.
5. This specification applies to the asynchronous GTL+ signal group.
6. The maximum output current is based on maximum current handling capability of the buffer and is not specified into the test load shown in [Figure 6](#).
7. Refer to the processor I/O Buffer Models for I/V characteristics.
8. Vol max of 0.270 Volts is guaranteed when driving into a test load of 50 Ω as indicated in [Figure 6](#) for the Asynchronous GTL+ signals.
9. Leakage to V_{SS} with pin held at V_{CC}.
10. Leakage to V_{CC} with pin held at 300 mV.
11. For a platform to be forward compatible with future portable processors it must be designed to support an Ron value of 8.4 Ω (min) and 13.2 Ω (max). A compatible platform is one that is designed for some level of compatibility with future Portable processors.

Table 12. PWRGOOD and TAP Signal Group DC Specifications

Symbol	Parameter	Min	Max	Unit	Notes ¹
V _{HYS}	Input Hysteresis	200	300	mV	8
V _{T+}	Input Low to High Threshold Voltage	$1/2*(V_{CC}+V_{HYS_MIN})$	$1/2*(V_{CC}+V_{HYS_MAX})$	V	5
V _{T-}	Input High to Low Threshold Voltage	$1/2*(V_{CC}-V_{HYS_MAX})$	$1/2*(V_{CC}-V_{HYS_MIN})$	V	5
V _{OH}	Output High Voltage	N/A	V _{CC}	V	2,3,5
I _{OL}	Output Low Current	N/A	40	mA	6,7
I _{HI}	Pin Leakage High	N/A	100	μA	9
I _{LO}	Pin Leakage Low	N/A	500	μA	10
R _{on}	Buffer On Resistance	8.75	13.75	Ω	4

NOTES:

1. Unless otherwise noted, all specifications in this table apply to all processor frequencies.
2. All outputs are open-drain.
3. TAP signal group must comply with the signal quality specifications in [Chapter 3](#).
4. Refer to I/O Buffer Models for I/V characteristics.
5. The V_{CC} referred to in these specifications refers to instantaneous V_{CC}.
6. The maximum output current is based on maximum current handling capability of the buffer and is not specified into the test load shown in [Figure 6](#).
7. Vol max of 0.320 Volts is guaranteed when driving into a test load of 50 Ω as indicated in [Figure 6](#) for the TAP Signals.
8. V_{HYS} represents the amount of hysteresis, nominally centered about 1/2 V_{CC} for all TAP inputs.
9. Leakage to V_{SS} with pin held at V_{CC}.
10. Leakage to V_{CC} with pin held at 300 mV.

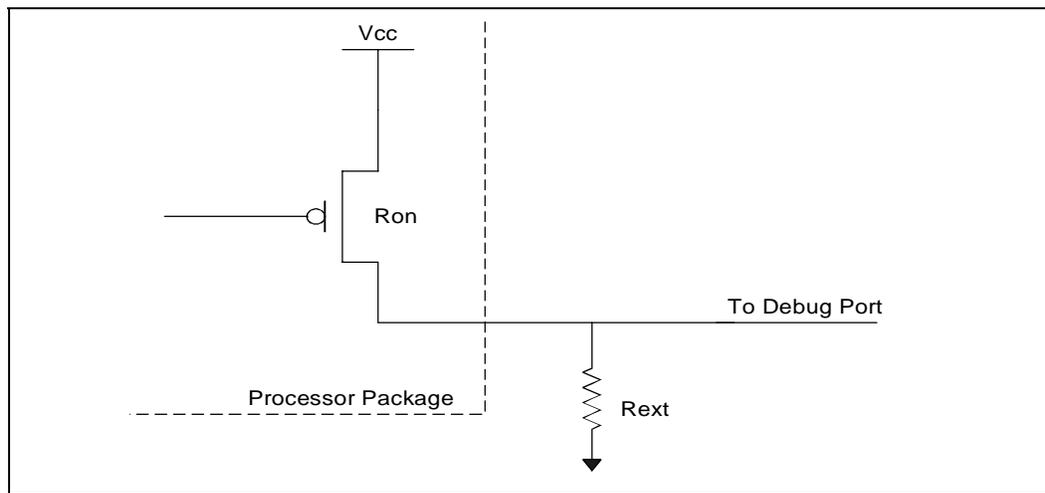
Table 13. ITPCLKOUT[1:0] DC Specifications

Symbol	Parameter	Min	Max	Unit	Notes ¹
R _{on}	Buffer On Resistance	27	46	Ω	2,3

NOTES:

1. Unless otherwise noted, all specifications in this table apply to all processor frequencies.
2. These parameters are not tested and are based on design simulations.
3. See [Figure 4](#) for ITPCLKOUT[1:0] output buffer diagram.

Figure 4. ITPCLKOUT[1:0] Output Buffer Diagram


NOTES:

1. See Table 13 for range of Ron.
2. The Vcc referred to in this figure is the instantaneous Vcc.
3. Refer to the *ITP700 Debug Port Design Guide* and the appropriate platform design guidelines for the value of Rext.

Table 14. BSEL [1:0] and VID[4:0] DC Specifications

Symbol	Parameter	Min	Max	Unit	Notes ¹
Ron (BSEL)	Buffer On Resistance	9.2	14.3	Ω	2
Ron (VID)	Buffer On Resistance	7.8	12.8	Ω	2
I _{HI}	Pin Leakage Hi	N/A	100	μA	3

NOTES:

1. Unless otherwise noted, all specifications in this table apply to all processor frequencies.
2. These parameters are not tested and are based on design simulations.
3. Leakage to Vss with pin held at 2.50 V.

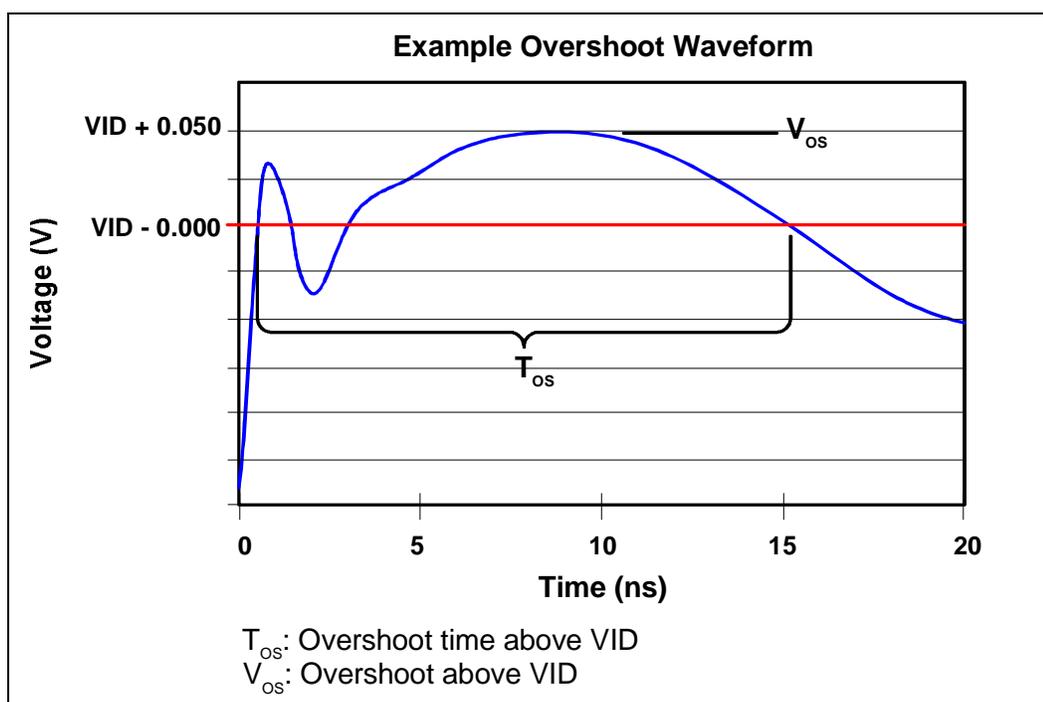
2.12 V_{CC} Overshoot Specification

The mobile Intel Pentium 4 processor can tolerate short transient overshoot events where V_{CC} exceeds the VID voltage when transitioning from a high to low current load condition. This overshoot cannot exceed VID + V_{OS_MAX} (V_{OS_MAX} is the maximum allowable overshoot voltage). The time duration of the overshoot event must not exceed T_{OS_MAX} (T_{OS_MAX} is the maximum allowable time duration above VID). These specifications apply to the processor die voltage as measured across the VCC_SENSE and VSS_SENSE pins.

Table 15. V_{CC} Overshoot Specifications

Symbol	Parameter	Min	Typ	Max	Unit	Figure	Notes
V _{OS_MAX}	Magnitude of V _{CC} overshoot above VID			0.050	V	5	
T _{OS_MAX}	Time duration of V _{CC} overshoot above VID			25	μs	5	

Figure 5. V_{CC} Overshoot Example Waveform



NOTES:

1. V_{os} is measured overshoot voltage.
2. T_{os} is measured time duration above VID.

2.12.1 Die Voltage Validation

Overshoot events from application testing on real processors must meet the specifications in Table 15 when measured across the VCC_SENSE and VSS_SENSE pins. Overshoot events that are < 10 ns in duration may be ignored. These measurements of processor die level overshoot should be taken with a 100-MHz bandwidth limited oscilloscope.

2.13 GTL+ FSB Specifications

Routing topology recommendations may be found in the appropriate platform design guidelines listed in [Table 1](#). Termination resistors are not required for most GTL+ signals, as these are integrated into the processor silicon.

Valid high and low levels are determined by the input buffers which compare a signal's voltage with a reference voltage called GTLREF (known as V_{REF} in previous documentation).

[Table 16](#) lists the GTLREF specifications. The GTL+ reference voltage (GTLREF) should be generated on the system board using high precision voltage divider circuits. It is important that the system board impedance is held to the specified tolerance, and that the intrinsic trace capacitance for the GTL+ signal group traces is known and well-controlled. For more details on platform design see the appropriate platform design guidelines listed in [Table 1](#).

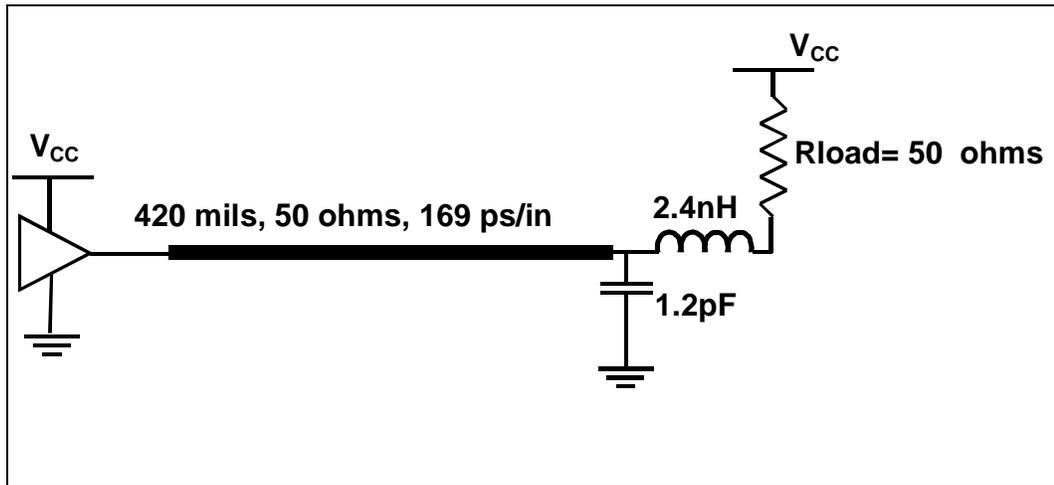
Table 16. GTL+ Bus Voltage Definitions

Symbol	Parameter	Min	Typ	Max	Units	Notes ¹
GTLREF	Bus Reference Voltage	$2/3 V_{CC} - 2\%$	$2/3 V_{CC}$	$2/3 V_{CC} + 2\%$	V	2, 3, 6, 7
GTLREF_COMPATIBLE	Bus Reference Voltage	$0.63 V_{CC} - 2\%$	$0.63 V_{CC}$	$0.63 V_{CC} + 2\%$	V	2, 3, 6, 7
R_{TT}	Termination Resistance	45	50	55	Ω	4, 7
$R_{TT_COMPATIBLE}$	Termination Resistance	54	60	66	Ω	4, 7
COMP[1:0]	COMP Resistance	50.49	51	51.51	Ω	5, 7
COMP[1:0]_COMPATIBLE	COMP Resistance	61.3	61.9	62.5	Ω	5, 7

NOTES:

1. Unless otherwise noted, all specifications in this table apply to all processor frequencies.
2. The tolerances for this specification have been stated generically to enable the system designer to calculate the minimum and maximum values across the range of V_{CC} .
3. GTLREF should be generated from V_{CC} by a voltage divider of 1% tolerance resistors or 1% tolerance matched resistors. Refer to the appropriate platform design guidelines for implementation details.
4. R_{TT} is the on-die termination resistance measured at V_{OL} of the GTL+ output driver. Refer to processor I/O buffer models for I/V characteristics.
5. COMP resistance must be provided on the system board with 1% tolerance resistors. See the appropriate platform design guidelines listed in [Table 1](#) for implementation details.
6. The V_{CC} referred to in these specifications is the instantaneous V_{CC} .
7. For a platform to be forward compatible with future Portable processors it must be designed to support an R_{tt} value of 60 Ω and a GTLREF value of $0.63 \cdot V_{CC}$. A compatible platform is one that is designed for some level of compatibility with future portable processors.

Figure 6. Test Circuit



3 Package Mechanical Specifications

The mobile Intel Pentium 4 processor with 533 MHz FSB is packaged in a 478-pin, FC-PGA2 package. Components of the package include an integrated heat spreader (IHS), processor die, and the substrate which is the pin carrier. Different views of the package are shown in Figure 7 through Figure 12. Package dimensions are shown in Table 17.

Note: For Figure 7 through Figure 12, the following notes apply:

1. Unless otherwise specified, the following drawings are dimensioned in millimeters.
2. Figures and drawings labeled as "Reference Dimensions" are provided for informational purposes only. Reference dimensions are extracted from the mechanical design database and are nominal dimensions with no tolerance information applied. Reference dimensions are NOT checked as part of the processor manufacturing process. Unless noted as such, dimensions in parentheses without tolerances are reference dimensions.
3. Drawings are not to scale.

Note: The drawing below is not to scale and is for reference only. The socket and system board are supplied as a reference only.

Figure 7. Exploded View of Processor Components on a System Board

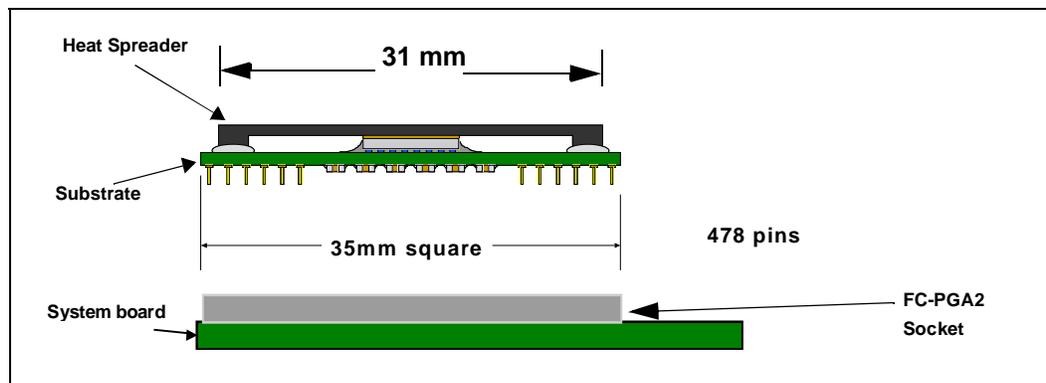


Figure 8. Processor Package

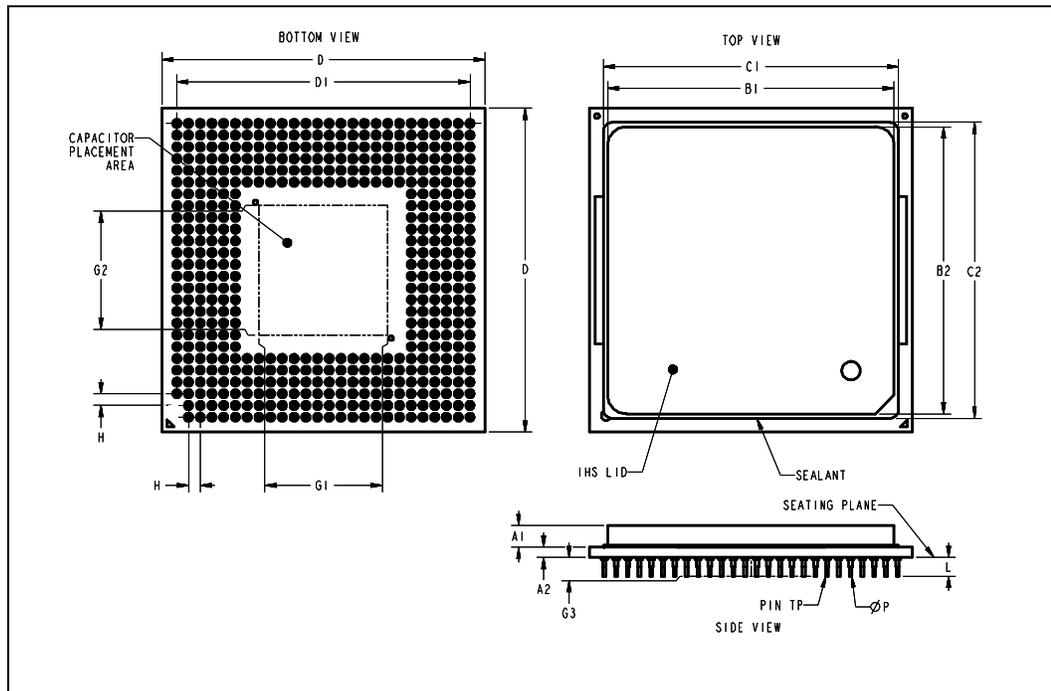


Table 17. Description Table for Processor Dimensions

Code Letter	Dimension (mm)			Notes
	Min	Nominal	Max	
A1	2.266	2.378	2.490	Original Package (6 layer)
A2	0.980	1.080	1.180	Original Package (6 layer)
A1	2.42	2.55	2.67	Equivalent Package (8 layer)
A2	1.13	1.20	1.27	Equivalent Package (8 layer)
B1	30.800	31.000	31.200	
B2	30.800	31.000	31.200	
C1			33.000	Includes Placement Tolerance
C2			33.000	Includes Placement Tolerance
D	34.900	35.000	35.100	
D1	31.500	31.750	32.000	
G1			13.970	Keep-In Zone Dimension
G2			13.970	Keep-In Zone Dimension
G3			1.250	Keep-In Zone Dimension
H		1.270		
L	1.950	2.030	2.110	
φP	0.280	0.305	0.330	
PIN TP			0.254	Diametric True Position (Pin-to-Pin)
IHS Flatness			0.05	

Figure 9. Cross-Section and Keep-in

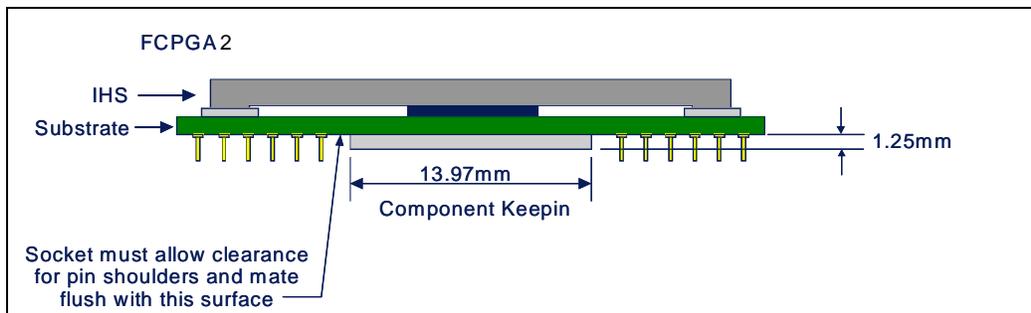
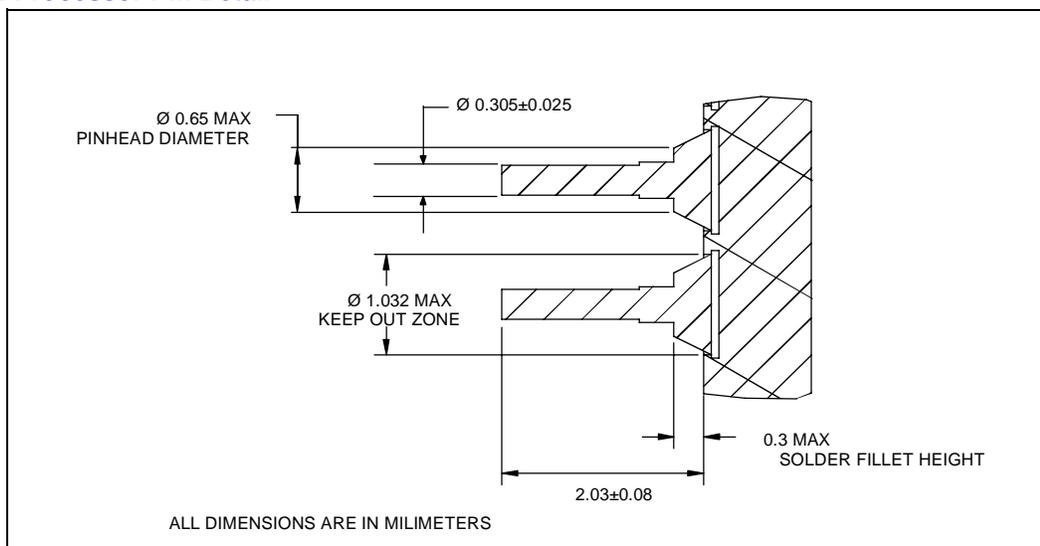


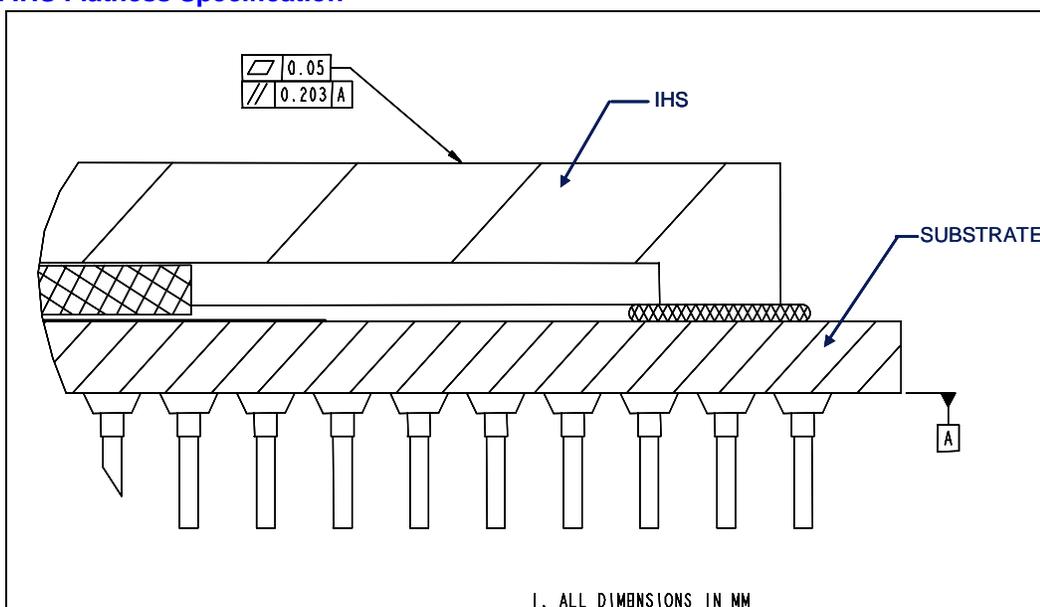
Figure 10. Processor Pin Detail



NOTES:

1. Pin plating consists of 0.2 micrometers Au over 2.0 micrometer Ni.
2. 0.254 mm diametric true position, pin to pin.

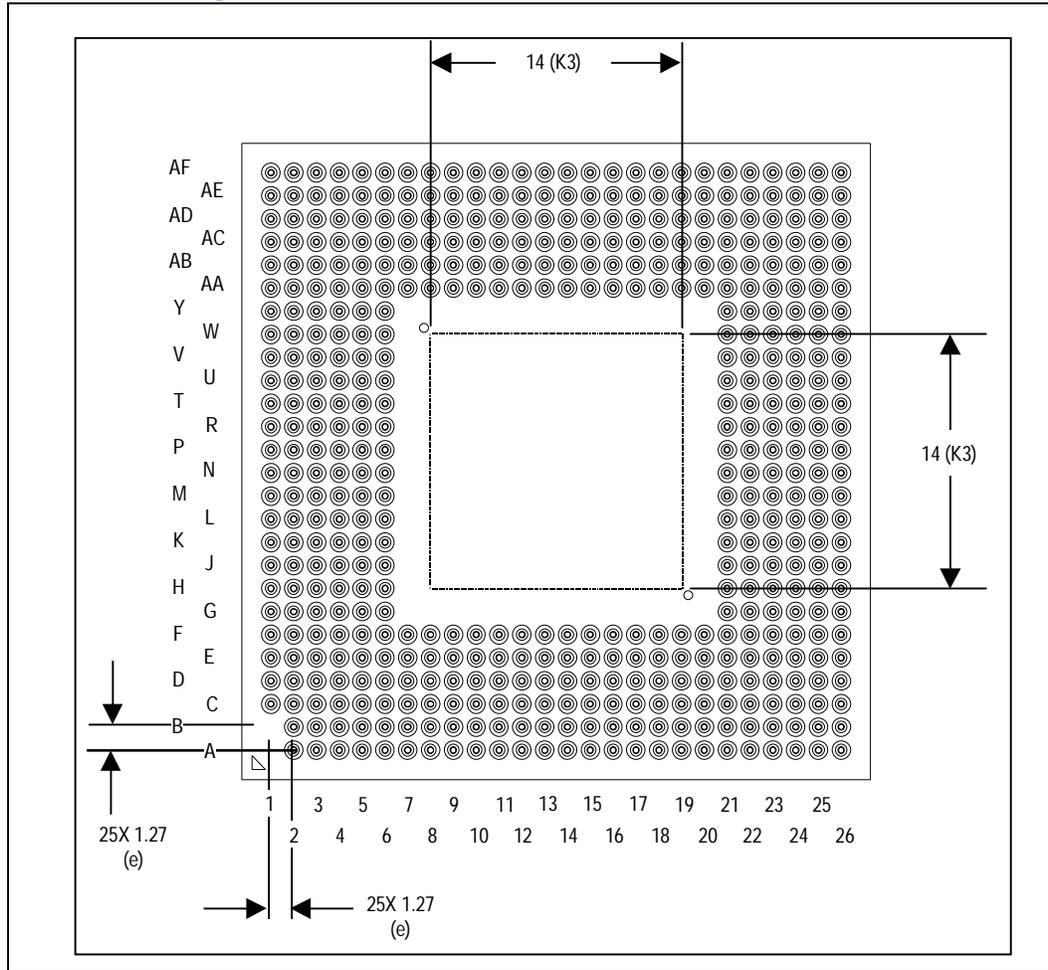
Figure 11. IHS Flatness Specification



NOTES:

1. Flatness is specific as overall, not per unit of length.
2. All dimensions are in millimeters.

Figure 12. FC-PGA2 Package - Bottom View



NOTE: All dimensions in millimeters. Values shown are for reference only.

The mobile Intel Pentium 4 processor with 533 MHz FSB may contain pin side capacitors mounted to the processor package.

3.1 Package Load Specifications

Table 18 provides dynamic and static load specifications for the processor IHS. These mechanical load limits should not be exceeded during heatsink assembly, mechanical stress testing, or standard drop and shipping conditions. The heatsink attach solutions must not induce continuous stress onto the processor with the exception of a uniform load to maintain the heat sink-to-processor thermal interface contact. It is not recommended to use any portion of the processor substrate as a mechanical reference or load bearing surface for thermal solutions.

Table 18. Package Dynamic and Static Load Specifications

Parameter	Max	Unit	Notes
Static	100	lbf	1, 2
Dynamic	200	lbf	1, 3

NOTES:

1. This specification applies to a uniform compressive load.
2. This is the maximum static force that can be applied by the heatsink and clip to maintain the heatsink and processor interface.
3. Dynamic loading specifications are defined assuming a maximum duration of 11 ms and 200 lbf is achieved by superimposing a 100-lbf dynamic load (1 lbf at 50 g) on the static compressive load.

3.2 Processor Insertion Specifications

The mobile Intel Pentium 4 processor with 533 MHz FSB can be inserted and removed 15 times from a mPGA478B socket meeting the Intel Pentium 4 processor 478-Pin (mPGA478B) Socket Design Guidelines document.

3.3 Processor Mass Specifications

Table 19 specifies the processor’s mass. This includes all components which make up the entire processor product.

Table 19. Processor Mass

Processor	Mass (grams)
Intel Pentium 4 processor with 512-kB L2 Cache on 0.13 micron process	19

3.4 Processor Materials

The mobile Intel Pentium 4 processor with 533 MHz FSB is assembled from several components. The basic material properties are described in [Table 22](#).

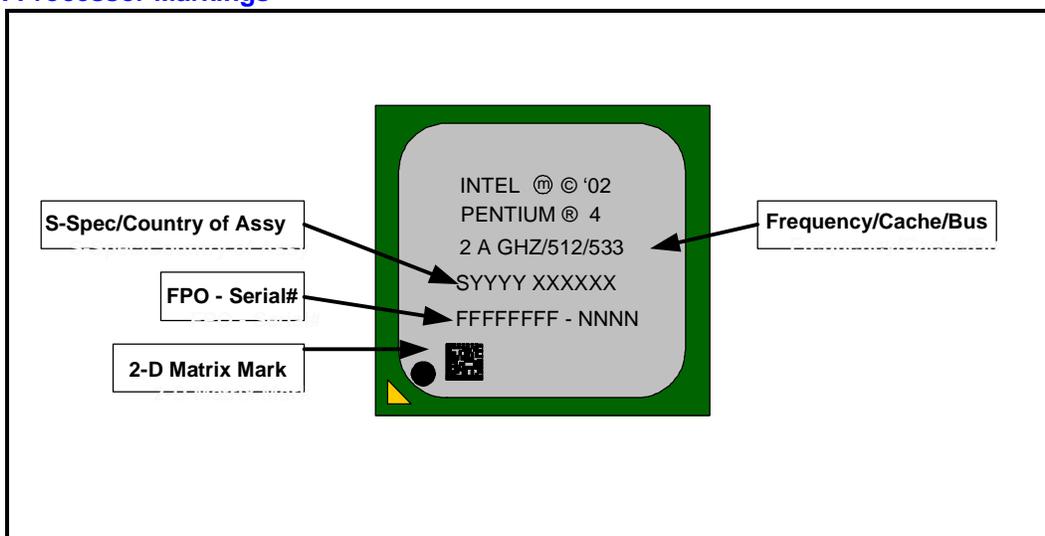
Table 20. Processor Material Properties

Component	Material
Integrated Heat Spreader	Nickel over copper
Substrate	Fiber-reinforced resin
Substrate pins	Gold over nickel

3.5 Processor Markings

The following section details the processor top-side markings and is provided to aid in the identification of the mobile Intel Pentium 4 processor with 533 MHz FSB.

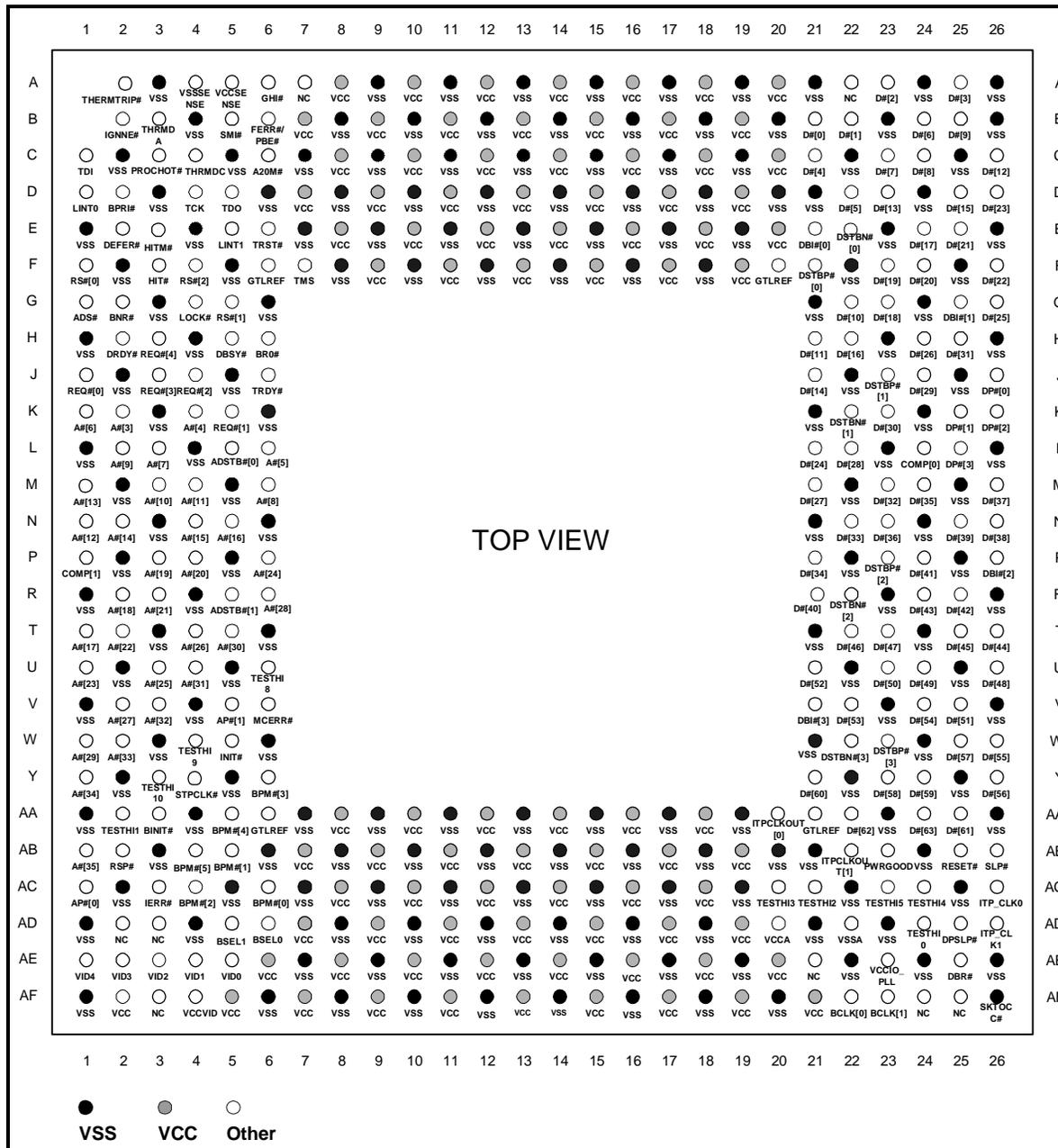
Figure 13. Processor Markings



3.6 Processor Pin-Out

Figure 14 shows the top view pinout of the mobile Intel Pentium 4 processor with 533 MHz FSB.

Figure 14. The Coordinates of the Processor Pins as Viewed From the Top of the Package.



4 Pin Listing and Signal Definitions

4.1 Mobile Intel Pentium 4 Processor Pin Assignments

Section 4.1 contains the preliminary pin list for the mobile Intel Pentium 4 processor with 533 MHz FSB in [Table 21](#) and [Table 22](#). [Table 21](#) is a listing of all processor pins ordered alphabetically by pin name. [Table 22](#) is also a listing of all processor pins but ordered by pin number.

Table 21. Pin Listing by Pin Name

Pin Name	Pin Number	Signal Buffer Type	Direction
A#[03]	K2	Source Synch	Input/Output
A#[04]	K4	Source Synch	Input/Output
A#[05]	L6	Source Synch	Input/Output
A#[06]	K1	Source Synch	Input/Output
A#[07]	L3	Source Synch	Input/Output
A#[08]	M6	Source Synch	Input/Output
A#[09]	L2	Source Synch	Input/Output
A#[10]	M3	Source Synch	Input/Output
A#[11]	M4	Source Synch	Input/Output
A#[12]	N1	Source Synch	Input/Output
A#[13]	M1	Source Synch	Input/Output
A#[14]	N2	Source Synch	Input/Output
A#[15]	N4	Source Synch	Input/Output
A#[16]	N5	Source Synch	Input/Output
A#[17]	T1	Source Synch	Input/Output
A#[18]	R2	Source Synch	Input/Output
A#[19]	P3	Source Synch	Input/Output
A#[20]	P4	Source Synch	Input/Output
A#[21]	R3	Source Synch	Input/Output
A#[22]	T2	Source Synch	Input/Output
A#[23]	U1	Source Synch	Input/Output
A#[24]	P6	Source Synch	Input/Output
A#[25]	U3	Source Synch	Input/Output
A#[26]	T4	Source Synch	Input/Output
A#[27]	V2	Source Synch	Input/Output
A#[28]	R6	Source Synch	Input/Output
A#[29]	W1	Source Synch	Input/Output
A#[30]	T5	Source Synch	Input/Output
A#[31]	U4	Source Synch	Input/Output
A#[32]	V3	Source Synch	Input/Output
A#[33]	W2	Source Synch	Input/Output
A#[34]	Y1	Source Synch	Input/Output
A#[35]	AB1	Source Synch	Input/Output
A20M#	C6	Asynch GTL+	Input
ADS#	G1	Common Clock	Input/Output
ADSTB#[0]	L5	Source Synch	Input/Output
ADSTB#[1]	R5	Source Synch	Input/Output

Table 21. Pin Listing by Pin Name

Pin Name	Pin Number	Signal Buffer Type	Direction
AP#[0]	AC1	Common Clock	Input/Output
AP#[1]	V5	Common Clock	Input/Output
BCLK[0]	AF22	Bus Clock	Input
BCLK[1]	AF23	Bus Clock	Input
BINIT#	AA3	Common Clock	Input/Output
BNR#	G2	Common Clock	Input/Output
BPM#[0]	AC6	Common Clock	Input/Output
BPM#[1]	AB5	Common Clock	Input/Output
BPM#[2]	AC4	Common Clock	Input/Output
BPM#[3]	Y6	Common Clock	Input/Output
BPM#[4]	AA5	Common Clock	Input/Output
BPM#[5]	AB4	Common Clock	Input/Output
BPRI#	D2	Common Clock	Input
BR0#	H6	Common Clock	Input/Output
BSEL0	AD6	Power/Other	Output
BSEL1	AD5	Power/Other	Output
COMP[0]	L24	Power/Other	Input/Output
COMP[1]	P1	Power/Other	Input/Output
D#[0]	B21	Source Synch	Input/Output
D#[01]	B22	Source Synch	Input/Output
D#[02]	A23	Source Synch	Input/Output
D#[03]	A25	Source Synch	Input/Output
D#[04]	C21	Source Synch	Input/Output
D#[05]	D22	Source Synch	Input/Output
D#[06]	B24	Source Synch	Input/Output
D#[07]	C23	Source Synch	Input/Output
D#[08]	C24	Source Synch	Input/Output
D#[09]	B25	Source Synch	Input/Output
D#[10]	G22	Source Synch	Input/Output
D#[11]	H21	Source Synch	Input/Output
D#[12]	C26	Source Synch	Input/Output
D#[13]	D23	Source Synch	Input/Output
D#[14]	J21	Source Synch	Input/Output
D#[15]	D25	Source Synch	Input/Output
D#[16]	H22	Source Synch	Input/Output
D#[17]	E24	Source Synch	Input/Output
D#[18]	G23	Source Synch	Input/Output
D#[19]	F23	Source Synch	Input/Output
D#[20]	F24	Source Synch	Input/Output

Table 21. Pin Listing by Pin Name

Pin Name	Pin Number	Signal Buffer Type	Direction
D#[21]	E25	Source Synch	Input/Output
D#[22]	F26	Source Synch	Input/Output
D#[23]	D26	Source Synch	Input/Output
D#[24]	L21	Source Synch	Input/Output
D#[25]	G26	Source Synch	Input/Output
D#[26]	H24	Source Synch	Input/Output
D#[27]	M21	Source Synch	Input/Output
D#[28]	L22	Source Synch	Input/Output
D#[29]	J24	Source Synch	Input/Output
D#[30]	K23	Source Synch	Input/Output
D#[31]	H25	Source Synch	Input/Output
D#[32]	M23	Source Synch	Input/Output
D#[33]	N22	Source Synch	Input/Output
D#[34]	P21	Source Synch	Input/Output
D#[35]	M24	Source Synch	Input/Output
D#[36]	N23	Source Synch	Input/Output
D#[37]	M26	Source Synch	Input/Output
D#[38]	N26	Source Synch	Input/Output
D#[39]	N25	Source Synch	Input/Output
D#[40]	R21	Source Synch	Input/Output
D#[41]	P24	Source Synch	Input/Output
D#[42]	R25	Source Synch	Input/Output
D#[43]	R24	Source Synch	Input/Output
D#[44]	T26	Source Synch	Input/Output
D#[45]	T25	Source Synch	Input/Output
D#[46]	T22	Source Synch	Input/Output
D#[47]	T23	Source Synch	Input/Output
D#[48]	U26	Source Synch	Input/Output
D#[49]	U24	Source Synch	Input/Output
D#[50]	U23	Source Synch	Input/Output
D#[51]	V25	Source Synch	Input/Output
D#[52]	U21	Source Synch	Input/Output
D#[53]	V22	Source Synch	Input/Output
D#[54]	V24	Source Synch	Input/Output
D#[55]	W26	Source Synch	Input/Output
D#[56]	Y26	Source Synch	Input/Output
D#[57]	W25	Source Synch	Input/Output
D#[58]	Y23	Source Synch	Input/Output
D#[59]	Y24	Source Synch	Input/Output

Table 21. Pin Listing by Pin Name

Pin Name	Pin Number	Signal Buffer Type	Direction
D#[60]	Y21	Source Synch	Input/Output
D#[61]	AA25	Source Synch	Input/Output
D#[62]	AA22	Source Synch	Input/Output
D#[63]	AA24	Source Synch	Input/Output
DBI#[0]	E21	Source Synch	Input/Output
DBI#[1]	G25	Source Synch	Input/Output
DBI#[2]	P26	Source Synch	Input/Output
DBI#[3]	V21	Source Synch	Input/Output
DBR#	AE25	Power/Other	Output
DBSY#	H5	Common Clock	Input/Output
DEFER#	E2	Common Clock	Input
DP#[0]	J26	Common Clock	Input/Output
DP#[1]	K25	Common Clock	Input/Output
DP#[2]	K26	Common Clock	Input/Output
DP#[3]	L25	Common Clock	Input/Output
DPSLP#	AD25	Asynch GTL+	Input
DRDY#	H2	Common Clock	Input/Output
DSTBN#[0]	E22	Source Synch	Input/Output
DSTBN#[1]	K22	Source Synch	Input/Output
DSTBN#[2]	R22	Source Synch	Input/Output
DSTBN#[3]	W22	Source Synch	Input/Output
DSTBP#[0]	F21	Source Synch	Input/Output
DSTBP#[1]	J23	Source Synch	Input/Output
DSTBP#[2]	P23	Source Synch	Input/Output
DSTBP#[3]	W23	Source Synch	Input/Output
FERR#/PBE#	B6	Asynch AGL+	Output
GHI#	A6	Asynch GTL+	Input
GTLREF	AA21	Power/Other	Input
GTLREF	AA6	Power/Other	Input
GTLREF	F20	Power/Other	Input
GTLREF	F6	Power/Other	Input
HIT#	F3	Common Clock	Input/Output
HITM#	E3	Common Clock	Input/Output
IERR#	AC3	Common Clock	Output
IGNNE#	B2	Asynch GTL+	Input
IMPSEL	AE26	Power/Other	Input
INIT#	W5	Asynch GTL+	Input
ITPCLKOUT[0]	AA20	Power/Other	Output
ITPCLKOUT[1]	AB22	Power/Other	Output

Table 21. Pin Listing by Pin Name

Pin Name	Pin Number	Signal Buffer Type	Direction
ITP_CLK0	AC26	TAP	input
ITP_CLK1	AD26	TAP	input
LINT0	D1	Asynch GTL+	Input
LINT1	E5	Asynch GTL+	Input
LOCK#	G4	Common Clock	Input/Output
MCERR#	V6	Common Clock	Input/Output
NC	A22		
NC	A7		
NC	AD2		
NC	AD3		
NC	AE21		
NC	AF3		
NC	AF24		
NC	AF25		
PROCHOT#	C3	Asynch GTL+	Input/Output
PWRGOOD	AB23	Power/Other	Input
REQ#[0]	J1	Source Synch	Input/Output
REQ#[1]	K5	Source Synch	Input/Output
REQ#[2]	J4	Source Synch	Input/Output
REQ#[3]	J3	Source Synch	Input/Output
REQ#[4]	H3	Source Synch	Input/Output
RESET#	AB25	Common Clock	Input
RS#[0]	F1	Common Clock	Input
RS#[1]	G5	Common Clock	Input
RS#[2]	F4	Common Clock	Input
RSP#	AB2	Common Clock	Input
SKTOCC#	AF26	Power/Other	Output
SLP#	AB26	Asynch GTL+	Input
SM#	B5	Asynch GTL+	Input
STPCLK#	Y4	Asynch GTL+	Input
TCK	D4	TAP	Input
TDI	C1	TAP	Input
TDO	D5	TAP	Output
TESTHI0	AD24	Power/Other	Input
TESTHI1	AA2	Power/Other	Input
TESTHI2	AC21	Power/Other	Input
TESTHI3	AC20	Power/Other	Input
TESTHI4	AC24	Power/Other	Input
TESTHI5	AC23	Power/Other	Input

Table 21. Pin Listing by Pin Name

Pin Name	Pin Number	Signal Buffer Type	Direction
TESTHI8	U6	Power/Other	Input
TESTHI9	W4	Power/Other	Input
TESTHI10	Y3	Power/Other	Input
THERMDA	B3	Power/Other	
THERMDC	C4	Power/Other	
THERMTRIP#	A2	Asynch GTL+	Output
TMS	F7	TAP	Input
TRDY#	J6	Common Clock	Input
TRST#	E6	TAP	Input
VCC	A10	Power/Other	
VCC	A12	Power/Other	
VCC	A14	Power/Other	
VCC	A16	Power/Other	
VCC	A18	Power/Other	
VCC	A20	Power/Other	
VCC	A8	Power/Other	
VCC	AA10	Power/Other	
VCC	AA12	Power/Other	
VCC	AA14	Power/Other	
VCC	AA16	Power/Other	
VCC	AA18	Power/Other	
VCC	AA8	Power/Other	
VCC	AB11	Power/Other	
VCC	AB13	Power/Other	
VCC	AB15	Power/Other	
VCC	AB17	Power/Other	
VCC	AB19	Power/Other	
VCC	AB7	Power/Other	
VCC	AB9	Power/Other	
VCC	AC10	Power/Other	
VCC	AC12	Power/Other	
VCC	AC14	Power/Other	
VCC	AC16	Power/Other	
VCC	AC18	Power/Other	
VCC	AC8	Power/Other	
VCC	AD11	Power/Other	
VCC	AD13	Power/Other	
VCC	AD15	Power/Other	
VCC	AD17	Power/Other	

Table 21. Pin Listing by Pin Name

Pin Name	Pin Number	Signal Buffer Type	Direction
VCC	AD19	Power/Other	
VCC	AD7	Power/Other	
VCC	AD9	Power/Other	
VCC	AE10	Power/Other	
VCC	AE12	Power/Other	
VCC	AE14	Power/Other	
VCC	AE16	Power/Other	
VCC	AE18	Power/Other	
VCC	AE20	Power/Other	
VCC	AE6	Power/Other	
VCC	AE8	Power/Other	
VCC	AF11	Power/Other	
VCC	AF13	Power/Other	
VCC	AF15	Power/Other	
VCC	AF17	Power/Other	
VCC	AF19	Power/Other	
VCC	AF2	Power/Other	
VCC	AF21	Power/Other	
VCC	AF5	Power/Other	
VCC	AF7	Power/Other	
VCC	AF9	Power/Other	
VCC	B11	Power/Other	
VCC	B13	Power/Other	
VCC	B15	Power/Other	
VCC	B17	Power/Other	
VCC	B19	Power/Other	
VCC	B7	Power/Other	
VCC	B9	Power/Other	
VCC	C10	Power/Other	
VCC	C12	Power/Other	
VCC	C14	Power/Other	
VCC	C16	Power/Other	
VCC	C18	Power/Other	
VCC	C20	Power/Other	
VCC	C8	Power/Other	
VCC	D11	Power/Other	
VCC	D13	Power/Other	
VCC	D15	Power/Other	
VCC	D17	Power/Other	

Table 21. Pin Listing by Pin Name

Pin Name	Pin Number	Signal Buffer Type	Direction
VCC	D19	Power/Other	
VCC	D7	Power/Other	
VCC	D9	Power/Other	
VCC	E10	Power/Other	
VCC	E12	Power/Other	
VCC	E14	Power/Other	
VCC	E16	Power/Other	
VCC	E18	Power/Other	
VCC	E20	Power/Other	
VCC	E8	Power/Other	
VCC	F11	Power/Other	
VCC	F13	Power/Other	
VCC	F15	Power/Other	
VCC	F17	Power/Other	
VCC	F19	Power/Other	
VCC	F9	Power/Other	
VCCA	AD20	Power/Other	
VCCIOPLL	AE23	Power/Other	
VCCSENSE	A5	Power/Other	Output
VCCVID	AF4	Power/Other	Input
VID0	AE5	Power/Other	Output
VID1	AE4	Power/Other	Output
VID2	AE3	Power/Other	Output
VID3	AE2	Power/Other	Output
VID4	AE1	Power/Other	Output
VSS	A11	Power/Other	
VSS	A13	Power/Other	
VSS	A15	Power/Other	
VSS	A17	Power/Other	
VSS	A19	Power/Other	
VSS	A21	Power/Other	
VSS	A24	Power/Other	
VSS	A26	Power/Other	
VSS	A3	Power/Other	
VSS	A9	Power/Other	
VSS	AA1	Power/Other	
VSS	AA11	Power/Other	
VSS	AA13	Power/Other	
VSS	AA15	Power/Other	

Table 21. Pin Listing by Pin Name

Pin Name	Pin Number	Signal Buffer Type	Direction
VSS	AA17	Power/Other	
VSS	AA19	Power/Other	
VSS	AA23	Power/Other	
VSS	AA26	Power/Other	
VSS	AA4	Power/Other	
VSS	AA7	Power/Other	
VSS	AA9	Power/Other	
VSS	AB10	Power/Other	
VSS	AB12	Power/Other	
VSS	AB14	Power/Other	
VSS	AB16	Power/Other	
VSS	AB18	Power/Other	
VSS	AB20	Power/Other	
VSS	AB21	Power/Other	
VSS	AB24	Power/Other	
VSS	AB3	Power/Other	
VSS	AB6	Power/Other	
VSS	AB8	Power/Other	
VSS	AC11	Power/Other	
VSS	AC13	Power/Other	
VSS	AC15	Power/Other	
VSS	AC17	Power/Other	
VSS	AC19	Power/Other	
VSS	AC2	Power/Other	
VSS	AC22	Power/Other	
VSS	AC25	Power/Other	
VSS	AC5	Power/Other	
VSS	AC7	Power/Other	
VSS	AC9	Power/Other	
VSS	AD1	Power/Other	
VSS	AD10	Power/Other	
VSS	AD12	Power/Other	
VSS	AD14	Power/Other	
VSS	AD16	Power/Other	
VSS	AD18	Power/Other	
VSS	AD21	Power/Other	
VSS	AD23	Power/Other	
VSS	AD4	Power/Other	
VSS	AD8	Power/Other	

Table 21. Pin Listing by Pin Name

Pin Name	Pin Number	Signal Buffer Type	Direction
VSS	AE11	Power/Other	
VSS	AE13	Power/Other	
VSS	AE15	Power/Other	
VSS	AE17	Power/Other	
VSS	AE19	Power/Other	
VSS	AE22	Power/Other	
VSS	AE24	Power/Other	
VSS	AE7	Power/Other	
VSS	AE9	Power/Other	
VSS	AF1	Power/Other	
VSS	AF10	Power/Other	
VSS	AF12	Power/Other	
VSS	AF14	Power/Other	
VSS	AF16	Power/Other	
VSS	AF18	Power/Other	
VSS	AF20	Power/Other	
VSS	AF6	Power/Other	
VSS	AF8	Power/Other	
VSS	B10	Power/Other	
VSS	B12	Power/Other	
VSS	B14	Power/Other	
VSS	B16	Power/Other	
VSS	B18	Power/Other	
VSS	B20	Power/Other	
VSS	B23	Power/Other	
VSS	B26	Power/Other	
VSS	B4	Power/Other	
VSS	B8	Power/Other	
VSS	C11	Power/Other	
VSS	C13	Power/Other	
VSS	C15	Power/Other	
VSS	C17	Power/Other	
VSS	C19	Power/Other	
VSS	C2	Power/Other	
VSS	C22	Power/Other	
VSS	C25	Power/Other	
VSS	C5	Power/Other	
VSS	C7	Power/Other	
VSS	C9	Power/Other	

Table 21. Pin Listing by Pin Name

Pin Name	Pin Number	Signal Buffer Type	Direction
VSS	D10	Power/Other	
VSS	D12	Power/Other	
VSS	D14	Power/Other	
VSS	D16	Power/Other	
VSS	D18	Power/Other	
VSS	D20	Power/Other	
VSS	D21	Power/Other	
VSS	D24	Power/Other	
VSS	D3	Power/Other	
VSS	D6	Power/Other	
VSS	D8	Power/Other	
VSS	E1	Power/Other	
VSS	E11	Power/Other	
VSS	E13	Power/Other	
VSS	E15	Power/Other	
VSS	E17	Power/Other	
VSS	E19	Power/Other	
VSS	E23	Power/Other	
VSS	E26	Power/Other	
VSS	E4	Power/Other	
VSS	E7	Power/Other	
VSS	E9	Power/Other	
VSS	F10	Power/Other	
VSS	F12	Power/Other	
VSS	F14	Power/Other	
VSS	F16	Power/Other	
VSS	F18	Power/Other	
VSS	F2	Power/Other	
VSS	F22	Power/Other	
VSS	F25	Power/Other	
VSS	F5	Power/Other	
VSS	F8	Power/Other	
VSS	G21	Power/Other	
VSS	G24	Power/Other	
VSS	G3	Power/Other	
VSS	G6	Power/Other	
VSS	H1	Power/Other	
VSS	H23	Power/Other	
VSS	H26	Power/Other	

Table 21. Pin Listing by Pin Name

Pin Name	Pin Number	Signal Buffer Type	Direction
VSS	H4	Power/Other	
VSS	J2	Power/Other	
VSS	J22	Power/Other	
VSS	J25	Power/Other	
VSS	J5	Power/Other	
VSS	K21	Power/Other	
VSS	K24	Power/Other	
VSS	K3	Power/Other	
VSS	K6	Power/Other	
VSS	L1	Power/Other	
VSS	L23	Power/Other	
VSS	L26	Power/Other	
VSS	L4	Power/Other	
VSS	M2	Power/Other	
VSS	M22	Power/Other	
VSS	M25	Power/Other	
VSS	M5	Power/Other	
VSS	N21	Power/Other	
VSS	N24	Power/Other	
VSS	N3	Power/Other	
VSS	N6	Power/Other	
VSS	P2	Power/Other	
VSS	P22	Power/Other	
VSS	P25	Power/Other	
VSS	P5	Power/Other	
VSS	R1	Power/Other	
VSS	R23	Power/Other	
VSS	R26	Power/Other	
VSS	R4	Power/Other	
VSS	T21	Power/Other	
VSS	T24	Power/Other	
VSS	T3	Power/Other	
VSS	T6	Power/Other	
VSS	U2	Power/Other	
VSS	U22	Power/Other	
VSS	U25	Power/Other	
VSS	U5	Power/Other	
VSS	V1	Power/Other	
VSS	V23	Power/Other	

Table 21. Pin Listing by Pin Name

Pin Name	Pin Number	Signal Buffer Type	Direction
VSS	V26	Power/Other	
VSS	V4	Power/Other	
VSS	W21	Power/Other	
VSS	W24	Power/Other	
VSS	W3	Power/Other	
VSS	W6	Power/Other	
VSS	Y2	Power/Other	
VSS	Y22	Power/Other	
VSS	Y25	Power/Other	
VSS	Y5	Power/Other	
VSSA	AD22	Power/Other	
VSSSENSE	A4	Power/Other	Output

Table 22. Pin Listing by Pin Number

Pin Number	Pin Name	Signal Buffer Type	Direction
A25	D#[03]	Source Synch	Input/Output
A26	VSS	Power/Other	
AA1	VSS	Power/Other	
AA2	TESTH1	Power/Other	Input
AA3	BINIT#	Common Clock	Input/Output
AA4	VSS	Power/Other	
AA5	BPM#[4]	Common Clock	Input/Output
AA6	GTLREF	Power/Other	Input
AA7	VSS	Power/Other	
AA8	VCC	Power/Other	
AA9	VSS	Power/Other	
AA10	VCC	Power/Other	
AA11	VSS	Power/Other	
AA12	VCC	Power/Other	
AA13	VSS	Power/Other	
AA14	VCC	Power/Other	
AA15	VSS	Power/Other	
AA16	VCC	Power/Other	
AA17	VSS	Power/Other	
AA18	VCC	Power/Other	
AA19	VSS	Power/Other	
AA20	ITPCLKOUT [0]	Power/Other	Output
AA21	GTLREF	Power/Other	Input
AA22	D#[62]	Source Synch	Input/Output
AA23	VSS	Power/Other	
AA24	D#[63]	Source Synch	Input/Output
AA25	D#[61]	Source Synch	Input/Output
AA26	VSS	Power/Other	
AB1	A#[35]	Source Synch	Input/Output
AB2	RSP#	Common Clock	Input
AB3	VSS	Power/Other	
AB4	BPM#[5]	Common Clock	Input/Output
AB5	BPM#[1]	Common Clock	Input/Output
AB6	VSS	Power/Other	
AB7	VCC	Power/Other	
AB8	VSS	Power/Other	
AB9	VCC	Power/Other	
AB10	VSS	Power/Other	

Table 22. Pin Listing by Pin Number

Pin Number	Pin Name	Signal Buffer Type	Direction
A2	THERMTRIP#	Asynch GTL+	Output
A3	VSS	Power/Other	
A4	VSSSENSE	Power/Other	Output
A5	VCCSENSE	Power/Other	Output
A6	GHI#	Asynch GTL+	Input
A7	NC		
A8	VCC	Power/Other	
A9	VSS	Power/Other	
A10	VCC	Power/Other	
A11	VSS	Power/Other	
A12	VCC	Power/Other	
A13	VSS	Power/Other	
A14	VCC	Power/Other	
A15	VSS	Power/Other	
A16	VCC	Power/Other	
A17	VSS	Power/Other	
A18	VCC	Power/Other	
A19	VSS	Power/Other	
A20	VCC	Power/Other	
A21	VSS	Power/Other	
A22	NC		
A23	D#[02]	Source Synch	Input/Output
A24	VSS	Power/Other	

Table 22. Pin Listing by Pin Number

Pin Number	Pin Name	Signal Buffer Type	Direction
AB11	VCC	Power/Other	
AB12	VSS	Power/Other	
AB13	VCC	Power/Other	
AB14	VSS	Power/Other	
AB15	VCC	Power/Other	
AB16	VSS	Power/Other	
AB17	VCC	Power/Other	
AB18	VSS	Power/Other	
AB19	VCC	Power/Other	
AB20	VSS	Power/Other	
AB21	VSS	Power/Other	
AB22	ITPCLKOUT [1]	Power/Other	Output
AB23	PWRGOOD	Power/Other	Input
AB24	VSS	Power/Other	
AB25	RESET#	Common Clock	Input
AB26	SLP#	Asynch GTL+	Input
AC1	AP#[0]	Common Clock	Input/Output
AC2	VSS	Power/Other	
AC3	IERR#	Common Clock	Output
AC4	BPM#[2]	Common Clock	Input/Output
AC5	VSS	Power/Other	
AC6	BPM#[0]	Common Clock	Input/Output
AC7	VSS	Power/Other	
AC8	VCC	Power/Other	
AC9	VSS	Power/Other	
AC10	VCC	Power/Other	
AC11	VSS	Power/Other	
AC12	VCC	Power/Other	
AC13	VSS	Power/Other	
AC14	VCC	Power/Other	
AC15	VSS	Power/Other	
AC16	VCC	Power/Other	
AC17	VSS	Power/Other	
AC18	VCC	Power/Other	
AC19	VSS	Power/Other	
AC20	TESTHI3	Power/Other	Input
AC21	TESTHI2	Power/Other	Input
AC22	VSS	Power/Other	

Table 22. Pin Listing by Pin Number

Pin Number	Pin Name	Signal Buffer Type	Direction
AC23	TESTHI5	Power/Other	Input
AC24	TESTHI4	Power/Other	Input
AC25	VSS	Power/Other	
AC26	ITP_CLK0	TAP	input
AD1	VSS	Power/Other	
AD2	NC		
AD3	NC		
AD4	VSS	Power/Other	
AD5	BSEL1	Power/Other	Output
AD6	BSEL0	Power/Other	Output
AD7	VCC	Power/Other	
AD8	VSS	Power/Other	
AD9	VCC	Power/Other	
AD10	VSS	Power/Other	
AD11	VCC	Power/Other	
AD12	VSS	Power/Other	
AD13	VCC	Power/Other	
AD14	VSS	Power/Other	
AD15	VCC	Power/Other	
AD16	VSS	Power/Other	
AD17	VCC	Power/Other	
AD18	VSS	Power/Other	
AD19	VCC	Power/Other	
AD20	VCCA	Power/Other	
AD21	VSS	Power/Other	
AD22	VSSA	Power/Other	
AD23	VSS	Power/Other	
AD24	TESTHI0	Power/Other	Input
AD25	DPSLP#	Asynch GTL+	Input
AD26	ITP_CLK1	TAP	input
AE1	VID4	Power/Other	Output
AE2	VID3	Power/Other	Output
AE3	VID2	Power/Other	Output
AE4	VID1	Power/Other	Output
AE5	VID0	Power/Other	Output
AE6	VCC	Power/Other	
AE7	VSS	Power/Other	
AE8	VCC	Power/Other	
AE9	VSS	Power/Other	

Table 22. Pin Listing by Pin Number

Pin Number	Pin Name	Signal Buffer Type	Direction
AE10	VCC	Power/Other	
AE11	VSS	Power/Other	
AE12	VCC	Power/Other	
AE13	VSS	Power/Other	
AE14	VCC	Power/Other	
AE15	VSS	Power/Other	
AE16	VCC	Power/Other	
AE17	VSS	Power/Other	
AE18	VCC	Power/Other	
AE19	VSS	Power/Other	
AE20	VCC	Power/Other	
AE21	NC		
AE22	VSS	Power/Other	
AE23	VCCIOPLL	Power/Other	
AE24	VSS	Power/Other	
AE25	DBR#	Asynch GTL+	Output
AE26	IMPSEL	Power/Other	Input
AF1	VSS	Power/Other	
AF2	VCC	Power/Other	
AF3	NC		
AF4	VCCVID	Power/Other	Input
AF5	VCC	Power/Other	
AF6	VSS	Power/Other	
AF7	VCC	Power/Other	
AF8	VSS	Power/Other	
AF9	VCC	Power/Other	
AF10	VSS	Power/Other	
AF11	VCC	Power/Other	
AF12	VSS	Power/Other	
AF13	VCC	Power/Other	
AF14	VSS	Power/Other	
AF15	VCC	Power/Other	
AF16	VSS	Power/Other	
AF17	VCC	Power/Other	
AF18	VSS	Power/Other	
AF19	VCC	Power/Other	
AF20	VSS	Power/Other	
AF21	VCC	Power/Other	
AF22	BCLK[0]	Bus Clock	Input

Table 22. Pin Listing by Pin Number

Pin Number	Pin Name	Signal Buffer Type	Direction
AF23	BCLK[1]	Bus Clock	Input
AF24	NC		
AF25	NC		
AF26	SKTOCC#	Power/Other	Output
B2	IGNNE#	Asynch GTL+	Input
B3	THERMDA	Power/Other	
B4	VSS	Power/Other	
B5	SMI#	Asynch GTL+	Input
B6	FERR#/PBE#	Asynch AGL+	Output
B7	VCC	Power/Other	
B8	VSS	Power/Other	
B9	VCC	Power/Other	
B10	VSS	Power/Other	
B11	VCC	Power/Other	
B12	VSS	Power/Other	
B13	VCC	Power/Other	
B14	VSS	Power/Other	
B15	VCC	Power/Other	
B16	VSS	Power/Other	
B17	VCC	Power/Other	
B18	VSS	Power/Other	
B19	VCC	Power/Other	
B20	VSS	Power/Other	
B21	D#[0]	Source Synch	Input/Output
B22	D#[01]	Source Synch	Input/Output
B23	VSS	Power/Other	
B24	D#[06]	Source Synch	Input/Output
B25	D#[09]	Source Synch	Input/Output
B26	VSS	Power/Other	
C1	TDI	TAP	Input
C2	VSS	Power/Other	
C3	PROCHOT#	Asynch GTL+	Input/Output
C4	THERMDC	Power/Other	
C5	VSS	Power/Other	
C6	A20M#	Asynch GTL+	Input
C7	VSS	Power/Other	
C8	VCC	Power/Other	
C9	VSS	Power/Other	
C10	VCC	Power/Other	

Table 22. Pin Listing by Pin Number

Pin Number	Pin Name	Signal Buffer Type	Direction
C11	VSS	Power/Other	
C12	VCC	Power/Other	
C13	VSS	Power/Other	
C14	VCC	Power/Other	
C15	VSS	Power/Other	
C16	VCC	Power/Other	
C17	VSS	Power/Other	
C18	VCC	Power/Other	
C19	VSS	Power/Other	
C20	VCC	Power/Other	
C21	D#[04]	Source Synch	Input/Output
C22	VSS	Power/Other	
C23	D#[07]	Source Synch	Input/Output
C24	D#[08]	Source Synch	Input/Output
C25	VSS	Power/Other	
C26	D#[12]	Source Synch	Input/Output
D1	LINT0	Asynch GTL+	Input
D2	BPRI#	Common Clock	Input
D3	VSS	Power/Other	
D4	TCK	TAP	Input
D5	TDO	TAP	Output
D6	VSS	Power/Other	
D7	VCC	Power/Other	
D8	VSS	Power/Other	
D9	VCC	Power/Other	
D10	VSS	Power/Other	
D11	VCC	Power/Other	
D12	VSS	Power/Other	
D13	VCC	Power/Other	
D14	VSS	Power/Other	
D15	VCC	Power/Other	
D16	VSS	Power/Other	
D17	VCC	Power/Other	
D18	VSS	Power/Other	
D19	VCC	Power/Other	
D20	VSS	Power/Other	
D21	VSS	Power/Other	
D22	D#[05]	Source Synch	Input/Output
D23	D#[13]	Source Synch	Input/Output

Table 22. Pin Listing by Pin Number

Pin Number	Pin Name	Signal Buffer Type	Direction
D24	VSS	Power/Other	
D25	D#[15]	Source Synch	Input/Output
D26	D#[23]	Source Synch	Input/Output
E1	VSS	Power/Other	
E2	DEFER#	Common Clock	Input
E3	HITM#	Common Clock	Input/Output
E4	VSS	Power/Other	
E5	LINT1	Asynch GTL+	Input
E6	TRST#	TAP	Input
E7	VSS	Power/Other	
E8	VCC	Power/Other	
E9	VSS	Power/Other	
E10	VCC	Power/Other	
E11	VSS	Power/Other	
E12	VCC	Power/Other	
E13	VSS	Power/Other	
E14	VCC	Power/Other	
E15	VSS	Power/Other	
E16	VCC	Power/Other	
E17	VSS	Power/Other	
E18	VCC	Power/Other	
E19	VSS	Power/Other	
E20	VCC	Power/Other	
E21	DBI#[0]	Source Synch	Input/Output
E22	DSTBN#[0]	Source Synch	Input/Output
E23	VSS	Power/Other	
E24	D#[17]	Source Synch	Input/Output
E25	D#[21]	Source Synch	Input/Output
E26	VSS	Power/Other	
F1	RS#[0]	Common Clock	Input
F2	VSS	Power/Other	
F3	HIT#	Common Clock	Input/Output
F4	RS#[2]	Common Clock	Input
F5	VSS	Power/Other	
F6	GTLREF	Power/Other	Input
F7	TMS	TAP	Input
F8	VSS	Power/Other	
F9	VCC	Power/Other	
F10	VSS	Power/Other	

Table 22. Pin Listing by Pin Number

Pin Number	Pin Name	Signal Buffer Type	Direction
F11	VCC	Power/Other	
F12	VSS	Power/Other	
F13	VCC	Power/Other	
F14	VSS	Power/Other	
F15	VCC	Power/Other	
F16	VSS	Power/Other	
F17	VCC	Power/Other	
F18	VSS	Power/Other	
F19	VCC	Power/Other	
F20	GTLREF	Power/Other	Input
F21	DSTBP#[0]	Source Synch	Input/Output
F22	VSS	Power/Other	
F23	D#[19]	Source Synch	Input/Output
F24	D#[20]	Source Synch	Input/Output
F25	VSS	Power/Other	
F26	D#[22]	Source Synch	Input/Output
G1	ADS#	Common Clock	Input/Output
G2	BNR#	Common Clock	Input/Output
G3	VSS	Power/Other	
G4	LOCK#	Common Clock	Input/Output
G5	RS#[1]	Common Clock	Input
G6	VSS	Power/Other	
G21	VSS	Power/Other	
G22	D#[10]	Source Synch	Input/Output
G23	D#[18]	Source Synch	Input/Output
G24	VSS	Power/Other	
G25	DBI#[1]	Source Synch	Input/Output
G26	D#[25]	Source Synch	Input/Output
H1	VSS	Power/Other	
H2	DRDY#	Common Clock	Input/Output
H3	REQ#[4]	Source Synch	Input/Output
H4	VSS	Power/Other	
H5	DBSY#	Common Clock	Input/Output
H6	BR0#	Common Clock	Input/Output
H21	D#[11]	Source Synch	Input/Output
H22	D#[16]	Source Synch	Input/Output
H23	VSS	Power/Other	
H24	D#[26]	Source Synch	Input/Output
H25	D#[31]	Source Synch	Input/Output

Table 22. Pin Listing by Pin Number

Pin Number	Pin Name	Signal Buffer Type	Direction
H26	VSS	Power/Other	
J1	REQ#[0]	Source Synch	Input/Output
J2	VSS	Power/Other	
J3	REQ#[3]	Source Synch	Input/Output
J4	REQ#[2]	Source Synch	Input/Output
J5	VSS	Power/Other	
J6	TRDY#	Common Clock	Input
J21	D#[14]	Source Synch	Input/Output
J22	VSS	Power/Other	
J23	DSTBP#[1]	Source Synch	Input/Output
J24	D#[29]	Source Synch	Input/Output
J25	VSS	Power/Other	
J26	DP#[0]	Common Clock	Input/Output
K1	A#[06]	Source Synch	Input/Output
K2	A#[03]	Source Synch	Input/Output
K3	VSS	Power/Other	
K4	A#[04]	Source Synch	Input/Output
K5	REQ#[1]	Source Synch	Input/Output
K6	VSS	Power/Other	
K21	VSS	Power/Other	
K22	DSTBN#[1]	Source Synch	Input/Output
K23	D#[30]	Source Synch	Input/Output
K24	VSS	Power/Other	
K25	DP#[1]	Common Clock	Input/Output
K26	DP#[2]	Common Clock	Input/Output
L1	VSS	Power/Other	
L2	A#[09]	Source Synch	Input/Output
L3	A#[07]	Source Synch	Input/Output
L4	VSS	Power/Other	
L5	ADSTB#[0]	Source Synch	Input/Output
L6	A#[05]	Source Synch	Input/Output
L21	D#[24]	Source Synch	Input/Output
L22	D#[28]	Source Synch	Input/Output
L23	VSS	Power/Other	
L24	COMP[0]	Power/Other	Input/Output
L25	DP#[3]	Common Clock	Input/Output
L26	VSS	Power/Other	
M1	A#[13]	Source Synch	Input/Output
M2	VSS	Power/Other	

Table 22. Pin Listing by Pin Number

Pin Number	Pin Name	Signal Buffer Type	Direction
M3	A#[10]	Source Synch	Input/Output
M4	A#[11]	Source Synch	Input/Output
M5	VSS	Power/Other	
M6	A#[08]	Source Synch	Input/Output
M21	D#[27]	Source Synch	Input/Output
M22	VSS	Power/Other	
M23	D#[32]	Source Synch	Input/Output
M24	D#[35]	Source Synch	Input/Output
M25	VSS	Power/Other	
M26	D#[37]	Source Synch	Input/Output
N1	A#[12]	Source Synch	Input/Output
N2	A#[14]	Source Synch	Input/Output
N3	VSS	Power/Other	
N4	A#[15]	Source Synch	Input/Output
N5	A#[16]	Source Synch	Input/Output
N6	VSS	Power/Other	
N21	VSS	Power/Other	
N22	D#[33]	Source Synch	Input/Output
N23	D#[36]	Source Synch	Input/Output
N24	VSS	Power/Other	
N25	D#[39]	Source Synch	Input/Output
N26	D#[38]	Source Synch	Input/Output
P1	COMP[1]	Power/Other	Input/Output
P2	VSS	Power/Other	
P3	A#[19]	Source Synch	Input/Output
P4	A#[20]	Source Synch	Input/Output
P5	VSS	Power/Other	
P6	A#[24]	Source Synch	Input/Output
P21	D#[34]	Source Synch	Input/Output
P22	VSS	Power/Other	
P23	DSTBP#[2]	Source Synch	Input/Output
P24	D#[41]	Source Synch	Input/Output
P25	VSS	Power/Other	
P26	DBI#[2]	Source Synch	Input/Output
R1	VSS	Power/Other	
R2	A#[18]	Source Synch	Input/Output
R3	A#[21]	Source Synch	Input/Output
R4	VSS	Power/Other	
R5	ADSTB#[1]	Source Synch	Input/Output

Table 22. Pin Listing by Pin Number

Pin Number	Pin Name	Signal Buffer Type	Direction
R6	A#[28]	Source Synch	Input/Output
R21	D#[40]	Source Synch	Input/Output
R22	DSTBN#[2]	Source Synch	Input/Output
R23	VSS	Power/Other	
R24	D#[43]	Source Synch	Input/Output
R25	D#[42]	Source Synch	Input/Output
R26	VSS	Power/Other	
T1	A#[17]	Source Synch	Input/Output
T2	A#[22]	Source Synch	Input/Output
T3	VSS	Power/Other	
T4	A#[26]	Source Synch	Input/Output
T5	A#[30]	Source Synch	Input/Output
T6	VSS	Power/Other	
T21	VSS	Power/Other	
T22	D#[46]	Source Synch	Input/Output
T23	D#[47]	Source Synch	Input/Output
T24	VSS	Power/Other	
T25	D#[45]	Source Synch	Input/Output
T26	D#[44]	Source Synch	Input/Output
U1	A#[23]	Source Synch	Input/Output
U2	VSS	Power/Other	
U3	A#[25]	Source Synch	Input/Output
U4	A#[31]	Source Synch	Input/Output
U5	VSS	Power/Other	
U6	TESTHI8	Power/Other	Input
U21	D#[52]	Source Synch	Input/Output
U22	VSS	Power/Other	
U23	D#[50]	Source Synch	Input/Output
U24	D#[49]	Source Synch	Input/Output
U25	VSS	Power/Other	
U26	D#[48]	Source Synch	Input/Output
V1	VSS	Power/Other	
V2	A#[27]	Source Synch	Input/Output
V3	A#[32]	Source Synch	Input/Output
V4	VSS	Power/Other	
V5	AP#[1]	Common Clock	Input/Output
V6	MCERR#	Common Clock	Input/Output
V21	DBI#[3]	Source Synch	Input/Output
V22	D#[53]	Source Synch	Input/Output

Table 22. Pin Listing by Pin Number

Pin Number	Pin Name	Signal Buffer Type	Direction
V23	VSS	Power/Other	
V24	D#[54]	Source Synch	Input/Output
V25	D#[51]	Source Synch	Input/Output
V26	VSS	Power/Other	
W1	A#[29]	Source Synch	Input/Output
W2	A#[33]	Source Synch	Input/Output
W3	VSS	Power/Other	
W4	TESTHI9	Power/Other	Input
W5	INIT#	Asynch GTL+	Input
W6	VSS	Power/Other	
W21	VSS	Power/Other	
W22	DSTBN#[3]	Source Synch	Input/Output
W23	DSTBP#[3]	Source Synch	Input/Output
W24	VSS	Power/Other	
W25	D#[57]	Source Synch	Input/Output
W26	D#[55]	Source Synch	Input/Output
Y1	A#[34]	Source Synch	Input/Output
Y2	VSS	Power/Other	
Y3	TESTHI10	Power/Other	Input
Y4	STPCLK#	Asynch GTL+	Input
Y5	VSS	Power/Other	
Y6	BPM#[3]	Common Clock	Input/Output
Y21	D#[60]	Source Synch	Input/Output
Y22	VSS	Power/Other	
Y23	D#[58]	Source Synch	Input/Output
Y24	D#[59]	Source Synch	Input/Output
Y25	VSS	Power/Other	
Y26	D#[56]	Source Synch	Input/Output

4.2 Alphabetical Signals Reference

Table 23. Signal Description (Sheet 1 of 8)

Name	Type	Description												
A[35:3]#	Input/Output	<p>A[35:3]# (Address) define a 2³⁶-byte physical memory address space. In sub-phase 1 of the address phase, these pins transmit the address of a transaction. In sub-phase 2, these pins transmit transaction type information. These signals must connect the appropriate pins of all agents on the Mobile Intel Pentium 4 Processor FSB. A[35:3]# are protected by parity signals AP[1:0]#. A[35:3]# are source synchronous signals and are latched into the receiving buffers by ADSTB[1:0]#.</p> <p>On the active-to-inactive transition of RESET#, the processor samples a subset of the A[35:3]# pins to determine power-on configuration. See Section 6.1 for more details.</p>												
A20M#	Input	<p>If A20M# (Address-20 Mask) is asserted, the processor masks physical address bit 20 (A20#) before looking up a line in any internal cache and before driving a read/write transaction on the bus. Asserting A20M# emulates the 8086 processor's address wrap-around at the 1-Mbyte boundary. Assertion of A20M# is only supported in real mode.</p> <p>A20M# is an asynchronous signal. However, to ensure recognition of this signal following an Input/Output write instruction, it must be valid along with the TRDY# assertion of the corresponding Input/Output Write bus transaction.</p>												
ADS#	Input/Output	<p>ADS# (Address Strobe) is asserted to indicate the validity of the transaction address on the A[35:3]# and REQ[4:0]# pins. All bus agents observe the ADS# activation to begin parity checking, protocol checking, address decode, internal snoop, or deferred reply ID match operations associated with the new transaction.</p>												
ADSTB[1:0]#	Input/Output	<p>Address strobes are used to latch A[35:3]# and REQ[4:0]# on their rising and falling edges. Strobes are associated with signals as shown below.</p> <table border="1"> <thead> <tr> <th>Signals</th> <th>Associated Strobe</th> </tr> </thead> <tbody> <tr> <td>REQ[4:0]#, A[16:3]#</td> <td>ADSTB0#</td> </tr> <tr> <td>A[35:17]#</td> <td>ADSTB1#</td> </tr> </tbody> </table>	Signals	Associated Strobe	REQ[4:0]#, A[16:3]#	ADSTB0#	A[35:17]#	ADSTB1#						
Signals	Associated Strobe													
REQ[4:0]#, A[16:3]#	ADSTB0#													
A[35:17]#	ADSTB1#													
AP[1:0]#	Input/Output	<p>AP[1:0]# (Address Parity) are driven by the request initiator along with ADS#, A[35:3]#, and the transaction type on the REQ[4:0]#. A correct parity signal is high if an even number of covered signals are low and low if an odd number of covered signals are low. This allows parity to be high when all the covered signals are high. AP[1:0]# should connect the appropriate pins of all mobile Intel Pentium 4 processor FSB agents. The following table defines the coverage model of these signals.</p> <table border="1"> <thead> <tr> <th>Request Signals</th> <th>subphase 1</th> <th>subphase 2</th> </tr> </thead> <tbody> <tr> <td>A[35:24]#</td> <td>AP0#</td> <td>AP1#</td> </tr> <tr> <td>A[23:3]#</td> <td>AP1#</td> <td>AP0#</td> </tr> <tr> <td>REQ[4:0]#</td> <td>AP1#</td> <td>AP0#</td> </tr> </tbody> </table>	Request Signals	subphase 1	subphase 2	A[35:24]#	AP0#	AP1#	A[23:3]#	AP1#	AP0#	REQ[4:0]#	AP1#	AP0#
Request Signals	subphase 1	subphase 2												
A[35:24]#	AP0#	AP1#												
A[23:3]#	AP1#	AP0#												
REQ[4:0]#	AP1#	AP0#												
BCLK[1:0]	Input	<p>The differential pair BCLK (Bus Clock) determines the FSB frequency. All processor FSB agents must receive these signals to drive their outputs and latch their inputs. All external timing parameters are specified with respect to the rising edge of BCLK0 crossing V_{CROSS}.</p>												

Table 23. Signal Description (Sheet 2 of 8)

Name	Type	Description
BINIT#	Input/ Output	<p>BINIT# (Bus Initialization) may be observed and driven by all processor FSB agents and if used, must connect the appropriate pins of all such agents. If the BINIT# driver is enabled during power-on configuration, BINIT# is asserted to signal any bus condition that prevents reliable future operation.</p> <p>If BINIT# observation is enabled during power-on configuration, and BINIT# is sampled asserted, symmetric agents reset their bus LOCK# activity and bus request arbitration state machines. The bus agents do not reset their IOQ and transaction tracking state machines upon observation of BINIT# activation. Once the BINIT# assertion has been observed, the bus agents will re-arbitrate for the FSB and attempt completion of their bus queue and IOQ entries.</p> <p>If BINIT# observation is disabled during power-on configuration, a central agent may handle an assertion of BINIT# as appropriate to the error handling architecture of the system.</p>
BNR#	Input/ Output	<p>BNR# (Block Next Request) is used to assert a bus stall by any bus agent who is unable to accept new bus transactions. During a bus stall, the current bus owner cannot issue any new transactions.</p>
BPM[5:0]#	Input/ Output	<p>BPM[5:0]# (Breakpoint Monitor) are breakpoint and performance monitor signals. They are outputs from the processor which indicate the status of breakpoints and programmable counters used for monitoring processor performance. BPM[5:0]# should connect the appropriate pins of all mobile Intel Pentium 4 processor FSB agents.</p> <p>BPM4# provides PRDY# (Probe Ready) functionality for the TAP port. PRDY# is a processor output used by debug tools to determine processor debug readiness.</p> <p>BPM5# provides PREQ# (Probe Request) functionality for the TAP port. PREQ# is used by debug tools to request debug operation of the processor.</p> <p>Please refer to the appropriate platform design guidelines listed in Table 1 and <i>ITP700 Debug Port Design Guide</i> for more detailed information.</p> <p>These signals do not have on-die termination and must be terminated on the system board.</p>
BPRI#	Input	<p>BPRI# (Bus Priority Request) is used to arbitrate for ownership of the processor FSB. It must connect the appropriate pins of all processor FSB agents. Observing BPRI# active (as asserted by the priority agent) causes all other agents to stop issuing new requests, unless such requests are part of an ongoing locked operation. The priority agent keeps BPRI# asserted until all of its requests are completed, then releases the bus by deasserting BPRI#.</p>
BR0#	Input/ Output	<p>BR0# drives the BREQ0# signal in the system and is used by the processor to request the bus. During power-on configuration this pin is sampled to determine the agent ID = 0.</p> <p>This signal does not have on-die termination and must be terminated.</p>
BSEL[1:0]	Output	<p>BSEL[1:0] (Bus Select) are used to select the processor input clock frequency. Table 5 defines the possible combinations of the signals and the frequency associated with each combination. The required frequency is determined by the processor, chipset and clock synthesizer. All agents must operate at the same frequency. The mobile Intel Pentium 4 processor operates at a 533 MHz FSB frequency (133-MHz BCLK[1:0] frequency). For more information about these pins, including termination recommendations refer to Section 2 and the appropriate platform design guidelines.</p>
COMP[1:0]	Analog	<p>COMP[1:0] must be terminated on the system board using precision resistors. Refer to the appropriate platform design guidelines listed in Table 1 for details on implementation.</p>

Table 23. Signal Description (Sheet 3 of 8)

Name	Type	Description															
D[63:0]#	Input/Output	<p>D[63:0]# (Data) are the data signals. These signals provide a 64-bit data path between the processor FSB agents, and must connect the appropriate pins on all such agents. The data driver asserts DRDY# to indicate a valid data transfer.</p> <p>D[63:0]# are quad-pumped signals and will thus be driven four times in a common clock period. D[63:0]# are latched off the falling edge of both DSTBP[3:0]# and DSTBN[3:0]#. Each group of 16 data signals correspond to a pair of one DSTBP# and one DSTBN#. The following table shows the grouping of data signals to data strobes and DBI#.</p> <p>Quad-Pumped Signal Groups</p> <table border="1"> <thead> <tr> <th>Data Group</th> <th>DSTBN#/DSTBP#</th> <th>DBI#</th> </tr> </thead> <tbody> <tr> <td>D[15:0]#</td> <td>0</td> <td>0</td> </tr> <tr> <td>D[31:16]#</td> <td>1</td> <td>1</td> </tr> <tr> <td>D[47:32]#</td> <td>2</td> <td>2</td> </tr> <tr> <td>D[63:48]#</td> <td>3</td> <td>3</td> </tr> </tbody> </table> <p>Furthermore, the DBI# pins determine the polarity of the data signals. Each group of 16 data signals corresponds to one DBI# signal. When the DBI# signal is active, the corresponding data group is inverted and therefore sampled active high.</p>	Data Group	DSTBN#/DSTBP#	DBI#	D[15:0]#	0	0	D[31:16]#	1	1	D[47:32]#	2	2	D[63:48]#	3	3
Data Group	DSTBN#/DSTBP#	DBI#															
D[15:0]#	0	0															
D[31:16]#	1	1															
D[47:32]#	2	2															
D[63:48]#	3	3															
DBI[3:0]#	Input/Output	<p>DBI[3:0]# (Data Bus Inversion) are source synchronous and indicate the polarity of the D[63:0]# signals. The DBI[3:0]# signals are activated when the data on the data bus is inverted. If more than half the data bits, within a 16-bit group, would have been asserted electrically low, the bus agent may invert the data bus signals for that particular sub-phase for that 16 bit group.</p> <p>DBI[3:0] Assignment To Data Bus</p> <table border="1"> <thead> <tr> <th>Bus Signal</th> <th>Data Bus Signals</th> </tr> </thead> <tbody> <tr> <td>DBI3#</td> <td>D[63:48]#</td> </tr> <tr> <td>DBI2#</td> <td>D[47:32]#</td> </tr> <tr> <td>DBI1#</td> <td>D[31:16]#</td> </tr> <tr> <td>DBI0#</td> <td>D[15:0]#</td> </tr> </tbody> </table>	Bus Signal	Data Bus Signals	DBI3#	D[63:48]#	DBI2#	D[47:32]#	DBI1#	D[31:16]#	DBI0#	D[15:0]#					
Bus Signal	Data Bus Signals																
DBI3#	D[63:48]#																
DBI2#	D[47:32]#																
DBI1#	D[31:16]#																
DBI0#	D[15:0]#																
DBR#	Output	<p>DBR# (Data Bus Reset) is used only in processor systems where no debug port is implemented on the system board. DBR# is used by a debug port interposer so that an in-target probe can drive system reset. If a debug port is implemented in the system, DBR# is a no connect in the system. DBR# is not a processor signal.</p>															
DBSY#	Input/Output	<p>DBSY# (Data Bus Busy) is asserted by the agent responsible for driving data on the processor FSB to indicate that the data bus is in use. The data bus is released after DBSY# is deasserted. This signal must connect the appropriate pins on all processor FSB agents.</p>															
DEFER#	Input	<p>DEFER# is asserted by an agent to indicate that a transaction cannot be guaranteed in-order completion. Assertion of DEFER# is normally the responsibility of the addressed memory or Input/Output agent. This signal must connect the appropriate pins of all processor FSB agents.</p>															
DP[3:0]#	Input/Output	<p>DP[3:0]# (Data parity) provide parity protection for the D[63:0]# signals. They are driven by the agent responsible for driving D[63:0]#, and must connect the appropriate pins of all mobile Intel Pentium 4 processor FSB agents.</p>															

Table 23. Signal Description (Sheet 4 of 8)

Name	Type	Description										
DPSP#	Input	DPSP# when asserted on the platform causes the processor to transition from the Sleep State to the Deep Sleep state. In order to return to the Sleep State, DPSP# must be deasserted and BCLK[1:0] must be running.										
DRDY#	Input/Output	DRDY# (Data Ready) is asserted by the data driver on each data transfer, indicating valid data on the data bus. In a multi-common clock data transfer, DRDY# may be deasserted to insert idle clocks. This signal must connect the appropriate pins of all processor FSB agents.										
DSTBN[3:0]#	Input/Output	Data strobe used to latch in D[63:0]#. <table border="1" data-bbox="625 598 1107 808"> <thead> <tr> <th>Signals</th> <th>Associated Strobe</th> </tr> </thead> <tbody> <tr> <td>D[15:0]#, DBI0#</td> <td>DSTBN0#</td> </tr> <tr> <td>D[31:16]#, DBI1#</td> <td>DSTBN1#</td> </tr> <tr> <td>D[47:32]#, DBI2#</td> <td>DSTBN2#</td> </tr> <tr> <td>D[63:48]#, DBI3#</td> <td>DSTBN3#</td> </tr> </tbody> </table>	Signals	Associated Strobe	D[15:0]#, DBI0#	DSTBN0#	D[31:16]#, DBI1#	DSTBN1#	D[47:32]#, DBI2#	DSTBN2#	D[63:48]#, DBI3#	DSTBN3#
Signals	Associated Strobe											
D[15:0]#, DBI0#	DSTBN0#											
D[31:16]#, DBI1#	DSTBN1#											
D[47:32]#, DBI2#	DSTBN2#											
D[63:48]#, DBI3#	DSTBN3#											
DSTBP[3:0]#	Input/Output	Data strobe used to latch in D[63:0]#. <table border="1" data-bbox="625 877 1107 1087"> <thead> <tr> <th>Signals</th> <th>Associated Strobe</th> </tr> </thead> <tbody> <tr> <td>D[15:0]#, DBI0#</td> <td>DSTBP0#</td> </tr> <tr> <td>D[31:16]#, DBI1#</td> <td>DSTBP1#</td> </tr> <tr> <td>D[47:32]#, DBI2#</td> <td>DSTBP2#</td> </tr> <tr> <td>D[63:48]#, DBI3#</td> <td>DSTBP3#</td> </tr> </tbody> </table>	Signals	Associated Strobe	D[15:0]#, DBI0#	DSTBP0#	D[31:16]#, DBI1#	DSTBP1#	D[47:32]#, DBI2#	DSTBP2#	D[63:48]#, DBI3#	DSTBP3#
Signals	Associated Strobe											
D[15:0]#, DBI0#	DSTBP0#											
D[31:16]#, DBI1#	DSTBP1#											
D[47:32]#, DBI2#	DSTBP2#											
D[63:48]#, DBI3#	DSTBP3#											
FERR#/PBE#	Output	FERR#/PBE# (floating point error/pending break event) is a multiplexed signal and its meaning is qualified by STPCLK#. When STPCLK# is not asserted, FERR#/PBE# indicates a floating-point error and will be asserted when the processor detects an unmasked floating-point error. When STPCLK# is not asserted, FERR#/PBE# is similar to the ERROR# signal on the INTEL 387 coprocessor, and is included for compatibility with systems using MS-DOS*-type floating-point error reporting. When STPCLK# is asserted, an assertion of FERR#/PBE# indicates that the processor has a pending break event waiting for service. The assertion of FERR#/PBE# indicates that the processor should be returned to the Normal state. When FERR#/PBE# is asserted, indicating a break event, it will remain asserted until STPCLK# is deasserted. For additional information on the pending break event functionality, including the identification of support of the feature and enable/disable information, refer to volume 3 of the <i>Intel Architecture Software Developer's Manual and the Intel Processor Identification and the CPUID Instruction</i> application note.										
GHI#	Input	The GHI# signal controls the selection of the operating mode bus ratio and voltage in the mobile Intel Pentium 4 processor. On the mobile Intel Pentium 4 processor featuring Enhanced Intel SpeedStep technology, this signal is latched on entry to Sleep state and is observed during the Deep Sleep state. GHI# determines which of two performance states is selected for operation. This signal is ignored when the processor is not in the Deep Sleep state. This signal should be driven with an Open-drain driver. Refer to the appropriate platform design guidelines listed in Table 1 for termination and connection guidelines.										
GTLREF	Input	GTLREF determines the signal reference level for GTL+ input pins. GTLREF should be set at $\frac{2}{3} V_{CC}$. GTLREF is used by the GTL+ receivers to determine if a signal is a logical 0 or logical 1. Refer to the appropriate platform design guidelines listed in Table 1 for more information.										

Table 23. Signal Description (Sheet 5 of 8)

Name	Type	Description
HIT# HITM#	Input/ Output Input/ Output	HIT# (Snoop Hit) and HITM# (Hit Modified) convey transaction snoop operation results. Any FSB agent may assert both HIT# and HITM# together to indicate that it requires a snoop stall, which can be continued by reasserting HIT# and HITM# together.
IERR#	Output	IERR# (Internal Error) is asserted by a processor as the result of an internal error. Assertion of IERR# is usually accompanied by a SHUTDOWN transaction on the processor FSB. This transaction may optionally be converted to an external error signal (e.g., NMI) by system core logic. The processor will keep IERR# asserted until the assertion of RESET#. This signal does not have on-die termination and must be terminated on the system board.
IGNNE#	Input	IGNNE# (Ignore Numeric Error) is asserted to force the processor to ignore a numeric error and continue to execute noncontrol floating-point instructions. If IGNNE# is deasserted, the processor generates an exception on a noncontrol floating-point instruction if a previous floating-point instruction caused an error. IGNNE# has no effect when the NE bit in control register 0 (CR0) is set. IGNNE# is an asynchronous signal. However, to ensure recognition of this signal following an Input/Output write instruction, it must be valid along with the TRDY# assertion of the corresponding Input/Output Write bus transaction.
IMPSEL	Input	IMPSEL input will determine whether the processor uses a 50 ohm or 60 ohm buffer. This pin must be tied to GND on 50 ohm platforms and left as NC on 60 ohm platforms.
INIT#	Input	INIT# (Initialization), when asserted, resets integer registers inside the processor without affecting its internal caches or floating-point registers. The processor then begins execution at the power-on Reset vector configured during power-on configuration. The processor continues to handle snoop requests during INIT# assertion. INIT# is an asynchronous signal and must connect the appropriate pins of all processor FSB agents. If INIT# is sampled active on the active to inactive transition of RESET#, then the processor executes its Built-in Self-Test (BIST).
ITPCLKOUT [1:0]	Output	ITPCLKOUT[1:0] is an uncompensated differential clock output that is a delayed copy of the BCLK[1:0], which is an input to the processor. This clock output can be used as the differential clock into the ITP port that is designed onto the motherboard. If ITPCLKOUT[1:0] outputs are not used, they must be terminated properly. Refer to Section 2.5 for additional details and termination requirements. Refer to the <i>ITP700 Debug Port Design Guide</i> for details on implementing a debug port.
ITP_CLK[1:0]	Input	ITP_CLK[1:0] are copies of BCLK that are used only in processor systems where no debug port is implemented on the system board. ITP_CLK[1:0] are used as BCLK[1:0] references for a debug port implemented on an interposer. If a debug port is implemented in the system, ITP_CLK[1:0] are no connects in the system. These are not processor signals.
LINT[1:0]	Input	LINT[1:0] (Local APIC Interrupt) must connect the appropriate pins of all APIC Bus agents. When the APIC is disabled, the LINT0 signal becomes INTR, a maskable interrupt request signal, and LINT1 becomes NMI, a nonmaskable interrupt. INTR and NMI are backward compatible with the signals of those names on the Pentium processor. Both signals are asynchronous. Both of these signals must be software configured via BIOS programming of the APIC register space to be used either as NMI/INTR or LINT[1:0]. Because the APIC is enabled by default after Reset, operation of these pins as LINT[1:0] is the default configuration.

Table 23. Signal Description (Sheet 6 of 8)

Name	Type	Description
LOCK#	Input/ Output	<p>LOCK# indicates to the system that a transaction must occur atomically. This signal must connect the appropriate pins of all processor FSB agents. For a locked sequence of transactions, LOCK# is asserted from the beginning of the first transaction to the end of the last transaction.</p> <p>When the priority agent asserts BPRI# to arbitrate for ownership of the processor FSB, it will wait until it observes LOCK# deasserted. This enables symmetric agents to retain ownership of the processor FSB throughout the bus locked operation and ensure the atomicity of lock.</p>
MCERR#	Input/ Output	<p>MCERR# (Machine Check Error) is asserted to indicate an unrecoverable error without a bus protocol violation. It may be driven by all processor FSB agents. MCERR# assertion conditions are configurable at a system level. Assertion options are defined by the following options:</p> <ul style="list-style-type: none"> • Enabled or disabled. • Asserted, if configured, for internal errors along with IERR#. • Asserted, if configured, by the request initiator of a bus transaction after it observes an error. • Asserted by any bus agent when it observes an error in a bus transaction. <p>For more details regarding machine check architecture, please refer to the <i>IA-32 Software Developer's Manual, Volume 3: System Programming Guide</i>.</p>
PROCHOT#	Input/ Output	<p>As an output, PROCHOT# (Processor Hot) will go active when the processor temperature monitoring sensor detects that the processor has reached its maximum safe operating temperature. This indicates that the processor Thermal Control Circuit has been activated, if enabled. As an input, assertion of PROCHOT# by the system will activate the TCC, if enabled. The TCC will remain active until the system deasserts PROCHOT#. See Section 6 for more details.</p>
PWRGOOD	Input	<p>PWRGOOD (Power Good) is a processor input. The processor requires this signal to be a clean indication that the clocks and power supplies are stable and within their specifications. 'Clean' implies that the signal will remain low (capable of sinking leakage current), without glitches, from the time that the power supplies are turned on until they come within specification. The signal must then transition monotonically to a high state. Figure 14 illustrates the relationship of PWRGOOD to the RESET# signal. PWRGOOD can be driven inactive at any time, but clocks and power must again be stable before a subsequent rising edge of PWRGOOD. It must also meet the minimum pulse width specification in Table 22, and be followed by a 1 to 10 ms RESET# pulse.</p> <p>The PWRGOOD signal must be supplied to the processor; it is used to protect internal circuits against voltage sequencing issues. It should be driven high throughout boundary scan operation.</p>
REQ[4:0]#	Input/ Output	<p>REQ[4:0]# (Request Command) must connect the appropriate pins of all processor FSB agents. They are asserted by the current bus owner to define the currently active transaction type. These signals are source synchronous to ADSTB0#. Refer to the AP[1:0]# signal description for details on parity checking of these signals.</p>
RESET#	Input	<p>Asserting the RESET# signal resets the processor to a known state and invalidates its internal caches without writing back any of their contents. For a power-on Reset, RESET# must stay active for at least one millisecond after Vcc and BCLK have reached their proper specifications. On observing active RESET#, all FSB agents will deassert their outputs within two clocks. RESET# must not be kept asserted for more than 10 ms while PWRGOOD is asserted.</p> <p>A number of bus signals are sampled at the active-to-inactive transition of RESET# for power-on configuration. These configuration options are described in the Section 6.1.</p> <p>This signal does not have on-die termination and must be terminated on the system board.</p>

Table 23. Signal Description (Sheet 7 of 8)

Name	Type	Description
RS[2:0]#	Input	RS[2:0]# (Response Status) are driven by the response agent (the agent responsible for completion of the current transaction), and must connect the appropriate pins of all processor FSB agents.
RSP#	Input	RSP# (Response Parity) is driven by the response agent (the agent responsible for completion of the current transaction) during assertion of RS[2:0]#, the signals for which RSP# provides parity protection. It must connect to the appropriate pins of all processor FSB agents. A correct parity signal is high if an even number of covered signals are low and low if an odd number of covered signals are low. While RS[2:0]# = 000, RSP# is also high, since this indicates it is not being driven by any agent guaranteeing correct parity.
SKTOCC#	Output	SKTOCC# (Socket Occupied) will be pulled to ground by the processor. System board designers may use this pin to determine if the processor is present.
SLP#	Input	SLP# (Sleep), when asserted in Stop-Grant state, causes the processor to enter the Sleep state. During Sleep state, the processor stops providing internal clock signals to all units, leaving only the Phase-Locked Loop (PLL) still operating. Processors in this state will not recognize snoops or interrupts. The processor will only recognize the assertion of the RESET# signal, deassertion of SLP#, and assertion of DPSP# input while in Sleep state. If SLP# is deasserted, the processor exits Sleep state and returns to Stop-Grant state, restarting its internal clock signals to the bus and processor core units. If the BCLK input is stopped or if DPSP# is asserted while in the Sleep state, the processor will exit the Sleep state and transition to the Deep Sleep state.
SMI#	Input	SMI# (System Management Interrupt) is asserted asynchronously by system logic. On accepting a System Management Interrupt, the processor saves the current state and enter System Management Mode (SMM). An SMI Acknowledge transaction is issued, and the processor begins program execution from the SMM handler. If SMI# is asserted during the deassertion of RESET# the processor will tristate its outputs.
STPCLK#	Input	Assertion of STPCLK# (Stop Clock) causes the processor to enter a low power Stop-Grant state. The processor issues a Stop-Grant Acknowledge transaction, and stops providing internal clock signals to all processor core units except the FSB and APIC units. The processor continues to snoop bus transactions and service interrupts while in Stop-Grant state. When STPCLK# is deasserted, the processor restarts its internal clock to all units and resumes execution. The assertion of STPCLK# has no effect on the bus clock; STPCLK# is an asynchronous input.
TCK	Input	TCK (Test Clock) provides the clock input for the processor Test Bus (also known as the Test Access Port).
TDI	Input	TDI (Test Data In) transfers serial test data into the processor. TDI provides the serial input needed for JTAG specification support.
TDO	Output	TDO (Test Data Out) transfers serial test data out of the processor. TDO provides the serial output needed for JTAG specification support.
TESTHI[10:8] TESTHI[5:0]	Input	TESTHI[10:8] and TESTHI[5:0] must be connected to a V _{CC} power source through a resistor for proper processor operation. See Section 2.5 for more details.
THERMDA	Other	Thermal Diode Anode. See Section 5.
THERMDC	Other	Thermal Diode Cathode. See Section 5.

Table 23. Signal Description (Sheet 8 of 8)

Name	Type	Description
THERMTRIP#	Output	Assertion of THERMTRIP# (Thermal Trip) indicates the processor junction temperature has reached a level beyond which permanent silicon damage may occur. Measurement of the temperature is accomplished through an internal thermal sensor which is configured to trip at approximately 135°C. Upon assertion of THERMTRIP#, the processor will shut off its internal clocks (thus halting program execution) in an attempt to reduce the processor junction temperature. To protect the processor, its core voltage (V _{CC}) must be removed following the assertion of THERMTRIP#. Driving of the THERMTRIP# signal is enabled within 10us of the assertion of PWRGOOD and is disabled on deassertion of PWRGOOD. Once activated, THERMTRIP# remains latched until PWRGOOD is de-asserted. While the deassertion of the PWRGOOD signal will de-assert THERMTRIP#, if the processor's junction temperature remains at or above the trip level, THERMTRIP# will again be asserted within 10us of the assertion of PWRGOOD.
TMS	Input	TMS (Test Mode Select) is a JTAG specification support signal used by debug tools.
TRDY#	Input	TRDY# (Target Ready) is asserted by the target to indicate that it is ready to receive a write or implicit writeback data transfer. TRDY# must connect the appropriate pins of all FSB agents.
TRST#	Input	TRST# (Test Reset) resets the Test Access Port (TAP) logic. TRST# must be driven low during power on Reset. This can be done with a 680-ohm, pull-down resistor.
V _{CCA}	Input	V _{CCA} provides isolated power for the internal processor core PLL's. Refer to the appropriate platform design guidelines listed in Table 1 for complete implementation details.
V _{CCIOPLL}	Input	V _{CCIOPLL} provides isolated power for internal processor FSB PLL's. Follow the guidelines for V _{CCA} , and refer to the appropriate platform design guidelines listed in Table 1 for complete implementation details.
V _{CCSENSE}	Output	V _{CCSENSE} is an isolated low impedance connection to processor core power (V _{CC}). It can be used to sense or measure power near the silicon with little noise.
VCCVID	Input	Independent 1.2-V supply must be routed to VCCVID pin for the mobile Intel Pentium 4 processor's Voltage Identification circuit.
VID[4:0]	Output	VID[4:0] (Voltage ID) pins are used to support automatic selection of power supply voltages (V _{CC}). Unlike some previous generations of processors, these are open drain signals that are driven by the mobile Intel Pentium 4 processor and must be pulled up to 3.3 V (max.) with 1-kohm resistors. The voltage supply for these pins must be valid before the VR can supply V _{CC} to the processor. Conversely, the VR output must be disabled until the voltage supply for the VID pins becomes valid. The VID pins are needed to support the processor voltage specification variations. See Table 3 for definitions of these pins. The VR must supply the voltage that is requested by the pins, or disable itself.
V _{SSA}	Input	V _{SSA} is the isolated ground for internal PLLs.
V _{SSSENSE}	Output	V _{SSSENSE} is an isolated low impedance connection to processor core V _{SS} . It can be used to sense or measure ground near the silicon with little noise.

5 Thermal Specifications and Design Considerations

5.1 Processor Thermal Specifications

The mobile Intel Pentium 4 processor with 533 MHz FSB processor requires a thermal solution to maintain temperatures within the operating limits as set forth in [Section 5.1.1](#). Any attempt to operate the processor outside these operating limits may result in permanent damage to the processor and potentially other components within the system. As processor technology changes, thermal management becomes increasingly crucial when building computer systems. Maintaining the proper thermal environment is key to reliable, long-term system operation.

A complete thermal solution includes both component and system level thermal management features. Component level thermal solutions can include active or passive heatsinks attached to the processor Integrated Heat Spreader (IHS). Typical system level thermal solutions may consist of system fans combined with ducting and venting.

For more information on designing a component level thermal solution, refer to the *Mobile Intel® Pentium® 4 Processor Thermal Design Guidelines for Transportable Systems*.

5.1.1 Thermal Specifications

To allow for the optimal operation and long-term reliability of Intel processor-based systems, the system/processor thermal solution should be designed such that the processor remains between the minimum and maximum case temperature (TC) specifications when operating at or below the corresponding Thermal Design Power (TDP) value listed per frequency in [Table 24](#). Thermal solutions not designed to provide this level of thermal capability may affect the long-term reliability of the processor and system. For more details on thermal solution design, please refer to the appropriate processor thermal design guidelines.

The case temperature is defined at the geometric top center of the processor IHS. Analysis indicates that real applications are unlikely to cause the processor to consume maximum power dissipation for sustained periods of time. Intel recommends that complete thermal solution designs target the TDP indicated in [Table 24](#) instead of the maximum processor power consumption. The Intel® Thermal Monitor feature is intended to help protect the processor in the unlikely event that an application exceeds the TDP recommendation for a sustained period of time. For more details on the usage of this feature, refer to [Section 6.2](#). To ensure maximum flexibility for future requirements, systems should be designed to the Fixed Mobile Solution (FMS) guidelines, even if a processor with a lower thermal dissipation is currently planned. **In all cases, the Intel Thermal Monitor feature must be enabled for the processor to remain within specification.**

Table 24. Processor Thermal Design Power

Processor and Core Frequency ³	Thermal Design Power ^{1,2} (W)	Minimum T _{CASE} (°C)	Maximum T _{CASE} (°C)	Notes
Processors with multiple VIDs:				
2.40 GHz	59.8	5	71	
2.66 GHz	66.1	5	74	5
2.80 GHz	68.4	5	75	5
3.06 GHz	70	5	74	5
3.20 GHz	76	5	72	5
FMS0	70	5	74	4
FMS0.5	76	5	72	4

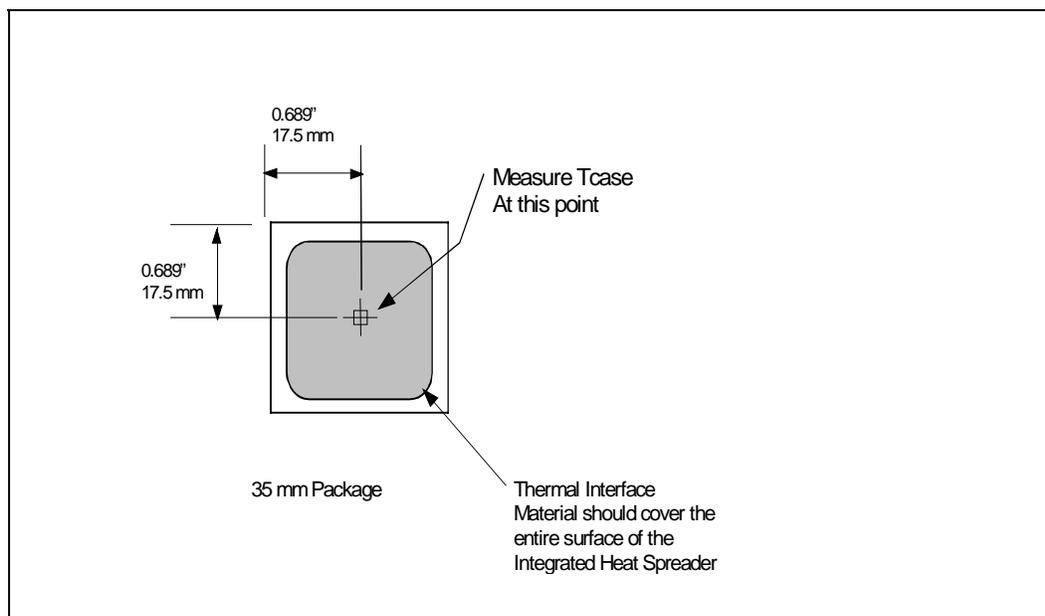
NOTES:

1. These values are specified at V_{CC_MAX} for the processor. Systems must be designed to ensure that the processor is not subjected to any static V_{CC} and I_{CC} combination wherein V_{CC} exceeds V_{CC_MAX} at specified I_{CC} . Please refer to loadline specifications in [Section 2](#).
2. The numbers in this column reflect Intel's recommended design point and are not indicative of the maximum power the processor can dissipate under worst case conditions. For more details refer to the *Mobile Intel® Pentium® 4 Processor Thermal Design Guidelines for Transportable Systems*.
3. Listed frequency and VID combinations are not necessarily committed production frequency and VID combinations.
4. FMS, or Fixed Mobile Solution guidelines provide a design target for meeting future thermal requirements.
5. This product is also available with Hyper-Threading Technology.

5.1.2 Measurements for Thermal Specifications

5.1.2.1 Processor Case Temperature Measurement

The maximum and minimum case temperature (T_C) for the mobile Intel Pentium 4 processor with 533 MHz FSB is specified in [Table 24](#). This temperature specification is meant to help ensure proper operation of the processor. [Figure 15](#) illustrates where Intel recommends T_C thermal measurements should be made.

Figure 15. Guideline Locations for Case Temperature (T_{CASE}) Thermocouple Placement

5.2 Processor Thermal Features

5.2.1 Intel Thermal Monitor

The Intel Thermal Monitor feature helps control the processor temperature by activating the thermal control circuit (TCC) when the processor silicon reaches its maximum operating temperature. The TCC reduces processor power consumption by modulating (starting and stopping) the internal processor core clocks. **The Intel Thermal Monitor feature must be enabled for the processor to be operating within specifications.** The temperature at which Intel Thermal Monitor activates the thermal control circuit is not user configurable and is not software visible. Bus traffic is snooped in the normal manner, and interrupt requests are latched (and serviced during the time that the clocks are on) while the TCC is active.

When the Intel Thermal Monitor feature is enabled, and a high temperature situation exists (i.e. TCC is active), the clocks will be modulated by alternately turning the clocks off and on at a duty cycle specific to the processor (typically 30-50%). Clocks often will not be off for more than 3.0 microseconds when the TCC is active. Cycle times are processor speed dependent and will decrease as processor core frequencies increase. A small amount of hysteresis has been included to prevent rapid active/inactive transitions of the TCC when the processor temperature is near its maximum operating temperature. Once the temperature has dropped below the maximum operating temperature, and the hysteresis timer has expired, the TCC goes inactive and clock modulation ceases.

With a properly designed and characterized thermal solution, it is anticipated that the TCC would only be activated for very short periods of time when running the most power intensive applications. The processor performance impact due to these brief periods of TCC activation is expected to be so minor that it would be immeasurable. An under-designed thermal solution that is not able to prevent excessive activation of the TCC in the anticipated ambient environment may

cause a noticeable performance loss, and in some cases may result in a T_C that exceeds the specified maximum temperature and may affect the long-term reliability of the processor. In addition, a thermal solution that is significantly under designed may not be capable of cooling the processor even when the TCC is active continuously. Refer to the *Mobile Intel® Pentium® 4 Processor Thermal Design Guidelines for Transportable Systems* for information on designing a thermal solution.

The duty cycle for the TCC, when activated by the Intel Thermal Monitor, is factory configured and cannot be modified. The Intel Thermal Monitor does not require any additional hardware, software drivers, or interrupt handling routines.

5.2.2 On-Demand Mode

The mobile Intel Pentium 4 processor with 533 MHz FSB provides an auxiliary mechanism that allows system software to force the processor to reduce its power consumption. This mechanism is referred to as "On-Demand" mode and is distinct from the Intel Thermal Monitor feature. On-Demand mode is intended as a means to reduce system level power consumption. Systems utilizing the mobile Intel Pentium 4 processor with 533 MHz FSB must not rely on software usage of this mechanism to limit the processor temperature.

If bit 4 of the ACPI P_CNT Control register (located in the processor IA32_THERM_CONTROL MSR) is written to a 1, the processor will immediately reduce its power consumption via modulation (starting and stopping) of the internal core clock, independent of the processor temperature. When using On-Demand mode, the duty cycle of the clock modulation is programmable via bits 3:1 of the same ACPI P_CNT Control register. In On-Demand mode, the duty cycle can be programmed from 12.5% on/87.5% off, to 87.5% on/12.5% off in 12.5% increments. On-Demand mode may be used in conjunction with the Intel Thermal Monitor. If the system tries to enable On-Demand mode at the same time the TCC is engaged, the factory configured duty cycle of the TCC will override the duty cycle selected by the On-Demand mode.

5.2.3 PROCHOT# Signal Pin

An external signal, PROCHOT# (processor hot), is asserted when the processor die temperature has reached its maximum operating temperature. If the Intel Thermal Monitor is enabled (note that the Intel Thermal Monitor must be enabled for the processor to be operating within specification), the TCC will be active when PROCHOT# is asserted. The processor can be configured to generate an interrupt upon the assertion or deassertion of PROCHOT#. Refer to the *Intel Architecture Software Developer's Manuals* and *Intel NetBurst micro-architecture BIOS Writer's Guide* for specific register and programming details.

The mobile Intel Pentium 4 processor with 533 MHz FSB implements a bi-directional PROCHOT# capability to allow system designs to protect various components from over-temperature situations. The PROCHOT# signal is bi-directional in that it can either signal when the processor has reached its maximum operating temperature or be driven from an external source to activate the TCC. The ability to activate the TCC via PROCHOT# can provide a means for thermal protection of system components.

One application is the thermal protection of voltage regulators (VR). System designers can create a circuit to monitor the VR temperature and activate the TCC when the temperature limit of the VR is reached. By asserting PROCHOT# (pulled-low) and activating the TCC, the VR can cool down as a result of reduced processor power consumption. Bi-directional PROCHOT# can allow VR thermal designs to target maximum sustained current instead of maximum current. Systems should still provide proper cooling for the VR, and rely on bi-directional PROCHOT# only as a backup in

case of system cooling failure. The system thermal design should allow the power delivery circuitry to operate within its temperature specification even while the processor is operating at its TDP. With a properly designed and characterized thermal solution, it is anticipated that PROCHOT# would only be activated for very short periods of time when running the most power intensive applications. An under-designed thermal solution that is not able to prevent excessive assertion of PROCHOT# in the anticipated ambient environment may cause a noticeable performance loss. Refer to the *Intel® 852GM/852PM Chipset Platform Design Guide* for details on implementing the bi-directional PROCHOT# feature.

5.2.4 THERMTRIP# Signal Pin

Regardless of whether or not the Intel Thermal Monitor feature is enabled, in the event of a catastrophic cooling failure, the processor will automatically shut down when the silicon has reached an elevated temperature (refer to the THERMTRIP# definition in [Table 23](#)). At this point, the FSB signal THERMTRIP# will go active and stay active as described in [Table 23](#). THERMTRIP# activation is independent of processor activity and does not generate any bus cycles. If THERMTRIP# is asserted, processor core voltage (Vcc) must be removed within the timeframe defined in [Table 22](#).

5.2.5 Thermal Diode

The mobile Intel Pentium 4 processor with 533 MHz FSB incorporates an on-die thermal diode. A thermal sensor located on the system board may monitor the die temperature of the processor for thermal management/long term die temperature change purposes. [Table 25](#) and [Table 26](#) provide the diode parameter and interface specifications. This thermal diode is separate from the Intel Thermal Monitor's thermal sensor and cannot be used to predict the behavior of the Intel Thermal Monitor.

Note: The reading of the thermal sensor connected to the thermal diode does not reflect the temperature of the hottest location on the die. This is due to inaccuracies in the thermal diode, on-die temperature gradients between the location of the thermal diode and the hottest location on the die, and time based variations in the die temperature. Time based variations can occur since the sampling rate of the sensor is much slower than the die level temperature changes.

Table 25. Thermal Diode Parameters

Symbol	Parameter	Min	Typ	Max	Unit	Notes
I_{FW}	Forward Bias Current	5		300	uA	1
n	Diode Ideality Factor	1.0011	1.0021	1.0030		2,3,4
R_T	Series Resistance		3.64			2,3,4, 5

NOTES:

- Intel does not support or recommend operation of the thermal diode under reverse bias.
- Characterized at 75C.
- Not 100% tested. Specified by design characterization.
- The ideality factor, n, represents the deviation from ideal diode behavior as exemplified by the diode equation:

$$I_{FW} = I_s * (e^{(qV_D/nkT)} - 1)$$
 Where I_s = saturation current, q = electronic charge, V_D = voltage across the diode, k = Boltzmann Constant, and T = absolute temperature (Kelvin).
- The series resistance, R_T , is provided to allow for a more accurate measurement of the diode junction temperature. R_T as defined includes the pins of the processor but does not include any socket resistance or board trace resistance between the socket and the external remote diode thermal sensor. R_T can be used by remote diode thermal sensors with automatic series resistance cancellation to calibrate out this error term. Another application is that a temperature offset can be manually calculated and programmed into an offset register in the remote diode thermal sensors as exemplified by the equation:

$$T_{error} = [R_T * (N - 1) * I_{FWmin}] / [(nk/q) * \ln N]$$
 Where T_{error} = sensor temperature error, N = sensor current ratio, k = Boltzmann Constant, q = electronic charge.

Table 26. Thermal Diode Interface

Pin Name	Pin Number	Pin Description
THERMDA	B3	diode anode
THERMDC	C4	diode cathode

6 Configuration and Low Power Features

6.1 Power-On Configuration Options

Several configuration options can be configured by hardware. The mobile Intel Pentium 4 processor samples its hardware configuration at reset, on the active-to-inactive transition of RESET#. For specifications on these options, please refer to [Table 27](#).

Frequency determination functionality will exist on engineering sample processors which means that samples can run at varied frequencies. Production material will have the bus to core ratio locked during manufacturing and can only be operated at the rated frequency.

The sampled information configures the processor for subsequent operation. These configuration options cannot be changed except by another reset. All resets reconfigure the processor.

Table 27. Power-On Configuration Option Pins

Configuration Option	Pin ¹
Output tristate	SMI#
Execute BIST	INIT#
In Order Queue pipelining (set IOQ depth to 1)	A7#
Disable MCERR# observation	A9#
Disable BINIT# observation	A10#
APIC Cluster ID (0-3)	A[12:11]#
Disable bus parking	A15#
Symmetric agent arbitration ID	BR0#

NOTE: Asserting this signal during RESET# will select the corresponding option.

6.2 Clock Control and Low Power States

The use of AutoHALT, Stop-Grant, Sleep, Deep Sleep and Deeper Sleep states is allowed in mobile Intel Pentium 4 processor based systems to reduce power consumption by stopping the clock to internal sections of the processor, depending on each particular state. See [Figure 16](#) for a visual representation of the processor low-power states.

6.2.1 Normal State

This is the normal operating state for the processor.

6.2.2 AutoHALT Powerdown State

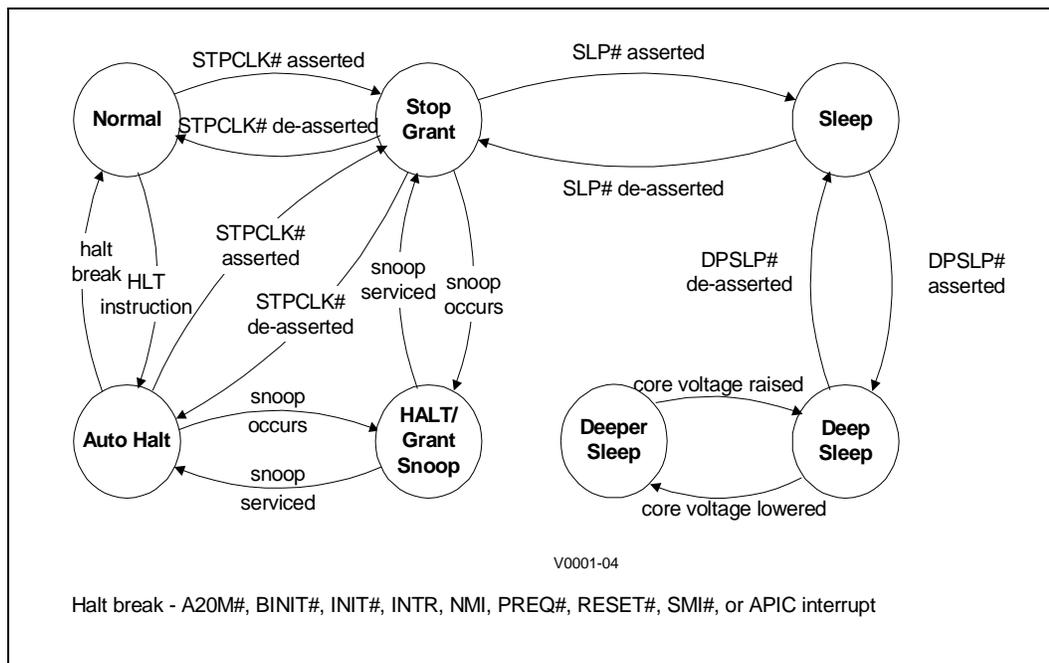
AutoHALT is a low-power state entered when the processor executes the HALT instruction. The processor will transition to the Normal state upon the occurrence of SMI#, BINIT#, INIT#, LINT[1:0] (NMI, INTR), or PSB interrupt message. RESET# will cause the processor to immediately initialize itself.

The return from a System Management Interrupt (SMI) handler can be to either Normal mode or the AutoHALT Powerdown state. See the *Intel Architecture Software Developer's Manual, Volume III: System Programmer's Guide* for more information.

The system can generate a STPCLK# while the processor is in the AutoHALT Powerdown state. When the system deasserts the STPCLK# interrupt, the processor will return execution to the HALT state.

While in AutoHALT Power Down state, the processor will process FSB snoops and interrupts.

Figure 16. Clock Control States



6.2.3 Stop-Grant State

When the STPCLK# pin is asserted, the Stop-Grant state of the processor is entered 20 bus clocks after the response phase of the processor-issued Stop Grant Acknowledge special bus cycle.

Since the GTL+ signal pins receive power from the FSB, these pins should not be driven (allowing the level to return to V_{CC}) for minimum power drawn by the termination resistors in this state. In addition, all other input pins on the FSB should be driven to the inactive state.

BINIT# will not be serviced while the processor is in Stop-Grant state. The event will be latched and can be serviced by software upon exit from the Stop-Grant state.

RESET# will cause the processor to immediately initialize itself, but the processor will stay in Stop-Grant state. A transition back to the Normal state will occur with the deassertion of the STPCLK# signal. When re-entering the Stop-Grant state from the Sleep state, STPCLK# should only be deasserted ten or more bus clocks after the de-assertion of SLP#.

A transition to the HALT/Grant Snoop state will occur when the processor detects a snoop on the FSB (see [Section 6.2.4](#)). A transition to the Sleep state (see [Section 6.2.5](#)) will occur with the assertion of the SLP# signal.

While in the Stop-Grant State, SMI#, INIT#, BINIT#, and LINT[1:0] will be latched by the processor, and only serviced when the processor returns to the Normal state. Only one occurrence of each event will be recognized upon return to the Normal state.

While in Stop-Grant state, the processor will process snoops on the FSB and it will latch interrupts delivered on the FSB.

The PBE# signal can be driven when the processor is in Stop-Grant state. PBE# will asserted if there is any pending interrupt latched within the processor. Pending interrupts that are blocked by the EFLAGS.IF bit being clear will still cause assertion of PBE#. Assertion of PBE# indicates to system logic that it should return the processor to the Normal state.

6.2.4 HALT/Grant Snoop State

The processor will respond to snoop or interrupt transactions on the FSB while in Stop-Grant state or in AutoHALT Power Down state. During a snoop or interrupt transaction, the processor enters the HALT/Grant Snoop state. The processor will stay in this state until the snoop on the FSB has been serviced (whether by the processor or another agent on the FSB) or the interrupt has been latched. After the snoop is serviced or the interrupt has been latched, the processor will return to the Stop-Grant state or AutoHALT Power Down state, as appropriate.

6.2.5 Sleep State

The Sleep state is a low-power state in which the processor maintains its context, maintains the phase-locked loop (PLL), and has stopped all internal clocks. The Sleep state can only be entered from Stop-Grant state. Once in the Stop-Grant state, the processor will enter the Sleep state upon the assertion of the SLP# signal. The SLP# pin should only be asserted when the processor is in the Stop Grant state. SLP# assertions while the processor is not in the Stop-Grant state is out of specification and may result in unapproved operation.

Snoop events that occur while in Sleep state or during a transition into or out of Sleep state will cause unpredictable behavior.

In the Sleep state, the processor is incapable of responding to snoop transactions or latching interrupt signals. No transitions or assertions of signals (with the exception of SLP#, DPSLP#, or RESET#) are allowed on the FSB while the processor is in Sleep state. Any transition on an input signal before the processor has returned to Stop-Grant state will result in unpredictable behavior.

If RESET# is driven active while the processor is in the Sleep state, and held active as specified in the RESET# pin specification, then the processor will reset itself, ignoring the transition through Stop-Grant state. If RESET# is driven active while the processor is in the Sleep state, the SLP# and STPCLK# signals should be deasserted immediately after RESET# is asserted to ensure the processor correctly executes the Reset sequence.

While in the Sleep state, the processor is capable of entering an even lower power state, the Deep Sleep state, by asserting the DPSLP# pin. (See [Section 6.2.6](#).) Once in the Sleep or Deep Sleep states, the SLP# pin must be de-asserted if another asynchronous FSB event needs to occur. The SLP# pin has a minimum assertion of one BCLK period.

When the processor is in Sleep state, it will not respond to interrupts or snoop transactions.

6.2.6 Deep Sleep State

Deep Sleep state is a very low power state the processor can enter while maintaining context. Deep Sleep state is entered by asserting the DPSLP# pin. The DPSLP# pin must be deasserted to re-enter the Sleep state. A period of 30 microseconds (to allow for PLL stabilization) must occur before the processor can be considered to be in the Sleep State. Once in the Sleep state, the SLP# pin can be deasserted to re-enter the Stop-Grant state.

The clock may be stopped when the processor is in the Deep Sleep state in order to support the ACPI S1 state. The clock may only be stopped after DPSLP# is asserted and must be restarted before DPSLP# is deasserted. To provide maximum power conservation when stopping the clock during Deep Sleep, hold the BCLK0 input at V_{OL} and the BCLK1 input at V_{OH} .

While in Deep Sleep state, the processor is incapable of responding to snoop transactions or latching interrupt signals. No transitions of signals are allowed on the FSB while the processor is in Deep Sleep state. Any transition on an input signal before the processor has returned to Stop-Grant state will result in unpredictable behavior.

6.2.7 Deeper Sleep State

The Deeper Sleep state is the lowest state power the processor can enter. This state is functionally identical to the Deep Sleep state but at a lower core voltage. The control signals to the voltage regulator to initiate a transition to the Deeper Sleep state are provided on the platform. Please refer the appropriate platform design guidelines listed in [Table 1](#).

6.3 Enhanced Intel SpeedStep Technology

The mobile Intel Pentium 4 processor, when used in conjunction with the requisite Intel SpeedStep technology applet or its equivalent, supports Enhanced Intel SpeedStep technology. Enhanced Intel SpeedStep technology allows the processor to switch between two core frequencies automatically based on CPU demand, without having to reset the processor or change the FSB frequency. The processor has two bus ratios and voltages programmed into it instead of one and the GHI# signal controls which bus ratio and voltage is used. After reset, the processor will start in the lower of its two core frequencies, the Battery Optimized mode. An operating mode transition to the high core frequency can be made by setting GHI# low, putting the processor into the Deep Sleep state, regulating to the new VID output, and returning to the Normal state. This puts the processor into the high core frequency, or Maximum Performance mode. Going through these steps with GHI# set high, transitions the processor back to the low core frequency operating mode. The processor will drive the VID[4:0] pins with the VID of the current operating mode and the system logic is required to regulate the core voltage within specification for the driven VID.

7 Debug Tools Specifications

Please refer to the *ITP700 Debug Port Design Guide* and the appropriate platform design guidelines listed in [Table 1](#) for more detailed information regarding debug tools specifications.

7.1 Logic Analyzer Interface (LAI)

Intel is working with two logic analyzer vendors to provide logic analyzer interfaces (LAIs) for use in debugging mobile Intel Pentium 4 processor systems. Tektronix* and Agilent* should be contacted to get specific information about their logic analyzer interfaces. The following information is general in nature. Specific information must be obtained from the logic analyzer vendor.

Due to the complexity of mobile Intel Pentium 4 processor systems, the LAI is critical in providing the ability to probe and capture FSB signals. There are two sets of considerations to keep in mind when designing a mobile Intel Pentium 4 processor system that can make use of an LAI: mechanical and electrical.

7.1.1 Mechanical Considerations

The LAI is installed between the processor socket and the mobile Intel Pentium 4 processor. The LAI pins plug into the socket, while the mobile Intel Pentium 4 processor pins plug into a socket on the LAI. Cabling that is part of the LAI egresses the system to allow an electrical connection between the mobile Intel Pentium 4 processor and a logic analyzer. The maximum volume occupied by the LAI, known as the keepout volume, as well as the cable egress restrictions, should be obtained from the logic analyzer vendor. System designers must make sure that the keepout volume remains unobstructed inside the system. Note that it is possible that the keepout volume reserved for the LAI may differ from the space normally occupied by the mobile Intel Pentium 4 processor with 533 MHz FSB heatsink. If this is the case, the logic analyzer vendor will provide a cooling solution as part of the LAI.

7.1.2 Electrical Considerations

The LAI will also affect the electrical performance of the FSB; therefore, it is critical to obtain electrical load models from each of the logic analyzer vendors to be able to run system level simulations to prove that their tool will work in the system. Contact the logic analyzer vendor for electrical specifications and load models for the LAI solution they provide.