82562EP Design Checklist v1.0

Project Name	
Fab Revision	
Date	
Designer	
Intel Contact	
Reviewer	

SECTION	CHECK ITEMS	REMARKS	√ DONE	COMMENTS
General	Have up-to-date product documentation and spec updates	Documents are subject to frequent change		
	Observe instructions for special pins needing pull-up or pull-down resistors	Do not connect pull-up or pull-down resistors to any pins marked No Connect.		
82562EP LCI Device Option	Connect LCI signals to corresponding signals on ICH device.			
	Each of the four control pins TESTEN, ISOL_TCK, ISOL_TI, and ISOL_EXEC should be connected to a LAN disable circuit through 100 Ω resistors.	Contact Intel for latest LAN disable circuit recommendations. If the LOM disable function is not used, connect Ball E8 to ground through a 3.3 K resistor.		
	Use a 93C46 EEPROM. **Note:** DO NOT use a Catalyst 93C46 Revision H.	EEPROM for 82562EP attaches to ICH. Add decoupling capacitor. EEPROMs should be rated for at least 1 MHz.		
	Connect Ball F2 RBIAS10 to ground through a 619 Ω 1% resistor.	Recommended starting value. Measure PCB's output amplitude and adjust as required to meet IEEE specification.		
	Connect Ball F1 RBIAS100 to ground through a 649 Ω 1% resistor.	Recommended starting value. Measure PCB's output amplitude and adjust as required to meet IEEE specification.		
Clock Source	Use 25 MHz 30 ppm accuracy crystal.	Parallel resonant crystals are preferred.		
	Connect two 27 pF load caps to crystal.	Capacitance affects accuracy of the frequency. Must be matched to crystal specs, including estimated trace capacitance in calculation. Use low ESR caps.		
EEPROM and FLASH Memory	Use decoupling capacitor.	Applies to EEPROM or FLASH devices.		

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	EEPROM ORG ties to 3.3 V for x16 access.	For Microwire EEPROMs. Depends on EEPROM used.		
Transmit and Receive Differential Pairs	82562EP controllers use pairs of 54.9 Ω termination resistors.	Apply to both differential pairs.		
Magnetics Module (10/100 Base-T Applications)	Integrated magnetics modules/RJ-45 connectors are available to minimize space requirements.	Modules with pin compatibility from 10/100 to Gigabit are available, containing internal jumpers for the unused pairs. Multivendor pin compatibility is possible. Contact manufacturers.		
	Qualify magnetics module carefully for Return Loss, Insertion Loss, Open Circuit Inductance, Common Mode Rejection, and Crosstalk Isolation	Magnetics module is critical to passing IEEE PHY conformance tests and EMI test.		
	Use 5-core model.	Autotransformer models (10/100) provide better cable termination.		
	For 82562EP devices that do not support MDI-X, use 0.1 μF capacitor on receive center tap.	Improves bit error rate.		
Discrete Magnetics Module/RJ-45 Connector Option (10/100 Base-T applications)	Bob Smith termination: use 4 x 75 Ω resistors for cable-side center taps and unused pins.	Terminates pair-to-pair common mode impedance of the CAT5 cable.		
	Bob Smith termination: use an EFT capacitor attached to the termination plane. Suggested values are 1500 pF/2KV or 1000 pF/3KV	Maintain greater than 25 mil spacing from capacitor to traces and components.		
	Connect signal pairs correctly to RJ-45 connector.	The differential pairs use pins 1-2 (Transmit in 10/100) and 3-6 (Receive in 10/100). Take care not to reverse the polarity.		
Power Supply and Signal Ground	For the 82562EP device, provide a 3.3 V supply.	The 82562EP component is a single-voltage device.		
	Design with power supplies that start up properly.	A good guideline is that all voltages should ramp to within their control bands in 20 ms. or less. It is desirable that voltages ramp in sequence and that the voltage rise be monotonic.		
	Ensure that there is adequate capacitance on the PNPs.	Please check the reference schematic.		
	Use auxiliary power supplies.	Auxiliary power is necessary to support wake up from powerdown states.		

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	Use decoupling and bulk capacitors generously.	Add approximately 20-30 µF of bulk capacitance per voltage rail, typically using 10 µF capacitors. If power is distributed on traces, bulk capacitors should be used at both ends. If power is distributed on cards, bulk capacitors should be used at the connector.		
Chassis Ground (10/100 Base-T applications)	If possible, provide a separate chassis ground to connect the shroud of the RJ-45 connector and to terminate the line side of the magnetics module.	This design improves EMI behavior.		
	Place pads for approximately four "stitching" capacitors to bridge the gap from chassis ground to signal ground.	Typical values range from 0.1µF to 4.7µF. Determine experimentally.		
Termination Plane	For designs with non-integrated magnetics modules, lay out Bob Smith termination plane. Term plane floats over chassis ground.	Splits in ground plane should be at least 50 mils to prevent arcing during hi-pot tests.		
LED Circuits	Basic recommendation is a single green LED for Activity and a dual (bi-color) LED for Speed. Many other configurations are possible.	Two LED configuration is compatible with integrated magnetics modules. For the Link/Activity LED, connect the anode to the ACTLED# pin (Ball A7) and the cathode to the LILED# pin (Ball D8). For the bi-color speed LED pair, have the SPDLED# signal drive one end. The other end should be connected to 3.3 V.		
	Connect LEDs to 3.3V as indicated in reference schematics.	Use 3.3V AUX for designs supporting wakeup. Consider adding 1-2 filtering capacitors per LED for extremely noisy situations. Suggested starting value 470 pF.		
	Connect LEDs to 3.3 V as indicated in reference schematics.	Use 3.3 V AUX for designs supporting wakeup. Consider adding filtering capacitors for extremely noisy situations. Suggested starting value 470 pF.		
	Add current limiting resistors to LED paths.	Typical current limiting resistors are 250 to 330 Ω when using a 3.3V supply. Current limiting resistors are typically included with integrated magnetics modules.		

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