82541ER/PI Schematic Checklist (Version 2.0)

Project Name	
Fab Revision	
Date	
Designer	
Intel Contact	
Reviewer	

SECTION	CHECK ITEMS	REMARKS	DONE	COMMENTS
	Completed by:	Design Engineer Name:		
General	Obtain the most recent documentation and specification updates.	Documents are subject to frequent change.		
	Observe instructions for special pins needing pull-up or pull-down resistors.	Do not connect pull-up or pull-down pins marked "No Connect".		

SECTION	CHECK ITEMS	REMARKS	DONE	COMMENTS
Support Pins	Connect 32-bit PCI interface pins to the corresponding pins on the system.			
	Connect Ball A9 LAN_PWR_GOOD to RSM_RST# or other voltage supervisor circuit.	Input should remain low until all power supplies are stable and for approximately 80 ms. LAN_PWR_GOOD works like an auxiliary chip reset. It should be a clean, glitch-free signal. It is not intended for use as a LAN Disable. LAN_PWR_GOOD must be asserted during power down states to allow wakeup.		
	For the 82541PI, connect ball A6 PME# to system for wake up signaling.	Typical connection is PME# on ICHx.		
	Connect Ball J12 AUX_PWR signals correctly.	AUX_PWR is a logic input denoting that auxiliary power is connected to the device. AUX_PWR = 1b is a requirement for wake up.		
	Connect Ball B9 RST# to RST# on system.			

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Support Pins	Connect a 0.01 µF capacitor between Ball C2 M66EN and ground. M66EN should have a pullup resistor somewhere in the system.	Capacitor per spec for signal integrity. This signal may be grounded anywhere on the segment for any PCI device incapable of 66 MHz operation.		
	Connect Ball G2 VIO to 5 Vdc Standby or 3.3 Vdc Standby to match PCI signaling voltage.	Use a 100 KΩ resistor as a current limiter and a 0.1 µF bypass capacitor.		
	Ball H4 and G4 are connected to PLL_1.2 V.	Place appropriate stuffing options for each controller.		
	If a LAN disable function is required, drive Ball P9 FLSH_SO/ LAN_ DISABLE#.	Use a GPIO pin.		

SECTION	CHECK ITEMS	REMARKS	DONE	COMMENTS
Support Pins	Use a 93C46 EEPROM. **Note:** DO NOT use a Catalyst 93C46 Revision H.	For Microwire* EEPROMs, install a 100 Ω pull-down resistor on Ball J4 EEMODE. Do not install a pull-down resistor on the EEDO pin. For SPI EEPROMs, use a 3.3 K Ω pull-up resistor on write protect (WP#) and a 3.3 KΩ pull-up resistor on HOLD#. Microwire EEPROMs should be rated for at least 1 MHz and SPI EEPROMs should be rated for at least 2 MHz.		

SECTION	CHECK ITEMS	REMARKS	DONE	COMMENTS
Support Pins	For the 82541PI, use a 93C46 EEPROM for non-alerting applications, an AT25040 for ASF 1.0, or an AT25080 for ASF 2.0. Note: DO NOT use a Catalyst 93C46 Revision H.	For Microwire* EEPROMs, install a 100 Ω pull-down resistor on Ball J4 EEMODE. Do not install a pulldown resistor on the EEDO pin. For SPI EEPROMs, install a 1 KΩ pull-up resistor on ball J4 EEMODE, use a 3.3 KΩ pull-up resistor on write protect (WP#) and a 3.3 KΩ pull-up resistor on HOLD#. Microwire EEPROMs should be rated for at least 1 MHz and SPI EEPROMs should be rated for at least 2 MHz.		
	For the 82541PI, check reference schematic for connection of Software Defined Pins (SDPs).	Intel driver software might expect t use SDPs for special functions.		
	Connect Balls C9, A10, B10 to VCC.	1 K Ω pull-up resistors are reasonable values.		
	Provide a location for through-hole 2-pin header for IEEE PHY conformance testing. Depopulate the header for production.	This equates to a header between Balls B14 and D14 (differential clock output).		

SECTION	CHECK ITEMS	REMARKS	DONE	COMMENTS
Support Pins	Bring out Ball B14's (IEEE_TEST+) and Ball D14's (IEEE_TEST-) traces as a differential pair and place a resistor pad between traces, but do not populate a resistor.	This facilitates IEEE testing.		
Clock Source (Crystal Option)	Use a 25 MHz 30 ppm accuracy @ 25 °C crystal. Avoid components that introduce jitter.	Parallel resonant crystals are preferred.		
	Connect two 22 pF load capacitors to the crystal.	Capacitance affects accuracy of the frequency. Must be matched to crystal specifications, including estimated trace capacitance in calculation. Use low ESR capacitors.		
EEPROM and Flash Memory	Use a decoupling capacitor.	Applies to both EEPROM or Flash devices.		
	EEPROM ORG ties to 3.3 Vdc for x16 access.	For Microwire EEPROMs. Depends on the EEPROM used.		
	Consider whether or not to use Flash memory.	Most LOM systems with boot ROM places the image in the system Flash.		
	If Flash memory is used, select the appropriate device.	The 82541ER/PI uses a serial Flash.		

SECTION	CHECK ITEMS	REMARKS	DONE	COMMENTS
Transmit and Receive Differential Pairs	The 82541ER/PI uses pairs of 49.9 Ω termination resistors with 0.1 µF capacitors attached between center nodes and ground.	Apply to all four differential pairs.		
Magnetics Module (10/100/1000 BASE-T Applications)	Integrated magnetics modules/RJ-45 connectors are available to minimize space requirements.	Modules with pin compatibility from 10/100 to Gigabit are available, containing internal jumpers for the unused pairs. Multivendor pin compatibility is possible. Contact manufacturers.		
	Qualify magnetics module carefully for Return Loss, Insertion Loss, Open Circuit Inductance, Common Mode Rejection, and Crosstalk Isolation.	Magnetics module is critical to passing IEEE PHY conformance tests and EMI test.		
	The 82541ER/PI controller uses a 12-core model.	Auto-transformer models (10/100) provide better cable termination. All Gigabit models contain auto-transformers.		

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Magnetics Module (10/100/1000 BASE-T Applications)	Supply 1.8 Vdc to the transformer center taps and use 0.1 µF bypass capacitors.	These voltages bias the controller's output buffers. Magnetics with four center tap pins may have better characteristics than those with 1-2 center tap pins. Use capacitors with low Equivalent Series Resistance (ESR).		
	If possible, provide a separate chassis ground to connect the shroud of the RJ-45 connector and to terminate the line side of the magnetic module.	This design improves EMI behavior. Also, if using integrated magnetics with USB, do not isolate ground for RJ45.		
Discrete Magnetics Module/RJ-45 Connector Option (10/100/1000 BASE-T Applications)	Bob Smith termination: use 4 x 75 Ω resistors for cable-side center taps and unused pins.	Terminates pair-to-pair common mode impedance of the CAT5 cable.		
	Bob Smith termination: use an EFT capacitor attached to the termination plane. Suggested values are 1500 pF/2KV or 1000 pF/3KV.	Maintain greater than 25 mil spacing from capacitor to traces and components.		

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Discrete Magnetics Module/RJ-45 Connector Option (10/100/1000 BASE-T Applications)	Connect signal pairs correcly to the RJ-45 connector.	The differential pairs use pins 1-2 (Transmit in 10/100), 3-6 (Receive in 10/100), 4-5 (Gigabit only), and 7-8 (Gigabit only). Take care not to reverse the polarity.		
Power Supply and Signal Ground	Connect external PNP transistors to the regulator control CTRL12 and CTRL18 outputs to supply 1.2 Vdc and 1.8 Vdc, respectively. The connections and transistor parameters are critical.	Alternatively, provide external regulators to generate these voltages. If the internal voltage regulator control circuit is not used, the CTRL pins may be left unconnected.		
	For the 82541PI, consider using two 0.5 Ω resistors in parallel to the emitter path of the 1.2 Vdc power supply PNP transistor for regulator power dissipation.			
	Provide a 3.3 Vdc supply.			
	Design with power supplies that start up properly.	A good guideline is that all voltages should ramp to within their control bands in 20 ms. or less. It is desirable that voltages ramp in sequence and that the voltage rise be monotonic.		

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Power Supply and Signal Ground	Make sure that there is adequate capacitance on the PNPs.	Refer to the reference schematic for more details.		
	Use auxiliary power supplies.	Auxiliary power is necessary to support wake up from power down states.		
	Use decoupling and bulk capacitors gererously.	Use approximately 12 bypass capacitors. Add approximately 20-30 µF of bulk capacitance per voltage rail, typically using 10 µF capacitors. If power is distributed on traces, bulk capacitors should be used at both ends. If power is distributed on cards, bulk capacitors should be used at the connector.		
Chassis Ground (10/100/1000 BASE-T Applications)	If possible, provide a separate chassis ground to connect the shroud of the RJ-45 connector and to terminate the line side of the magnetics module.	This design improves EMI behavior.		
	Place pads for approximately four "stitching" capacitors to bridge the gap from chassis ground to signal ground.	Typical values range from 0.1 µF to 4.7 µF. Determine experimentally.		

SECTION	CHECK ITEMS	REMARKS	DONE	COMMENTS
Termination Plane	For designs with non-integrated magnetics modules, lay out Bob Smith termination plane. Term plane floats over chassis ground.	Splits in ground plane should be at least 50 mils to prevent arcing during hi-pot tests.		
LED Circuits	Basic recommendation is a single green LED for Activity and a dual (bi-color) LED for Speed. Many other configurations are possible. LEDs are configurable through the EEPROM.	A two-LED configuration is compatible with integrated magnetics modules. For the Link/Activity LED, connect the anode to the ACTIVITY# pin (Ball C11) and the cathode to the LINK_UP# pin (Ball A12). For the bi-color speed LED pair, have the Link 100# signal drive one end. The other end should be connected to LINK1000#.		
	Connect LEDs to 3.3 Vdc as indicated in reference schematics.	Use 3.3 V AUX for designs supporting wakeup. Consider adding 1-2 filtering capacitors per LED for extremely noisy situations. Suggested starting value 470 pF.		
	Add current limiting resistors to LED paths.	Typical current limiting resistors are 250 to 330 Ω (300 to 330 Ω for the 82541PI) when using a 3.3 Vdc supply. Current limiting resistors are typically included with integrated magnetics modules.		

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Mfg Test	The 82541ER uses a JTAG Test Access Port.	Place 100 Ω pull-down resistors on Ball L13 JTAG_TRST# and Ball L14 JTAG_TCK. These connections hold the TAP controller in an inactive state.		

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General	Obtain the most recent documentation and specification updates.	Documents are subject to frequent change.		
	Route the transmit and receive differential traces before routing the digital traces.	Layout of differential traces is critical.		
Placement of the Controller	Place the Ethernet controller at least one inch from the edge of the board (two inches is preferred) and at least one inch from any integrated magnetics module.	With closer spacing, fields can follow the surface of the magnetics module or wrap past edge of the board. As a result, EMI might increase. Optimum location is approximately one inch behind the magnetics module.		
Clock Source	Place the crystal less than 0.75 inches from the 82577.	This reduces EMI. The Ethernet clock plays a key role in EMI.		
EEPROM and Flash Memory	Placement is not critical due to slow signal speeds.	Acceptable to place a few inches away from the Ethernet controller to provide better spacing of critical components.		
Transmit and Receive Differential Pairs	Design traces 100 Ω differential impedance.	Primary requirement for 10/100/1000 Mb/s Ethernet. Paired 49.9 Ω traces do not make 100 Ω differential. Check impedance calculator.		
	Use short traces.	Keep trace length under four inches from the Ethernet controller through the magnetics to the RJ-45 connector.		

SECTION	CHECK ITEMS	REMARKS	DONE	COMMENTS
Transmit and Receive Differential Pairs	Avoid highly resistive traces, for example, four mil traces longer than four inches.	If trace length is a problem, use thicker board dielectrics to allow wider traces. Thicker copper is even better than wider traces.		
	Make traces symmetrical.	Try to match the pairs at pads, vias and turns. Establish rules carefully for the autorouter. Asymmetry contributes to impedance mismatch.		
	Do not make 90° bends.	Bevel corners with turns based on 45° angles.		
	Avoid through holes (vias).	If using through holes (vias), the budget is two per trace.		
	Keep traces close together within differential pairs.	Keep within 30 mils regardless of trace geometry.		
	Keep trace-to-trace length difference within each pair to less than 50 mils.	Minimizes signal skew and common mode noise. Improves long cable performance.		
	Keep differential pairs 100 mils or more away from each other and away from parallel digital traces.	Minimizes crosstalk and noise injection. 300 mil spacing is better. Guard traces are generally not recommended and will reduce the impedance if done incorrectly.		
	Keep traces away from the board edge.	Controls EMI.		
	Avoid unused pads and stubs along the traces.			
	Route traces on layers on appropriate layers.	Run pairs on different layers as needed to improve routing. Use layers adjacent to ground or power layers if possible. Make sure digital signals on adjacent layers cross at 90 degree angles.		
	Place termination resistors (and capacitors if applicable) close to Ethernet controller.	Prevents reflections. Use symmetrical pads.		
Magnetics Module	Capacitors connected to center taps should be placed very close to the magnetics module.	This improves BER.		

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Power Supply and Ground	When using the internal regulator control circuits of the Ethernet controller with external PNP transistors, keep the distance from the CTRL12/CTRL15/ CTRL18 output balls to the transistors very short (less than 1 inch) and use 25 mil (minimum) wide traces.	Reduces oscillation and ripple in the power supply.		
	Use of power planes is essential for optimized performance of the Ethernet controller.	Narrow finger-like planes and very wide traces are not recommended and a continuous plane should be used.		
	Use decoupling and bulk capacitors generously.	Place decoupling and bulk capacitors close to Ethernet controller, with some along every side, using short, wide traces and large vias. If power is distributed on traces, bulk capacitors should be used at both ends. If power is distributed on cards, bulk capacitors should be used at the connector.		
	If using decoupling capacitors on LED lines, place them carefully.	Capacitors on LED lines should be placed near the LEDs.		
	Use a wide ground plane under the area covering the Ethernet controller, the external transistors (for both 1.2 Vdc and 1.8 Vdc generation) and the filter capacitors.			
	Bypass the emitter and collector of the external PNP transistors as closely as possible to the body of the transistors.			
	The bypass capacitor at the emitter should be at least 4.7 µF (preferably 10 to 20 µF).	Ceramic X5R or X7R type capacitors should be placed as closely as possible to the body of the transistors.		
	The larger capacitors should be concentrated near the transistor.	Do not disperse the large capacitors in a large area as this can cause instability to the circuit.		

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Power Supply and Ground	The high frequency bypass capacitors (0.1 µF X7R capacitors) for the Ethernet controller should be placed as closely as possible to the corresponding balls.			
	Trace lengths should have around eight mils of width.			
Chassis Ground	If possible, provide a separate chassis ground "island" to ground the shroud of the RJ-45 connector and to terminate the line side of the magnetics module. This design improves EMI behavior.	Split in ground plane should be at least 50 mils. Split should run under center of magnetics module. Differential pairs never cross the split.		
	Place four to six pairs of pads for "stitching" capacitors to bridge the gap from chassis ground to signal ground.	Determine exact number and values empirically based on EMI performance. Expect to populate approximately two capacitor sites.		
Termination Plane	For designs with non-integrated magnetics modules, lay out Bob Smith termination plane. Term plane floats over chassis ground.	Splits in ground plane should be at least 50 mils.		
LED Circuits	Keep LED traces away from sources of noise, for example, high speed digital traces running in parallel.	LED traces can carry noise into integrated magnetics modules, RJ-45 connectors, or out to the edge of the board, increasing EMI.		

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