Intel® Socket Test Technology

for the LGA775 Socket

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Revision History

Revision Number	Description	Revision Date
-001	Initial Release.	October 2004
-002	Corrected Figures 2 and 3 Remove duplicate information in tables 1 and 3	November 2004

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1 Introduction

The Intel® Socket Test Technology for the LGA775 socket is a test chip that enables testing for the mechanical integrity and electrical continuity of both socket-to-board solder ball connectivity and socket-to-CPU contact connectivity. Once inserted into the board's LGA775 socket, the test chip works with either in-circuit testers (ICT) or manufacturing defect analyzers (MDA) that have access to all the socket nets through test fixture probes.

An ICT uses digital test vectors which execute very quickly when power is applied to the board—typically less than a couple of milliseconds depending upon test head capability. An MDA doesn't power the board, but uses its analog measurement capability. Test time using an MDA is typically longer.

Figure 1 - Intel® Socket Test Technology for the LGA775 Socket—Test Chip

1.1 Terminology

Term	Description
ICT	In-circuit Test
LGA775 socket	The surface mount socket designed to accept the Intel® Pentium® 4 processor in the 775-Land LGA package
MDA	Manufacturing Defect Analyzer
VCCP	Processor core voltage
VTT	I/O termination voltage for the front side bus

1.2 Reference Documents

Document	Document Location
Intel® Pentium® 4 Processor Extreme Edition on 0.13 Micron Process in the 775-Land Package Datasheet	http://www.intel.com/design/Pentium4/datashts/302350.htm
Intel® Pentium® 4 Processor 560, 550, 540, 530 and 520Δ Datasheet on 90 nm Process in the 775-Land LGA Package Supporting Hyper-Threading Technology[1]	http://www.intel.com/design/pentium4/datashts/302351.htm
Voltage Regulator-Down (VRD) 10.1 Design Guide for Desktop LGA775 Socket	http://www.intel.com/design/Pentium4/guides/302356.htm

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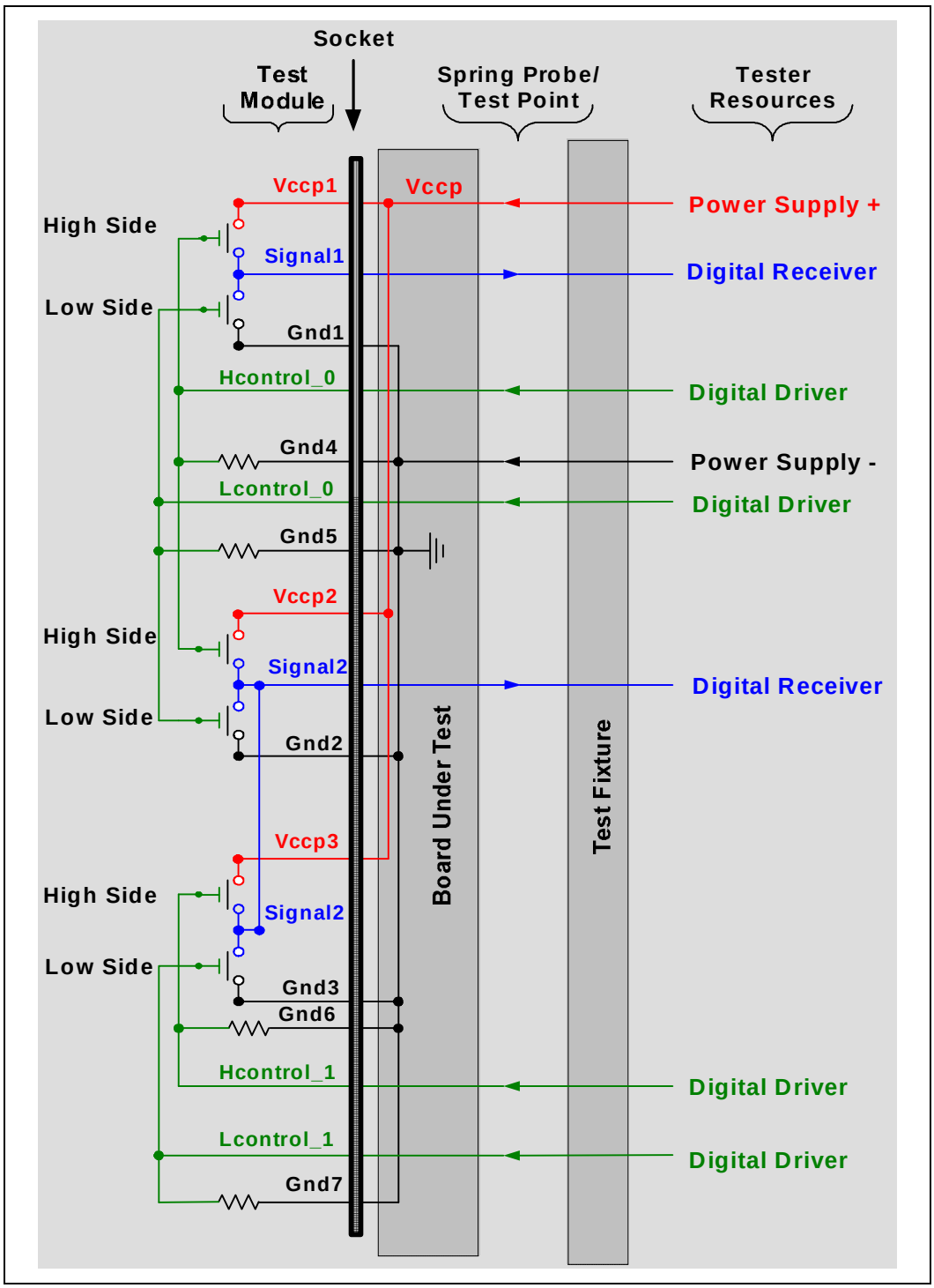
2 Theory

The Intel® Socket Test Technology LGA775 socket test chip consists of an array of switch pairs. Each switch pair, together with a control signal, can be used to test one signal, one power, and one ground. The control signal enables the **ON**/**OFF** condition of each switch. Testing is accomplished by checking the **ON** and **OFF** condition of each switch. There are fewer signals than power and ground electrical socket connections. To compensate there are four pairs of Hcontrol and Lcontrol signals that allow the multiplexing of signals between power and ground electrical socket connections. Signal multiplexing provides testing for as many power and grounds as possible. Testing of resistors that are also on the test chip help to provide some additional open coverage not provided by the switch pairs.

The control signals are pulled to ground with a resistor to keep the switches in an **OFF** state when a powered test method is being used on an ICT.

Figure 2 - Intel® Socket Test Technology for the LGA775 Socket—Block Diagram



3 Powered Testing With Digital Vectors (ICT)

3.1 Using Voltage Identifier (VID) Signals

VCCP and VTT are used to power the test chip. The test chip does not provide control on the VID signals to establish a VCCP voltage when plugged into a socket. A VID signal combination should be connected to ground and controlled by the test equipment in such a way that an on-board VCCP is generated that equals the on-board VTT voltage.

To determine which VID lines to use in order to keep VCCP equal to VTT, refer to the Voltage Regulator Down (VRD) Design Guide for the processor being used. Design Guides are available from the Intel® Developer web site at http://www.intel.com/design/Pentium4/documentation.htm.

Table 1 - Voltage Identifier Signals

Signal Name	VID Ball
VID_0	AM2
VID_1	AL5
VID_2	AM3
VID_3	AL6
VID_4	AK4
VID_5	AL4

3.2 Using Control Signals

To ensure that the switches default to **OFF** when power is applied or while other devices are being tested, the control signals are pulled to ground with 1KΩ resistors. Each control signal can turn a grouping of approximately 64 switches **ON** and **OFF**.

Each **ON**/**OFF** switch pair tests three socket solder balls and socket contacts, not including the control signals. A logic level high on the control signal will turn its associated switch to the **ON** state.

Four pairs of Hcontrol and Lcontrol inputs are used to multiplex the signals that are received by the test equipment across more than one switch pair in order to test the majority of power and ground electrical socket connections.

Caution: At no time should the control signal for the *High Side* and *Low Side* switches be driven high at the same time, as occurs with some automated fault injection tools. A direct short

from power to ground would result and possibly damage the Intel® Socket Test Technology test chip and the board under test. To prevent damage, drive only one control signal high at any time during the test while all others are low.

The High Side switch of each switch pair is used to test a VCCP solder ball and contact along with the shared signal solder ball and contact of the High and Low Side switch pair. The control line for the High Side switch is driven to a logic high, thus turning the switch **ON** and enabling an electrical connection between VCCP and the shared signal. When this happens, a logic high should be received on the shared signal. At the same time, the Low Side switch control signal will be at a logic low.

The Low Side switch of each switch pair is used to test a GND solder ball and contact along with the shared signal solder ball and contact of the High and Low Side switch pair. The control line for the Low Side switch is driven to a logic high, thus turning the switch **ON** and enabling an electrical connection between GND and the shared signal. A logic low should be received on the shared signal. At the same time, the High Side switch control signal will be at a logic low.

One shared signal is used to test one VCCP and one GND connection. The lack of the high/low signal transition would indicate an open on either the shared signal or the power/ground connection used by that switch pair.

Figure 2 shows that **Signal1**, **Vccp1**, and **Gnd1** as well as **Signal2**, **Vccp2**, and **Gnd2** can be verified through **Hcontrol_0** and **Lcontrol_0**.

Table 2 - Control Signals

Signal Name	Signal Ball
Hcontrol_0	U2
Lcontrol_0	J16
Hcontrol_1	U3
Lcontrol_1	H15
Hcontrol_2	E7
Lcontrol_2	H16
Hcontrol_3	F6
Lcontrol_3	J17

As with all powered digital in-circuit testing, all other active components on the board that are connected to the socket should be placed in a tri-state mode before testing with this technique.

3.3 Using Test Head Loads

Test head loads (pull-ups/pull-downs) improve the detection of opens. With the switch pair **OFF**, the signals would be pulled to a logic level low if test head pull-downs are used and a logic level high if test head pull-ups are used. Using pull-ups with the Low Side switch **ON** would receive a logic level high on the signal if the signal or GND connection were open and a logic level low if they were not open. Using pull-downs with the High Side switch **ON** would receive a logic level low on the signal if the signal or VCCP ball were open and a logic level high if they were not open. Note: On-board pull-up/down resistors must be taken into consideration when test head loads are used.

Table 3. Sample Table

Low Side Control	High Side Control	Signal	Test Head Load
0	0	0	Pull-Down
0	0	1	Pull-Up
1	0	0	Pull-Up
0	1	1	Pull-Down
1	1		N/A

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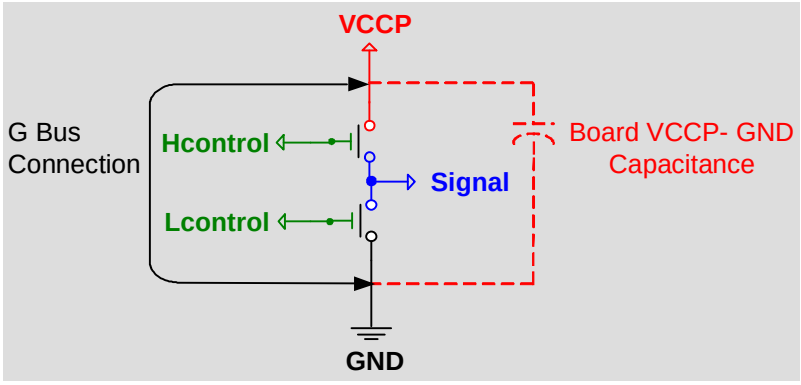
4 Un-Powered Testing (MDA)

The following test method was developed using an Agilent* 3070 Series II In-circuit tester in an un-powered mode. The technique and results should be similar when using test equipment with similar capabilities as described below. (Please note that Agilent was formerly known as Hewlett Packard* –HP).

Bus	Description
S Bus	Primary Source. Provides -10.0V to +10.0V (VDC) by connecting the high side to the Device under Test (DUT) through a 500 ohm series resistance. The low side connects itself automatically to digital and switched analog GND.
A Bus	Auxiliary Source. Provides -10.0V to +10.0V (VDC) by connecting the high side to the DUT and the low side automatically to digital and switched analog GND.
I Bus	The high side of a DC voltmeter connected to the DUT.
L Bus	The low side of a DC voltmeter connected to digital and switched analog GND unless otherwise specified through software.
G Bus	Guard Bus. Used to break parallel impedance paths. In this case, it connects VCCP and GND to keep them at the same potential.

The typical Intel® Socket Test Technology switch pair is shown in Figure 2 using the G Bus to short circuit VCCP to GND and potentially eliminates the charge/discharge time caused by the large capacitance present on the board when testing the High Side switch. The intent is to make the over all test as fast and reliable as possible.

Figure 3 - Typical Switch Pair Configuration



Each switch is tested by connecting the A Bus to the Hcontrol or Lcontrol, the S and I Buses to the Signal, and the L Bus to GND. The A Bus is set to 1.2V to ensure a positive turn on of the switch. The S Bus is set to 600mV for the High and Low Side switch. The S Bus uses a 500 ohm series resistance for both the High and Low Side switch.

The resistance of the switch is equal to approximately 40 ohms in the **ON** state and is infinite in the **OFF** state. In an isolated environment, the **ON** state voltage measured at the signal would be approximately 44mV as a voltage divider exists between the 40 ohm switch resistance and the 500 ohm resistance of the source termination.

It has been observed that the **OFF** state voltage doesn't reach the 600mV level that circuit theory would lead one to expect. This is due to the influence of other on-board devices that cause the level to settle at approximately 250mV.

Figure 4 - Instrument Setup For Low Side Switch

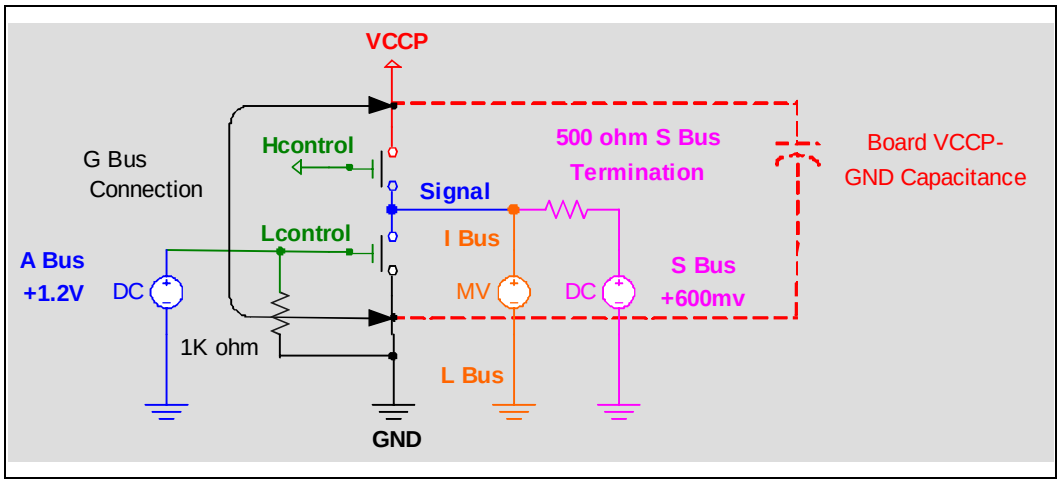
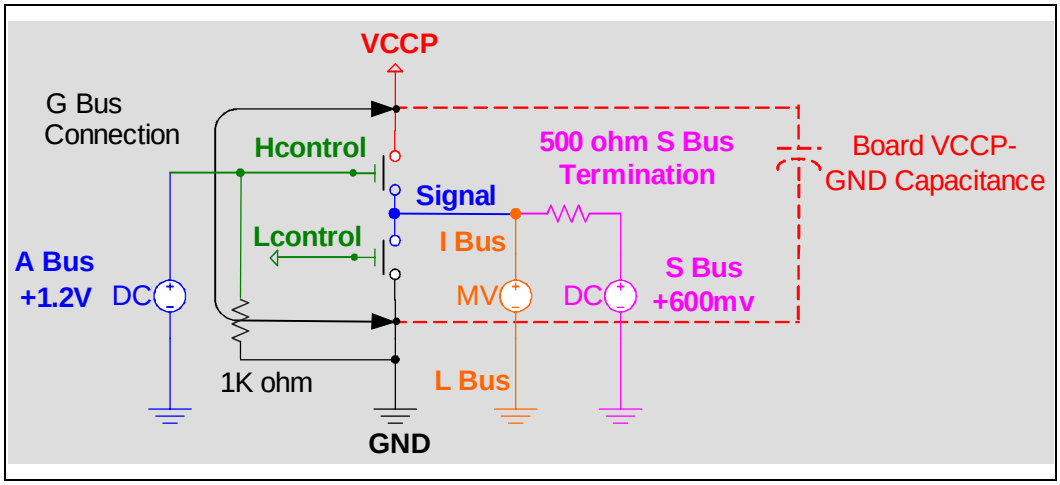


Figure 5 - Instrument Setup For High Side Switch



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5 Related Specifications

Operating temperature: Between 10° C and 50° C

Electrostatic Discharge (ESD) Environment: Controlled to less than 300 volts

Table 4 - Electrical Operating Parameters

Symbol	Parameter	Value	Units
Vccp	Applied Voltage(Powered)	0.8 to 1.2 max	V
CtrlOnThres	Switch On Threshold	300	mv
HctrlEnVih	High Switch Enable VIH(Powered)	Vccp + 0.3 max	V
LctrlEnVih	Low Switch Enable VIH(Powered)	Vccp to Vccp + 0.3 max	V
CtrlDisVil	Switch Disable VIL	0.0	V
CtrlEnVih	Switch Enable Voltage(Un-powered)	1.2 max	V
Sd(on)	Switch Control On To Signal Out Delay(Powered)	20	us
Sd(off)	Switch Control Off To Signal Out Delay(Powered)	20	us
Rval	Resistor Values(Un-Powered)	1K(+-5%)	ohm
Hid(on)	High Switch On Saturation Current	20	ma
Lid(on)	High Switch On Saturation Current	26	ma

Table 5 - Test Condition for High Side Switch (Powered Digital)

Symbol	Parameter	Value	Units
Vccp	Applied Voltage	1.2 max	V
Hcontrol	Enable High Side Switch	1.5 max	V
Lcontrol	Disable Low Side Switch	0.0	V
Signal	Minimum VOH	600	mv
Signal Load	Current Source from Signal to Ground(Pull Down)	5	ma
Signal VohTh	Test VOH Threshold Setting	400	mv
Signal VolTh	Test VOL Threshold Setting	400	mv

Table 6 - Test Condition for Low Side Switch (Powered Digital)

Symbol	Parameter	Value	Units
Vccp	Applied Voltage	1.2 max	V
Hcontrol	Enable High Side Switch	0.0	V
Lcontrol	Disable Low Side Switch	1.2 max	V
Signal	Maximum VOL	200	mv
Signal Load	Current Source from Signal to Vccp(Pull Up)	2	ma
Signal VohTh	Test VOH Threshold Setting	400	mv
Signal VolTh	Test VOL Threshold Setting	400	mv

Table 7 - Test Condition for Switch (Un-powered Analog)

Symbol	Parameter	Value	Units
VccpToGnd	Vccp Connected To Gnd	0.0	V
HctrlEn	Enable High Side Switch	1.2 max	V
HctrlDis	Disable High Side Switch	0.0	V
LctrlEn	Enable Low Side Switch	1.2 max	V
LctrlDis	Disable Low Side Switch	0.0	V
SigSrcVolt	Signal Applied Source Voltage	600 max	mv
SigSrcVR	Signal Applied Source Voltage Resistance	500	ohm

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6 Ball Usage

Table 8 identifies the balls used for the 8 control lines, also referred to as Lcontrol_0 – Lcontrol_3 and Hcontrol_0 – Hcontrol_3.

Table 8 - Balls Used as Control Signals

Low Side Control (Lcontrol)	High Side Control (Hcontrol)
J16	U2
H15	U3
H16	E7
J17	F6

Table 9 maps the ball of the *High* and *Low Side* controls with the signal ball, ground ball and power ball for each switch pair. The table can be used to generate tests and diagnose test failures.

Table 9 - Ball Groupings/Functions

Low Side Control	High Side Control	Signal	GND	VCCP
J16	U2	G16	H27	T27
J16	U2	G17	L30	T28
J16	U2	F15	AE24	T29
J16	U2	G15	H26	T26
J16	U2	G14	H24	T24
J16	U2	F17	H25	T23
J16	U2	E15	AF30	T30
J16	U2	F14	H23	U30
J16	U2	G18	H21	U29
J16	U2	E16	H22	U28
J16	U2	E18	AF29	N23
J16	U2	F18	H19	N24
J16	U2	E13	E28	U27
J16	U2	G13	H20	N25
J16	U2	D17	AF28	N26

Low Side Control	High Side Control	Signal	GND	VCCP
J16	U2	D13	E29	N27
J16	U2	E19	D24	N29
J16	U2	G19	E26	N28
J16	U2	E12	AF27	M23
J16	U2	D19	E25	N30
J16	U2	G12	A24	M25
J16	U2	F12	C24	M24
J16	U2	F11	AF26	M27
J16	U2	G11	B24	M26
J16	U2	G20	D21	M29
J16	U2	D11	F22	M28
J16	U2	D20	E20	K23
J16	U2	F20	A21	M30
J16	U2	E10	AF25	K25
J16	U2	C20	B20	K24
J16	U2	F21	C19	K27
J16	U2	D10	F19	K26
J16	U2	G22	AJ30	K29
J16	U2	G21	D18	K28
J16	U2	C18	B17	J30
J16	U2	B19	A18	K30
J16	U2	C15	C16	J28
J16	U2	C17	F16	J29
J16	U2	C12	A15	J26
J16	U2	C14	D15	J27
J16	U2	B9	C13	J24
J16	U2	C11	E14	J25
J16	U2	F9	F13	J22
J16	U2	E9	B14	J23

Low Side Control	High Side Control	Signal	GND	VCCP
J16	U2	E21	D12	J20
J16	U2	G9	A12	J21
J16	U2	B21	E11	J18
J16	U2	C21	B11	J19
J16	U2	B16	D9	C27
J16	U2	B18	C10	C25
J16	U2	B12	B8	C30
J16	U2	B15	A9	C29
J16	U2	A19	C7	B26
J16	U2	B10	F10	B25
J16	U2	A16	A6	B28
J16	U2	A17	D6	B27
J16	U2	A11	F4	B30
J16	U2	A14	B5	B29
J16	U2	A8	D3	A26
J16	U2	A10	C4	A25
J16	U2	F8	A2	A28
J16	U2	G8	E2	A27
J16	U2	C8	G1	A30
J16	U2	D8	B1	A29
H15	U3	U6	Y7	V8
H15	U3	R6	AA6	AH19
H15	U3	P6	AA3	W8
H15	U3	T5	W7	AJ19
H15	U3	U5	Y5	Y8
H15	U3	V5	Y2	AK19
H15	U3	U4	AE17	AH22
H15	U3	T4	AN17	AG22
H15	U3	R4	W4	AA8

Low Side Control	High Side Control	Signal	GND	VCCP
H15	U3	V4	V7	AL19
H15	U3	M4	V6	AB8
H15	U3	M5	V3	AM19
H15	U3	M6	AJ20	AF22
H15	U3	W5	AG23	AE21
H15	U3	W6	U7	AC8
H15	U3	P3	AH23	AE22
H15	U3	M3	T6	AG19
H15	U3	L4	T7	U8
H15	U3	L5	AH20	AN21
H15	U3	Y4	AJ23	AN22
H15	U3	Y6	R2	AF19
H15	U3	P2	AK23	AE23
H15	U3	N2	AG20	AE19
H15	U3	L2	AK24	AK25
H15	U3	K3	P7	P8
H15	U3	K4	R7	T8
H15	U3	K6	P4	R8
H15	U3	AA4	AJ24	AJ25
H15	U3	AA5	N6	N8
H15	U3	AB4	N3	AM21
H15	U3	AB5	AF20	AM22
H15	U3	AB6	AH24	AH25
H15	U3	J5	N7	AL22
H15	U3	J6	AG24	AG25
H15	U3	AC5	M7	L8
H15	U3	AD5	M1	M8
H15	U3	AD6	AE20	AF21
H15	U3	G5	AF24	AJ26

Low Side Control	High Side Control	Signal	GND	VCCP
H15	U3	F5	L3	AG21
H15	U3	L1	AL24	AK26
H15	U3	K1	L7	J10
H15	U3	F2	L6	K8
H15	U3	E3	AL20	AH21
H15	U3	E4	AL23	AL25
H15	U3	AF4	K2	AJ21
H15	U3	AF5	AM24	AL26
H15	U3	D2	K5	J11
H15	U3	D4	K7	AJ22
H15	U3	C1	AM23	AN25
H15	U3	C2	AN24	AM26
H15	U3	C3	H3	AK21
H15	U3	C5	J4	J12
H15	U3	C6	AM20	AM25
H15	U3	B2	J7	J13
H15	U3	G7	AN23	AL21
H15	U3	B3	AN20	AN26
H15	U3	B6	H6	AK22
H15	U3	B4	H7	AG26
H15	U3	A4	H8	J15
H15	U3	A3	AF23	AG27
H15	U3	D7	H10	AH27
H15	U3	A5	H9	J14
H15	U3	A7	H12	J9
H15	U3	B7	H11	J8
H16	E7	U6	AN17	AN14
H16	E7	R6	AB1	V8
H16	E7	P6	AN16	Y8

Low Side Control	High Side Control	Signal	GND	VCCP
H16	E7	T5	AA7	W8
H16	E7	U5	AC3	AB8
H16	E7	V5	AB7	AA8
H16	E7	U4	AC7	AL8
H16	E7	T4	AC6	AC8
H16	E7	R4	AM17	AD8
H16	E7	V4	AM16	AN15
H16	E7	M4	AD4	AN9
H16	E7	M5	AD7	AM9
H16	E7	M6	AL17	AM15
H16	E7	W5	AE2	AL9
H16	E7	W6	AE16	AN11
H16	E7	P3	AF3	AJ9
H16	E7	M3	AE7	AE9
H16	E7	L4	AE5	AK9
H16	E7	L5	AF7	AL11
H16	E7	Y4	AF6	AM11
H16	E7	Y6	AH1	AF11
H16	E7	P2	AG7	AK11
H16	E7	N2	AG17	AG11
H16	E7	L2	AF17	AM14
H16	E7	K3	AH3	AJ11
H16	E7	K4	AH6	AH11
H16	E7	K6	AH17	AL15
H16	E7	AA4	AH7	AE11
H16	E7	AA5	AJ4	AM12
H16	E7	AB4	AJ7	AN12
H16	E7	AB5	AL16	AK12
H16	E7	AB6	AK2	AL12

Low Side Control	High Side Control	Signal	GND	VCCP
H16	E7	J5	AL3	AH12
H16	E7	J6	AK7	AJ12
H16	E7	AC5	AK17	AF12
H16	E7	AD5	AJ17	AL14
H16	E7	AD6	AE10	AE12
H16	E7	G5	AL7	AG12
H16	E7	F5	AF10	AJ14
H16	E7	L1	AG10	AH14
H16	E7	K1	AK16	AK14
H16	E7	F2	AH10	AG14
H16	E7	E3	AL10	AE18
H16	E7	E4	AJ10	AF14
H16	E7	AF4	AF16	AH18
H16	E7	AF5	AK10	AF18
H16	E7	D2	AM1	AJ18
H16	E7	D4	AM7	AG18
H16	E7	C1	AG16	AE15
H16	E7	C2	AN1	AH19
H16	E7	C3	AH16	AK19
H16	E7	G7	AM10	AL19
H16	E7	C5	AN2	AJ19
H16	E7	C6	AN10	AL18
H16	E7	B2	AJ16	AK15
H16	E7	B3	AN13	AM19
H16	E7	B4	AK13	AN19
H16	E7	B6	AM13	AM18
H16	E7	A3	AE13	AJ15
H16	E7	A4	AL13	AN18
H16	E7	A5	AG13	AG15

Low Side Control	High Side Control	Signal	GND	VCCP
H16	E7	AG4	AJ13	AE14
H16	E7	AG5	AF13	AF15
H16	E7	AG6	AH13	AH15
J17	F6	G16	L28	T28
J17	F6	G17	L29	T27
J17	F6	F15	L26	T26
J17	F6	G15	L27	T29
J17	F6	G14	L24	T23
J17	F6	F17	L25	T24
J17	F6	E15	P30	U30
J17	F6	F14	L23	T30
J17	F6	G18	P28	U28
J17	F6	E16	P29	U29
J17	F6	E18	P26	N24
J17	F6	F18	P27	N23
J17	F6	E13	P24	N25
J17	F6	G13	P25	U27
J17	F6	D17	R30	N27
J17	F6	D13	P23	U24
J17	F6	E19	R29	N26
J17	F6	G19	AJ27	AD30
J17	F6	E12	R27	U26
J17	F6	D19	R28	AD29
J17	F6	G12	R26	W30
J17	F6	F12	V29	W28
J17	F6	F11	R24	U23
J17	F6	G11	V30	W27
J17	F6	G20	R25	U25
J17	F6	D11	R23	W29

Low Side Control	High Side Control	Signal	GND	VCCP
J17	F6	D20	V27	W23
J17	F6	F20	AK30	W24
J17	F6	E10	V26	W25
J17	F6	C20	V28	W26
J17	F6	F21	V23	Y30
J17	F6	D10	V24	AC23
J17	F6	C17	AA29	AC24
J17	F6	G22	AA30	Y29
J17	F6	C15	AA27	Y27
J17	F6	C18	AA28	Y28
J17	F6	C14	AA25	Y26
J17	F6	G21	AA26	AC25
J17	F6	C12	AA23	Y25
J17	F6	B19	AA24	Y23
J17	F6	B9	AB29	Y24
J17	F6	C11	AB30	AC26
J17	F6	F9	AB27	AC27
J17	F6	E9	AB28	AD27
J17	F6	E21	AB26	AD28
J17	F6	G9	AB25	AD25
J17	F6	B21	AK29	AH29
J17	F6	C21	AJ29	AG29
J17	F6	B16	AK28	AH28
J17	F6	B18	AJ28	AG28
J17	F6	B12	AM28	AM29
J17	F6	B15	AL28	AL29
J17	F6	A19	AB23	AD26
J17	F6	B10	AB24	AC28
J17	F6	A16	AE29	AD24

Low Side Control	High Side Control	Signal	GND	VCCP
J17	F6	A17	AE30	AC30
J17	F6	A11	AE27	AD23
J17	F6	A14	AE28	AG30
J17	F6	A8	AE25	AH30
J17	F6	A10	AE26	AC29
J17	F6	D22	AL27	AL30
J17	F6	E22	AN28	AN29
J17	F6	A22	AN27	AN30
J17	F6	B22	AM27	AM30

The test chip's zero ohm resistors, listed in Table 10, can be used to generate tests that can detect 0 ohm resistance between the two points, thus adding more open test coverage.

Table 10 - Zero Ohm Resistor

Shorted Ball	Shorted Ball
J1	D25
AA1	D26
AN4	AM4
AN6	AN7
AN3	AN8
AN5	AM8
F29	D28
H29	H28
E7	E23
F6	F23

The test chip has **VID_0-VID_5** signals pulled to VCCP with 1KΩ resistors. Socket electrical connections can be tested by measuring resistors between the respective electrical connections. The following table can be used to generate tests that can detect 1KΩ resistance between the two points, thus adding more open test coverage.

Table 11 - 1K Ohm Measurements

VID Ball	Power Ball
AM2	AJ8
AL5	AG9
AM3	AH8
AL6	AF8
AK4	AF9
AL4	AG8

Each pull-down resistor can be used to verify connectivity of a ground ball and a control signal ball. The following table can be used to generate tests that can detect 1KΩ resistance between the two points, thus adding more open test coverage.

Table 12 - 1K Ohm Measurements

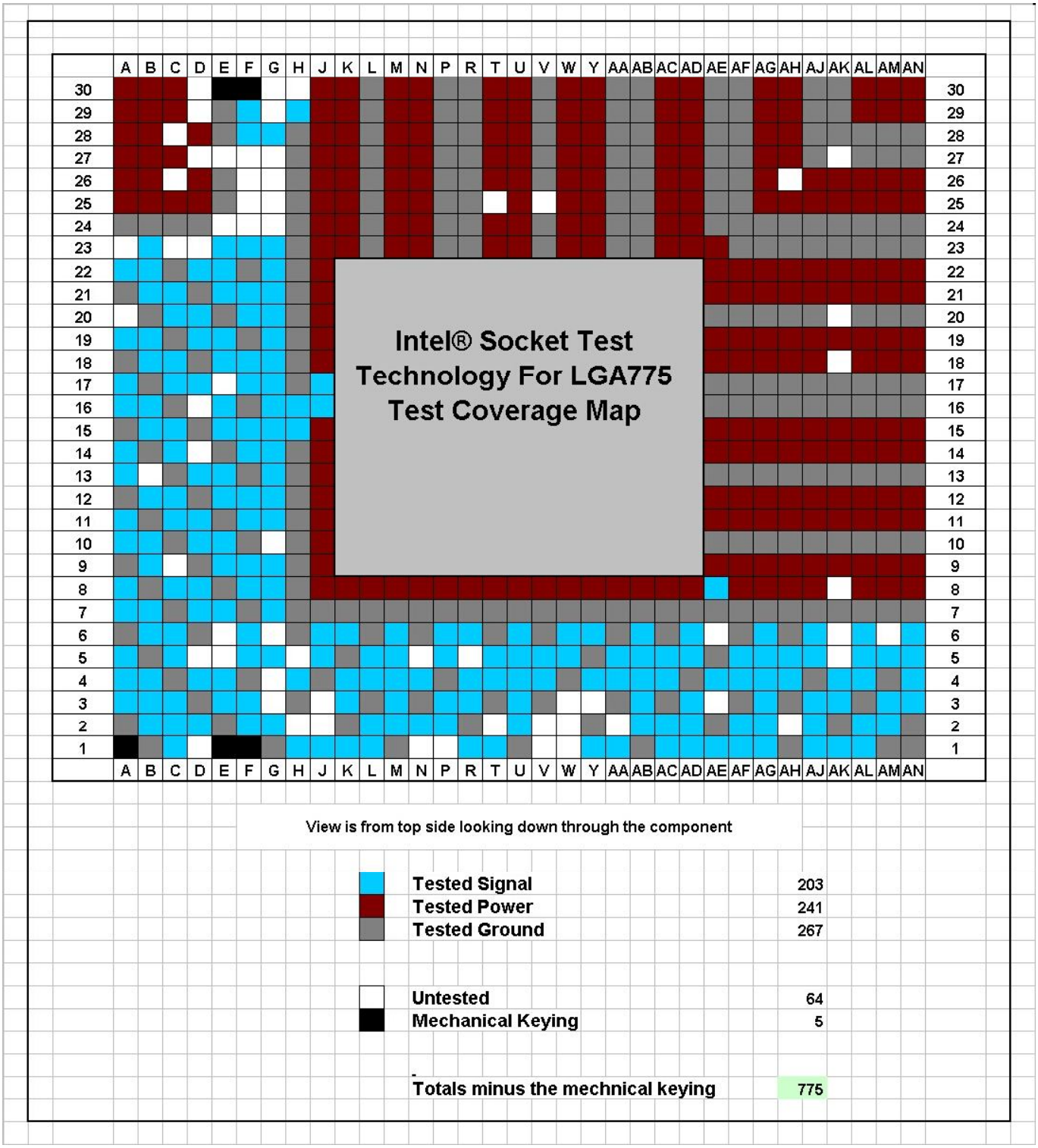
Control Resistor Ball	GND Ball
U2	U1
U3	T3
E7	E8
F6	F7
J16	H13
H15	H14
H16	H17
J17	H18

The following table can be used to generate tests that can detect 1KΩ resistance between the two points which will add more open test coverage.

Table 13 - 1K Ohm Measurements

Resistor Ball	Resistor Ball
AJ1	AJ2
AD2	AF2
AG2	AG3
AJ3	AK3
AD1	AC1
AF1	AB2
AE1	AG1
R3	Y1
F28	G28
F3	G23
A13	T1
B23	C22
AL1	AK1
G2	R1
H1	AL2
AC2	AE8
N4	P5
AC4	AE4
AH4	AH5
AJ5	AJ6
AB3	AD3
H4	M2
AM5	AH9

Figure 6 - Optimized Ball Coverage Map



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