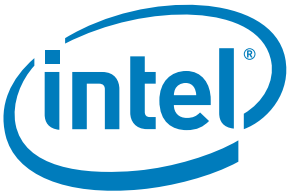


Avoiding New Design Errors When Using Intel® Ethernet Controllers

August 2008

319069-001
Revision 1.0

Contents

Revision History

Rev	Rev Date	Description
1.0	Aug 2008	Initial release (Intel Public)

1.0 Introduction

This document was created to help designers using Intel® LAN controllers avoid the most common issues that can cause them to lose valuable time needed to complete their design and get it to market on time. Equally valuable is the reduction in frustration every engineer experiences when a design has problems requiring troubleshooting and, if unable to solve it, contacting customer support for assistance. The issues are divided into three basic categories:

- Documentation and Software Issues
- Schematic Design Issues
- Printed Circuit Board (PCB) Layout Issues

1.1 Scope

This document discusses the most commonly repeated issues design engineers have experienced. Design engineers should follow the instructions in this document when checking new designs to help avoid any unnecessary lost time and frustration.

References to specific Ethernet controllers by part number is avoided. The desire is to list the issues common across multiple devices. Specific devices are referenced only when absolutely necessary such as when an issue is seen on only one device that is used by many different designers.

2.0 Documentation and Software

Documentation and software issues are the most frequently submitted design issues received by Intel LAN component customer support engineers.

For documentation, these include:

- No available documentation
- Out of date or incorrect documentation
- Not following recommendations in the proper documentation
- Relying on documentation for a similar (or believed to be similar) product

For software, an outdated device driver is the leading cause of reported issues. Some customers are not aware of the fact that Intel's device drivers are constantly being improved and updated. This is especially true during the first 6 to 12 months after a product's release. Through testing during this early post-launch window, Intel's validation teams and customers might discover problems and areas for improvement. If you appear to have a software issue related to a device driver, ensure you are using the latest version. Refer to Section 2.1 for information on obtaining the latest device drivers.

2.1 List of Critical Documentation

The following documents are required when designing with an Intel LAN component:

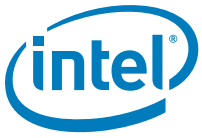
- Datasheet - details product features, external architecture including device operation, pin descriptions, register definitions, EEPROM/NVM, programming information, design considerations, and board layout considerations.
- Specification Update - an update that contains specification changes and clarifications as well as errata; sometimes incorrectly referred to as the errata document).
- The EEPROM and/or NVM Information Guide - This guide might also be called an NVM Map and Programming Guide since newer silicon can store the configuration data directly to the Flash device. Note that this information is included in the Datasheet for newer silicon, such as the 82574, 82576, and the 82598.
- Software Developer's Manual (SDM) - The SDM or software section of the datasheet details customized functions. This is helpful for designs that cannot be set up by the EEPROM or the Intel device driver. Most Intel device drivers include an installed tool, PROSet, for modifying a wide array of device driver functions. The SDM gives instructions that enables a designer to write customized software routines if required. Note that this information is included in the Datasheet for newer silicon, such as the 82574, 82576, and the 82598.
- Design Guide - This guide provides board design and layout information for older silicon (this information is also available in Platform Design Guides (PDGs) for devices such as the 82566 and 82567). Design Guide information includes: details of various frequency control devices, methods for crystal validation, Ethernet layout considerations, Bill of Materials (BOMs), etc. If a Design Guide is not available, use the design checklists for both schematic and layout reviews. Note that this information is included in the Datasheet for newer silicon, such as the 82574, 82576, and the 82598.

Additional documentation for designing with LAN components can be found on the line card on Intel's web site at:

www.intel.com/products/ethernet

Refer to Section 2.2 for detailed access instructions. Each device has the above basic and necessary design documents but each might also have additional documents covering other design subjects unique to its capabilities that might be of interest. An example is the ATCA (PICMG 3.1) compliant SerDes-to-SerDes over a backplane. (Refer to the 82571EB documents URL by picking it off the line card).

If unable to locate required documentation on the web site, first check with your Intel representative before submitting a support issue to Intel Premier Support (if applicable). Some documentation remains Intel Confidential or might not yet have been declassified for the public site. An Intel representative can help you locate the correct document and assist in making the information available.



2.2 Accessing Documentation and Software

A line card URL of all released Ethernet controllers can be found at:

http://www.intel.com/products/ethernet/

You can navigate to this page using the following steps:

1. Go to http://developer.intel.com/design/index.htm
   a. Select the Products and Technologies tab.
   b. Select the Network Connectivity link.
   c. Select Ethernet Controllers.

The line card lists product information for each released Ethernet controller that is recommended for current designs. Products can be filtered by category (10 Gigabit, Fast Ethernet, or Gigabit). To view product collateral, select the link to a specific product. This provides you a list of all public documentation and driver downloads with links to all. Note that the default setting is for 10 items per page; additional items show on a second page.

The links to driver downloads takes you to a list of supported operating systems from which you select the one you are using. Select the Go button to download. If an operating system is not on the list, it could be Intel® doesn't supply device drivers for that operating system, or they might not yet be publicly available for newer devices. In the case of a new operating system or device, if the operating system or device driver is not listed, check with your Intel representative. The device driver might be available in the beta stage, and if a device driver whose development is still in process meets your needs, you might be able to get a copy.

Be sure to check back from time to time as the documentation and software are updated each time it is needed for corrections or improvements. The newer the silicon the more frequently the designer should check for documentation and software updates.

In the case of Linux, the device drivers are at:

www.sourceforge.net

At the front page of the site, type `e1000` in the search box for 10/100 Mb/s (Fast Ethernet), Gigabit Ethernet (GbE) and 10 GbE controllers' device drivers and then follow their navigation path to the listing of the device drivers and related documentation. Be sure to pick the stable driver; for example, `e100 stable` for 10/100 Mb/s, `e1000 stable` for GbE device drivers, and, in a naming deviation, i`xgbe stable` for the 10 GbE device drivers. Any others are still under development. FreeBSD drivers are in the latest distribution at:

www.freebsd.org

This document does not cover issues concerning unclear documentation. Please contact your Intel representative as soon as possible if you discover areas of documentation that require clarification. If your FAE can't resolve it, he or she will submit a request for clarification to customer support which, in most cases, is answered quickly. Don't hesitate to contact your FAE to help clear up a passage or if you suspect there might be an error in documentation.

All of the required public documentation, as well as software like device drivers, and firmware such as Intel Boot Agent, for released LAN silicon are available on the Intel® public website. This should be a designer's first stop before beginning a design using an Intel LAN device.

3.0 Not Following Recommendations in Design Documentation

Having the proper documentation is critical as previously explained but once you have it you must use it. That might seem obvious, and it is, but the amount of documentation might seem just too daunting to carefully study to someone new to Intel® LAN component design and unnecessary to someone experienced with it alike. A new designer can feel overwhelmed by the amount of data in a design guide, for instance, which are generally fairly sizable as compared to a plain datasheet which is just a datasheet rather than one with the design guide incorporated. A datasheet with the design guide incorporated generally always has the software developer's manual included making for a very large document but keep in mind it is three documents in one so don't allow the size to intimidate you. Stick to the datasheet for the component's feature list, pin descriptions, thermal information, clock and DC and AC specification and the design guide for the critical requirements and recommendations for the actual design. Keep in mind that recommendations (as compared to requirements) are not that different as they've come from extensive testing and it we strongly advise adhering to the recommendations for the best chance of a successful design.

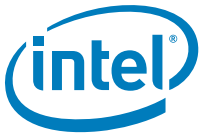
The design guide either includes checklists for both schematic design and the PCB's layout or they are available as separate documents. Checklists are very important as they give the designer a way to go through the listing of the critical elements of the design and, as their name indicates, check off each item once it is verified the design adheres to the item.

A design guide provides the necessary guidelines to choosing item's that are part of the LAN design such as the clock, the magnetics both discrete and integrated with the LAN connector, as noted previously often referred to as Magjacks, EEPROMs, Flash components, critical passive components such as resistors that must be 1% tolerance and etc. It also provides guidance for proper layout of critical traces, proper placement of specific components where needed, proper power supply decoupling, etc. Also included is a reference schematic, another valuable tool for checking the design's schematic. Later in this document, starting with the next section, untested magnetics, some of these requirements and recommendations that are most often either not followed or are not followed properly will be presented. As previously stated, if you do not understand a document's recommendation or explanation contact your Intel® representative immediately.

We depend on our customers to let us know when documentation is unclear, missing needed information, has conflicting information, etc., so we can fix the issue and release an updated version.

3.1 Critical Component Documentation - Clocks

Be sure to pay close attention to the datasheet specifications for the components listed in the design guides as critical such as the clock generation circuits. Clock problems arise far too often due to designers not following the datasheet specifications and design guide requirements for the clock. When the clock circuit is not properly designed and operating well within its proper parameters a wide variety of problems can be exhibited, many of which don't even seem to be clock related. The clock can be considered the heart of the LAN controller and the healthier the clock circuit the better the LAN controller can be expected to perform.



If the design guide says do not use a certain type of part, such as a ceramic resonators, don't use it. The reason so many designs end up with clock (and many other) problems are likely due to not having the right documentation and/or not following the requirements and recommendations of the documentation. We single out the clock source specifically here as it is a sensitive, critical circuit and thus must be designed with care.

Please note crystals and oscillators are not the same thing even though an oscillator chip might have a crystal in it as its frequency source. We prefer the use of quartz crystal, which must be series resonant but whether using a crystal or an oscillator be sure it meets the requirements specified in the design guide and datasheet for the LAN device being used.

4.0 Use of Magnetics Intel® Has Not Tested

Although a particular magnetics module, whether discrete or integrated with the RJ45 LAN connector (commonly known as a Magjack* and from here on will be referred to as such), might appear to or even match the specifications of those documented in the design guides or datasheets to have been tested successfully by Intel does not guarantee that part to be the equal to those tested successfully by Intel.

Due to the competitive environment in today's markets, designers of components strive to keep the costs down just as system manufacturers do and this can result in less reliable components and more variation in different manufacturers' lots of a component. A lot is a batch of the same component run on a manufacturing line at one time. That same manufacturing line is often then retooled as needed and used to make a different component then will retool again to make another lot of the first component which is given a new lot number. Since no two lots are completely identical the differences can result in one lot passing tests in a circuit without error and another lot having a percentage fail or produce marginal results when the same tests are performed. The only way to reduce to a minimum the possibility of different lots from a manufacturer causing problems is run the compliance or conformance tests on multiple parts from multiple lots.

When Intel tests a magnetics module with one of our LAN devices that's exactly how it is done; testing is done on multiple parts from multiple lots from each manufacturer's products selected for testing. Therefore, the magnetics listed are known to work with the Intel LAN product under the conditions and in the circuit they were tested in. This in no way means they will work in every circuit even if the design guide is carefully followed. It means however, the designer can have more confidence that they are compatible with the LAN component.

To avoid any confusion, this testing is not qualification testing. We make no claims to have qualified the magnetics only tested them under specific conditions. Nor do we recommend any specific magnetics modules. The ones we've tested and listed in the design guide or datasheet are simply magnetics we've tested, as stated already, under specific conditions, and those conditions might differ greatly from the conditions a customer's design has to operate in. That's why our documents have statements concerning the magnetics modules listed that only say things like, "The following magnetics modules have been used successfully in previous designs." Note there is no claim they will work in just any design, only that they've worked in previous designs they were used or tested in. Therefore, we still strongly recommend each design prototype be tested thoroughly with the magnetics module selected which is why despite the listing of certain modules we've tested you'll also find detailed sections on qualifying magnetics modules for your design. Starting with a magnetics module we've tested and listed in the documentation provides you with the advantage of using one that has worked satisfactorily in our tests and/or in other designs as opposed to using one that may never been tested by us or known to been used successfully with the LAN controller in question under any conditions.

To demonstrate the critical nature of proper magnetics selection, note that we have found that improper magnetics selection can account for as much as 50% of IEEE test failures during the late stages of a design's development.

5.0 Poor Routing of Differential (MDI) Traces

This is one of the most critical aspects of layout design in a LAN circuit and therefore the design guide must be followed when routing these traces that go from the PHY to the magnetics and then from the magnetics to the RJ45, if discrete magnetics are used. If integrated Magjacks are used, the MDI traces are the traces from the PHY to the Magjack. When performing a board layout, the CAD tool must not automatically route the differential pairs without intervention. In most cases, the differential pairs will have to be routed manually. Since the full details of routing these traces is given in the design guides we will just cover the most common errors with visual examples. Tolerances such as how close the lengths of traces with a differential pair should be maintained will not be given as all of that is also in the design guides. Only general statements will be used to highlight the problem subject.

5.1 Symmetrical Routing of Differential Traces

Keep the two traces in a differential pair equal in length and close together and symmetric (which simply means each is as much alike the other as possible.) Asymmetrical and unequal length traces in the differential pairs contribute to common mode noise.

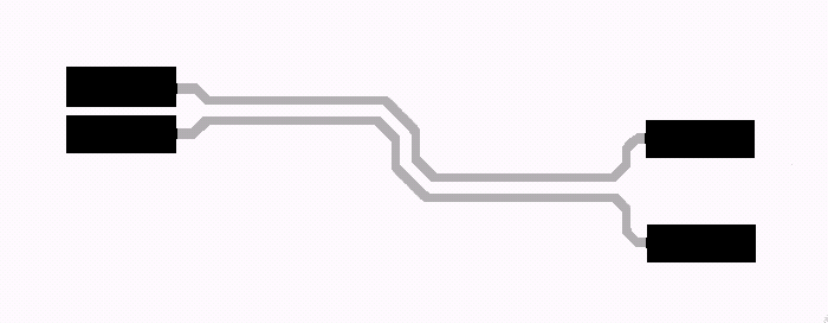


Figure 1. Properly Routed MDI Trace Pair

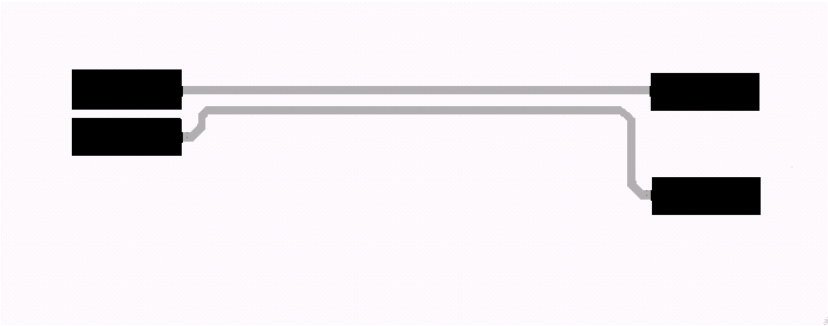


Figure 2. Poorly Routed MDI Trace Pair (Top Trace Shorter Than Bottom Trace

Figure 3. Poorly Routed MDI Trace Pair (Top Trace Method to Match Lengths Creates a Section That is not 100 Ω Differential as Required)

5.2 Keep Differential Pairs Separated

Trace pairs need to be kept well apart to avoid crosstalk between them.

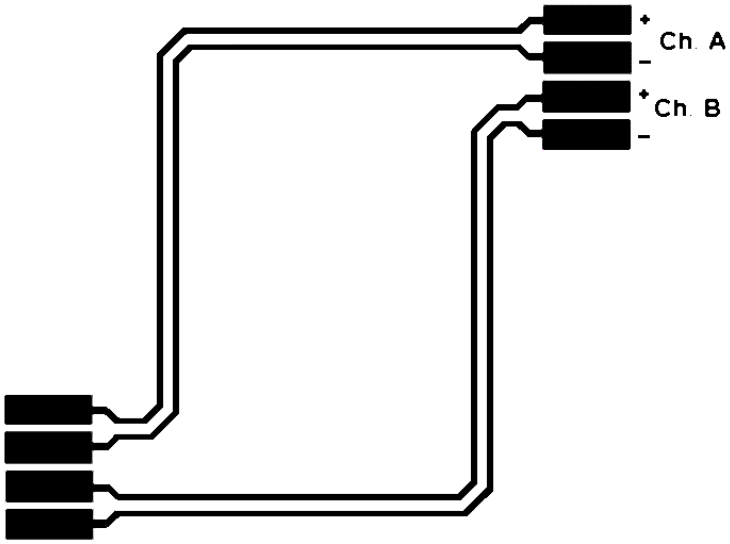


Figure 4. Properly Separated Pairs

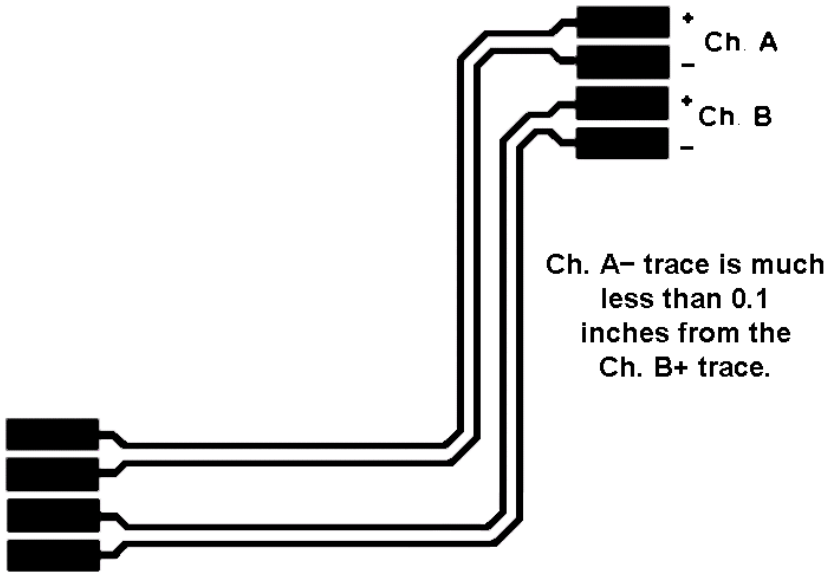


Figure 5. Trace Pair to Channel A is too Close to Channel B Pair

6.0 LAN POWER GOOD (LPG) Pulled to 3.3 V dc

Note: Also referred to as Internal Power On Reset.

This is a very common mistake made worse by the fact it often seems to work especially during the prototype stage but then when a design goes into production various power-up problems begin to happen, generally intermittently and sometimes on just a percentage of the products.

LAN power good is meant to be connected to some type of voltage supervisor circuit that gives a reliable signal after all power rails are up and stable. There is a specified minimum delay from the time the power rails reach their operating voltage and LAN power good being asserted. On most computers there is a power good signal output provided for just that purpose but the designer not designing an add-on system for a computer has to be sure to design in a reliable supervisory circuit.

To do this, there are some requirements to be taken into account:

- Apply power supplies from high to low. For example, 3.3 V dc, then 1.8 V dc, then 1.1 V dc depending, of course, on what voltages are used by the device.
- Wait at least 60 to 80 milliseconds before asserting LAN power good

Note: Moving forward with future devices, starting with the 82571EB/82572EI, our LAN devices will have an internal LPG feature and this will no longer be a consideration so be sure which type you are using. The 82571/82572's older datasheets showed them having a LAN power good pin but that it was to be left unconnected. This has been corrected in the newer datasheets and shows it as a no connect pin, which is another reason to be sure to have up to date documentation.

The best way to ensure your design meets the previous power sequencing requirements is to cascade the power supplies so that they are dependent on the previous higher voltage one. For example, have 3.3 V dc create the 1.8 V dc power, which in turn creates the 1.2 V dc again depending on the actual voltages used. However, the sequencing is done though connect a supervisory circuit to the lowest voltage rail and base the LAN power good signal on it remembering to wait at least 60 to 80 milliseconds after the voltage has reached it operating level before asserting LAN power good to give it time to stabilize.

7.0 Issues With Power Delivery to the Intel Controller

There are three key needs when designing the power supplies for use with Intel controllers listed in this section and shown in the accompanying figures.

7.1 Metal Thermal Ground Pads

Use metal thermal ground pads to create a heat sink effect to help regulators dissipate heat.

Use as large a pad a feasible since the larger the area the more heat dissipation can occur. In many cases the right sized pad can alleviate the need for a heat sink and, even when one is still necessary, still reduce its size and cost.

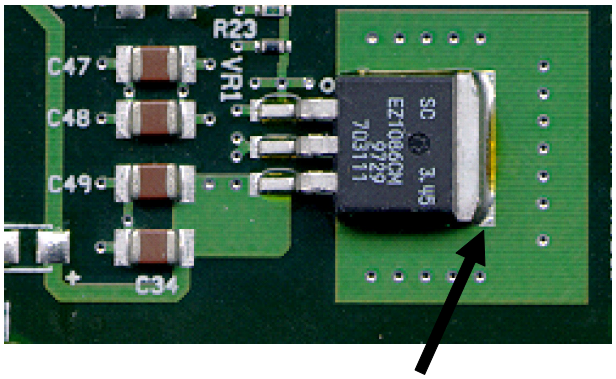
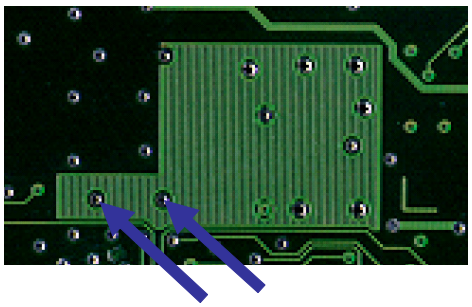


Figure 6. Plated Metal Thermal Ground Pad for Regulator

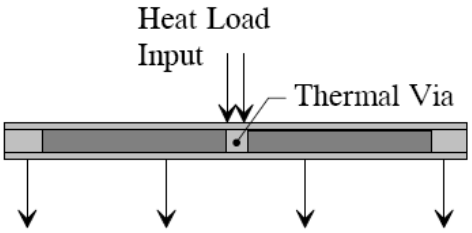
7.2 Thermal Vias

Connect each voltage regulator's thermal pad to ground or power planes with multiple thermal vias.

This helps conduct heat away from the regulator much more efficiently. Use as many as economically feasible as too many would be overly expensive and too few would do little to reduce the heat.



Thermal Vias on PCB



Functional Illustration

Figure 7. Thermal Vias (Functionality Illustrated)

7.3 Decoupling Capacitors

Make sure to place decoupling capacitors as near to the Intel controller's power inputs as possible.

The closer to the power inputs a decoupling capacitor is the more effectively it is able to filter out unwanted noise and transients due to minimizing the resistance of the traces between the capacitor and the LAN controller's pin. If at all possible connect the ground side of the decoupling capacitor to a filled via which goes directly through to the ground plane for the same reason.

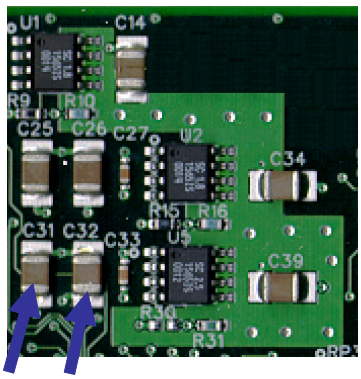


Figure 8. Good Decoupling Capacitor Placement

8.0 Not Enough Decoupling and Bulk Capacitance on Voltage Supplies

Decoupling capacitance cleans up noisy DC power supplies and removes spikes that might be out of the specification for the device's needs. Decoupling and bulk capacitance become important to make sure that the voltages you apply to the LAN controller really are DC (direct current) as you expect them to be without high ripple content. Be sure to adhere to the recommendations given in the design guide for the LAN device you are designing with. Once the PCB is built it is an expensive and difficult problem to add more capacitance. When in the prototype stage even though you've followed the design guide you should check the voltage rails and make sure the noise is within the specifications for the device.

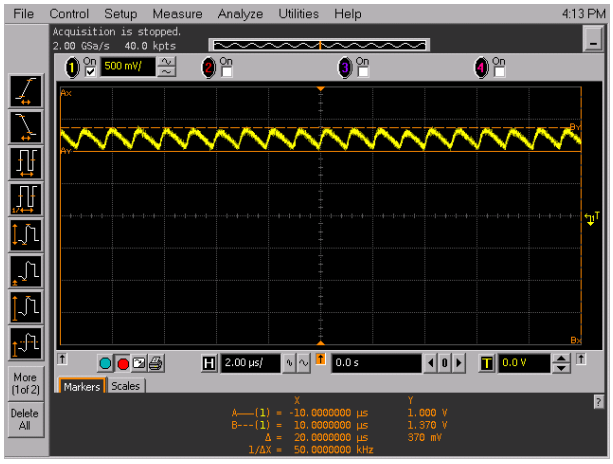


Figure 9. Example of the Effect That Lack of Decoupling Causes

This 1.2 V dc voltage supply with no decoupling has >30% ripple while the specification is 10%.

9.0 Intel LAN Controller Too Close to Integrated Magnetics (Magjack) or Board Edge

If the LAN silicon is too close to the built in connector, then some of the strongest magnetic, or as better known in the electronics industry, E-Fields will couple onto the connector shield. If too close to the board's edge the fields escape from the board and possibly couple into nearby electronics as well as increase Electromagnetic Radiation (EMI) but if far enough from the Magjack connector and far enough from the edge of the board, then the strongest E-Fields will couple back onto the board and be harmlessly dissipated into the ground and power planes (see Figure 10 and Figure 11).

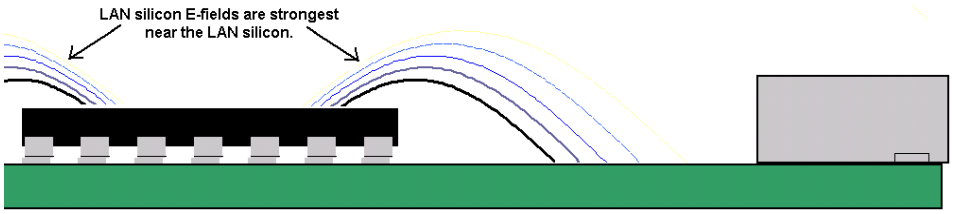


Figure 10. Problem With Having LAN Silicon Too Close to Board's Edge

As clearly seen on the left side of Figure 10, the E-Field is exiting the edge of the PCB.

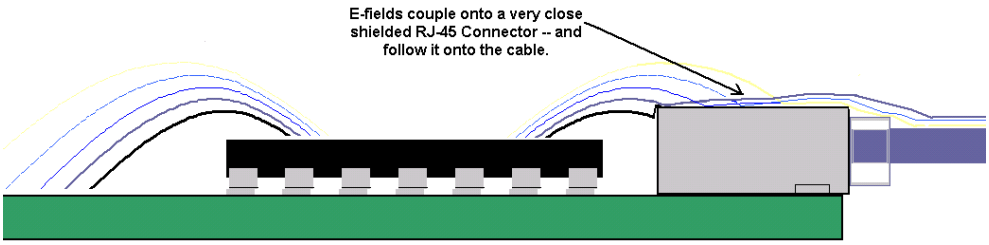


Figure 11. Problem With Having LAN Silicon Too Close to Magjack

Again, Figure 11 clearly shows that when the LAN silicon is too close to the connector the E-Field is coupled into the shield and then into the cable where it is likely to decrease signal integrity, possibly even significantly, as well as possibly insert noise into the link partner's circuitry.

10.0 Connecting RST# on 82551xx Devices to System PCI Reset

This has become a frequently repeated mistake but a natural one since the most popular Fast Ethernet (FE) or 10/100 Mb/s Intel® LAN controller prior to the 82551 family were the 82559/82559ER/82559ER extended temperature controllers.

Now that the 82551QM is recommended for new FE designs instead of the 82559, the 82551ER instead of the 82559ER and the 82551IT instead of the 82559ER extended temperature, many designers assumed they were drop in replacements and they actually can be hardware wise (See AP-442 "82559/82559ER to 82551ER/IT/QM Migration" for the minor differences that need to be accounted for especially in the software and firmware (EEPROM)). Included in that assumption was that the PCI reset pin, RST#, should still be connected to the system's main PCI reset signal. In the previously mentioned AP-442, the last sentence in the note under the pin differences table states "No hardware changes are required" and that is true but not recommended for new designs. For existing 82559xx designs the corresponding 82551xx device can be placed without hardware changes. For new designs it is required that the ISOLATE# pin be connected to the system's main PCI reset signal and the 82551xx RST# pin be tied to 3.3 volts.

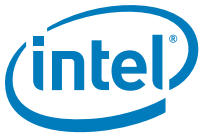
11.0 Not Asking For Help Soon Enough

As design engineers ourselves the authors know it is in our nature to try to determine what is causing a problem on a design and only ask for help when absolutely necessary. This results in many customer support issues being filed as urgent and by frustrated, upset designers. We urge you to of course make a reasonable effort to find the problem but don't wait until you are running out of time or the design is in jeopardy of being delayed before contacting your Intel® representative. Remember even after filing a support request it CAN take some time for the Intel engineers to find the problem so be sure to ask for help while there is still plenty of time to find and fix it without endangering your time to market. This is especially true in the case where you don't understand something in the documentation. Don't try to figure it out by trying different ideas but call for assistance. If you find it hard to understand there's a very good chance others do to and it MIGHT well need to be reworded or, if in error, corrected.

12.0 Not Taking Full Advantage of Intel®'s Offer to do Schematic AND Layout Reviews

Schematics and board layout checklists are available for ALL silicon. One time schematic and layout reviews available via QuAD using the product called "One_Time_Schematic_Review (Networking)". Use it for layout reviews for now as we rarely get those and if we start getting enough we'll add it as a separate product. We will even perform reviews of non-IA designs with Intel Ethernet LAN products. Be sure to have the schematic and layout reviews done early in the design cycle to find any issues to fix before they become serious problems. The following are the basic rules for a QuAD (Intel Premier Support) schematic review:

- Be sure to have (and use) the design guide and the schematic checklist for the product being designed in. Go through each item in the checklist before requesting the review; in other words do a self-review first. That way at least two different engineers will review the design. If we find too many issues that should have been caught during the self-review we will terminate the review and request the customer go through the checklist again.
- We'll need a copy of the schematics in Adobe Acrobat* (.pdf) format with searchable text. We will accept schematics in their native format if a viewer is available, but will also require a copy in Adobe Acrobat (.pdf).



- All traces must have off-page references. Off-page grid references for signal names are optional unless you are unable to output PDF files with searchable text. Please provide full system schematics as we need to see all pages with connections to the part being reviewed as well as where power is generated.
- A system block diagram is very helpful but not essential if you don't have one available.

For layout reviews check first that we have a viewer since they have to be sent in their native CAD format. If we do we'll also need the schematics to help with identifying and locating the parts. Follow the previous requirements for the schematics except if possible provide a block diagram of the device placement with the LAN device and it's companion components such as the magnetics module and RJ45 or the Magjack, EEPROM, etc., labeled, which speeds up the review even more.

Some other things that will help you get the most out of your Intel design review are:

- Provide us the datasheets for parts that are not Intel tested, if any, and remember they must be in English.
- Let us know What features are supposed to be enabled such as the SMBus, WOL, CSA, Intel® Active Management Technology (Intel® AMT), etc.
- Is this a last review of the board or first spin (version)?
- What versions of the documentation was used to generate these schematics? This will help us be sure you had up to date documents. If you didn't we'll know if there are items missing or updated in the latest documentation and be able to check to see if the changes are incorporated in your design or not. If not we can immediately notify you of those changes.

13.0 Summary

It is our sincere hope this document will save you time by helping you identify some of the most commonly overlooked areas in designs we've had issues submitted on before they delay your progress in any way even just by causing you to call your Intel® representative. Please let us know through your representative of any improvements we can make to this document as we will be changing it as the more common issues change as they almost always do with the introduction of new silicon. As a last note we want to reiterate our admonition to be sure to get and study the critical documentation before designing your product. It will pay big dividends in time saved even though at the time it may seem to be using time that could be better used; it isn't. Nothing can improve your chances of having a successful design than knowing the design requirements and recommendations that come from extensive testing by the Intel® LAN engineering departments.