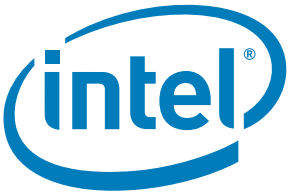
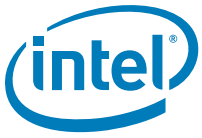


# Intel® 82598 Power Supply Sequencing/Power On Reset/ LAN_PWR_GOOD Design Clarifications

***December 2008***

321136-001EN
Revision 1.0



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# Revision History

| Rev | Rev Date | Description |
|---|---|---|
| 1.0 | Dec 2008 | Initial public release. |

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# 1.0 Introduction

This document describes the power supply sequencing and the Power On Reset (POR)/ LAN_PWR_GOOD design clarifications for the 82598 10 GbE controller.

## 1.1 Products Affected

| Part Number | Product Name | Description |
|---|---|---|
| 82598EB<br>JL82598EB | Intel® 82598 10 GbE Ethernet Controller | High-Performance, Dual-Port 10 Gigabit Network Connectivity Designed for Multi-Core Processors and Optimized for Virtualization. |

## 1.2 Reference Documents

- *Intel® 82598 10 GbE Ethernet Controller Open Source Datasheet*, Intel Corporation
- *Intel® 82598 10 Gigabit Ethernet Controller Specification Update,* Intel Corporation

# 2.0 Proper Power Supply Sequencing

The proper power on sequencing of the power supply voltage rails and the use of the internal Power On Reset (POR) versus the use of the externally generated LAN_PWR_GOOD signal (as specified in the current Intel® 82598 10 GbE Ethernet Controller Open Source Datasheet) are located in multiple sections of the document. Consequently, all sections should be looked at for proper power on sequencing as well as the use of POR or the LAN_PWR_GOOD signal.

Voltage rail sequencing must be followed (as described in the 82598 Datasheet) and as summarized below or excessive current leakage and/or device latch-up might occur.

Intel has made several updates/clarifications to the *Intel® 82598 10 GbE Ethernet Controller Open Source Datasheet*, and recommends that designers follow the summary steps below to assure that the Intel® 82598 is properly initialized and does not subject the silicon to latch-up and/or forward biasing the internal ESD protection diodes.

## 2.1 Voltage Rail Sequencing

- +3.3 V dc rail:
  - 3.3 V dc must come up first.
- +1.8 V dc rail:
  - 1.8 V dc follows 3.3 V dc and must come up* no sooner than 10 µs and no later than 100 ms after 3.3 V dc.
- +1.2 V dc rail:
  - 1.2 V dc follows 3.3 V dc and must come up* no sooner than 10 µs and no later than 100 ms after 3.3 V dc.
  - If 1.2 V dc rail ramp is leading 1.8 V dc; 1.2 V dc must not be more than 0.3 V (max) voltage difference from 1.8 V dc (for the entire ramp duration). See the following diagram.
  - If 1.2 V dc rail ramp is lagging 1.8 V dc; 1.2 V dc must not lag 1.8 V dc by more than 0.5 ms (when measured at 0.4 V dc). See Figure 1.

*Note:* If board designers have difficulty meeting this parameter, use the LAN_PWR_GOOD (external) timing parameter instead.

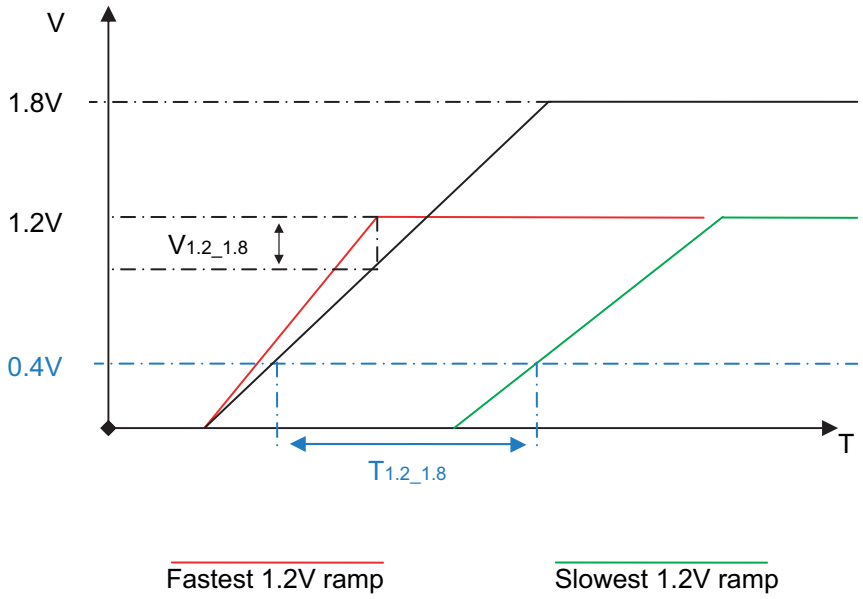


**Figure 1. 82598 Power Supply Sequencing Diagram**

*Note:* * measured at 90% of final nominal voltage amplitude.

For more detailed timing information, please refer to revision 2.5 (or later) of the *Intel® 82598 10 GbE Ethernet Controller Open Source Datasheet* (Section 5).

## 2.2 Power On Reset Timing

There are two methods of initializing the 82598: internally or externally. The desired implementation method can be determined by complying with the following power on sequence instructions.

### 2.2.1 POR_BYPASS Timing - Internally Generated

1. Disable the POR_BYPASS pin (via external 470 Ω pull-down resistor as specified in the Reference Schematics provided in the *Intel® 82598 10 GbE Ethernet Controller Open Source Datasheet*.
2. The LAN_POWER_GOOD pin should be left unconnected (has an internal pull-up resistor).
3. Apply power following the requirements described in Section 2.1.

For more detailed timing information, please refer to revision 2.5 (or later) of the *Intel® 82598 10 GbE Ethernet Controller Open Source Datasheet* (Section 3).

### 2.2.2 LAN_PWR_GOOD Timing - Externally Generated

*Note:* if +1.2 V dc/+1.8 V dc voltage rail sequencing requirements cannot be met (refer to Section 2.1 for details).

1. Enable the POR_BYPASS pin (via external 8.2 KΩ pull-up resistor to 3.3 V dc).
2. Apply the externally generated signal to the LAN_PWR_GOOD pin:
   a. Initially de-asserted (low).
   b. Assert (high) 40 to 80 ms after 3.3 V dc rail is stable (100%).
   c. Must stay asserted for at least 100 ms (hold time for PERST#).

For more detailed timing information, please refer to revision 2.5 (or later) of the *Intel® 82598 10 GbE Ethernet Controller Open Source Datasheet* (Section 5).



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