82573 NVM Map and Programming Information Guide

September 2008

Order No.: 315483-005
Revision 2.7

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Revision History

Date	Revision	Description
September 2005	2.0	Initial release.
January 2006	2.1	Updated values for the default of Word 12h Device ID Value added for the 82573L Included new (11/05) NVM Images in Appendix A
September 2006	2.2	Included 82573V in section 2.4
October 2006	2.3	Major edit all sections Updated Table 3 “Compatible Flash Parts”. Added document ordering number.
October 2006	2.4	Updated Tables 1, 3, 14, and 16. Removed the note from Section 2.1.11.
January 2007	2.5	Removed Table 31 “LED Control”.
May 2007	2.6	Updated Table 16 (bit 0 description). Changed setting to 1b for the **82573E/V** only.
September 2008	2.7	Updated Boot Agent bit descriptions (removed all references to RPL).

1.0 Introduction and Scope

This document covers programming information for the Non-Volatile Memory (NVM) of the Intel® 82573. For purposes of this document, 82573 refers to the 82573E, 82573V and 82573L, unless otherwise stated.

The Intel® 82573 requires non-volatile content for device configuration, log events and firmware extensions. The NVM might contain the following four main regions:

- **LAN Configuration Space for Hardware.** This area is accessed by hardware and loaded by the 82573 after power-up, PCI reset de-assertion, D3 to D0 transition, or software commanded EEPROM reset (CTRL_EXT.EE_RST).
- **Firmware Space.** This space is accessed by the 82573E/V in Alert Standard Format (ASF) mode or by the 82573E in Intel® Active Management Technology (Intel® AMT) mode. In ASF mode, the 82573E/V loads the data following power-up, ASF soft reset (ASF FRC_RST), or software commanded ASF EEPROM read (ASF FRC_EELD). In Intel® AMT mode, this space is protected against software access, and the firmware might access it at any time.
- **LAN Configuration Space for Software.** This space is used by software only. Register descriptions are listed here as a convention for the software only and are ignored by the 82573.
- **Boot Expansion Space.** This is accessed by software and is used by the BIOS at boot time.

A software utility based in Microsoft* DOS called EEUPDATE was created by Intel and can be used to program EEPROM images in development or production line environments. To obtain copies of this program, contact your Intel representative.

Unless otherwise specified, all numbers in this document use the following numbering convention:

- Numbers with a suffix of “b” are binary (base 2).
- Numbers that do not have a suffix are decimal (base 10).
- Numbers with a suffix of “h” are hexadecimal (base 16).

Note: The 82573V and 82573L devices do not support Intel® AMT. Any references relating to Intel® AMT only apply to the 82573E.

1.1 Supported NVM Devices

Predecessors to the 82573 required both an EEPROM and Flash device for storing LAN data. However, the 82573 reduces the Bill of Material (BOM) cost by consolidating the EEPROM and Flash into a single non-volatile memory device. The NVM is connected to a single Serial Peripheral Interface (SPI). In addition, the 82573 reduces the BOM by enabling a solution that merges the BIOS and 82573 storage into a single shared Flash device. Shared Flash with the BIOS is valuable for Intel® AMT, ASF and basic functionality.

The 82573 is compatible with many sizes of 4-wire SPI EEPROM devices. The required EEPROM size is dependent upon the manageability platform. The 82573 accesses the EEPROM at a frequency of 2 MHz and supports EEPROM devices from STM*, SST*, and Chingis*.

The 82573 can operate with an SPI Flash as a stand alone device or shared device with the system BIOS. The Flash size is selected by the system integrator according to its usage. However, a minimum 4-Mb Flash is required for Intel® AMT support.

Table 1. EEPROM / Flash Configuration Size

Configuration	Minimum NVM Size	Memory Family
ASF or APT Manageability	64 Kb	SPI EEPROM
No Manageability (Intel® AMT, ASF or APT)	1 Kb	SPI EEPROM
Shared Flash with Intel® AMT (82573E only)	8 Mb to 16 Mb total The minimum requirement for Intel® AMT is 4 Mb.	SPI Flash
Shared Flash without Intel® AMT	8 Mb to 16 Mb total for mobile 4 Mb to 16 Mb total for desktop 128 Kb (minimum) is reserved for the LAN image.	SPI Flash
Dedicated Flash with Intel® AMT (82573E only)	4 Mb	SPI Flash
Dedicated Flash without Intel® AMT	128 Kb	SPI Flash

Table 2. Compatible EEPROM Parts

Vendor	1 Kb
Atmel*	AT25010N-10SI-2.7
STM*	95010WMN6
Catalyst*	CAT25010S

Table 3. Compatible Flash Parts

Vendor	4 Mb	8 Mb	16 Mb
ST Micro*	25PE40[1], M45PE40[2]	25PE80[1], M45PE80[2]	
Chingis*	PM25LV040		
SST*	25VF040B 25LF040A	25VF080B	25VF016B

1. ST Micro* parts can only be used with non-Intel® AMT Systems.
2. These parts have been fully tested but are not pin compatible with the other Flash components listed in this table.

In a shared Flash, 82573 implements SPI arbitration with the ICH. At any size, the 82573 has the following requirements from the Flash: block erase instruction of 4 KB or 256 bytes with the Flash supporting the Read Device ID instruction that enables software to identify an empty device type. The 82573 drives the Flash at a frequency of approximately 15.6 MHz and supports devices from STM*, SST*, and Chingis*. (Intel is currently working with these SPI Flash vendors. More details can be obtained through your technical representative.) The following table lists existing Flash devices and their specifications.

Note: Additional 8 Mb and 16 Mb Flash parts will become available in early 2007 and will be validated for use with the 82573 GbE controller. Consult your local Intel representative for availability information.

Table 4. Specifications for Flash Devices

	STM* Family	SST* Family	Chingis* Family
Size (bytes)	0.5 Mb, 1 Mb	0.5 Mb, 1 Mb, 2 Mb	64 KB, 128 Kb
Maximum Write Burst Size (Word 4Ah, bit 5) Sector Size	256 byte	1 byte	256 bytes
Minimum Block Erase Size (Word 12h, bits 3:2) Sector Size	256 bytes	4 Kb	4 Kb
Device Erase Instruction (Word 4Ah, bits 15:8) Sector Size	-	60h	C7h
Minimum Block Erase Instruction (Word 11h, bits 15:8) Sector Size	DBh	20h	D7h

1.2 NVM Device Detection

82573 detects the device connected on the SPI interface in two phases:

1. It first detects the device type by the state of the NVM Type (NVMT) strapping pin.
2. It looks at the NVM content depending on a valid signature in word 12h of the NVM device.

1.2.1 CRC Field

In ASF Mode, the 82573 ASF function reads the ASF CRC word to determine whether the EEPROM is valid. If the CRC is not valid, the ASF configuration registers retain their default value. This CRC does not affect any of the remaining 82573 configuration, including the Management Control Register.

1.3 Device Operation with EEPROM

When the 82573 is connected to an external EEPROM it provides similar functionality to its predecessors with the following enhancements:

- Enables a complete parallel interface for reads and writes to the EEPROM.
- Enables software to explicitly specify the address length, eliminating the need for bit clocking accesses even with an empty EEPROM.

1.4 Device Operation with Flash

The 82573 merges the legacy EEPROM and Flash content in a single Flash device. This mechanism provides a seamless backwards compatible interface for the software and firmware to the legacy EEPROM space. This also enables the 82573 to share the BIOS content with the LAN content on the same device at separate regions.

The 82573 supports Flash devices with block erase size of 256 bytes and 4 Kb. The 82573 firmware relates to logical sectors of 4 Kb regardless of the block erase size.

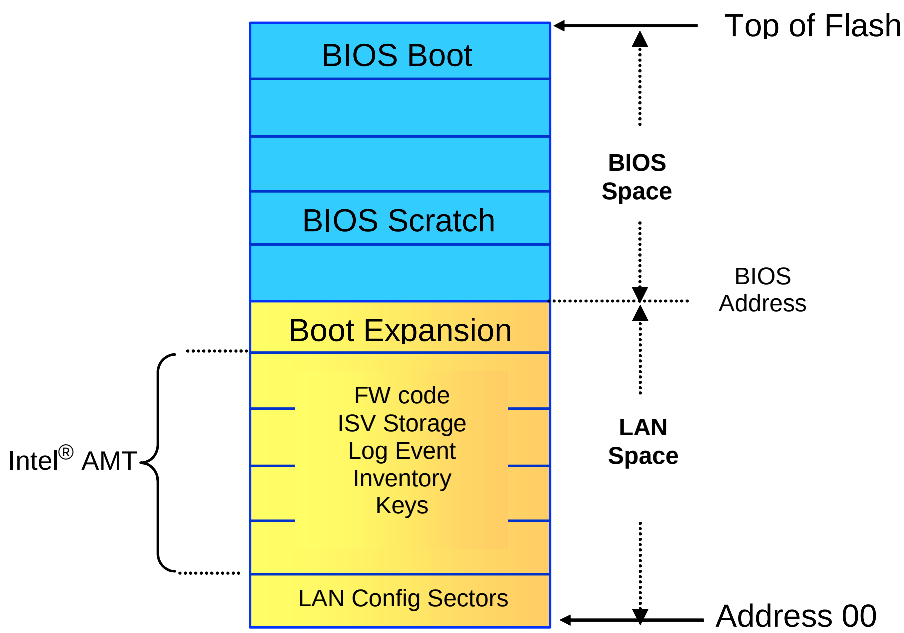
Note: Many Flash vendors use the term sector differently. For purposes of this document, the term Flash sector refers to a logic section of 4 Kb.

In a shared Flash, the LAN data and BIOS content reside side by side. Each entity spans across non-overlapping regions and sectors. The BIOS is located at the top of the Flash and the LAN content is located at the bottom of the Flash. Figure 1 shows the Flash memory mapping of LAN and BIOS regions.

1.4.1 Shadow RAM

The 82573 uses shadow RAM to minimize the number of times the Flash is read. The Flash is read once into shadow RAM at power up and is not read again until the next power up. During normal operation and when the 82573 resumes from any Sx state, the shadow RAM is used instead of the Flash.

Figure 1. Flash Mapping of the LAN and BIOS Regions



1.5 EEPROM Mode

When an external EEPROM is present any access to the EEPROM interface is directed to the external EEPROM device.

1.6 NVM Clients

Several client systems can access the NVM through their software driver, BIOS, firmware and hardware. Table 5 lists the systems and their interfaces.

Table 5. NVM Client Interface

Client & Interface	NVM Port	NVM Instruction
Host CPU on EEC CSR	EEPROM	Legacy bit clocking.
Host CPU on EERD and EEWR	EEPROM	Parallel word read and write to EEPROM (controlled by the EEC.SELSHAD bit).
MNG on EEMNG CSR	EEPROM	Parallel word read and write to EEPROM.
Host CPU on FLA CSR	Flash	Flash erase instructions (only for non-protected Flash).[1], [2]
MNG on DMA Engine	Flash	Read and write DMA to the Flash and Block Erase.[1]
MNG via the cache	Flash	Code fetch and data read. Access to FL1 and FL2 spaces.
Host CPU via BAR	Flash	Read byte word and Dword and byte programming.[1]
Host CPU via FLSWxxx CSR registers	Flash	Host write access to the Flash.
Direct hardware accesses	Both	

1. After a write or erase instruction to the Flash, the 82573 initiates a seamless write enable before the write or erase instruction is executed and polls the status at the end to verify its completion.
2. Bit clocking access and device erase are enabled only for non-protected Flash devices.

1.7 Flash NVM Protection Scheme

The 82573 Flash protection protects the BIOS area and Intel® AMT in shared Flash configurations in Intel® AMT enabled systems. Systems that do not share the Flash with the ICH or include Intel® AMT functionality do not require the Flash device protection.

The 82573 Flash device is protected when a valid image has been programmed onto the device and the protection mechanism has been switched on. Once the security mechanism is invoked, it might only be overridden by setting the NVM_PROT strapping pin to 0. A jumper can be installed to physically disable the protection. The jumper must be connected to NVM_PROT pin A5. (The *Intel® 82573 Family of GbE Controllers Datasheet* and the *Intel® 82573/82562 Dual Footprint Design Guide* can be used for reference.)

When the Flash device is programmed by an external Flash burner for shared Flash configurations, setting word 10h bits 5:4 to 11b ensures the protection mechanism is enabled. Bit 4 enables the Flash vendor identification, which adapts the image according to the installed Flash part, and bit 5 enables the protection.

The EEUPDATE program can be used to program a blank Flash when it is not protected using the No Protection (NoProt) flag. The No Protection flag disables protection.

The BADDR value in word 11h enables BIOS protection on shared Flash configurations. This value sets the highest address that the LAN device might read or write. BADDR should be set to the highest address of the LAN image on a protection enabled Flash image.

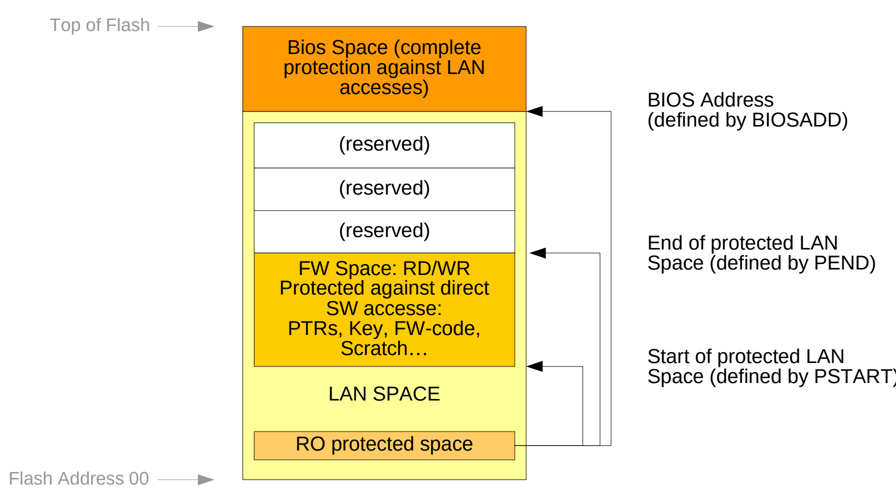
When the Flash is protected, the legacy LAN image, except word 10h, 11h, and 12h, can be updated using the EEUPDATE tool. EEUPDATE does not have the ability to modify the Intel® AMT Flash component. This is updated using the Intel® AMT network interface through the tftp server or the Intel® AMT Firmware Update tool (available in the 82573E software release).

Table 6. Protected Spaces

Space	Conditions	Protected Space Behavior
Device Protected	NVPROTN 12h[4] = 0 NVM_PROT samples 1 NVM Signature is valid 12h[15:8] = 7Eh	Legacy bit clocking is disabled. The Flash Erase is not propagated to the Flash. Protected spaces are enabled and some CSR are read only.
Words 11h and 12h	Device Protected	Host software or firmware cannot write to these addresses in the EEPROM, Flash S0, Flash S1, or Shadow RAM.
Word 10h	Device Protected	Host software cannot write to this address in the EEPROM, Flash S0, Flash S1, or Shadow RAM.
Intel® AMT Protected Space [1]	Device Protected PEND 10h is not equal to 0 NVM_Type samples 0 (equals Flash)	For the 82573E, host software cannot access (read or write) this area of protected space. This space is defined by PSTART and PEND fields in word 10h.
BIOS Protected Space	Device Protected BADDR is not equal to 0 NVM_Type samples 0 (equals Flash)	Host software and firmware cannot access (read or write) any address above BADDR. BADDR is valid for shared Flash with the BIOS as well as non-shared setup.

1. This protected space is defied only by Intel® AMT mode (all other spaces might exist at any operation mode). At this mode the PEND pointer in the NVM word 10h should have a valid (null) value while the PSTART pointer in the same location defines the beginning of the Intel® AMT protected space. In ASF mode, the PEND should have a null value while the PSTART defines the starting address of the ASF space.

Figure 2. NVM Protected Space Mapping



1.7.1 Initial Programming for Shared Flash with ICH

The Flash device should be programmed using an external Flash burner. The image must be combined including the LAN and BIOS components. The LAN image programmed using the external burner should have word 10h bit 4 set to 1b. This ensures that firmware identifies the Flash device and re-configures the image accordingly when the 82573 powers up from the default image (no Flash vendor specific configuration). Setting word 10h bit 5 to 1b enables the Flash protection mechanism.

For the 82573E, in a shared Flash configuration, the Intel® AMT component cannot be updated or modified using tools such as EEUPDATE after the initial programming cycle. The Intel® AMT component can only be updated using the firmware update application.

1.7.2 Initial Programming for Non-Shared Configurations

EEUPDATE can be used to program a blank Flash and update a valid Flash image. EEUPDATE is unable to update a Flash image if protection has been enabled without installing an override jumper.

1.8 EEUPDATE Utility

Intel has created a DOS* utility that meets the two basic requirements for an in-circuit programming utility. First, the utility can be used to update EEPROM images as part of an end-of-line production tool. Secondly, it can be used as a standalone development tool. The tool uses the two basic data files outlined in the following section (static data file and IA address file). To obtain a copy of this program, contact your Intel representative.

The EEUPDATE utility is flexible and can be used to update the entire EEPROM image or update only the IA address of the 82573.

Note: EEUPDATE can only be used to program the image in non-shared mode. Programming in shared mode requires the use of an external programmer.

1.8.1 Command Line Parameters

The DOS* command format is a follows:

```
EEUPDATE Parameter_1 Parameter_2 Parameter 3
```

where:

```
Parameter_1 = filename or /D

Parameter_2 = filename or /A

Parameter_3 = /noprot
```

`Parameter 1`, in this example case, is `file1.eep`, which contains the complete EEPROM image in a specific format that is used to update the complete EEPROM. All comments in the `.eep` file must be preceded by a semicolon (;).

`Parameter 1` can also be a switch, “/D.” The switch /D means, “Do not update the complete EEPROM image.”

`Parameter 2`, in this example case, is `file2.dat`, which contains a list of IA addresses. the EEUPDATE utility picks up the first unused address from this file and uses it to update the EEPROM. An address is marked as used by following the address with a date stamp. When the utility uses a specific address, it updates that address as used in a log file called eelog.dat. This file should then be used as the `.dat` file for the next update.

`Parameter 2` can also be a switch, “/A.” The switch /A implies, “Do not update the IA address.”

The following flags are defined as follows:

```
/D <imagefile> or /DATA <imagefile>
```

This programs the EEPROM with the contents of <imagefile> without changing the MAC address.

```
/A <addrfile> or /address <addrfile>
```

This programs the EEPROM with only the MAC address from the <addrfile> without changing the rest of the EEPROM.

```
/NOPROT
```

This disables protection while an image is being programmed. This switch has no effect if it is not used with the /data command.

See Appendix A for an example of the raw EEPROM contents.

2.0 NVM Memory Map

The NVM contains two regions located at fixed addresses and various regions located at programmable addresses throughout the physical NVM space.

The NVM base area resides at word addresses 00h through 3Fh. All defined fields are fixed, while reserved words can be used by programmable areas. The base area is present in the NVM of all system configurations. Words 10h through 12h of the base area are protected.

The base area at 40h to 4Fh contains additional configuration that is applicable and loaded only when the Base Area 40h bit is set in Initialization Control Word 1. This area has fixed locations for its fields and contains Flash and Intel® AMT (for the 82573E device only) configuration data.

The programmable areas are as follows:

- An optional Preboot eXecutable Environment (PXE) configuration area resides in word addresses 30h to 3Fh of the base area. A pointer at address 3Dh indicates the Boot Configuration area.
- These words within the base area provide a pointer to the optional manageability area, which can serve either ASF or Intel® AMT. (Intel® AMT is only available on the 82573E.)
  - — When the 82573E/V is configured to ASF mode in the Management Capabilities word, the Start Address (PSTART) points to the beginning of the ASF configuration area.
  - — When the 82573E is configured for Intel® AMT in the Management Capabilities word, the Start Address (PSTART) points to the beginning of the Intel® AMT programmable configuration area. The Base Area 40h is also enabled and loaded when Intel® AMT is enabled. The BADDR field in the protected area indicates the beginning of the BIOS code. This field is relevant only in a shared NVM configuration.

2.1 Basic Configuration Table

The following table lists the NVM map for words 00h through 3Fh of the 82573. Each word listed is described in the sections that follow.

Table 7. 82573 NVM Map for Address Range 00h to 3Fh (Sheet 1 of 2)

Word	Used By	High Byte Bits 15:8	Low Byte Bits 7:0
00h 01h 02h	HW HW HW	Ethernet Address Byte 2 Ethernet Address Byte 4 Ethernet Address Byte 6	Ethernet Address Byte 1 Ethernet Address Byte 3 Ethernet Address Byte 5
03h 04h 05h 06h 07h		Compatibility High	Compatibility Low
08h 09h	SW	PBA, byte 1 PBA, byte 3	PBA, byte 2 PBA, byte 4
0Ah	HW	Initialization Control 1	
0Bh	HW	Subsystem ID (Vendor)	
0Ch	HW	Subsystem Vendor ID	
0Dh	HW	Device ID	
0Eh	HW	Vendor ID	
0Fh	HW	Initialization Control 2	
10h	HW	NVM Word 0 (NVM0)	
11h	HW	NVM Word 1 (NVM1)	
12h	HW	NVM Word 2 (NVM2)	
13h	HW	Management Enable	Management Capabilities
14h	HW	Extended Configuration Word 1	
15h	HW	Extended Configuration Word 2	
16h	HW	Extended Configuration Word 3	
17h	HW	Reserved	Memory Scrub Control
18h	HW	PCI Express* (PCIe*) Initial Configuration 1	
19h	HW	PCIe Initial Configuration 2	
1Ah	HW	PCIe Initial Configuration 3	
1Bh	HW	PCIe Control	
1Ch	HW	PHY Configuration	LEDCTL 1 Default
1Dh	HW	Reserved	
1Eh	HW	Device Revision ID	
1Fh	HW	LEDCTL 0 and 2 Default	
20h	HW	Firmware Bits	
21h		Reserved	
22h	HW	LAN Power Consumption	
23h	SW	Flash Software Detection	
24h	HW	Initialization Control 3	

Table 7. 82573 NVM Map for Address Range 00h to 3Fh (Sheet 2 of 2)

Word	Used By	High Byte Bits 15:8	Low Byte Bits 7:0
25h 26h 27h 28h 29h 2Ah 2Bh 2Ch 2Dh 2Eh 2Fh		Reserved	
30h 31h 32h 33h 34h ... 3Eh	PXE	PXE Word 0 (Software Use) Configuration PXE Word 1 (Software Use) Configuration PXE Word (Software Use) PXE Version PXE Word (Software Use) EFI Version PXE Word ... PXE Word	
3Fh		Software Checksum, words 00h through 3Fh	

2.1.1 Ethernet Address (Words 00h-02h)

The Ethernet Individual Address (IA) is a six-byte field that must be unique for each Ethernet port and unique for each copy of the NVM image. The first three bytes are vendor specific. The value from this field is loaded into the Receive Address Register 0 (RAL0/RAH0). An example is provided in the table below for the Ethernet address of: 12 34 56 78 90 ABh.

Table 8. MAC Address Example

Word	Value Loaded
0	3412h
1	7856h
2	AB90h

Note: The values are byte-swapped.

2.1.2 Compatibility Field (Word 03h-07h)

This area is reserved for compatibility information to be used by software drivers.

Table 9. Compatibility Field (Word 03h)

Bit	Name	Default	Description
15:13	Reserved	000b	These bits are reserved and should be set to 000b.
12	ASF SMBus Connect		This bit identifies whether or not the ASF SMBus is connected. 0b = ASF SMBus is not connected. 1b = ASF SMBus is connected.
11	LOM Design		This bit identifies whether or not the implementation is a LAN on Motherboard (LOM) design or not. 0b = Network Interface Card (NIC) 1b = LOM design (default)
10	Server NIC		This bit identifies whether or not the system is a server or a client. 0b = Client 1b = Server
9	Client NIC		This bit identifies whether or not the system is a server or a client. 0b = Server 1b = Client
8	Retail/OEM		This bit identifies a retail or OEM status. 0b = Retail 1b = OEM
7:6	Reserved		These bits are reserved and should be set to 0b.
5	Reserved		This bit is reserved and should be set to 1b.
4	SMB Connect		This bit identifies whether or not the SMB is connected. 0b = SMB is not connected. 1b = SMB is connected.
3	Reserved		This bit is reserved and should be set to 0b.
2	PCI Bridge Present		This bit identifies whether or not a PCI bridge is present. 0b = PCI bridge is not present. 1b = PCI bridge is present.
1:0	Reserved		These bits are reserved and should be set to 00b.

Table 10. Compatibility Field (Word 04h)

Bit	Name	Default	Description
15:12	Reserved		These bits are reserved and should be set to 0000b.
11:8	LED 2 Control		This field is the control for LED 2.
7:4	LED 1 Control		This field is the control for LED 1.
3:0	LED 0 Control		This field is the control for LED 0.

Table 11. Compatibility Field (Word 05h)

Bit	Name	Default	Description
15:8	EEPROM Major Version		This field contains the major version number of the EEPROM.
7:0	EEPROM Minor Version		This field contains the minor version number of the EEPROM.

Table 12. Compatibility Field (Word 06h)

Bit	Name	Default	Description
15:0	OEM Configuration		This word is used for OEM configuration.

Table 13. Compatibility Field (Word 07h)

Bit	Name	Default	Description
15:0	OEM Configuration		This word is used for OEM configuration.

2.1.3 PBA Number (Word 08h-09h)

A nine-digit Printed Board Assembly (PBA) number, used for Intel manufactured NICs, are stored in a four-byte field. Other hardware manufacturers can use these fields as desired. Network driver software should not rely on this field to identify the product or its capabilities.

2.1.4 Initialization Control Word 1 (Word 0Ah)

This is the first word read by the 82573 and contains initialization values that:

- Set defaults for some internal registers.
- Enable/disable specific features.
- Determine which PCI configuration space values are loaded from the NVM.

Table 14. Initialization Control Word 1 (Word 0Ah) (Sheet 1 of 2)

Bit	Name	Default	Description
15	Link Status Change Wake Enable	0b	This bit enables wake on link status change as part of APM wake capabilities. It is not read automatically by the hardware. Software reads the NVM and writes it to hardware.
14	Link Status Change Wake Override	0b	If this bit equals 1b, the wake on link status change does not depend on the LNKC bit of the Wake Up Filter Control Register (WUFC). The wake on link status change is determined by the APM settings in the Wake Up Register. This bit is not read automatically by the hardware. Software reads the NVM and writes it to hardware.
13	Base Area 40h	1b	When this bit is set, it indicates that the Base Area starting at address 40h must be loaded from the NVM.
12	Reserved	0b	This bit is reserved and must be set to 0b.
11	FRCSPD	0b	This bit reflects the Force Speed bit in the device Control Register (CTRL[11]). When it is set to 1b, the speed is forced. When it is 0b, it does not force speed.
10	FD	0b	This bit reflects the duplex setting. It is mapped to the Control Register bit 0. It has a hardware reset value of 1b. When it is set to 1b, full duplex is enabled. When it is set to 0b, full duplex is disabled.
9	Reserved	1b	This bit is reserved and should be set to 1b.
8:7	Reserved	00b	These bits are reserved and should be set to 0bb.
6	Mask g_fnc_tar_g MSB	1b	When this bit is set to 1b, the most significant bit of g_fnc_tar_g is masked by the EEPROM or Flash.

Table 14. Initialization Control Word 1 (Word 0Ah) (Sheet 2 of 2)

Bit	Name	Default	Description
5	Reserved	1b	This bit is reserved and should be set to 1b.
4	ILOS	0b	This bit represents the default setting for the loss of signal polarity setting of Control Register bit 7. The hardware default value is 0.
3	Power Management	1b	When this bit is set to 1b (default), full support for power management is enabled. When it is set to 0b, the power management register settings are read only, and the 82573 does not execute a hardware transition to D3.
2	Reserved	0b	This bit is reserved and should be set to 0b.
1	Load Subsystem IDs	1b	When this bit is set to 1b (default), it indicates that the device needs to load its PCIe) Subsystem ID and Subsystem Vendor ID from the NVM (words 0Bh and 0Ch). When it is set to 0b, the device loads the default PCI Subsystem ID and Subsystem Vendor ID.
0	Load Vendor/Device IDs	1b	When this bit equals 1b, the device loads the default values for PCIe Vendor and Device IDs from the NVM (words 0Dh and 0Eh).

2.1.5 Subsystem ID (Word 0Bh)

If Load Subsystem IDs bit of word 0Ah is valid, this word is read in to initialize the Subsystem ID. The Subsystem ID default value is 0h.

2.1.6 Subsystem Vendor ID (Word 0Ch)

If Load Subsystem IDs bit of word 0Ah is valid, this word is read in to initialize the Subsystem Vendor ID. The Subsystem Vendor ID default value is 8086h.

2.1.7 Device ID (Word 0Dh)

If the Load Vendor/Device IDs bit in word 0Ah is set, this word is read to initialize the Device ID of the LAN function. 108Bh is used for a basic 82573 based design, and 108Ch for a design based on the 82573E with Intel® AMT.

Table 15. Device ID Values

Vendor ID	Device ID	String Name
8086h	108Bh	Intel® PRO/1000 PM Network Connection (82573 based design)
8086h	108Ch	Intel® PRO/1000 PM Network Connection (82573E based design with Intel AMT)
8086h	109Ah	Intel® PRO/1000 PM Network Connection (82573L based design)

Note: The Vendor ID for Intel is always 8086h.

2.1.8 Vendor ID (Word 0Eh)

If the Load Vendor/Device IDs bit in word 0Ah is set, this word is read to initialize the Vendor ID. The default Vendor ID value is 8086h.

2.1.9 Initialization Control Word 2 (Word 0Fh)

This is the second word read by the 82573 and contains additional initialization values that:

- Set defaults for some internal registers.
- Enable or disable specific features.

Table 16. Initialization Control Word 2 (Word 0Fh)

Bit	Name	Default	Description
15	APM PME# Enable	1b	This bit reflects the initial value of the Assert PME On APM Wakeup bit in the Wake Up Control Register (WUC.APMPME). When it is set to 0b, PME# is de-asserted on wakeup.
14	Reserved	0b	This bit is reserved and should be set to 0b.
13:12	NVMTYPE	00b	These bits indicate the type of NVM present. 00b = EEPROM 01b = Stand alone Flash 10b = SPI Flash 11b = Reserved
11:8	NVSIZE	0000b	When the NVM is a Flash device, the NVSIZE should be greater than or equal to 9 (the minimum supported Flash size is 64 KB).
7	CLK_CNT_1_4	1b	This bit enables the automatic reduction of the DMA frequency. It is mapped to the Status Register bit 30.
6	PHY Power Down Enable	1b	When this bit is set, the PHY can enter a low power state.
5	MAC_CSR_MNG	0b	When this bit is set, the mng_mac_csr FSM is reset on IN_BAND PCIe* reset or PERST. When it is cleared, the FSM is reset on a soft reset.
4	CCM PLL Shutdown Enable	1b	When this bit is set, the CCM PLL shuts down in low power states when the PHY is in power down mode (for example, during a link disconnect). When it is cleared, the CCM PLL does not shut down in a low power state.
3	DMA Dynamic Gating Enable	1b	When this bit is set, dynamic clock gating of the DMA and MAC units is enabled.
2	Clock Power Management	0b	For the 82573L, a value of 1b indicates that the device supports the removal of any reference clocks when the link is in the L1 and L2/3 ready link states. A value of 0b indicates that the device does not have this capability; therefore, reference clocks must not be removed in these link states. This feature is only applicable in designs that support the clock request signal (CLKREQ#). For a multi-function device, each function indicates its capability independently. Power management configuration software must only permit reference clock removal if all functions of the multi-function device indicate a 1b in this bit. **Note:** For the 82573E and 82573V, this bit is reserved and should be set to 1b.
1	Wake DMA Dynamic Clock Gating Disable	1b	When this bit is set, dynamic clock gating of the wake DMA clock is disabled in the D0a state with wakeup enabled or MNG enabled or in the auto-read process.
0	D0a DMA Dynamic Clock Gating Disable	0b 1b[1]	When this bit is set, dynamic clock gating of the DMA clock in the D0a state is disabled.

1. **82573E/V** only.

2.1.10 NVM Word 0: NVM0 (Word 10h)

Note: NVM0 is used by Intel® AMT and is not applicable to the 82573V and 82573L devices.

Table 17. NVM Word 0 (Word 10h)

Bit	Name	Default	Description
15:8	PEND	00h	This field defines the end of the protected space plus one. The address is defined as: Protected End Word Address = 4 KB * PEND. A zero value is a null pointer, which means that the space defined by PSTART and PEND is not protected. A value of one is invalid.
7	ICH7 (Check for Intel AMT Disable)	0b	This firmware configuration bit is only for the A1 stepping of the device and is not accessed by hardware. For the A3 silicon, this bit must be set to 0b. 1b = ICH7 check for Intel® AMT mode disable. 0b = ICH7 check for Intel® AMT mode enable.
6	Ignore Intel AMT Skew	0b	This firmware configuration bit is only for the A1 stepping of the device and is not accessed by hardware. For the A3 silicon, this bit must be set to 0b. 1b = Ignore Intel® AMT SKU. 0b = Don't ignore Intel® AMT SKU.
5	FW Protect Image	1b	This bit should be set when the initial programming is done on an external burner. This setting is used in conjunction with bit 4, Firmware Flash Vendor Identification. If bit 4 equals 0b, this bit is ignored. 0b = No protection. 1b = Firmware enables protection at first power up.
4	FW Flash Vendor Identification	0b	This bit determines whether the 82573 identifies the Flash and updates the image with appropriate opcodes. This bit should be set when the initial programming is done on an external burner. 0b = 82573 does not perform Flash Identification. 1b = 82573 performs Flash Identification at power up. The 82573 automatically clears this bit at the end of the Flash ID sequence so that it is only performed once.
3:2	MNGM	00b	This field selects one of the manageability operation modes. 00b = MNG disable mode (clock gated) 01b = ASF mode 10b = Pass through mode 11b = Intel® AMT mode[1]
1:0	PSTART		The protected start address field is used in Intel® AMT mode to define the starting address for this mode (PEND ≠ zero). 00b = Reserved 01b = 4 Kword 10b = Reserved 11b = Reserved In ASF mode, the PSTART defines the starting address of the ASF space (PEND = Zero). 00b = Word 40h 01b = Word 80h 10b = Reserved 11b = Reserved

1. When Intel® AMT is enabled, all MNG functions (KCS, Serial, IDE) should be enabled in word 49h of the NVM.

2.1.11 NVM Word 1: NVM1 (Word 11h)

Table 18. NVM Word 1 (Word 11h)

Bit	Name	Default	Description
15:8	FSECER	1111b 1111b	This field defines the instruction code for the block erase used by the 82573. The erase block size is defined by the SECSIZE field in address 12h.
7:0	BADDR	0000b 0000b	The BADDR defines the starting address of the BIOS space in a shared Flash as follows: BIOS Word Address = 4 KB * BADDR.

2.1.12 NVM Word 2: NVM2 (Word 12h)

Table 19. NVM Word 2 (Word 12h)

Bit	Name	Default	Description
15:8	Reserved	0111b 1110b	These bits are reserved.
7:4	Reserved for the 82573E/V	0001b	These bits are reserved and should be set to 0001b for the 82573E/V.
7:4	Reserved for the 82573L	0101b	These bits are reserved and should be set to 0101b for the 82573L.
3:2	SECSIZE	01b	The Flash sector size is defined as: 00b = 256 bytes. 01b = 4 KB 10b = Reserved 11b = Reserved
1:0	Reserved	0b	These bits are reserved and should be set to 00b.

2.1.13 Management Enable (Word 13h, High Byte)

This byte contains information for firmware that has manageability functionality enabled. After updating this byte, the software device driver should notify the firmware of the change. If the manageability subsystem is in a mode where its host interface is functional, then it should be done by a manageability host command. If the host interface is not functional, then the software device driver should wake the manageability subsystem by asserting the WMNG bit in the SWSM register.

Table 20. Management Enable Byte (Word 13h, High Byte)

Bit	Name	Default	Description
15:9	Reserved	00h	These bits are reserved and should be set to 00h.
8	MNG Mode	0b	0b = None 1b = ASF mode Other values are reserved.

Note: If the additional PCI functions (KCS, IDE, COM) are enabled in the NVM, it indicates to the firmware that their relevant functionality is enabled.

2.1.14 Management Capabilities (Word 13h, Low Byte)

This byte contains the device manageability capabilities. This word is for the device software only. It should not enable any capability (in the high byte) that is not enabled in this byte. The OEM is responsible for initializing this byte.

Table 21. Management Capabilities Byte (Word 13h, Low Byte)

Bit	Name	Default	Description
7	Reserved	0b	This bit is reserved and should be set to 0b.
6	Manageability Capable	0b	When this bit is set, it indicates that settings in bits 5:0 are applicable.
5	IDE Redirection Capable	0b	When this bit is set, it indicate that the device supports IDE redirection functionality if it is enabled.
4	COM Capable	0b	When this bit is set, the device supports COM functionality if it is enabled.
3	Pass Through Capable	0b	When this bit is set, the pass through functionality is enabled.
2	Reserved	0b	This bit is reserved and should be set to 0b.
1	ASF 2 Capable	0b	When this bit is set, ASF 2 functionality is enabled.
0	ASF 1 Capable	0b	When this bit is set, ASF 1 functionality is enabled.

2.1.15 Extended Configuration Word 1 (Word 14h)

Table 22. Extended Configuration Word 1 (Word 14h)

Bit	Name	Default	Description
15:13	Reserved	000b	These bits are reserved and should be set to 000b.
12	Wake Behavior	0b	This field defines behavior of the WAKE# signal. WAKE# signal behaves as specified in the PCIe* Specification. WAKE# must always be asserted on PME. (This is asserted in all system modes.)
11:0	Reserved	00h	These bits are reserved and should be set to 00h.

2.1.16 Extended Configuration Word 2 (Word 15h)

Table 23. Extended Configuration Word 2 (Word 15h)

Bit	Name	Default	Description
15:0	Reserved	00D8h	This field is reserved and should be set to 00D8h.

2.1.17 Extended Configuration Word 3 (Word 16h)

Table 24. Extended Configuration Word 3 (Word 16h)

Bit	Name	Default	Description
15:0	Reserved	00h	These bits are reserved and should be set to 00h.

2.1.18 Memory Scrub Control / PCIe* Delay (Word 17h)

Table 25. Memory Scrub Control / PCIe Delay (Word 17h)

Bit	Name	Default	Description
15:13	Reserved	000b	These bits are reserved and should be set to 000b.
12:8	Electrical Idle Delay	00111b	This field identifies the delay cycles before entering the electrical idle allowing data path flush. The default value for this field is 7h.
7:0	Reserved	00h	These bits are reserved and should be set to 00h.

2.1.19 PCIe* Initial Configuration Word 1 (Word 18h)

This field:

- Sets the default values for some internal registers.
- Enables and disables specific features.

Table 26. PCIe Initial Configuration Word 1 (Word 18h)

Bit	Name	Default	Description
15	Reserved	0b	This bit is reserved and should be set to 0.
14:12	L1 Active Exit Latency	110b	This field represents the L1 active exit latency for the Configuration Space. The default value equals 32 µs to 64 µs (110b).
11:9	L1 Active Acceptance Latency	110b	This field represents the L1 active acceptable latency for the Configuration Space. The default value equals 32 µs to 64 µs (110b).
8:6	L0 Active Acceptance Latency	110b	This field represents the L0 active acceptable latency for the Configuration Space. The default value equals 32 µs to 64 µs (110b).
5:3	L0 Separated Exit Latency	001b	This field represents the L0 exit latency for the active power state with a separated reference clock. The latency range is 64 ns to 128 ns.
2:0	L0 Common Exit Latency	001b	This field represents the L0 exit latency for the active power state with a common reference clock. The latency range is 64 ns to 128 ns.

2.1.20 PCIe* Initial Configuration Word 2 (Word 19h)

This word sets the default values for some of the internal registers.

Table 27. PCIe Initial Configuration Word 2 (Word 19h)

Bit	Name	Default	Description
15	DLLP Timer Enable	0b	When this bit is set, the DLLP timer counter is enabled.
14	DISMN2CSR	0b	The assertion of this bit disables a read or write transaction to the CSR from MNG. The default value of 0b enables the MNG to access the CSR.
13	Device Type	1b	This bit defines the device type reported in the PCIe* Capability register of the IDE function. 1b = Legacy End Point 0b = Native End Point DEVTYPE must be set to 1b since all other functions are defined as native devices.

Table 27. PCIe Initial Configuration Word 2 (Word 19h)

Bit	Name	Default	Description
12	Reserved	1b	This bit is reserved and should be set to 1b.
11:8	Extra NFTS	0001b	This field represents the Extra Number of Fast Training Signal (NFTS), which is added to the original requested number of NFTS (as requested by the upstream component).
7:0	NFTS	0011b 0000b	This field defines the number of special sequences for L0s transition to L0. The default value for this field is 50h.

2.1.21 PCIe* Initial Configuration Word 3 (Word 1Ah)

This word sets the default values for some of the internal registers.

Table 28. PCIe Initial Configuration Word 3 (Word 1Ah)

Bit	Name	Default	Description
15	Master Enable	0b	When this bit is set to 1b, it enables the PHY to be a bus master (upstream component/cross link functionality).
14	Scrambling Disable	0b	This bit disables the PCIe* LFSR scrambling when it is set to 1b.
13	Ack/Nack Scheme	0b	This bit define the Acknowledge/Not Acknowledged scheme: 0b = Scheduled for transmission following any TLP. 1b = Scheduled for transmission according to time-outs specified in the PCIe* specification.
12	Cache Line Size	0b	This bit identifies the cache line size. 0b = 64 bytes 1b = 128 bytes The value loaded must be equal to the actual cache line size used by the platform configured by system software.
11:10	Reserved	01b	These bits are reserved and should be set to 01b.
9	IO Support	1b	This bit identifies whether I/O is supported. 0b = I/O not supported 1b = I/O supported
8	Packet Size	1b	This bit indicates the packet size. 0b = 128 bytes (default) 1b= 256 bytes
7:6	Reserved	00b	These bits are reserved and should be set to 00b.
5	Elastic Buffer Control	1b	When this bit is set to 1b, the elastic buffers are activated in a mode that enables phase setting only during electrical idle states.
4	Elastic Buffer Diff	0b	When this bit is set to 1b, the elastic buffers are activated in a more limited mode.
3:2	Active State PM Support	11b	This bit determines support for Active State Link Power Management. It is loaded into the PCIe* Active State Link PM Support register.
1	Slot Clock Configuration	1b	When this bit is set, the 82573 uses the PCIe* reference clock supplied on the connector for add-in solutions.
0	Loopback Polarity Inversion	0b	This bit indicates the polarity inversion in loopback master entry.

2.1.22 PCIe* Control (Word 1Bh)

This word configures initial settings for the PCIe* default functionality.

Table 29. PCIe Control (Word 1Bh)

Bit	Name	Default	Description
15	GIO Receive Valid	0b	This bit identifies if receiver presence is detected. When it is set, the 82573 overrides the receiver (partner) detection status.
14	Reserved	0b	For the 82573E and 82573V, this bit is reserved and should be set to 0b. For the 82573L, this bit is reserved and should be set to 1b.
13	GIO Down Reset Disable	0b	This bit enables the ability to disable a core reset when the PCIe* link goes down.
12	GIO LTSSM	0b	When this bit is cleared, LTSSM complies with the SlimPIPE specification (power mode transition). When it is set, LTSSM operates as in the 82571.
11	Extended FTS	0b	When this bit is set, the 82573 sets the Extended NFTS bit in TS1/ TS2 according to the PCIe* specification. Also, when the bit is set the upstream sends 4096 NFTS to 82573.
10	Leaky Bucket Disable	0b	This bit disables the leaky bucket mechanism in the PCIe* PHY. Disabling this mechanism holds the link from going to recovery retrain in the case of disparity errors.
9:6	Reserved	00h	This field is reserved and should be set to 00h.
5	L2 Disable	0b	This bit disables the link from entering the L2 state.
4	Skip Disable	0b	This bit disables the skip symbol insertion in the Elastic buffer.
3	L0s Clock Gate Enable	0b	This bit disables the clock gating when the device is entering the L0s state. Its default value is 0b, which disables clock gating. When it equals 1b, clock gating is enabled.
2	Electrical Idle Mask	0b	The Electrical Idle Mask bit checks for illegal electrical idle sequences (for example, an electrical idle may be set without common mode or vice versa) and masks them as correct sequences. The specification can be interpreted so that the idle ordered set is sufficient for transition to power management states. The use of this bit allows this interpretation and avoids the possibility of correct behavior being interpreted as an illegal sequence.
1:0	Latency to Enter L1	11b	This is defined as the period in the L0s state before the device transitions to an L1 state: 00b = 64 µs 01b = 256 µs 10b = 1 ms 11b = 4 ms

2.1.23 PHY Configuration (Word 1Ch, High Byte)

The high byte of this word contains the PHY configuration bits loaded to register 25 in page 0 of the PHY configuration space.

Table 30. PHY Configuration (Word 1Ch, High Byte)

Bit	Name	Default	Description
15	Reserved	0b	This bit is reserved and should be set to 0b.
14	Gigabit Disable	0b	When this bit is set, GbE operation is disabled in all modes.
13	Reserved	0b	This bit is reserved and should be set to 0b.
12	Class AB	0b	When this bit is set, the PHY operates in Class A mode rather than Class B mode. This mode only applies for 1000BASE-T operation. 10BASE-T and 100BASE-TX operation continues to run in Class B mode by default regardless of this signal value.
11	Disable Gigabit in Non-D0a	1b	This bit disables GbE operation in non-D0 active states.
10	LPLU	0b	This bit represents the low power link up status. When this bit is set, it enables the decrease in link speed in non-D0 active states when the power policy and power management states require it.
9	D0 LPLU	0b	This bit represents the low power link up status in D0 active states. When this bit is set, it enables the decrease in link speed in D0 active states when the power policy and power management states require it.
8	Reserved	1b	This bit is reserved and should be set to 1b.

2.1.24 LED Control Registers

The 82573 implements three output drivers intended to drive external LED circuits per port. Each of the three LED outputs can be individually configured to select the particular event, state, or activity, which are indicated on that output. In addition, each LED can be individually configured for output polarity as well as for blinking versus non-blinking (steady-state) indication.

The configuration for LED outputs is specified through the LED Control (LEDCTL) register. The hardware default configuration for all the LED outputs can be specified through the NVM fields, enabling the support or LED displays configurable to a particular OEM preference. (See Table 31, Table 32, and Table 33.)

Each of the three LEDs can be configured to use one of a variety of sources for output indication. The MODE bits control the LED source:

- LINK 100/1000 is asserted when link is established at either 100 Mb/s or 1000 Mb/s.
- LINK 10/1000 is asserted when link is established at either 10 Mb/s or 1000 Mb/s.
- LINK UP is asserted when any speed link is established and maintained.
- ACTIVITY is asserted when link is established and packets are being transmitted or received.
- LINK/ACTIVITY is asserted when link is established and there is no transmit or receive activity.
- LINK 10 is asserted when a 10 Mb/s link is established and maintained.
- LINK 100 is asserted when a 100 Mb/s link is established and maintained.

- LINK 1000 is asserted when a 1000 Mb/s link is established and maintained.
- FULL DUPLEX is asserted when the link is configured for full duplex operation.
- LED ON is always asserted. LED OFF is always de-asserted.

The invert bits allow the LED source to be inverted before being output or observed by the blink control logic. LED outputs are typically connected to the negative side (cathode) of an external LED.

The BLINK bits control whether the LED blinks while the LED source is asserted. The blinking frequency is either 200 ms on and 200 ms off or 83 ms on and 83 ms off. In Smart Power-Down Mode, the blinking durations are increased by 5x to 1 second and 415 ms, respectively. The blink control can be used to ensure that certain events (such as the ACTIVITY indication) cause LED transitions, which are sufficiently visible to the human eye. The same blinking rate is shared by all LEDs.

Note: The LINK/ACTIVITY source functions are slightly different from the others when BLINK is enabled. The LED are off if there is no link present and on if link is present without activity. The LED blinks if there is LINK and ACTIVITY.

2.1.24.1 LED 1 Configuration Defaults (Word 1Ch, Low Byte)

The low byte of word 1Ch of the NVM specifies the hardware defaults for the LED control register fields that determine LED1 output behaviors.

Table 31. LED 1 Configuration Defaults (Word 1Ch, Low Byte)

Bit	Name	Default	Description
7	LED1 Blink	1b	This bit indicates the initial value of the LED1_BLINK field. If it equals 0b, the LED is non-blinking.
6	LED1 Invert	0b	This bit indicates the initial value of the LED1_IVRT field. If it equals 0b, the LED has an active low output.
5	LED1 Blink Mode	0b	This bit defines the LED blink mode: 0b = Blink at 200 ms on and 200 ms off. 1b = Blink at 83 ms on and 83 ms off.
4	Reserved	0b	This bit is reserved and should be set to 0b.
3:0	LED1 Mode		These bits represent the initial value of the LED1_MODE field, which specifies the event, state, or pattern displayed on LED1 (ACTIVITY) output. A value of 0011b causes this to indicate the activity state.

2.1.24.2 LED 0 and 2 Configuration Defaults (Word 1Fh)

This NVM word specifies the hardware defaults for the LEDCTL register fields controlling the LED0 (LINK_UP) and LED2 (LINK_100) output behaviors.

Table 32. LED 0 and 2 Configuration Defaults (Word 1Fh)

Bit	Name	Default	Description
15	LED2 Blink	0b	This bit indicates the initial value of the LED2_BLINK field. If it equals 0b, the LED is non-blinking.
14	LED2 Invert	0b	This bit indicates the initial value of the LED2_IVRT field. If it equals 0b, the LED has an active low output.
13	LED2 Blink Mode	0b	This bit defines the LED blink mode: 0b = Blink at 200 ms on and 200 ms off. 1b = Blink at 83 ms on and 83 ms off.
12	Reserved	0b	This bit is reserved and should be set to 0b.
11:8	LED2 Mode		These bits represent the initial value of the LED2_MODE field, which specifies the event, state, or pattern displayed on LED2 (LINK_100) output. A value of 0110b causes this to indicate 100 Mbps operation.
7	LED0 Blink	0b	This bit indicates the initial value of the LED0_BLINK field. If it equals 0b, the LED is non-blinking.
6	LED0 Invert	0b	This bit indicates the initial value of the LED0_IVRT field. If it equals 0b, the LED has an active low output.
5	LED0 Blink Mode	0b	This bit defines the LED blink mode: 0b = Blink at 200 ms on and 200 ms off. 1b = Blink at 83 ms on and 83 ms off.
4	Reserved	0b	This bit is reserved and should be set to 0b.
3:0	LED0 Mode		These bits represent the initial value of the LED0_MODE field, which specifies the event, state, or pattern displayed on LED0 (LINK_UP) output. A value of 0010b causes this to indicate link up state.

Table 33. LED Control Source

Mode	Selected Mode	Source Indication
0000	Link 10/1000	Asserted when either a 10 Mb/s or a 1000 Mb/s link is established and maintained.
0001	Link 100/1000	Asserted when either a 100 Mb/s or a 1000 Mb/s link is established and maintained.
0010	Link Up	Asserted when any speed link is established and maintained.
0011	Reserved	Reserved.
0100	Link/Activity	Asserted when any speed link is established and when no transmit or receive activity is present.
0101	Link 10	Asserted when a 10 Mb/s link is established and maintained.
0110	Link 100	Asserted when a 100 Mb/s link is established and maintained.
0111	Link 1000	Asserted when a 1000 Mb/s link is established and maintained.
1000	Reserved	Reserved.
1001	Full Duplex	Asserted when the link is configured for full duplex operation.
1010	Reserved	Reserved.

Table 33. LED Control Source

Mode	Selected Mode	Source Indication
1011	Activity	Asserted when link is established and packets are being transmitted or received.
1100	Reserved	Reserved.
1101	Reserved	Reserved.
1110	LED On	Always asserted.
1111	LED Off	Always de-asserted.

Notes:
1. When LED Blink is enabled, the appropriate LED Invert Bit should be set to zero.
2. The dynamic LEDs modes (Link/Activity and Activity) should be used with LED Blink enabled.
3. When LED Blink is enabled and CCM PLL is shut, the blinking frequencies will be one-fifth of the rates stated in the table above.

2.1.25 Device Revision ID (Word 1Eh)

Table 34. Device Revision ID (Word 1Eh)

Bit	Name	Default	Description
15	Device Off Enable	1b	When this bit is set, the 82573 can enter the Device Disable mode and the Dr Disable mode. When it is cleared, both modes are disabled.
14	MNG Reset Fix Enable	1b	When this bit is asserted, the reset scheme change for Manageability Reset is enabled and the MNG block can access the CSR at Dr.
13:10	Reserved	0000b	These bits are reserved and should be set to 0000b.
9	Reserved	1b	This bit is reserved and should be set to 1b.
8	GIO D3 Gate	0b	This bit enables or disables GIO gate clocking in the D3 power state. This feature will be enabled in a future release of the device.
7:0	Reserved	00h	This field is reserved and should be set to 00h.

2.1.26 Firmware Configuration (Word 20h)

Table 35. Firmware Configuration (Word 20h)

Bit	Name	Default	Description
15	Power Save Enable	0b	This bit indicates whether power save is enabled. 0b = Power Save disabled. 1b = Power Save enabled.
14	IDE Register Enable	0b	This bit indicates whether the IDE registers are enabled. 0b = IDE firmware default mode is disabled (no IDE device). 1b = IDE firmware default mode is enabled (IDE device present).
13:1	Reserved	00h	These bits are reserved and should be set to 00h.
0	Force TCO Reset Disable	0b	This bit indicates whether a Force TCO Reset is enabled or disabled. 0b = LAN Force TCO enabled. 1b = LAN Force TCO disabled.

2.1.27 LAN Power Consumption (Word 22h)

This word is applicable only if the NVM signature in word 0Ah is valid and power management is enabled.

Table 36. LAN Power Consumption (Word 22h)

Bit	Name	Default	Description
15:8	LAN D0 Power		The value in this field is reflected in the PCI Power Management Data Register of the LAN function for D0 power consumption and dissipation (Data_Select = 0 or 4). Power is defined in 100 mW units and includes the external logic required for the LAN function.
7:5	Function 0 Common Power		The value in this field is reflected in the PCI Power Management Data Register of function 0 when the Data_Select field is set to 8 (common function). The most significant bits in the Data Register that reflects the power values are padded with zeros.
4:0	LAN D3 Power		The value in this field is reflected in the PCI Power Management Data Register of the LAN function for D3 power consumption and dissipation (Data_Select = 3 or 7). Power is defined in 100 mW units and includes the external logic required for the LAN function. The most significant bits in the Data Register that reflects the power values are padded with zeros.

2.1.28 Flash Software Detection Word (Word 23h)

Table 37. Flash Software Detection Word (Word 23h)

Bit	Name	Default	Description
15	Checksum Validity	0b	This bit indicates whether the checksum has been verified and updated by software. Software has not yet updated the checksum. Software has already updated the checksum.
14:8	Reserved		This field is reserved and all bits should be set to 1b.
7:0	Flash Vendor Detect		This field must have all bits set to 1.

2.1.29 Initialization Control Word 3 (Word 24h)

Table 38. Initialization Control Word 3 (Word 24h) (Sheet 1 of 2)

Bit	Name	Default	Description
15	APM Flexible Filter Allocation	0b	This bit is loaded to the APMFFA bit in the Wake Up Control Register (WUC) and allocates the flexible TCO1 filter for APM wake. It is read by firmware in to hardware.
14	Multiple Read Request Enable	1b	When this bit equals 0b, the 82573 initiates one transmit DMA request at a time. When it equals 1b, the 82573 can initiate up to four outstanding multiple transmit DMA requests. This bit sets the default value of the MULR bit in the TCTL register.
13	Reserved	1b	This bit is reserved and should be set to 1b.
12	Interrupt Pin	0b	This bit controls the value advertised in the Interrupt Pin field of the PCI Configuration header for this device and function. A value of 0b reflects that this device uses INTA#. A value of 1b indicates that this device uses INTB#.
11	Reserved	1b	This bit is reserved and should be set to 1b.

Table 38. Initialization Control Word 3 (Word 24h) (Sheet 2 of 2)

10	APM Enable	0b	This bit reflects the initial value of Advanced Power Management Wake Up Enable bit in the Wake Up Control Register (WUC.APME) and is mapped to CTRL[6] and to WUC[0].
9:1	Reserved	00h	These bits are reserved and should be set to 00h.
0	No PHY Reset for IDE		When this bit is asserted, PHY resets and the power changes reflected in the PHY, according to the MANC. BLK_PHY_RST value, are prevented.

2.1.30 PXE Words (Words 30h to 3Eh)

Words 30h through 3Eh have been reserved for configuration and version values to be used by Preboot eXecutable Environment (PXE) code.

2.1.30.1 Boot Agent Main Setup Options (Word 30h)

The boot agent software configuration is controlled by the EEPROM with the main setup options stored in word 30h. These options can be changed by using the Control-S setup menu or by using the Intel Boot Agent (IBA) utility.

Table 39. Boot Agent Main Setup Options (Word 30h) (Sheet 1 of 2)

Bit	Name	Description
15	PPB	A value of 0b (default) for this bit indicates that the image in the Flash contains a PXE image. To be backward compatible with existing systems in the field, this bit must equal 0b. A value of 1 in this bit indicates that no PXE image is contained. If this bit is set to 0b, NVM word 32h (PXE Version) is valid. When EPB is set to 1b and this bit is set to 0b, both images are present in the Flash.
14	EPB	Setting this bit to 1b indicates that the image in the Flash contains an EFI image, and setting this bit to 0b, no EFI image is contained. The default for this bit is 0b in order to be backwards compatible with existing systems already in the field. If this bit is set to 1b, NVM word 33h (EFI Version) is valid. When PPB is set to 0b and this bit is set to 1b, both images (PXE and EFI) are present in the Flash.
13	Reserved	This bit is reserved and should be set to 0b.
12	FDP	If this bit is 0b the 82573 is forced to half duplex mode. If it is set to 1b, the device is in full duplex mode. This bit is a “don’t care” unless bits 11:10 are set.
11:10	FSP	These bits determine speed. 00b = Auto-Negotiate (current bit state) 01b = 10 Mbps 10b = 100 Mbps 11b = Not allowed Bit 12 (FDP) is a don’t care unless these bits are set.
9	LWS	The Legacy OS Wakeup Support bit is used for compatibility with 82559-based adapters only. If it is set to 1b, the agent enables PME in the adapter PCI Configuration space during initialization. This allows remote wakeup under legacy operating systems that are not normally supported. 0b = Disabled (default) 1b = Enabled Enabling this bit makes the network controller technically non-compliant with the ACPI specification.
8	DSM	If the Display Setup Message bit is set to 1b, the "Press Control-S" message appears after the title message. The default value for this bit is 1b.

Table 39. Boot Agent Main Setup Options (Word 30h) (Sheet 2 of 2)

Bit	Name	Description
7:6	PT	Prompt Time bits control how long the "Press Control-S" setup prompt message appears if it is enabled by the DSM bit. 00b = 2 seconds (default) 01b = 3 seconds 10b = 5 seconds 11b = 0 seconds The Ctrl-S message does not appear if 0 seconds prompt time is selected.
5	LBS	This bit is typically not used. Previous versions of the boot agent used this bit to enable or disable local boot if local boot is selected by the default boot selection. The default value for this bit is 1b, enabling local boot. The boot agent, at runtime, no longer uses this bit.
4:3	DBS	The Default Boot Select bits represent which device is the default boot device. These bits are only used if the agent detects that the BIOS does not support boot order selection or if the MODE field of word 31h is set to MODE_LEGACY. 00b = Network boot, then local boot. 01b = Local boot, then network boot. 10b = Network boot only. 11b = Local boot only.
2	BBS	The BIOS Boot Specification bit is obsolete. In previous versions of the agent, this bit enabled or disabled the use of the BBS to determine boot order. If it equals 1b, the BIOS boot order was used, and the DBS bits were ignored. The boot agent at runtime no longer uses this bit. The runtime checks for BBS/PnP and the setting in the MODE field of word 31h are used instead.
1:0	PS	The Protocol Select bits represent the boot protocol. 00b = PXE (default) 01b = Reserved Other values are not defined.

2.1.30.2 Boot Agent Configuration Custom Options (Word 31h)

Word 31h contains settings that can be programmed by an OEM or network administrator to customize the operation of the software. These settings cannot be changed from within the Control-S setup menu or the IBA utility. The lower byte contains settings that would typically be configured by a network administrator using the Intel Boot Agent utility. These settings generally control which setup menu options are changeable. The upper byte contains settings that would be used by an OEM to control the operation of the agent in a LOM environment; however, there is nothing in the agent to prevent their use on a NIC implementation.

Table 40. Boot Agent Configuration Custom Options (Word 31h)

Bit	Name	Description
15:14	SIG	Signature. These bits must be set to 11b to indicate that this word has been programmed by the agent or other configuration software.
13:11	Reserved	These bit are reserved and should be set to 000b.
10:8	MODE	The MODE field selects the agent's boot order setup mode. This field changes the default behavior in order to make it compatible with systems that do not completely support the BBS and PnP Expansion ROM standards. Valid values and their meanings are: 000b - Normal behavior. The agent attempts to detect BBS and PnP Expansion ROM support as it normally does. 001b - Force Legacy mode. The agent does not attempt to detect BBS or PnP Expansion ROM supports in the BIOS and assumes the BIOS is not compliant. The BIOS boot order can be changed in the Setup Menu. 010b - Force BBS mode. The agent assumes the BIOS is BBS compliant, even if it is not detected as such by the agent's detection code. The BIOS boot order cannot be changed in the Setup Menu. 011b - Force PnP Int18 mode. The agent assumes the BIOS allows boot order setup for PnP Expansion ROMs and hooks interrupt 18h (to inform the BIOS that the agent is a bootable device) in addition to registering as a BBS IPL device. The BIOS boot order cannot be changed in the Setup Menu. 100b - Force PnP Int19 mode. The agent assumes the BIOS allows boot order setup for PnP Expansion ROMs and hooks interrupt 19h (to inform the BIOS that the agent is a bootable device) in addition to registering as a BBS IPL device. The BIOS boot order cannot be changed in the Setup Menu. 101b - Reserved and should be treated as value 000b. 110b - Reserved and should be treated as value 000b. 111b - Reserved and should be treated as value 000b.
7:6	Reserved	These bits are reserved and should be set to 00b.
5	DFU	The Disable Flash Update bit is used to enable or disable updates to the Flash image. If it equals 0b (default), Flash image updates using PROSet is allowed. If it is set to 1b, Flash image updates using PROSet is not allowed.
4	DLWS	The Disable Legacy Wakeup Support bit enables or disables changes to the legacy OS wakeup support menu. If it equals 0b (default), changes are allowed. If it equals 1b, changes are not allowed.
3	DBS	The Disable Boot Selection bit enables or disables menu option changes for boot order. If it equals 0b (default), changes for the boot order menu are allowed. If it is set to 1b, changes are not allowed.
2	DPS	This is the Disable Protocol Select bit. If this bit equals 0b (default), changes to the boot protocol are allowed. If it is set to 1b, no changes to the boot protocol are allowed.
1	DTM	The Disable Title Message bit enables or disables the title message. If it equals 0b (default), the boot agent version and Control-S message are displayed. If it is set to 1b, the boot agent version and Control-S message are suppressed. (This is useful for OEMs who do not want the boot agent to display any messages at system boot.)
0	DSM	This bit represents the Disable Setup Menu. If it equals 0b (default), the setup menu can be invoked by pressing Control-S. If it is set to 1b, the setup menu cannot be invoked. In this case, the NVM can only be changed through an external program.

2.1.30.3 Boot Agent Configuration Custom Options (Word 32h)

Word 32h is used to store the version of the boot agent contained in the Flash image. When the Boot Agent loads, it can check this value to determine if any first-time configuration needs to be performed. Then, the agent updates this word with its version. Some diagnostic tools used for reporting the Boot Agent version in the Flash also have the ability to read this word. This word is only valid if the PPB is set to 0b. Otherwise the contents may be undefined.

Table 41. Boot Agent Configuration Custom Options (Word 32h)

Bit	Name	Description
15:12	MAJOR	PXE boot agent major version. The default for these bits is 00h.
11:8	MINOR	PXE boot agent minor version. The default for these bits is 00h
7:0	BUILD	PXE boot agent build number. The default for these bits is 00h.

2.1.30.4 IBA Capabilities (Word 33h)

Word 33h is used to enumerate the boot technologies that have been programmed into the Flash. It is updated by IBA configuration tools and is not updated or read by IBA.

Table 42. IBA Capabilities (Word 33h)

Bit	Name	Description
15:14	SIG	This field represents the signature. These bits must be set to 11b to indicate that this word has been programmed by the agent or other configuration software.
13:5	Reserved	Reserved for future use. Set these bits to 0b.
4	SAN	SAN capability is present in Flash. 0b = The SAN capability is not present (default). 1b = The SAN capability is present.
3	EFI	EFI UNDI capability is present in Flash. 0b = The EFI code is not present (default). 1b = The EFI code is present.
2	Reserved	Reserved
1	UNDI	PXE/UNDI capability is present in Flash. 1b = The PXE base code is present (default). 0b = The PXE base code is not present.
0	BC	PXE base code is present in Flash. 0b = The PXE base code is present (default). 1b = The PXE base code is not present.

2.1.30.5 Boot Configuration Start Address (Word 3Dh)

Table 43. Boot Configuration Start Address (Word 3Dh)

Bit	Name	Description
15:0	Address	This field defines the starting location of the word address in the NVM space of the Boot Configuration structure.

2.1.30.6 Boot Agent Configuration Custom Options (Word 3Eh)

This structure is listed as follows:

Table 44. Boot Agent Configuration Custom Options (Word 3Eh)

Configuration Item	Maximum Size (Bytes)	Description
Boot Signature	2	
Total Size	2	The structure size is stored in this field and is set depending on the amount of free NVM space available. The total size of this structure, including variable length fields, must fit within this space.
Structure Version	1	The structure version is stored in this field and should be set to 1b.
Checksum	1	This field holds the 8-bit checksum of this structure.
Flags	2	01h = Enable boot 02h = Valid configuration (This should be set to 1b if the configuration information is valid, and 0, otherwise.) 03h = Enable DHCP 04h to 05h = Configuration prompt time displayed 0 = 0 seconds 1 = 2 seconds 2 = 3 seconds 3 = 5 seconds 06h to 0Ah = Number of connection retries
Initiator IP	4	If the DHCP flag is not set, this field should contain the configured IP address. If the DHCP flag is set, this field should be set to 0b or the last configured IP address should be saved.
Initiator Subnet Mask	4	If the DHCP flag is not set, this field should contain the configured subnet mask. If the DHCP flag is set, this field should be set to 0b or the last subnet mask should be saved.
Target IP	4	IP address of target.
Target Port	2	IP port of target. The default is 3260.
CHAP Password	32	
CHAP User Name	255+1	This is a variable length field.
Initiator Name	255+1	This is a variable length field.
Target Name	255+1	This is a variable length field.

The maximum amount of boot configuration information that will be stored is 834 bytes (417 words); however, the boot implementation can limit this value in order to work with a smaller NVM.

Variable length fields are used to limit the total amount of NVM used for boot information. Each field is preceded by a single byte that indicates how much space is available for that field. For example, if the Initiator Name field is limited to 128 bytes, it will be preceded with a single byte with the value 128. The following field will begin 128 bytes after the beginning of the Initiator Name field regardless of the actual size of the field. The variable length fields must be NULL terminated unless they reach the maximum size specified in the length byte.

2.1.31 Checksum Word Calculation (Word 3Fh)

The Checksum word (3Fh) is calculated such that after adding all words (00h-3Fh), including the Checksum word itself, the sum should equal BABAh. The initial value in the 16-bit summing register should be 0000h and the carry bit should be ignored after each addition. This checksum is not accessed by the 82573 controller. If CRC checking is required, it must be performed by software.

Note: Hardware does not calculate checksum word 3Fh during NVM write; it must be calculated by software independently and included in the NVM write data. Hardware does not compute a checksum over words 00h-3Fh during NVM reads in order to determine the validity of the NVM image. This field is provided strictly for software verification of NVM validity. All hardware configuration based on word 00h-3Fh content is based on the validity of the signature field of the NVM.

2.2 Base Area 40h

The Base Area 40h is loaded in the NVM if the Base Area 40h bit in the Initialization Control Word 1 is set. Its general structure is defined below.

Table 45. 82573 NVM Map for Address Range 40h to 4Fh

Word	Used By	High Byte Bits 15:8	Low Byte Bits 7:0	Image Value
40h	HW	MNG D1 Power Consumption		
41h	HW	MNG D3 Power Consumption		
42h	HW	IDE Device ID		
43h	HW	Serial Port Device ID		
44h	HW	KCS Device ID		
45h	HW	IDE Subsystem ID		
46h	HW	Serial Port Subsystem ID		
47h	HW	KCS Subsystem ID		
48h	HW	Future Request Time-out		
49h	HW	Functions Control		
4Ah	HW	Flash Parameters		
4Bh	HW	Boot Expansion Addresses		
4Ch	HW	Boot Expansion Size		
4Dh		Reserved		
4Eh	HW	KCS Device Class Code Low		
4Fh	HW	KCS Device Class Code High		

2.2.1 Manageability D0 Power Consumption (Word 40h)

Note: This word is only relevant to the 82573E.

Table 46. Manageability D0 Power Consumption (Word 40h)

Bit	Name	Default	Description
15	Reserved	1b	This bit is reserved and should be set to 1b.
14:10	IDE D0 PWR	00000b	This is the power consumption value reflected in the data register of the IDE function in the power management registers at the D0 power state. This same value is reflected in the power consumption and power dissipation.
9:5	Serial D0 PWR	00000b	This is the power consumption value reflected in the data register of the serial port function in the power management registers at the D0 power state. This same value is reflected in the power consumption and power dissipation.
4:0	KCS D0 PWR	00000b	This is the power consumption value reflected in the data register of the KCS function in the power management registers at the D0 power state. This same value is reflected in the power consumption and power dissipation.

2.2.2 Manageability D3 Power Consumption (Word 41h)

Note: This word is only relevant to the 82573E.

Table 47. Manageability D3 Power Consumption (Word 41h)

Bit	Name	Default	Description
15	Reserved	1b	This bit is reserved and should be set to 1b.
14:10	IDE D3 PWR	00000b	This is the power consumption value reflected in the data register of the IDE function in the power management registers at the D3 power state. This same value is reflected in the power consumption and power dissipation.
9:5	Serial D3 PWR	00000b	This is the power consumption value reflected in the data register of the serial port function in the power management registers at the D3 power state. This same value is reflected in the power consumption and power dissipation.
4:0	KCS D3 PWR	00000b	This is the power consumption value reflected in the data register of the KCS function in the power management registers at the D3 power state. This same value is reflected in the power consumption and power dissipation.

2.2.3 IDE Device Word (Word 42h)

This word contains the IDE device identification. Its default value is 108Dh, Intel® AMT IDE-R.

2.2.4 Serial Port Device ID (Word 43h)

Note: This word is only relevant to the 82573E.

This word contains the serial port device identification. Its default value is 108Fh, Intel® AMT SOL.

2.2.5 KCS Device ID (Word 44h)

Note: This word is only relevant to the 82573E.

This word contains the KCS device identification. Its default value is 108Eh, Intel® AMT KCS-R.

2.2.6 IDE Subsystem ID (Word 45h)

Note: This word is only relevant to the 82573E.

This word contains the IDE subsystem vendor identification, which is defined by the OEM. Its default value is 0000h.

2.2.7 Serial Port Subsystem ID (Word 46h)

Note: This word is only relevant to the 82573E.

This word contains the serial port subsystem vendor identification, which is defined by the OEM. Its default value is 0000h.

2.2.8 KCS Subsystem ID (Word 47h)

Note: This word is only relevant to the 82573E.

This word contains the KCS subsystem vendor identification, which is defined by the OEM. Its default value is 0000h.

2.2.9 Future Request Time-Out (Word 48h)

Table 48. Future Request Time-Out (Word 48h)

Bit	Name	Default	Description
15:8	Reserved	00h	These bits are reserved and should be set to 00h.
7:4	FRBTO	1111b	This field represents the boot time future request time-out. A future request locks time-out after the de-assertion of the PCIe* reset. During this time, the firmware minimizes its activity in order to maximize Flash bandwidth for the BIOS during boot code execution.[1] This time is defined as 1 s * FRBTO.
3:0	FRRTO	0000b	This field represents the run time future request time-out. A future request locks time-out during run time.[1] This time is defined as 100 ms * FRRTO.

1. Future request time-outs are implemented by firmware. After the timer expires, firmware can override the future request and initiate a long, single SPI cycle.

2.2.10 Functions Control (Word 49h)

Table 49. Functions Control (Word 49h)

Bit	Name	Default	Description
15	IDE Enable	0b	This bit enables the IDE function in the PCI Configuration Space. When it is set to 0b (default), the IDE configuration space is not visible to the system. This bit is reflected in the FACTPS register.
14	Serial Enable	0b	This bit enables the serial port function in the PCI Configuration Space. When it is set to 0b (default), the serial port configuration space is not visible to the system. This bit is reflected in the FACTPS register.
13	KCS Enable	0b	This bit enables the KCS function in the PCI Configuration Space. When it is set to 0b (default), the KCS configuration space is not visible to the system. This bit is reflected in the FACTPS register.
12	Reserved	0b	This bit is reserved and should be set to 0b.
11:10	IDE INT Select	01b	This field sets the default for the IDE Interrupt Pin. The value is loaded to the interrupt pin register in the PCI Configuration Space. Its default value is INT D (01b).
9:8	Serial INT Select	10b	This field sets the default for the Serial Interrupt Pin. The value is loaded to the interrupt pin register in the PCI Configuration Space. Its default value is INT C (10b).
7:6	KCS INT Select	11b	This field sets the default for the KCS Interrupt Pin. The value is loaded to the interrupt pin register in the PCI Configuration Space. Its default value is INT D (11b).
5:0	Reserved	00h	These bits are reserved and should be set to 00h.

2.2.11 Flash Parameters (Word 4Ah)

Table 50. Flash Parameters (Word 4Ah)

Bit	Name	Default	Description
15:8	FDEVER	1111b 1111b	This field defines the instruction code for the Flash device erase. A value of 00h indicates that the device does not support device erase. Its default value is FFh.
7:6	Reserved	00b	These bits are reserved and should be set to 00b.
5	FLSSTn	0b	When this bit is 0b (default), write access to the Flash is limited to 1 byte at a time and a clear write protection is required at power up. When it is set to 1b, burst write access to the Flash is enabled up to 256 bytes and a clear write protection at power up is not required.
4	LONGC	0b	When this bit equals 0b (default), a write cycle to the Flash is not a long cycle. When it is 1b, this indicates that the Flash write instruction is long.
3:0	Reserved	0000b	These bits are reserved and should be set to 0000b.

2.2.12 Boot Expansion Address (Word 4Bh)

Table 51. Boot Expansion Address (Word 4Bh)

Bit	Name	Default	Description
15:0	Reserved	00h	These bits are reserved and should be set to 00h.

2.2.13 Boot Expansion Size (Word 4Ch)

Table 52. Boot Expansion Size (Word 4Ch)

Bit	Name	Default	Description
15	Disable KCS Expansion	1b	When this bit is set to 1b (default), the KCS Expansion Boot ROM BAR is disabled.
14	Disable IDE Expansion	1b	When this bit is set to 1b (default), the IDE Expansion Boot ROM BAR is disabled.
13	Disable LAN Expansion	1b	When this bit is set to 1b (default), the LAN Expansion Boot ROM BAR is disabled.
12	Disable LAN Flash BAR	0b	When this bit is set to 1b (default), the LAN Flash BAR is disabled.
11:0	Reserved	00h	This bit is reserved and should be set to 00h.

2.2.14 KCS Device Class Code Low (Word 4Eh)

Note: This word is only relevant to the 82573E.

This word specifies the device class code for the KCS function.

Table 53. KCS Device Class Code Low (Word 4Eh)

Bit	Name		Description
15:8	Class Code (Mid)	0000b 0111b	This is the middle byte of the KCS class code. It is a subclass equal to 07h.
7:0	Class Code (LSB)	0000b 0001b	This is the least significant byte of the KCS class code. It is a base class code equal to 01h.

2.2.15 KCS Device Class Code High (Word 4Fh)

Note: This word is only relevant to the 82573E.

This word specifies the device class code for the KCS function.

Table 54. KCS Device Class Code High (Word 4Fh)

Bit	Name		Description
15:8	Reserved	0b	These bits are reserved and should be set to 0.
7:0	Class Code (MSB)	0000b 1100b	This is the most significant byte of the Intel AMT class code. It is a base class code equal to 0Ch.

2.3 Intel® AMT Main Area

Note: This area is not used for designs using the 82573V or 82573L device.

2.3.1 Intel® AMT MAC Address (Words 80h - 82h)

The 82573E requires an Intel® AMT dedicated Ethernet address (also known as the manageability MAC address). This function supports dedicated static IP mode only if the device has an assigned dedicated Intel® AMT Ethernet address.

The manageability MAC address is the Intel AMT Ethernet Individual Address (IA) and is a 6-byte field reserved for a dedicated Intel AMT MAC address. Intel's default factory settings for these offsets are: FFh, FFh, FFh, FFh, FF, FFh.

An identical MAC address should not be used in both the LAN MAC section at word 00h to 02h and the manageability dedicated MAC section at word 80h to 82h. This type of configuration is considered to be invalid.

The Intel® AMT device assumes correct image configuration and does not perform any checksum.

2.4 ASF Control Words

Note: ASF is only relevant to the 82573E and 82573V.

When the 82573E/V is in ASF mode, it reads the ASF words from the management section starting at the address contained in the START field. These words are read after power-up, ASF Soft Reset, or software commanded ASF NVM read. These words should be programmed by the ASF configuration software. Their values from the factory should all equal FFh.

2.4.1 ASF Words: Content

The interpretation of these words will be described in future revisions of this document.

2.4.2 ASF Words: NVM Checksum (CRC)

While reading the ASF NVM words, the 82573E/V computes the ASF CRC word. Words 00h to B7h (relative to PSTART) are included in the ASF CRC calculation. The result is compared against the CRC value present in word B7h. If the CRC values mismatch, the 82573E/V will not overwrite the ASF Configuration Registers with the NVM values. Therefore, if the ASF CRC is invalid, hardware default values will initially be present in ASF registers and any subsequent re-read of NVM will leave the ASF registers unchanged from the values at the time of the NVM read.

2.4.3 ASF Configuration Map

The following table defines the contents of the ASF configuration area. The base address for this area is defined by the PSTART field.

Table 55. 82573E/V NVM Map for ASF (Sheet 1 of 2)

Word	Used By	High Byte Bits 15:8	Low Byte Bits 7:0	Image Value
00h 01h 02h 03h 04h 05h 06h 07h	FW	Reset SMB Command Power-Off SMB Address Power-Off Data Value Power-On SMB Command Power Cycle SMB Address Power Cycle Data Value Reserved (default is 0) Reserved (default is 0)	Reset SMB Address Reset SMB Data Value Power-Off SMB Command Power-On Address Power-On Data Value Power Cycle SMB Command Reserved (default is 0) Reserved (default is 0)	
08h 09h ... 0Eh 0Fh	FW	ASF Polling Descriptor 1 ASF Polling Descriptor 3 ... ASF Polling Descriptor 13 ASF Polling Descriptor 15	ASF Polling Descriptor 0 ASF Polling Descriptor 2 ... ASF Polling Descriptor 12 ASF Polling Descriptor 14	
10h 11h 12 13h ... 1Eh 1Fh	FW	Poll 1 SMB Command Poll 1 SMB Data Compare Poll 2 SMB Command Poll 2 SMB Data Compare ... Poll 8 SMB Command Poll 8 SMB Data Compare	Poll 1 SMB Address Poll 1 SMB Data Mask Poll 2 SMB Address Poll 2 SMB Data Mask ... Poll 8 SMB Address Poll 8 SMB Data Mask	
20h 21h 22h 23h ... 3Ch 3Dh 3Eh 3Fh	FW	Poll 1 PET Event Type Poll 1 PET Event Source Type Poll 1 PET Sensor Number Poll 1 PET Entity Instance ... Poll 8 PET Event Type Poll 8 PET Event Source Type Poll 8 PET Sensor Number Poll 8 PET Entity Instance	Poll 1 Pet Event Sensor Type Poll 1 PET Event Offset Poll 1 Pet Event Severity Poll 1 PET Entity ... Poll 8 Pet Event Sensor Type Poll 8 PET Event Offset Poll 8 Pet Event Severity Poll 8 PET Entity	
40h 41h ... 46h 47h				
48h 49h ... 4Eh 4Fh	FW	Capabilities Data Byte 1 Capabilities Data Byte 3 ... Capabilities Data Byte 13 Capabilities Data Byte 15	Capabilities Data Byte 0 Capabilities Data Byte 2 ... Capabilities Data Byte 12 Capabilities Data Byte 14	
50h 51h 52h 53h 54h 55h 56h 57h	FW	ASF Register E1h ASF Register E3h ASF Register E5h ASF Register E7h ASF Register E9h ASF Register EBh ASF Register EDh Reserved (default is 0)	ASF Register EFh ASF Register E2h ASF Register E4h ASF Register E6h ASF Register E8h ASF Register EAh ASF Register ECh ASF Register F6h	
58h ... 5Fh		Reserved (default is 0)		

Table 55. 82573E/V NVM Map for ASF (Sheet 2 of 2)

Word	Used By	High Byte Bits 15:8	Low Byte Bits 7:0	Image Value
60h ... 8Fh	FW	RSP Data		
90h ... B3h	FW	PET Descriptor		
B4h ... B6h		Reserved (default is 0)		
B7h	FW	Firmware Configuration Bits for ASF/APT Modes		
B8h B9h	FW	Patch Pointer 1 (default is 0)		
BAh BBh	FW	Patch Pointer 2 (default is 0)		
BCh	FW	Reserved (default is 0)		
BDh	FW	ASF and Pointers Area CRC	Reserved (default is 0)	
BEh BFh	FW	Power Up Counter in EEPROM Image Reserved in Flash Image (default is 0)		

Appendix A 82573 NVM Contents

This appendix contains a sample of raw NVM contents for the 82573. All values for this image are in hexadecimal.

Note: This silicon has not been developed using the NVM process.

These images are for base reference only. They are tested production images designed for a generic NIC using the silicon specified. They do not necessarily have every possible feature enabled or configured.

Note: Design implementations can vary. Settings should be reviewed for application to a particular design.

A.1 82573E/V with No Management and 1 Kb EEPROM Image

```
0/8  1/9  2/A  3/B  4/C  5/D  6/E  7/F

8888 8888 8887 0B30 F746 3001 FFFF FFFF
FFFF FFFF 026B 0000 8086 108B 8086 80DF
0000 2000 7E14 0000 0000 00D8 0000 2700
6CC9 3150 072E 040B 0984 0000 C000 0706
1008 0000 0F04 7FFF 4D01 FFFF FFFF FFFF
FFFF FFFF FFFF FFFF FFFF FFFF FFFF FFFF
0100 4000 121C 4007 FFFF FFFF FFFF FFFF
FFFF FFFF FFFF FFFF FFFF FFFF FFFF FFFF
```

A.2 82573L with No Management and 1 Kb EEPROM Image

```
0/8  1/9  2/A  3/B  4/C  5/D  6/E  7/F

8888 8888 8887 0B30 F746 0057 FFFF FFFF
FFFF FFFF 026B 0000 8086 109A 8086 80DF
0000 2000 7E54 0000 0014 00DA 0004 2700
6CC9 3150 0732 040B 2984 0000 F000 0706
1008 0000 0F04 7FFF 4D01 FFFF FFFF FFFF
0014 001D 0014 001D AAAF 001E 0000 001D
0100 4000 121C 4007 FFFF FFFF FFFF FFFF
FFFF FFFF FFFF FFFF FFFF FFFF FFFF FFFF

-----------Range [0x40-0x7F]----------
FFFF FFFF FFFF FFFF FFFF FFFF FFFF FFFF
FFFF FFFF FFFF FFFF FFFF FFFF FFFF FFFF
FFFF FFFF FFFF FFFF FFFF FFFF FFFF FFFF
FFFF FFFF FFFF FFFF FFFF FFFF FFFF FFFF
FFFF FFFF FFFF FFFF FFFF FFFF FFFF FFFF
FFFF FFFF FFFF FFFF FFFF FFFF FFFF FFFF
FFFF FFFF FFFF FFFF FFFF FFFF FFFF FFFF
FFFF FFFF FFFF FFFF FFFF FFFF FFFF FFFF
```

Appendix B Intel® AMT Guidelines for Local Programming of Shared SPI Devices

This appendix is applicable to the 82573E device only.

B.1 Overview

This appendix explains the steps required to locally program the SPI Flash device in a shared BIOS design with the 82573E GbE controllers. The shared SPI configuration includes both BIOS and Intel® AMT content. The procedures outlined below can be implemented by an OEM, ODM, or IBV to correctly and safely update the contents of the SPI Flash without corrupting the content.

B.1.1 Intel® Active Management Technology

Intel® AMT is a hardware-based solution that uses out-of-band communication for management access to client systems. It enables designers to remotely discover, heal and protect networked computing assets, regardless of system state.

B.2 Intel® AMT Flash Image Map

Intel® AMT firmware divides the Flash device into 4 KB sectors. If the Flash device has a smaller block size (like STM, which has block size of 256 bytes), the firmware uses logical sectors of 4 KB.

The following table lists the high-level mapping of the Flash device when the 82573E device is configured for Intel® AMT (not including the BIOS area).

Start Offset	End Offset	Description
00000h	00FFFh	Legacy area
01000h	01FFFh	Legacy area scratch sector
02000h	02FFFh	Manageability Configuration Area (MCA)
03000h	03FFFh	MCA scratch sector
04000h	0EFFFh	Intel AMT configuration (provisioning data)
0F000h	26FFFh	Third party data (ISV storage)
27000h	CodeEnd	Intel® AMT code
CodeEnd+1	PatchEnd	Intel® AMT patches

B.2.1 Legacy Area

The legacy area contains the following data:

- Hardware configuration data: PHY configuration, PCIe configuration and LED configuration.
- LAN configuration: MAC address, device and vendor ID, part number, etc.
- Intel AMT configuration:
  - — Firmware mode (AMT, ASF, APT, NO_MNG).
  - — Intel AMT protection start and end offsets.
  - — Configuration bits.

B.2.2 Legacy Area Scratch Sector

Since the first 4 Kb contain crucial data essential for hardware, firmware and software functionality, this data has a built-in backup mechanism in the 82573E hardware. The hardware uses the two first sectors interchangeably in the following manner:

- Initial state. Data is stored in the first sector (valid sector), and the second sector is empty (invalid sector).
- The valid sector contains the signature 7Eh in byte offset 25h, and the invalid sector has a value of 00h in the same offset.
- When the legacy data needs to be updated (from software or firmware), the hardware copies the valid sector data with the new information and signature to the invalid sector and then invalidates the valid sector (by deleting the signature). This mechanism ensures that at least one valid sector is present.

This mechanism is used only when accessing the Flash device through 82573E hardware. When the BIOS accesses the Flash directly through the SPI interface, this mechanism is not active.

B.2.3 Manageability Configuration Area

The Manageability Configuration Area (MCA) contains configuration data for the core firmware (for example, firmware that is running from ROM), therefore the data structures and offsets cannot be changed (only the data), since the code that uses them cannot be changed.

The MCA has a scratch mechanism similar to the legacy scratch sector mechanism. It also uses two sectors and has a mechanism to switch between them. The signature of the MCA contains the 32-byte string for the Manageability Configuration Area in the first 32 bytes of the valid sector. The invalid sector contains 32 values equaling 00h.

The most important data in the MCA are the Patch pointers. The Patch pointers (each 4 bytes) are located in the last 8 bytes of the valid MCA sector and must be correlated with the firmware code (in other words, the Patch pointers must point to the start of the patches). Patch pointers of version X will not point to the Patches of version Y. Each firmware version has its own set of patches and Patch pointers.

If a fatal error occurs or the Flash image is corrupted, the MCA should be updated as part of the firmware update process.

B.2.4 Intel® AMT Configuration Area

This area contains configuration data for the firmware applications running from the Flash, not the ROM). It holds the provisioning data (for example, certificates, passwords, etc.).

When the firmware code is updated, this area should not be updated. Therefore, there is no need to provision Intel® AMT again.

If a fatal error occurs or the Flash image is corrupted, this area should be updated as part of the firmware update process.

B.2.5 ISV Storage (Third Party Data)

This area contains third party information. When the firmware is updated, this area should not be updated.

B.2.6 Intel® AMT Code

This area contains Intel® AMT firmware application code (compressed). It is the main area that is updated by the firmware update process.

B.2.7 Intel® AMT Patches

The patches are parts of the firmware that the core firmware runs to work around errata in the ROM code. The patches must be pointed to by the Patch pointers in the MCA. These patches are always be updated when the code is updated. Therefore, the firmware update process must always update the Patch pointers in the MCA.

B.3 Local Firmware Update Process – Code Only

The following series of steps outline the process to update Intel® AMT firmware code while leaving the provisioning data and the third party data untouched. This process is designed for a tool with access to the protected areas of Intel® AMT and does not work if the tool cannot access the protected areas.

The firmware update tool needs to contain two parts from the new image:

- The new patch pointers, located at offset 02FF8h to 02FFFh in the new image.
- The new code (code and patches), located at offset 27000h to the end of the image.

All offsets in this process are absolute (from offset 00h) unless otherwise stated.

1. Find the valid sector of the legacy area.
   - — Check if byte offset 25h = 7Eh.
   - — If yes, sector 0 (00000h through 00FFFh) is the valid sector.
   - — If no, check if byte offset 01025h = 7Eh.
   - — If yes, sector 1 (01000h through 01FFFh) is the valid sector.
   - — If neither offsets contain the signature, the image is corrupted and the whole image (from offset 0) should be programmed.
2. Stop Intel® AMT firmware.
   a. If sector 0 is valid:
   - — Copy sector 0 (00000h through 00FFFh) to RAM.
   - — In the RAM sector, clear bits 2 and 3 in byte offset 20h.
   - — In the RAM sector, set byte offset 25h to 7Eh.
   - — Erase sector 1 (01000h through 01FFFh).
   - — Write the RAM sector to sector 1 (01000h through 01FFFh).
   - — In sector 0 of the Flash, delete the signature by clearing byte 25h.
   - — Clear byte 47h bit 7 so that the device driver recalculates the software checksum.

   b. If sector 1 is valid:
   - — Copy sector 1 (01000h through 01FFFh) to RAM.
   - — In the RAM sector, clear bits 2 and 3 in byte offset 20h.
   - — In the RAM sector, set byte offset 25h to 7Eh.
   - — Erase sector 0 (00000h through 00FFFh).
   - — Write the RAM sector to sector 0 (00000h through 00FFFh).

— In sector 1 of the Flash, delete the signature by clearing byte 01025h.

— Clear bit 7 of byte 1047h so that device driver recalculates the software checksum.

Find BAR0 of the 82573E device.

Write 000000C0h to BAR0 + 8F00h.

Wait 10 ms.

The Intel® AMT firmware is now stopped.

If a power loss occurred during this step, there is a valid sector, but it might not contain the changes done to stop the AMT firmware. The tool should verify the value of byte offset 20h in the valid sector and execute this step again in case the Intel® AMT firmware was not disabled.

3. Find the valid MCA sector.

   — Compare 32 bytes from byte offset 02000h with the string Manageability Configuration Area.

   — If the data is equal, sector 2 (02000h through 02FFFh) is the valid MCA sector.

   — If the data is not equal, compare 32 bytes from byte offset 03000h with the same string.

   — If the data is equal, sector 3 (03000h through 03FFFh) is the valid MCA sector.

   — If neither sectors contain the MCA signature, the image is corrupted and a recovery update should be performed (see Appendix C”).

4. Update Patch pointers.

   a. If sector 2 is the valid MCA sector:

   — Copy sector 2 (02000h through 02FFFh) to RAM.

   — In the RAM sector, write the new Patch pointers (using the tool) to offset FF8h through FFFh.

   — Erase sector 3 (03000h through 03FFFh).

   — Write the RAM sector to sector 3 (03000h through 03FFFh).

   — In sector 2, delete the MCA signature by clearing bytes 02000h through 02031h.

   b. If sector 3 is the valid MCA sector:

   — Copy sector 3 (03000h through 03FFFh) to RAM.

   — In the RAM sector, write the new Patch pointers (using the tool) to offset FF8h through FFFh.

   — Erase sector 2 (02000h through 02FFFh).

   — Write the RAM sector to sector 2 (02000h through 02FFFh).

   — In sector 2, delete the MCA signature by clearing bytes 03000h through 03031h.

In the event of a power loss during this step, there is a valid MCA sector. However, it might not contain the changes done to update the Patch pointers. The tool should verify the value of byte offset FF8h through FFFh in the valid MCA sector and execute this step again in case the Patch pointers were not updated.

5. Update Intel® AMT code area.

   a. Erase all code sectors in the Flash from byte offset 27000h to the first BIOS sector (excluded).

b. Write the new code to offset 27000h until end of code.

c. If power loss occurred during this step, the tool should repeat this step.

6. Start Intel® AMT firmware.

Find the valid legacy sector (this should already be known by the tool since it swapped the sectors in step 1.

a. If sector 0 is valid:

— Copy sector 0 (00000h through 00FFFh) to RAM.

— In the RAM sector, set bits 2 and 3 in byte offset 20h to 11b.

— In the RAM sector, set byte offset 25h to 7Eh.

— Erase Sector 1 (01000h through 01FFFh).

— Write the RAM sector to sector 1 (01000h through 01FFFh).

— In sector 0 of the Flash, delete the signature by clearing byte 25h.

— Clear byte 47h bit 7 so that the device driver recalculates the software checksum.

b. If sector 1 is valid:

— Copy sector 1 (01000h through 01FFFh) to RAM.

— In the RAM sector, set bits 2 and 3 in byte offset 20h to 11b.

— In the RAM sector, set byte offset 25h to 7Eh.

— Erase Sector 0 (00000h through 00FFFh).

— Write the RAM sector to sector 0 (00000h through 00FFFh).

— In sector 1 of the Flash, delete the signature by clearing byte 01025h.

— Clear byte 1047h bit 7 so that the device driver recalculates the software checksum.

Write 00000004h to BAR0 + 5B50h.

Wait 10 ms.

The Intel® AMT firmware is now running.

If a power loss occurred during the middle of this step, there is a valid sector but it might not contain the changes done to start the Intel® AMT firmware. The tool should verify the value of byte offset 20h in the valid sector and execute this step again in case the Intel® AMT firmware was not enabled.

7. Validate.

To validate Intel® AMT firmware is running, perform one of the following:

a. Issue the GetPtState command over the KCS interface.

b. Poll the value of BAR0 + 5B54h until the lower word is 8046h.

c. Send SMB ARP and wait for a reply from Intel® AMT firmware.

Appendix C Local Firmware Update Process – Recovery Mode

In the situation of a corrupted image or a required provisioning data update, an alternate process that updates the whole Intel® AMT area including the MCA, firmware configuration, third party data and the code can be performed. The following series of steps outline the process for updating only the Intel® AMT firmware code while leaving the provisioning data and the third party data untouched. This process is designed for a tool that has access to the protected areas of Intel® AMT and does not work if the tool cannot access the protected areas.

The firmware update tool needs to contain part of the new image (MCA + Intel® AMT configuration + code + patches) located at offset 02000h to end of the image.

1. Perform steps 1 and 2 defined in Appendix B.3, to stop the Intel® AMT firmware.
2. Replace the Image:
    a. Erase all sectors in the Flash from byte offset 02000h to the first BIOS sector (excluded).
    b. Write the new data from offset 02000h to the end of the code.
3. Perform steps 6 and 7 defined in Appendix B.3, to start the Intel® AMT firmware again.