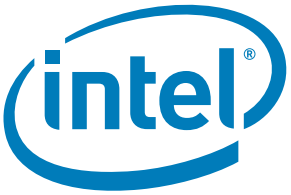


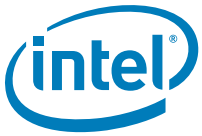
82571EB/82572EI Gigabit Ethernet Controller Design Guide

Application Note

February 2008

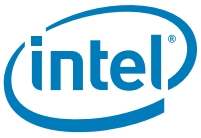
Order Number: 315337-002

Contents



Revision History

Revision	Dae	Description
0.15	Oct 2002	Initial publication of preliminary design guide information.
0.50	Apr 2003	Added Design and Layout Checklists; revised reference schematic
0.75	Oct 2003	Revised reference schematics; added design checklist.
0.80	Dec 2003	Revised schematics
0.85	Apr 2004	Revised schematics, engineering review.
0.90	January 2005	Added 82572 EI information; revised power supply information; added crystal information, moved schematics and checklist to seperate document, added reference design bills of materials
0.91	Feb 2005	Corrected Reference Schematic password
0.92	May 2005	Corrected Layout and Design Checklists password
1.0	November 2005	Added updated schematics and checklists
1.1	January 2007	Changed signal names: PERST# to PE_RST_N and WAKE# to PE_WAKE_N; SMBCLK1 and SMBD1 are now reserved, do not use these pins--connect to 3.3 V through 100k ohms.
1.2	February 2008	Updated schematics, corrected SMBus section of Design Checklist, added information regarding grounds in Secs. 7.1.10 and 7.1.12



1.0 Introduction

The Intel® 82571/82572 Gigabit Ethernet Controller is a single, compact component that offers either one (82572) or two (82571) fully integrated Gigabit Ethernet Media Access Control (MAC) and physical layer (PHY) ports. This device uses the PCI Express* (PCIe) architecture (Rev. 1.0a). The Intel 82571/82572 Gigabit Ethernet Controller enables single- or dual-port Gigabit Ethernet implementation in a very small area and can be used for server and workstation network designs with critical space constraints.

The Intel 82571/82572 Gigabit Ethernet Controller provides a standard IEEE 802.3 Ethernet interface for 1000BASE-T, 100BASE-TX, and 10BASE-T applications (802.3, 802.3u, and 802.3ab). Each port also contains a Serializer-Deserializer (SERDES) to support 1000Base-SX/LX (optical fiber) and Gigabit backplane applications. In addition to managing MAC and PHY Ethernet layer functions, the controller manages PCI Express packet traffic across its transaction, link, and physical/logical layers.

The Intel 82571/82572 Gigabit Ethernet Controller's on-board System Management Bus (SMB) ports enable network manageability implementations required by information technology personnel for remote control and alerting via the LAN. With SMB, management packets can be routed to or from a management processor. The SMB ports enable industry standards, such as Intelligent Platform Management Interface (IPMI) and Alert Standard Forum (ASF) 2.0, to be implemented using the 82571/82572 Gigabit Ethernet Controller. In addition, on-chip ASF 2.0 circuitry provides alerting and remote control capabilities with standardized interfaces. The 82571EB/82572EI controller contains a dedicated microcontroller for manageability.

The 82571/82572 Gigabit Ethernet Controller with PCIe architecture is designed for high-performance and low-host-memory access latency. The device connects directly to a system Memory Control Hub (MCH) using either one or four PCIe Lanes.

Wide internal data paths eliminate performance bottlenecks by efficiently handling large address and data words. Combining a parallel and pipelined logic architecture optimized for gigabit ethernet and independent transmit and receive queues, the 82571/82572 Gigabit Ethernet Controller efficiently handles packets with minimum latency. The 82571/82572 Gigabit Ethernet Controller includes advanced interrupt handling features. The 82571/82572 Gigabit Ethernet Controller uses efficient ring buffer descriptor data structures, with up to 64 packet descriptors cached on chip. A large 48 KByte on-chip packet buffer maintains superior performance. In addition, using hardware acceleration, the controller offloads tasks from the host, such as TCP/UDP/IP checksum calculations and TCP segmentation.

The device is packaged in a 17 mm x 17 mm 256-ball grid array.

1.1 Scope

This application note contains Ethernet design guidelines applicable to LOM designs based on PCI Express-supported chipsets.

Section 2 describes PCIe interface design guidelines specific to the 82571EB/82572EI controller.

Section 3 gives recommendations for selecting components and describes special pins.

Section 4 gives information for frequency control device selection.

Section 5 provides crystal selection information.

Section 6 describes how to design with an oscillator instead of a crystal.

Section 7 provides layout guidelines.

Section 8 contains the bills of material for the reference designs

Section 9 provides the design and layout checklists

Section 10 contains the reference design schematics

1.2 Reference Documents

This application assumes that the designer is acquainted with high-speed design and board layout techniques. The following documents provide additional information:

- *82571/82572 Gigabit Ethernet Controller Product Datasheet*. Intel Corporation.
- *PCI Express Base Specification, Revision 1.0a.* PCI Special Interest Group.
- *PCI Express Card Electromechanical Specification, Revision 1.0a*. PCI Special Interest Group.
- *PCI Bus Power Management Interface Specification, Revision 1.1*. PCI Special Interest Group.
- *IEEE Standard 802.3, 2000 Edition*. Institute of Electrical and Electronics Engineers (IEEE).
- *82571EB/82572EI EEPROM Information Guide Application Note, AN496*.
- *Designing SERDES Applications--82545/82546, 82571/82572 & 631xESB/632xESB Application Note--AN498*

Note: Intel documentation is subject to frequent revision. Verify with your local Intel sales office that you have the latest information before finalizing a design.

2.0 PCI Express Port Connection to the Device

PCIe is a dual-simplex point-to-point serial differential low-voltage interconnect. The signaling bit rate is 2.5 Gbps per lane per direction. Each port consists of a group of transmitters and receivers located on the same chip. Each lane consists of a transmitter and a receiver pair. A link between the ports of two devices is a collection of lanes. The device supports up to four lanes on the PCIe interface.

Each signal is 8b/10b encoded with an embedded clock.

The PCI Express topology consists of a transmitter (Tx) located on one device connected through a differential pair connected to the receiver (Rx) on a second device. The controller may be located on the motherboard or on an add-in card using a connector specified by PCI Express.

The lane is AC-coupled between its corresponding transmitter and receiver. The AC coupling capacitor is located on the board close to transmitter side. Each end of the link is terminated on the die into nominal 100 Ω differential DC impedance. Board termination is not required.

For more information on PCI Express, refer to the *PCI Express* Base Specification, Revision 1.0a* and *PCI Express* Card Electromechanical Specification, Revision 1.0a.*

Note: In manufacturing, vias are required for testing and troubleshooting purposes. The via size should be a 17-mil (±2 mils for manufacturing variance) finished hole size (FHS).

2.1 PCI Express Reference Clock

The device uses a 100 MHz differential reference clock, denoted PE_CLKp and PE_CLKn. This signal is typically generated on the system board and routed to the PCI Express port. For add-in cards, the clock is furnished at the PCI Express connector.

The frequency tolerance for the PCI Express reference clock is +/- 300 ppm.

2.2 Other PCI Express Signals

The device also implements other signals required by the PCI Express specification. The Ethernet controller signals power management events to the system using the PE_WAKE_N signal, which operates similarly to the familiar PCI PME# signal. Finally, there is a PE_RST_N signal that serves as the familiar reset function for the controller.

2.3 PCI Express Routing Example

For information regarding the PCIe signal routing, please refer to the Intel PCIe Design Guide. Contact your Intel representative for information.

3.0 Ethernet Component Design Guidelines

These sections provide recommendations for selecting components and connecting special pins. For 1000 BASE-T designs, the main design elements are the 82571EB/ 82572EI Gigabit Ethernet Controller, an integrated or discrete magnetics module with RJ-45 connector, an EEPROM, and a clock source.

In 1000 BASE-SX designs, the magnetics module is omitted and the SerDes interface is connected to an optical transceiver in order to drive fiber connections. Backplane designs are similar, but operate SERDES-to-SERDES without the optical module.

3.1 General Design Considerations for Ethernet Controllers

Follow good engineering practices with respect to unused inputs by terminating them with pull-up or pull-down resistors, unless the datasheet, design guide or reference schematic indicates otherwise. Do not attach pull-up or pull-down resistors to any balls identified as No Connect. These devices may have special test modes that could be entered unintentionally.

3.1.1 Clock Source

All designs require a 25 MHz clock source. The 82571EB/82572EI Gigabit Ethernet Controller uses the 25 MHz source to generate clocks up to 125 MHz and 1.25 GHz for the PHY circuits, and 1.25 GHz for the SERDES. For optimum results with lowest cost, connect a 25 MHz parallel resonant crystal and appropriate load capacitors at the XTAL1 and XTAL2 leads. The frequency tolerance of the timing device should be 30 ppm or better.

3.1.2 Integrated Magnetics Module for 1000 BASE-T

The magnetics module has a critical effect on overall IEEE and emissions conformance. The module should meet the performance required for a design with reasonable margin to allow for manufacturing variation. Occasionally, components that meet basic specifications may cause the system to fail IEEE testing because of interactions with other components or the printed circuit board itself. Carefully qualifying new magnetics modules prevents this problem.

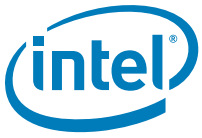
3.1.2.1 Magnetics Module Qualification Steps

The steps involved in magnetics module qualification are similar to those for crystal qualification:

1. Verify that the vendor's published specifications in the component datasheet meet or exceed the required IEEE specifications.
2. Independently measure the component's electrical parameters on the test bench, checking samples from multiple lots. Check that the measured behavior is consistent from sample to sample and that measurements meet the published specifications.
3. Perform physical layer conformance testing and EMC (FCC and EN) testing in real systems. Vary temperature and voltage while performing system level tests.

3.1.2.2 Modules for 1000 BASE-T Ethernet

Magnetics modules for 1000 BASE-T Ethernet are similar to those designed solely for 10/100 Mbps, except that there are four differential signal pairs instead of two. Use the following guidelines to verify specific electrical parameters:



1. Verify that the rated return loss is 19 dB or greater from 2 MHz through 30 MHz for 100 BASE-TX.
2. Verify that the rated return loss is 12 dB or greater at 80 MHz for 100 BASE-TX (the specification requires greater than or equal to 10 dB).
3. Verify that the rated return loss is 10 dB or greater at 100 MHz for 1000 BASE-TX (the specification requires greater than or equal to 8 dB).
4. Verify that the insertion loss is less than 1.0 dB at 100 kHz through 80 MHz for 100 BASE-TX.
5. Verify that the insertion loss is less than 1.4 dB at 100 kHz through 100 MHz for 1000 BASE-T.
6. Verify at least 30 dB of crosstalk isolation between adjacent channels (through 150 MHz).
7. Verify high voltage isolation to 15000 Vrms
8. Transmitter OCL should be greater than or equal to 350 μH with 8 mA DC bias.

3.2 Discrete Magnetics

Designs can use discrete magnetics also. The characteristics will be similar to those for integrated magnets.

When using discrete magnetics it is necessary to use Bob Smith termination: Use four 75 Ω resistors for cable-side center taps and unused pins. This method terminates pair-to-pair common mode impedance of the CAT5 cable.

Use an EFT capacitor attached to the termination plane. Suggested values are 1500 pF/ 2 kV or 1000 pF/3 kV. A minimum of 50-mil spacing from capacitor to traces and components should be maintained.

3.3 Third-Party Magnetics Manufacturers

The following magnetics modules have been used successfully in previous designs.

Manufacturer	Part Number
Pulse	JW0A2P019D
Discrete	H5007 Bel 0344FLA

3.4 Designing with the 82571EB/82572EI Gigabit Ethernet Controller

This section provides design guidelines specific to the 82571EB/82572EI controller.

3.4.1 LAN Disable for 82571EB/82572EI Gigabit Ethernet Controller

The 82571EB/82572EI device has three signals that can be used for disabling Ethernet functions from system BIOS. LAN0_DIS_N and LAN1_DIS_N are the separated port disable signals and DEV_OFF_N is the device disable signal. Each signal can be driven from a system output port. Choose outputs from devices that retain their values during reset. It is important not to use these signals to drive LAN0_DIS_N or LAN1_DIS_N because these inputs are latched upon the rising edge of PE_RSTn or an inband reset end. The DEV_OFF_N input is completely asynchronous and does not have this restriction.

Note: LAN0_DIS_N and LAN1_DIS_N cannot both be low at the same time; this is an invalid operating mode.

3.4.2 LAN Power Good Generation

No signal should be connected to pin R4 (LAN_PWR_GOOD); the 82571EB and 82572EI generates the LPG signal internally. The LPG signal at pin R4 will be held low for approximately 80ms after all voltages are stable and in the normal operating range.

This recommendation is to leave this input floating and not connect any reset line to this pin. Please note that this is different than previous Ethernet controllers. LPG is the fundamental device reset and is not intended for use as a LAN disable.

3.4.3 CDE Suppression

The 82571EB and 82572EI require external device protection for Cable Discharge Event (CDE) suppression. TVS diodes connected to the line side of the magnetics (between the magnetics module and RJ45 connector) have shown to be effective in suppressing CD events. Diodes with low capacitance should be used to minimize impacts to the return loss on the Ethernet interface.

The Low Capacitance TVS Array by Semtech, part number RClamp3304N, diodes have been successfully tested on the line side.

3.4.4 Serial EEPROM for 82571EB/82572EI Controller Implementations

The 82571EB/82572EI Gigabit Ethernet Controller uses an SPI* serial EEPROM. Several words of the EEPROM are accessed automatically by the device after reset to provide pre-boot configuration data before it is accessed by host software. The remainder of the EEPROM space is available to software for storing the MAC address, serial numbers, and additional information.

Intel has an MS-DOS* software utility called EEUPDATE, which can be used to program EEPROM images in development or production line environments. To obtain a copy of this program, contact your Intel representative.

Atmel's AT25128N and Microchips 25LC128 Serial EEPROMs have been fully validated with the device and are recommended.

Alternate SPI EEPROMs that have been found to work with the 82571EB/82572EI device are listed in Table 1. SPI EEPROMs must be rated for a clock rate of at least 2 MHz.

To determine the EEPROM size required for your application, follow the size guidance given in the *82571EB/82572EI EEPROM Information Guide, Application Note (AP-476)*.

Table 1. Alternative SPI Serial EEPROMs for 82571EB/82572EI Controller

Manufacturer	Size	Manufacturer's Part Number
Catalyst	32Kb	25C32S 0113A
Catalyst	8Kb	25C08S
Catalyst	64Kb	25C64S 0139B
STM	256Kb	95256W6 K350V
STM	64Kb	95640W6

Table 1. Alternative SPI Serial EEPROMs for 82571EB/82572EI Controller

Manufacturer	Size	Manufacturer's Part Number
STM	32Kb	95320W6
STM	16Kb	95160W6
STM	8Kb	95080W6
Motorola	64Kb	25AA640
Motorola	32kb	25AA320
Motorola	16Kb	25AA160A

For more information on the various manageability options, refer to Intel's Application Note 497, *82571/82572/ESB2 LAN System Management Bus.*

3.4.5 EEPROM Map Information

For more about the using an EEPROM, see the *82571EB/82572EI EEPROM Map and Programming Information Guide, Application Note (AP-476)*.

3.5 Manageability Connection Options

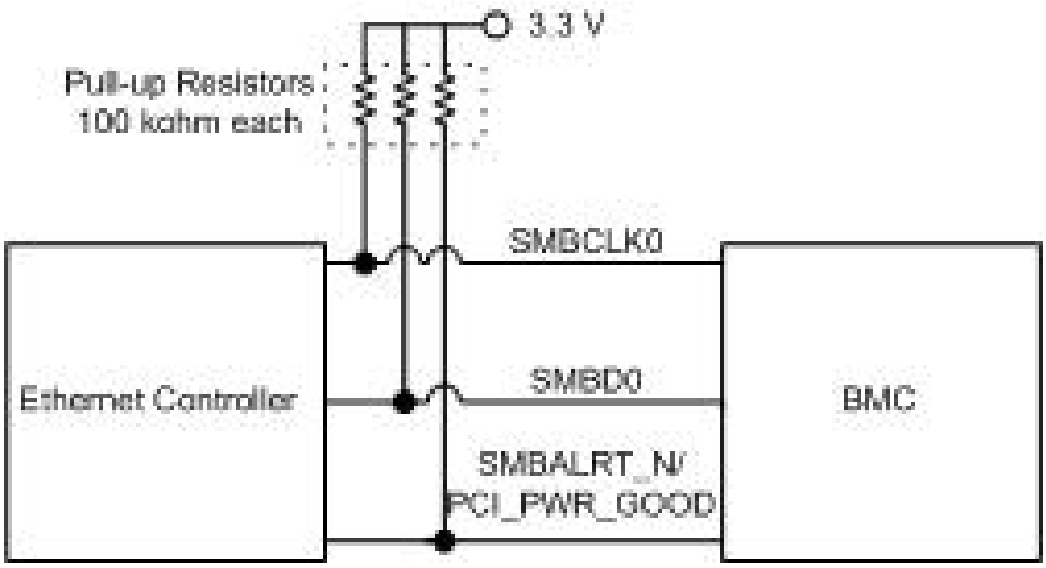


Figure 1. Connection Scheme for SMBus

Note: P12 (SMBD1) and P13 (SMBCLK1) are reserved. Do not use these pins. Connect them to 3.3 V through a 100 kom resistor.

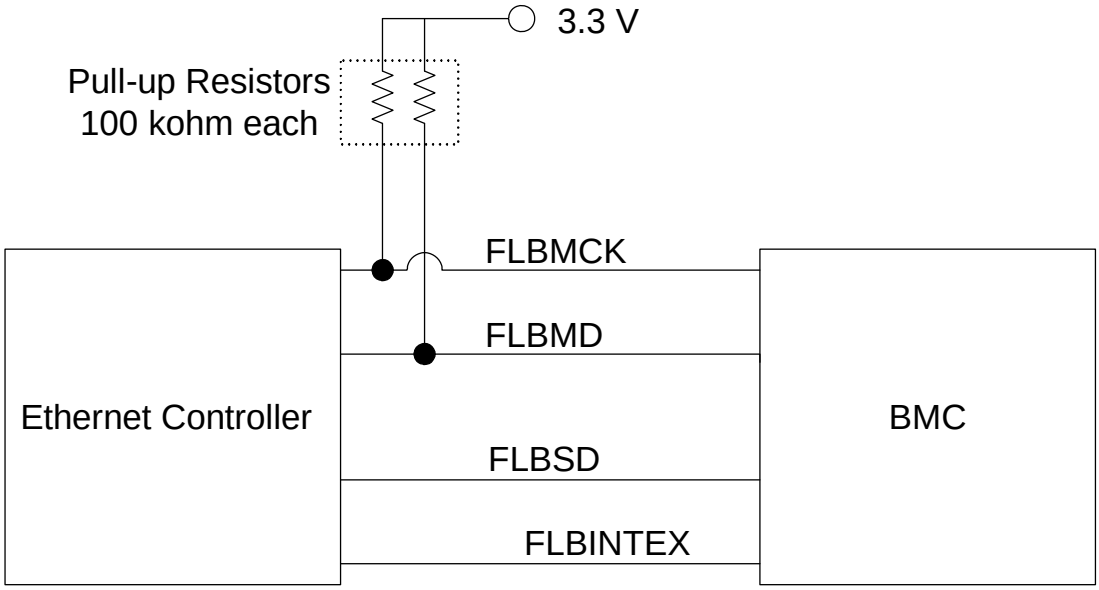


Figure 2. Connection Scheme for FML

3.6 Power Supplies for the 82571EB/82572EI Controllers

The 82571EB and 82572EI Gigabit Ethernet Controllers require three power rails: 3.3 V, 1.8 V and 1.1 V. (See the *82571EB/82572EB Product Datasheet* for power requirements.) A central power supply can provide all the required voltage sources, or the power can be derived from the 3.3 V supply and regulated locally using external regulators. If the LAN wake capability will be used, all voltages must remain present during system power down. Local regulation of the LAN voltages from system 3.3Vmain and 3.3 Vaux voltages is recommended.

External voltage regulators need to generate the proper voltage, supply current requirements (with adequate margin), and provide the proper power sequencing.

Due to the current demand, a Switching Voltage Regulator (SVR) is highly recommended for the 1.1 V power rail. Figure 1 shows an example of a compact, low-part count, SVR that can be used for both the 1.1 V and 1.8 V power supplies.

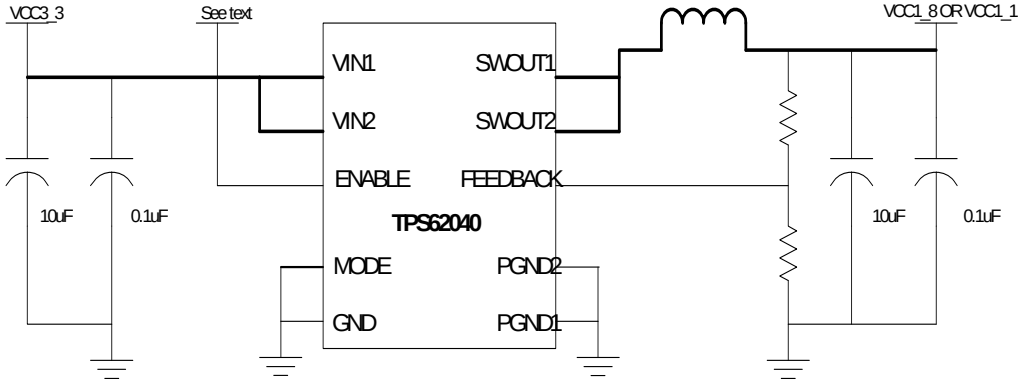


Figure 3. Example Switching Voltage Regulator for 1.1 V and 1.8 V

The 1.8 V rail has a lower current requirement; however, the use of a SVR is still recommended for adequate margin. Using an LVR in this application is acceptable as long as adequate margin exists in the design, and sequencing can be controlled. Figure 2 shows an example of a compact low-part -count LVR that could be used for the 1.8 V supply.

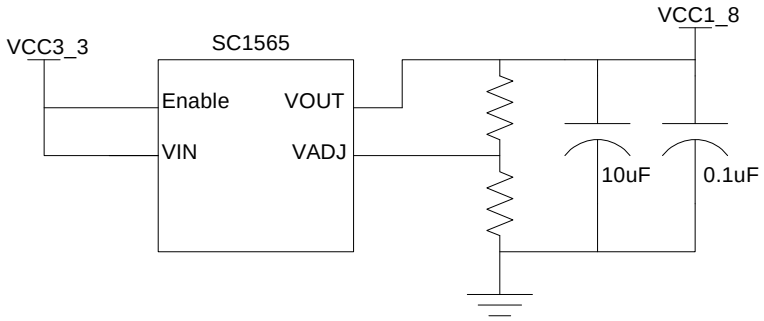


Figure 4. Example of Linear Voltage Regulator for 1.8 V power rail

3.6.1 82571EB/82572EI Power Sequencing

Regardless of which type of regulator used, all regulators need to adhere to the sequencing shown in Figure 5 to avoid latch-up and forward-biased internal diodes.

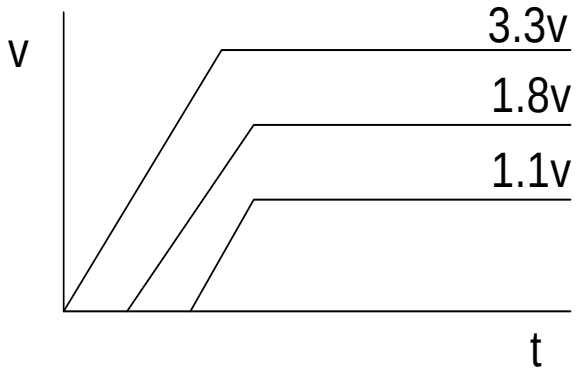


Figure 5. Proper power-up sequencing for 82571EB/82572EI

In addition, the following limitations exist:

- 1.8 V must not exceed 3.3 V.
- 1.1 V must not exceed 3.3 V.
- 1.1 V must not exceed 1.8 V.

The power supplies are all expected to ramp during a short power-up interval (approximately 20 ms or less). Do not leave the device in a prolonged state were some, but not all, voltages are applied. Also, for power down it is recommended all the voltage rails are removed as close together as possible.

3.6.1.1 Using Regulators With Enable Pins

The use of regulators with enable pins is very helpful in controlling sequencing. Connecting the enable of the 1.8 V regulator to 3.3 V will allow the 1.8 V to ramp as shown in Figure 3. Connecting the enable of the 1.1 V regulator to the 1.8 V output assures that the 1.1 V rail will ramp after the 1.8 V rail. This provides a quick solution to power sequencing. Make sure to check design parameters for inputs with this configuration. This is also adequate for power down as well.

3.6.2 82571EB/82572EI Device Power Supply Filtering

Provide several high-frequency bypass capacitors for each power rail (see table below), selecting values in the range of 0.01 µF to 0.1 µF. If possible, orient the capacitors close to the device and adjacent to power pads. Decoupling capacitors should connect to the power planes with short, thick (18 mils or more) traces and 14 mil vias. Long and thin traces are more inductive and would reduce the intended effect of decoupling capacitors.

Power Rail	4.7 uF or 10 uF	0.1 uF
3.3 V	1	2
1.8 V	1	4
1.1 V	1	6

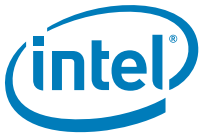


Table 2. **Table 2: Minimum Number of Bypass Capacitors per Power Rail.**

Furnish approximately 4.7 µF to 10 µF of bulk capacitance for all the power rails; placement should be as close to the device power connection as possible.

3.6.3 82571EB/82572EI Controller Power Management and Wake Up

The 82571EB/82572EI Gigabit Ethernet Controller supports low-power operation as defined in the PCI Bus Power Management Specification. There are two defined power states, D0 and D3. The D0 state provides full power operation and is divided into two sub-states: D0u (uninitialized) and D0a (active). The D3 state provides low-power operation and is also divided into two sub-states: D3hot and D3cold.

To enter the low-power state (D3), the software driver must stop data transmission and reception. Either the operating system or the driver must program the Power Management Control/Status Register (PMCSR) and the Wakeup Control Register (WUC). If wakeup is desired, the appropriate wakeup LAN address filters must also be set. The initial power management settings are specified by EEPROM bits.

When the 82571EB/82572EI controller transitions to either of the D3 low power states, the 1.1 V, 1.8 V, and 3.3 V sources must continue to be supplied to the device. Otherwise, it will not be possible to use a wakeup mechanism. The AUX_PWR signal is a logic input to the 82571EB/82572EI controller that denotes auxiliary power is available. If AUX_PWR is asserted, the 82571EB/82572EI device will advertise that it supports wake up from a D3cold state.

The 82571EB/82572EI device supports both Advanced Power Management (APM) wakeup and Advanced Configuration and Power Interface (ACPI) wakeup. APM wakeup has also been known in the past as “Wake on LAN” and as “Magic Packet Wake-up”.

Wakeup uses the PE_WAKEn signal to wake the system up. PE_WAKEn is an active low signal typically connected to a GPIO port on the chipset that goes active in response to receiving a “Magic Packet”, a network wakeup packet, or link status change indication. PE_WAKEn remains asserted until it is disabled through the 82571EB/82572EI’s Power Management Control/Status Register.

3.7 82571EB/82572EI Device Test Capability

The 82571EB/82572EI Gigabit Ethernet Controller contains a test access port (3.3 V only) conforming to the IEEE 1149.1a-1994 (JTAG) Boundary Scan specification. To use the test access port, connect these balls to pads accessible by your test equipment.

A BSDL (Boundary Scan Definition Language) file describing the 82571EB/82572EI device is available for use in your test environment. For information on the JTAG commands supported see the *PCIe* Family of Gigabit Ethernet Controllers Software Developer’s Manual* or the BSDL file.

Note: The optional JTAG IDCODE command is not support by the 82571EB/82572EI.

Information about how to obtain a BSDL file is available from your Intel representative.

4.0 Frequency Control Device Design Considerations

This section provides information regarding frequency control devices, crystals and oscillators, for use with all Intel Ethernet controllers. Several suitable frequency control devices are available; none of which present any unusual challenges in selection. The concepts documented herein are applicable to other data communication circuits, including Platform LAN Connect devices (PHYs).

The Intel Ethernet controllers contain amplifiers which, when used with the specific external components, form the basis for feedback oscillators. These oscillator circuits, which are both economical and reliable, are described in more detail in “Crystal Selection Parameters”.

The Intel Ethernet controllers also have bus clock input functionality, however a discussion of this feature is beyond the scope of this document, and will not be addressed.

The chosen frequency control device vendor should be consulted early in the design cycle. Crystal and oscillator manufacturers familiar with networking equipment clock requirements may provide assistance in selecting an optimum, low-cost solution.

Clock sources should not be placed near I/O ports or board edges. Radiation from these devices can couple onto the I/O ports and radiate beyond the system chassis. Crystals should not be placed near the Ethernet magnetic module to prevent interference

4.1 Frequency Control Component Types

Several types of third-party frequency reference components are currently marketed. A discussion of each follows, listed in preferred order.

4.1.1 Quartz Crystal

Quartz crystals are generally considered to be the mainstay of frequency control components due to their low cost and ease of implementation. They are available from numerous vendors in many package types and with various specification options.

4.1.2 Fixed Crystal Oscillator

A packaged fixed crystal oscillator comprises an inverter, a quartz crystal, and passive components conveniently packaged together. The device renders a strong, consistent square wave output. Oscillators used with microprocessors are supplied in many configurations and tolerances.

Crystal oscillators should be restricted to use in special situations, such as shared clocking among devices or multiple controllers. As clock routing can be difficult to accomplish, it is preferable to provide a separate crystal for each device.

For Intel Ethernet controllers, it is acceptable to overdrive the internal inverter by connecting a 25 MHz external oscillator to the XTAL1 lead, leaving the XTAL2 lead unconnected. The oscillator should be specified to drive CMOS logic levels, and the clock trace to the device should be as short as possible. Device specifications typically call for a 40% (minimum) to 60% (maximum) duty cycle and a ±50 ppm frequency tolerance.

Note: Please contact your Intel Customer Representative to obtain the most current device documentation prior to implementing this solution.

4.1.3 Programmable Crystal Oscillators

A programmable oscillator can be configured to operate at many frequencies. The device contains a crystal frequency reference and a phase lock loop (PLL) clock generator. The frequency multipliers and divisors are controlled by programmable fuses.

A programmable oscillator's accuracy depends heavily on the Ethernet device's differential transmit lines. The Physical Layer (PHY) uses the clock input from the device to drive a differential Manchester (for 10 Mbps operation), an MLT-3 (for 100 Mbps operation) or a PAM-5 (for 1000 Mbps operation) encoded analog signal across the twisted pair cable. These signals are referred to as self-clocking, which means the clock must be recovered at the receiving link partner. Clock recovery is performed with another PLL that locks onto the signal at the other end.

PLLs are prone to exhibit frequency jitter. The transmitted signal can also have considerable jitter even with the programmable oscillator working within its specified frequency tolerance. PLLs must be designed carefully to lock onto signals over a reasonable frequency range. If the transmitted signal has high jitter and the receiver's PLL loses its lock, then bit errors or link loss can occur.

PHY devices are deployed for many different communication applications. Some PHYs contain PLLs with marginal lock range and cannot tolerate the jitter inherent in data transmission clocked with a programmable oscillator. The American National Standards Institute (ANSI) X3.263-1995 standard test method for transmit jitter is not stringent enough to predict PLL-to-PLL lock failures, therefore, the use of programmable oscillators is generally not recommended.

4.1.4 Ceramic Resonator

Similar to a quartz crystal, a ceramic resonator is a piezoelectric device. A ceramic resonator typically carries a frequency tolerance of ±0.5%, – inadequate for use with Intel Ethernet controllers, and therefore, should not be used.

5.0 Crystal Selection Parameters

All crystals used with Intel Ethernet controllers are described as “AT-cut,” which refers to the angle at which the unit is sliced with respect to the long axis of the quartz stone. Table 4 lists crystals which have been used successfully in past designs (however no particular product is recommended):

Table 3. Crystal Manufacturers and Part Numbers

Manufacturer	Part No.
RALTRON	AS-25.000-20-F-SMD-T
CITIZEN AMERICA CORP	HCM4925.000MBBKTR
NDK AMERICA INC	41CD25.0S11005020
TXC CORPORATION - USA	6C25000131

Table 4 lists the crystal electrical parameters and provides suggested values for typical designs. The parameters are described in the subsections following the table.

Table 4. Crystal Parameters

Parameter	Suggested Value
Vibrational Mode	Fundamental
Nominal Frequency	25.000 MHz at 25° C (required)
Frequency Tolerance	±30 ppm recommended ±50 ppm across the entire operating temperature range (required by IEEE specifications)
Temperature Stability	±30 ppm at 0° C to 70° C
Calibration Mode	Parallel
Load Capacitance	16 pF to 20 pF
Shunt Capacitance	6 pF maximum
Equivalent Series Resistance	50 Ω maximum
Drive Level	0.5 mW maximum
Aging	±5 ppm per year maximum
Operating Temperature Range	-20 C to 70 C

Note: When placing the crystal, ensure that you follow the layout guidance given in section 7.13.

5.1 Vibrational Mode

Crystals in the above-referenced frequency range are available in both fundamental and third overtone. Unless there is a special need for third overtone, use fundamental mode crystals.

At any given operating frequency, third overtone crystals are thicker and more rugged than fundamental mode crystals. Third overtone crystals are more suitable for use in military or harsh industrial environments. Third overtone crystals require a trap circuit (extra capacitor and inductor) in the load circuitry to suppress fundamental mode oscillation as the circuit powers up. Selecting values for these components is beyond the scope of this document.

5.2 Nominal Frequency

Intel Ethernet controllers use a crystal frequency of 25.000 MHz. The 25 MHz input is used to generate a 125 MHz transmit clock for 100BASE-TX and 1000BASE-TX operation – 10 MHz and 20 MHz transmit clocks, for 10BASE-T operation.

5.3 Frequency Tolerance

The frequency tolerance for an Ethernet Platform LAN Connect is specified by the IEEE 802.3 specification as ±50 parts per million (ppm). This measurement is referenced to a standard temperature of 25° C. Intel recommends a frequency tolerance of ±30 ppm.

5.4 Temperature Stability and Environmental Requirements

Temperature stability is a standard measure of how the oscillation frequency varies over the full operational temperature range (and beyond). Several optional temperature ranges are currently available, including -40° C to +85° C for industrial environments. Some vendors separate operating temperatures from temperature stability. Manufacturers may also list temperature stability as 50 ppm in their data sheets.

Note: Crystals also carry other specifications for storage temperature, shock resistance, and reflow solder conditions. Crystal vendors should be consulted early in the design cycle to discuss the application and its environmental requirements.

5.5 Calibration Mode

The terms “series-resonant” and “parallel-resonant” are often used to describe crystal oscillator circuits. Specifying parallel mode is critical to determining how the crystal frequency is calibrated at the factory.

A crystal specified and tested as series resonant oscillates without problem in a parallel-resonant circuit, but the frequency is higher than nominal by several hundred parts per million. The purpose of adding load capacitors to a crystal oscillator circuit is to establish resonance at a frequency higher than the crystal’s inherent series resonant frequency.

Figure 3 illustrates a simplified schematic of the internal oscillator circuit. Pin X1 and X2 refers to XTAL1 and XTAL2 in the Ethernet device, respectively. The crystal and the capacitors form a feedback element for the internal inverting amplifier. This combination is called parallel-resonant, because it has positive reactance at the

selected frequency. In other words, the crystal behaves like an inductor in a parallel LC circuit. Oscillators with piezoelectric feedback elements are also known as “Pierce” oscillators.

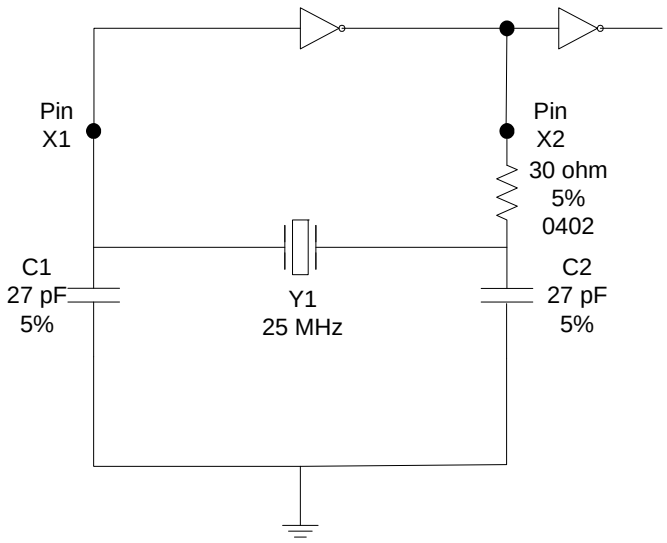


Figure 6. Internal Oscillator Circuit

5.6 Load Capacitance

The formula for crystal load capacitance is as follows:

$$C_L = \frac{(C1 \cdot C2)}{(C1 + C2)} + C_{stray}$$

where C1 = C2 = 27 pF
and C_{stray} = allowance for additional capacitance in pads, traces and the chip carrier within the Ethernet device package

An allowance of 3 pF to 7 pF accounts for lumped stray capacitance. The calculated load capacitance is 16 pF with an estimated stray capacitance of about 5 pF.

Individual stray capacitance components can be estimated and added. For example, surface mount pads for the load capacitors add approximately 2.5 pF in parallel to each capacitor. This technique is especially useful if Y1, C1 and C2 must be placed farther than approximately one-half (0.5) inch from the device. It is worth noting that thin circuit boards generally have higher stray capacitance than thick circuit boards. Consult the PCIe Design Guide for more information.

Standard capacitor loads used by crystal manufacturers include 16 pF, 18 pF and 20 pF. Any of these values will generally operate with the device. However, a difference of several picofarads between the calibrated load and the actual load will pull the oscillator slightly off frequency.

The oscillator frequency should be measured with a precision frequency counter where possible. The load specification or values of C1 and C2 should be fine tuned for the design. As the actual capacitance load increases, the oscillator frequency decreases.

Note: C1 and C2 may vary by as much as 5% (approximately 1 pF) from their nominal values.

5.7 Shunt Capacitance

The shunt capacitance parameter is relatively unimportant compared to load capacitance. Shunt capacitance represents the effect of the crystal's mechanical holder and contacts. The shunt capacitance should equal a maximum of 7 pF.

5.8 Equivalent Series Resistance

Equivalent Series Resistance (ESR) is the real component of the crystal's impedance at the calibration frequency, which the inverting amplifier's loop gain must overcome. ESR varies inversely with frequency for a given crystal family. The lower the ESR, the faster the crystal starts up. Use crystals with an ESR value of 50 Ω or better.

5.9 Drive Level

Drive level refers to power dissipation in use. The allowable drive level for a Surface Mounted Technology (SMT) crystal is less than its through-hole counterpart, because surface mount crystals are typically made from narrow, rectangular AT strips, rather than circular AT quartz blanks.

Some crystal data sheets list crystals with a maximum drive level of 1 mW. However, Intel Ethernet controllers drive crystals to a level less than the suggested 0.5 mW value. This parameter does not have much value for on-chip oscillator use.

5.10 Aging

Aging is a permanent change in frequency (and resistance) occurring over time. This parameter is most important in its first year because new crystals age faster than old crystals. Use crystals with a maximum of ±5 ppm per year aging.

5.11 Reference Crystal

The normal tolerances of the discrete crystal components can contribute to small frequency offsets with respect to the target center frequency. To minimize the risk of tolerance-caused frequency offsets causing a small percentage of production line units to be outside of the acceptable frequency range, it is important to account for those shifts while empirically determining the proper values for the discrete loading capacitors, C1 and C2.

Even with a perfect support circuit, most crystals will oscillate slightly higher or slightly lower than the exact center of the target frequency. Therefore, frequency measurements (which determine the correct value for C1 and C2) should be performed with an ideal reference crystal. When the capacitive load is exactly equal to the crystal's load rating, an ideal reference crystal will be perfectly centered at the desired target frequency.

5.11.1 Reference Crystal Selection

There are several methods available for choosing the appropriate reference crystal:

- If a Saunders and Associates (S&A) crystal network analyzer is available, then discrete crystal components can be tested until one is found with zero or nearly zero ppm deviation (with the appropriate capacitive load). A crystal with zero or near zero ppm deviation will be a good reference crystal to use in subsequent frequency tests to determine the best values for C1 and C2.
- If a crystal analyzer is not available, then the selection of a reference crystal can be done by measuring a statistically valid sample population of crystals, which has units from multiple lots and approved vendors. The crystal, which has an oscillation frequency closest to the center of the distribution, should be the reference crystal used during testing to determine the best values for C1 and C2.
- It may also be possible to ask the approved crystal vendors or manufacturers to provide a reference crystal with zero or nearly zero deviation from the specified frequency when it has the specified CLoad capacitance.

When choosing a crystal, customers must keep in mind that to comply with IEEE specifications for 10/100 and 10/100/1000Base-T Ethernet LAN, the transmitter reference frequency must be precise within ±50 ppm. Intel recommends that customers use a transmitter reference frequency that is accurate to within ±30 ppm to account for variations in crystal accuracy due to crystal manufacturing tolerance.

5.11.2 Circuit Board

Since the dielectric layers of the circuit board are allowed some reasonable variation in thickness, the stray capacitance from the printed board (to the crystal circuit) will also vary. If the thickness tolerance for the outer layers of dielectric are controlled within ±17 percent of nominal, then the circuit board should not cause more than ±2 pF variation to the stray capacitance at the crystal. When tuning crystal frequency, it is recommended that at least three circuit boards are tested for frequency. These boards should be from different production lots of bare circuit boards.

Alternatively, a larger sample population of circuit boards can be used. A larger population will increase the probability of obtaining the full range of possible variations in dielectric thickness and the full range of variation in stray capacitance.

Next, the exact same crystal and discrete load capacitors (C1 and C2) must be soldered onto each board, and the LAN reference frequency should be measured on each circuit board.

The circuit board, which has a LAN reference frequency closest to the center of the frequency distribution, should be used while performing the frequency measurements to select the appropriate value for C1 and C2.

5.11.3 Temperature Changes

Temperature changes can cause the crystal frequency to shift. Therefore, frequency measurements should be done in the final system chassis across the system's rated operating temperature range.

6.0 Oscillator Support

The 82571EB/82572EI clock input circuit is optimized for use with an external crystal. However, an oscillator can also be used in place of the crystal with the proper design considerations:

- The clock oscillator has an internal voltage regulator of 1.2 V to isolate it from the external noise of other circuits to minimize jitter. If an external clock is used, this imposes a maximum input clock amplitude of 1.2 V.
- The input capacitance introduced by the 82571EB/82572EI (approximately 20 pF) is greater than the capacitance specified by a typical oscillator (approximately 15 pF).
- The input clock jitter from the oscillator can impact the 82571EB/82572EI clock and its performance.

Table 5. 82571EB/82572EI Clock Oscillator Specifications

Symbol	Parameter	Specifications			Units
		Min	Typical	Max	
f0	Frequency	-	25	-	MHz
df0	Frequency Variation	-50	-	+50	ppm
Dc	Duty Cycle	40	-	60	%
tr	Rise Time	-	-	5	ns
tf	Fall Time	-	-	5	ns
σi	Clock Jitter, rms (if specified)	-	-	50	ps
C1	Clock Capacitance (pushed by clock)	-	15	50	pF
VDD	Supply Voltage	-	3.3	-	V
Operating temperature	-	-	-	70	° C
CMOS output levels	Voltage Output High (V_{oh}), Voltage Output Low (V_{ol})	80% VDD	-	 20% VDD	V V

Note: The power consumption of additional circuitry equals about 1.5 mW.

The following table lists oscillators that have been used successfully in past designs (however, no particular product is recommended):

Table 6. Oscillator Manufacturers and Part Numbers

Manufacturer	Part No.
RALTRON	CO4305-25.000-TR
CITIZEN AMERICA CORP	CSX750FBB25.000MTR

6.1 Oscillator Solution

There are two possible oscillator solutions: high voltage and low voltage.

6.1.1 High Voltage Solution (VDD=3.3V)

This solution involves capacitor C1, which forms a capacitor divider with C_{stray} of about 20 pF. This attenuates the input clock amplitude and adjusts the clock oscillator load capacitance.

V_{in} = VDD * (C1/(C1 + C_{stray}))

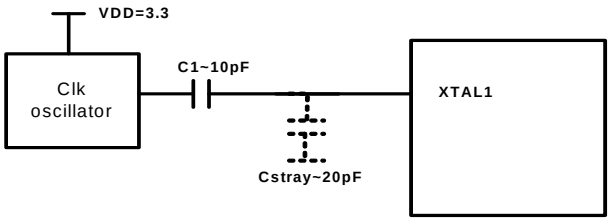
V_{in} = 3.3 * (C1/(C1 + C_{stray}))

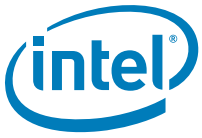
This enables load clock oscillators of 15 pF to be used. If the value of C_{stray} is unknown, C1 should be adjusted by tuning the input clock amplitude to approximately 1 V_{ptp}. If C_{stray} equals 20 pF, then C1 is 10 pF ±10%.

A low capacitance, high impedance probe (C < 1 pF, R > 500 KΩ) should be used for testing. Probing the parameters can affect the measurement of the clock amplitude and cause errors in the adjustment. A test should also be done after the probe has been removed for circuit operation.

If jitter performance is poor, a lower jitter clock oscillator can be implemented.

Note: Cstray shown in the figure below is not an actual discrete capacitor, but a representation of the board capacitance and should not be placed in the design itself.





7.0 Ethernet Component Layout Guidelines

These sections provide recommendations for performing printed circuit board layouts. Good layout practices are essential to meet IEEE PHY conformance specifications and EMI regulatory requirements.

7.1 Layout Considerations for 82571EB/82572EI Ethernet Controllers

Critical signal traces should be kept as short as possible to decrease the likelihood of being affected by high frequency noise from other signals, including noise carried on power and ground planes. Keeping the traces as short as possible can also reduce capacitive loading.

Since the transmission line medium extends onto the printed circuit board, special attention must be paid to layout and routing of the differential signal pairs.

Designing for 1000 BASE-T Gigabit operation is very similar to designing for 10 and 100 Mbps. For the 82571EB/82572EI Gigabit Ethernet controller, system level tests should be performed at all three speeds.

Designing for 1000 BASE-SX operation requires less attention to the physical transmission medium because the optical transceivers are manufactured as closed, tested units. However, the analog signals between the 82571EB/82572EI controller's SERDES outputs and the optical transceivers run at Gigahertz speeds, requiring careful attention to layout and routing.

Designing for SERDES backplane operation (SERDES-to-SERDES) is similar to designing for 1000 BASE-SX, but the analog traces are longer. For more information regarding SERDES designs, please see the application note: *Designing SERDES Applications--82545/82546, 82571/82572 & 631xESB/632xESB Application Note--AN498*.

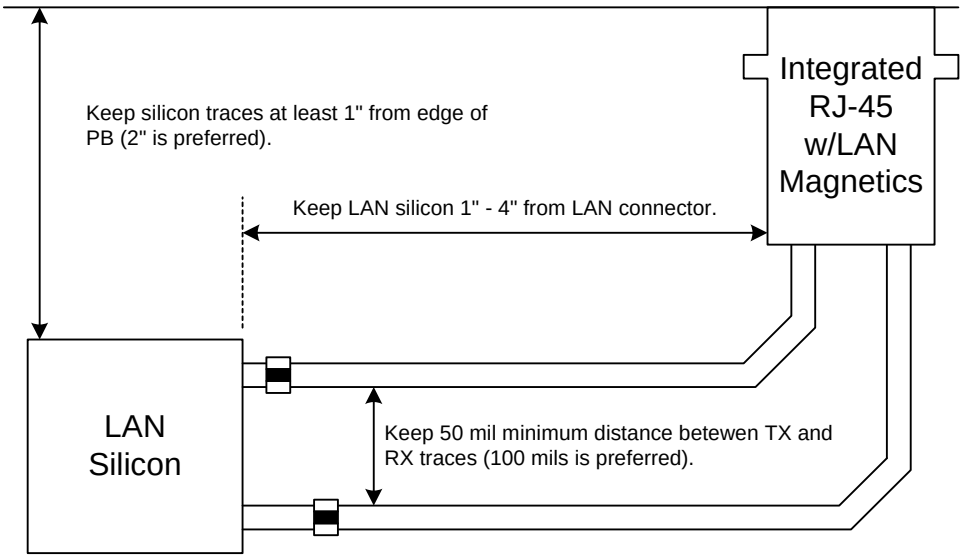
7.1.1 Guidelines for Component Placement

Component placement can affect signal quality, emissions, and component operating temperature This section provides guidelines for component placement.

Careful component placement can:

- Decrease potential problems directly related to electromagnetic interference (EMI), which could cause failure to meet applicable government test specifications.
- Simplify the task of routing traces. To some extent, component orientation will affect the complexity of trace routing. The overall objective is to minimize turns and crossovers between traces.

Minimizing the amount of space needed for the Ethernet LAN interface is important because other interfaces will compete for physical space on a motherboard near the connector. The Ethernet LAN circuits need to be as close as possible to the connector.



NOTE: This figure represents a 10/100 diagram. Use the same design considerations for the two differential pairs not shown for gigabit implementations.

Figure 7. General Placement Distances for 1000 BASE-T Designs

Figure 5 shows some basic placement distance guidelines. The figure shows two differential pairs, but can be generalized for a Gigabit system with four analog pairs. The ideal placement for the Ethernet silicon would be approximately one inch behind the magnetics module.

While it is generally a good idea to minimize lengths and distances, this figure also illustrates the need to keep the LAN silicon away from the edge of the board and the magnetics module for best EMI performance.

7.1.2 Crystals and Oscillators

Clock sources should not be placed near I/O ports or board edges. Radiation from these devices can couple onto the I/O ports and radiate beyond the system chassis. Crystals should not be placed near the Ethernet magnetic module to prevent interference

7.1.3 Crystal Device Placement and Layout Considerations

Note: Failure to follow these guidelines can result in the 25 MHz clock failing to start.

When designing the layout for the crystal circuit, the following rules must be used:

- Place load capacitors as close as possible (within design-for-manufacturability rules) to the crystal solder pads. They should be no more than 90 mils away from crystal pads.
- The two load capacitors, crystal component, the Ethernet controller device, and the crystal circuit traces must all be located on the same side of the circuit board (maximum of one via-to-ground load capacitor on each Xtal trace).

- Use 27 pF (5% tolerance) 0402 load capacitors.
- Place load capacitor solder pad directly in line with circuit trace (see Figure 8, point A).
- Place a 30-ohm (5% tolerance) 0402 series resistor on Xtal2. (see Figure 8, point C). The placement of the resistor along the Xtal trace is flexible, as long as it is between the controller and load capacitor.
- Use 50-ohm impedance single-ended microstrip traces for the crystal circuit.
- Route traces so that electro-magnetic fields from Xtal2 do not couple onto Xtal1. No differential traces.
- Route Xtal1 and Xtal2 traces to nearest inside corners of crystal pad (see Figure 8, point B).
- Ensure that the traces from Xtal1 and Xtal2 are symmetrically routed and that their lengths are matched.
- The total trace length of Xtal1 or Xtal2 should be less than 750 mils.

Refer to the following diagram for an example of a good layout.

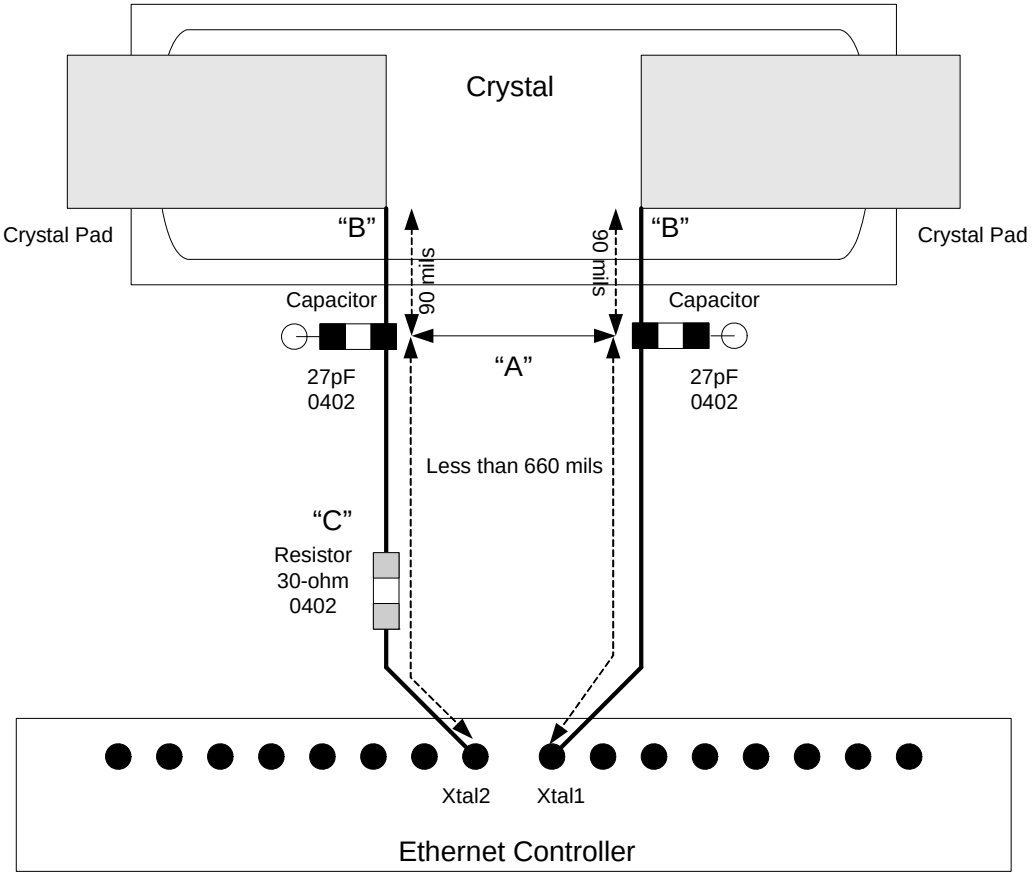


Figure 8. Recommended Crystal Placement and Layout

7.1.4 Board Stack Up Recommendations

Printed circuit boards for these designs typically have six, eight, or more layers. Although, the 82571/82572 does not dictate the stackup, here is an example of a typical six-layer board stackup:

- Layer 1 is a signal layer. It can contain the differential analog pairs from the Ethernet device to the magnetics module, or to an optical transceiver.
- Layer 2 is a signal ground layer. Chassis ground may also be fabricated in Layer 2 under the connector side of the magnetics module.
- Layer 3 is used for power planes.
- Layer 4 is a signal layer.
- Layer 5 is an additional ground layer.
- Layer 6 is a signal layer. For 1000 BASE-T (copper) Gigabit designs, it is common to route two of the differential pairs (per port) on this layer.

This board stack up configuration can be adjusted to conform to your company's design rules

7.1.5 Differential Pair Trace Routing for 10/100/1000 Designs

Trace routing considerations are important to minimize the effects of crosstalk and propagation delays on sections of the board where high-speed signals exist. Signal traces should be kept as short as possible to decrease interference from other signals, including those propagated through power and ground planes. Observe the following suggestions to help optimize board performance:

- Maintain constant symmetry and spacing between the traces within a differential pair.
- Minimize the difference in signal trace lengths of a differential pair.
- Keep the total length of each differential pair under 4 inches. Although possible, designs with differential traces longer than 5 inches are much more likely to have degraded receive BER (Bit Error Rate) performance, IEEE PHY conformance failures, and/or excessive EMI (Electromagnetic Interference) radiation.
- Do not route a pair of differential traces closer than 100 mils to another differential pair.
- Do not route any other signal traces parallel to the differential traces, and closer than 100 mils to the differential traces (300 mils is recommended).
- Keep maximum separation within differential pairs to 7 mils.
- For high-speed signals, the number of corners and vias should be kept to a minimum. If a 90° bend is required, it is recommended to use two 45° bends instead. Refer to Figure 9.
- Traces should be routed away from board edges by a distance greater than the trace height above the reference plane. This allows the field around the trace to couple more easily to the ground plane rather than to adjacent wires or boards.
- Do not route traces and vias under crystals or oscillators. This will prevent coupling to or from the clock. And as a general rule, place traces from clocks and drives at a minimum distance from apertures by a distance that is greater than the largest aperture dimension

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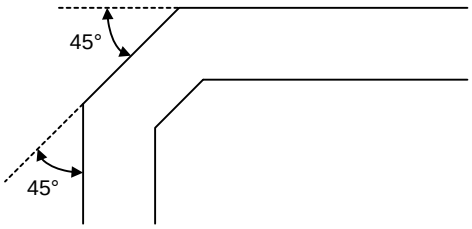


Figure 9. Trace Routing

- The reference plane for the differential pairs should be continuous and low impedance. It is recommended that the reference plane be either ground or 1.8V (the voltage used by the PHY). This provides an adequate return path for and high frequency noise currents.
- Do not route differential pairs over splits in the associated reference plane as it may cause discontinuity in impedances.

7.1.5.1 Signal Termination and Coupling

The four differential pairs of each port are terminated with 49.9 Ω (1% tolerance) resistors, placed near the 82571EB/82572EI controller. One resistor connects to the MDI+ signal trace and another resistor connects to the MDI- signal trace. The opposite ends of the resistors connect together and to ground through a single 0.1μF capacitor. The capacitor should be placed as close as possible to the 49.9 ohm resistors, using a wide trace. Stubs created by the 49.9 Ω (1% tolerance) termination resistors should be kept at a minimum.

Do not vary the suggested component values. Be sure to lay out symmetrical pads and traces for these components such that the length and symmetry of the differential pairs are not disturbed.

7.1.6 Signal Trace Geometry for 1000 BASE-T Designs

The key factors in controlling trace EMI radiation are the trace length and the ratio of trace-width to trace-height above the reference plane. To minimize trace inductance, high-speed signals and signal layers that are close to a reference or power plane should be as short and wide as practical. Ideally, this trace width to height above the ground plane ratio is between 1:1 and 3:1. To maintain trace impedance, the width of the trace should be modified when changing from one board layer to another if the two layers are not equidistant from the neighboring planes.

Each pair of signal should have a differential impedance of 100 Ω. +/- 15%. If a particular tool cannot design differential traces, it is permissible to specify 55-65 Ω single-ended traces as long as the spacing between the two traces is minimized. As an example, consider a differential trace pair on Layer 1 that is 8 mils (0.2 mm) wide and 2 mils (0.05 mm) thick, with a spacing of 8 mils (0.2 mm). If the fiberglass layer is 8 mils (0.2mm) thick with a dielectric constant, E_R, of 4.7, the calculated single-ended impedance would be approximately 61 Ω and the calculated differential impedance would be approximately 100 Ω.

When performing a board layout, do not allow the CAD tool auto-router to route the differential pairs without intervention. In most cases, the differential pairs will have to be routed manually.

Note: Measuring trace impedance for layout designs targeting 100 Ω often results in lower actual impedance. Designers should verify actual trace impedance and adjust the layout accordingly. If the actual impedance is consistently low, a target of 105 Ω– 110 Ω should compensate for second order effects.

It is necessary to compensate for trace-to-trace edge coupling, which can lower the differential impedance by up to 10 Ω, when the traces within a pair are closer than 30 mils (edge to edge).

7.1.7 Trace Length and Symmetry for 1000 BASE-T Designs

As indicated earlier, the overall length of differential pairs should be less than four inches measured from the Ethernet device to the magnetics.

The differential traces (within each pair) should be equal in total length to within 50 mils (1.25 mm) and as symmetrical as possible. Asymmetrical and unequal length traces in the differential pairs contribute to common mode noise. If a choice has to be made between matching lengths and fixing symmetry, more emphasis should be placed on fixing symmetry. Common mode noise can degrade the receive circuit's performance and contribute to radiated emissions.

7.1.8 Trace Routing, Geometry and Length for SERDES-Based designs

Layout considerations for 1000BASE-SX and SERDES backplane designs are very similar to those for 1000BASE-T indicated in the preceding sections. The data lines are clocked at a 1.25 GHz rate over differential pairs with a target differential impedance of 100 Ω. Board traces are likely to require manual routing.

The differential pairs between the SERDES pins and an optical transceiver should be routed to be as short and symmetrical as possible. Asymmetrical and unequal length traces in the differential pairs contribute to common mode noise. The length of the traces is not as critical as the length of the analog traces in 1000BASE-T designs. Intel® PRO/1000 Gigabit Ethernet Adapters are manufactured with board traces as long as approximately seven inches between SERDES pins and optical transceiver.

SERDES point-to-point and backplane designs require special layout attention because the trace lengths are typically much longer than seven inches. The key design consideration is making the traces *thick* enough to minimize resistive losses while still maintaining 100 Ω differential impedance.

The lengths of the differential traces (within each pair) should be equal within 10 mils (0.25 mm). The distance from trace to trace within each pair should be minimized. Six mil (0.15 mm) trace spacing is good. To further reduce crosstalk interference on signals between pairs, the minimum distance between unlike differential pairs must be 50 mils (1.25 mm).

As with copper-based designs, SERDES-based designs must not have bends tighter than 45 degrees.

7.1.8.1 Signal Termination and Coupling

Intel recommends AC coupling in SERDES-based Gigabit designs. Carefully design 0.01 µF capacitors in series with the SERDES traces. Many optical transceivers contain internal AC coupling capacitors, simplifying the design.

7.1.8.2 Signal Detect

Each port of the 82571EB/82572EI controller has a Signal Detect pin for connection to optical transceivers. For designs without optical transceivers, these signals can be left unconnected because they have internal pull-up resistors. Signal Detect is not a high speed signal and does not require special layout. For more information on SerDes based design see Application note (AP-498) Designing SerDes applications.

7.1.9 Impedance Discontinuities

Impedance discontinuities cause unwanted signal reflections. Minimize vias (signal through holes) and other transmission line irregularities. If vias must be used, a reasonable budget is two per differential trace. Unused pads and stub traces should also be avoided.

7.1.10 Reducing Circuit Inductance

Traces should be routed over a continuous reference plane with no interruptions. If there are vacant areas on a reference or power plane, the signal conductors should not cross the vacant area. This causes impedance mismatches and associated radiated noise levels. Noisy logic grounds should be separated from analog signal grounds to reduce coupling, However, in most designs one ground plane is sufficient for the analog and digital grounds of the 82571/82572. Noisy logic grounds can sometimes affect sensitive DC subsystems such as analog to digital conversion, operational amplifiers, etc. All ground vias should be connected to every ground plane; and similarly, every power via, to all power planes at equal potential. This helps reduce circuit inductance. Another recommendation is to physically locate grounds to minimize the loop area between a signal path and its return path. Rise and fall times should be as slow as possible. Because signals with fast rise and fall times contain many high frequency harmonics, which can radiate significantly. The most sensitive signal returns closest to the chassis ground should be connected together. This will result in a smaller loop area and reduce the likelihood of crosstalk. The effect of different configurations on the amount of crosstalk can be studied using electronics modeling software.

7.1.11 Signal Isolation

To maintain best signal integrity, keep digital signals far away from the analog traces. A good rule of thumb is no digital signal should be within 300 mils (7.5mm) of the differential pairs. If digital signals on other board layers cannot be separated by a ground plane, they should be routed perpendicular to the differential pairs. If there is another LAN controller on the board, take care to keep the differential pairs from that circuit away.

Some rules to follow for signal isolation:

- Separate and group signals by function on separate layers if possible. If possible, maintain a gap of 100 mils between all differential pairs (Ethernet) and other nets, but group associated differential pairs together. Note: Over the length of the trace run, each differential pair should be at least 0.3 inches away from any parallel signal traces.
- Physically group together all components associated with one clock trace to reduce trace length and radiation.
- Isolate I/O signals from high-speed signals to minimize crosstalk, which can increase EMI emission and susceptibility to EMI from other signals.
- Avoid routing high-speed LAN traces near other high-frequency signals associated with a video controller, cache controller, processor, or other similar devices.

7.1.12 Power and Ground Planes

Good grounding requires minimizing inductance levels in the interconnections and keeping ground returns short, signal loop areas small, and power inputs bypassed to signal return, will significantly reduce EMI radiation.

The following guidelines help reduce circuit inductance in both backplanes and motherboards:

- Route traces over a continuous plane with no interruptions. Do not route over a split power or ground plane. If there are vacant areas on a ground or power plane, avoid routing signals over the vacant area. This will increase inductance and EMI radiation levels.
- Separate noisy digital grounds from analog grounds to reduce coupling. Noisy digital grounds may affect sensitive DC subsystems, however, in most designs one ground plane is sufficient for the analog and digital grounds of the 82571/82572
- All ground vias should be connected to every ground plane; and every power via should be connected to all power planes at equal potential. This helps reduce circuit inductance.
- Physically locate grounds between a signal path and its return. This will minimize the loop area.
- Avoid fast rise/fall times as much as possible. Signals with fast rise and fall times contain many high frequency harmonics, which can radiate EMI.
- The ground plane beneath a magnetics module should be split. The RJ45 connector side of the transformer module should have chassis ground beneath it.

7.1.13 Traces for Decoupling Capacitors

Traces between decoupling and I/O filter capacitors should be as short and wide as practical. Long and thin traces are more inductive and would reduce the intended effect of decoupling capacitors. Also for similar reasons, traces to I/O signals and signal terminations should be as short as possible. Vias to the decoupling capacitors should be sufficiently large in diameter to decrease series inductance.

7.1.14 Ground Planes Under a Magnetics Module (copper-based Gigabit designs)

The magnetics module chassis or output ground (secondary side of transformer) should be separated from the digital or input ground (primary side) by a physical separation of 100 mils minimum. (See Figure 10.) Splitting the ground planes beneath the

transformer minimizes noise coupling between the primary and secondary sides of the transformer and between the adjacent coils in the magnetics. This arrangement also improves the common mode choke functionality of magnetics module.

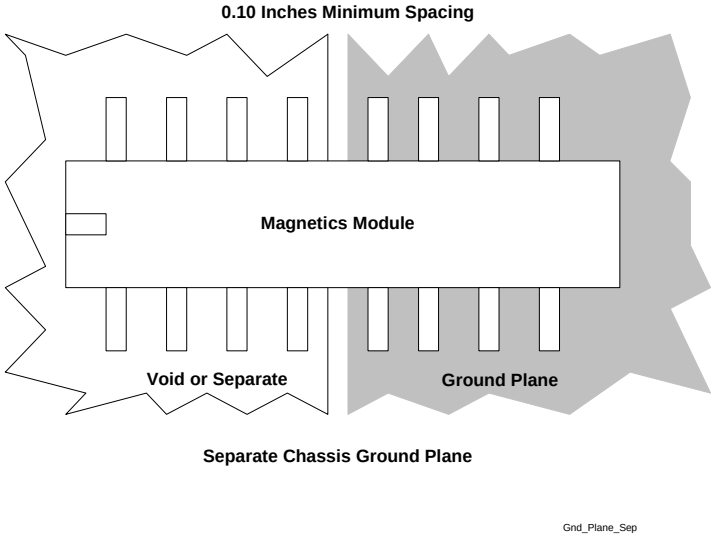


Figure 10. Ground Plane Separation

Figure 10 illustrates the split plane layout for a discrete magnetics module. Capacitors are used to interconnect chassis ground and signal ground.

Figure 11 below shows the preferred method for implementing a ground split under an integrated magnetics module/RJ-45 connector. This example shows a single port jack, but the same technique applies to a dual integrated module. The capacitor stuffing options (C1 – C6) are used to reduce/filter high frequency emissions. The value(s) of the capacitor stuffing options may be different for each board. Experiments will need to be performed to determine which value(s) provide best EMI performance. See the following diagram.

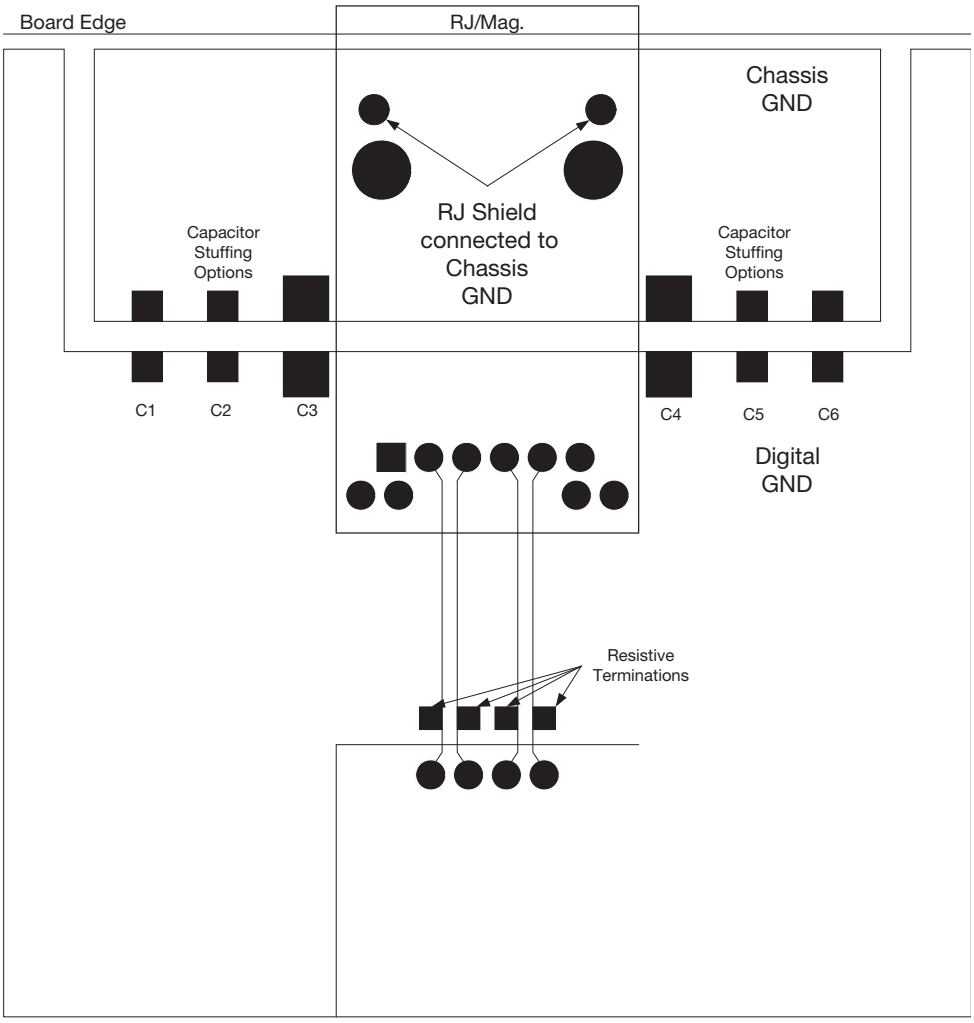


Figure 11. Ideal Ground Split Implementation

The table below gives some starting values for these capacitors.

Capacitors	Value
C3, C4	4.7µF or 10 µF
C1, C2, C5, C6	470 pF to 0.1 µF

The placement of C1 – C6 may also be different for each board design (i.e., not all of the capacitors may need to be populated). Also, the capacitors may not be needed on both sides of the magnetic module.

7.1.15 Light Emitting Diodes for Designs Based on 82571EB/82572EI Controller

The 82571EB/82572EI controller provides four programmable high-current outputs per port to directly drive LEDs for link activity and speed indication. Since the LEDs are likely to be integral to a magnetics module, take care with care to route the LED traces away from potential sources of EMI noise. In some cases, it may be desirable to attach filter capacitors.

7.1.16 Thermal Design Considerations

The 82571EB/82572EI Gigabit Ethernet Controller requires a heatsink under certain conditions. Please refer to the *82571EB/82572EI Gigabit Ethernet Controller Product Datasheet* and the *82571EB/82572EB Thermal Application Note, AP-490.*

IcePak* and FlowTherm* models are available; contact your Intel representative for information.

7.2 Physical Layer Conformance Testing

Physical layer conformance testing (also known as IEEE testing) is a fundamental capability for all companies with Ethernet LAN products. PHY testing is the final determination that a layout has been performed successfully. If your company does not have the resources and equipment to perform these tests, consider contracting the tests to an outside facility.

7.2.1 Conformance Tests for 10/100/1000 Mbps Designs

Crucial tests are as follows, listed in priority order:

- Bit Error Rate (BER). Good indicator of real world network performance. Perform bit error rate testing with long and short cables and many link partners. The test limit is 10^{-11} errors.
- Output Amplitude, Rise and Fall Time (10/100Mbps), Symmetry and Droop (1000Mbps). For the 82571EB/82572EI controller, use the appropriate PHY test waveform.
- Return Loss. Indicator of proper impedance matching, measured through the RJ-45 connector back toward the magnetics module.
- Jitter Test (10/100Mbps) or Unfiltered Jitter Test (1000Mbps). Indicator of clock recovery ability (master and slave for Gigabit controller).

7.2.2 Conformance Tests for 1000 BASE-SX Designs

Physical layer conformance tests for optical fiber designs are more specialized than tests for copper Gigabit designs and require an optical adapter for the network analyzer.

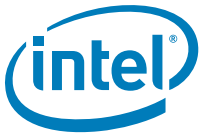
Important tests for 1000 BASE-SX designs are as follows (listed in priority order):

- Bit Error Rate. The test limit for the fiber implementation is 10^{-12} errors.
- Jitter. Indication of clock integrity.
- Extinction Ratio and Launch Power. Tests specific to fiber Ethernet implementations.

7.3 Troubleshooting Common Physical Layout Issues

The following is a list of common physical layer design and layout mistakes in LAN On Motherboard Designs.

1. Lack of symmetry between the two traces within a differential pair. Asymmetry can create common-mode noise and distort the waveforms. For each component and/or via that one trace encounters, the other trace should encounter the same component or a via at the same distance from the Ethernet silicon.
2. Unequal length of the two traces within a differential pair. Inequalities create common-mode noise and will distort the transmit or receive waveforms.
3. Excessive distance between the Ethernet silicon and the magnetics. Long traces on FR4 fiberglass epoxy substrate will attenuate the analog signals. In addition, any impedance mismatch in the traces will be aggravated if they are longer than the four inch guideline.
4. Routing any other trace parallel to and close to one of the differential traces. Crosstalk getting onto the receive channel will cause degraded long cable BER. Crosstalk getting onto the transmit channel can cause excessive EMI emissions and can cause poor transmit BER on long cables. At a minimum, other signals should be kept 0.3 inches from the differential traces.
5. Routing one pair of differential traces too close to another pair of differential traces. After exiting the Ethernet silicon, the trace pairs should be kept 0.3 inches or more away from the other trace pairs. The only possible exceptions are in the vicinities where the traces enter or exit the magnetics, the RJ-45 connector, and the Ethernet silicon.
6. Use of a low quality magnetics module.
7. Re-use of an out-of-date physical layer schematic in a Ethernet silicon design. The terminations and decoupling can be different from one PHY to another.
8. Incorrect differential trace impedances. It is important to have ~100 W impedance between the two traces within a differential pair. This becomes even more important as the differential traces become longer. To calculate differential impedance, many impedance calculators only multiply the single-ended impedance by two. This does not take into account edge-to-edge capacitive coupling between the two traces. When the two traces within a differential pair are kept close to each other, the edge coupling can lower the effective differential impedance by 5 W to 20 W. Short traces will have fewer problems if the differential impedance is slightly off target.



8.0 Reference Design Bill of Materials

The lists below are the bill of materials for Intel's reference designs.

8.1 82571EB Copper-Based Reference Design (w/ Integrated Magnetics Module) Bill of Material (represents two ports populated the same)

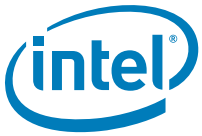
DNP = Do Not Populate

Item	Qty	Part Description	Comments
1	4	CAPC,C0G,0603,470.000 PF,50.000V, 5%	
2	2	CAPC,NPO0603,50V,27PF,5%	
3	3	CAPC,X5R,1206,10.000 UF,6.300V, 20%	
4	9	CAPC,Y5V,0603,0.100 UF,25.000V,20%>	
5	8	CAPC,Y5V,0603,0.100 UF,25.000V,20%>	
6	1	CAPC,Y5V,0603,0.100 UF,25.000V,20%>	
7	17	CAPC,Y5V,0603,25V,.1UF	
8	2	CAPC,Y5V,0603,25V,.1UF	
9	2	CONN, INTEGRATED MAGNETICS MODULE	
10	1	CONN,HDR,1X2,PLG,VT,0.1,093ST,KP	IEEE_TEST - Populate only for testing
11	1	CONN,HDR,1X2,PLG,VT,0.1,093ST,KP	IEEE_TEST - Populate only for testing
12	1	IC,CS,82571EB,C	82571EB LAN Controller
13	1	IC,EEPROM,BL,SOIC,2.1MHZ,1024X8	EEPROM
14	1	IC,FLASH,AT25F1024N-1,8,SOIC,NA	FLASH
15	1	RES D,0603,0.00 OHM,5.00%,1/16W	
16	7	RESD,0603,3.3K,5.00%,1/16W	
17	8	RESD,0603,10K,5.00%,1/16W	9 if not using aux power
18	16	RESD,0603,49.9OHM,1%,1/16W	Must be 1%
19	4	RESD,0603,100K,5.00%,1/16W	SMBus pullups
20	4	RESD,0603,1000.0OHM,5%,1/16W	
21	1	RESD,0603,1400.0OHM,.1.0%,1/16W	Must be 1%
22	3	RESD,0603,1400.0OHM,1%,1/16W	Must be 1%
23	1	Xtal, HC49S, 25MHz, 20pF, 30ppm	30 ppm crystal
	98	Part total	

8.2 82571EB Copper-Based Reference Design Bill of Material (Discrete Magnetics)

DNP = Do Not Populate

Item	Qty	Part Description	Comments
1	4	CAPC,C0G0805,50V,1000PF,5%	
2	2	CAPC,NPO0603,50V,27PF,5%	
3	3	CAPC,X5R,1206,10.000 UF,6.300V, 20%	
4	4	CAPC,X5R,1206,10.000 UF,6.300V, 20%	
5	8	CAPC,X7R,0402,330.000 PF,25.000V, 5%	
6	8	CAPC,X7R,0603,0.010UF,50V,20%	
7	2	CAPC,X7R,1808,2KV,1500PF	
8	9	CAPC,Y5V,0603,0.100 UF,25.000V,20%	
9	1	CAPC,Y5V,0603,0.100 UF,25.000V,20%	
10	17	CAPC,Y5V,0603,25V,.1UF	
11	8	CAPC,Y5V,0603,25V,.1UF	
12	1	CONN,HDR,1X2,PLG,VT,0.1,093ST,KP	IEEE_TEST - Populate only for testing
13	1	CONN,HDR,1X2,PLG,VT,0.1,093ST,KP	IEEE_TEST - Populate only for testing
14	2	CONN,RJ45 w/LEDs,THMT,JI5101-S001	RJ-45 connector with LED's
15	1	IC,CS,82571EB,C	82571EB LAN Controller
16	1	IC,EEPROM,BL,SOIC,2.1MHZ,1024X8	EEPROM
17	1	IC,FLASH,AT25F1024N-1,8,SOIC,NA	FLASH
18	1	RES D,0603,0.00 OHM,5.00%,1/16W	
19	8	RES,D,0603,0.000 OHM,5%,1/16W	
20	8	RESA,1206,75.0OHM,5%,1/4W	
21	7	RESD,0603,3.3K,5.00%,1/16W	
22	8	RESD,0603,10K,5.00%,1/16W	9 if not using aux power
23	16	RESD,0603,49.9OHM,1%,1/16W	Must be 1%
24	4	RESD,0603,100K,5.00%,1/16W	SMBus pull-ups
25	4	RESD,0603,330.0OHM,5%,1/16W	
26	4	RESD,0603,1000.0OHM,5%,1/16W	
27	1	RESD,0603,1400.0OHM,.1.0%,1/16W	Must be 1%
28	3	RESD,0603,1400.0OHM,1%,1/16W	Must be 1%
29	2	XFMR LAN,1000 BASE T,SMT,24 PINS,SINGLE	Discrete Magnetics Mdule
30	1	Xtal, HC49S, 25MHz, 20pF, 30ppm	30 ppm crystal
	140	Parts Total	



8.3 82571EB Copper-Based Reference Design (w/Dual Stacked Integrated Magnetics Module) Bill of Material (represents two ports populated the same)

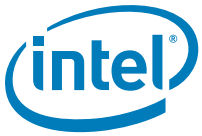
DNP = Do Not Populate

Item	Qty	Part Description	Comments
1	4	CAPC,C0G,0603,470.000 PF,50.000V, 5%	
2	2	CAPC,NPO0603,50V,27PF,5%	
3	3	CAPC,X5R,1206,10.000 UF,6.300V, 20%	
4	9	CAPC,Y5V,0603,0.100 UF,25.000V,?20%>	
5	16	CAPC,Y5V,0603,0.100 UF,25.000V,?20%>	
6	1	CAPC,Y5V,0603,0.100 UF,25.000V,?20%>	
7	17	CAPC,Y5V,0603,25V,.1UF	
8	1	CONN, Dual Stack Intergrated Magnetics Module	Dual Stacked IMM /with LEDS
9	1	CONN,HDR,1X2,PLG,VT,0.1,093ST,KP	IEEE_TEST - Populate only for testing
10	1	CONN,HDR,1X2,PLG,VT,0.1,093ST,KP	IEEE_TEST - Populate only for testing
11	1	IC,CS,82571EB,C	82571EB LAN Controller
12	1	IC,EEPROM,BL,SOIC,2.1MHZ,1024X8	EEPROM
13	1	IC,FLASH,AT25F1024N-1,8,SOIC,NA	FLASH
14	1	RES D,0603,0.00 OHM,5.00%,1/16W	
15	7	RESD,0603,3.3K,5.00%,1/16W	
16	8	RESD,0603,10K,5.00%,1/16W	9 if not using aux power
17	16	RESD,0603,49.9OHM,1%,1/16W	Must be 1%
18	4	RESD,0603,100K,5.00%,1/16W	SMBus pull-ups
19	4	RESD,0603,330.0OHM,5%,1/16W	
20	4	RESD,0603,1000.0OHM,5%,1/16W	
21	1	RESD,0603,1400.0OHM,.1.0%,1/16W	Must be 1%
22	3	RESD,0603,1400.0OHM,1%,1/16W	Must be 1%
23	1	Xtal, HC49S, 25MHz, 20pF, 30ppm	30ppm crystal
	107	Part total	

8.4 82571EB Optical SerDes-Based Reference Design Bill of Material

DNP = Do Not Populate

Item	Qty	Part Description	Comments
1	4	CAPC,C0G,0603,470.000 PF,50.000V, 5%	
2	2	CAPC,NPO0603,50V,27PF,5%	
3	3	CAPC,X5R,1206,10.000 UF,6.300V, 20%	
4	4	CAPC,X7R,0603,0.100UF,16V,10%	
5	27	CAPC,Y5V,0603,25V,.1UF	
6	1	CONN,HDR,1X2,PLG,VT,0.1,093ST,KP	IEEE_TEST - Populate only for testing
7	1	CONN,HDR,1X2,PLG,VT,0.1,093ST,KP	IEEE_TEST - Populate only for testing
8	4	FER-BEAD,0603,600.0 OHM,0.2 A,25%	
9	1	IC,CS,82571EB,C	82571EB LAN Controller
10	1	IC,EEPROM,AT25128, SOIC,2.100 MHZ,1024X8	EEPROM
11	1	IC,FLASH,AT25F1024N-1,8,SOIC,NA	FLASH
12	2	IC,VLSI,OTHER,V23818-K,THM,10	OPTICAL LASERS
13	1	RES,D,0603,0.000 OHM,5%,1/16W	
14	2	RESA,1206,100000.0OHM,5%,1/4W	
15	7	RESD,0603,3.3K,5.00%,1/16W	
16	8	RESD,0603,10K,5.00%,1/16W	9 if not using Aux power
17	4	RESD,0603,100K,5.00%,1/16W	SMBus pull-ups
18	4	RESD,0603,1000.0OHM,5%,1/16W	
19	1	RESD,0603,1400.0OHM,.1.0%,1/16W	Must be 1%
20	3	RESD,0603,1400.0OHM,1%,1/16W	Must be 1%
21	1	Xtal, HC49S, 25MHz, 20pF, 30ppm	30ppm crystal
	82	Part Total	



8.5 82571EB Backplane SerDes-Based Reference Design Bill of Material

This BOM only includes the SERDES caps and a Generaic Backplane Connector

DNP = Do Not Populate

Item	Qty	Part Description	Comments
1	2	CAPC,NPO0603,50V,27PF,5%	
2	3	CAPC,X5R,1206,10.000 UF,6.300V, 20%	
3	4	CAPC,X7R,0402,0.010 UF,25.000V, 10%	
4	27	CAPC,Y5V,0603,25V,.1UF	
5	1	CONN,HDR,1X2,PLG,VT,0.1,093ST,KP	IEEE_TEST - Populate only for testing
6	1	CONN,HDR,1X2,PLG,VT,0.1,093ST,KP	IEEE_TEST - Populate only for testing
7	1	Connector, Backplane	
8	1	IC,CS,82571EB,C	82571EB LAN Controller
9	1	IC,EEPROM,AT25128, SOIC,2.100 MHZ,1024X8	EEPROM
10	1	IC,FLASH,AT25F1024N-1,8,SOIC,NA	FLASH
11	1	RES,D,0603,0.000 OHM,5%,1/16W	
12	7	RESD,0603,3.3K,5.00%,1/16W	
13	8	RESD,0603,10K,5.00%,1/16W	9 if not using aux power
14	4	RESD,0603,100K,5.00%,1/16W	SMBus pull-ups
15	4	RESD,0603,1000.0OHM,5%,1/16W	
16	1	RESD,0603,1400.0OHM,.1.0%,1/16W	Must be 1%
17	3	RESD,0603,1400.0OHM,1%,1/16W	Must be 1%
18	1	Xtal, HC49S, 25MHz, 20pF, 30ppm	30ppm crystal
	71	Part Total	

8.6 82572EI Copper-based Reference Design Bill of Material (w/ Integrated Magnetics Module)

DNP = Do Not Populate

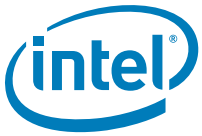
Item	Qty	Part Description	Comments
1	2	CAPC,C0G,0603,470.000 PF,50.000V, 5%	
2	2	CAPC,NPO0603,50V,27PF,5%	
3	3	CAPC,X5R,1206,10.000 UF,6.300V, 20%	
4	5	CAPC,Y5V,0603,0.100 UF,25.000V,20%>	
5	1	CAPC,Y5V,0603,0.100 UF,25.000V,20%>	
6	26	CAPC,Y5V,0603,25V,.1UF	
7	1	CONN, INTEGRATED MAGNETICS MODULE	Integrated Magnetics Module
8	1	CONN,HDR,1X2,PLG,VT,0.1,093ST,KP	IEEE_TEST - Populate only for testing
9	1	IC,CS,82572EI,C	82572EI LAN Controller
10	1	IC,EEPROM,BL,SOIC,2.1MHZ,1024X8	EEPROM
11	1	IC,FLASH,AT25F1024N-1,8,SOIC,NA	FLASH
12	1	RES D,0603,0.00 OHM,5.00%,1/16W	
13	7	RESD,0603,3.3K,5.00%,1/16W	
14	8	RESD,0603,10K,5.00%,1/16W	9 if not using aux power
15	8	RESD,0603,49.900OHM,1.00%,1/16W	Must be 1%
16	2	RESD,0603,100K,5.00%,1/16W	SMBus pull-ups
17	4	RESD,0603,1000.0OHM,5%,1/16W	
18	1	RESD,0603,1400.0OHM,.1.0%,1/16W	Must be 1%
19	2	RESD,0603,1400.0OHM,1%,1/16W	Must be 1%
20	1	Xtal, HC49S, 25MHz, 20pF, 30ppm	30 ppm crystal
	78	Part Total	

8.7 82572EI Copper-based Reference Design Bill of Material (w/Discrete Magnetics)

DNP = Do Not Populate

Item	Qty	Part Description	Comments
1	2	CAPC,C0G0805,50V,1000PF,5%	
2	2	CAPC,NPO0603,50V,27PF,5%	
3	3	CAPC,X5R,1206,10.000 UF,6.300V, 20%	
4	2	CAPC,X5R,1206,10.000 UF,6.300V, 20%	
5	4	CAPC,X7R,0402,330.000 PF,25.000V, 5%>	
6	4	CAPC,X7R,0603,0.010UF,50V,20%	
7	1	CAPC,X7R,1808,2KV,1500PF	
8	1	CAPC,Y5V,0603,0.100 UF,25.000V,?20%>	
9	26	CAPC,Y5V,0603,25V,.1UF	
10	4	CAPC,Y5V,0603,25V,.1UF	
11	1	CONN,HDR,1X2,PLG,VT,0.1,093ST,KP	IEEE_TEST - Populate only for testing
12	1	CONN,RJ45 w/LEDs,THMT,JI5101-S001	RJ45 Connector
13	1	IC,CS,82572EI,C	82572EI LAN Controller
14	1	IC,EEPROM,BL,SOIC,2.1MHZ,1024X8	EEPROM
15	1	IC,FLASH,AT25F1024N-1,8,SOIC,NA	FLASH
16	1	RES D,0603,0.00 OHM,5.00%,1/16W	
17	4	RES,D,0603,0.000 OHM,5%,1/16W	
18	4	RESA,1206,75.0OHM,5%,1/4W	
19	7	RESD,0603,3.3K,5.00%,1/16W	
20	8	RESD,0603,10K,5.00%,1/16W	9 if not using aux power
21	8	RESD,0603,49.9OHM,1%,1/16W	Must be 1%
22	2	RESD,0603,100K,5.00%,1/16W	SMBus pullup
23	2	RESD,0603,330.0OHM,5%,1/16W	
24	4	RESD,0603,1000.0OHM,5%,1/16W	
25	1	RESD,0603,1400.0OHM,.1.0%,1/16W	Must be 1%
26	2	RESD,0603,1400.0OHM,1%,1/16W	Must be 1%
27	1	XFMR LAN,1000 BASE T,SMT,24 PINS,SINGLE	Discrete Magnetics Module
28	1	Xtal, HC49S, 25MHz, 20pF, 30ppm	30ppm crystal
	99	Part Total	

NOTE: TVS Diodes for CDE suppresion are not included in this BOM



8.8 82572EI Optical SerDes-based Reference Design Bill of Material

DNP = Do Not Populate

Item	Qty	Part Description	Comments
1	2	CAPC,C0G,0603,470.000 PF,50.000V, 5%	
2	2	CAPC,NPO0603,50V,27PF,5%	
3	3	CAPC,X5R,1206,10.000 UF,6.300V, 20%	
4	2	CAPC,X7R,0603,0.100UF,16V,10%	
5	27	CAPC,Y5V,0603,25V,.1UF	
6	1	CONN,HDR,1X2,PLG,VT,0.1,093ST,KP	IEEE_TEST - Populate only for testing
7	1	CONN,HDR,1X2,PLG,VT,0.1,093ST,KP	IEEE_TEST - Populate only for testing
8	2	FER-BEAD,0603,600.0 OHM,0.2 A,25%	
9	1	IC,CS,82572EI,C	82572EI LAN Controller
10	1	IC,EEPROM,AT25128, SOIC,2.100 MHZ,1024X8	EEPROM
11	1	IC,FLASH,AT25F1024N-1,8,SOIC,NA	FLASH
12	1	IC,VLSI,OTHER,V23818-K,THM,10	OPTICAL LASERS
13	1	RES,D,0603,0.000 OHM,5%,1/16W	
14	2	RESA,1206,100000.0OHM,5%,1/4W	
15	7	RESD,0603,3.3K,5.00%,1/16W	
16	8	RESD,0603,10K,5.00%,1/16W	9 if not using aux power
17	2	RESD,0603,100K,5.00%,1/16W	SMBus pull-ups
18	4	RESD,0603,1000.0OHM,5%,1/16W	
19	1	RESD,0603,1400.0OHM,.1.0%,1/16W	Must be 1%
20	3	RESD,0603,1400.0OHM,1%,1/16W	Must be 1%
21	1	Xtal, HC49S, 25MHz, 20pF, 30ppm	30ppm crystal
	73	Part Total	

8.9 82572EI Backplane SerDes-based Reference Design Bill of Material

This BOM only includes the SERDES caps and a Generaic Backplane Connector

DNP = Do Not Populate

Item	Qty	Part Description	Comments
1	2	CAPC,NPO0603,50V,27PF,5%	
2	3	CAPC,X5R,1206,10.000 UF,6.300V, 20%	
3	2	CAPC,X7R,0402,0.010 UF,25.000V, 10%	
4	27	CAPC,Y5V,0603,25V,.1UF	
5	1	CONN,HDR,1X2,PLG,VT,0.1,093ST,KP	IEEE_TEST - Populate only for testing
6	1	CONN,HDR,1X2,PLG,VT,0.1,093ST,KP	IEEE_TEST - Populate only for testing
7	1	Connector, Backplane	
8	1	IC,CS,82572EI,C	82572EI LAN Controller
9	1	IC,EEPROM,AT25128, SOIC,2.100 MHZ,1024X8	EEPROM
10	1	IC,FLASH,AT25F1024N-1,8,SOIC,NA	FLASH
11	1	RES,D,0603,0.000 OHM,5%,1/16W	
12	7	RESD,0603,3.3K,5.00%,1/16W	
13	8	RESD,0603,10K,5.00%,1/16W	9 if not using aux power
14	2	RESD,0603,100K,5.00%,1/16W	SMBus pull-ups
15	4	RESD,0603,1000.0OHM,5%,1/16W	
16	1	RESD,0603,1400.0OHM,.1.0%,1/16W	Must be 1%
17	3	RESD,0603,1400.0OHM,1%,1/16W	Must be 1%
18	1	Xtal, HC49S, 25MHz, 20pF, 30ppm	30ppm crystal
	67	Part Total	

9.0 Design and Layout Checklists

These checklists are provided for use during the design phase to ensure that important items are considered for the design.

9.1 Design Checklists

Table 7. 82571EB Schematic Checklist

SECTION	CHECK ITEMS	REMARKS	DONE	COMMENTS
General	Have up-to-date product documentation and specification updates	Documents are subject to frequent change		
	Observe instructions for special pins needing pull-up or pull-down resistors.	Do not connect pull-up or pull-down resistors to any pins marked No Connect.		
82571EB Controller	Connect PCI Express interface pins to corresponding pins on MCH.			
	Connect balls J2 PE_CLKn and K2 PE_CLKp to 100MHz PCI Express system clock.			
	Connect a 1.4K 1% resistor across Balls G2 PE_RCOMPn and H2 PE_RCOMPp.			
	Connect a 1.4K 1% resistor across balls D14 (RBIAS0n) and E14 (RBIAS0p) and Balls M14 (RBIAS1n/ RSVD_M14) and N14 (RBIAS1p/RSVD_N14).			
	Connect a 1.4K 1% resistor across Balls H14 SRDS_RCOMPn and H15 SRDS_RCOMPp			
	Do not connect anything to Ball R4 LAN_PWR_GOOD.	The device generates its own internal PWR_GOOD signal.		
	Connect Ball P11 (PE_WAKE_N) to ICH for wake up signaling.	Device must be powered by 3V aux to enable wake events		
	Connect Ball C8 AUX_PWR signals correctly.	AUX_PWR is a logic input denoting that auxiliary power is connected to the device. AUX_PWR=1 is a requirement for wakeup		

Table 7. 82571EB Schematic Checklist

SECTION	CHECK ITEMS	REMARKS	DONE	COMMENTS
	Connect Ball T6 PE_RST_N to the ICH in the same way that PCI_RST# would be connected in a PCI-based system.	This pin functions the same as an in-band PCI Express reset and will latch changes in LAN0_DIS_N, LAN1_DIS_N.		
	If a LAN disable function is required, drive Ball B7 LAN0_DIS_N, Ball B8 LAN1_DIS_N.	Use a pin that can be written by BIOS. The state of the pin should be "sticky" upon assertion of EXP_RST# (PCI_RST#)		
	Use an SPI* serial EEPROM	Use a 3.3K pull-up resistor on write protect (WP#) and a 3.3K pull-up resistor on HOLD#. EEPROMs should be rated for at least 2 MHz		
	Check reference schematic for connection of Software Defined Pins	Intel driver software may expect to use Software Defined Pins for special functions.		
	Connect Ball R5 TEST_EN to ground, using a 1K pull-down resistor.			
	Connect Balls A6, A7, B5, C3, C5, C7 to 3.3V using a 10K pull-up resistor.	These connections ensure proper device operation.		
	Connect a two-pin header to each IEEE_TEST balls for IEEE phy conformance testing. For productionapplications, all testpoints may be deleted. For production applications, leave all IEEE_TEST unconnected.			
	Balls A3, B3, H1, J1, J14, J15, R4 and T7 should not be connected to anything.			
Clock Source	Use 25MHz 30 ppm accuracy @ 25°C clock source. Avoid components that introduce jitter.	Parallel resonant crystals are preferred. Use oscillator if testability rules require turning off the clock. If using an oscillator, consider a series termination resistor of 22-33 Ω. Avoid PLL clock buffers.		

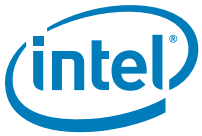


Table 7. 82571EB Schematic Checklist

SECTION	CHECK ITEMS	REMARKS	DONE	COMMENTS
	Connect two 27 pF (5% tolerance) load caps to crystal.	Capacitance affects accuracy of the frequency. Must be matched to crystal specs, including estimated trace capacitance in calculation. Consult design guide for more information.		
	Be sure to follow layout guidance given in section 7.1.3.	Ensure that a 30 Ω, 5%, 0402 resistor is in series on Xtal2. All recommendations in section 7.1.3 should be followed. Not doing so can lead to the crystal failing to start up.		
EEPROM & FLASH	Use decoupling capacitor.	Applies to EEPROM or FLASH devices.		
	Consider whether to use FLASH memory	Most LOM systems with boot ROM place the image in the system FLASH.		
	If FLASH memory is used, select the appropriate device.	The 82571EB controller uses serial FLASH.		
SMBus	If SMBus0 is not used, connect pull-up resistors to SMBCLK0/ FLBMCK, SMBD0/ FLBMD, and SMBALRT_N/ PCI_PWR_GOOD.	100 kΩ pull-ups are reasonable values. If 4.7K pullups are already on these signals then these resistors are not needed.		
	If SMBus is used, system should have pull-up resistors.	SMBus signals are open-drain.		
	For ASF applications with SMBus port A, connect Ball R11 SMBALRT_N/ PCI_PWR_GOOD to the system PWR_GOOD signal or to Vcc through a 3.3K pull-up resistor.	Use 3.3V, not 3.3V AUX. Alternatively, Ball R11 can be configured as an SMBALRT_N output.		
	If SMBus0 is configured as a Fast Link Bus (FML), connect SMBCLK0/FLBMCK, SMBD0/FLBMD, FLBSD and FLBINTEX to the system.			
	P12 (SMBD1) & P13 (SMBCLK1) are reserved. DO NOT USE THESE PINS. Connect both of them to 3.3 V through a 100 kΩ resistor.			

Table 7. 82571EB Schematic Checklist

SECTION	CHECK ITEMS	REMARKS	DONE	COMMENTS
Transmit and Receive Differential Pairs	For 10/100/1000 Base-T applications, the 82571EB controller uses pairs of 49.9 Ω termination resistors with 0.1µF capacitors attached between center nodes and ground.	Apply to all four differential pairs of each port. Place components close to LAN Controller.		
	For 1000Base-SX applications (or SerDes backplanes), the differential pairs are internally terminated. Connect the differential signals to another SerDes or optical transceiver through AC coupling capacitors. Caps should be 0.01uF.	Optical transceiver may contain integrated AC coupling caps.		
Magnetics Module (10/100/1000 Base-T applications)	Integrated magnetics modules/RJ-45 connectors are available to minimize space requirements.	Multivendor pin compatibility is possible. Contact manufacturers.		
	Qualify magnetics module carefully for Return Loss, Insertion Loss, Open Circuit Inductance, Common Mode Rejection, and Crosstalk Isolation	Magnetics module is critical to passing IEEE PHY conformance tests and EMI test.		
	Supply 1.8V to the transformer center taps and use 0.1µF bypass capacitors.	1.8V biases the controller's output buffers. Magnetics with four center tap pins may have better characteristics than those with 1-2 center tap pins. Use capacitors with low Equivalent Series Resistance. Place capacitors close to center tap pins.		
Discrete Magnetics Module/RJ-45 Connector Option (10/100/1000 Base-T applications)	Bob Smith termination: use 4 x 75 Ω resistors for cable-side center taps and unused pins.	Terminates pair-to-pair common mode impedance of the CAT5 cable.		
	Bob Smith termination: use an EFT capacitor. Suggested values are 1500pF/2KV or 1000pF/3KV	Maintain greater than 25 mil spacing from capacitor to traces and components.		
	Connect signal pairs correctly to RJ-45 connector.			

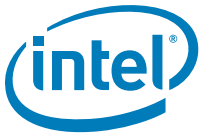


Table 7. 82571EB Schematic Checklist

SECTION	CHECK ITEMS	REMARKS	DONE	COMMENTS
Power Supply and Signal Ground	Provide a 3.3V supply. Use auxiliary power supplies.	Auxiliary power is necessary to support wake up from powerdown states.		
	Design with power supplies that start up properly. Power sequnece is: 3.3V , then 1.8V and 1.1V	A good guideline is that all voltages should ramp to within their control bands in 20 ms. or less. It is desirable that that voltages ramp in sequence and that the voltage rise be monotonic.		
	Use decoupling and bulk capacitors generously.	Use approximately 12 bypass capacitors for the Ethernet silicon (0.1uf). Add approximately 10-20µF of bulk capacitance per voltage rail, typically using 10µF capacitors. If power is distributed on traces, bulk capacitors should be used at both ends. If power is distributed on cards, bulk capacitors should be used at the connector.		
Chassis Ground (10/100/1000 Base-T applications)	If possible, provide a separate chassis ground to connect the shroud of the RJ-45 connector and to terminate the line side of the magnetics module.	This design improves EMI behavior.		
	Place pads for approximately 4-6 "stitching" capacitors to bridge the gap from chassis ground to signal ground.	Typical values range from 0.1µF to 4.7µF. Determine experimentally.		
LED Circuits	Basic recommendation is a single green LED for Activity and a dual (bi-color) LED for Speed. Each port should have its own dedicated LED's. Many other configurations are possible.	Two LED configuration is compatible with integrated magnetics modules. For the Link/Activity LED, connect the anode to the LED1/ACT# pin and the cathode to the LED0/LINK_UP# pin. For the bi-color speed LED pair, have the LED2/LINK100# signal drive one end. The other end should be connected to LED3/LINK1000#		

Table 7. 82571EB Schematic Checklist

SECTION	CHECK ITEMS	REMARKS	DONE	COMMENTS
	Connect LEDs to 3.3V as indicated in reference schematics.	Use 3.3V AUX for designs supporting wakeup. Consider adding 1-2 filtering capacitors per LED for extremely noisy situations. Suggested starting value 470pF.		
	Add current limiting resistors to LED paths.	Typical current limiting resistors are 300-330 ohms when using a 3.3V supply. Current limiting resistors are typically included with integrated magnetics modules.		
Mfg Test	82571EB controller uses a JTAG Test Access Port.	Place a 1K pull-down resistor on Ball P4 JTCK. Place a 3.3 K ohm pull-up resistor on JTDO.		

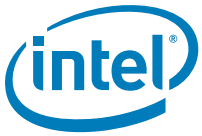


Table 8. 82572EI Schematic Checklist

SECTION	CHECK ITEMS	REMARKS	DONE	COMMENTS
General	Have up-to-date product documentation and specification updates	Documents are subject to frequent change		
	Observe instructions for special pins needing pull-up or pull-down resistors.	Do not connect pull-up or pull-down resistors to any pins marked No Connect.		
82572EI Controller	Connect PCI Express interface pins to corresponding pins on MCH.			
	Connect balls J2 PE_CLKn and K2 PE_CLKp to 100MHz PCI Express system clock.			
	Connect a 1.4K 1% resistor across Balls G2 PE_RCOMPn and H2 PE_RCOMPp.			
	Connect a 1.4K 1% resistor across balls D14 (RBIAS0n) and E14 (RBIAS0p).			
	Connect a 1.4K 1% resistor across Balls H14 SER_RCMPn and H15 SER_RCMPp			
	Do not connect anything to Ball R4 LAN_PWR_GOOD .	The device generates its own internal PWR_GOOD signal.		
	Connect Ball P11 WAKE# to ICH for wake up signaling.	Device must be powered by 3V aux to enable wake events		
	Connect Ball C8 AUX_PWR signals correctly.	AUX_PWR is a logic input denoting that auxiliary power is connected to the device. AUX_PWR=1 is a requirement for wakeup		
	Connect Ball T6 PE_PWR_GOOD to the ICH in the same way that PCI_RST# would be connected in a PCI-based system.	On the 82572EI controller, this pin functions the same as an in-band PCI Express reset and will latch changes in LAN0_DIS_N, LAN1_DIS_N and DEVICE_DIS_N.		
	If a LAN disable function is required, drive Ball B7 LAN0_DIS_N, Ball B8 LAN1_DIS_N or Ball A7 DEVICE_DIS_N	Use a pin that can be written by BIOS. The state of the pin should be "sticky" upon assertion of EXP_RST# (PCI_RST#)		

Table 8. 82572EI Schematic Checklist

SECTION	CHECK ITEMS	REMARKS	DONE	COMMENTS
	Use an SPI* serial EEPROM	Use a 3.3K pull-up resistor on write protect (WP#) and a 3.3K pull-up resistor on HOLD#. EEPROMs should be rated for at least 2 MHz		
	Check reference schematic for connection of Software Defined Pins	Intel driver software may expect to use Software Defined Pins for special functions.		
	Connect Balls A6, A7, B5, C3, C5, C7 to 3.3V using a 10K pull-up resistor.	These connections ensure proper device operation.		
	Connect a two-pin header to each IEEE_TEST balls for IEEE phy conformance testing. For productionapplications, all testpoints may be deleted. For production applications, leave all IEEE_TEST unconnected.			
	Balls A3, B3, H1, J1, J14, J15, R4 and T7 should not be connected to anything.			
	Connect Ball R5 TEST_EN to ground, using a 1K pull-down resistor.	Connect a two-pin header to each ATEST for IEEE phy conformance testing. For production applications, all test points may be deleted. For production applications, leave TEST unconnected.		
Clock Source	Use 25MHz 30 ppm accuracy @ 25 °C clock source. Avoid components that introduce jitter.	Parallel resonant crystals are preferred. Use oscillator if testability rules require turning off the clock. If using an oscillator, consider a series termination resistor of 22-33 Ω. Avoid PLL clock buffers.		
	Connect two 27pF (5% tolerance) load caps to crystal.	Capacitance affects accuracy of the frequency. Must be matched to crystal specs, including estimated trace capacitance in calculation. Consult design guide for more information.		

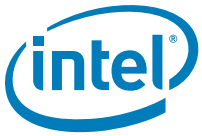


Table 8. 82572EI Schematic Checklist

SECTION	CHECK ITEMS	REMARKS	DONE	COMMENTS
	Be sure to follow layout guidance given in sec. 7.1.3.	Ensure that a 30 Ω, 5%, 0402 resistor is in series with Xtal2. Not following the layout guidance can cause the crystal to not start up.		
EEPROM & FLASH	Use decoupling capacitor.	Applies to EEPROM or FLASH devices.		
	Consider whether to use FLASH memory	Most LOM systems with boot ROM place the image in the system FLASH.		
	If FLASH memory is used, select the appropriate device.	The 82572EI controller uses serial FLASH.		
SMBus	If SMBus0 is not used, connect pull-up resistors to SMBCLK0/ FLBMCK, SMBD0/ FLBMD and SMBALRT_N.	100 kΩ pull-ups are reasonable values. If 4.7 kΩ pullups are already on these signals, then these resistors are not needed.		
	If either SMBus is used, system should have pull-up resistors.	SMBus signals are open-drain.		
	For ASF applications with SMBus port A, connect Ball R11 SMBALRT_N/ PCI_PWR_GOOD to the system PWR_GOOD signal or to Vcc through a 3.3 kΩ pull-up resistor.	Use 3.3 V, not 3.3 V AUX. Alternatively, Ball R11 can be configured as an SMBALRT_N output.		
	If SMBus port A is configured as a Fast Link Bus, connect SMBCLK0/FLBMCK, SMBD0/FLBMD, FLBSD and FLBINTEX to the system.			
	P12 (SMBD1) & P13 (SMBCLK1) are reserved. DO NOT USE THESE PINS. Connect both of them to 3.3 V through a 100 kΩ resistor.			
Transmit and Receive Differential Pairs	For 10/100/1000 Base-T applications, the 82572EI controller uses pairs of 49.9 Ω termination resistors with 0.1 µF capacitors attached between center nodes and ground.	Apply to all the differential pairs of each port. Place components close to LAN Controller.		

Table 8. 82572EI Schematic Checklist

SECTION	CHECK ITEMS	REMARKS	DONE	COMMENTS
	For 1000Base-SX applications (or SerDes backplanes), the differential pairs are internally terminated. Connect the differential signals to another SerDes or optical transceiver through AC coupling capacitors. Caps should be 0.01 uF.	Optical transceiver may contain integrated AC coupling caps.		
Magnetics Module (10/100/1000 Base-T applications)	Integrated magnetics modules/RJ-45 connectors are available to minimize space requirements.	Multivendor pin compatibility is possible. Contact manufacturers.		
	Qualify magnetics module carefully for Return Loss, Insertion Loss, Open Circuit Inductance, Common Mode Rejection, and Crosstalk Isolation	Magnetics module is critical to passing IEEE PHY conformance tests and EMI test.		
	Supply 1.8 V to the transformer center taps and use 0.1 µF bypass capacitors.	1.8 V biases the controller's output buffers. Magnetics with four center tap pins may have better characteristics than those with 1-2 center tap pins. Use capacitors with low Equivalent Series Resistance. Place capacitors close to center tap pins.		
Discrete Magnetics Module/RJ-45 Connector Option (10/100/1000 Base-T applications)	Bob Smith termination: use 4 x 75 Ω resistors for cable-side center taps and unused pins.	Terminates pair-to-pair common mode impedance of the CAT5 cable.		
	Bob Smith termination: use an EFT capacitor. Suggested values are 1500 pF/2 kV or 1000 pF/3 kV	Maintain greater than 25 mil spacing from capacitor to traces and components.		
	Connect signal pairs correctly to RJ-45 connector.			
Power Supply and Signal Ground	Provide a 3.3 V supply. Use auxiliary power supplies.	Auxiliary power is necessary to support wake up from powerdown states.		

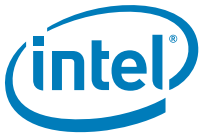
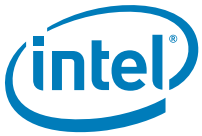


Table 8. 82572EI Schematic Checklist

SECTION	CHECK ITEMS	REMARKS	DONE	COMMENTS
	Design with power supplies that start up properly. Power sequnece is: 3.3 V , then 1.8 V and 1.1 V	A good guideline is that all voltages should ramp to within their control bands in 20 ms. or less. It is desirable that that voltages ramp in sequence and that the voltage rise be monotonic.		
	Use decoupling and bulk capacitors generously.	Use approximately 12 bypass capacitors for the Ethernet silicon (0.1 uf). Add approximately 10-20 µF of bulk capacitance per voltage rail, typically using 10 µF capacitors. If power is distributed on traces, bulk capacitors should be used at both ends. If power is distributed on cards, bulk capacitors should be used at the connector.		
Chassis Ground (10/100/1000 Base-T applications)	If possible, provide a separate chassis ground to connect the shroud of the RJ-45 connector and to terminate the line side of the magnetics module.	This design improves EMI behavior.		
	Place pads for approximately 4-6 "stitching" capacitors to bridge the gap from chassis ground to signal ground.	Typical values range from 0.1µF to 4.7µF. Determine experimentally.		
LED Circuits	Basic recommendation is a single green LED for Activity and a dual (bi-color) LED for Speed.	Two-LED configuration is compatible with integrated magnetics modules. For the Link/Activity LED, connect the anode to the LED1/ACT# pin and the cathode to the LED0/LINK_UP# pin. For the bi-color speed LED pair, have the LED2/LINK100# signal drive one end. The other end should be connected to LED3/LINK1000#		

Table 8. 82572EI Schematic Checklist

SECTION	CHECK ITEMS	REMARKS	DONE	COMMENTS
	Connect LEDs to 3.3 V as indicated in reference schematics.	Use 3.3 V AUX for designs supporting wakeup. Consider adding one or two filtering capacitors per LED for extremely noisy situations. Suggested starting value 470 pF.		
	Add current limiting resistors to LED paths.	Typical current limiting resistors are 300-330 ohms when using a 3.3V supply. Current limiting resistors are typically included with integrated magnetics modules.		
Mfg Test	82572EI controller uses a JTAG Test Access Port.	Place a 1K pull-down resistor on Ball P4 JTAG_TCK.		



9.2 Layout Checklists

Table 9. 82571EB Layout Checklist

SECTION	CHECK ITEMS	REMARKS	DONE	COMMENTS
General	Have up-to-date product documentation and specification updates	Documents are subject to frequent change		
	Route the transmit and receive differential traces before routing the digital traces.	Layout of differential traces is critical.		
Ethernet Device	Place the Ethernet silicon at least 1 inch from the edge of the board and at least 1 inch from any integrated magnetics module.	With closer spacing, fields can follow the surface of the magnetics module or wrap past edge of board. EMI may increase. Optimum location is approximately 1 inch behind the magnetics module.		
	For the 82571EB controller, the trace impedance for the PCI Express differential pairs is 100 Ω +/- 15%	Match trace lengths between pairs to within 3 inches. Match trace lengths in each pair to within 5 mils.		
	For the 82571EB controller, place the PCI Express termination components carefully.	Connect the high-speed serial compensation resistor no more than 1" from the PE_RCMPp / PE_RCMPn balls. For 10/100/1000BASE-T applications, connect the MDI bias resistor no farther than 1" from the RBIAS0p / RBIAS0n and RBIAS1p / RBIAS1n balls. For 1000BASE-SX applications, connect the SerDes impedance compensation resistor no farther than 1" from the SER_RCMPp / SER_RCMPn balls.		
Clock Source	Place crystal and load capacitors within 0.75 inches from Ethernet device.	The Ethernet clock plays a key role in EMI.		
	Keep clock lines away from other digital traces, I/O ports, board edge, transformers and differential pairs			

Table 9. 82571EB Layout Checklist

SECTION	CHECK ITEMS	REMARKS	DONE	COMMENTS
	Follow crystal layout guidance in section 7.1.3	• 30 Ω (5%) 0402 resistor in series on Xtal2 • Device (ethernet controler), crystal, and load caps all on the same side of the board • Maximum of two (2) vias for load caps to ground • Maximum of 90 mils between load caps and crystal pads		
EEPROM and FLASH Memory	Placement is not critical due to slow signal speeds.	EEPROM and FLASH may be placed a few inches away from Ethernet controller to provide better spacing of critical components.		
Transmit and Receive Differential Pairs (10/100/1000 Base-T applications)	Design traces for 100 Ω differential impedance (± 15%)	Primary requirement for 10/100/1000 Mb/s Ethernet. Paired 50 Ω traces do not make 100 Ω differential. Check impedance calculator.		
	Use short traces.	Keep trace length under 4 inches from the Ethernet controller through the magnetics to the RJ-45 connector.		
	Avoid highly resistive traces, for example, 4 mil traces longer than 4 inches.	If trace length is a problem, use thicker board dielectrics to allow wider traces. Thicker copper is even better than wider traces.		
	Make traces symmetrical	Try to match the pairs at pads, vias and turns. Establish rules carefully for the autorouter. Asymmetry contributes to impedance mismatch.		
	Do not make 90° bends.	Bevel corners with turns based on 45° angles		
	Avoid through holes (vias).	If using through holes (vias), the budget is two per trace.		
	Keep traces close together within differential pairs.	Keep within 30 mils regardless of trace geometry.		

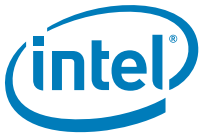


Table 9. 82571EB Layout Checklist

SECTION	CHECK ITEMS	REMARKS	DONE	COMMENTS
	Keep trace-to-trace length difference within each pair to less than 50 mils.	Minimizes signal skew and common mode noise. Improves long cable performance.		
	Pair-to-pair differences in length are not critical.	A 25% difference in length from longest pair to shortest pair is typical.		
	Try to keep differential pairs 100 mils or more away from each other and away from parallel digital traces.	Minimizes crosstalk and noise injection. Pairs may be spaced as close as 50 mils as long as crosstalk isolation is 34dB or more. Tighter spacing is allowed closer to connections. Guard traces are generally not recommended and will reduce the impedance if done incorrectly.		
	Keep traces away from the board edge.	Controls EMI.		
	Avoid unused pads and stubs along the traces.	Unused pads and stubs cause impedance discontinuities.		
	Route traces on appropriate layers.	Run pairs on different layers as needed to improve routing. For two-port designs, try to route no more than 4 pairs per layer. Use layers adjacent to ground or power layers if possible. Make sure digital signals on adjacent layers cross at 90° angles. Do not cross splits in power and ground planes.		
	Place termination resistors (and capacitors if applicable) close to Ethernet device	Prevents reflections. Use symmetrical pads. Do not connect termination components to differential pairs with stub traces.		
Transmit and Receive Differential Pairs (1000 Base-SX applications)	Design traces for 100 Ω differential impedance (± 15%)	Paired 50 Ω traces do not make 100 Ω differential. Check impedance calculator.		

Table 9. 82571EB Layout Checklist

SECTION	CHECK ITEMS	REMARKS	DONE	COMMENTS
	Avoid highly resistive traces, for example, 4 mil traces longer than 4 inches.	If trace length is a problem, use thicker board dielectrics to allow wider traces. Thicker copper is even better than wider traces.		
	Make traces symmetrical	Try to match the pairs at pads, vias and turns. Establish rules carefully for the autorouter. Asymmetry contributes to impedance mismatch.		
	Do not make 90° bends	Bevel corners with turns based on 45° angles.		
	Avoid through holes (vias).	If using through holes (vias), the budget is two per trace.		
	Keep traces close together within differential pairs.	Six mil spacing is good.		
	Keep trace-to-trace length difference within the transmit/receiver pairs to less than 10 mils.			
	Try to keep differential pairs 50 mils or more away from each other and away from parallel digital traces.	Minimizes crosstalk and noise injection. Tighter spacing is allowed closer to connections. Guard traces are generally not recommended and will reduce the impedance if done incorrectly.		
	Keep traces away from the board edge.	Controls EMI.		
	Avoid unused pads and stubs along the traces	Unused pads and stubs cause impedance discontinuities.		
	Route traces on appropriate layers.	Use layers adjacent to ground or power layers if possible. Make sure digital signals on adjacent layers cross at 90° angles. Do not cross splits in power and ground planes.		
	Place termination components close to the optical transceiver, if specified.	Prevents reflections. Use symmetrical pads. Do not connect termination components to differential pairs with stub traces.		

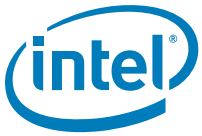


Table 9. 82571EB Layout Checklist

SECTION	CHECK ITEMS	REMARKS	DONE	COMMENTS
	On SerDes backplane applications, place AC coupling caps close to the receiver.			
Magnetics Module (10/100/1000 Base-T applications)	Capacitors connected to center taps should be placed very close to magnetics module.			
Power Supply and Signal Ground	Use planes if possible.	Narrow finger-like planes and very wide traces are allowed. If using traces, aim for 100 mils (minimum).		
	Use decoupling and bulk capacitors generously.	Place decoupling and bulk capacitors close to Ethernet device, with some along every side, using short, wide traces and large vias. If power is distributed on traces, bulk capacitors should be used at both ends. If power is distributed on cards, bulk capacitors should be used at the connector.		
	If using decoupling capacitors on LED lines, place them carefully.	Capacitors on LED lines should be placed near the LEDs.		
Chassis Ground	If possible, provide a separate chassis ground "island" to ground the shroud of the RJ-45 connector and to terminate the line side of the magnetics module. This design improves EMI behavior. This recommendation also applies to 1000 Base-SX designs.	Split in ground plane should be at least 50 mils. Split should run under center of magnetics module. Differential pairs never cross the split.		

Table 9. 82571EB Layout Checklist

SECTION	CHECK ITEMS	REMARKS	DONE	COMMENTS
	Place 4-6 pairs of pads for "stitching" capacitors to bridge the gap from chassis ground to signal ground.	Determine exact number and values empirically based on EMI performance.		
Termination Plane (10/100/1000 Base-T applications)	For designs with non-integrated magnetics modules, lay out chassis ground plane.	Splits in ground plane should be at least 50 mils.		
LED Circuits	Keep LED traces away from sources of noise, for example, high speed digital traces running in parallel.	LED traces can carry noise into integrated magnetics modules, RJ-45 connectors, or out to the edge of the board, increasing EMI.		

Table 10. 82572EI Layout Checklist

SECTION	CHECK ITEMS	REMARKS	DONE	COMMENTS
General	Have up-to-date product documentation and specification updates	Documents are subject to frequent change		
	Route the transmit and receive differential traces before routing the digital traces.	Layout of differential traces is critical.		
Ethernet Device	Place the Ethernet silicon at least 1 inch from the edge of the board and at least 1 inch from any integrated magnetics module.	With closer spacing, fields can follow the surface of the magnetics module or wrap past edge of board. EMI may increase. Optimum location is approximately 1 inch behind the magnetics module.		
	For the 82572EI controller, the trace impedance for the PCI Express differential pairs is 100 Ω +/- 15%	Match trace lengths between pairs to within 3 inches. Match trace lengths in each pair to within 5 mils.		

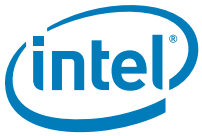


Table 10. 82572EI Layout Checklist

SECTION	CHECK ITEMS	REMARKS	DONE	COMMENTS
	For the 82572EI controller, place the PCI Express termination components carefully.	Connect the high-speed serial compensation resistor no more than 1" from the PE_RCMPp / PE_RCMPn balls. For 10/100/1000BASE-T applications, connect the MDI bias resistor no farther than 1" from the RBIAS0p / RBIAS0n and RBIAS1p / RBIAS1n balls. For 1000BASE-SX applications, connect the SerDes impedance compensation resistor no farther than 1" from the SER_RCMPp / SER_RCMPn balls.		
Clock Source	Place crystal and load capacitors within 0.75 inches from Ethernet device.	The Ethernet clock plays a key role in EMI.		
	Keep clock lines away from other digital traces, I/O ports, board edge, transformers and differential pairs			
	Follow crystal layout guidance in section 7.1.3	• 30 Ω (5%) 0402 resistor in series on Xtal2 • Device (ethernet controler), crystal, and load caps all on the same side of the board • Maximum of two (2) vias for load caps to ground • Maximum of 90 mils between load caps and crystal pads		
EEPROM and FLASH Memory	Placement is not critical due to slow signal speeds.	EEPROM and FLASH may be placed a few inches away from Ethernet controller to provide better spacing of critical components.		
Transmit and Receive Differential Pairs (10/100/1000 Base-T applications)	Design traces for 100 Ω differential impedance (± 15%)	Primary requirement for 10/100/1000 Mb/s Ethernet. Paired 50 Ω traces do not make 100 Ω differential. Check impedance calculator.		

Table 10. 82572EI Layout Checklist

SECTION	CHECK ITEMS	REMARKS	DONE	COMMENTS
	Use short traces.	Keep trace length under 4 inches from the Ethernet controller through the magnetics to the RJ-45 connector.		
	Avoid highly resistive traces, for example, 4 mil traces longer than 4 inches.	If trace length is a problem, use thicker board dielectrics to allow wider traces. Thicker copper is even better than wider traces.		
	Make traces symmetrical	Try to match the pairs at pads, vias and turns. Establish rules carefully for the autorouter. Asymmetry contributes to impedance mismatch.		
	Do not make 90° bends.	Bevel corners with turns based on 45° angles		
	Avoid through holes (vias).	If using through holes (vias), the budget is two per trace.		
	Keep traces close together within differential pairs.	Keep within 30 mils regardless of trace geometry.		
	Keep trace-to-trace length difference within each pair to less than 50 mils.	Minimizes signal skew and common mode noise. Improves long cable performance.		
	Pair-to-pair differences in length are not critical.	A 25% difference in length from longest pair to shortest pair is typical.		
	Try to keep differential pairs 100 mils or more away from each other and away from parallel digital traces.	Minimizes crosstalk and noise injection. Pairs may be spaced as close as 50 mils as long as crosstalk isolation is 34dB or more. Tighter spacing is allowed closer to connections. Guard traces are generally not recommended and will reduce the impedance if done incorrectly.		
	Keep traces away from the board edge.	Controls EMI.		
	Avoid unused pads and stubs along the traces.	Unused pads and stubs cause impedance discontinuities.		

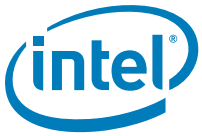


Table 10. 82572EI Layout Checklist

SECTION	CHECK ITEMS	REMARKS	DONE	COMMENTS
	Route traces on appropriate layers.	Run pairs on different layers as needed to improve routing. For two-port designs, try to route no more than 4 pairs per layer. Use layers adjacent to ground or power layers if possible. Make sure digital signals on adjacent layers cross at 90° angles. Do not cross splits in power and ground planes.		
	Place termination resistors (and capacitors if applicable) close to Ethernet device	Prevents reflections. Use symmetrical pads. Do not connect termination components to differential pairs with stub traces.		
Transmit and Receive Differential Pairs (1000 Base-SX applications)	Design traces for 100 Ω differential impedance (± 15%)	Paired 50 Ω traces do not make 100 Ω differential. Check impedance calculator.		
	Avoid highly resistive traces, for example, 4 mil traces longer than 4 inches.	If trace length is a problem, use thicker board dielectrics to allow wider traces. Thicker copper is even better than wider traces.		
	Make traces symmetrical	Try to match the pairs at pads, vias and turns. Establish rules carefully for the autorouter. Asymmetry contributes to impedance mismatch.		
	Do not make 90° bends	Bevel corners with turns based on 45° angles.		
	Avoid through holes (vias).	If using through holes (vias), the budget is two per trace.		
	Keep traces close together within differential pairs.	Six mil spacing is good.		
	Keep trace-to-trace length difference within the transmit/receiver pairs to less than 10 mils.			

Table 10. 82572EI Layout Checklist

SECTION	CHECK ITEMS	REMARKS	DONE	COMMENTS
	Try to keep differential pairs 50 mils or more away from each other and away from parallel digital traces.	Minimizes crosstalk and noise injection. Tighter spacing is allowed closer to connections. Guard traces are generally not recommended and will reduce the impedance if done incorrectly.		
	Keep traces away from the board edge.	Controls EMI.		
	Avoid unused pads and stubs along the traces	Unused pads and stubs cause impedance discontinuities.		
	Route traces on appropriate layers.	Use layers adjacent to ground or power layers if possible. Make sure digital signals on adjacent layers cross at 90° angles. Do not cross splits in power and ground planes.		
	Place termination components close to the optical transceiver, if specified.	Prevents reflections. Use symmetrical pads. Do not connect termination components to differential pairs with stub traces.		
	On SerDes backplane applications, place AC coupling caps close to the receiver.			
Magnetics Module (10/100/1000 Base-T applications)	Capacitors connected to center taps should be placed very close to magnetics module.			
Power Supply and Signal Ground	Use planes if possible.	Narrow finger-like planes and very wide traces are allowed. If using traces, aim for 100 mils (minimum).		
	Use decoupling and bulk capacitors generously.	Place decoupling and bulk capacitors close to Ethernet device, with some along every side, using short, wide traces and large vias. If power is distributed on traces, bulk capacitors should be used at both ends. If power is distributed on cards, bulk capacitors should be used at the connector.		

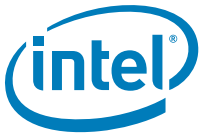


Table 10. 82572EI Layout Checklist

SECTION	CHECK ITEMS	REMARKS	DONE	COMMENTS
	If using decoupling capacitors on LED lines, place them carefully.	Capacitors on LED lines should be placed near the LEDs.		
Chassis Ground	AIf possible, provide a separate chassis ground "island" to ground the shroud of the RJ-45 connector and to terminate the line side of the magnetics module. This design improves EMI behavior. This recommendation also applies to 1000 Base-SX designs.	Split in ground plane should be at least 50 mils. Split should run under center of magnetics module. Differential pairs never cross the split.		
	Place 4-6 pairs of pads for "stitching" capacitors to bridge the gap from chassis ground to signal ground.	Determine exact number and values empirically based on EMI performance.		
Termination Plane (10/100/1000 Base-T applications)	For designs with non-integrated magnetics modules, lay out chassis ground plane.	Splits in ground plane should be at least 50 mils.		
LED Circuits	Keep LED traces away from sources of noise, for example, high speed digital traces running in parallel.	LED traces can carry noise into integrated magnetics modules, RJ-45 connectors, or out to the edge of the board, increasing EMI.		

10.0 Reference Schematics

The following are reference schematics describing typical designs for the 82571EB/ 82572EI Gigabit Ethernet Controller. Both copper and SERDES are included.

82571EB REFERENCE DESIGN (Copper)

PAGE INDEX

For power delivery solutions refer to the "82571EB/82572EI Gigabit Ethernet Controller Design Guide" Application Note (AP-447)

Rev. 8.0
01/2008

DNP

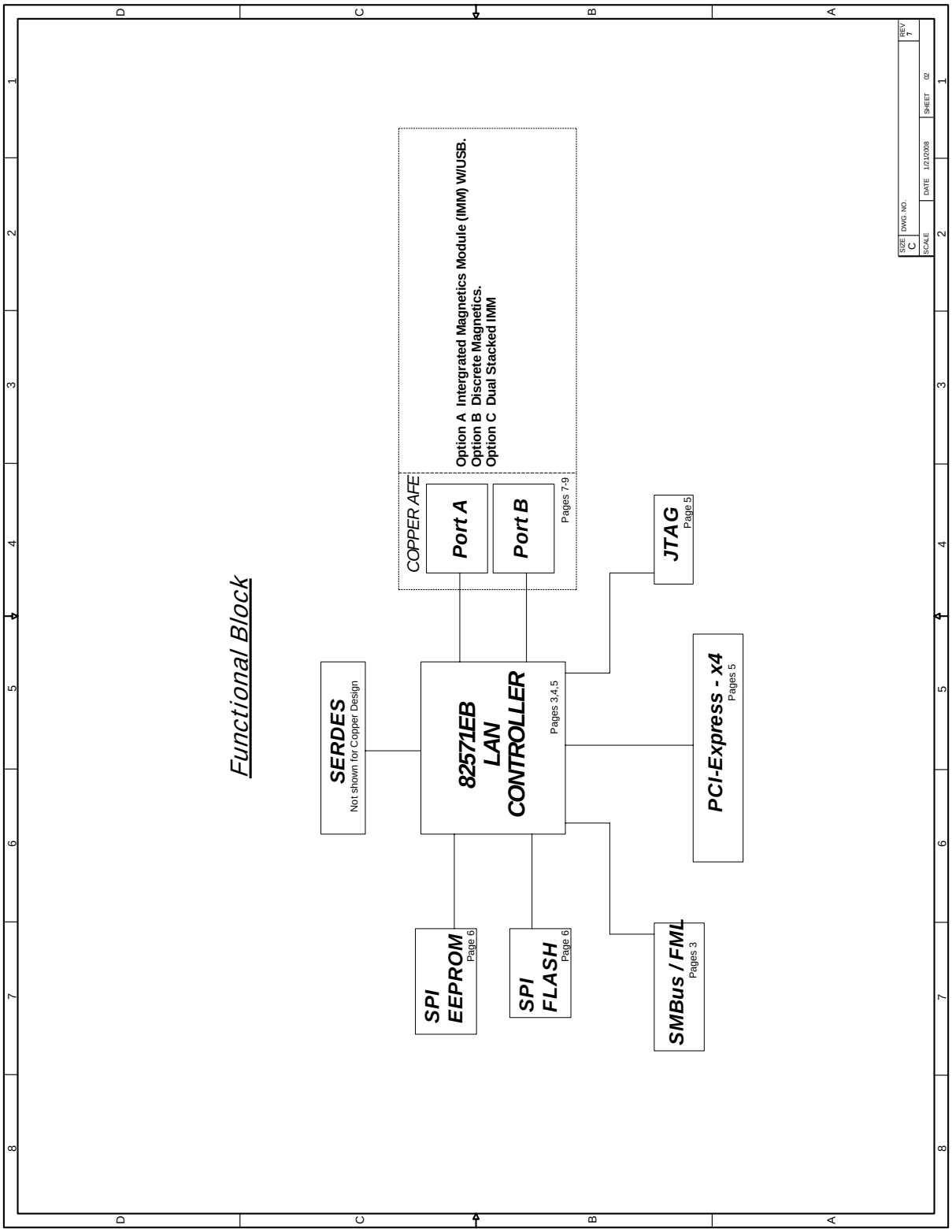
DNP - Do Not Populate symbol. This is a component stuffing option for an optional feature, special debug or testing purposes.

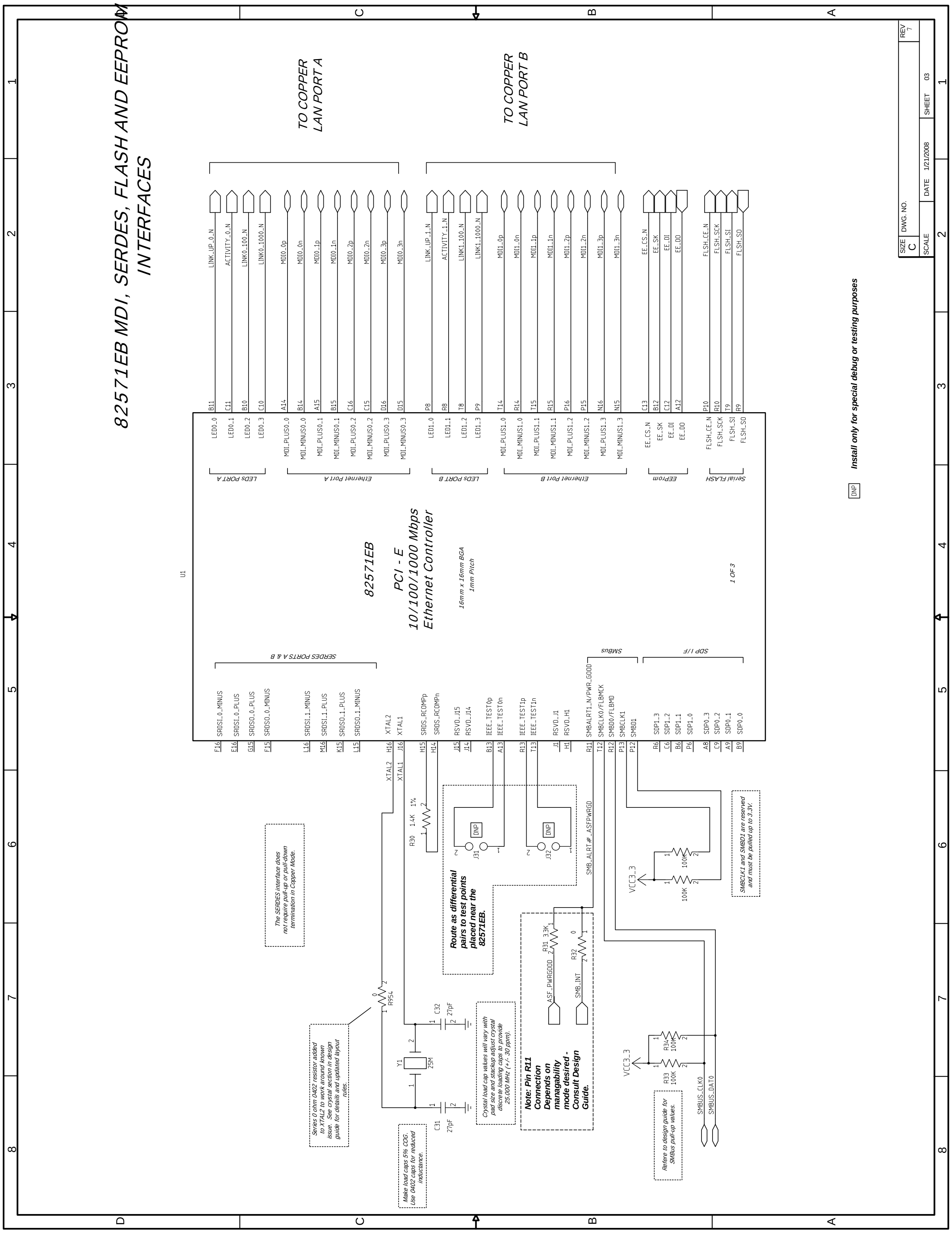
intel
2111 N. E. 25th Avenue
Hillsboro, OR 97124-5961

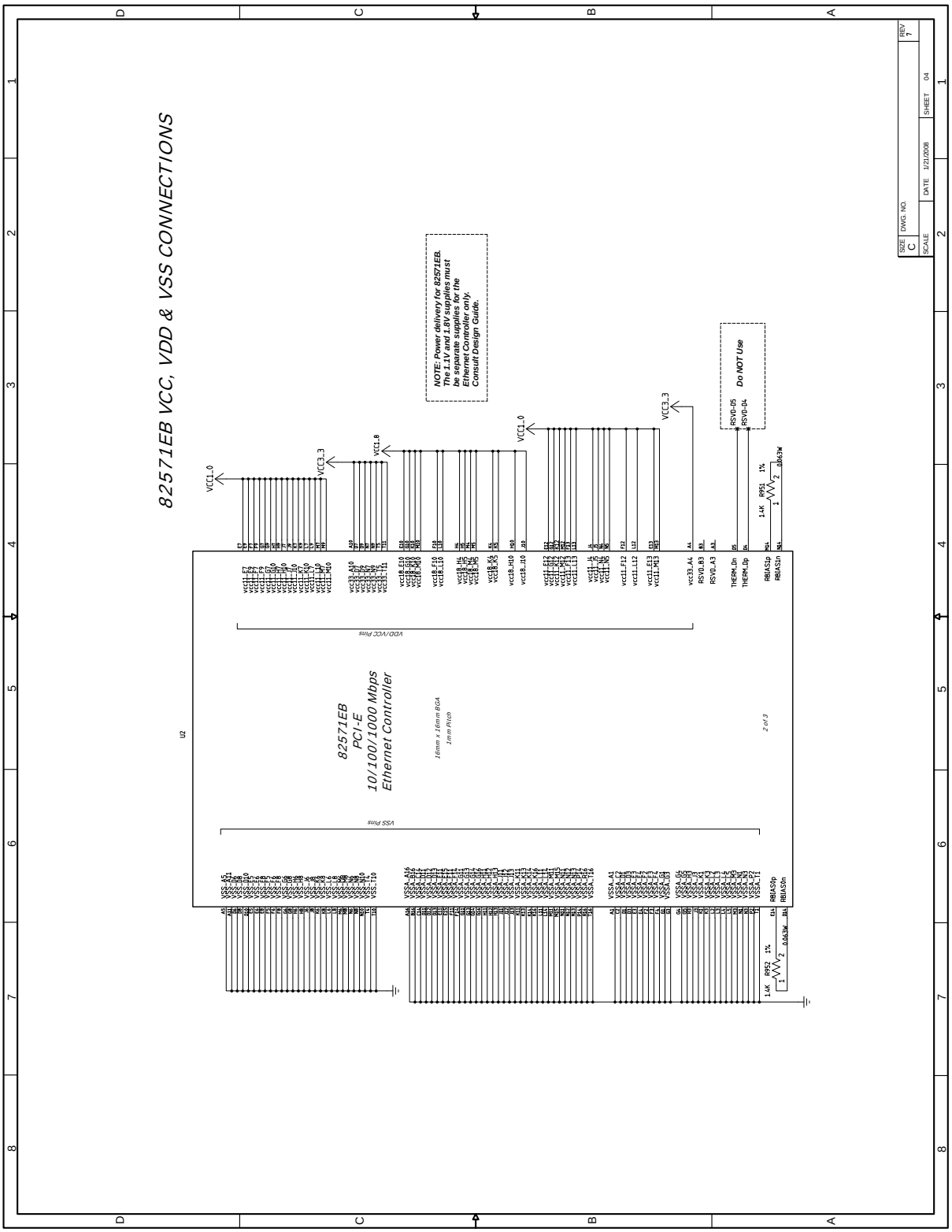
TITLE: 82571EB Reference Design

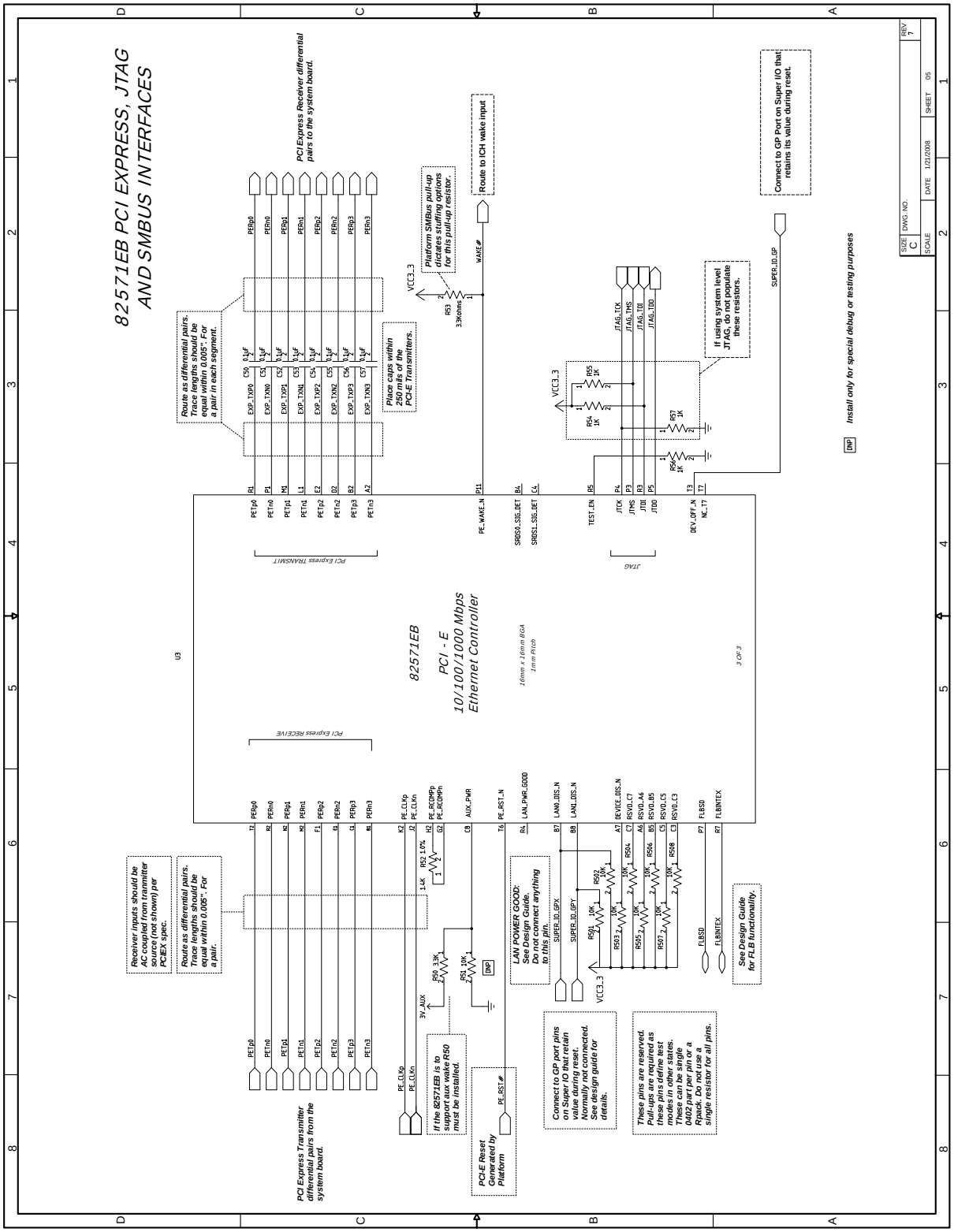
SIZE: C | DWG. NO. | REV: 7

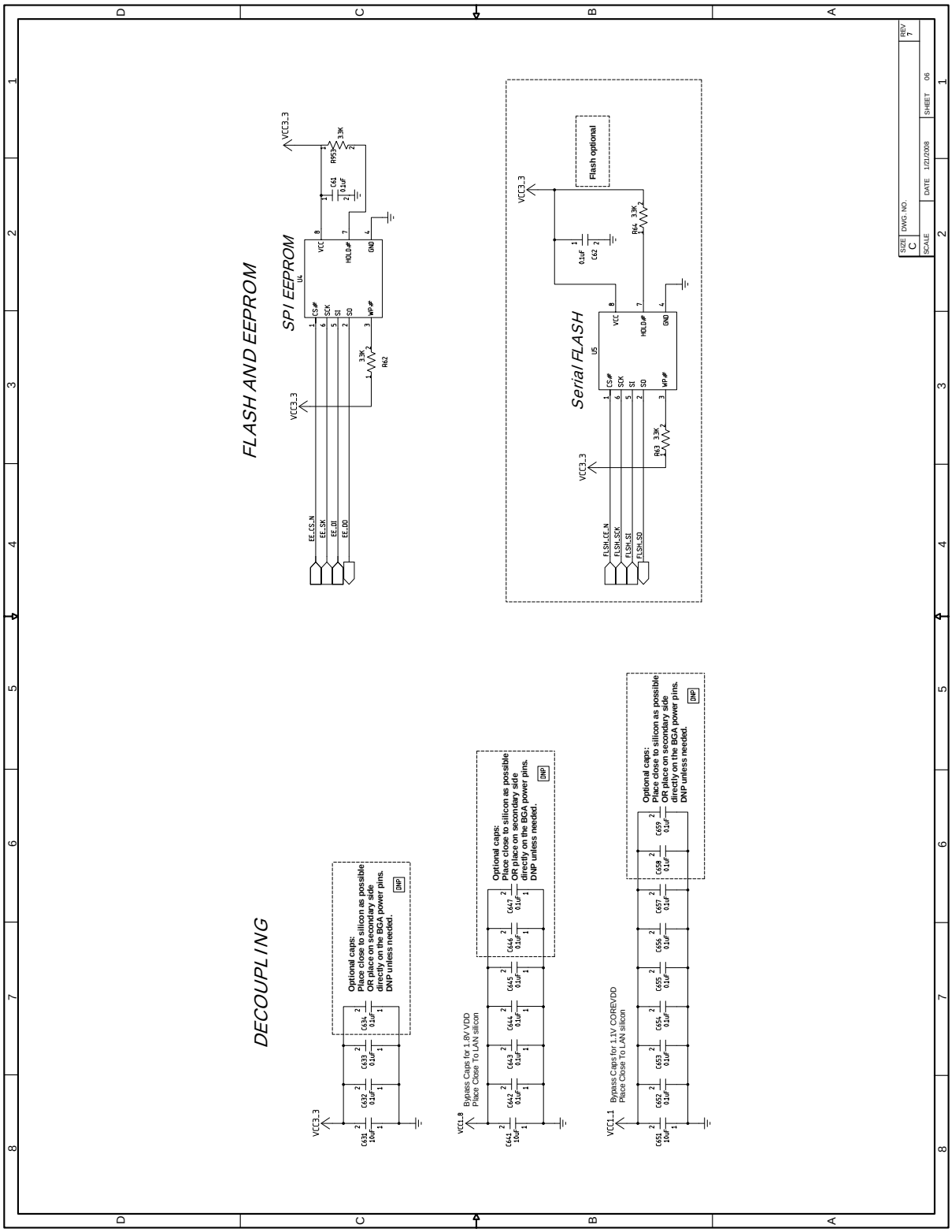
SCALE | DATE 1/21/2008 | SHEET 01

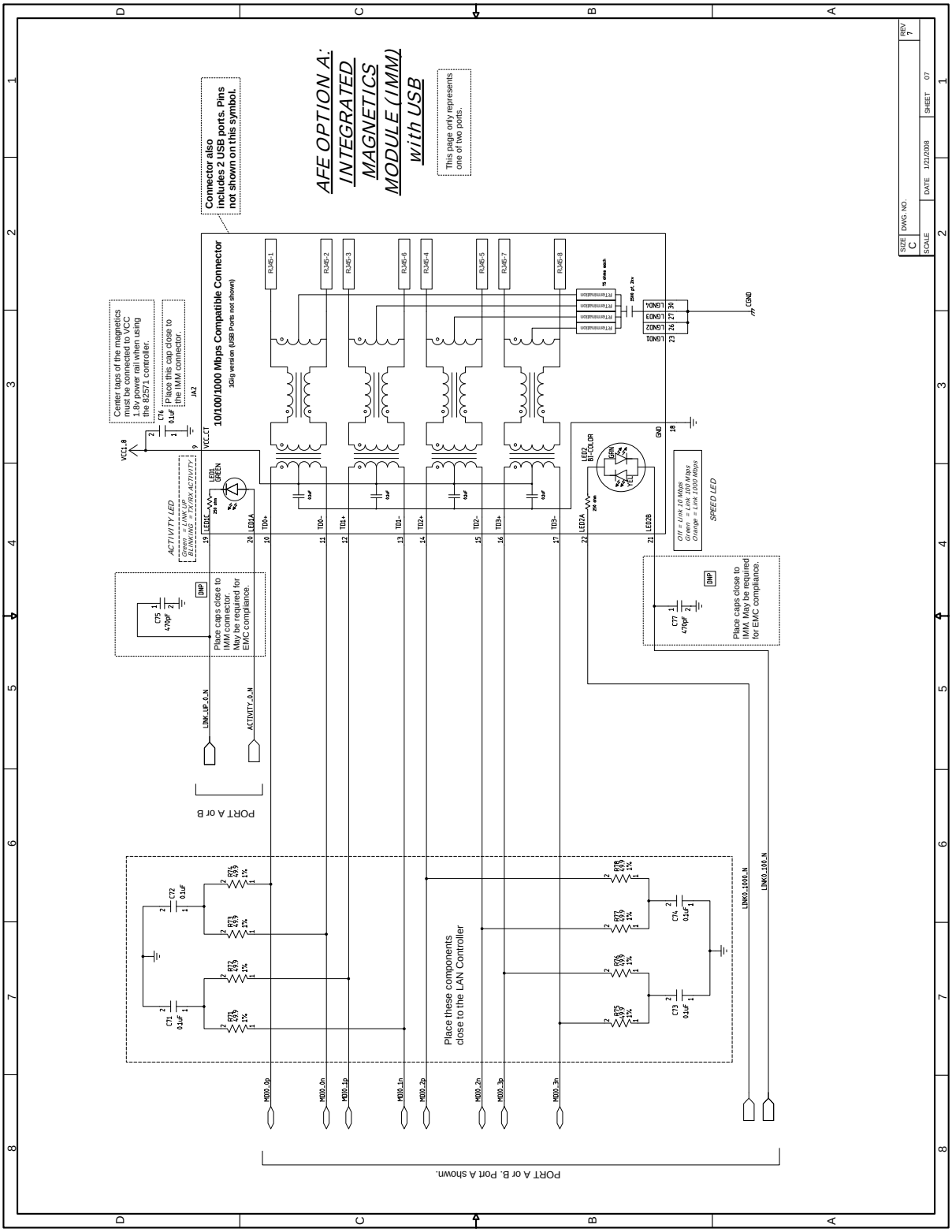

Functional Block
COPPER AFE
Port A
Port B
Pages 7-9
Option A Intergrated Magnetics Module (IMM) W/USB.
Option B Discrete Magnetics.
Option C Dual Stacked IMM
SERDES
Not shown for Copper Design
82571EB
LAN
CONTROLLER
Pages 3,4,5
JTAG
Page 5
PCI-Express - x4
Pages 5
SPI
EEPROM
Page 6
SPI
FLASH
Page 6
SMBus / FML
Pages 3
SIZE
C
DWG. NO.
SCALE
DATE
1/21/2008
SHEET
02
REV
1

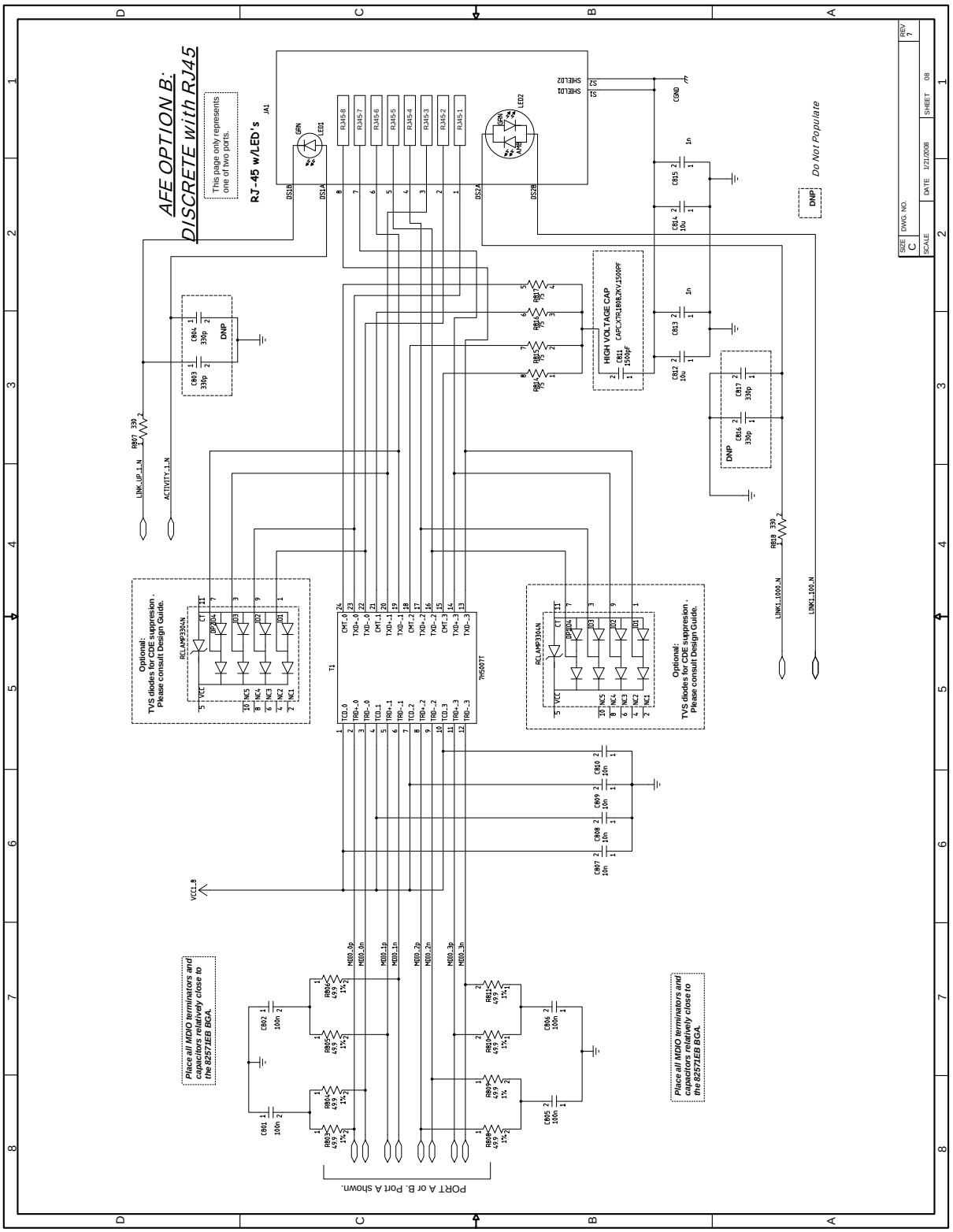

82571EB MDI, SERDES, FLASH AND EEPROM INTERFACES
TO COPPER LAN PORT A
TO COPPER LAN PORT B
82571EB
PCI - E
10/100/1000 Mbps
Ethernet Controller
16mm x 16mm BGA
1mm Pitch
1 OF 3
Install only for special debug or testing purposes
Route as differential pairs to test points placed near the 82571EB.
Note: Pin R11 Connection Depends on managability mode desired - Consult Design Guide.
Make load caps 5% COG. Use 0402 caps for reduced inductance.

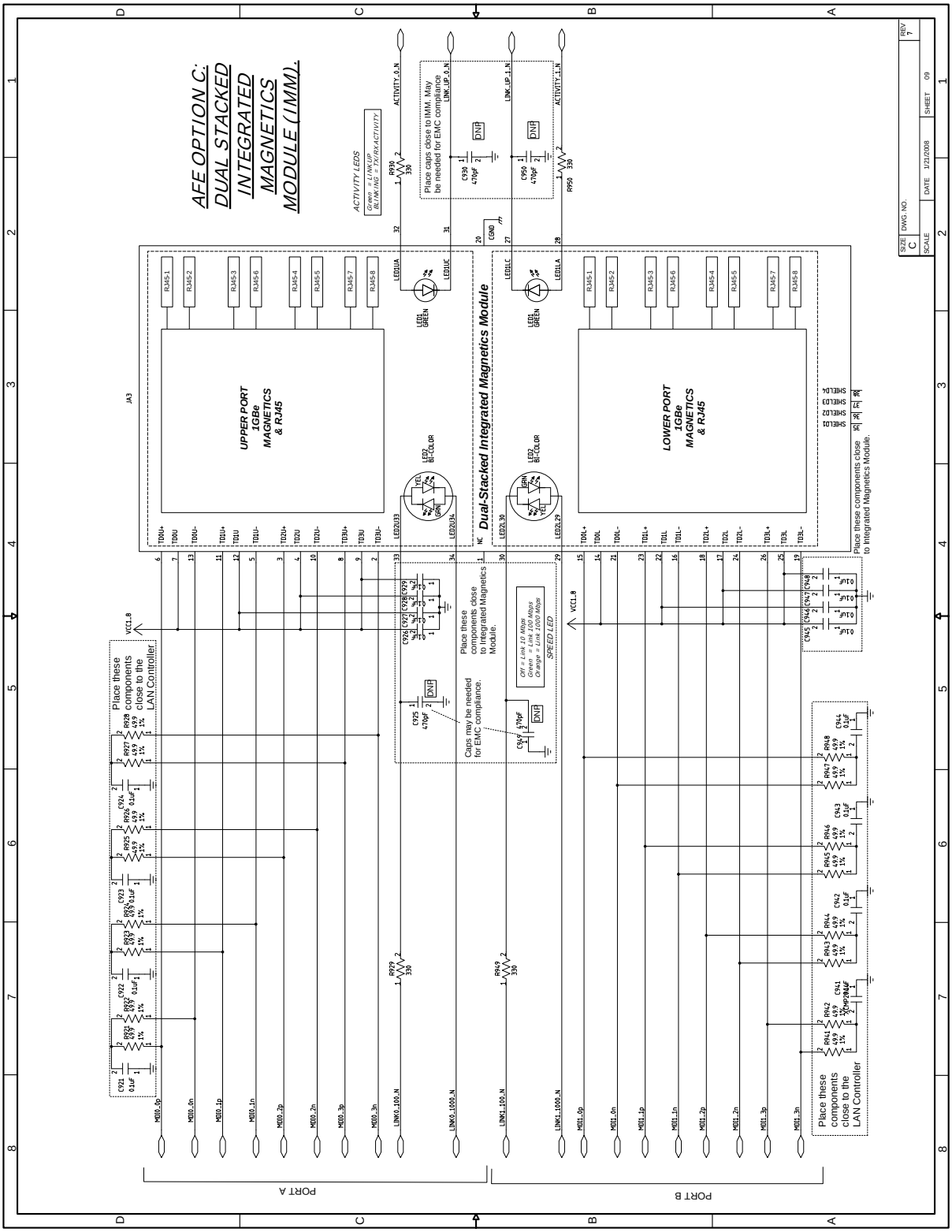

82571EB VCC, VDD & VSS CONNECTIONS
NOTE: Power delivery for 82571EB. The 1.1V and 1.8V supplies must be sourced from switching regulators. Consult Design Guide.
Do NOT Use
82571EB
PCI-E
10/100/1000 Mbps
Ethernet Controller
16mm x 16mm BGA
1mm Pitch
VDD/VCC Pins
VSS Pins
VCC1_0
VCC3_3
VCC1_8
RSVD-D5
RSVD-D4
RPS1
RPS2
1.4K
1%
0.063W
SIZE
C
DWG. NO.
REV
7
SCALE
DATE
1/21/2008
SHEET
04

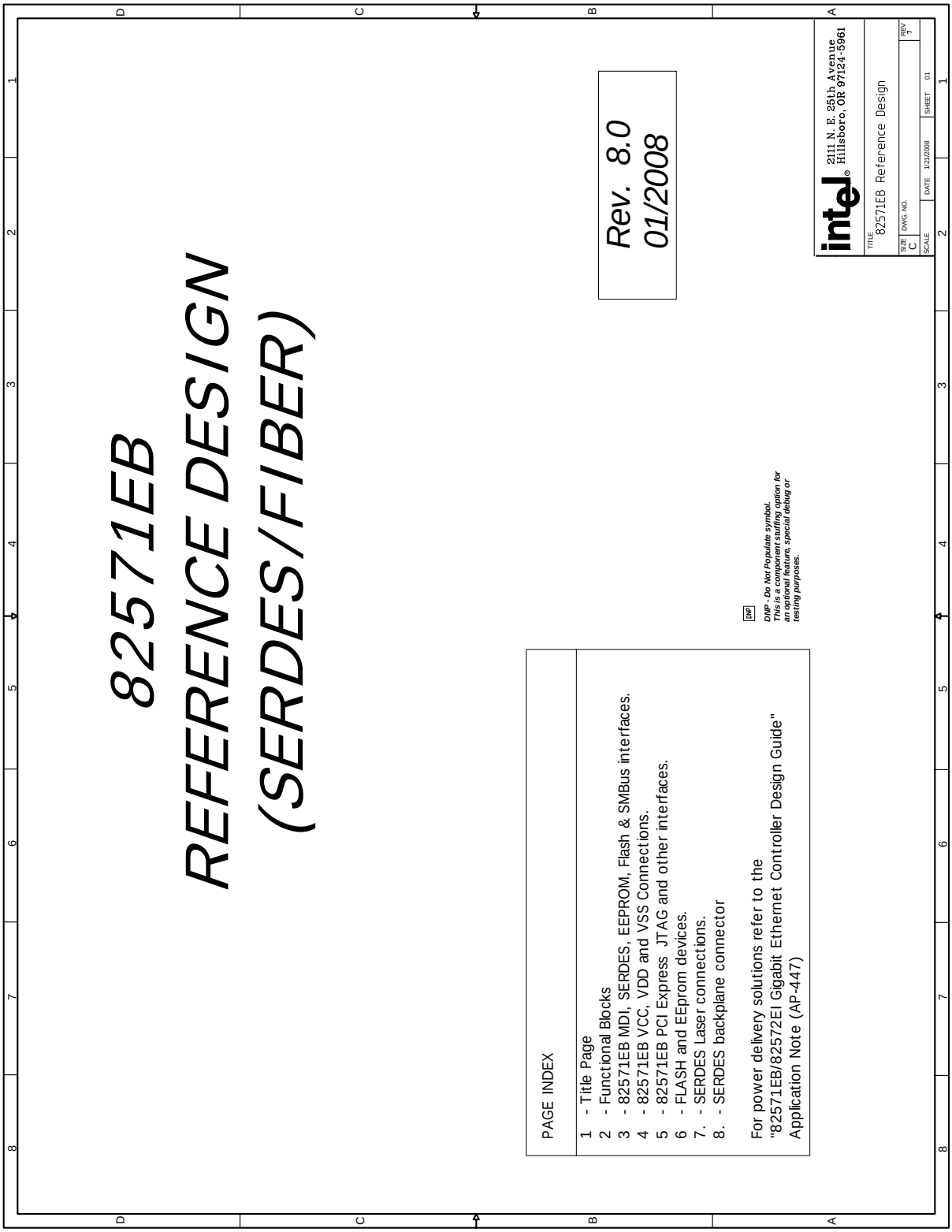

82571EB PCI EXPRESS, JTAG AND SMBUS INTERFACES
82571EB
PCI - E
10/100/1000 Mbps
Ethernet Controller
16mm x 16mm BGA
1mm Pitch
3 OF 3
PCI Express TRANSMIT
PCI Express RECEIVE
JTAG
Receiver inputs should be AC coupled from transmitter source (not shown) per PCIEX spec.
Route as differential pairs. Trace lengths should be equal within 0.005". For a pair.
PCI Express Transmitter differential pairs from the system board.
If the 82571EB is to support aux wake R50 must be installed.
PCI-E Reset Generated by Platform
Route as differential pairs. Trace lengths should be equal within 0.005". For a pair in each segment.
Place caps within 250 mils of the PCI-E Transmitters.
PCI Express Receiver differential pairs to the system board.
Platform SMBus pull-up dictates stuffing options for this pull-up resistor.
Route to ICH wake input
If using system level JTAG, do not populate these resistors.
Connect to GP Port on Super I/O that retains its value during reset.
LAN POWER GOOD: See Design Guide. Do not connect anything to this pin.
Connect to GP port pins on Super IO that retain value during reset. Normally not connected. See design guide for details.
These pins are reserved. Pull-ups are required as these pins define test modes in other states. These can be single 0402 part per pin or a Rpack. Do not use a single resistor for all pins.
See Design Guide for FLB functionality.
Install only for special debug or testing purposes
SIZE C
DWG. NO.
REV 7
SCALE
DATE 1/21/2008
SHEET 05

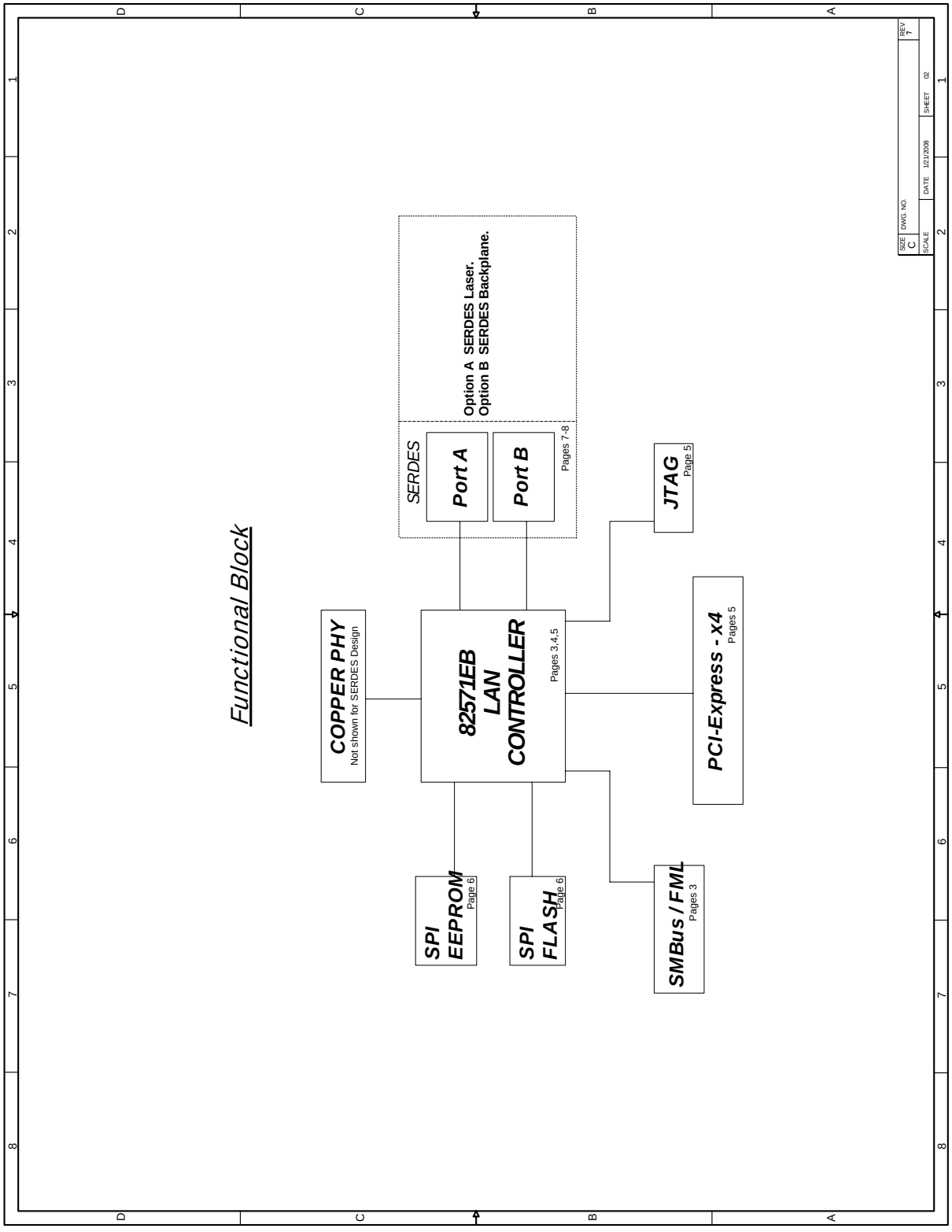

FLASH AND EEPROM
SPI EEPROM
Serial FLASH
Flash optional
DECOUPLING
Optional caps:
Place close to silicon as possible
OR place on secondary side
directly on the BGA power pins.
DNP unless needed.
DNP
Bypass Caps for 1.8V VDD
Place Close To LAN silicon
Bypass Caps for 1.1V COREVDD
Place Close To LAN silicon
EE_CS_N
EE_SCK
EE_DI
EE_DO
FLSH_CE_N
FLSH_SCK
FLSH_SI
FLSH_SO
SIZE C
DWG. NO.
REV 7
SCALE
DATE 1/21/2008
SHEET 06

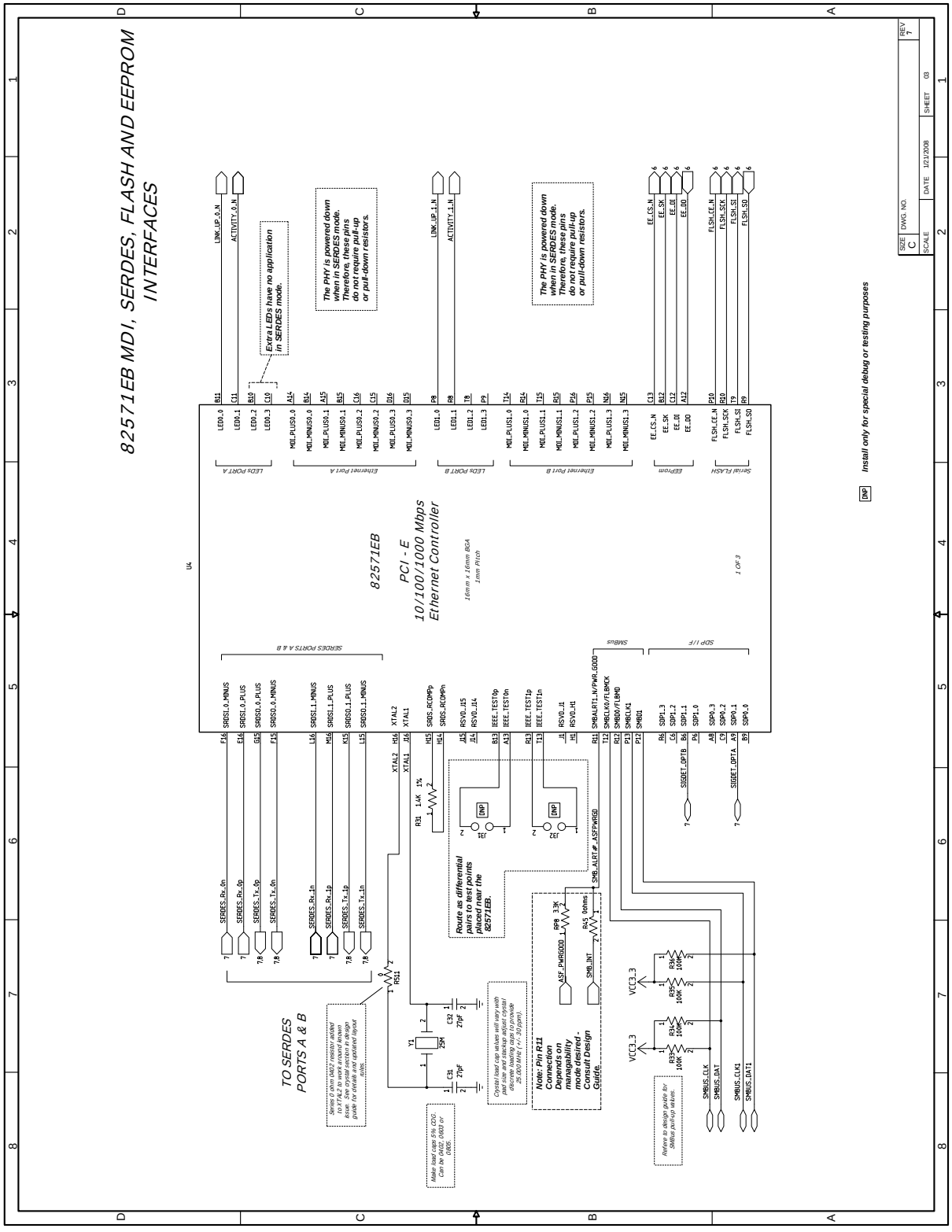

AFE OPTION A:
INTEGRATED
MAGNETICS
MODULE (IMM)
with USB
This page only represents one of two ports.
Connector also includes 2 USB ports. Pins not shown on this symbol.
10/100/1000 Mbps Compatible Connector
1Gig version (USB Ports not shown)
Center taps of the magnetics must be connected to VCC 1.8v power rail when using the 82571 controller.
Place this cap close to the IMM connector.
Place caps close to IMM connector. May be required for EMC compliance.
Place caps close to IMM. May be required for EMC compliance.
ACTIVITY LED
Green = LINK UP
BLINKING = TX/RX ACTIVITY
SPEED LED
Off = Link 10 Mbps
Green = Link 100 Mbps
Orange = Link 1000 Mbps
Place these components close to the LAN Controller
PORT A or B
PORT A or B. Port A shown.

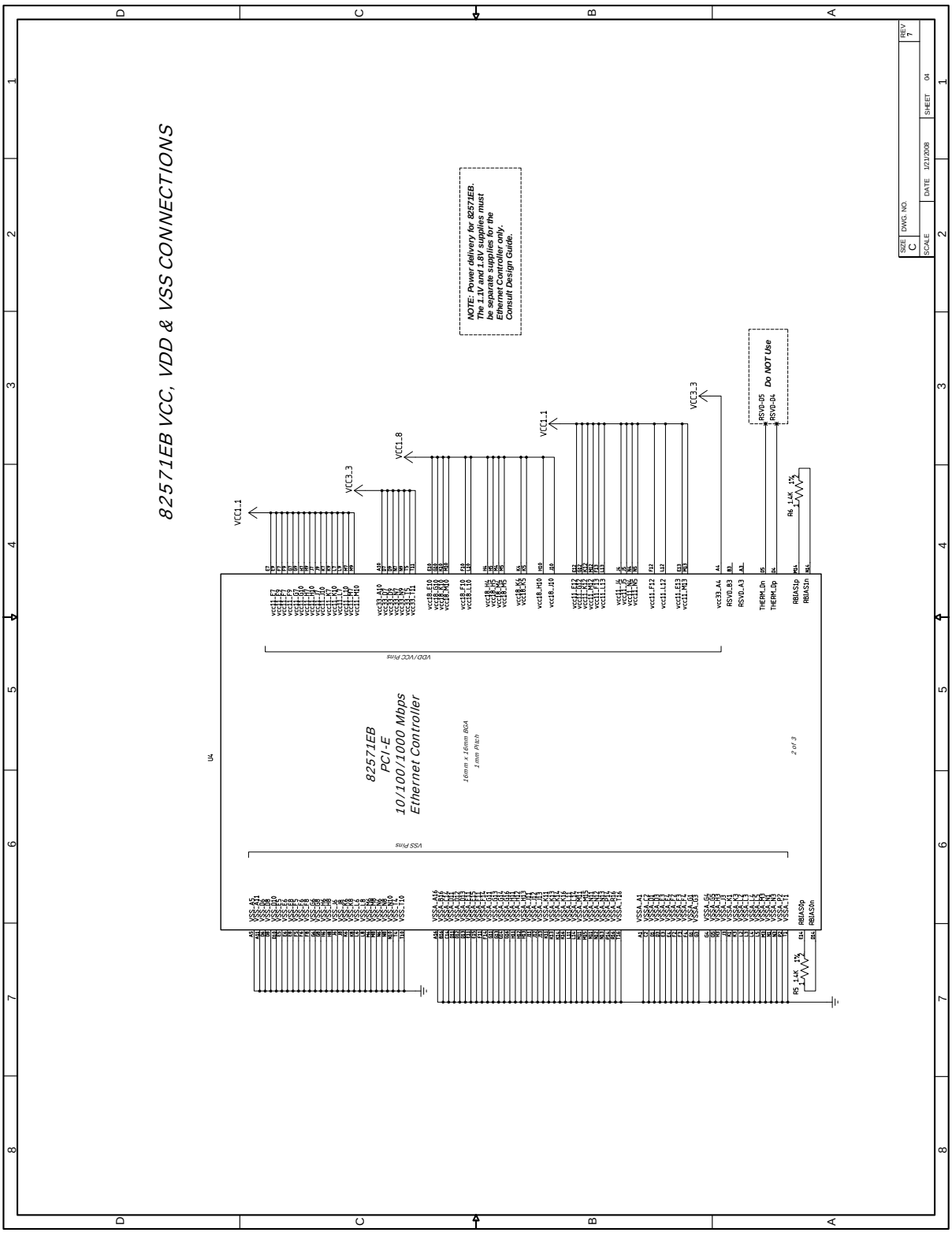

AFE OPTION B:
DISCRETE with RJ45
RJ-45 w/LED's
This page only represents one of two ports.
Do Not Populate
HIGH VOLTAGE CAP
Optional:
TVS diodes for CDE suppresion .
Please consult Design Guide.
Place all MDIO terminators and capacitors relatively close to the 82571EB BGA.
PORT A or B. Port A Shown.

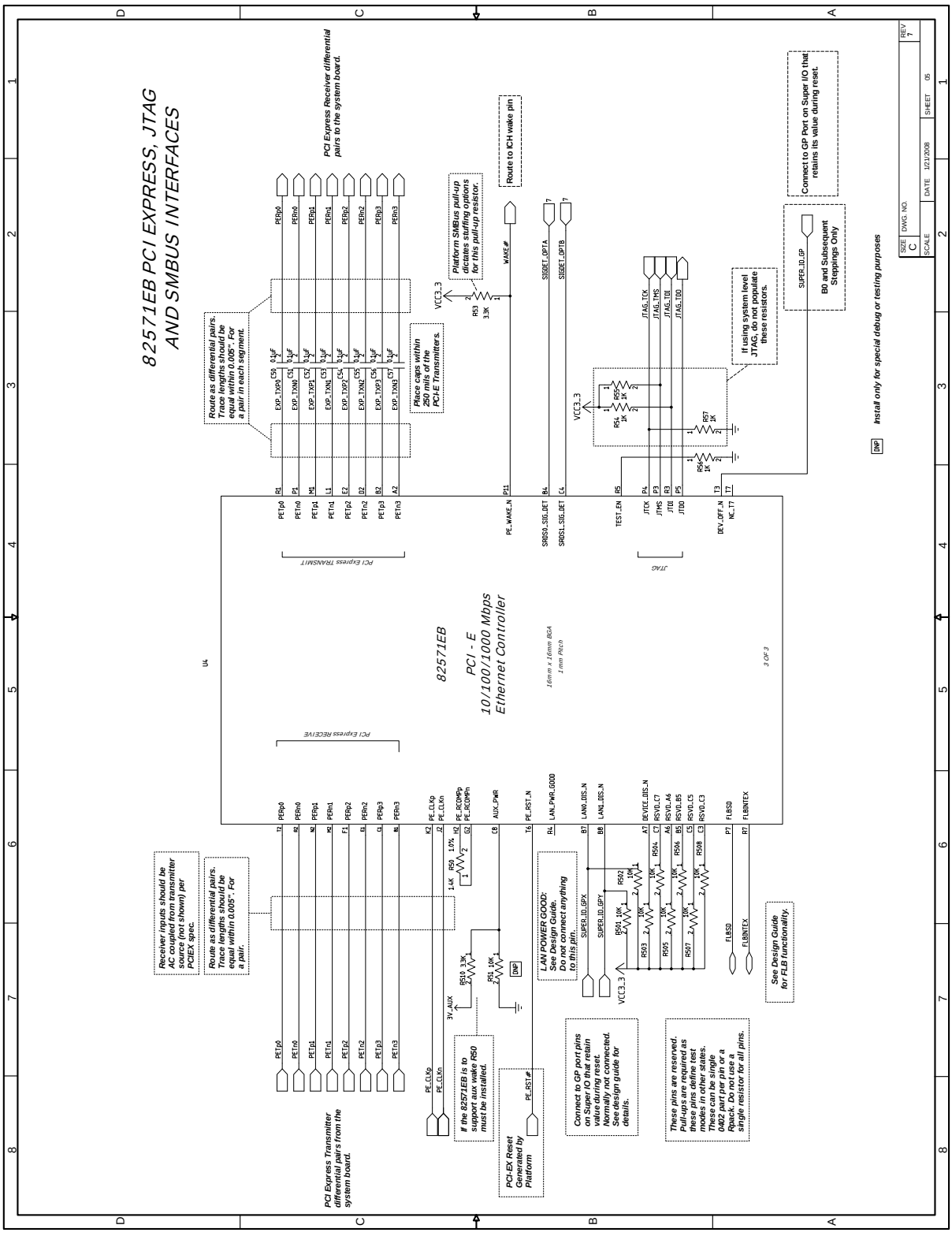

AFE OPTION C:
DUAL STACKED
INTEGRATED
MAGNETICS
MODULE (IMM).
Dual-Stacked Integrated Magnetics Module
UPPER PORT
1GBe
MAGNETICS
& RJ45
LOWER PORT
1GBe
MAGNETICS
& RJ45
ACTIVITY LEDS
Green = LINKUP
BLINKING = TX/RX ACTIVITY
Place caps close to IMM. May be needed for EMC compliance
Place these components close to the LAN Controller
Place these components close to Integrated Magnetics Module.
Caps may be needed for EMC compliance.
SPEED LED
Off = Link 10 Mbps
Green = Link 100 Mbps
Orange = Link 1000 Mbps
PORT A
PORT B
SIZE C
DWG. NO.
REV 7
SCALE
DATE 1/31/2008
SHEET 09

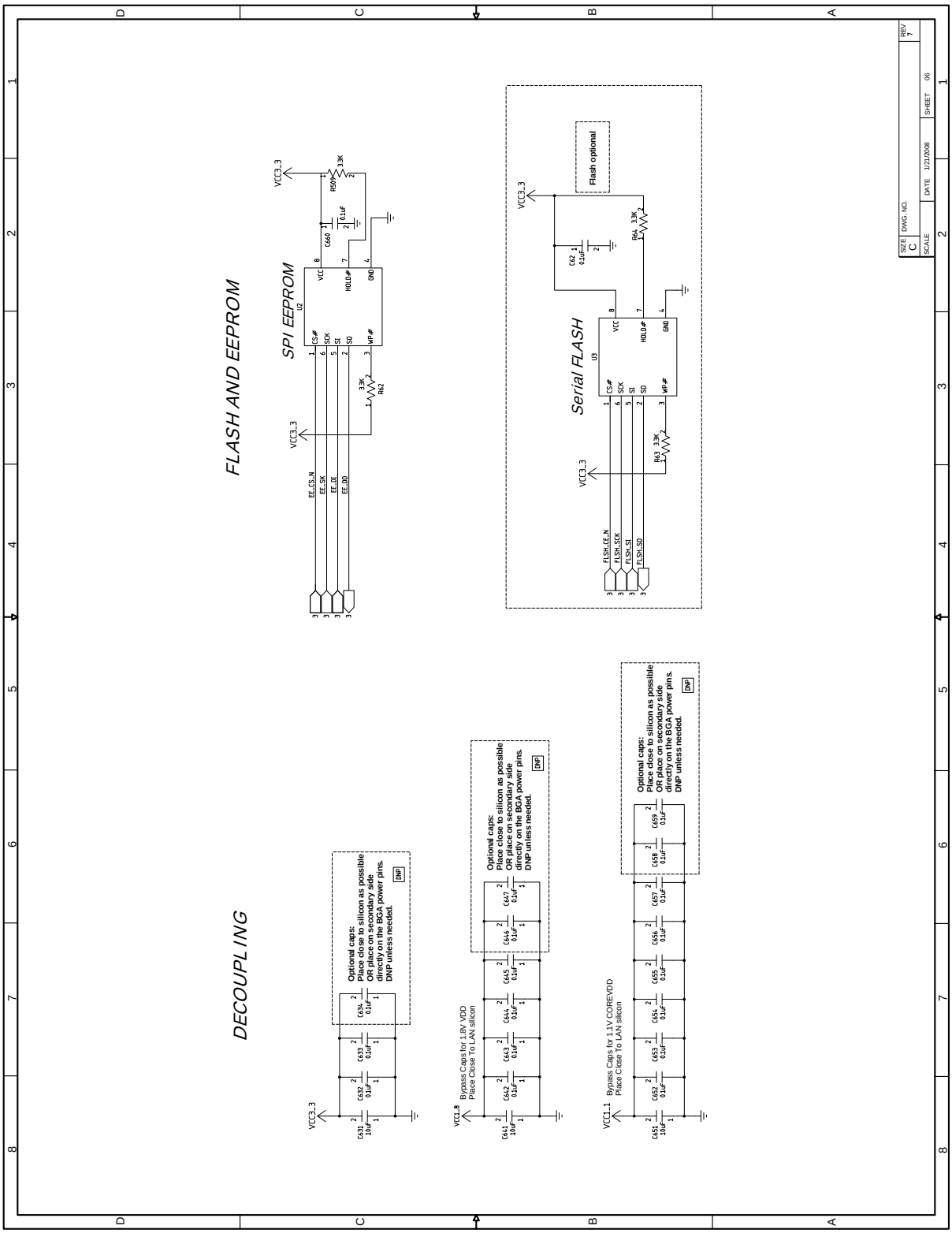

82571EB
REFERENCE DESIGN
(SERDES/FIBER)
Rev. 8.0
01/2008
PAGE INDEX
1 - Title Page
2 - Functional Blocks
3 - 82571EB MDI, SERDES, EEPROM, Flash & SMBus interfaces.
4 - 82571EB VCC, VDD and VSS Connections.
5 - 82571EB PCI Express JTAG and other interfaces.
6 - FLASH and EEprom devices.
7. - SERDES Laser connections.
8. - SERDES backplane connector
For power delivery solutions refer to the "82571EB/82572EI Gigabit Ethernet Controller Design Guide" Application Note (AP-447)
DNP
DNP - Do Not Populate symbol. This is a component stuffing option for assembly flexibility, special debug or testing purposes.
intel
2111 N. E. 25th Avenue
Hillsboro, OR 97124-5961
TITLE
82571EB Reference Design
SIZE C
DWG. NO.
REV 7
SCALE
DATE 1/21/2008
SHEET 01

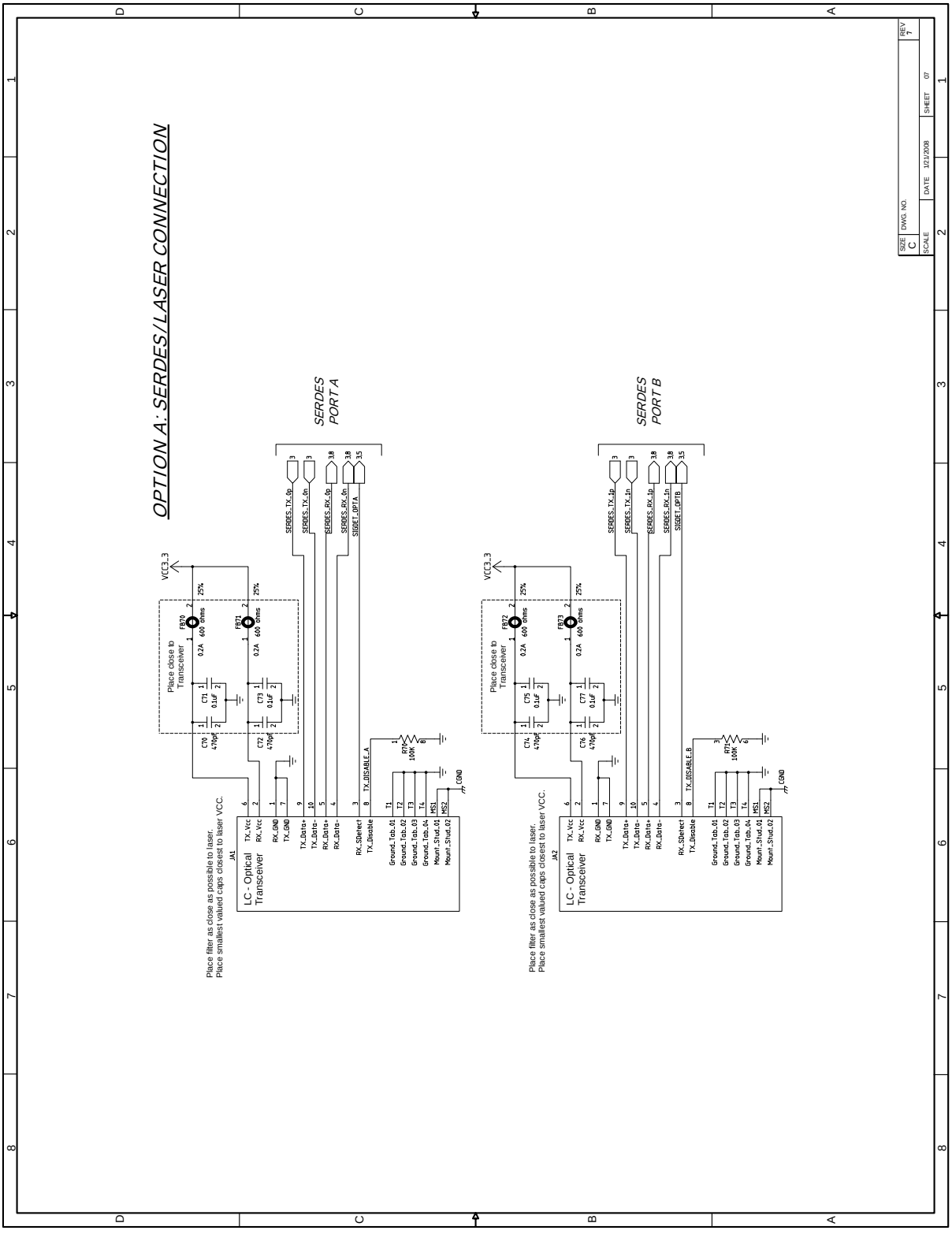

Functional Block
SERDES
Port A
Port B
Pages 7-8
Option A SERDES Laser.
Option B SERDES Backplane.
JTAG
Page 5
COPPER PHY
Not shown for SERDES Design
82571EB
LAN
CONTROLLER
Pages 3,4,5
PCI-Express - x4
Pages 5
SPI
EEPROM
Page 6
SPI
FLASH
Page 6
SMBus / FML
Pages 3
SIZE
C
DWG. NO.
REV
A
SCALE
DATE
1/21/2008
SHEET
02

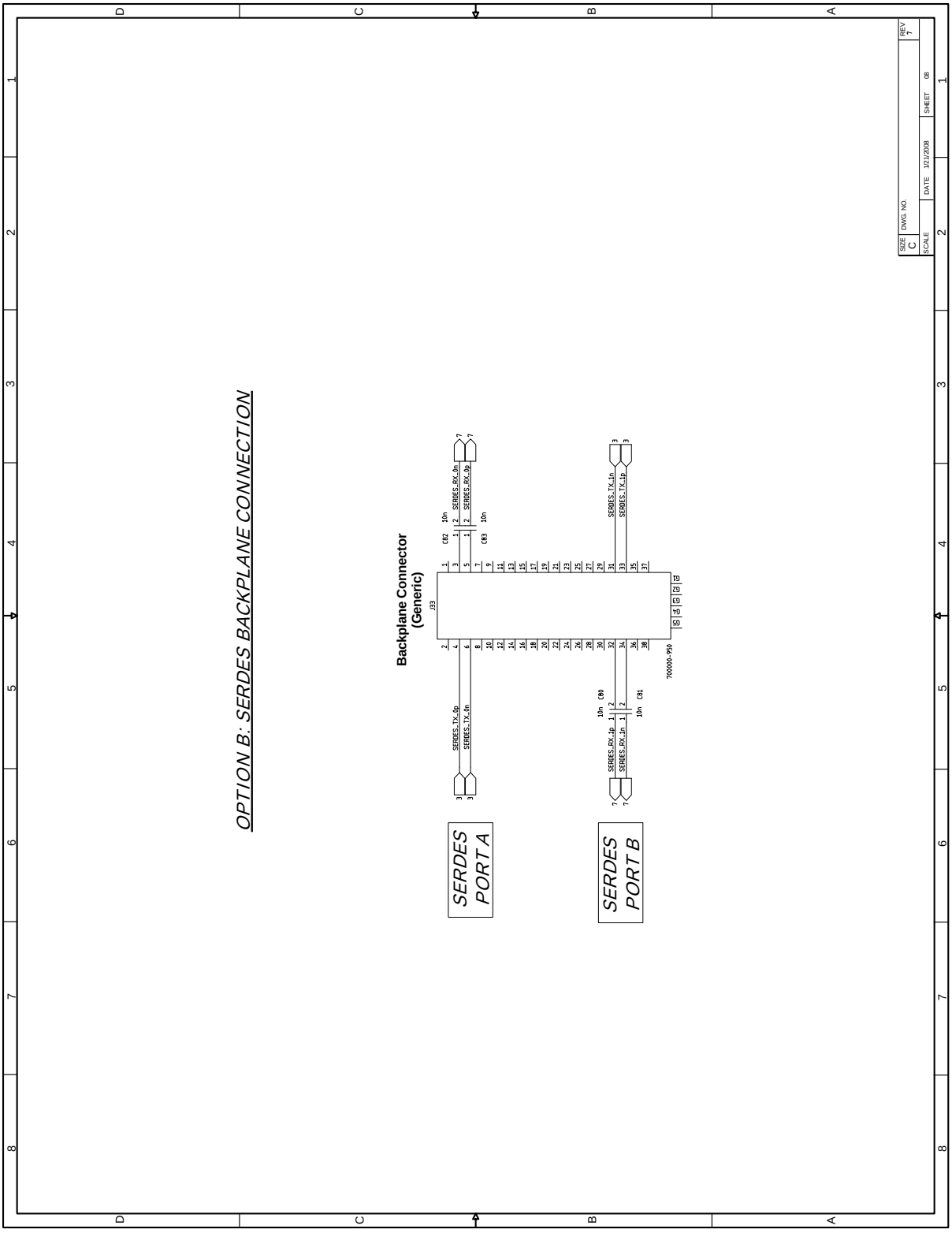

82571EB MDI, SERDES, FLASH AND EEPROM INTERFACES
82571EB
PCI - E
10/100/1000 Mbps
Ethernet Controller
16mm x 16mm BGA
1mm Pitch
1 OF 3
TO SERDES PORTS A & B
Route as differential pairs to test points placed near the 82571EB.
Note: Pin R11 Connection Depends on managability mode desired - Consult Design Guide.
The PHY is powered down when in SERDES mode. Therefore, these pins do not require pull-up or pull-down resistors.
Extra LEDs have no application in SERDES mode.
Install only for special debug or testing purposes
LED0_0
LED0_1
LED0_2
LED0_3
LED1_0
LED1_1
LED1_2
LED1_3
LINK_UP_0_N
ACTIVITY_0_N
LINK_UP_1_N
ACTIVITY_1_N
SERDES_Rx_0n
SERDES_Rx_0p
SERDES_Tx_0p
SERDES_Tx_0n
SERDES_Rx_1n
SERDES_Rx_1p
SERDES_Tx_1p
SERDES_Tx_1n
SMBUS_CLK
SMBUS_DAT
SMBUS_CLK1
SMBUS_DAT1
EE_CS_N
EE_SK
EE_DI
EE_DO
FLSH_CE_N
FLSH_SCK
FLSH_SI
FLSH_SO
SIDP1_3
SIDP1_2
SIDP1_1
SIDP1_0
SIDP0_3
SIDP0_2
SIDP0_1
SIDP0_0
SIGDET_OPTB
SIGDET_OPTA
SMB_ALRT#_ASFPWRGD
SMB_INT
ASF_PWRGOOD
VCC3_3
DNP

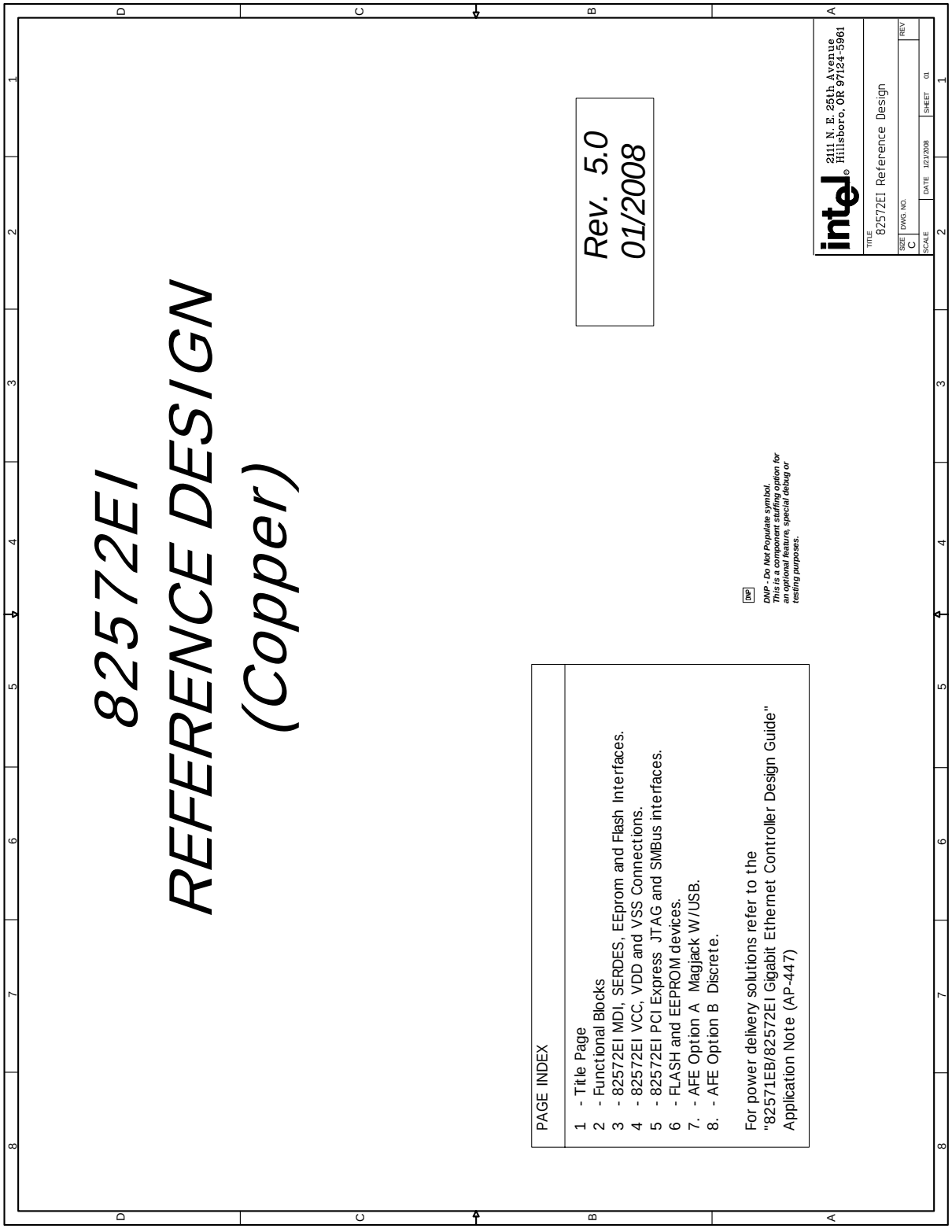

82571EB VCC, VDD & VSS CONNECTIONS
NOTE: Power delivery for 82571EB. The 1.1V and 1.8V supplies must be separate supplies for the Ethernet Controller only. Consult Design Guide.
Do NOT Use
82571EB
PCI-E
10/100/1000 Mbps
Ethernet Controller
16mm x 16mm BGA
1mm Pitch
2 of 3
VDD/VCC Pins
VSS Pins
VCC1_1
VCC3_3
VCC1_8
R5 1.4K 1%
R6 1.4K 1%
SIZE C
DWG. NO.
REV 7
SCALE
DATE 1/21/2008
SHEET 04

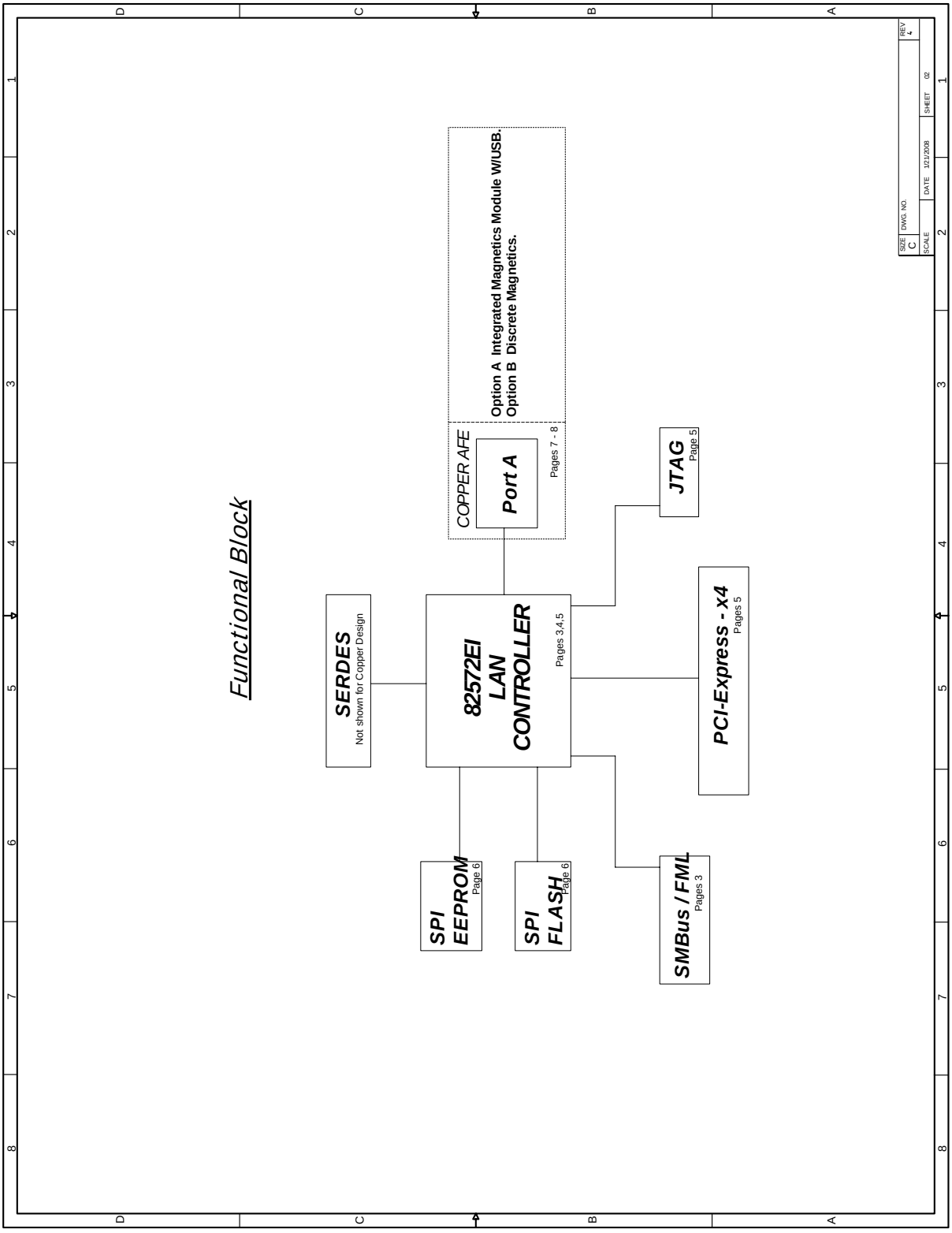

82571EB PCI EXPRESS, JTAG
AND SMBUS INTERFACES
82571EB
PCI - E
10/100/1000 Mbps
Ethernet Controller
16mm x 16mm BGA
1mm Pitch
3 OF 3
PCI Express TRANSMIT
PCI Express RECEIVE
JTAG
Route as differential pairs. Trace lengths should be equal within 0.005". For a pair in each segment.
PCI Express Receiver differential pairs to the system board.
Place caps within 250 mils of the PCI-E Transmitters.
Platform SMBus pull-up dictates stuffing options for this pull-up resistor.
Route to ICH wake pin
If using system level JTAG, do not populate these resistors.
Connect to GP Port on Super I/O that retains its value during reset.
B0 and Subsequent Steppings Only
Install only for special debug or testing purposes
Receiver inputs should be AC coupled from transmitter source (not shown) per PCIEX spec.
Route as differential pairs. Trace lengths should be equal within 0.005". For a pair.
If the 82571EB is to support aux wake R50 must be installed.
PCI-EX Reset Generated by Platform
LAN POWER GOOD: See Design Guide. Do not connect anything to this pin.
Connect to GP port pins on Super IO that retain value during reset. Normally not connected. See design guide for details.
These pins are reserved. Pull-ups are required as these pins define test modes in other states. These can be tied to 0Ω2 part (per pin) or a Rpack. Do not use a single resistor for all pins.
See Design Guide for FLB functionality.
PCI Express Transmitter differential pairs from the system board.
SIZE C
DWG. NO.
REV T
SCALE
DATE 1/21/2008
SHEET 05

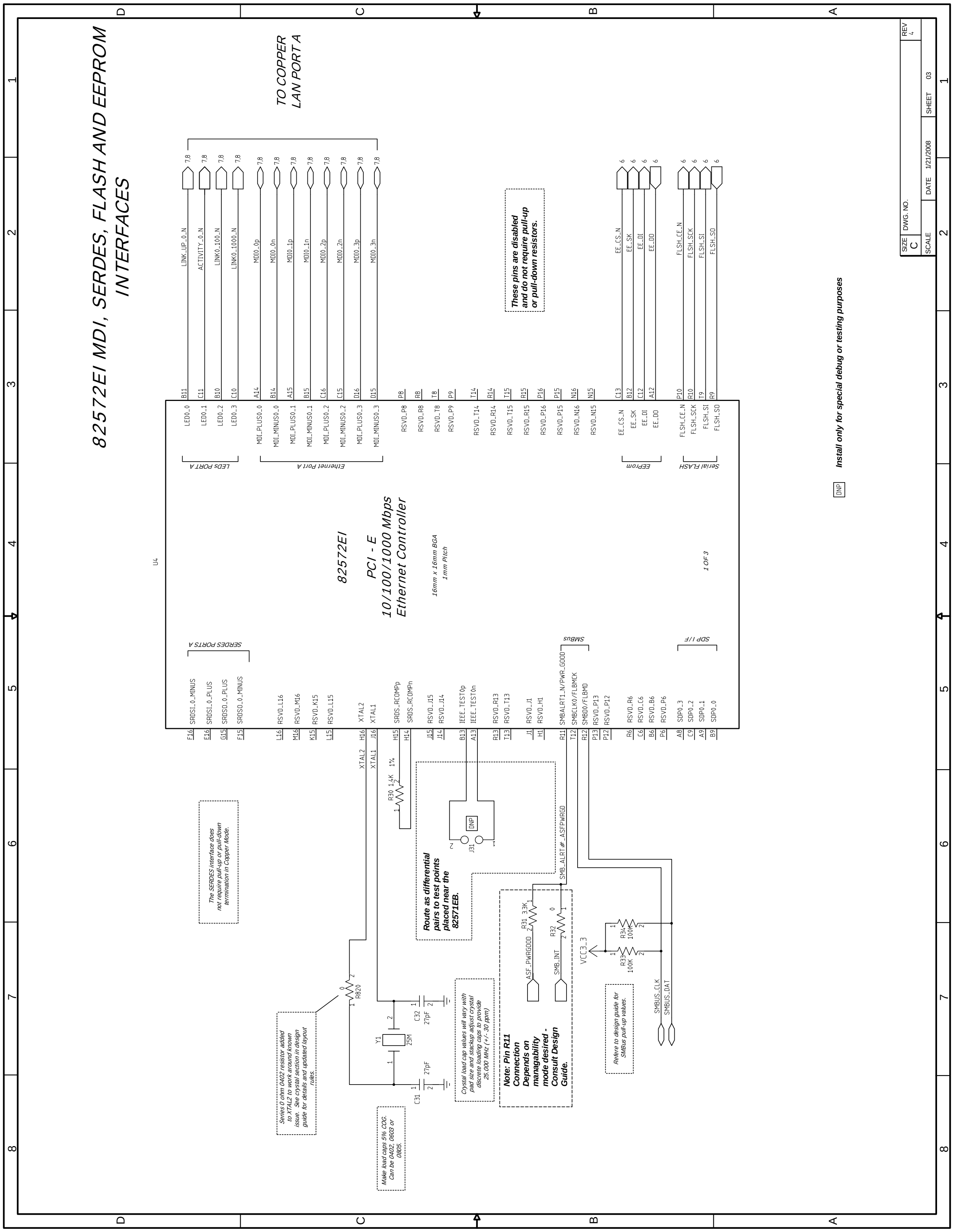

FLASH AND EEPROM
SPI EEPROM
Serial FLASH
Flash optional
DECOUPLING
Optional caps:
Place close to silicon as possible
OR place on secondary side
directly on the BGA power pins.
DNP unless needed.
Bypass Caps for 1.8V VDD
Place Close To LAN silicon
Bypass Caps for 1.1V COREVDD
Place Close To LAN silicon
SIZE C
DWG. NO.
REV 7
SCALE
DATE 1/21/2008
SHEET 06


OPTION A: SERDES/LASER CONNECTION
SERDES PORT A
SERDES PORT B
VCC3_3
Place close to Transceiver
FB70
FB71
FB72
FB73
600 ohms
0.2A
25%
C70 470pF
C71 0.1uF
C72 470pF
C73 0.1uF
C74 470pF
C75 0.1uF
C76 470pF
C77 0.1uF
SERDES_TX_Dp
SERDES_TX_Dn
SERDES_RX_Dp
SERDES_RX_Dn
SIGDET_OPTA
SIGDET_OPTB
TX_DISABLE_A
TX_DISABLE_B
R70 100K
R71 100K
CGND
JA1
JA2
LC - Optical Transceiver
TX_Vcc
RX_Vcc
RX_GND
TX_GND
TX_Data+
TX_Data-
RX_Data+
RX_Data-
RX_SDetect
TX_Disable
Ground_Tab_01
Ground_Tab_02
Ground_Tab_03
Ground_Tab_04
Mount_Stud_01
Mount_Stud_02
MS1
MS2
Place filter as close as possible to laser.
Place smallest valued caps closest to laser VCC.
SIZE C
DWG. NO.
REV 7
SCALE
DATE 1/21/2009
SHEET 07

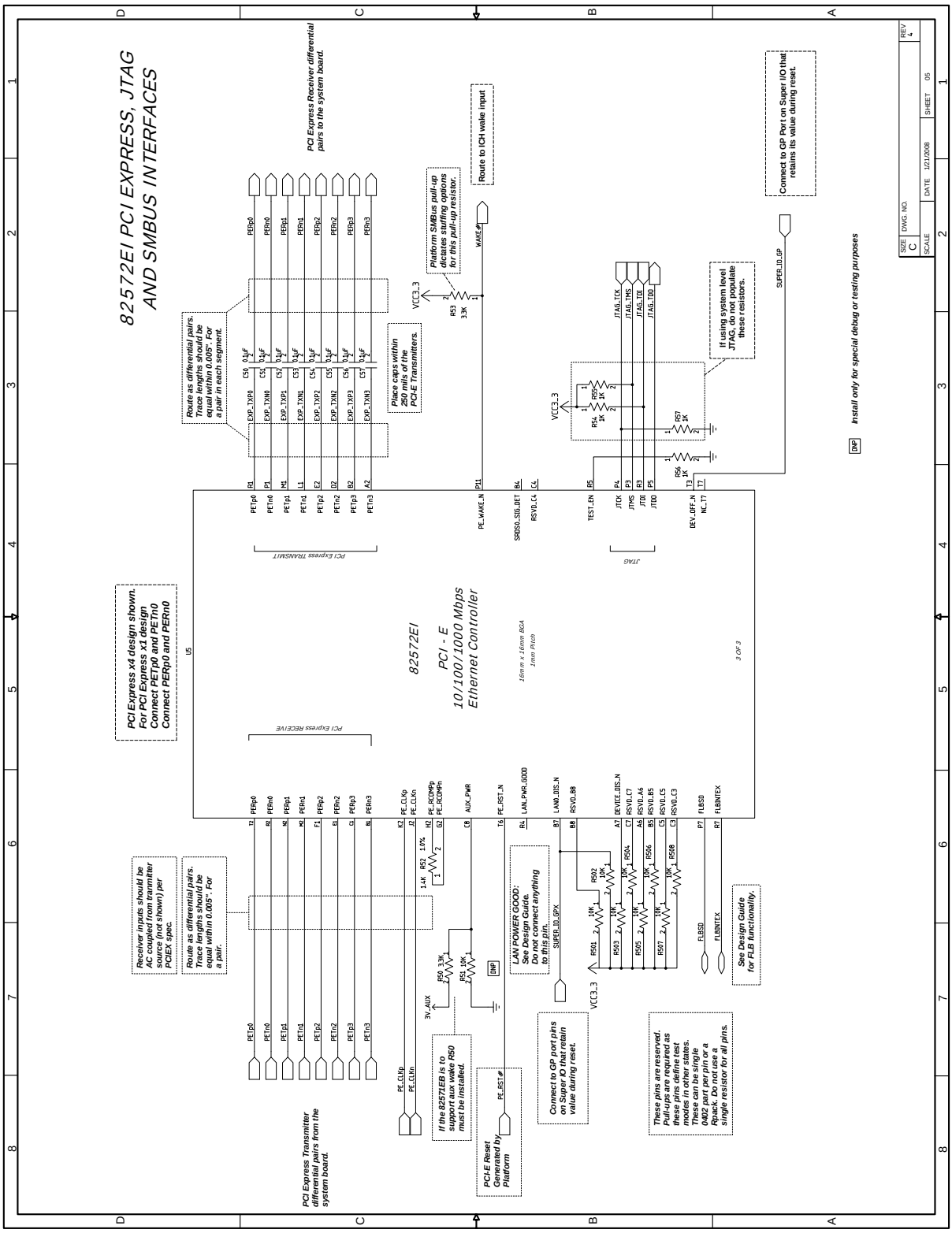

OPTION B: SERDES BACKPLANE CONNECTION
Backplane Connector
(Generic)
J33
SERDES PORT A
SERDES PORT B
SERDES_TX_Dp
SERDES_TX_Dn
SERDES_RX_Dp
SERDES_RX_Dn
SERDES_TX_Ip
SERDES_TX_In
SERDES_RX_Ip
SERDES_RX_In
10n
CB2
CB3
CB0
CB1
700000-P90
SIZE
C
DWG. NO.
REV
7
SCALE
DATE
1/21/2008
SHEET
08

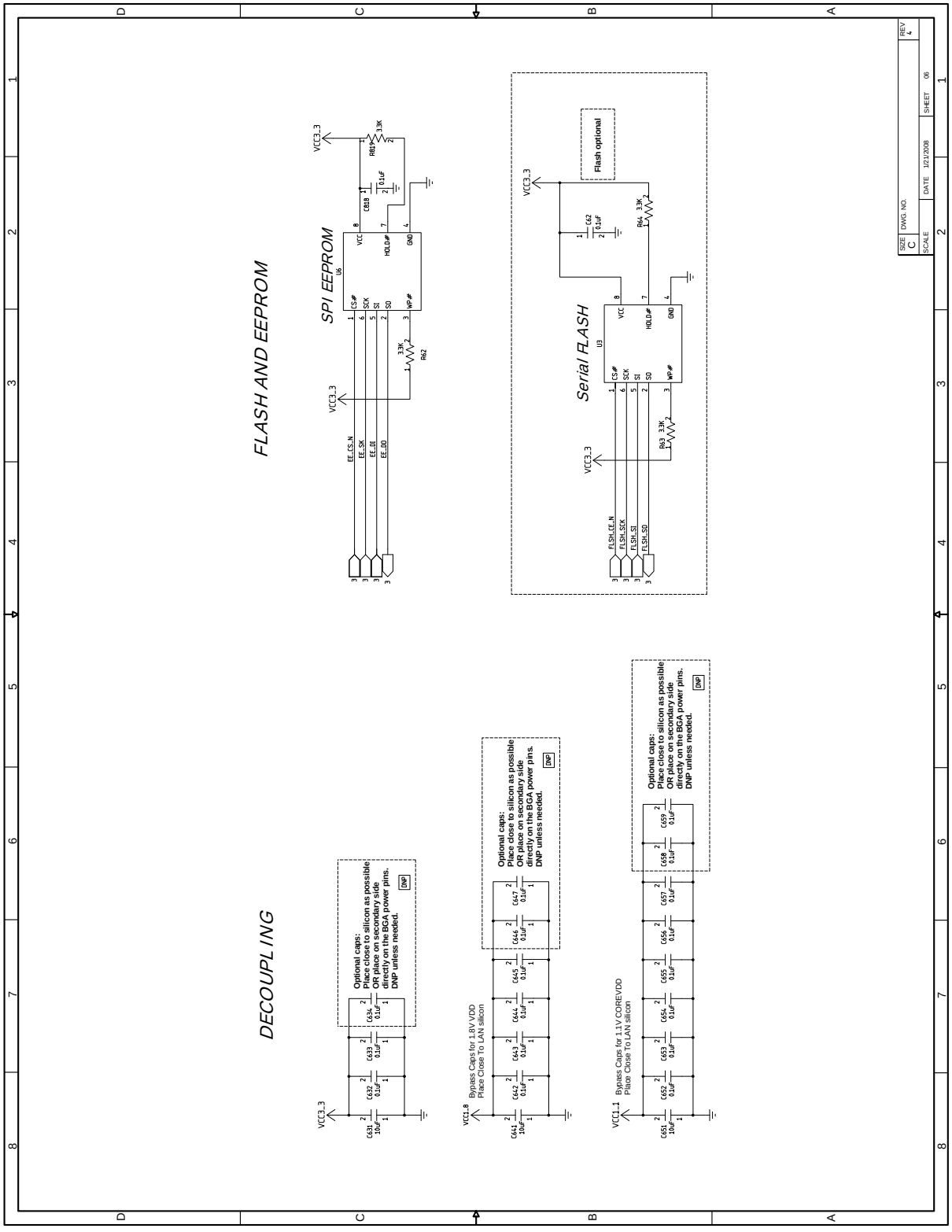

82572EI
REFERENCE DESIGN
(Copper)
Rev. 5.0
01/2008
PAGE INDEX
1 - Title Page
2 - Functional Blocks
3 - 82572EI MDI, SERDES, EEprom and Flash Interfaces.
4 - 82572EI VCC, VDD and VSS Connections.
5 - 82572EI PCI Express JTAG and SMBus interfaces.
6 - FLASH and EEPROM devices.
7. - AFE Option A Magjack W/USB.
8. - AFE Option B Discrete.
For power delivery solutions refer to the
"82571EB/82572EI Gigabit Ethernet Controller Design Guide"
Application Note (AP-447)
DNP
DNP - Do Not Populate symbol.
This is a component stuffing option for
an optional feature, special debug or
testing purposes.
intel
2111 N. E. 25th Avenue
Hillsboro, OR 97124-5961
TITLE
82572EI Reference Design
SIZE
C
DWG. NO.
REV
SCALE
DATE
1/21/2008
SHEET
01

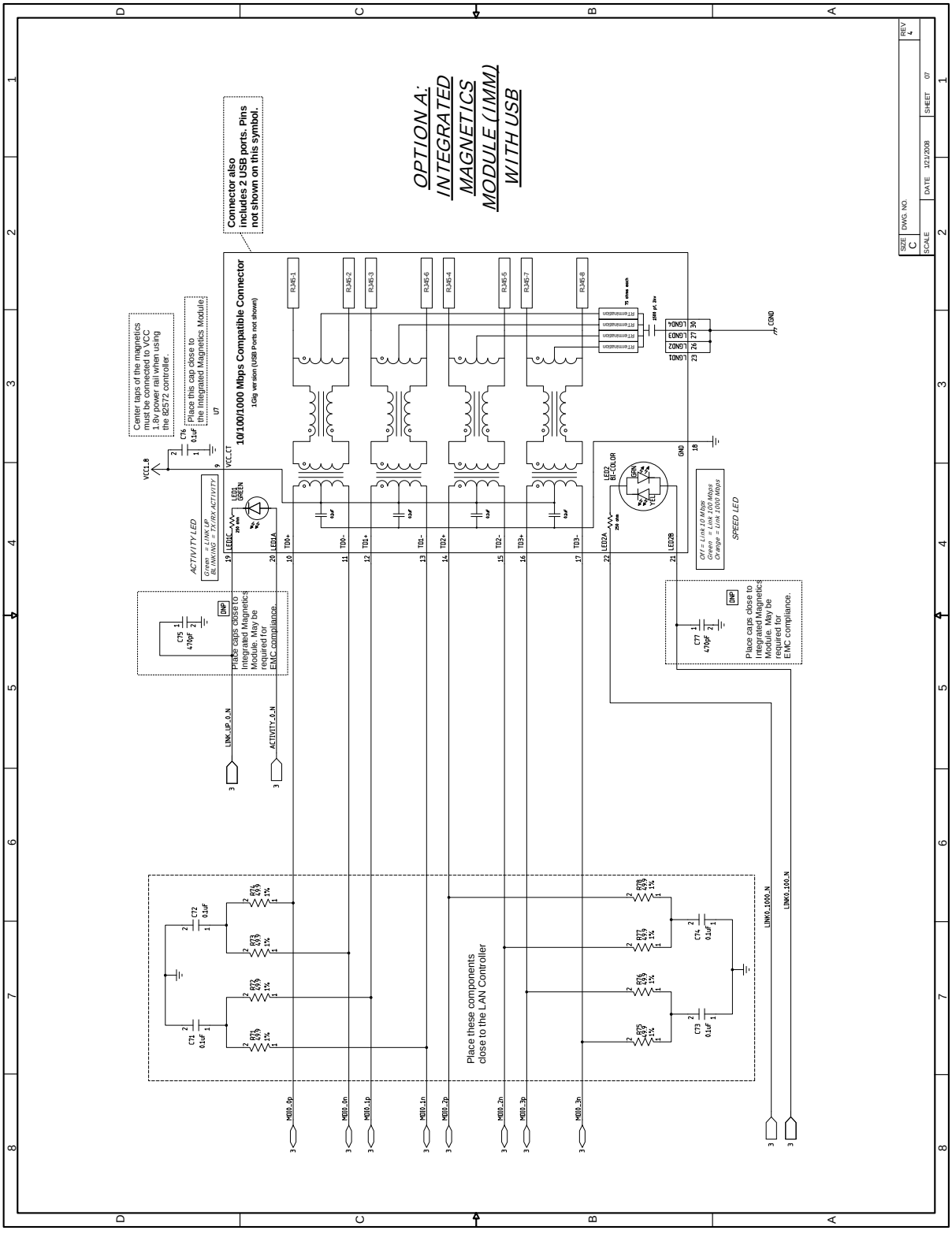

Functional Block
SERDES
Not shown for Copper Design
82572EI
LAN
CONTROLLER
Pages 3,4,5
COPPER AFE
Port A
Pages 7 - 8
Option A Integrated Magnetics Module W/USB.
Option B Discrete Magnetics.
JTAG
Page 5
PCI-Express - x4
Pages 5
SPI
EEPROM
Page 6
SPI
FLASH
Page 6
SMBus / FML
Pages 3
SIZE
C
DWG. NO.
REV
4
SCALE
DATE
1/21/2008
SHEET
02

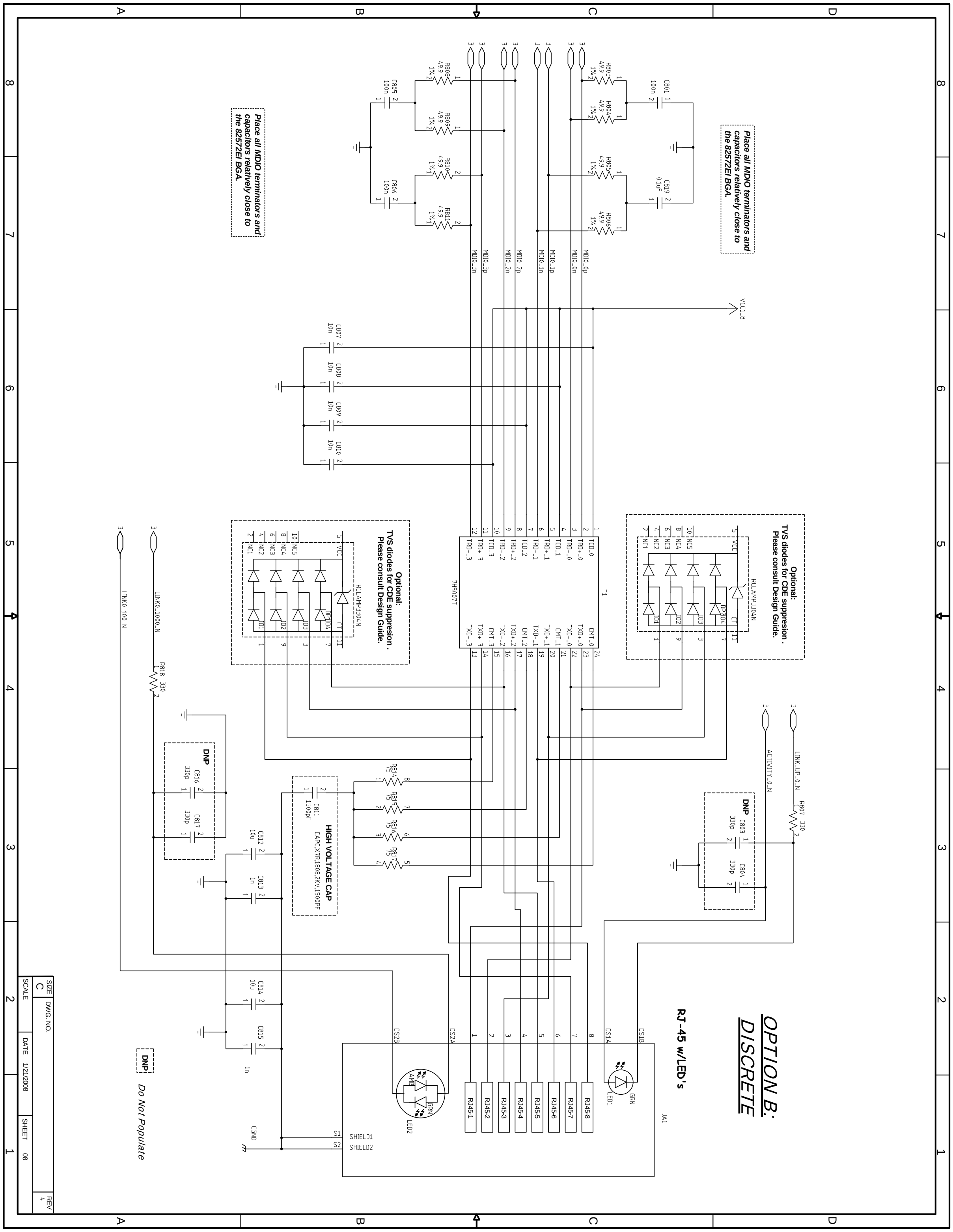

82572EI MDI, SERDES, FLASH AND EEPROM INTERFACES
TO COPPER LAN PORT A
82572EI
PCI - E
10/100/1000 Mbps
Ethernet Controller
16mm x 16mm BGA
1mm Pitch
1 OF 3
These pins are disabled and do not require pull-up or pull-down resistors.
Install only for special debug or testing purposes
The SERDES interface does not require pull-up or pull-down termination in Copper Mode.
Route as differential pairs to test points placed near the 82571EB.
Note: Pin R11 Connection Depends on managability mode desired - Consult Design Guide.
Refere to design guide for SMBus pull-up values.
Series 0 ohm 0402 resistor added to XTAL2 to work around known issue. See crystal section in design guide for details and updated layout rules.
Crystal load cap values will vary with XTAL size and stackup adjust crystal discrete loading caps to provide 25.000 MHz (+/- 30 ppm)
Make load caps 5% COG. Can be 0402, 0603 or 0805.

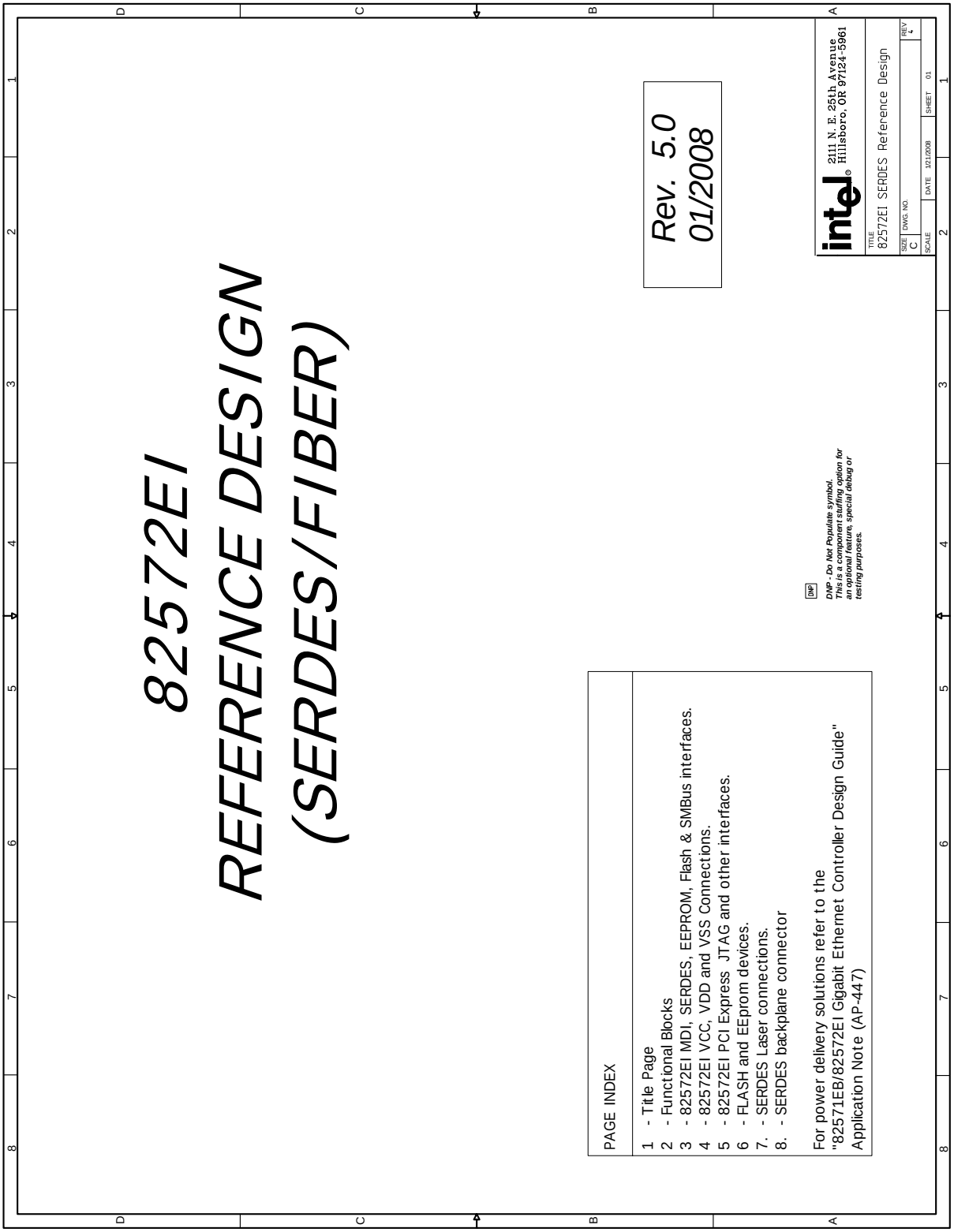

82572EI VCC, VDD & VSS CONNECTIONS
NOTE: Power delivery for 82572EI. The 1.1V and 1.8V supplies must be separate supplies for the Ethernet Controller only. Consult Design Guide.
Do NOT Use
RSV0-05
RSV0-04
VCC1.1
VCC3.3
VCC1.8
VCC1.1
VCC3.3
VDD/VCC Pins
VSS Pins
82572EI
PCI-E
10/100/1000 Mbps
Ethernet Controller
16mm x 16mm BGA
1mm Pitch
2 of 3
U5
THERM_Dn
THERM_Dp
RBIAS0p
RBIAS0n
1.4K
1%
SIZE
C
DWG. NO.
REV
4
SCALE
DATE
10/1/2008
SHEET
04

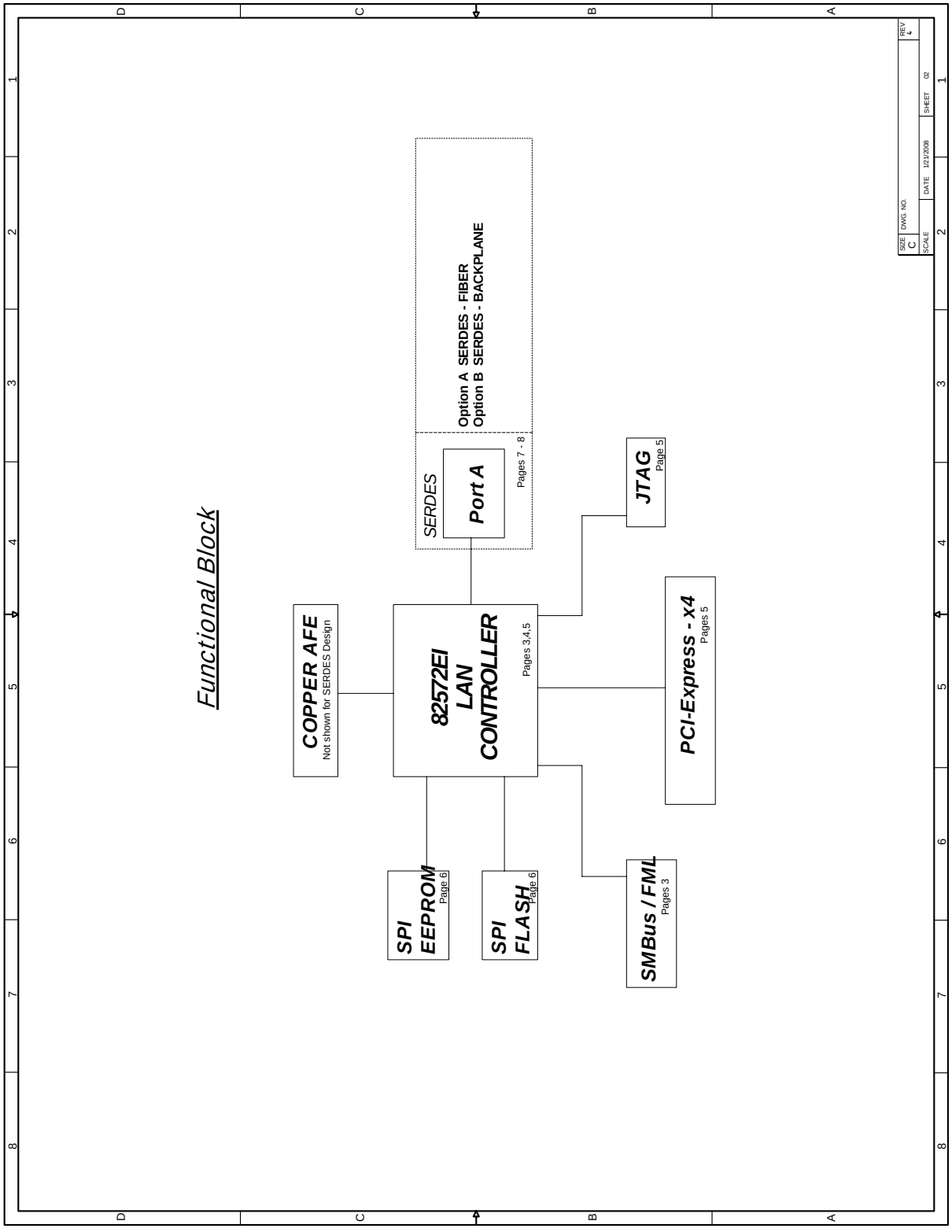

82572EI PCI EXPRESS, JTAG
AND SMBUS INTERFACES
PCI Express x4 design shown.
For PCI Express x1 design
Connect PETp0 and PETn0
Connect PERp0 and PERn0
Receiver inputs should be AC coupled to transmitter source (not shown) per PCIEX spec.
Route as differential pairs. Trace lengths should be equal within 0.005". For a pair.
PCI Express Transmitter differential pairs from the system board.
PCI Express Receiver differential pairs to the system board.
Route as differential pairs. Trace lengths should be equal within 0.005". For a pair in each segment.
Place caps within 250 mils of the PCIE Transmitters.
Platform SMBus pull-up dictates stuffing options for this pull-up resistor.
Route to ICH wake input
Connect to GP Port on Super I/O that retains its value during reset.
If using system level JTAG, do not populate these resistors.
Install only for special debug or testing purposes
If the 82571EB is to support aux wake R50 must be installed.
PCI-E Reset Generated by Platform
LAN POWER GOOD: See Design Guide. Do not connect anything to this pin.
Connect to GP port pins on Super IO that retain value during reset.
These pins are reserved. Pull-ups are required as these pins define test modes in other states. These can be single 0402 part per pin or a Rpack. Do not use a single resistor for all pins.
See Design Guide for FLB functionality.
82572EI
PCI - E
10/100/1000 Mbps
Ethernet Controller
16mm x 16mm BGA
1mm Pitch
3 OF 3
PCI Express RECEIVE
PCI Express TRANSMIT
JTAG
SIZE C
DWG. NO.
REV 4
SCALE
DATE 1/21/2008
SHEET 05

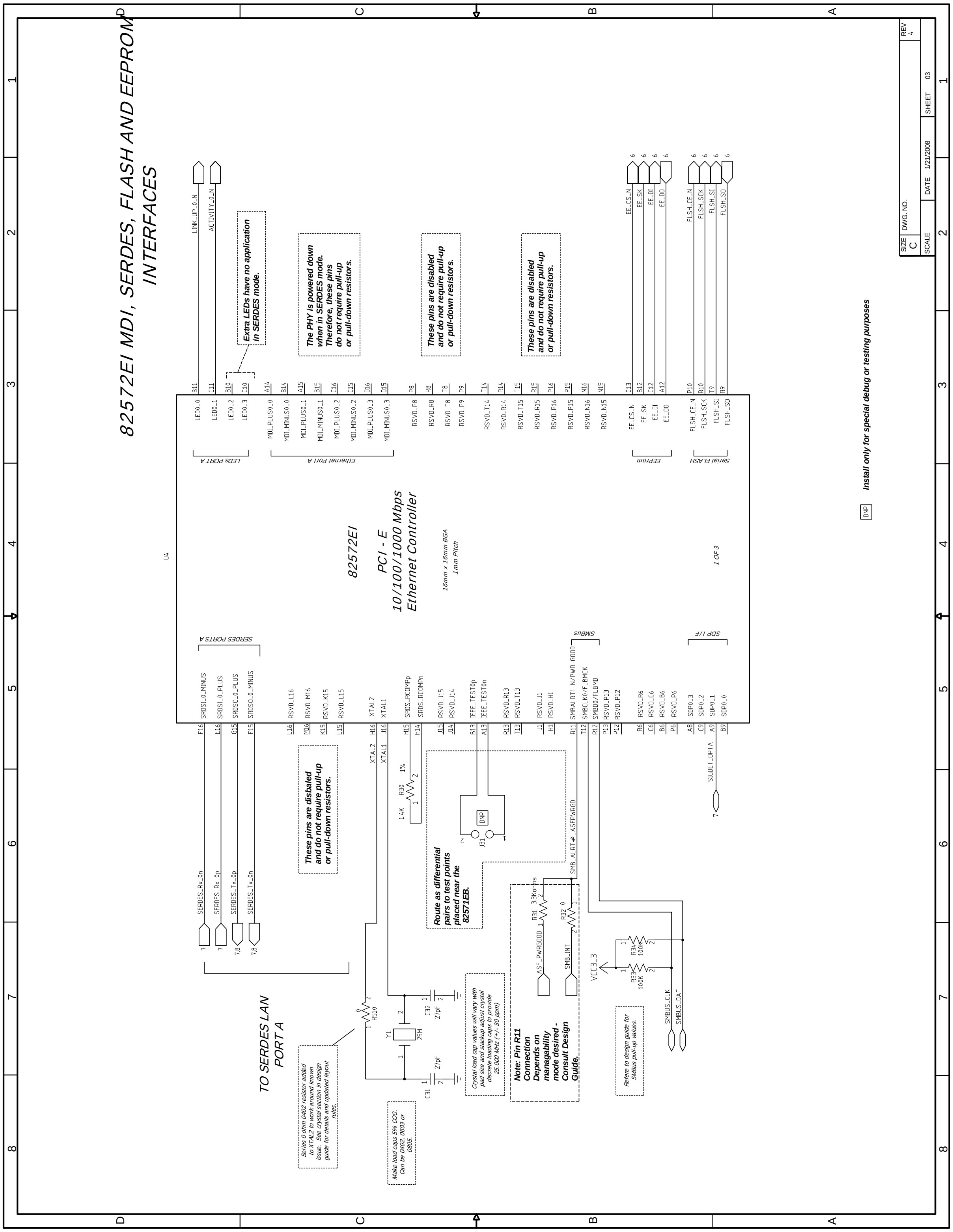

FLASH AND EEPROM
SPI EEPROM
Serial FLASH
Flash optional
DECOUPLING
Optional caps:
Place close to silicon as possible
OR place on secondary side
directly on the BGA power pins.
DNP unless needed.
Bypass Caps for 1.8V VDD
Place Close To LAN silicon
Bypass Caps for 1.1V COREVDD
Place Close To LAN silicon
SIZE C
DWG. NO.
REV A
SCALE
DATE 1/21/2008
SHEET 8

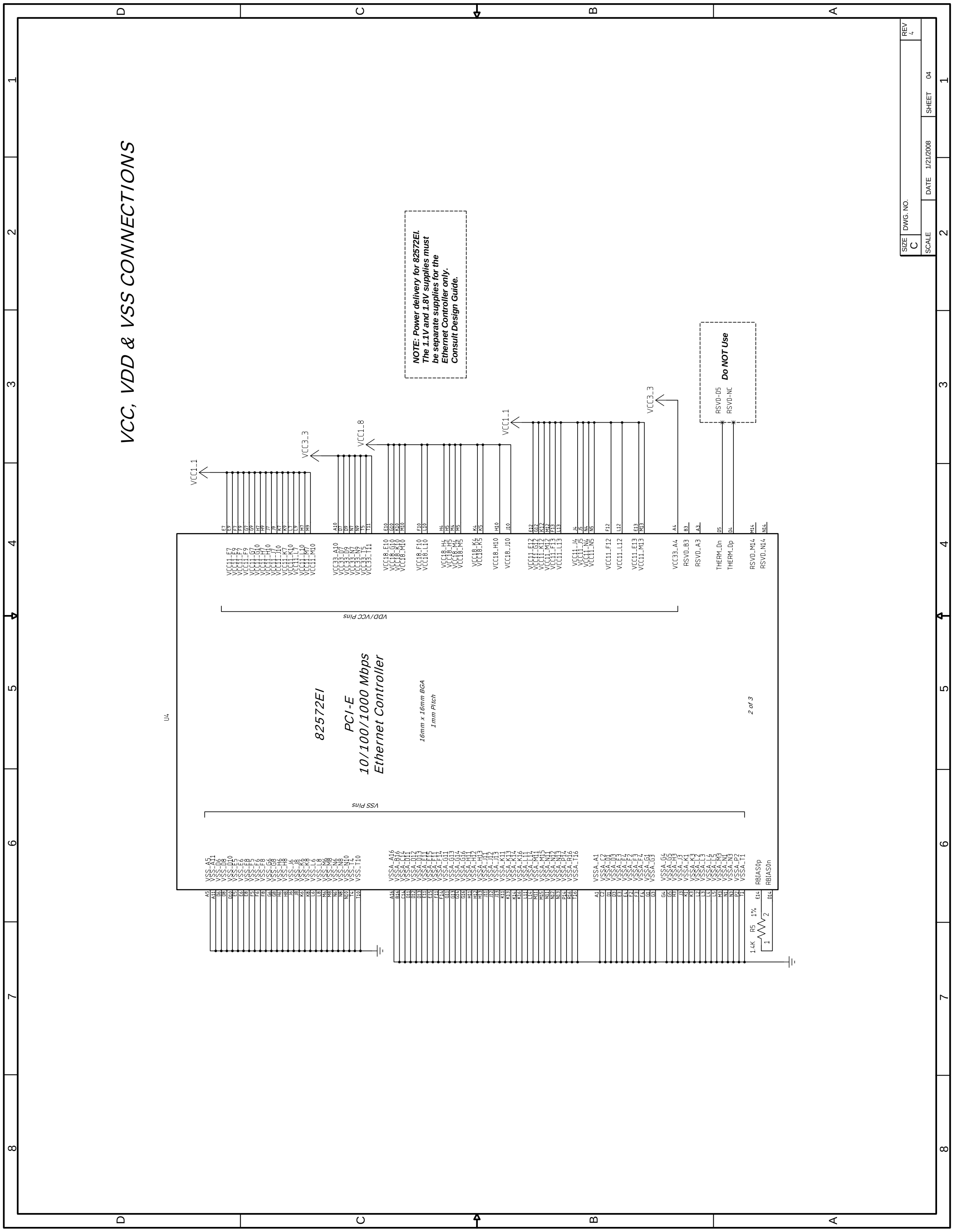

OPTION A:
INTEGRATED
MAGNETICS
MODULE (IMM)
WITH USB
10/100/1000 Mbps Compatible Connector
1Gig version (USB Ports not shown)
Connector also includes 2 USB ports. Pins not shown on this symbol.
Center taps of the magnetics must be connected to VCC through a capacitor using the 82572 controller.
Place this cap close to the Integrated Magnetics Module.
Place caps close to Integrated Magnetics Module. May be required for EMC compliance.
Place these components close to the LAN Controller
ACTIVITY LED
SPEED LED
Green = LINK up
Blinking = TX/RX ACTIVITY
Off = Link 10 Mbps
Green = Link 100 Mbps
Orange = 1000 Mbps
SIZE C
DWG. NO.
REV 4
SCALE
DATE 1/21/2009
SHEET 07

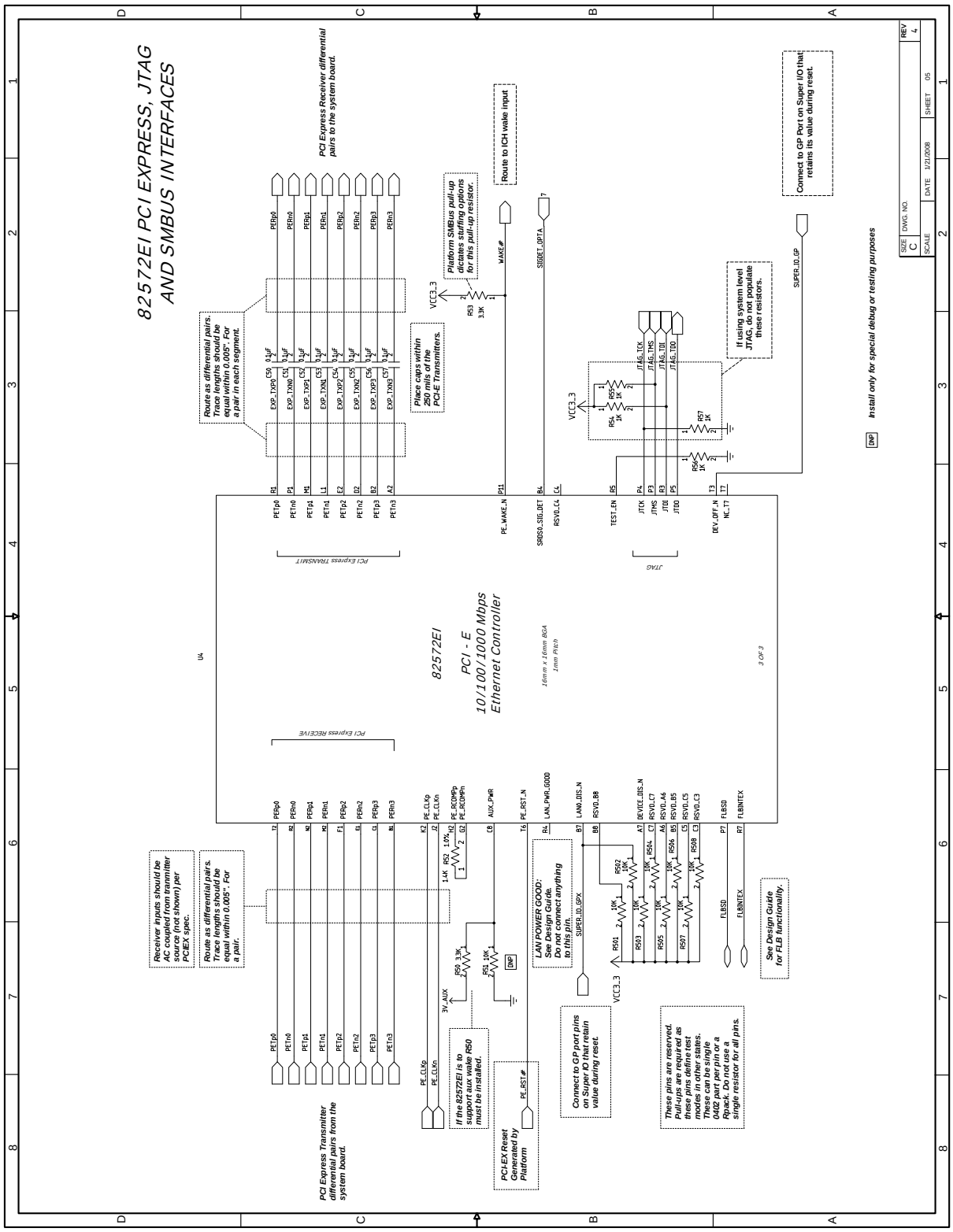

OPTION B:
DISCRETE
RJ-45 w/LED's
Place all MDIO terminators and capacitors relatively close to the 82572EI BGA.
Optional:
TVS diodes for CDE suppresion.
Please consult Design Guide.
HIGH VOLTAGE CAP
DNP
Do Not Populate
VCC1_8
LINK_UP_0_N
ACTIVITY_0_N
LINK0_1000_N
LINK0_100_N

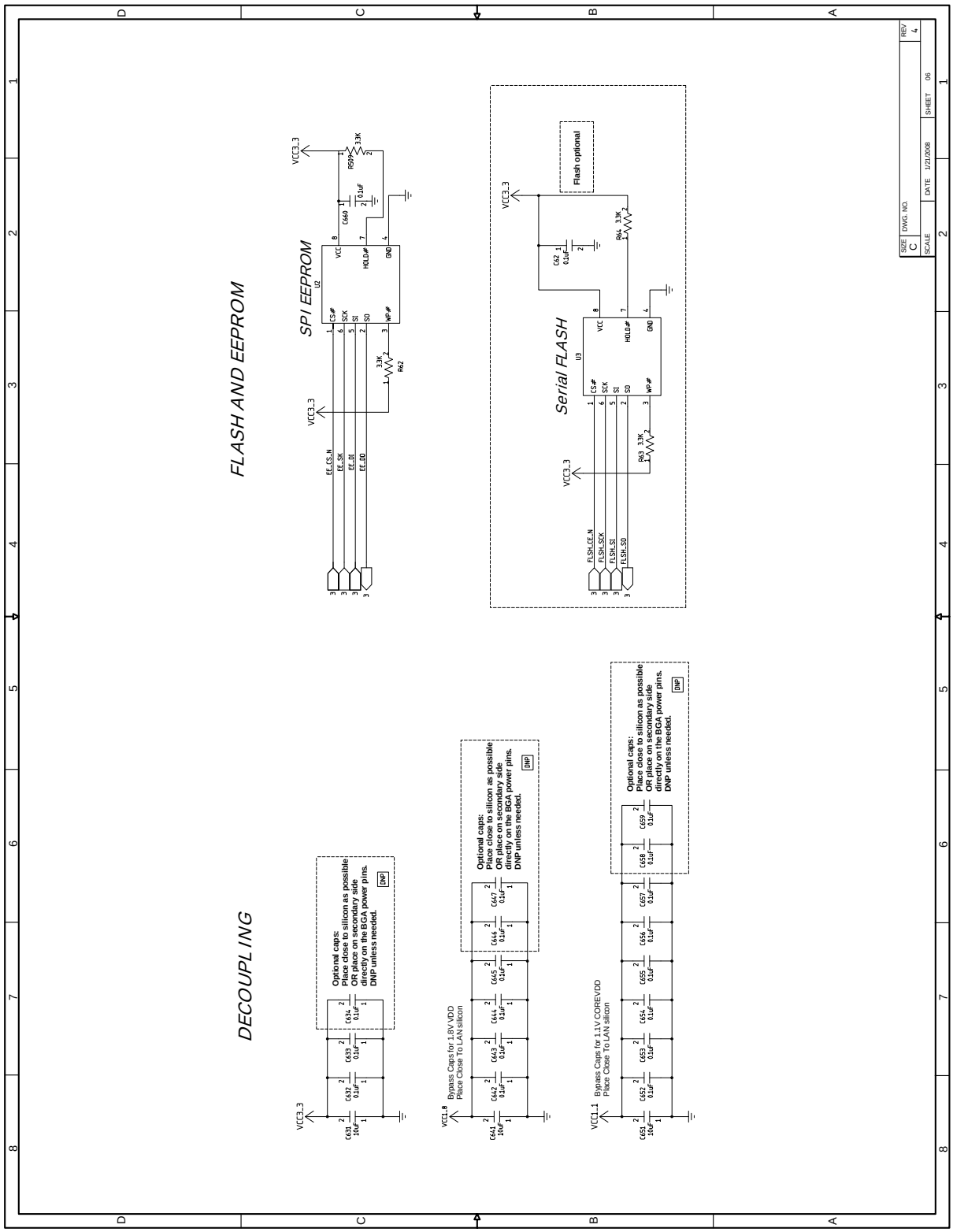

82572EI
REFERENCE DESIGN
(SERDES/FIBER)
Rev. 5.0
01/2008
PAGE INDEX
1 - Title Page
2 - Functional Blocks
3 - 82572EI MDI, SERDES, EEPROM, Flash & SMBus interfaces.
4 - 82572EI VCC, VDD and VSS Connections.
5 - 82572EI PCI Express JTAG and other interfaces.
6 - FLASH and EEprom devices.
7. - SERDES Laser connections.
8. - SERDES backplane connector
For power delivery solutions refer to the
"82571EB/82572EI Gigabit Ethernet Controller Design Guide"
Application Note (AP-447)
DNP
DNP - Do Not Populate symbol.
This is a component stuffing option for
an optional feature, special debug or
testing purposes.
intel
2111 N. E. 25th Avenue
Hillsboro, OR 97124-5961
TITLE
82572EI SERDES Reference Design
SIZE C
DWG. NO.
REV 4
SCALE
DATE 1/21/2008
SHEET 01

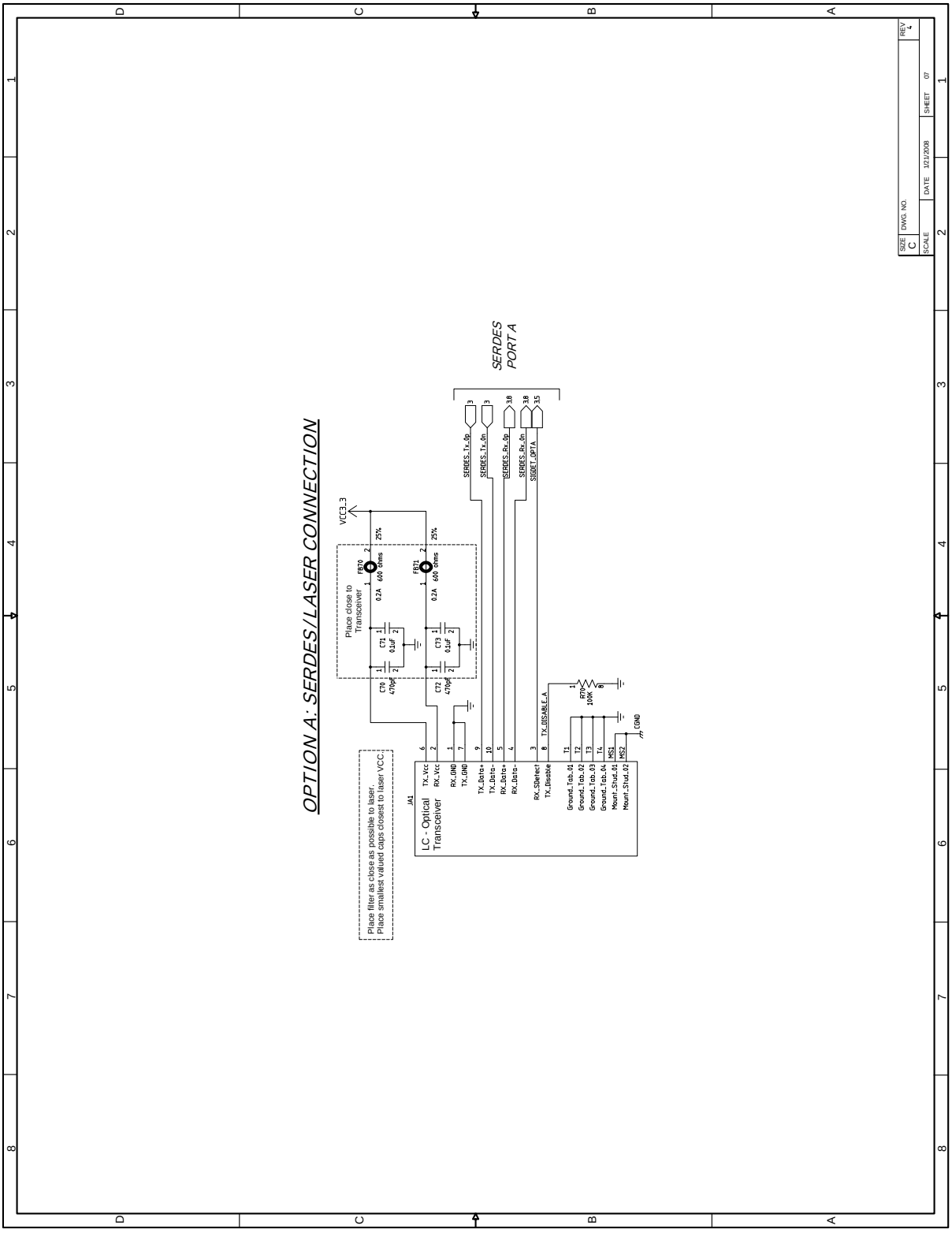

Functional Block
COPPER AFE
Not shown for SERDES Design
82572EI
LAN
CONTROLLER
Pages 3,4,5
SERDES
Port A
Pages 7 - 8
Option A SERDES - FIBER
Option B SERDES - BACKPLANE
JTAG
Page 5
PCI-Express - x4
Pages 5
SPI
EEPROM
Page 6
SPI
FLASH
Page 6
SMBus / FML
Pages 3
SIZE
C
DWG. NO.
REV
4
SCALE
DATE
1/21/2008
SHEET
02

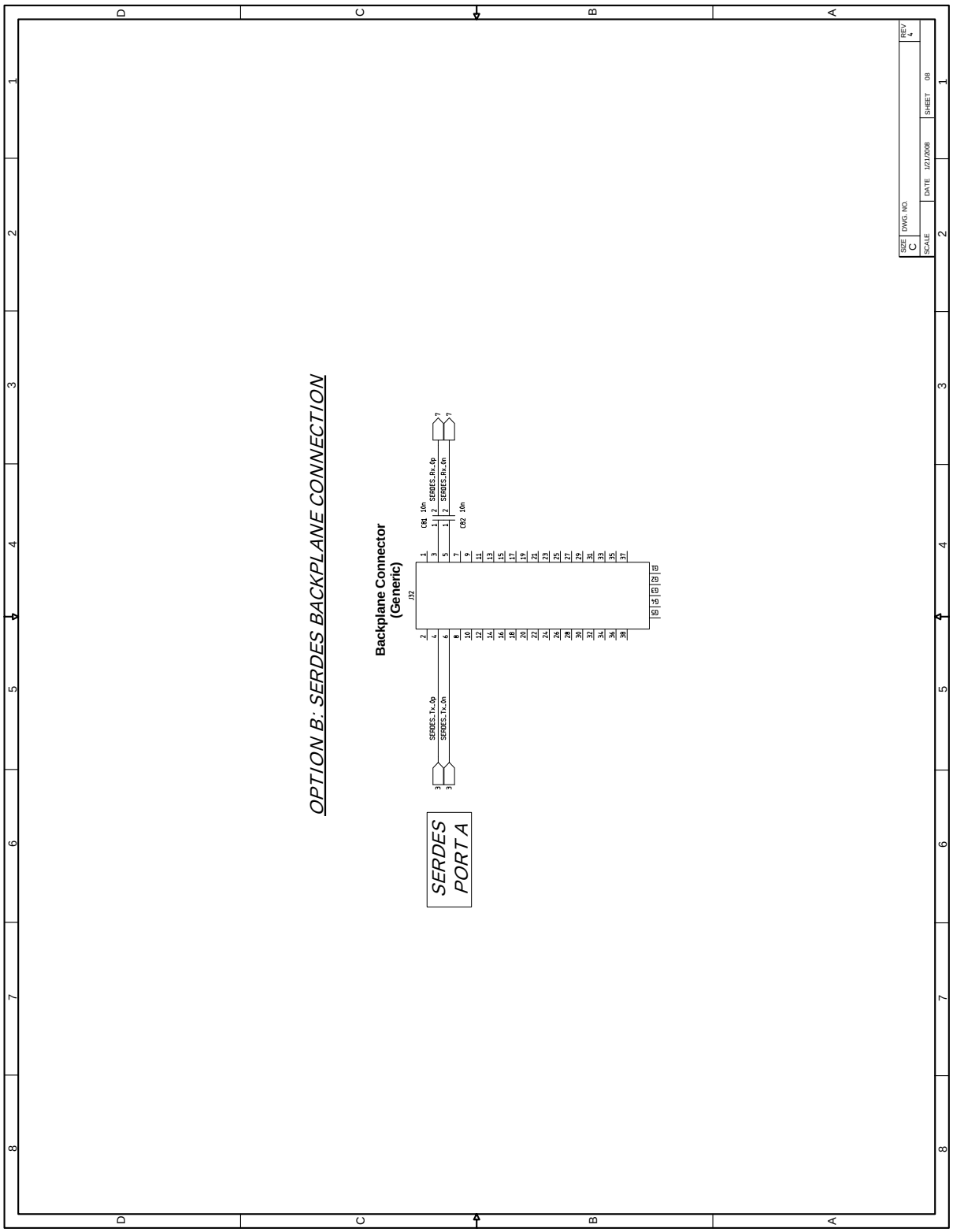

82572EI MDI, SERDES, FLASH AND EEPROM INTERFACES
82572EI
PCI - E
10/100/1000 Mbps
Ethernet Controller
16mm x 16mm BGA
1mm Pitch
TO SERDES LAN PORT A
Extra LEDs have no application in SERDES mode.
The PHY is powered down when in SERDES mode. Therefore, these pins do not require pull-up or pull-down resistors.
These pins are disabled and do not require pull-up or pull-down resistors.
These pins are disabled and do not require pull-up or pull-down resistors.
These pins are disbaled and do not require pull-up or pull-down resistors.
Route as differential pairs to test points placed near the 82571EB.
Note: Pin R11 Connection Depends on managability mode desired - Consult Design Guide.
Install only for special debug or testing purposes


VCC, VDD & VSS CONNECTIONS
NOTE: Power delivery for 82572EI.
The 1.1V and 1.8V supplies must
be separate supplies for the
Ethernet Controller only.
Consult Design Guide.
Do NOT Use
82572EI
PCI-E
10/100/1000 Mbps
Ethernet Controller
16mm x 16mm BGA
1mm Pitch
2 of 3
VDD/VCC Pins
VSS Pins
VCC1.1
VCC3.3
VCC1.8
U4
SIZE C
DWG. NO.
REV 4
SCALE
DATE 1/21/2008
SHEET 04


82572EI PCI EXPRESS, JTAG AND SMBUS INTERFACES
82572EI
PCI - E
10/100/1000 Mbps
Ethernet Controller
PCI Express Receiver differential pairs to the system board.
Route as differential pairs. Trace lengths should be equal within 0.005". For a pair in each segment.
Place caps within 250 mils of the PCI-E Transmitters.
Platform SMBus pull-up dictates stuffing options for this pull-up resistor.
Route to ICH wake input
If using system level JTAG, do not populate these resistors.
Connect to GP Port on Super I/O that retains its value during reset.
Install only for special debug or testing purposes
Receiver inputs should be AC coupled from tranmitter source (not shown) per PCIEX spec.
Route as differential pairs. Trace lengths should be equal within 0.005". For a pair.
PCI Express Transmitter differential pairs from the system board.
If the 82572EI is to support aux wake R50 must be installed.
PCI-EX Reset Generated by Platform
Connect to GP port pins on Super IO that retain value during reset.
LAN POWER GOOD: See Design Guide. Do not connect anything to this pin.
These pins are reserved. Pull-ups are required as these pins are latched in other modes for other states. These can be single 0402 part per pin or a Rpack. Do not use a single resistor for all pins.
See Design Guide for FLB functionality.
PCI Express TRANSMIT
PCI Express RECEIVE
JTAG
SIZE C
DWG. NO
REV 4
SCALE
DATE 1/21/2009
SHEET 05


FLASH AND EEPROM
SPI EEPROM
Serial FLASH
Flash optional
DECOUPLING
Optional caps:
Place close to silicon as possible
OR place on secondary side
directly on the BGA power pins.
DNP unless needed.
Bypass Caps for 1.8V VDD
Place close to LAN silicon
Bypass Caps for 1.1V COREVDD
Place Close To LAN silicon
SIZE
C
DWG. NO.
REV
4
SCALE
DATE
1/21/2008
SHEET
06


OPTION A: SERDES/LASER CONNECTION
SERDES PORT A
SERDES_Tx_dp
SERDES_Tx_dn
SERDES_Rx_dp
SERDES_Rx_dn
SSDET_OPTA
VCC3_3
Place close to Transceiver
FB70
FB71
600 ohms
0.2A
C70
C71
C72
C73
470pF
0.1uF
25%
JA1
LC - Optical Transceiver
TX_Vcc
RX_Vcc
RX_GND
TX_GND
TX_Data+
TX_Data-
RX_Data+
RX_Data-
RX_SDetect
TX_Disable
TX_DISABLE_A
R70
10K
Ground_Tab_01
Ground_Tab_02
Ground_Tab_03
Ground_Tab_04
Mount_Stud_01
Mount_Stud_02
MHS1
MHS2
CGND
Place filter as close as possible to laser.
Place smallest valued caps closest to laser VCC.
SIZE
C
DWG. NO.
REV
4
SCALE
DATE
1/21/2009
SHEET
07


OPTION B: SERDES BACKPLANE CONNECTION
Backplane Connector
(Generic)
J32
SERDES PORT A
SERDES_Tx_Dp
SERDES_Tx_Dn
SERDES_Rx_Dp
SERDES_Rx_Dn
CB1 10n
CB2 10n
SIZE C
DWG. NO.
SCALE
DATE 1/21/2008
SHEET 08
REV A