82563EB/82564EB LAN on Motherboard Design Guide

Application Note

May 2007

317104-001
Revision 2.6

Revision History

Revision	Revision Date	Description
2.6	May 2007	• Updated Exposed Pad* landing pattern options.
2.5	May 2006	• Initial public release.
2.0	Nov 2005	• Intel confidential release.
1.75	July 2005	• Added a third magnetics module to Table 3. • Changed power supply references from 1.8V to 1.9V. • Changed crystal load capacitance parameter from 20 pF to 27 pF.
1.5	April 2005	• Updated crystal specifications. • Added Bill of Materials (BOM) information.
1.0	Dec 2004	Major edits (including but not limited to), added landing pattern; added pointer to BSDL file; added pointer to design checklists; adding pointer to reference schematics.
0.70	Aug 2004	Added power supply guidelines, crystal guidelines.
0.50	May 2004	Initial publication of preliminary design guide information.

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1.0 Introduction

The Intel 82563EB/82564EB Gigabit Platform LAN Connect device is a dual/single, compact component designed for 10/100/1000 Mbps operation. The Intel 82563EB/82564EB Gigabit Platform LAN Connect device enables dual/single port Gigabit Ethernet implementation in a very small area — easing routing constraints from the chipset to the PHY. Note that the 82564EB Gigabit Platform LAN Connect device is the single port implementation.

The Intel 82563EB/82564EB Gigabit Platform LAN Connect device provides a standard IEEE 802.3 Ethernet interface for 1000BASE-T, 100BASE-TX, and 10BASE-T applications (802.3, 802.3u, and 802.3ab).

The 82563EB/82564EB Gigabit Platform LAN Connect device is designed for high performance. The device connects directly to the Intel® 631xESB/632xESB I/O Controller Hub using the serial Kumeran interface.

The 82563EB/82564EB Gigabit Platform LAN Connect device is packaged in a 14 mm x 14 mm x 1.2 mm with 0.5 mm pitch leads, 100-pin TQFL with Exposed-Pad*. An Exposed-Pad* is a central pad on the bottom of the package that serves as a ground and thermal connection.

1.1 Scope

This application note contains Ethernet design guidelines applicable to 82563EB/82564EB LOM designs based on 631xESB/632xESB designs. All guidelines are applicable to both the 82563EB and 82564EB unless specifically specified.

Section 1 – introduction and reference documents

Section 2 – describes the bus interfaces specific to the 82563EB/82564EB device

Section 3 – discusses Ethernet design considerations

Section 4 – discusses attributes of various frequency control devices

Section 5 – describes methods for crystal validation

Section 6 – discusses frequency control alternatives to crystal

Section 7 – discusses Ethernet layout considerations

Section 8 – shows the landing pattern options

Section 9 – lists the Bill of Materials (BOM).

Section 10 – provides schematic, board layout and placement, and validation checklists.

Section 11 – provides link to reference schematics

Appendix A – discusses use of a frequency counter to measure LAN reference signal

Note: This document contains information on products in the design phase of development. Product features and specifications are subject to change without notice. Verify with your local Intel sales office that you have the latest information before finalizing a design.

1.2 Reference Documents

This application note assumes that the designer is acquainted with high-speed design and board layout techniques. The following documents provide additional information:

- *82563EB/82564EB Gigabit Ethernet Platform LAN Connect Network Silicon Datasheet*, Intel Corporation.
- *631xESB/632xESB I/O Controller Hub EEPROM Information Guide Application Note (AP-477)*, Intel Corporation.
- *82571/82572/631xESB/632xESB System Manageability Application Note* (AP-497), Intel Corporation.
- *82563EB/82564EB Gigabit Platform LAN Connect Specification Update and Sighting Information*, Intel Corporation.
- *IEEE Standard 802.3*, 2000 Edition. Institute of Electrical and Electronics Engineers (IEEE).
  - — Incorporates various IEEE standards previously published separately.
- *IEEE Standard 1149*.1, 2001 Edition (JTAG). Institute of Electrical and Electronics Engineers (IEEE).
- *PICMG3.1 Ethernet/Fiber Channel Over PICMG 3.0 Draft Specification*, September 4, 2002, Version 0.90. PCI Industrial Computer Manufacturers Group (PICMG).
- *Intel® 631xESB/632xESB I/O Controller Hub External Design Specification (EDS) - Volume 1-3*, Intel Corporation.
- *Bensley/Bensley-VS Platform Design Guide*, Intel Corporation.
- *Oscillation Circuit Design Guide* Application Note, Epson Electronics America, Inc.
- *Quartz Crystal Theory of Operation and Design Notes*. Fox Electronics.
- *Crystal Technical Glossary*. Fox Electronics.
- *Crystal Frequently Asked Questions*. Fox Electronics.
- *Resonator Terminology and Formulas*. Piezo Technology, Inc.

Note: Intel documentation is subject to frequent revision. Verify with your local Intel sales office that you have the latest information before finalizing a design

1.3 Product Codes

The following Table 1 lists the product ordering codes for the 82563EB dual port device and the 82564EB single port device.

Table 1. Product Ordering Codes

Device	Product Code
Dual Port (Leaded)	HU82563EB
Single Port (Leaded)	HU82564EB
Dual Port (Lead Free)	HY82563EB
Single Port (Lead Free)	HY82564EB

2.0 Kumeran Connection to 82563EB/82564EB Gigabit Platform LAN Connect

The Kumeran interface is a 4-pin (RXx_PLUS, RXx_MINUS, TXx_PLUS, TXx_MINUS, where the lower case ‘x’ represents port ‘A’ or port ‘B’, if using the dual device) differential interface for each Ethernet port based on PICMG 3.1 standard. The clock is embedded within the differential signals and runs at 1.25 Gbps. There is no need for the additional MDIO/MDC signals as the PHY management information is passed through in-band. Special encoded packets will carry the MDIO information.

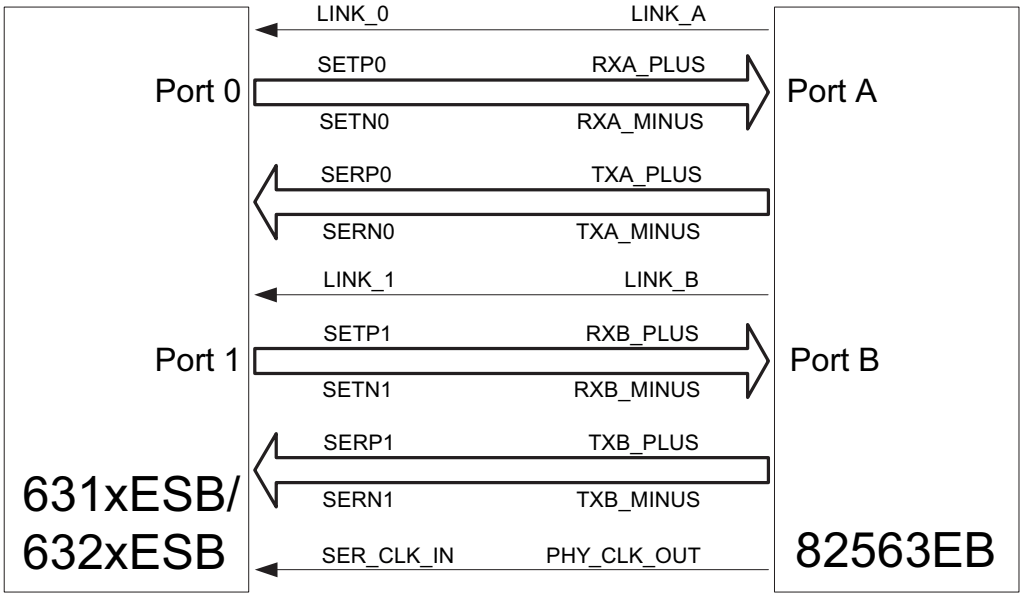
The Kumeran interface architecture in the PHY and in the MAC sides is symmetric.

In the TX side, the data is translated by the MAC to PCS order sets codes as described in 802.3 standard clause 36. The control data is inserted in the data flow and the data stream is serialized using 8b/10b encoding.

In the RX side, the clock is recovered from data stream and data is de-serialized. The 10 bits are translated to 8 bits by the PCS logic and the control data is removed from data flow.

The TX lane of the MAC side is responsible to insert Control & Status packets during data idle time. Theses packets include MDIO registers RD/WR access commands, power-saving commands or LED control. The RX lane of PHY side will remove these packets and transfer them to the PHY registers and LEDs.

The TX lane of the PHY side will insert the Control & Status packets with the response of registers RD/WR accesses or the twisted-pairs link status. The link status is sent automatically after link is changed, or after a constant time-out. The RX lane of MAC side will remove link status and registers access responses and update the MAC logic accordingly.



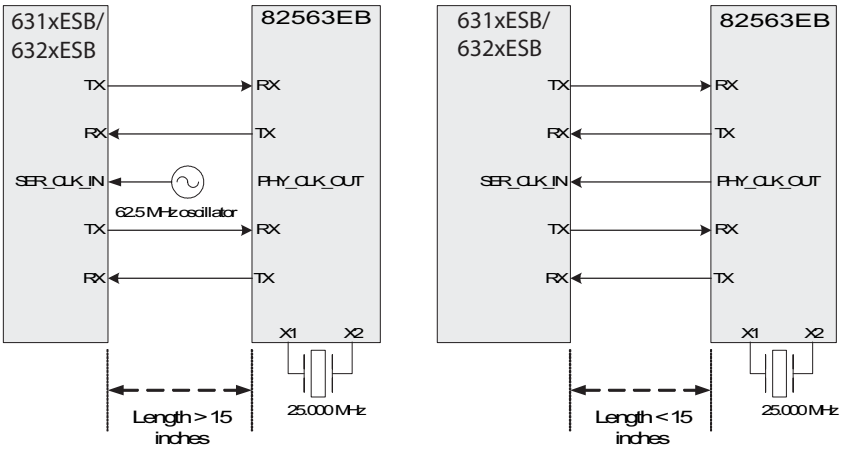
NOTE: 82564EB will only have Port 0 to Port A connections.

Figure 1. 82563EB/82564EB Connection to the 631xESB/632xESB

2.1 Kumeran Reference Clock

The 82563EB/82564EB Gigabit Ethernet Platform LAN Connect uses an embedded clock within the Kumeran differential signals to recover the data. This reference clock may be generated in one of two ways dependant on the length of the Kumeran interface board traces as shown in Figure 2.

Figure 2. 631xESB/632xESB Clock Source Diagrams



NOTE: Figure also reflects the same behavior in the single port 82564EB device.

If the length of the Kumeran board traces are 15 inches or less, then the 82563EB/82564EB uses its 25 MHz crystal and internal PLL to provide a 62.5 MHz clock to the 631xESB/632xESB. If the length of the Kumeran board traces are greater than 15 inches, an oscillator needs to be connected directly to the 631xESB/632xESB in addition to the 25 MHz crystal that is on the 82563EB/82564EB. In this case, the 82563EB/82564EB does not provide a direct reference clock to the 631xESB/632xESB. The oscillator at the 631xESB/632xESB is necessary due to the signal quality degradation as the routed distance is increased.

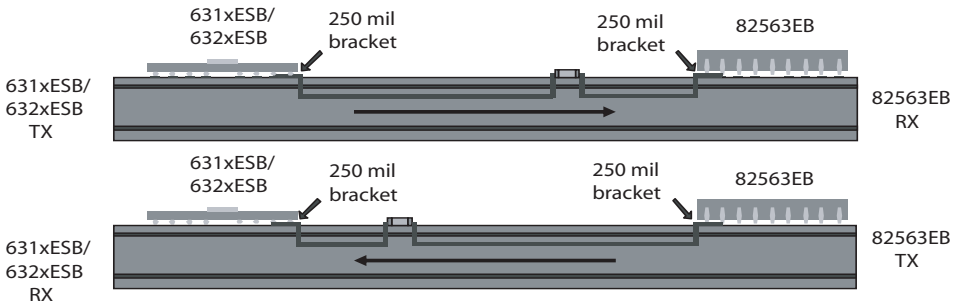
A 25 MHz crystal is required for the 82563EB/82564EB for both cases as seen in Table 2.

Table 2. Reference Clocks Required

Kumeran Length	25 MHz Crystal on the 82563EB/ 82564EB	62.5 MHz Oscillator on the 631xESB/632xESB
Less than or equal to 15 inches	Yes	No
More than 15 inches	Yes	Yes

2.2 631xESB/632xESB to 82563EB/82564EB Signals

The 82563EB/82564EB device implements signals such as the receive signals RXx_PLUS and RXx_MINUS, as well as the transmit signals TXx_PLUS and TXx_MINUS. Please note that documentation for 82563EB designates the two ports as A and B and the 631xESB/632xESB designates them as ports 0 and 1, respectively. Furthermore, unlike PCI-Express, there is no polarity correction; failure to match polarity correctly may result in a non-functional LAN solution. These four signals per port are AC-coupled and their respective capacitors (10 nF, type X7R, size 0402 or 0603) should be placed near the receiver side.



NOTE: Figure also reflects the same behavior in the single port 82564EB device.

Figure 3. AC Capacitor Placement

The Gigabit Ethernet Platform LAN Connect has the option to signal power management events to the system using:

- PHY_SLEEP signal, which will power down the PHY and the Kumeran interface
- PHY_RESET_N signal, which resets the PHY and Kumeran interface

Note: The above connection is *not recommended* for system designs — power management events will be passed in band via the Kumeran interface.

The PHY_PWR_GOOD signal indicates that stable power is available for all voltage rails that power the 82563EB/82564EB and that the device is ready to come out of an otherwise held reset. Typically, this connects to the system's RSM_RST# signal.

The PHY_CLK_OUT signal is the output clock available for use by the 631xESB/632xESB for Kumeran trace length less than or equal to 15 inches. For distances greater than 15 inches, a discrete oscillator needs to supply the reference clock to the 631xESB/632xESB directly via the SER_CLK_IN. To ensure signal integrity and feasibility of trace lengths a designer may want to do some simulations. If the Gigabit Ethernet Platform LAN Connect is supplying the clock to the 631xESB/632xESB via PHY_CLK_OUT, the designer should place a 40 Ω series termination resistor near the PHY_CLK_OUT pin. This is needed in order to reduce ringing due to the strong driver and is required regardless of the length of the clock trace to the 631xESB/632xESB.

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3.0 Ethernet Component Design Guidelines

These sections provide recommendations for selecting components and connecting special pins. For 1000 BASE-T designs, the main design elements are the 631xESB/632xESB, 82563EB/82564EB Gigabit Ethernet Platform LAN Connect, an integrated magnetics module with RJ-45 connector, an EEPROM, and a clock source.

3.1 General Design Considerations for Ethernet Platform LAN Connect Devices

Follow good engineering practices with respect to unused inputs by terminating them with pull-up or pull-down resistors, unless the datasheet, design guide or reference schematic indicates otherwise. Do not attach pull-up or pull-down resistors to any balls identified as No Connect. These devices may have special test modes that could be entered unintentionally.

3.1.1 Clock Source

All designs require a 25 MHz clock source. The 82563EB/82564EB Gigabit Ethernet Platform LAN Connect uses the 25 MHz source to generate clocks up to 125 MHz and 1.25 GHz for the PHY circuits, and 1.25 GHz for the Kumeran interface. For optimum results with lowest cost, connect a 25 MHz parallel resonant crystal and appropriate load capacitors at the XTAL1 and XTAL2 leads. The frequency tolerance of the timing device should be *30 ppm* or better. Refer to the sections, “Frequency Control Device Design Considerations” and “Crystal Selection Parameters”, for more information on choosing crystals.

There are three steps to crystal qualification:

1. Verify that the vendor’s published specifications in the component datasheet meet the required conditions for frequency, frequency tolerance, temperature, oscillation mode and load capacitance as specified in the 82563EB/82564EB datasheet.
2. Independently measure the component’s electrical parameters in real systems. Measure frequency at a test output to avoid test probe loading effects at LEDA_RX_ACTIVITY_N for port A and LEDB_RX_ACTIVITY_N for port B. Check that the measured behavior is consistent from sample to sample and that measurements meet the published specifications. For crystals, it is also important to examine startup behavior while varying system voltage and temperature. Refer to Appendix A, “Measuring LAN Reference Frequency Using a Frequency Counter”.
3. Perform physical layer conformance testing and EMC (FCC and EN) testing in real systems.

3.1.2 Integrated Magnetics Module for 1000 BASE-T

The magnetics module has a critical effect on overall IEEE and emissions conformance. The device should meet the performance required for a design with reasonable margin to allow for manufacturing variation. Occasionally, components that meet basic specifications may cause the system to fail IEEE testing because of interactions with other components or the printed circuit board itself. Carefully qualifying new magnetics modules prevents this problem.

The steps involved in magnetics module qualification are similar to those for crystal qualification:

1. Verify that the vendor's published specifications in the component datasheet meet or exceed the required IEEE specifications.
2. Independently measure the component's electrical parameters on the test bench, checking samples from multiple lots. Check that the measured behavior is consistent from sample to sample and that measurements meet the published specifications.
3. Perform physical layer conformance testing and EMC (FCC and EN) testing in real systems. Vary temperature and voltage while performing system level tests.

Magnetics modules for 1000 BASE-T Ethernet are similar to those designed solely for 10/100 Mbps, except that there are four differential signal pairs instead of two. Use the following guidelines to verify specific electrical parameters:

1. Verify that the rated return loss is 19 dB or greater from 2 MHz through 30 MHz for 100 BASE-TX.
2. Verify that the rated return loss is 12 dB or greater at 80 MHz for 100 BASE-TX (the specification requires greater than or equal to 10 dB).
3. Verify that the rated return loss is 10 dB or greater at 100 MHz for 1000 BASE-TX (the specification requires greater than or equal to 8 dB).
4. Verify that the insertion loss is less than 1.0 dB at 100 kHz through 80 MHz for 100 BASE-TX.
5. Verify that the insertion loss is less than 1.4 dB at 100 kHz through 100 MHz for 1000 BASE-T.
6. Verify at least 30 dB of crosstalk isolation between adjacent channels (through 150 MHz).
7. Verify high voltage isolation to 15000 Vrms
8. Transmitter OCL should be greater than or equal to 350 µH with 8 mA DC bias.

Table 3. Third-party Magnetics Modules[1]

Manufacturer	Part Number
Pulse	JW0A2P019D
Discrete	H5007 Bel 0344FLA

1. These modules have been used successfully in past designs, however no particular product is recommended.

3.2 Designing with the 82563EB/82564EB Gigabit Ethernet Platform LAN Connect

This section provides design guidelines specific to the 82563EB/82564EB Gigabit Ethernet Platform LAN Connect.

3.2.1 Powering Down the 82563EB/82564EB Gigabit Ethernet Platform LAN Connect

The 82563EB/82564EB device has a signal named PHY_SLEEP that can be used as an alternative to an in-band event for powering down the Ethernet PHY functions driven only by the 631xESB/632xESB. When using the in-band event, PHY_SLEEP should be connected to a pulldown resistor for normal operation.

3.2.2 Serial EEPROM for 82563EB/82564EB Gigabit Ethernet Platform LAN Connect Implementations

Please note that the EEPROM is connected to the 631xESB/632xESB and not directly to the 82563EB/82564EB. Several words of the EEPROM are accessed automatically by the device after reset to provide pre-boot configuration data before it is accessed by host software. The remainder of the EEPROM space is available to software for storing the MAC address, serial numbers, and additional information. More details may be obtained from the Bensley/Bensley-VS Platform Design Guide.

Intel has an MS-DOS* software utility called EEUPDATE, which can be used to program EEPROM images in development or production line environments. To obtain a copy of this program, contact your Intel representative.

3.2.3 Power Supplies for the 82563EB/82564EB Device

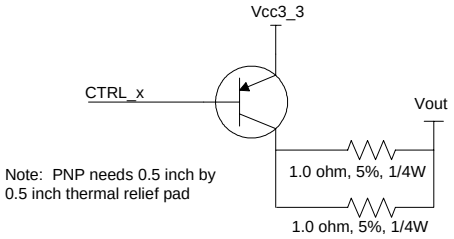
The 82563EB/82564EB device requires three power supplies (3.3V, 1.9V, and 1.2V). For 1000BASE-T designs, the 1.2V supply must provide approximately 580 mA current. The 1.9V supply must provide approximately 850 mA current. The 3.3V supply must provide approximately 25 mA current.

A central power supply can provide all the required voltage sources, or the power can be derived from the 3.3V supply and regulated locally near the Ethernet control circuitry. Keep in mind that all voltage sources must remain present during powerdown in order to use the 82563EB/82564EB Gigabit Ethernet Platform LAN Connect device's LAN wake up capability. This consideration makes it more likely that at least some of the voltage sources will be local.

Instead of using external regulators to supply 1.2V and 1.9V, the designer may use power transistors in conjunction with on-chip regulation circuitry. When using the internal voltage regulation control logic, the sequencing of the voltages are controlled internally by the 82563EB/82564EB. Refer to the 82563EB/82564EB Gigabit Platform LAN Connect Datasheet for specific internal power sequencing requirements.

The design may require two external PNP transistors, one for 1.9V and the other for 1.2V generation, if both voltages are going to be regulated by the 82563EB/82564EB. The beta for the PNP transistors must be 100 or better. For the 82563EB only (not applicable to 82564EB single port) resistors are required to dissipate heat with the dual-port platform LAN connect as shown in Figure 4. Ensure that there is a 0.5 inch by 0.5 inch thermal relief for both transistors. If standby 3.3V is being used for power management, then ensure that the same 3.3V VccAux is sourcing the transistor(s). To minimize inductance, CTRL_12 and CTRL_18 line must be less than two inches routed length, and use 12 mil traces.

Figure 4. LVR Circuit for the 82563EB (Dual Port)



The single port 82564EB Platform LAN Connect requires less power than the dual port 82563EB which eliminates the need for dissipation resistors as seen in Figure 5. The PNP transistor for the 82564EB still maintains the minimum beta of 100, with a separate transistor needed per voltage rail similar to the 82563EB.

Figure 5. LVR Circuit for the 82564EB (Single Port)

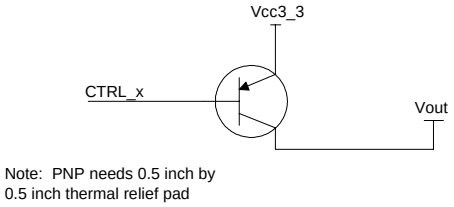


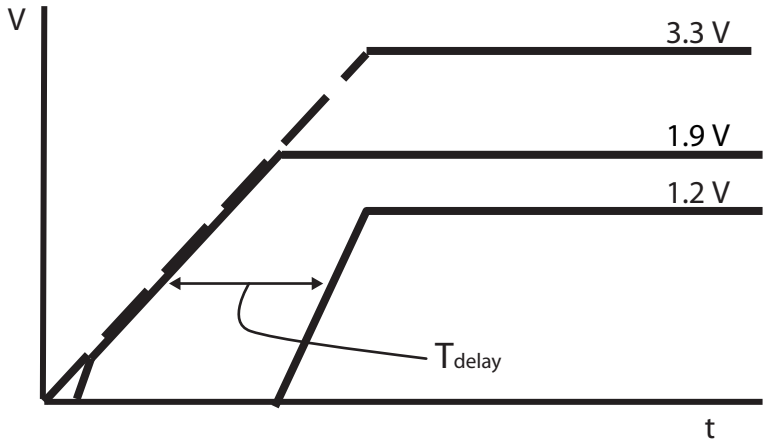
Table 4 shows several vendors and their respective part numbers that are recommended for the PNP transistors.

Table 4. PNP Transistors Vendors/Part Numbers

Vendor	Part Number
Infineon	BCP69-16
Philips	BCP69-16
On Semi	BCP69-16

If the designer chooses to do their own external voltage regulation and not use the PNP transistors, then they must adhere to the sequencing shown in Figure 6 to avoid latch-up and forward-biased internal diodes. The general guideline is that for power up, the higher voltage is up and stable prior to the next lower voltage. In other words, 3.3V is greater than1.9V > 1.2V.

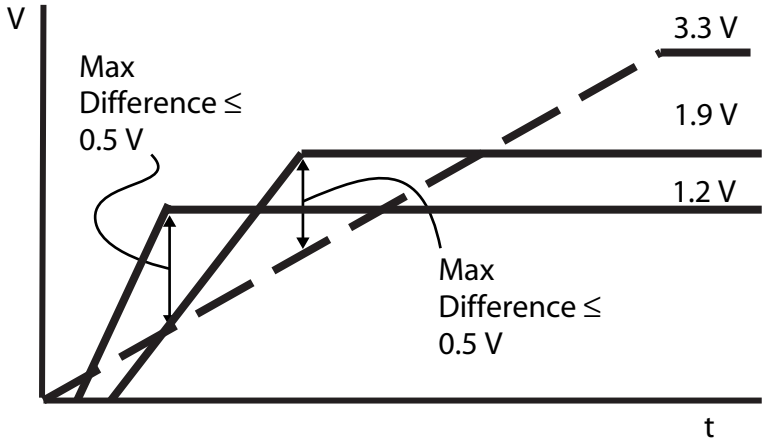
Figure 6. 82563EB Power Sequencing



In addition, as shown on Figure 7, the voltages must not exceed by more than 0.5V in each of the following cases:

- The 82563EB/82564EB core voltage (1.2V) cannot exceed the 3.3V supply by more than 0.5V at any time during the power up. The 82563EB core voltage (1.2V) can not exceed the 1.9V supply by more than 0.5V at any time during the power up. The core voltage is not required to begin ramping before the 3.3V or the 1.9V supply.
- The 82563EB/82564EB analog voltage (1.9V) cannot exceed the 3.3V supply by more than 0.5V at any time during the power up. The analog voltage is not required to begin ramping before the 3.3V supply.

Figure 7. Maximum Difference between Voltage Rails



For power down, there is no specific requirement, only charge that is stored in the decoupling caps remains.

The 82563EB/82564EB device has a PHY_PWR_GOOD input. Treat this signal as an external device reset which works in conjunction with the internal power-on reset circuitry. In the situation where a central power supply furnishes all the voltage sources, PHY_PWR_GOOD can possibly be tied to the platform's RSM_RST#. Designs that generate some of the voltages locally can connect PHY_PWR_GOOD to a power monitor chip that monitors all three required voltages. Ensure that the system holds PHY_PWR_GOOD inactive for at least 100 µsec after power-up of all three voltages rails.

The power sources are all expected to ramp up during a brief power-up interval with PHY_PWR_GOOD de-asserted. Do not leave the 82563EB/82564EB device in a prolonged state where some, but not all, voltages are applied.

Warning: Do ***not*** tie PHY_PWR_GOOD directly to a voltage supply.

3.2.4 82563EB/82564EB Device Power Supply Filtering

Provide several high-frequency bypass capacitors for each power rail, selecting values in the range of 0.001 µF to 0.01 µF. If possible, orient the capacitors close to the device and adjacent to power pads. Place one 470 pF capacitor near AVDDF (pin 92) and another one 470 pF capacitor near AVDDF (pin 86); these two power pins are used for the high speed Kumeran interface. Decoupling capacitors should connect to the power planes with short, thick (15 mils - 0.4 mm or more) traces and 14 mil (0.35 mm) vias.

Table 5. Minimum Number of Bypass Capacitors per Voltage Rail

Voltage Rail	4.7 uF	0.1 uF	470 pF
3.3V	1	1	-
1.9V	1	2	2
1.2V	1	2	1

Furnish approximately 4.7 µF of bulk capacitance for each of the main 1.2V and 1.9V levels, placing them as close to the device power connections as possible. The minimum recommended bypass capacitors for each voltage rail is shown in Figure 5. For internal voltage regulators, place the bulk capacitor as close to the collector of the transistor. A low reactance path is mandatory to maintain internal voltage regulator stability and reduce voltage oscillations.

3.2.5 82563EB/82564EB Device Test Capability

The 82563EB/82564EB Gigabit Ethernet Platform LAN Connect contains a test access port (3.3V only) conforming to the IEEE 1149.1a-1994 (JTAG) Boundary Scan specification. To use the test access port, connect these balls to pads accessible by your test equipment.

The device also contains an XOR test tree mechanism for simple board tests.

A BSDL (Boundary Scan Definition Language) file describing the 82563EB/82564EB device is available for use in your test environment, via the Intel Field Division Business Link (FDBL). The file is located at:

> Networking/Communications->Ethernet Products->Ethernet Controllers (all interfaces)-> LAN Silicon->82563EB->Technical

and:

> Networking/Communications->Ethernet Products->Ethernet Controllers (all interfaces)-> LAN Silicon-> 82564EB > Technical

Contact your local Intel representative for the latest information.

3.2.5.1 XOR Testing

A common board or system-level manufacturing test for proper electrical continuity between a silicon component and the board is some type of cascaded-XOR or NAND tree test. The 82563EB/82564EB implements an XOR tree spanning most I/O signals. The component XOR tree consists of a series of cascaded XOR logic gates, each stage feeding in the electrical value from a unique pin. The output of the final stage of the tree is visible on an output pin from the component.

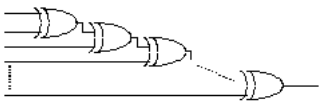


Figure 8. XOR Tree Concept

By connecting to a set of test-points or bed-of-nails fixture, a manufacturing test fixture may test connectivity to each of the component pins included in the tree by sequentially testing each pin, testing each pin when driven both high and low, and observing the output of the tree for the expected signal value and/or change.

To enter the XOR tree test mode, the following pins must be set to specific values on the rising edge of PHY_PWR_GOOD:

- TEST_JTAG = 0
- JTAG_TCK = 0
- JTAG_TMS = 1
- JTAG_TDI = 0

Once the 82563EB/82564EB enters XOR tree mode it will remain in XOR tree mode until PHY_PWR_GOOD is deasserted.

Note: Some of the pins that are inputs for the XOR test are listed as "may be left disconnected" in the pin descriptions. If XOR test is used, all inputs to the XOR tree must be connected.

When the XOR tree test is selected, the following behaviors occur:

- Output drivers for the pins listed as "tested" are all placed in high-impedance (tri-state) state to ensure that board/system test fixture may drive the tested inputs without contention.
- Internal pull-up and pull-down devices for pins listed as "tested" are also disabled to further ensure no contention with the board/system test fixture.
- The XOR tree is output on the MDIO_ADD[0] pin.

Table 6. Tested pins included in XOR Tree (33 pins)

Pin Name	Pin Name	Pin Name
PHY_SLEEP	LEDA_SPEED_1000_N	RESERVED_NC (pin 6)
MDIO	LINK_B	RESERVED_NC (pin 8)
MDC	LEDB_DUPLEX	RESERVED_NC (pin 9)
MDIO_ADD[3:1]	LEDB_TX_ACTIVITY	RESERVED_NC (pin 10)
LINK_A	LEDB_RX_ACTIVITY	RESERVED_NC (pin 13)
LEDA_DUPLEX	LEDB_LINK_UP_N	RESERVED_NC (pin 14)
LEDA_TX_ACTIVITY	LEDB_ACTIVITY_N	RESERVED_NC (pin 15)
LEDA_RX_ACTIVITY	LEDB_SPEED_100N	RESERVED_NC (pin 17)
LEDA_LINK_UP_N	LEDB_SPEED_1000_N	RESERVED_NC (pin 98)
LEDA_ACTIVITY_N	RESERVED_NC (pin 4)	
LEDA_SPEED_100_N	RESERVED_NC (pin 5)	

Table 7. Pins not included in the XOR tree (10 pins)

Pin Name	Pin Name
PHY_PWR_GOOD	JTAG_TMS
PHY_RESET_N	JTAG_TDO
RESERVED_PD (pin 82)	TEST_JTAG
JTAG_TCK	MDIO_ADD[0]
JTAG_TDI	PHY_CLK_OUT

Note: The XOR test inputs include some RESERVED_NC pins. If the XOR test is used, these specific pins must be connected. They should be connected through weak pull-ups or pull-downs, as they might be driven as outputs in functional operation. The remaining RESERVED_NC pins should not be connected. Also, while in XOR test mode, it is acceptable to drive RESERVED_PD high as long as it was low before and during the rising edge of PHY_PWR_GOOD.

4.0 Frequency Control Device Design Considerations

This section provides information regarding frequency control devices, including crystals and oscillators, for use with all Intel® Ethernet controllers. Several suitable frequency control devices are available; none of which present any unusual challenges in selection. The concepts documented herein are applicable to other data communication circuits, including Platform LAN Connect devices (PHYs).

The Intel® Ethernet controllers contain amplifiers which, when used with the specific external components, form the basis for feedback oscillators. These oscillator circuits, which are both economical and reliable, are described in more detail in “Crystal Selection Parameters”.

The Intel® Ethernet controllers also have bus clock input functionality, however a discussion of this feature is beyond the scope of this document, and will not be addressed.

The chosen frequency control device vendor should be consulted early in the design cycle. Crystal and oscillator manufacturers familiar with networking equipment clock requirements may provide assistance in selecting an optimum, low-cost solution.

4.1 Frequency Control Component Types

Several types of third-party frequency reference components are currently marketed. A discussion of each follows, listed in preferred order.

4.2 Quartz Crystal

Quartz crystals are generally considered to be the mainstay of frequency control components due to their low cost and ease of implementation. They are available from numerous vendors in many package types and with various specification options.

4.3 Fixed Crystal Oscillator

A packaged fixed crystal oscillator is comprised of an inverter, a quartz crystal, and passive components conveniently packaged together. The device renders a strong, consistent square wave output. Oscillators used with microprocessors are supplied in many configurations and tolerances.

Crystal oscillators should be restricted to use in special situations, such as shared clocking among devices or multiple controllers. As clock routing can be difficult to accomplish, it is preferable to provide a separate crystal for each device.

For Intel® Ethernet controllers, it is acceptable to overdrive the internal inverter by connecting a 25 MHz external oscillator to the XTAL1 lead, leaving the XTAL2 lead unconnected. The oscillator should be specified to drive CMOS logic levels, and the clock trace to the device should be as short as possible. Device specifications typically call for a 40% (minimum) to 60% (maximum) duty cycle and a ±50 ppm frequency tolerance.

Note: Please contact your Intel Customer Representative to obtain the most current device documentation prior to implementing this solution.

4.4 Programmable Crystal Oscillators

A programmable oscillator can be configured to operate at many frequencies. The device contains a crystal frequency reference and a phase lock loop (PLL) clock generator. The frequency multipliers and divisors are controlled by programmable fuses.

A programmable oscillator's accuracy depends heavily on the Ethernet device's differential transmit lines. The Physical Layer (PHY) uses the clock input from the device to drive a differential Manchester (for 10 Mbps operation), an MLT-3 (for 100 Mbps operation) or a PAM-5 (for 1000 Mbps operation) encoded analog signal across the twisted pair cable. These signals are referred to as self-clocking, which means the clock must be recovered at the receiving link partner. Clock recovery is performed with another PLL that locks onto the signal at the other end.

PLLs are prone to exhibit frequency jitter. The transmitted signal can also have considerable jitter even with the programmable oscillator working within its specified frequency tolerance. PLLs must be designed carefully to lock onto signals over a reasonable frequency range. If the transmitted signal has high jitter and the receiver's PLL loses its lock, then bit errors or link loss can occur.

PHY devices are deployed for many different communication applications. Some PHYs contain PLLs with marginal lock range and cannot tolerate the jitter inherent in data transmission clocked with a programmable oscillator. The American National Standards Institute (ANSI) X3.263-1995 standard test method for transmit jitter is not stringent enough to predict PLL-to-PLL lock failures, therefore, the use of programmable oscillators is generally not recommended.

4.5 Ceramic Resonator

Similar to a quartz crystal, a ceramic resonator is a piezoelectric device. A ceramic resonator typically carries a frequency tolerance of ±0.5%, – inadequate for use with Intel® Ethernet controllers, and therefore, should not be utilized.

5.0 Crystal Selection Parameters

All crystals used with Intel® Ethernet controllers are described as “AT-cut,” which refers to the angle at which the unit is sliced with respect to the long axis of the quartz stone. The following table lists crystals which have been used successfully in past designs (however no particular product is recommended):

Table 8. Crystal Manufacturers and Part Numbers

Manufacturer	Part No.
RALTRON	AS-25.000-20-SMD-TR-NS7
TXC CORPORATION - USA	6C25000131

Table 9 lists the crystal electrical parameters and provides suggested values for typical designs. Designers should refer to criteria outlined in the 82563EB/82564EB Datasheet. The parameters are described in the subsections following the table.

Table 9. Crystal Parameters

Parameter	Suggested Value	Conditions
Vibrational Mode	Fundamental	
Nominal Frequency	25.000 MHz	at 25° C
Frequency Tolerance	• ±30 ppm recommended • ±50 ppm across the entire operating temperature range (required by IEEE specifications)	at 25° C
Temperature Tolerance	±30 ppm	at 0° C to 70° C
Calibration Mode	Parallel	
Load Capacitance	27 pF	
Shunt Capacitance	6 pF maximum	
Equivalent Series Resistance	50 Ω maximum	at 25 MHz
Drive Level	750 µW	
Aging	±5 ppm per year maximum	

5.1 Vibrational Mode

Crystals in the above-referenced frequency range are available in both fundamental and third overtone. Unless there is a special need for third overtone, use fundamental mode crystals.

At any given operating frequency, third overtone crystals are thicker and more rugged than fundamental mode crystals. Third overtone crystals are more suitable for use in military or harsh industrial environments. Third overtone crystals require a trap circuit (extra capacitor and inductor) in the load circuitry to suppress fundamental mode oscillation as the circuit powers up. Selecting values for these components is beyond the scope of this document.

5.2 Nominal Frequency

Intel® Ethernet controllers use a crystal frequency of 25.000 MHz. The 25 MHz input is used to generate a 125 MHz transmit clock for 100BASE-TX and 1000BASE-TX operation – 10 MHz and 20 MHz transmit clocks, for 10BASE-T operation.

5.3 Frequency Tolerance

The frequency tolerance for an Ethernet Platform LAN Connect is dictated by the IEEE 802.3 specification as ±50 parts per million (ppm). This measurement is referenced to a standard temperature of 25° C. Intel recommends a frequency tolerance of ±30 ppm.

5.4 Temperature Stability and Environmental Requirements

Temperature stability is a standard measure of how the oscillation frequency varies over the full operational temperature range (and beyond). Several optional temperature ranges are currently available, including -40° C to +85° C for industrial environments. Some vendors separate operating temperatures from temperature stability. Manufacturers may also list temperature stability as 50 ppm in their data sheets.

Note: Crystals also carry other specifications for storage temperature, shock resistance, and reflow solder conditions. Crystal vendors should be consulted early in the design cycle to discuss the application and its environmental requirements.

5.5 Calibration Mode

The terms “series-resonant” and “parallel-resonant” are often used to describe crystal oscillator circuits. Specifying parallel mode is critical to determining how the crystal frequency is calibrated at the factory.

A crystal specified and tested as series resonant oscillates without problem in a parallel-resonant circuit, but the frequency is higher than nominal by several hundred parts per million. The purpose of adding load capacitors to a crystal oscillator circuit is to establish resonance at a frequency higher than the crystal’s inherent series resonant frequency.

Figure 9 illustrates a simplified schematic of the internal oscillator circuit. Pin X1 and X2 refers to XTAL1 and XTAL2 in the Ethernet device, respectively. The crystal and the capacitors form a feedback element for the internal inverting amplifier. This combination is called parallel-resonant,

because it has positive reactance at the selected frequency. In other words, the crystal behaves like an inductor in a parallel LC circuit. Oscillators with piezoelectric feedback elements are also known as “Pierce” oscillators.

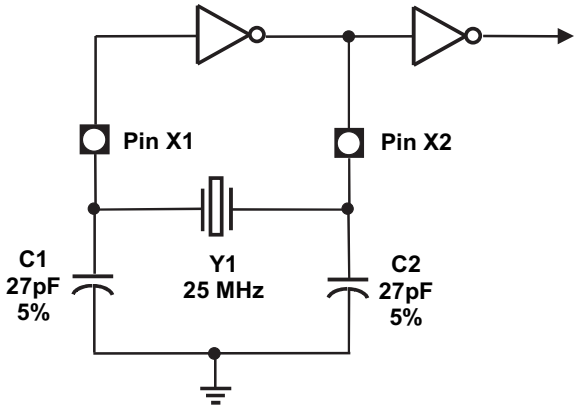


Figure 9. Internal Oscillator Circuit

5.6 Load Capacitance

The formula for crystal load capacitance is as follows:

$$C_L = \frac{(C1 \cdot C2)}{(C1 + C2)} + C_{stray}$$

where C1 = C2 = 27 pF (as suggested in most Intel reference designs)

and C_{stray} = allowance for additional capacitance in pads, traces and the chip carrier within the Ethernet device package

An allowance of 3 pF to 7 pF accounts for lumped stray capacitance. The calculated load capacitance is 20 pF with an estimated stray capacitance of about 5 pF.

Individual stray capacitance components can be estimated and added. For example, surface mount pads for the load capacitors add approximately 2.5 pF in parallel to each capacitor. This technique is especially useful if Y1, C1 and C2 must be placed farther than approximately one-half (0.5) inch from the device. It is worth noting that thin circuit boards generally have higher stray capacitance than thick circuit boards.

Standard capacitor loads used by crystal manufacturers include 16 pF, 18 pF and 20 pF. Any of these values will generally operate with the device. However, a difference of several picofarads between the calibrated load and the actual load will pull the oscillator slightly off frequency.

The oscillator frequency should be measured with a precision frequency counter where possible. The load specification or values of C1 and C2 should be fine tuned for the design. As the actual capacitance load increases, the oscillator frequency decreases.

Note: C1 and C2 may vary by as much as 5% (approximately 1 pF) from their nominal values.

5.7 Shunt Capacitance

The shunt capacitance parameter is relatively unimportant compared to load capacitance. Shunt capacitance represents the effect of the crystal's mechanical holder and contacts. The shunt capacitance should equal a maximum of 6 pF (7 pF is also acceptable).

5.8 Equivalent Series Resistance

Equivalent Series Resistance (ESR) is the real component of the crystal's impedance at the calibration frequency, which the inverting amplifier's loop gain must overcome. ESR varies inversely with frequency for a given crystal family. The lower the ESR, the faster the crystal starts up. Use crystals with an ESR value of 50 Ω or better.

5.9 Drive Level

Drive level refers to power dissipation in use. The allowable drive level for a Surface Mounted Technology (SMT) crystal is less than its through-hole counterpart, because surface mount crystals are typically made from narrow, rectangular AT strips, rather than circular AT quartz blanks.

Some crystal data sheets list crystals with a maximum drive level of 1 mW. However, Intel® Ethernet controllers drive crystals to a level less than the suggested 750 µW value. This parameter does not have much value for on-chip oscillator use.

5.10 Aging

Aging is a permanent change in frequency (and resistance) occurring over time. This parameter is most important in its first year because new crystals age faster than old crystals. Use crystals with a maximum of ±5 ppm per year aging.

5.11 Reference Crystal

The normal tolerances of the discrete crystal components can contribute to small frequency offsets with respect to the target center frequency. To minimize the risk of tolerance-caused frequency offsets causing a small percentage of production line units to be outside of the acceptable frequency range, it is important to account for those shifts while empirically determining the proper values for the discrete loading capacitors, C1 and C2.

Even with a perfect support circuit, most crystals will oscillate slightly higher or slightly lower than the exact center of the target frequency. Therefore, frequency measurements (which determine the correct value for C1 and C2) should be performed with an ideal reference crystal. When the capacitive load is exactly equal to the crystal's load rating, an ideal reference crystal will be perfectly centered at the desired target frequency.

5.11.1 Reference Crystal Selection

There are several methods available for choosing the appropriate reference crystal:

- If a Saunders and Associates (S&A) crystal network analyzer is available, then discrete crystal components can be tested until one is found with zero or nearly zero ppm deviation (with the appropriate capacitive load). A crystal with zero or near zero ppm deviation will be a good reference crystal to use in subsequent frequency tests to determine the best values for C1 and C2.
- If a crystal analyzer is not available, then the selection of a reference crystal can be done by measuring a statistically valid sample population of crystals, which has units from multiple lots and approved vendors. The crystal, which has an oscillation frequency closest to the center of the distribution, should be the reference crystal used during testing to determine the best values for C1 and C2.
- It may also be possible to ask the approved crystal vendors or manufacturers to provide a reference crystal with zero or nearly zero deviation from the specified frequency when it has the specified CLoad capacitance.

When choosing a crystal, customers must keep in mind that to comply with IEEE specifications for 10/100 and 10/100/1000Base-T Ethernet LAN, the transmitter reference frequency must be precise within ±50 ppm. Intel® recommends customers to use a transmitter reference frequency that is accurate to within ±30 ppm to account for variations in crystal accuracy due to crystal manufacturing tolerance. For information about measuring transmitter reference frequency, refer to Appendix A, “Measuring LAN Reference Frequency Using a Frequency Counter”.

5.11.2 Circuit Board

Since the dielectric layers of the circuit board are allowed some reasonable variation in thickness, the stray capacitance from the printed board (to the crystal circuit) will also vary. If the thickness tolerance for the outer layers of dielectric are controlled within ±17 percent of nominal, then the circuit board should not cause more than ±2 pF variation to the stray capacitance at the crystal. When tuning crystal frequency, it is recommended that at least three circuit boards are tested for frequency. These boards should be from different production lots of bare circuit boards.

Alternatively, a larger sample population of circuit boards can be used. A larger population will increase the probability of obtaining the full range of possible variations in dielectric thickness and the full range of variation in stray capacitance.

Next, the exact same crystal and discrete load capacitors (C1 and C2) must be soldered onto each board, and the LAN reference frequency should be measured on each circuit board.

The circuit board, which has a LAN reference frequency closest to the center of the frequency distribution, should be used while performing the frequency measurements to select the appropriate value for C1 and C2.

5.11.3 Temperature Changes

Temperature changes can cause the crystal frequency to shift. Therefore, frequency measurements should be done in the final system chassis across the system’s rated operating temperature range.

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6.0 Oscillator Support

The 82563EB/82564EB clock input circuit is optimized for use with an external crystal. However, an oscillator can also be used in place of the crystal with the proper design considerations:

- The clock oscillator has an internal voltage regulator of 1.2 V to isolate it from the external noise of other circuits to minimize jitter. If an external clock is used, this imposes a maximum input clock amplitude of 1.2 V.
- The input capacitance introduced by the 82563EB/82564EB (approximately 20 pF) is greater than the capacitance specified by a typical oscillator (approximately 15 pF).
- The input clock jitter from the oscillator can impact the 82563EB/82564EB clock and its performance.

Table 10. 82563EB/82564EB Clock Oscillator Specifications

Symbol	Parameter	Specifications			Units
		Min	Typical	Max	
f0	Frequency	-	25	-	MHz
df0	Frequency Variation	-50	-	+50	ppm
Dc	Duty Cycle	40	-	60	%
tr	Rise Time	-	-	5	ns
tf	Fall Time	-	-	5	ns
σi	Clock Jitter, rms (if specified)	-	-	50	ps
C1	Clock Capacitance (pushed by clock)	-	15	50	pF
VDD	Supply Voltage	-	3.3	-	V
Operating temperature	-	-	-	70	° C
CMOS output levels	Voltage Output High (V_{oh}), Voltage Output Low (V_{ol})	80% VDD	-	 20% VDD	V V

Note: The power consumption of additional circuitry equals about 1.5 mW.

The following table lists oscillators which have been used successfully in past designs (however no particular product is recommended):

Table 11. Oscillator Manufacturers and Part Numbers

Manufacturer	Part No.
RALTRON	CO4305-25.000-TR
CITIZEN AMERICA CORP	CSX750FBB25.000MTR

6.1 Oscillator Solution

There are two possible oscillator solutions: high voltage and low voltage.

6.1.1 High Voltage Solution (VDD = 3.3V)

This solution involves capacitor C1, which forms a capacitor divider with C_{stray} of about 20 pF. This attenuates the input clock amplitude and adjusts the clock oscillator load capacitance.

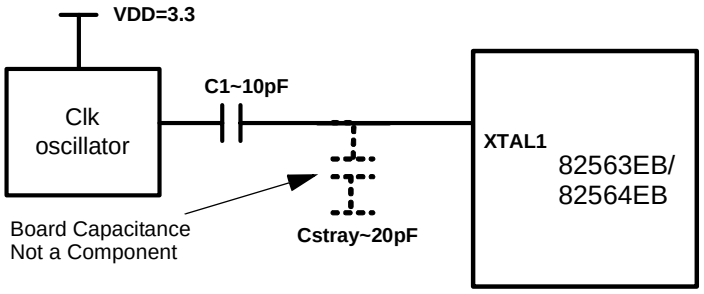
$$V_{in} = VDD * (C1/(C1 + C_{stray}))$$
$$V_{in} = 3.3 * (C1/(C1 + C_{stray}))$$

This enables load clock oscillators of 15 pF to be used. If the value of C_{stray} is unknown, C1 should be adjusted by tuning the input clock amplitude to approximately 1 V_{ptp}. If C_{stray} equals 20 pF, then C1 is 10 pF ±10%.

A low capacitance, high impedance probe (C < 1 pF, R > 500 K Ω) should be used for testing. Probing the parameters can affect the measurement of the clock amplitude and cause errors in the adjustment. A test should also be done after the probe has been removed for circuit operation.

If jitter performance is poor, a lower jitter clock oscillator can be implemented.

Note: Cstray shown in the figure below is not an actual discrete capacitor, but a representation of the board capacitance and should not be placed in the design itself.



7.0 Ethernet Component Layout Guidelines

These sections provide recommendations for performing printed circuit board layouts. Good layout practices are essential to meet IEEE PHY conformance specifications and EMI regulatory requirements.

7.1 Layout Considerations for the 82563EB/82564EB Ethernet Platform LAN Connect Devices

Critical signal traces should be kept as short as possible to decrease the likelihood of being affected by high frequency noise from other signals, including noise carried on power and ground planes. Keeping the traces as short as possible can also reduce capacitive loading.

Since the transmission line medium extends onto the printed circuit board, special attention must be paid to layout and routing of the differential signal pairs.

Designing for 1000 BASE-T Gigabit operation is very similar to designing for 10 and 100 Mbps. For the 82563EB/82564EB Gigabit Ethernet Platform LAN Connect, system level tests should be performed at all three speeds.

7.1.1 Guidelines for Component Placement

Component placement can affect signal quality, emissions, and component operating temperature This section provides guidelines for component placement.

Careful component placement can:

- Decrease potential problems directly related to electromagnetic interference (EMI), which could cause failure to meet applicable government test specifications.
- Simplify the task of routing traces. To some extent, component orientation will affect the complexity of trace routing. The overall objective is to minimize turns and crossovers between traces.

Minimizing the amount of space needed for the Ethernet LAN interface is important because other interfaces will compete for physical space on a motherboard near the connector. The Ethernet LAN circuits need to be as close as possible to the connector.

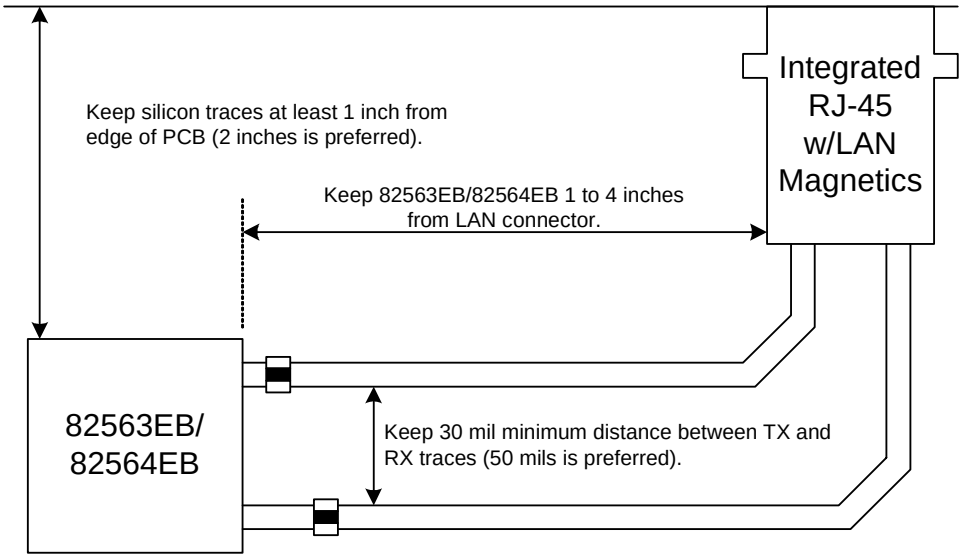


Figure 10. General Placement Distances for 1000 BASE-T Designs

Figure 10 shows some basic placement distance guidelines. For the sake of simplifying the figure; it shows only two differential pairs, but the layout can be generalized for a Gigabit system with four analog pairs. The ideal placement for the Ethernet silicon would be approximately one inch behind the magnetics module.

While it is generally a good idea to minimize lengths and distances, this figure also illustrates the need to keep the LAN silicon away from the edge of the board and the magnetics module for best EMI performance.

7.1.2 Crystals and Oscillators

Clock sources should not be placed near I/O ports or board edges. Radiation from these devices may be coupled onto the I/O ports or out of the system chassis. Crystals should also be kept away from the Ethernet magnetics module to prevent interference.

Place the crystal and load capacitors on the printed circuit boards as close to the Ethernet component as possible, within 0.75 of an inch. Ensure that the traces from XTAL1 and XTAL2 on the 82563EB/82564EB are routed symmetrically their lengths are matched.

If an oscillator is used instead, connect the clock signal with the shortest, most direct trace possible. Keep other potentially noisy traces away from the clock trace.

Refer back to Section 4.0 for more detail on timing device selection.

7.1.3 Board Stack Up Recommendations

Printed circuit boards for these designs typically have six or more layers. Although, the 82563EB/82564EB does not dictate the stackup, here is an example of a typical six-layer board stackup:

- Layer 1 is a signal layer. It can contain the differential analog pairs from the Ethernet device to the magnetics module.
- Layer 2 is a signal ground layer. Chassis ground may also be fabricated in Layer 2 under the connector side of the magnetics module.
- Layer 3 is a signal layer. It can contain the differential analog pairs from the Ethernet device to the magnetics module.
- Layer 4 is a signal layer. It can contain the differential analog pairs from the Ethernet device to the magnetics module.
- Layer 5 is used for power planes.
- Layer 6 is a signal layer. For 1000 BASE-T (copper) Gigabit designs, it is common to route two of the differential pairs (per port) on this layer.

This board stack up configuration can be adjusted to conform to your company's design rules. Please refer to the Blackford Platform Design Guide.

7.1.4 Differential Pair Trace Routing for 10/100/1000 Designs

Trace routing considerations are important to minimize the effects of crosstalk and propagation delays on sections of the board where high-speed signals exist. Signal traces should be kept as short as possible to decrease interference from other signals, including those propagated through power and ground planes.

7.1.4.1 Signal Termination and Coupling

The four differential pairs of each port are terminated with 49.9 Ω (1% tolerance) resistors, placed near the 82563EB/82564EB device. One resistor connects to the MDI+ signal trace and another resistor connects to the MDI- signal trace. The opposite ends of the resistors connect together and to ground through a single 0.1 µF capacitor. The capacitor should be placed as close as possible to the 49.9 Ω resistors, using a wide trace. Stubs created by the 49.9 Ω (1% tolerance) termination resistors should be kept at a minimum.

Do not vary the suggested component values. Be sure to lay out symmetrical pads and traces for these components such that the length and symmetry of the differential pairs are not disturbed.

7.1.5 Signal Trace Geometry for 1000 BASE-T Designs

The key factors in controlling trace EMI radiation are the trace length and the ratio of trace-width to trace-height above the reference plane. To minimize trace inductance, high-speed signals and signal layers that are close to a reference or power plane should be as short and wide as practical. Ideally, this trace width to height above the ground plane ratio is between 1:1 and 3:1. To maintain trace impedance, the width of the trace should be modified when changing from one board layer to another if the two layers are not equidistant from the neighboring planes.

Each pair of signal should have a differential impedance of 100 Ω +/- 20%. If a particular tool cannot design differential traces, it is permissible to specify 55-65 Ω single-ended traces as long as the spacing between the two traces is minimized. As an example, consider a differential trace pair on Layer 1 that is 8 mils (0.2 mm) wide and 2 mils (0.05 mm) thick, with a spacing of 8 mils (0.2 mm). If the fiberglass layer is 8 mils (0.2 mm) thick with a dielectric constant, E_R, of 4.7, the calculated single-ended impedance would be approximately 61 Ω and the calculated differential impedance would be approximately 100 Ω.

When performing a board layout, do *not* allow the CAD tool auto-router to route the differential pairs without intervention. In most cases, the differential pairs will have to be routed manually.

Note: Measuring trace impedance for layout designs targeting 100 Ω often results in lower actual impedance. Designers should verify actual trace impedance and adjust the layout accordingly. If the actual impedance is consistently low, a target of 105 – 110 Ω should compensate for second order effects.

It is necessary to compensate for trace-to-trace edge coupling, which can lower the differential impedance by up to 10 Ω, when the traces within a pair are closer than 30 mils (edge to edge).

7.1.6 Trace Length and Symmetry for 1000 BASE-T Designs

As indicated earlier, the overall length of differential pairs should be less than four inches measured from the Ethernet device to the magnetics.

The differential traces should be equal in total length to within 50 mils (1.25 mm) within each pair and as symmetrical as possible. Asymmetrical and unequal length traces in the differential pairs contribute to common mode noise. If a choice has to be made between matching lengths and fixing symmetry, more emphasis should be placed on fixing symmetry. Common mode noise can degrade the receive circuit's performance and contribute to radiated emissions.

7.1.7 Trace Routing, Geometry and Length for the Kumeran interface

Layout considerations for the Kumeran interface are very similar to those for PCIe*. The data lines are clocked at a 1.25 Gbps rate over differential pairs with a target differential impedance of 100 Ω., therefore board traces are likely to require manual routing.

The differential pairs between the Kumeran pins as symmetrical as possible. Asymmetrical and unequal length traces in the differential pairs contribute to common mode noise. The length of the traces is not as critical as the length of the analog traces in 1000BASE-T designs.

The Kumeran traces require special layout attention because the trace lengths are typically much longer. The key design consideration is making the traces *thick* enough to minimize resistive losses while still maintaining 100 Ω differential impedance. Refer to Section 2.1, "Kumeran Reference Clock" on page 4 for detail on length dependant clock sources for the Kumeran interface.

Observe the following suggestions to help optimize board performance:

- Maintain constant symmetry and spacing between the traces within a differential pair.
- Minimize the difference in signal trace lengths inside of a differential pair to less than 50 mils.
- Do not route a pair of differential traces closer than 30 mils to another differential pair.
- Do not route any other signal traces parallel to the differential traces, and closer than 30 mils to the differential traces (50 mils is recommended).

- Keep maximum separation within differential pairs to 9 mils.
- For high-speed signals, the number of corners and vias should be kept to a minimum. If a 90° bend is required, it is recommended to use two 45° bends instead. Refer to Figure 11.
- Traces should be routed away from board edges by a distance greater than the trace height above the reference plane. This allows the field around the trace to couple more easily to the ground plane rather than to adjacent wires or boards.
- Do not route traces and vias under crystals or oscillators. This will prevent coupling to or from the clock. And as a general rule, place traces from clocks and drives at a minimum distance from apertures by a distance that is greater than the largest aperture dimension.

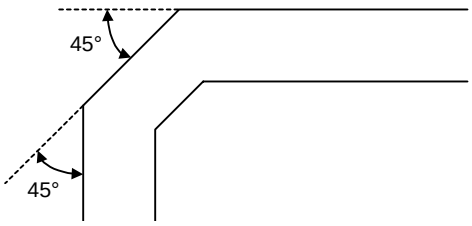


Figure 11. Trace Routing

- The reference plane for the differential pairs should be continuous and low impedance. It is recommended that the reference plane be either ground or 1.9V (the voltage used by the PHY). This provides an adequate return path for and high frequency noise currents.
- Do not route differential pairs over splits in the associated reference plane as it may cause discontinuity in impedances.
- Long traces are allowed up to 28 inches, but avoid highly resistive traces.
  - For long distances, thick traces are preferred over wide traces. Modify board stackup if necessary to avoid highly resistive traces.
  - Traces should be routed diagonal to the FR4 weave to maintain consistent impedance.
  - For differential traces that will be longer than 15 inches, the dielectric height under microstrip traces and the dielectric heights above/below stripline traces should be >= 4.3 mils nominal. For long distances, thick traces are preferred over wide traces.
  - If 1 oz. copper is used, minimum trace spacing within each differential pair must be >= 8 mils.
- Keep Kumeran differential pairs approximately 30 mils or greater away from each other.
  - Minimizes crosstalk and noise injection. This includes spacing to other digital traces, I/O ports, board edge, transformers and differential pairs.
  - If differential traces are less than 15 inches in length, keep adjacent traces away by at least 6X the dielectric thickness. For example, 4.5 mil thick FR4; spacing >= 27 mils.

7.1.7.1 Signal Termination and Coupling

Kumeran requires AC coupling at the receiver side of the signal. Carefully design 10 nF capacitors in series with the Kumeran traces.

7.1.8 Impedance Discontinuities

Impedance discontinuities cause unwanted signal reflections. Minimize vias (signal through holes) and other transmission line irregularities. If vias must be used, a reasonable budget is two per differential trace. Unused pads and stub traces should also be avoided.

7.1.9 Reducing Circuit Inductance

Traces should be routed over a continuous reference plane with no interruptions. If there are vacant areas on a reference or power plane, the signal conductors should not cross the vacant area. This causes impedance mismatches and associated radiated noise levels. Noisy logic grounds should be separated from analog signal grounds to reduce coupling. Noisy logic grounds can sometimes affect sensitive DC subsystems such as analog to digital conversion, operational amplifiers, etc. All ground vias should be connected to every ground plane; and similarly, every power via, to all power planes at equal potential. This helps reduce circuit inductance. Another recommendation is to physically locate grounds to minimize the loop area between a signal path and its return path. Rise and fall times should be as slow as possible. Because signals with fast rise and fall times contain many high frequency harmonics, which can radiate significantly. The most sensitive signal returns closest to the chassis ground should be connected together. This will result in a smaller loop area and reduce the likelihood of crosstalk. The effect of different configurations on the amount of crosstalk can be studied using electronics modeling software.

7.1.10 Signal Isolation

To maintain best signal integrity, keep digital signals far away from the analog traces. A good rule of thumb is no digital signal should be within 30 mils (7.5 mm) of the differential pairs. If digital signals on other board layers cannot be separated by a ground plane, they should be routed perpendicular to the differential pairs. If there is another LAN controller on the board, take care to keep the differential pairs from that circuit away.

Some rules to follow for signal isolation:

- Separate and group signals by function on separate layers if possible. If possible, maintain at least a gap of 50 mils between all differential pairs (Ethernet) and other nets, but group associated differential pairs together. Note: Over the length of the trace run, each differential pair should be at least 0.3 inches away from any parallel signal traces.
- Physically group together all components associated with one clock trace to reduce trace length and radiation.
- Isolate I/O signals from high-speed signals to minimize crosstalk, which can increase EMI emission and susceptibility to EMI from other signals.
- Avoid routing high-speed LAN traces near other high-frequency signals associated with a video controller, cache controller, processor, or other similar devices.

7.1.11 Power and Ground Planes

Good grounding requires minimizing inductance levels in the interconnections and keeping ground returns short, signal loop areas small, and power inputs bypassed to signal return, will significantly reduce EMI radiation.

The following guidelines help reduce circuit inductance in both backplanes and motherboards:

- Route traces over a continuous plane with no interruptions. Do not route over a split power or ground plane. If there are vacant areas on a ground or power plane, avoid routing signals over the vacant area. This will increase inductance and EMI radiation levels.
- Separate noisy digital grounds from analog grounds to reduce coupling. Noisy digital grounds may affect sensitive DC subsystems.
- All ground vias should be connected to every ground plane; and every power via should be connected to all power planes at equal potential. This helps reduce circuit inductance.
- Physically locate grounds between a signal path and its return. This will minimize the loop area.
- Avoid fast rise/fall times as much as possible. Signals with fast rise and fall times contain many high frequency harmonics, which can radiate EMI.
- The ground plane beneath a magnetics module should be split. The RJ45 connector side of the transformer module should have chassis ground beneath it.

7.1.12 Traces for Decoupling Capacitors

Traces between decoupling and I/O filter capacitors should be as short and wide as practical. Long and thin traces are more inductive and would reduce the intended effect of decoupling capacitors. Also for similar reasons, traces to I/O signals and signal terminations should be as short as possible. Vias to the decoupling capacitors should be sufficiently large in diameter to decrease series inductance.

7.1.13 Ground Planes Under a Magnetics Module (Copper-Based Gigabit designs)

The magnetics module chassis or output ground (secondary side of transformer) should be separated from the digital or input ground (primary side) by a physical separation of 100 mils minimum. Splitting the ground planes beneath the transformer minimizes noise coupling between the primary and secondary sides of the transformer and between the adjacent coils in the magnetics. This arrangement also improves the common mode choke functionality of magnetics module.

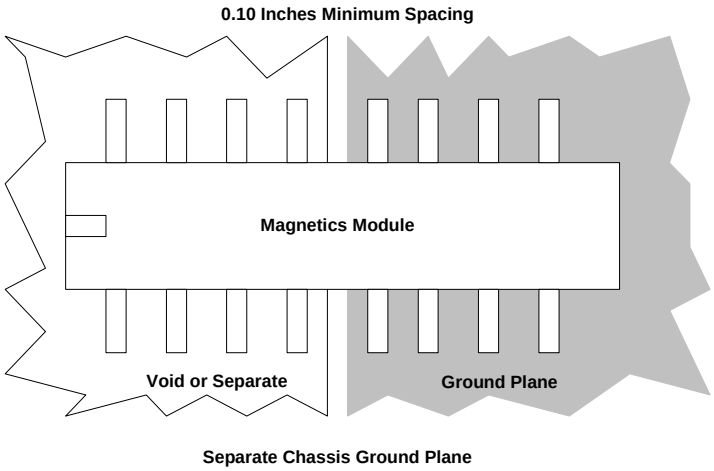


Figure 12. Ground Plane Separation

Figure 12 illustrates the split plane layout for a discrete magnetics module. Capacitors are used to interconnect chassis ground and signal ground.

Figure 13 below shows the preferred method for implementing a ground split under an integrated magnetics module/RJ-45 connector. This example shows a single port jack, but the same technique applies to a dual integrated module. The capacitor stuffing options (C1 – C6) are used to reduce/

filter high frequency emissions. The value(s) of the capacitor stuffing options may be different for each board. Experiments will need to be performed to determine which value(s) provide best EMI performance.

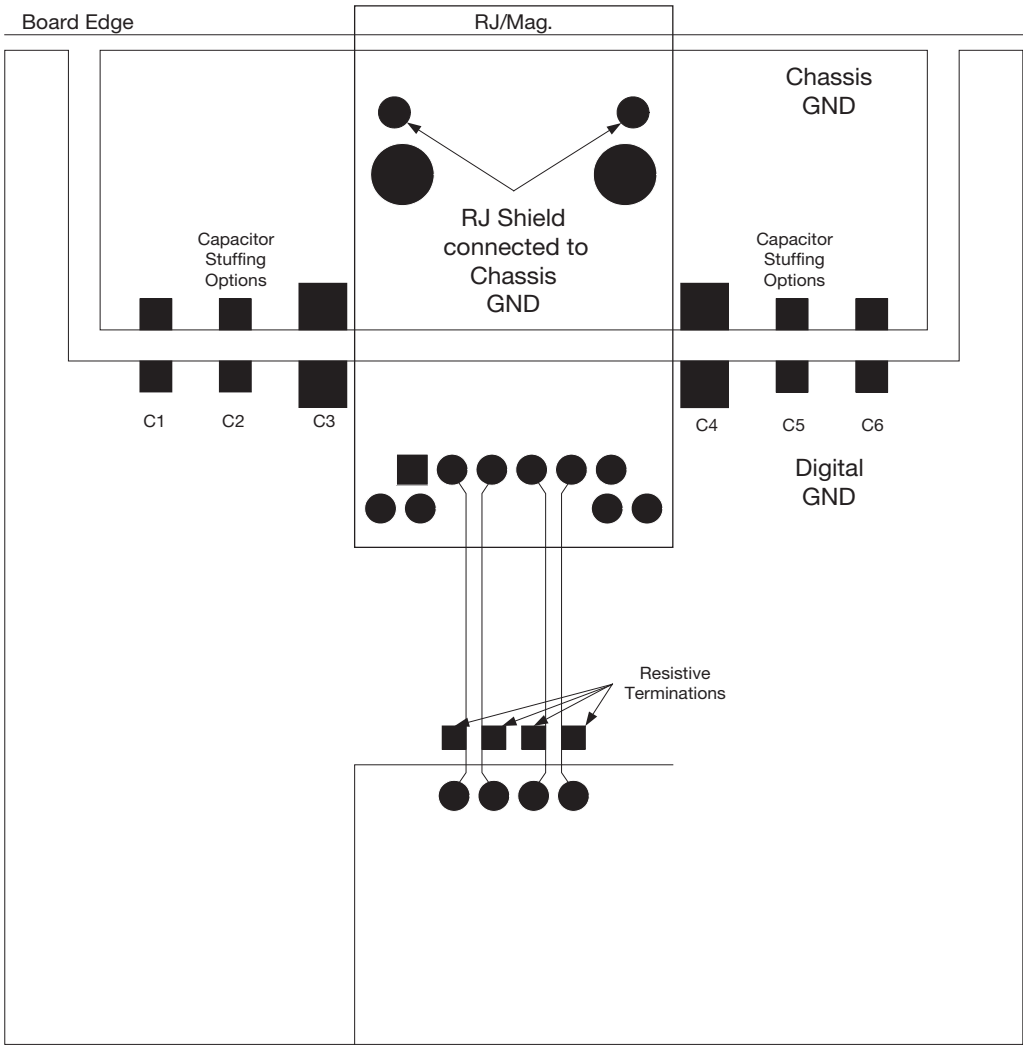


Figure 13. Ideal Ground Split Implementation

Table 12 below gives some starting values for these capacitors.

Table 12. Capacitor Stuffing Option Recommended Values

Capacitors	Value
C3, C4	4.7µF or 10 µF
C1, C2, C5, C6	470 pF to 0.1 µF

The placement of C1 – C6 may also be different for each board design (i.e., not all of the capacitors may need to be populated). Also, the capacitors may not be needed on both sides of the magnetic module.

7.1.14 Light Emitting Diodes for Designs Based on 82563EB/82564EB Device

The 82563EB/82564EB device provides seven total LEDs for each port. Four primary LEDs are programmable by the MAC in the 631xESB/632xESB enabling 16 different possible modes that are set in the EEPROM. Three LEDs are fixed and non-programmable. Of the three secondary LEDs, one is used for IEEE debug test header; it extracts the 125 MHz TX_TCLK for jitter measurements. See Section 3.1.1, “Clock Source” on page 7. The LED functions are restricted to the port such that Port B LEDs can not indicate status on Port A and vice versa. LEDs use a 12 mA totem pole driver which enable both discrete and integrated LEDs with their symmetric drive capability.

LED functions are determined by the 631xESB/632xESB’s EEPROM settings. The default 631xESB/632xESB settings are as follows (Port B LEDs not applicable to the 82564EB):

- LEDA_0: Port A LINK_UP
- LEDA_1: Port A ACTIVITY
- LEDA_2: Port A SPEED_100
- LEDA_3: Port A SPEED_1000
- LEDB_0: Port B LINK_UP
- LEDB_1: Port B ACTIVITY
- LEDB_2: Port B SPEED_100
- LEDB_3: Port B SPEED_1000

Since the LEDs are likely to be integral to a magnetics module, take care with care to route the LED traces away from potential sources of EMI noise. In some cases, it may be desirable to attach filter capacitors.

7.1.15 Thermal Design Considerations

The 82563EB/82564EB Gigabit Ethernet Platform LAN Connect does not require a heatsink across the operating ambient temperature range of 0° C to 60° C for 1000BASE-T designs without airflow. The maximum junction temperature is 120° C. Place the Ethernet Platform LAN Connect where it will receive sufficient airflow and allow extra space as needed for heatsink overhang and attachment hardware if needed. Heatsink and thermal coefficient data are contained in the 82563EB/82564EB Gigabit Ethernet Platform LAN Connect Datasheet.

7.2 Physical Layer Conformance Testing

Physical layer conformance testing (also known as IEEE testing) is a fundamental capability for all companies with Ethernet LAN products. PHY testing is the final determination that a layout has been performed successfully. If your company does not have the resources and equipment to perform these tests, consider contracting the tests to an outside facility.

7.2.1 Conformance Tests for 10/100/1000 Mbps Designs

Crucial tests are as follows, listed in priority order:

- Bit Error Rate (BER). Good indicator of real world network performance. Perform bit error rate testing with long and short cables and many link partners. The test limit is 10^{-8} errors.
- Output Amplitude, Rise and Fall Time (10/100 Mbps), Symmetry and Droop (1000 Mbps). Return Loss. Indicator of proper impedance matching, measured through the RJ-45 connector back toward the magnetics module.
- Jitter Test (10/100 Mbps) or Unfiltered Jitter Test (1000 Mbps). Indicator of clock recovery ability (master and slave for Gigabit device).

7.3 Troubleshooting Common Physical Layout Issues

The following is a list of common physical layer design and layout mistakes in LAN On Motherboard Designs.

1. Lack of symmetry between the two traces within a differential pair. Asymmetry can create common-mode noise and distort the waveforms. For each component and/or via that one trace encounters, the other trace should encounter the same component or a via at the same distance from the Ethernet silicon.
2. Unequal length of the two traces within a differential pair. Inequalities create common-mode noise and will distort the transmit or receive waveforms.
3. Excessive distance between the Ethernet silicon and the magnetics. Long traces on FR4 fiberglass epoxy substrate will attenuate the analog signals. In addition, any impedance mismatch in the traces will be aggravated if they are longer than the four inch guideline.
4. Routing any other trace parallel to and close to one of the differential traces. Crosstalk getting onto the receive channel will cause degraded long cable BER. Crosstalk getting onto the transmit channel can cause excessive EMI emissions and can cause poor transmit BER on long cables. At a minimum, other signals should be kept 0.3 inches from the differential traces.
5. Routing one pair of differential traces too close to another pair of differential traces. After exiting the Ethernet silicon, the trace pairs should be kept 0.3 inches or more away from the other trace pairs. The only possible exceptions are in the vicinities where the traces enter or exit the magnetics, the RJ-45 connector, and the Ethernet silicon.
6. Use of a low quality magnetics module.
7. Re-use of an out-of-date physical layer schematic in a Ethernet silicon design. The terminations and decoupling can be different from one PHY to another.
8. Incorrect differential trace impedances. It is important to have ~100 Ω impedance between the two traces within a differential pair. This becomes even more important as the differential traces become longer. To calculate differential impedance, many impedance calculators only multiply the single-ended impedance by two. This does not take into account edge-to-edge capacitive coupling between the two traces. When the two traces within a differential pair are kept close to each other, the edge coupling can lower the effective differential impedance by 5 Ω to 20 Ω. Short traces will have fewer problems if the differential impedance is slightly off target.

Note: This page is intentionally left blank.

8.0 82563EB/82564EB Exposed Pad*

8.1 Introduction

The 82563EB/82564EB is a 100-pin, 14 mm x 14 mm TQFP package with an Exposed-Pad*. The Exposed-Pad* is a central pad on the bottom of the package that provides the primary heat removal path as well as electrical grounding for a Printed Circuit Board (PCB).

In order to maximize both the removal of heat from the package and the electrical performance, a landing pattern must be incorporated on the PCB within the footprint of the package corresponding to the exposed metal pad or exposed heat slug on the package. The size of the landing pattern can be larger, smaller, or even take on a different shape than the Exposed-Pad* on the package. However, the solderable area, as defined by the solder mask, should be at least the same size/shape as the Exposed-Pad* on the package to maximize the thermal/electrical performance.

While the landing pattern on the PCB provides a means of heat transfer/electrical grounding from the package to the board through a solder joint, thermal vias are necessary to effectively conduct from the surface of the PCB to the ground plane(s). The number of vias are application specific and dependent upon the package power dissipation as well as electrical conductivity requirements. As a result, thermal and electrical analysis and/or testing are recommended to determine the minimum number needed.

Warning: Make sure that the 82563EB/82564EB has a good connection to ground. Check for solder voids on the Exposed Pad,* solder wicking, or a complete lack of solder. Failure to ensure a good connection to ground can result in functional failure.

The remainder of this section describes the silkscreen/component pads, solder mask, solder paste, and three potential landing patterns that can be used for the 82563EB/82564EB package. Note that these potential landing patterns have been used successfully in past designs, however no particular landing pattern is recommended. Please work with your manufacturer and assembler to ensure a process that is realiable.

8.2 Component Pad, Solder Mask and Solder Paste

Figure 14, Figure 15, and Figure 16 shows the silkscreen/components pad, solder mask and solder paste area for the 82563EB/82564EB package.

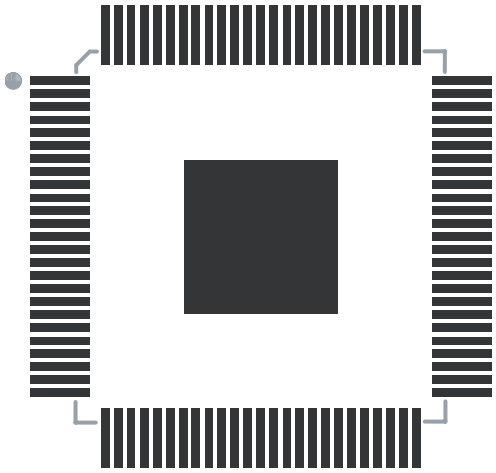


Figure 14. 82563EB/82564EB Silkscreen and Components Pad (Top View)

Figure 15. 82563EB/82564EB Solder Mask

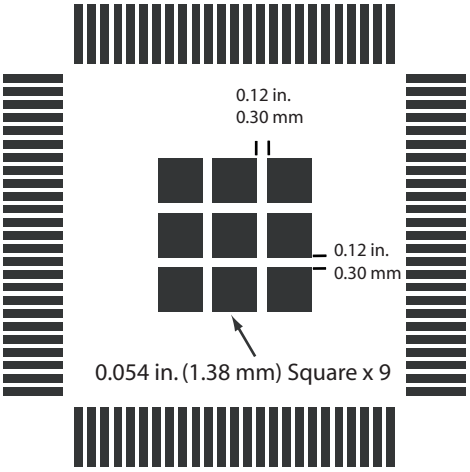


Figure 16. 82563EB/82564EB Solder Paste

The stencil for the solder paste should be 5 mils thick. Also, use a solder paste alloy consisting of 96.5Sn/3Ag/0.5Cu for a lead free process.

8.3 Landing Pattern A (No Via In Pad)

This landing pattern (vias outside Exposed Pad*) provides better solder coverage and less voiding than landing pattern C (vias inside Exposed Pad*). This landing pattern also meets Intel's recommendation for coverage >= 80%.

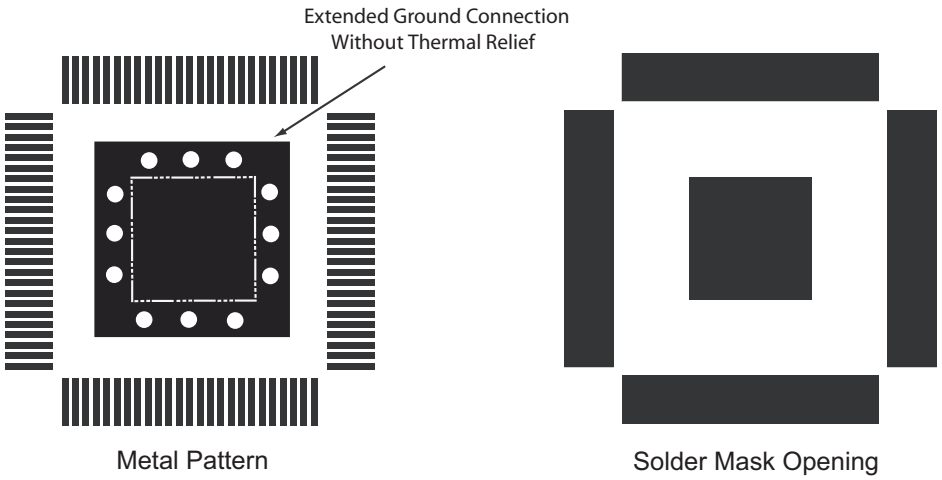


Figure 17. 82563EB/82564EB Landing Pattern A (Top View - Vias on the Outside of the Exposed Pad*)

Use 12 vias distributed on four sides (three per side, as shown in Figure 17) or three sides (four per side). Additional vias can be added to improve conductivity. If larger vias can be used (14 to 20 mil finished hole size), then a minimum of 9 vias can be evenly placed around the extended ground connection.

8.4 Landing Pattern B (Thermal Relief; No Via In Pad)

This landing pattern (vias outside Exposed Pad*) provides better solder coverage and less voiding than landing pattern C (vias inside Exposed Pad*). This landing pattern also meets Intel's recommendation for coverage >= 80%.

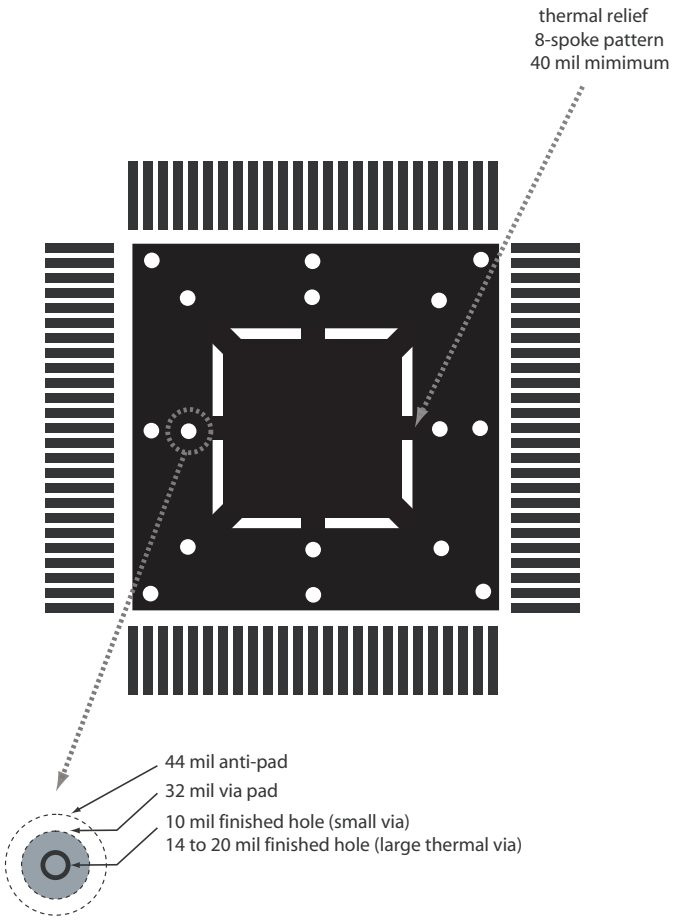


Figure 18. Landing Pattern B (Top View - Vias on the Outside of the Exposed Pad*)

Intel recommends using 16 vias evenly placed (as shown in Figure 18) around the extended ground connection. Additional vias can be added to improve conductivity. A minimum of 12 larger vias (14 to 20 mil finished hole size) can also be used .

8.5 Landing Pattern C (Via in Pad)

Intel recommends using nine vias evenly placed (as shown in Figure 19) inside the Exposed Pad*. This landing pattern also meets Intel's recommendation for coverage >= 80%.

Warning: Open vias can lead to solder wicking from the Exposed Pad*. Contact your board manufacturer for closed via options such as plated closed or plate-over epoxy fill.

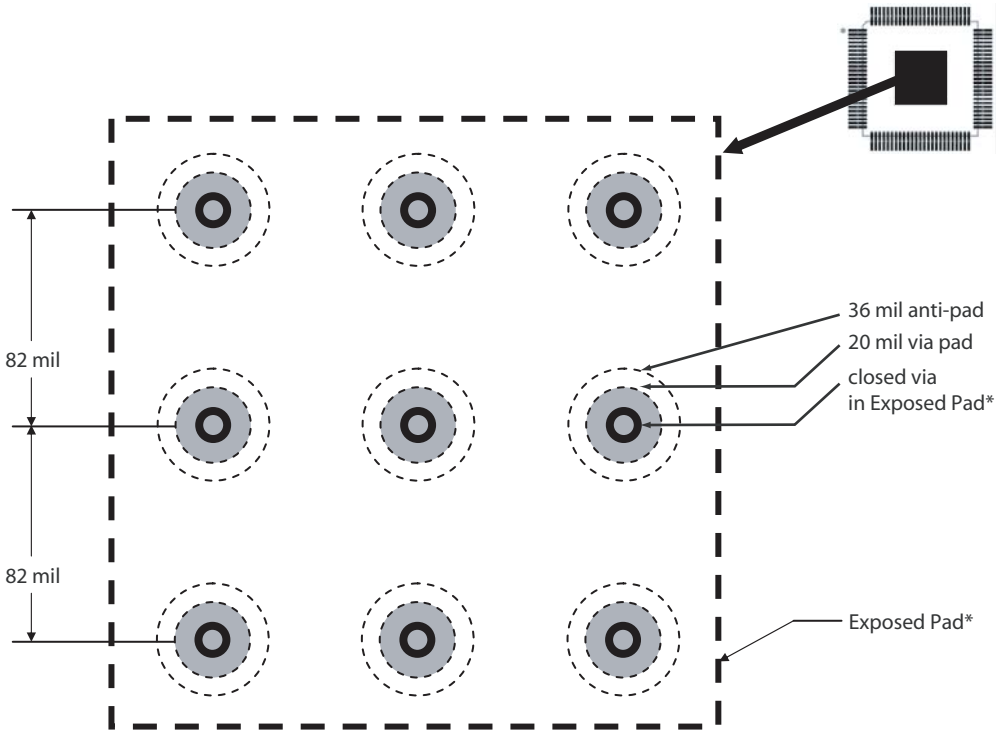


Figure 19. 82563EB/82564EB Landing Pattern C (Top View - Vias on the Inside of the Exposed Pad*)

9.0 Bill of Materials (BOM)

Table 13. BOM for the 631xESB/632xESB and the 82563EB/82564EB Gigabit Platform LAN Connect

Device	Qty	Component	Notes
631xESB/ 632xESB			Does not Include Management Interface
	1	24.9 Ω, 1% Tolerance	SEICOMP Resistor
	2	10 K Ω	Strappings
	2	4.7 K Ω	Strappings
	11	1 µF, X5R	1.5 Vaux Power Supply Decoupling
	1	22 µF, X5R	1.5 Vaux Power Supply Decoupling
	1	AT25128 EEPROM	

Device	Qty	Component	Notes
82563EB/ 82564EB			
	8	0.1µF, X7R, 10V, 0603	Kumeran AC Coupling
	6	4.7 K Ω, 5%	Strappings
	1	4.99 K Ω, 1%	BIAS Resistor
	3	1 K Ω, 5%	Strappings
	1	25.000 MHz, +/- 30 ppm Crystal	
	2	27 pF C0G, 5%, 50V Capacitor	Crystal Loading Caps
	5	10 K Ω	Strappings
	3	3.3 K Ω, 5%	Strappings
	1	40.2 Ω, 1% Tolerance	On PHY_CLK_OUT
	16	49.9 Ω, 1% Tolerance	MDI Termination
	8	0.1 µF Ceramic Capacitor	MDI Common Mode Termination
	1	Integrated Magnetics Module	Magnetics and RJ-45 with LEDs (Dual Stack)
	8	0.1 µF Ceramic Capacitor	Center Tap Capacitors for Magnetics Module (as required by module design)
	2	BCP69-16	Assuming a Discrete LVR is Used
	4	1 Ω, 1/4W, 1206, 5%	Regulator
	4	470 pF, 50V	LED EMI Decoupling
	4	330 Ω, 5% Tolerance	LEDs
	1	4.7 µF, 6.3V	3.3V Decoupling
	1	0.1 µF, X7R, 10V, 0603	3.3V Decoupling
	1	4.7 µF, 6.3V	1.9V Decoupling
	2	0.1 uF, X7R, 10V, 0603	1.9V Decoupling
	2	470 pF, 50V,	1.9V Decoupling
	1	4.7 µF, 6.3V	1.2V Decoupling
	2	0.1 µF, X7R, 10V, 0603	1.2V Decoupling
	1	470 pF, 50V,	1.2V Decoupling
	4	0.001 µF	GND Plane Split at Magnetics
	2	10 µF	GND Plane Split at Magnetics

10.0 Design, Layout, and Test Checklists

Design, Layout and Test checklists for the 82563EB/82564EB Gigabit Ethernet Platform LAN Connect are available to aid designers. These schematics are also available in spreadsheet format on the Intel public web site at: www.intel.com/developer.

Three checklists are available:

- Schematic
- Board Layout and Placement
- Validation

10.1 Schematic Checklist

SECTION	CHECK ITEMS	REMARKS
General	Have up-to-date product documentation and spec updates.	Documents are subject to frequent change.
	Observe instructions for special pins needing pull-up or pull-down resistors.	Do not connect pull-up or pull-down resistors to any pins marked No Connect.
Kumeran Interface	Connect Kumeran interface pins to corresponding pins on the 631xESB/632xESB.	
	Connect SETP0/SETN0 to RXA_PLUS/ RXA_MINUS on 82563EB/82564EB.	Correct polarity is mandatory, Kumeran interface does not support polarity correction.
	Connect SERP0/SERN0 to TXA_PLUS/ TXA_MINUS on 82563EB/82564EB.	Correct polarity is mandatory, Kumeran interface does not support polarity correction.
	Connect SETP1/SETN1 to RXB_PLUS/ RXB_MINUS on 82563EB/82564EB.	Correct polarity is mandatory, Kumeran interface does not support polarity correction.
		This connection is not available on the 82564EB.
	Connect SERP1/SERN1 to TXB_PLUS/ TXB_MINUS on 82563EB/82564EB.	Correct polarity is mandatory, Kumeran interface does not support polarity correction.
		This connection is not available on the 82564EB.
	All Kumeran interface AC coupling capacitors are 10 nF, X7R dielectric.	Use only 10 nF X7R capacitors on the Kumeran interface. Recommend 0402 package size, but 0603 is also acceptable.
		There are a total of 8 coupling capacitors for the 82563EB (4 for the 82564EB).

SECTION	CHECK ITEMS	REMARKS
Kumeran Interface	PHY_CLK_OUT connects to SER_CLK_IN on the 631xESB/632xESB through a 40 Ω series resistor.	Connect only if the routed length between the 82563EB/82564EB and 631xESB/632xESB is less than 15 inches. The 40 Ω series resistor is required for signal integrity.
		If the routed length between 82563EB/82564EB and the 631xESB/632xESB is greater than 15 inches, then PHY_CLK_OUT must be a no connect. Instead, use an oscillator clock source at 631xESB/632xESB.
	Connect PHY_RESET_N to VCCAUX3_3 using a 1 K to 10 K Ω Kumeran Interface resistor.	Signal is not used with 631xESB/632xESB.
	Connect PHY_SLEEP to GND using a 1K to 10 K Ω Kumeran Interface resistor.	Signal is not used with 631xESB/632xESB.
Clock Source	Use 25 MHz 30 ppm accuracy @ 25°C crystal clock source.	Parallel resonant crystals are required. The calibration load should be 20 pF. Specify Equivalent Series Resistance (ESR) to be 50 Ω or less.
		If using an oscillator instead, contact Intel for important circuit modifications. Avoid PLL clock buffers.
	Connect two load caps to crystal; one on XTAL1 and one on XTAL2. Use 27 pF capacitors as a starting point, but be prepared to change the value based on testing.	Capacitance affects accuracy of the frequency. Must be matched to crystal specs specified in datasheet, including estimated trace and pin capacitance.
		Use capacitors with low ESR (types C0G or NPO, for example).
LAN Controller	Connect LINK_A to GND with a 3.3 K to 10 K Ω resistor.	A pull-down resistor sets the frequency on PHY_CLK_OUT to 62.5 MHz; the recommended configuration.
		Use a 3.3 K to 10 K Ω resistor to VCCAUX3_3 to select 25 MHz.
		It is imperative that the frequency selected on the 82563EB/82564EB match the 631xESB/ 632xESB's SER_CLK_IN frequency selection.
	Connect LINK_B to GND with a 1 K to 3.3 K Ω resistor.	Enables PHY_CLK_OUT; the recommended configuration.
		Connect to GND with a 1 K to 3.3 K Ω resistor to enable PHY_CLK_OUT.
		If PHY_CLK_OUT is not desired, leave LINK_B as a no connect.
	Connect PHY_PWR_GOOD to system RSM_RST_N	Input must remain low until all power supplies are stable.
		PHY_PWR_GOOD must be a clean, glitch-free signal. It is not intended for use as a LAN disable. PHY_PWR_GOOD must be asserted during power-down states to allow wakeup.

SECTION	CHECK ITEMS	REMARKS
LAN Controller	Connect RESERVED_PD to GND with a 1 K to 10 K Ω resistor	Required for normal operation.
	Connect PHY_REF to GND with a 4.99 K Ω 1% tolerance resistor.	A 1% tolerance resistor is required for IEEE compliance.
	Connect TEST_JTAG to VCCAUX3_3 with a 1 to 10 K Ω resistor.	
	Connect MDIO_ADD[3:0] to GND with a 1 to 10 K Ω resistor.	The MDIO interface is not used on the 82563EB/ 82564EB.
	Connect MDC to GND with a 1 K to 10 K Ω resistor.	The MDC pin is not used on the 82563EB/ 82564EB.
	MDIO is a no connect.	This interface is not used on the 82563EB/ 82564EB. Leave as a no connect since MDIO has an internal pullup resistor.
	All RESERVED_NC signals are no connects.	Required for normal operation.
MDI Transmit and Receive Differential Pairs	82563EB device uses pairs of 49.9 Ω termination resistors with 0.1µF capacitors attached between center nodes and ground.	Apply to all four MDI differential pairs per port (8 pairs total).
		The 82564EB only has four MDI differential pairs.
	Connect signal pairs for port A correctly to RJ-45 connector.	The differential pairs must be mapped as follows:
		MDIA_PLUS[0] – RJ-45 pin 1.
		MDIA_MINUS[0] – RJ-45 pin 2.
		MDIA_PLUS[1] – RJ-45 pin 3.
		MDIA_MINUS[1] – RJ-45 pin 6.
		MDIA_PLUS[2] – RJ-45 pin 4.
		MDIA_MINUS[2] – RJ-45 pin 5.
		MDIA_PLUS[3] – RJ-45 pin 7.
		MDIA_MINUS[3] – RJ-45 pin 8.
		Do not reverse the polarity.
	Connect signal pairs for port B correctly to RJ-45 connector.	The differential pairs must be mapped as follows:
		MDIB_PLUS[0] – RJ-45 pin 1.
		MDIB_MINUS[0] – RJ-45 pin 2.
		MDIB_PLUS[1] – RJ-45 pin 3.
		MDIB_MINUS[1] – RJ-45 pin 6.
		MDIB_PLUS[2] – RJ-45 pin 4.
		MDIB_MINUS[2] – RJ-45 pin 5.

SECTION	CHECK ITEMS	REMARKS
MDI Transmit and Receive Differential Pairs		MDIB_PLUS[3] – RJ-45 pin 7,
		MDIB_MINUS[3] – RJ-45 pin 8,
		Do not reverse the polarity.
		This port is not available in the 82564EB. Leave unused MDI pins as no connect.
Magnetics Module	Integrated magnetics modules/RJ-45 connectors are available to minimize space requirements.	Dual and single port modules may be used. Modules with integrated USB are typical.
	Qualify magnetics module carefully for Return Loss, Insertion Loss, Open Circuit Inductance, Common Mode Rejection, and Crosstalk Isolation	Magnetics module is critical to passing IEEE PHY conformance tests and EMI test.
	Supply 1.9V to the silicon side of the transformer center taps and use a 0.1 µF bypass capacitor on every center tap pin (silicon side) of the magnetics module.	1.9V biases the device's output buffers. Magnetics with four center tap pins may have better characteristics than those with 1-2 center tap pins. Use capacitors with low ESR.
Power Supply and Signal Ground	Connect the base of external PNP transistors for the 1.2V supply to the regulator control CTRL_12 output.	Follow the reference schematic and do not substitute components. The connections and transistor parameters are critical. Use only BCP69-16 bipolar transistors. See the datasheet for transistor criteria.
		Alternatively, provide an external regulator to generate this voltage. If the internal voltage regulator control circuit is not used, connect the CTRL pin to GND through a 10 K Ω resistor.
		Check with your Intel representative for any circuit changes.
	Connect the base of external PNP transistors for the 1.9V supply to the regulator control CTRL_18 output.	Follow the reference schematic and do not substitute components. The connections and transistor parameters are critical. Use only BCP69-16 bipolar transistors. See the datasheet for transistor criteria.
		Alternatively, provide an external regulator to generate this voltage. If the internal voltage regulator control circuit is not used, connect the CTRL pin to GND through a 10 K Ω resistor.
		Check with your Intel representative for any circuit changes.
	Place two 1.0 Ω, 0.25 W, 5% resistors in parallel in the collector path of the PNP transistors.	Resistors are required when used with the 82563EB. The resistors must be in the collector path, not the emitter path for the regulator to operate without oscillations.
		Resistors are optional, but recommended, when used with the 82564EB.
	Connect the emitter of the 1.9V and 1.2V PNP transistors to VCCAUX3_3.	The input to the 1.9V and 1.2V transistors used with the internal LVR controller must be a 3.3V +/- 10% supply.

SECTION	CHECK ITEMS	REMARKS
Power Supply and Signal Ground		An auxiliary power supply is required to support Ethernet device wake up from powerdown states.
	Use decoupling and bulk capacitors generously.	The minimum acceptable decoupling by power supply is as follows (not including decoupling at magnetic):
		3.3V: 1 4.7 µF, 1 0.1 µF.
		1.9V: 1 4.7 µF, 2 0.1 µF, 2 470 pF.
		1.2V: 1 4.7 µF, 2 0.1 µF, 1 470 pF.
		If power is distributed on traces, bulk capacitors should be used at both ends. If power is distributed on cards, bulk capacitors should be used at the connector.
Chassis Ground (10/ 100/ 1000BASE-T Applications)	If possible, provide a separate chassis ground to connect the shroud of the RJ-45 connector and to terminate the line side of the magnetics module.	This design decreases EMI.
	Place pads for approximately four “stitching” capacitors to bridge the gap from chassis ground to signal ground.	Typical values range from 0.1 µF to 4.7 µF. Determine experimentally.
LED Circuits	Add sites for capacitors on LED lines.	Use 3.3V AUX for designs supporting wakeup. Add approximately one capacitor per LED for EMI. Suggested starting value 470 pF.
	Add current limiting resistors to LED paths.	Typical current limiting resistors are 300-330 Ω when using a 3.3V supply. Current limiting resistors are frequently included with integrated magnetics modules.
	Verify LEDA_RX_ACTIVITY has a test header.	Connect a two-pin header to the LEDA_RX_ACTIVITY pin for IEEE PHY conformance testing. The other header pin should go to GND.
		For production applications, all test points may be deleted and signal pins may be left unconnected.
	Verify LEDB_RX_ACTIVITY has a test header.	Connect a two-pin header to the LEDB_RX_ACTIVITY pin for IEEE PHY conformance testing. The other header pin should go to GND.
		For production applications, all test points may be deleted and signal pins may be left unconnected.
Mfg Test	82563EB device uses a 3.3V JTAG Test Access Port.	The TAP controller uses internal reset instead of an external pin.
	Connect JTAG_TCK to GND through a 1 K to 10 K Ω resistor.	JTAG_TMS and JTAG_TDI have internal pull-ups, so they don't need the external pull-up resistors

10.2 Board Layout and Placement Checklist

SECTION	CHECK ITEMS	REMARKS
General	Have up-to-date product documentation and spec updates.	Documents are subject to frequent change.
	Route the Kumeran and MDI differential traces before routing the digital traces.	Layout of differential traces is critical.
Ethernet Device	Place the silicon at least 1 inch from the edge of the board.	With closer spacing, the strongest fields do not have path to GND and may cause EMI problems.
	Place PHY_REF compensation resistor less than 1 inch from the silicon.	
	Place the PHY_CLK_OUT series resistor within 2 inches of the 82563EB/82564EB.	Use PHY_CLK_OUT only if the routed length between the 82563EB/82564EB and the 631xESB/632xESB is less than 15 inches. The 40 Ω series resistor is required for signal integrity. If the routed length between 82563EB/82564EB and the 631xESB/632xESB is greater than 15 inches, then PHY_CLK_OUT must be a no connect. Instead, use an oscillator clock source at the 631xESB/632xESB.
	Route the serial clock as a 50 Ω single-ended impedance (± 20%).	Controlled impedance is required to reduce ringing and improve signal quality at the 50 Ω input to the 631xESB/632xESB. Keep 15 mil spacing to digital traces, I/O ports, and board edge. More spacing may be required to other high speed traces or clocks.
Clock Source	Place crystal and load capacitors less than 0.75 inches from Ethernet device.	The Ethernet clock plays a key role in EMI.
	Keep clock lines 15 mils away from other signals.	This includes spacing to other digital traces, I/O ports, board edge, transformers and differential pairs.
	Crystal traces are 12 mil width.	12 mil width is the best compromise of low inductance and low capacitance.
MDI Differential Pairs	Design traces for 100 Ω differential impedance (± 20%).	Primary requirement for 10/100/1000 Mb/s Ethernet. Paired 50 Ω traces do not make 100 Ω differential. Check impedance calculator.
	Place the silicon at least 1 inch from the integrated magnetics module but less than 4 inches.	With closer spacing, fields can follow the surface of the magnetics module or wrap past edge of board, increasing EMI. If the board does not have power and ground planes along the edge, the problem could be worse. Larger spacing increases the insertion loss of the MDI signals and decreases amplitude which may cause IEEE failures. Optimum location is approximately 1 inch behind the magnetics module.

SECTION	CHECK ITEMS	REMARKS
MDI Differential Pairs	Avoid highly resistive traces, for example, 4 mil traces longer than 4 inches.	If trace length is a problem, use thicker board dielectrics to allow wider traces. Thicker copper is even better than wider traces.
	Make traces symmetrical.	Try to match the pairs at pads, vias and turns. Establish rules carefully for the autorouter. Asymmetry contributes to impedance mismatch.
	Do not make 90° bends.	Bevel corners with turns based on 45° angles
	Minimize through holes (vias).	If using through holes (vias), the budget is two 10 mil finished hole size vias per trace.
	Keep trace-to-trace length difference within each pair to less than 50 mils.	Minimizes signal skew and common mode noise. Improves long cable performance.
	Pair-to-pair differences in length are not critical.	Keep differences under approximately 2 inches. A 25% difference in length from longest pair to shortest pair is typical.
	Keep differential pairs 30 mils or more away from each other and away from parallel digital traces.	Minimizes crosstalk and noise injection. Guard traces are generally not recommended and will reduce the impedance if done incorrectly.
	Keep traces away from the board edge.	If the component or MDI traces are near the board edge, EMI could increase.
	Route traces on appropriate layers.	Run pairs on different layers as needed to improve routing. For two port designs, try to route no more than 4 pairs per layer. Use layers adjacent to ground or power layers if possible. When differential signals transition from one board layer to another, place ground vias within 40 mils of the signal vias. Make sure digital signals on adjacent layers cross at 90° angles.
	Place MDI termination resistors and capacitors less than 0.5 inches from the Ethernet device.	Prevents reflections. Use symmetrical pads. Minimize any stubs.
Magnetics Module	Capacitors connected to center taps should be placed less than 0.1 inch to magnetics module.	Placement contributes directly to IEEE performance.
	Deliver 1.9V to the magnetic center tap with a plane.	Narrow finger-like planes and very wide traces are allowed. If using traces, aim for 100 mils (minimum). Planes are lower inductance and lower resistance than traces and provide better IEEE performance.
Kumeran Transmit and Receive Interface	Design traces for 100 Ω differential impedance (± 20%).	Paired 50 Ω traces do not make 100 Ω differential. Check impedance calculator.
	Long traces are allowed up to 28 inches, but avoid highly resistive traces.	For long distances, thick traces are preferred over wide traces. Modify board stackup if necessary to avoid highly resistive traces. Traces should be routed diagonal to the FR4 weave to maintain consistent impedance.

SECTION	CHECK ITEMS	REMARKS
Kumeran Transmit and Receive Interface		For differential traces that will be longer than 15 inches, the dielectric height under microstrip traces and the dielectric heights above/below stripline traces should be >= 4.3 mils nominal. For long distances, thick traces are preferred over wide trac If 1 oz copper is used, minimim trace spacing within each differential pair must be >= 8 mils.
	Make traces symmetrical	Try to match the pairs at pads, vias and turns. Establish rules carefully for the autorouter. Asymmetry contributes to impedance mismatch.
	Do not make 90° bends	Bevel corners with turns based on 45° angles
	Minimize through holes (vias).	If using through holes (vias), the budget is two 10 mil finished hole size vias per trace.
	Keep traces close together within differential pairs.	6-9 mil spacing is best to maximize coupling effects. If spacing is less than 6 mils, it is almost impossible to achieve > 90 Ω differential impedance.
	Keep trace-to-trace length difference within each pair to less than 10 mils.	Minimizes signal skew and reduces common mode conversion.
	Keep Kumeran differential pairs approximately 30 mils or greater away from each other.	Minimizes crosstalk and noise injection. This includes spacing to other digital traces, I/O ports, board edge, transformers and differential pairs. If differential traces are less than 15 inches in length, keep adjacent traces away by at least 6X the dielectric thickness. For example, 4.5 mil thick FR4; spacing >= 27 mils. If differential traces are greater than 15 inches in length, keep adjacent traces away by at least 7X the dielectric thickness. For example, 4.5 mil thick FR4; spacin >= 31.5 mils.
	Keep traces greater than 0.1 inch from the board edge.	Reduces EMI.
	Avoid unused pads and stubs along the traces.	Use zero Ω resistors sparingly if needed.
	Route traces on appropriate layers always referenced to GND.	Run pairs on different layers as needed to improve routing. Use layers adjacent to ground layers. There must be no splits in the GND planes. When differential signals transition from one board layer to another, place ground vias within 40 mils of the signal vias. If the differential signals transition from a ground referenced layer to a power referenced layer, place a decoupling cap on the power and ground within 40 mils of the signal vias. Avoid broadside coupling to traces on other layers. The broadside effect will significantly increase the insertion loss and reduce signal quality.

SECTION	CHECK ITEMS	REMARKS
Kumeran Transmit and Receive Interface		Make sure digital signals on adjacent layers cross at 90° angles.
	For the Kumeran interface, place AC coupling capacitors close to the receivers.	The AC coupling is always at the receiver on the Kumeran interface.
Power Supply and Signal Ground	Keep the routed length of the CTRL_12 and CTRL_18 signals to the external PNP transistors less than 2 inches.	Reduces oscillation and ripple in the power supply.
	Route the CTRL_12 and CTRL_18 signals as 12 mil wide traces.	Low inductance and low capacitance feedback paths reduce oscillations and ripple in the power supply.
	Keep CTRL_12 and CTRL_18 lines greater than 10 mils away from other signals.	This includes spacing to other digital traces, I/O ports, board edge, transformers and differential pairs
	Use planes to deliver power.	Narrow finger-like planes and very wide traces are allowed. If using traces, aim for 100 mils (minimum). Planes are lower inductance and lower resistance than traces.
	Use decoupling and bulk capacitors generously.	Place decoupling and bulk capacitors close to Ethernet device, with some along every side, using short, wide traces and large vias. If power is distributed on traces, bulk capacitors should be used at both ends.
	Each of the 1.2V and 1.9V PNP transistors require 1/2 inch x 1/2 inch thermal relief plane on layer 1.	The extra copper on layer 1 reduces the Theta-ja of the transistor which improves the power dissipation. Shape is not important, but surface area is important. Connect the thermal relief to the ground plane with 5 vias to minimize the inductance in the power delivery circuit.
	Two 1 Ω 0.25 W resistors should be placed in parallel in the collector path of the PNP for the 1.2V and 1.9V regulators.	These resistors are required for heat dissipation on the 82563EB. These resistors are optional, but recommended, for the 82564EB.
	If using decoupling capacitors on LED lines, place them carefully.	Capacitors on LED lines should be placed near the LEDs (typically adjacent to integrated magnetics module).
Chassis Ground	If possible, provide a separate chassis ground “island” to ground the shroud of the RJ-45 connector and to terminate the line side of the magnetics module. This design improves EMI behavior.	Split in ground plane should be at least 50 mils. Split should run under center of magnetics module. Differential pairs never cross the split.
	Place 4-6 pairs of pads for “stitching” capacitors to bridge the gap from chassis ground to signal ground.	Determine exact number and values empirically based on EMI performance. Expect to populate approximately two capacitor sites.

SECTION	CHECK ITEMS	REMARKS
Landing Pattern	Make sure that the 82563EB/82564EB has a good connection to ground.	Check for solder voids on the Exposed-Pad,* solder wicking, or a complete lack of solder. Failure to ensure a good connection to ground might cause link-up problems.
LED Circuits	Keep LED traces away from sources of noise, for example, high speed digital traces running in parallel.	LED traces can carry noise into integrated magnetics modules, RJ-45 connectors, or out to the edge of the board, increasing EMI.

10.3 Validation Checklist

SECTION	CHECK ITEMS	REMARKS
General	Have up-to-date product documentation and spec updates.	Documents are subject to frequent change
Power Supplies	Observe the startup behavior of the voltage regulators.	All voltages meet the specifications outlined in the datasheet and design guide.
	Measure the ripple on the 3.3V, 1.2V and 1.9V supplies.	Ripple should meet the specification outlined in the datasheet.
Clock Source	Test the startup characteristics of the crystal oscillator.	Test across the full range of voltage and temperature.
	Measure the frequency accuracy. Tune the external load capacitors until the frequency accuracy is within ±10% of the target frequency. The practical range of capacitors is approximately 16 pF to 33 pF.	The frequency may be measured at LEDA_RX_ACTIVITY for Port A and LEDB_RX_ACTIVITY for Port B. Test setup is critical. Make measurements on multiple systems using a representative sample of crystals. Contact Intel for details.
Ethernet Device	Perform IEEE PHY conformance testing for 10/100/1000 copper-based Gigabit Ethernet.	Key tests are: Bit Error Rate; Output Amplitude, Rise and Fall Time, Symmetry and Droop; Return Loss; and Jitter. Contact Intel for detailed test information.
	Perform equivalent Kumeran testing.	Key tests are: Bit Error Rate; Jitter, Amplitude (measured at receivers); and Eye Pattern Opening. Keep in mind that the Kumeran outputs on the Ethernet Physical Layer Device use pre-emphasis.

11.0 Reference Schematic

Reference schematics describing a typical design layout for the 82563EB/82564EB Gigabit Ethernet Platform LAN Connect can be found in the Bensley/Bensley-VS Platform Design Guide (PDG).

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12.0 System Manageability

Refer to the *82571/82572/631xESB/632xESB System Manageability Application Note* (AP-497) for information about the pass through modes that enable an external Baseboard Management Controller (BMC) or TCO controller to communicate with 631xESB/632xESB I/O Controller Hub using a TCO port. The TCO port supports both SMBus and I^2C commands to pass traffic to and from an external BMC.

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Appendix A Measuring LAN Reference Frequency Using a Frequency Counter

A.1 Background

To comply with IEEE specifications for 10/100 Mbps and 10/100/1000Base-T Ethernet LAN, the transmitter reference frequency must be correct and accurate within ±50 parts per million (ppm).

Note: Intel recommends a frequency tolerance of ±30 (ppm).

Most Intel LAN devices will operate properly with a 25.000 MHz reference crystal, provided it meets the recommended requirements for frequency stability, equivalent series resistance at resonance (ESR), and load capacitance.

Most circuits for series resonant crystals include two discrete capacitors (typically C1 and C2), with values between 5 pF and 36 pF.

The most accurate way to determine the appropriate value for the discrete capacitors is to install the approximately correct values for C1 and C2. Next, a frequency counter should be used to measure the transmitter reference frequency (or transmitter reference clock).

- If the transmitter reference frequency is more than 20 ppm below the target frequency, then the values for C1 and C2 are too big and should be decreased.
- If the transmitter reference frequency is more than 20 ppm above the target frequency, then the values for C1 and C2 are too small and should be increased.

This Appendix provides instructions and illustrations that explain how to use a frequency counter and probe to determine the Ethernet LAN device transmit center frequency. An example describing how to calculate the frequency accuracy of the measured and averaged center frequency with respect to the target center frequency is also included.

A.2 Required Test Equipment

Tektronix CMC-251, or similar high resolution, digital counter

Tektronix P6246, or similar high bandwidth, low capacitance (less than 1 pF) probe

Tektronix 1103, or similar probe power supply or probe amplifier

BNC, 50-ohm coaxial cable (less than 6 feet long)

System with power supply and test software for the LAN circuit to be tested

A.3 Indirect Probing Method

The indirect probing test method is applicable foremost devices that support 100BASE-T. Since probe capacitance can load the reference crystal and affect the measured frequency, the preferred method is to use the indirect probing test method when possible.

Almost all Intel LAN silicon that support 1000BASE-T Ethernet can provide a buffered 125 MHz clock, which can be used for indirect probing of the transmitter reference clock. The buffered 125 MHz clock will be a 5X multiple of the crystal circuit's reference frequency (Figure 20).

Different LAN devices may require different register settings, to enable the buffered 125 MHz reference frequency. Please obtain the settings or instructions that are appropriate for the LAN device you are using.

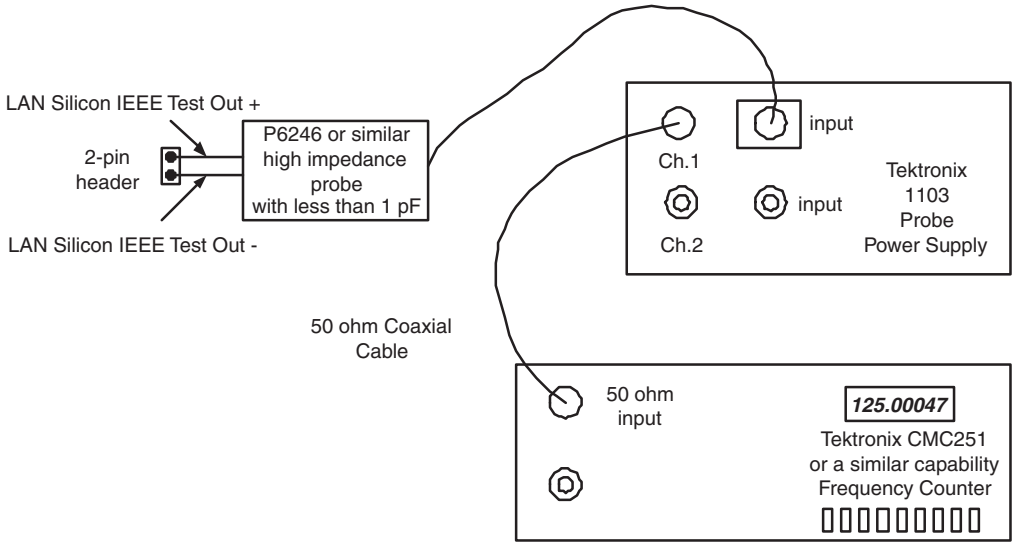

Figure 20. Indirect Probing Setup

A.4 Indirect Frequency Measurement and Frequency Accuracy Calculation Steps

1. Make sure the system BIOS has the LAN device enabled.
2. Connect the test equipment as shown in Figure 20.
3. Using the appropriate controls for your model of high resolution digital counter, make sure it can display ~125.0000 MHz with at least four decimal places frequency resolution.
4. Enable the 125 MHz buffered reference clock.
5. Determine the center reference frequency as accurately as possible. This can be done by taking 30 to 50 different readings using the frequency counter and then calculating the average results of the readings.
6. Calculate the accuracy of the measured and averaged center frequency with respect to an ideal 125.0000 MHz reference frequency.

$$FrequencyAccuracy(ppm) = \frac{(x - y)}{(y / 1000000)}$$

where x = Average measured frequency in Hertz and
y = Ideal reference frequency in Hertz

Example 1.

Given: The measured averaged center frequency is 124.99942 MHz (or 124,999,420 Hertz).

$$FrequencyAccuracy(ppm) = \frac{(124999420 - 125000000)}{(125000000 / 1000000)} = -4.64ppm$$

Example 2.

Given: The measured averaged center frequency is 125.00087 MHz (or 125,000,870 Hertz).

$$FrequencyAccuracy(ppm) = \frac{(125000870 - 125000000)}{(125000000 / 1000000)} = 6.96ppm$$

Note: The following items should be noted for an ideal reference crystal on a typical printed circuit board.

- If the transmitter reference frequency is more than 8 ppm below the target frequency, then the values for C1 and C2 are too big and they should be decreased. When tests are performed across temperature, it may be acceptable for the center frequency deviation to be a little greater than 8 ppm.
- If the transmitter reference frequency is more than 8 ppm above the target frequency, then the values for C1 and C2 are too small and they should be increased. When tests are performed across temperature, it may be acceptable for the center frequency deviation to be a little greater than 8 ppm.

A.5 Direct Probing Test Method, Applicable for Most 10/100 Devices (Devices that do NOT support 1000Base-T)

Because probe capacitance can load the reference crystal affecting the measured frequency, it is preferable to use a probe with less than 1 pF capacitance.

The probe should be connected between the XTAL2 pin of the LAN device and a nearby ground. Typically, it is possible to connect the probe pins across one of the discrete load capacitors (C2 in Figure 21).

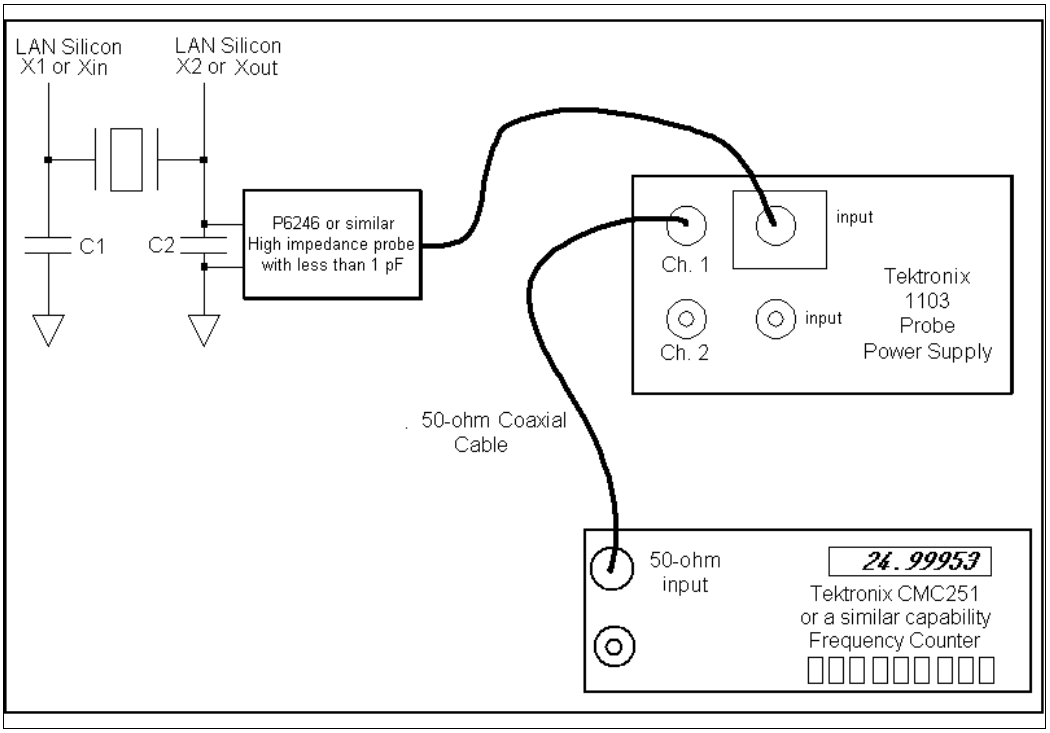

Figure 21. Direct Probing Method

A.6 Direct Frequency Measurement and Frequency Accuracy Calculation Steps

1. Make sure the system BIOS has the LAN device enabled.
2. Connect the test equipment as shown in Figure 21.
3. Using the appropriate controls for your model of high resolution digital counter, make sure it can display ~25.0000 MHz with at least four decimal places frequency resolution.
4. Ensure the LAN circuits are powered.
5. Determine the center reference frequency as accurately as possible. This can be done by taking 30 to 50 different readings using the frequency counter and then calculating the average results of the readings.
6. Calculate the accuracy of the measured and averaged center frequency with respect to an ideal 25.0000 MHz reference frequency.

$$FrequencyAccuracy(ppm) = \frac{(x-y)}{(y/1000000)}$$

where x = Average measured frequency in Hertz and
y = Ideal reference frequency in Hertz

Example 1.

Given: The measured averaged center frequency is 24.99963 MHz (or 24,999,630 Hertz).

$$FrequencyAccuracy(ppm) = \frac{(24999630-25000000)}{(25000000/1000000)} = -14.8ppm$$

Example 2.

Given: The measured averaged center frequency is 25.00027 MHz (or 25,000,270 Hertz).

$$FrequencyAccuracy(ppm) = \frac{(25000270-25000000)}{(25000000/1000000)} = 10.8ppm$$

Note: The following items should be noted for an ideal reference crystal on a typical printed circuit board.

- If the transmitter reference frequency is more than 8 ppm below the target frequency, then the values for C1 and C2 are too big and they should be decreased. When tests are performed across temperature, it may be acceptable for the center frequency deviation to be a little greater than 8 ppm.
- If the transmitter reference frequency is more than 8 ppm above the target frequency, then the values for C1 and C2 are too small and they should be increased. When tests are performed across temperature, it may be acceptable for the center frequency deviation to be a little greater than 8 ppm.

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