82562EZ(EX)/82551QM & 82540EM Combined Footprint LOM Design Guide

Application Note

Networking Silicon

317503-001
Revision 1.7

Revision History

Revision	Revision Date	Description
0.75	Jan 2002	Preliminary Draft
0.80	August 2002	Revised pin assignments: E1, E12, G5, G6, G13, H5, H6, H7, H8, H11, J5, J6, J7, J8, J9, J10, J11, K5, K6, K7, K8, K9, K10, K11, L4, L5, L9, L10.
1.0	April 2003	Non-classified release. Section 1.0. Added product ordering codes.
1.1	September 2003	Appended reference schematics.
1.2	November 2004	Updated reference schematics to reflect MDI-X feature (82551QM only). Added crystal start-up information. Information includes: • New crystal parameters • Crystal selection guidelines • Crystal validation methods • Crystal testing methods Added new values for TX and RX terminations (next to LAN silicon). New values are now 110 Ω for both TX and RX terminations. Added new starting values for RBIAS100 and RBIAS10. New starting values are now 649 Ω for RBIAS100 and 619 Ω for RBIAS10. Updated reference schematics to reflect new Tx and Rx termination values, new LAN disable circuit, RBIAS100/RBIAS10 values, VIO signaling connection and pullup resistor value. Changed pin A13 output resistor value from 3.3K Ω to 1K Ω.
1.3	January 2005	• Changed text in the Catalyst EEPROM revision H table note from “Revision H or higher not supported” to “Revision H is not supported”. • Added a 0.01 µf capacitor between Ball C2 (M66EN) and ground to meet IEEE PCI specification (sheet 3 of reference schematics). • Removed the Self-Review Checklist for Combined Footprint LOM. This checklist is now a separate Microsoft* Excel spreadsheet.
1.4	January 2005	Updated reference schematics to: • Reflect current differential pair termination resistor values for the 82540EM. • Removed 0.01µf capacitors attached between center nodes and ground (82562EZ/EX and 82551QM only). • Removed center tap connection to VCC 2.5 V (82562EZ/EX and 82551ER/IT only). Added Section 5.1.2.1 “Terminating Differential Pairs for 82562EZ/EX and 82551QM-Based Designs”. Added Section 5.1.2.2 “Terminating Differential Pairs for 82540EM-Based Designs”.
1.5	August 2005	Removed all references to the LAN Disable circuit for the 82540EM. Affected areas include: • Section “82540EM Ethernet Controller LAN Disable Guidelines” (removed). • Figure 3 ”82540EM LAN Disable Circuitry” (removed). • Page 8 of the Reference Schematics (updated). Page 8 is applicable only to the 82562EZ(EX).
1.6	July 2006	Added a LAN Disable solution note to section 4.2.1.
1.7	January 2008	Updated reference schematic pages: sheet 2, 4, 5, and 6.

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1.0 Introduction

The 82540EM Gigabit Ethernet Controller, the 82551QM Fast Ethernet Controller, and the 82562EZ(EX) Fast Ethernet Controller are all manufactured in a footprint compatible 15 mm x 15 mm, 196-ball grid array package. Many of the critical signal pin locations on the 82540EM and 82551QM are identical to signals on the 82562EZ(EX) allowing designers to create a single design that accommodates these three parts. Because the usage of some pins on the 82540EM differ from the usage on the 82551QM and the 82562EZ(EX), the three parts are not referred to as "pin compatible". The term "footprint compatible" refers to the fact that the parts share the same package size, same number and pattern of pins, and layout of signals that allow for the flexible, cost effective, multipurpose design. As a result, it is easy to populate a single board design with any of the three parts to maximize value matching your customers' performance needs.

1.1 Scope

This application note identifies the design differences between the 82540EM, 82551QM, and 82562EZ(EX). The table in Section 8.0 lists the stuffing (population) options for the three parts.

For other necessary design collateral, please refer to “Reference Documents” (Section 1.2).

1.2 Reference Documents

This application note assumes that the designer is acquainted with high-speed design and board layout techniques. The following documents provide additional information:

- 82540EM Datasheet, Intel Corporation.
- 82551QM Datasheet, Intel Corporation.
- 82562EZ 10/100 Mbps Platform LAN Connect (PLC) Networking Silicon Datasheet, Intel Corporation.
- I/O Control Hub 2, 3, and 4 EEPROM Map and Programming Information, Intel Corporation.
- I/O Control Hub 5, 6, and 7 EEPROM Map and Programming Information, Intel Corporation.
- 82551QM/ER/IT EEPROM Map and Programming Information Guide, Intel Corporation
- 82540EM and 82540EP EEPROM Map and Programming Information, Intel Corporation
- PCI Local Bus Specification, Revision 2.2 and 2.3, PCI Special Interest Group
- PCI Bus Power Management Interface Specification, Rev. 1.1, PCI Special Interest Group
- IEEE Standard 802.3, 1996 Edition, Institute of Electrical and Electronics Engineers
- IEEE Standard 802.3u, 1995 Edition, Institute of Electrical and Electronics Engineers
- IEEE Standard 802.3x, 1997 Edition, Institute of Electrical and Electronics Engineers
- IEEE Standard 802.3z, 1998 Edition, Institute of Electrical and Electronics Engineers
- IEEE Standard 802.3ab, 1999 Edition, Institute of Electrical and Electronics Engineers
- Oscillation Circuit Design Guide Application Note, Epson Electronics America, Inc. (www.eea.epson.com).
- Quartz Crystal Theory of Operation and Design Notes. Fox Electronics (www.foxonline.com).

- Crystal Technical Glossary. Fox Electronics.
- Crystal Frequently Asked Questions. Fox Electronics.
- Resonator Terminology and Formulas. Piezo Technology, Inc. (www.piezotech.com).

1.3 Product Codes

Table 1 lists the product ordering codes for the 82562EZ(EX), 82551QM, and 82540EM.

Table 1. Product Ordering Codes

Device	Product Code	Product Code (Lead Free)
82562EZ	GD82562EZ	LU82562EZ
82562EX	GD82562EX	LU82562EX
82551QM	GD82551QM	LU82551QM
82540EM	RC82540EM	LU82540EM

2.0 Frequency Control Device Design Considerations

This section provides information regarding frequency control devices, including crystals and oscillators, for use with all Intel® Ethernet controllers. Several suitable frequency control devices are available; none of which present any unusual challenges in selection. The concepts documented herein are applicable to other data communication circuits, including Physical Layer devices (PHYs).

The Intel® Ethernet controllers contain amplifiers which, when used with the specific external components, form the basis for feedback oscillators. These oscillator circuits, which are both economical and reliable, are described in more detail in “Crystal Selection Parameters”.

The Intel® Ethernet controllers also have bus clock input functionality, however a discussion of this feature is beyond the scope of this document, and will not be addressed.

The chosen frequency control device vendor should be consulted early in the design cycle. Crystal and oscillator manufacturers familiar with networking equipment clock requirements may provide assistance in selecting an optimum, low-cost solution.

2.1 Frequency Control Component Types

Several types of third-party frequency reference components are currently marketed. A discussion of each follows, listed in preferred order.

2.2 Quartz Crystal

Quartz crystals are generally considered to be the mainstay of frequency control components due to their low cost and ease of implementation. They are available from numerous vendors in many package types and with various specification options.

2.3 Fixed Crystal Oscillator

A packaged fixed crystal oscillator is comprised of an inverter, a quartz crystal, and passive components conveniently packaged together. The device renders a strong, consistent square wave output. Oscillators used with microprocessors are supplied in many configurations and tolerances.

Crystal oscillators should be restricted to use in special situations, such as shared clocking among devices or multiple controllers. As clock routing can be difficult to accomplish, it is preferable to provide a separate crystal for each device.

For Intel® Ethernet controllers, it is acceptable to overdrive the internal inverter by connecting a 25 MHz external oscillator to the X1 lead, leaving the X2 lead unconnected. The oscillator should be specified to drive CMOS logic levels, and the clock trace to the controller should be as short as possible. Controller specifications typically call for a 40% (minimum) to 60% (maximum) duty cycle and a ±50 ppm frequency tolerance.

Note: Please contact your Intel Customer Representative to obtain the most current device documentation prior to implementing this solution.

2.4 Programmable Crystal Oscillators

A programmable oscillator can be configured to operate at many frequencies. The device contains a crystal frequency reference and a phase lock loop (PLL) clock generator. The frequency multipliers and divisors are controlled by programmable fuses.

A programmable oscillator's accuracy depends heavily on the Ethernet controller's differential transmit lines. The Physical Layer (PHY) uses the clock input from the device to drive a differential Manchester (for 10 Mbps operation), an MLT-3 (for 100 Mbps operation) or a PAM-5 (for 1000 Mbps operation) encoded analog signal across the twisted pair cable. These signals are referred to as self-clocking, which means the clock must be recovered at the receiving link partner. Clock recovery is performed with another PLL that locks onto the signal at the other end.

PLLs are prone to exhibit frequency jitter. The transmitted signal can also have considerable jitter even with the programmable oscillator working within its specified frequency tolerance. PLLs must be designed carefully to lock onto signals over a reasonable frequency range. If the transmitted signal has high jitter and the receiver's PLL loses its lock, then bit errors or link loss can occur.

PHY devices are deployed for many different communication applications. Some PHYs contain PLLs with marginal lock range and cannot tolerate the jitter inherent in data transmission clocked with a programmable oscillator. The American National Standards Institute (ANSI) X3.263-1995 standard test method for transmit jitter is not stringent enough to predict PLL-to-PLL lock failures, therefore, the use of programmable oscillators is generally not recommended.

2.5 Ceramic Resonator

Similar to a quartz crystal, a ceramic resonator is a piezoelectric device. A ceramic resonator typically carries a frequency tolerance of ±0.5%, – inadequate for use with Intel® Ethernet controllers, and therefore, should not be utilized.

3.0 Crystal Selection Parameters

All crystals used with Intel® Ethernet controllers are described as "AT-cut," which refers to the angle at which the unit is sliced with respect to the long axis of the quartz stone.

Table 2 lists the crystal electrical parameters and provides suggested values for typical designs. These parameters are described in the following subsections.

Table 2. Crystal Parameters

Parameter	Suggested Value
Vibrational Mode	Fundamental
Nominal Frequency	25.000 MHz at 25° C (required)
Frequency Tolerance	• ±30 ppm recommended • ±50 ppm across the entire operating temperature range (required by IEEE specifications)
Temperature Stability	±50 ppm at 0° C to 70° C
Calibration Mode	Parallel
Load Capacitance	16 pF to 20 pF
Shunt Capacitance	6 pF maximum
Equivalent Series Resistance	50 Ω maximum
Drive Level	0.5 mW maximum
Aging	±5 ppm per year maximum

3.1 Vibrational Mode

Crystals in the above-referenced frequency range are available in both fundamental and third overtone. Unless there is a special need for third overtone, use fundamental mode crystals.

At any given operating frequency, third overtone crystals are thicker and more rugged than fundamental mode crystals. Third overtone crystals are more suitable for use in military or harsh industrial environments. Third overtone crystals require a trap circuit (extra capacitor and inductor) in the load circuitry to suppress fundamental mode oscillation as the circuit powers up. Selecting values for these components is beyond the scope of this document.

3.2 Nominal Frequency

Intel® Ethernet controllers use a crystal frequency of 25.000 MHz. The 25 MHz input is used to generate a 125 MHz transmit clock for 100BASE-TX and 1000BASE-TX operation – 10 MHz and 20 MHz transmit clocks, for 10BASE-T operation.

3.3 Frequency Tolerance

The frequency tolerance for an Ethernet physical layer device is dictated by the IEEE 802.3 specification as ±50 parts per million (ppm). This measurement is referenced to a standard temperature of 25° C. Intel recommends a frequency tolerance of ±30 ppm.

3.4 Temperature Stability and Environmental Requirements

Temperature stability is a standard measure of how the oscillation frequency varies over the full operational temperature range (and beyond). Several optional temperature ranges are currently available, including -40° C to +85° C for industrial environments. Some vendors separate operating temperatures from temperature stability. Manufacturers may also list temperature stability as 50 ppm in their data sheets.

Note: Crystals also carry other specifications for storage temperature, shock resistance, and reflow solder conditions. Crystal vendors should be consulted early in the design cycle to discuss the application and its environmental requirements.

3.5 Calibration Mode

The terms “series-resonant” and “parallel-resonant” are often used to describe crystal oscillator circuits. Specifying parallel mode is critical to determining how the crystal frequency is calibrated at the factory.

A crystal specified and tested as series resonant oscillates without problem in a parallel-resonant circuit, but the frequency is higher than nominal by several hundred parts per million. The purpose of adding load capacitors to a crystal oscillator circuit is to establish resonance at a frequency higher than the crystal’s inherent series resonant frequency.

Figure 1 illustrates a simplified schematic of the 82551QM’s oscillator circuit. Note that 82540EM controllers are similar. The crystal and the capacitors form a feedback element for the internal inverting amplifier. This combination is called parallel-resonant, because it has positive reactance at the selected frequency. In other words, the crystal behaves like an inductor in a parallel LC circuit. Oscillators with piezoelectric feedback elements are also known as “Pierce” oscillators.

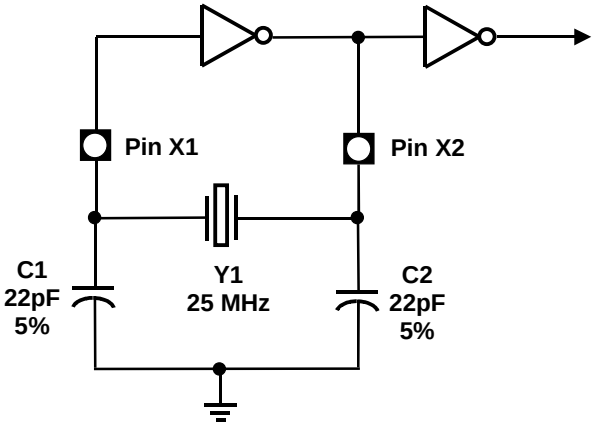

Figure 1. 82551QM Oscillator Circuit

3.6 Load Capacitance

The formula for crystal load capacitance is as follows:

$$C_L = \frac{(C1 \cdot C2)}{(C1 + C2)} + C_{stray}$$

where C1 = C2 = 22 pF (as suggested in most Intel reference designs)

and C_{stray} = allowance for additional capacitance in pads, traces and the chip carrier within the Ethernet controller package

An allowance of 3 pF to 7 pF accounts for lumped stray capacitance. The calculated load capacitance is 16 pF with an estimated stray capacitance of about 5 pF.

Individual stray capacitance components can be estimated and added. For example, surface mount pads for the load capacitors add approximately 2.5 pF in parallel to each capacitor. This technique is especially useful if Y1, C1 and C2 must be placed farther than approximately one-half (0.5) inch from the controller. It is worth noting that thin circuit boards generally have higher stray capacitance than thick circuit boards.

Standard capacitor loads used by crystal manufacturers include 16 pF, 18 pF and 20 pF. Any of these values will generally operate with the controller. However, a difference of several picofarads between the calibrated load and the actual load will pull the oscillator slightly off frequency.

The oscillator frequency should be measured with a precision frequency counter where possible. The 82551QM Fast Ethernet controller has a FLA16 signal output for this purpose. The load specification or values of C1 and C2 should be fine tuned for the design. As the actual capacitance load increases, the oscillator frequency decreases.

Note: C1 and C2 may vary by as much as 5% (approximately 1 pF) from their nominal values.

3.7 Shunt Capacitance

The shunt capacitance parameter is relatively unimportant compared to load capacitance. Shunt capacitance represents the effect of the crystal's mechanical holder and contacts. The shunt capacitance should equal a maximum of 6 pF (7 pF is also acceptable).

3.8 Equivalent Series Resistance

Equivalent Series Resistance (ESR) is the real component of the crystal's impedance at the calibration frequency, which the inverting amplifier's loop gain must overcome. ESR varies inversely with frequency for a given crystal family. The lower the ESR, the faster the crystal starts up. Use crystals with an ESR value of 50 Ω or better.

Note: Check the specific controller documentation carefully; some devices may have tighter ESR requirements.

3.9 Drive Level

Drive level refers to power dissipation in use. The allowable drive level for a Surface Mounted Technology (SMT) crystal is less than its through-hole counterpart, because surface mount crystals are typically made from narrow, rectangular AT strips, rather than circular AT quartz blanks.

Some crystal data sheets list crystals with a maximum drive level of 1 mW. However, Intel® Ethernet controllers drive crystals to a level less than the suggested 0.5 mW value. This parameter does not have much value for on-chip oscillator use.

3.10 Aging

Aging is a permanent change in frequency (and resistance) occurring over time. This parameter is most important in its first year because new crystals age faster than old crystals. Use crystals with a maximum of ±5 ppm per year aging.

3.11 Reference Crystal

The normal tolerances of the discrete crystal components can contribute to small frequency offsets with respect to the target center frequency. To minimize the risk of tolerance-caused frequency offsets causing a small percentage of production line units to be outside of the acceptable frequency range, it is important to account for those shifts while empirically determining the proper values for the discrete loading capacitors, C1 and C2.

Even with a perfect support circuit, most crystals will oscillate slightly higher or slightly lower than the exact center of the target frequency. Therefore, frequency measurements (which determine the correct value for C1 and C2) should be performed with an ideal reference crystal. When the capacitive load is exactly equal to the crystal's load rating, an ideal reference crystal will be perfectly centered at the desired target frequency.

3.11.1 Reference Crystal Selection

There are several methods available for choosing the appropriate reference crystal:

- If a Saunders and Associates (S&A) crystal network analyzer is available, then discrete crystal components can be tested until one is found with zero or nearly zero ppm deviation (with the appropriate capacitive load). A crystal with zero or near zero ppm deviation will be a good reference crystal to use in subsequent frequency tests to determine the best values for C1 and C2.

- If a crystal analyzer is not available, then the selection of a reference crystal can be done by measuring a statistically valid sample population of crystals, which has units from multiple lots and approved vendors. The crystal, which has an oscillation frequency closest to the center of the distribution, should be the reference crystal used during testing to determine the best values for C1 and C2.
- It may also be possible to ask the approved crystal vendors or manufacturers to provide a reference crystal with zero or nearly zero deviation from the specified frequency when it has the specified CLoad capacitance.

When choosing a crystal, customers must keep in mind that to comply with IEEE specifications for 10/100 and 10/100/1000Base-T Ethernet LAN, the transmitter reference frequency must be precise within ±50 ppm. Intel® recommends customers to use a transmitter reference frequency that is accurate to within ±30 ppm to account for variations in crystal accuracy due to crystal manufacturing tolerance. For information about measuring transmitter reference frequency, refer to Appendix A, “Measuring LAN Reference Frequency Using a Frequency Counter”.

3.11.2 Circuit Board

Since the dielectric layers of the circuit board are allowed some reasonable variation in thickness, the stray capacitance from the printed board (to the crystal circuit) will also vary. If the thickness tolerance for the outer layers of dielectric are controlled within ±17 percent of nominal, then the circuit board should not cause more than ±2 pF variation to the stray capacitance at the crystal. When tuning crystal frequency, it is recommended that at least three circuit boards are tested for frequency. These boards should be from different production lots of bare circuit boards.

Alternatively, a larger sample population of circuit boards can be used. A larger population will increase the probability of obtaining the full range of possible variations in dielectric thickness and the full range of variation in stray capacitance.

Next, the exact same crystal and discrete load capacitors (C1 and C2) must be soldered onto each board, and the LAN reference frequency should be measured on each circuit board.

The circuit board, which has a LAN reference frequency closest to the center of the frequency distribution, should be used while performing the frequency measurements to select the appropriate value for C1 and C2.

3.11.3 Temperature Changes

Temperature changes can cause the crystal frequency to shift. Therefore, frequency measurements should be done in the final system chassis across the system’s rated operating temperature range.

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4.0 Ethernet Component Design Guidelines

This section provides recommendations for selecting components and connecting special pins. The main design elements are the 82562EZ(EX) Platform LAN Connect device, the 82540EM Gigabit Ethernet Controller, and the 82551QM Fast Ethernet Controller, a magnetics module with RJ-45 connector, and a crystal clock source.

4.1 Designing with the 82562EZ(EX) Platform LAN Connect Device

This section provides design guidelines specific to the PLC device.

4.1.1 Power Supplies for 82562EZ(EX) PLC Implementations

The 82562EZ(EX) PLC device uses a single 3.3 V power supply. The 3.3 V supply must provide approximately 90 mA current for full speed operation. Standby power must be furnished in order to wake up from a power down.

4.1.2 82562EZ(EX) Device Test Capability

The device contains an XOR test tree mechanism for simple board tests. Details of the XOR tree operation are contained in the 82562ET LAN on Motherboard Design Guide.

4.1.3 82562EZ(EX) PCL Device LAN Disable Guidelines

Note: ICHx Integrated LAN Controller resides on the ICHx VccSus3_3 and VccSus1_8 power wells (typically referred to as “auxiliary” (“aux”) or “standby” supplies at the platform level).

The ICHx Integrated LAN’s RST# is the ICHx Resume-Well input. It can be held low indefinitely to keep the ICHx Integrated LAN Controller in a reset state. The LAN Reset (RST#) signal must not be de-asserted sooner than 10 ms after the Resume power supply reaches it nominal voltage. This ensures that the ICHx Integrated LAN Controller is initialized. Figure 2 illustrates a possible solution for ICHx Integrated LAN disable.

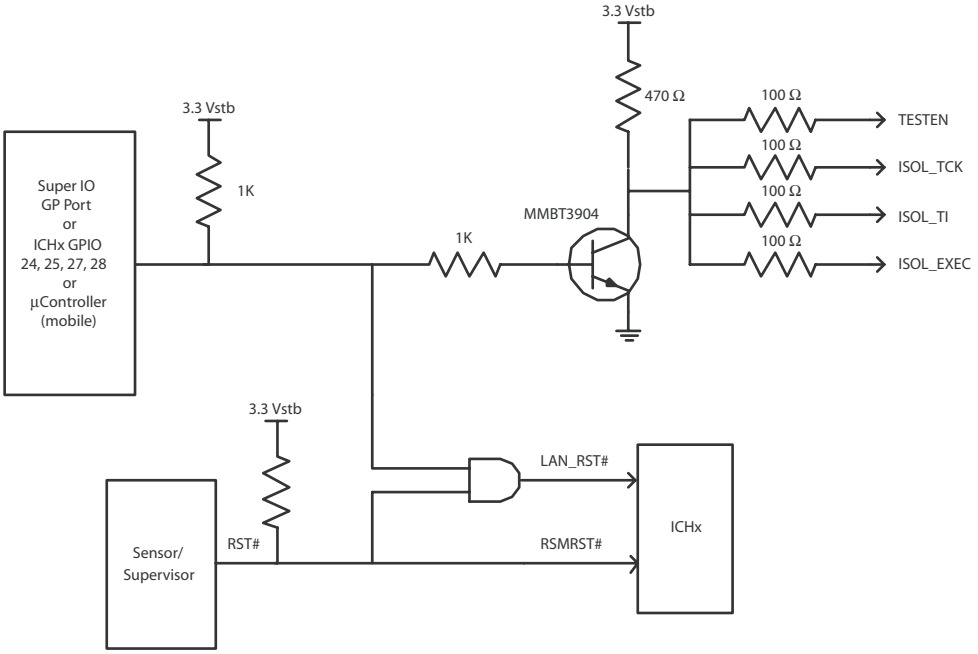


Figure 2. 82562EZ(EX) LAN Disable Circuitry

Note: The 100 Ω resistors for the Test Mode signals are required for the Exclusive OR (XOR) Tree and Isolate Mode.

4.2 Designing with the 82540EM Gigabit Controllers

This section provides design guidelines specific to the 82540EM Gigabit Ethernet Controllers.

4.2.1 Power Supplies for the 82540EM Controller

The 82540EM controller requires three power supplies: 1.5 V, 2.5 V, and 3.3 V. The 1.5 V supply must provide approximately 400 mA current, the 2.5 V supply approximately 145 mA current, and the 3.3 V supply approximately 125 mA current.

A central power supply can provide all the required voltage sources, or the power can be derived and regulated locally near the Ethernet control circuitry. All voltage sources must remain present during lower power states in order to use the 82540EM LAN wake up capability. This consideration makes it more likely that at least some of the voltage sources will be local.

Instead of using external regulators to supply 1.5 V and 2.5 V, power transistors can be used in conjunction with on-chip regulation circuitry. (See the reference schematic for an implementation example.)

The 82540EM controller has a LAN_PWR_GOOD input. Treat this signal as an external device reset which works in conjunction with the internal power-on reset circuitry. In the situation where a central power supply furnishes all the voltage sources, LAN_PWR_GOOD can be tied to the POWER_GOOD output of the power supply. Designs that generate some of the voltages locally can connect LAN_PWR_GOOD to a power monitor chip.

Note: The 82540EM does not support LAN Disable; however, A LAN Disable solution can be implemented by holding LAN_PWR_GOOD to 0b.

The power sources are all expected to ramp up during a brief power-up interval (approximately 20 ms) with LAN_PWR_GOOD de-asserted. The 82540EM controller must not be left in a prolonged state where some, but not all, voltages are applied. The 3.3 V source should be powered up prior to the 1.5 V or 2.5 V sources. The 1.5 V and 2.5 V power supplies may power up simultaneously. At any time during power up, the supply voltages must be: 1.5 V < 2.5 V < 3.3 V.

4.2.2 82540EM Controller Power Supply Filtering

The 82540EM controller switches relatively high currents at high frequencies, requiring generous use of both bulk capacitance and high speed decoupling capacitance adjacent to the device.

Bypass capacitors for each power rail should be 0.1 µF. If possible, orient the capacitors close to the device and adjacent to power pads. Decoupling capacitors should connect to the power and ground planes with short, thick traces (15 mils or 0.4 mm or more), and 14 mil (3.5 mm) vias per capacitor pad.

Furnish approximately 20 µF of bulk capacitance for each of the main 1.5 V and 2.5 V levels. This can be easily achieved by using two 10 µF capacitors, placing them as close to the device power connections as possible.

4.2.3 82540EM Controller Power Management and Wake Up

The 82540EM Gigabit Ethernet Controller supports low power operation as defined in the PCI Bus Power Management Specification. There are two defined power states, D0 and D3. The D0 state provides full power operation and is divided into two sub-states: D0u (uninitialized) and D0a (active). The D3 state provides low power operation and is also divided into two sub-states: D3hot and D3cold.

To enter the low power state, the software driver must stop data transmission and reception. Either the operating system or the driver must program the Power Management Control/Status Register (PMCSR) and the Wakeup Control Register (WUC). If wakeup is desired, the appropriate wakeup LAN address filters must also be set. The initial power management settings are specified by EEPROM bits.

When the 82540EM controller transitions to either of the D3 low power states, the 1.5 V, 2.5 V, and 3.3 V sources must continue to be supplied to the device. Otherwise, it will not be possible to use a wakeup mechanism. The AUX_POWER signal is a logic input to the 82540EM controller that denotes auxiliary power is available. If AUX_POWER is asserted, the 82540EM device will advertise that it supports wake up from a D3cold state.

The 82540EM device supports both Advanced Power Management (APM) wakeup and Advanced Configuration and Power Interface (ACPI) wakeup. APM wakeup has also been known in the past as “Wake on LAN.”

Wakeup uses the PME# signal to wake the system. PME# is an active low signal connected to a GPIO port on the ICH5 that goes active in response to receiving a Magic Packet*, a network wake-up packet, or link status change indication. PME# remains asserted until it is disabled through the Power Management Control/Status Register.

4.2.4 82540EM Device Test Capability

The 82540EM Gigabit Ethernet Controller contains a test access port conforming to the IEEE 1149.1a-1994 (JTAG) Boundary Scan specification. To use the test access port, these balls need to be connected to pads accessible by the test equipment. The TRST# input also needs to be connected to ground through a pull-down resistor (approximately 100 Ω) so that the test capability cannot be invoked by mistake.

A Boundary Scan Definition Language (BSDL) file describing the 82540EM device is available for use in your test environment.

The controller also contains an XOR test tree mechanism for simple board tests. Details of XOR tree operation may be obtained through your Intel representative.

5.0 PCB Routing Guidelines

5.1 Critical Dimensions for Discrete Magnetics Module and RJ-45

There are four critical dimensions that must be considered during the layout phase of an 82540EM, 82551QM, and 82562EZ(EX) LAN On Motherboard (LOM) implementation. These dimensions are identified in Figure 3 as A, B, C and D.

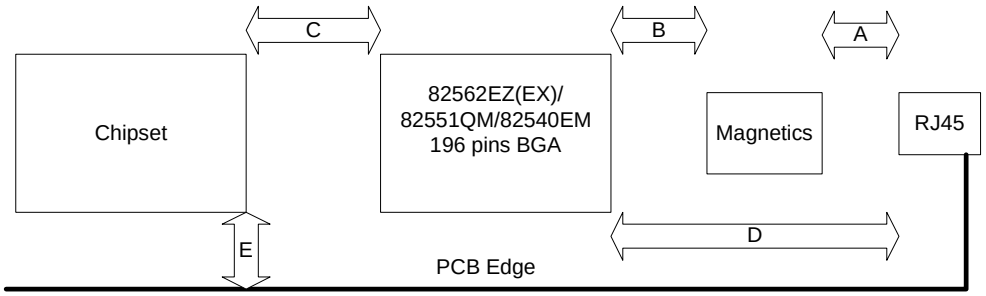


Figure 3. Critical Dimensions for 82562EZ(EX), 82551QM and 82540EM Component Placement

5.1.1 Distance A: Magnetics to RJ-45

The distance labeled “A” in Figure 1 should be given highest priority in board layout. The distance between the magnetics and RJ-45 should be less than 1 inch of separation. The following trace characteristics are important and should be observed.

- Differential Impedance: The differential impedance should be 100 Ω. The single ended trace impedance will be approximately 50 Ω; however, the differential impedance can also be affected by the spacing between the traces.
- Trace Symmetry: Differential pairs should be routed with consistent separation and with exactly the same lengths and physical dimensions.

5.1.2 Distance B: LAN Controller to Magnetics

The distance labeled “B” should also be designed to be less than one inch between devices. The high-speed nature of the signals propagating through the traces requires that the distance between these components be closely observed. In general, any section of traces intended for use with high-speed signals should observe proper termination practices. Proper termination of signals can reduce reflections caused by impedance mismatches between device and traces.

5.1.2.1 Terminating Differential Pairs for 82562EZ(EX) and 82551QM-Based Designs

Two differential pairs are terminated using 54.9 Ω (1% tolerance) resistors, placed near the LAN controller. One resistor connects to the MDI+ (MDI positive) signal trace and another resistor connects to the MDI- (MDI negative) signal trace.

Termination resistor values were recently increased from 49.9 Ω to 54.9 Ω to improve return loss. However, on some designs, this change caused the PCB's output amplitude to be slightly above the peak-to-peak center of the IEEE specification. As a result, RBIAS resistor values were increased (RBIAS10 549 to 619 Ω and RBIAS100 619 to 649 Ω) to reduce the PCB's output amplitude to better meet the IEEE peak-to-peak center specification.

For 100Base-TX designs, the IEEE specification allows a -950 mVpk to -1050 mVpk for the negative peak and +950 mVpk to +1050 mVpk for the positive peak. Ideally, a typical PCB output amplitude should be within -975 mVpk to -1025 mVpk for the negative peak and +975 mVpk to +1025 mVpk for the positive peak.

For 10Base-T designs, the IEEE specification allows a -2.2 mVpk to -2.8 mVpk for the negative peak and +2.2 mVpk to +2.8 mVpk for the positive peak. Ideally, a typical PCB output amplitude should be within -2.35 mVpk to -2.55 mVpk for the negative peak and +2.35 mVpk to +2.55 mVpk for the positive peak.

The RBIAS values previously listed should be considered starting values. Intel recommends that board designers measure each of their PCB's output amplitude and then adjust the RBIAS values as required.

5.1.2.2 Terminating Differential Pairs for 82540EM-Based Designs

Four differential pairs are terminated using 49.9 Ω (1% tolerance) resistors, placed near the LAN controller. One resistor connects to the MDI+ (MDI positive) signal trace and another resistor connects to the MDI- (MDI negative) signal trace. The opposite ends of the resistors connect together and to ground through a single 0.1 µf capacitor. The capacitor should be placed as close as possible to the 49.9 Ω resistors, using a wide trace.

Note: Do not vary the suggested component values. Be sure to lay out symmetrical pads and traces for these components such that the length and symmetry of the differential pairs are not disturbed.

5.1.3 Distance C: LAN Controller to Chipset

This section between the chipset and LAN controller should be addressed separately between the 82562EZ(EX) and 82551QM/82540EM.

5.1.3.1 LAN Connect Interface (LCI) for 82562EZ(EX)

The 82562EZ(EX) Platform LAN Connect device uses the LAN Connect Interface (LCI) to connect to the I/O Control Hub 5 (ICH5). LCI is a point-to-point interface optimized to support one device.

Line termination mechanisms are not specified for the LCI. Slew rate controlled output buffers achieve acceptable signal integrity by controlling signal reflection, undershoot and ringing.

For details about how to connect the LCI interface between the 82562EZ(EX) Platform LAN Connect device and ICH5, please refer to the 82562ET/EM Platform LAN Connect Printed Circuit Board (PCB) Design Guide, the Intel® 865 Chipset design guide, or the Intel® 875 Chipset design guide.

5.1.3.2 PCI Interface for 82540EM/82551QM

The PCI bus on 82540EM and 82551QM meet the PCI 2.2 specification.The trace routing on the bus should follow this PCI specification.

The Ethernet controllers operate as PCI slave devices for configuration and register programming. After the devices have been properly initialized, they can also operate as PCI masters to fetch memory descriptors and to read/write data buffers.

The devices are capable of operating in either a 5 V or 3.3 V signaling environment. The VIO terminals can be connected to either 3.3 V or 5 V to choose the appropriate PCI bus levels.These connections bias the controller PCI I/O buffers for the correct switching strength. However, all other digital inputs and outputs use 3.3 V signaling unless specified separately.

5.1.4 Distance D: The Overall Length of Differential Traces from LAN to RJ-45

The overall length of differential pairs should be less than four inches measured from the LAN controller to RJ-45 through the magnetics module.

The lengths of the differential traces (within each pair) should be equal within 50 mils (1.25 mm) and as symmetrical as possible.

5.1.5 Distance E: LAN Controller to PCB Edge

The LAN controller should be placed at least two inches from the printed circuit board edge.

5.2 Critical Dimensions for Integrated Magnetics Module

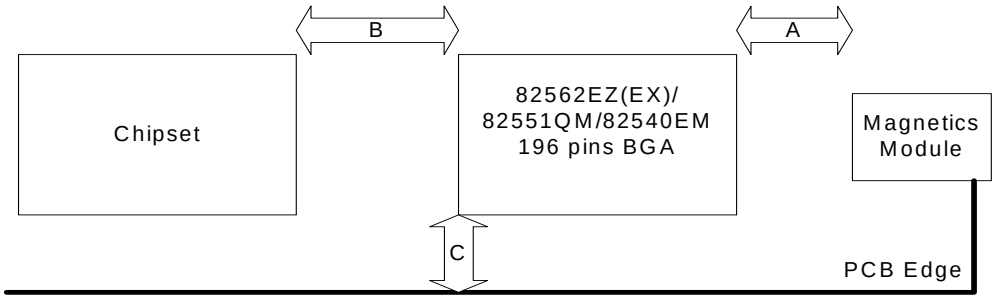


Figure 4. Critical Dimensions for 82562EZ(EX), 82551QM, and 82540EM Component Placement with Integrated Magnetics Module

5.2.1 Distance A: The Overall Length of Differential Traces

The overall length of differential pairs should be less than four inches measured from the LAN controller across the magnetics module to the RJ-45 connector.

5.2.2 Distance B: LAN Controller to Chipset

For LCI on 82562EZ(EX), the maximum length should be less than 12 inches on an ICH4 platform. For PCI bus on 82551QM, or the 82540EM, the bus routing should meet PCI 2.2 specifications.

5.2.3 Distance C: LAN Controller to PCB Edge

The LAN controller should be placed at least two inches from the PCB edge.

5.3 General LAN Differential Pair Trace Routing Considerations

Trace routing considerations are important to minimize the effects of crosstalk and propagation delays on sections of the board where high-speed signals exist. Signal traces should be kept as short as possible to decrease interference from other signals, including those propagated through power and ground planes.

Observe the following suggestions to help optimize board performance (Note: Some suggestions are specific to a 4.3 mil stackup.):

- Maintain constant symmetry and spacing between the traces within a differential pair.
- Keep the signal trace lengths of a differential pair equal to each other.
- Keep the total length of each differential pair under four inches. Many customer designs with differential traces longer than five inches have had one or more of the following issues:
  - IEEE PHY conformance failures
  - Excessive Electromagnetic Interference (EMI)
  - Degraded receive Bit Error Rate (BER)
- Do not route the transmit differential traces closer than 100 mils to the receive differential traces.
- Do not route any other signal traces both parallel to the differential traces and closer than 100 mils to the differential traces (300 mils is recommended).
- Keep maximum separation between differential pairs to seven mils.
- For high-speed signals, the number of corners and vias should be kept to a minimum. If a 90° bend is required, it is recommended to use two 45° bends instead.
- Traces should be routed away from board edges by a distance greater than the trace height above the ground plane. This allows the field around the trace to couple more easily to the ground plane rather than to adjacent wires or boards.
- Do not route traces and vias under crystals or oscillators. This prevents coupling to or from the clock. And as a general rule, place traces from clocks and drives at a minimum distance from apertures by a distance that is greater than the largest aperture dimension.

5.3.1 Trace Routing and Geometry

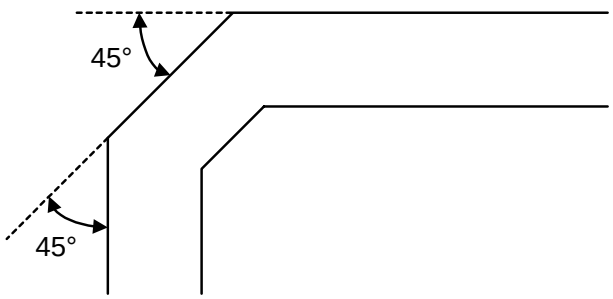


Figure 5. Trace Routing

The key factors in controlling trace EMI radiation are the trace length and the ratio of trace-width to trace-height above the ground plane. To minimize trace inductance, high-speed signals and signal layers that are close to a ground or power plane should be as short and wide as practical. Ideally, this trace width to height above the ground plane ratio is between 1:1 and 3:1. To maintain trace impedance, the width of the trace should be modified when changing from one board layer to another if the two layers are not equidistant from the power or ground plane. Differential trace impedances should be controlled to be ~100 Ω. It is necessary to compensate for trace-to-trace edge coupling, which can lower the differential impedance by up to 10 Ω, when the traces within a pair are closer than 30 mils (edge-to-edge).

Traces between decoupling and I/O filter capacitors should be as short and wide as practical. Long and thin traces are more inductive and would reduce the intended effect of decoupling capacitors. Also for similar reasons, traces to I/O signals and signal terminations should be as short as possible. Vias to the decoupling capacitors should be sufficiently large in diameter to decrease series inductance. Additionally, the PLC should not be closer than one inch to the connector/ magnetics/edge of the board.

5.3.1.1 Signal Isolation

Some rules to follow for signal isolation:

- Separate and group signals by function on separate layers if possible. Maintain a gap of 100 mils between all differential pairs (Ethernet) and other nets, but group associated differential pairs together. Note: Over the length of the trace run, each differential pair should be at least 0.3 inches away from any parallel signal traces.
- Physically group together all components associated with one clock trace to reduce trace length and radiation.

- Isolate I/O signals from high speed signals to minimize crosstalk, which can increase EMI emission and susceptibility to EMI from other signals.
- Avoid routing high-speed LAN traces near other high-frequency signals associated with a video controller, cache controller, CPU, or other similar devices.

5.3.1.2 Magnetics Module General Power and Ground Plane Considerations

To properly implement the common mode choke functionality of the magnetics module the chassis or output ground (secondary side of transformer) should be separated from the digital or input ground (primary side) by a physical separation of 100 mils minimum.

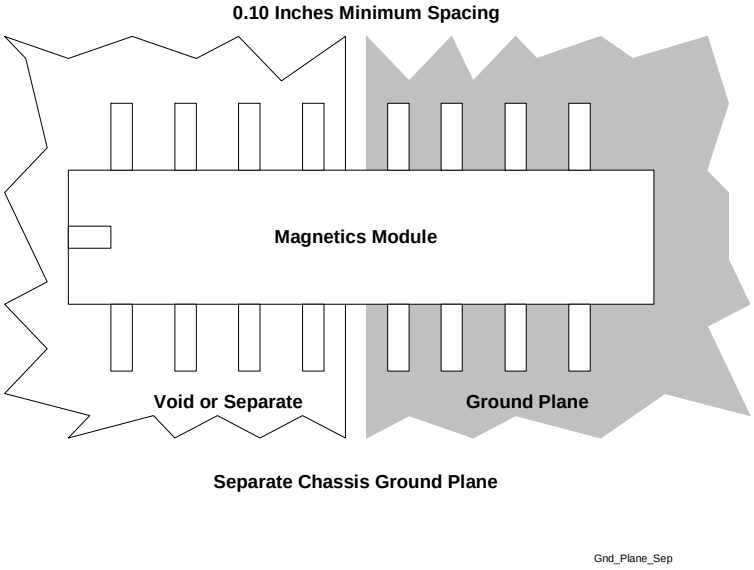


Figure 6. Separate Chassis Ground Plane

5.3.1.3 Separation

Good grounding requires minimizing inductance levels in the interconnections and keeping ground returns short, signal loop areas small, and power inputs bypassed to signal return, will significantly reduce EMI radiation.

Follow these rules to help reduce circuit inductance in both back planes and motherboards:

- Route traces over a continuous plane with no interruptions (don't route over a split plane). If there are vacant areas on a ground or power plane, avoid routing signals over the vacant area. This increases inductance and EMI radiation levels.
- Separate noisy digital grounds from analog grounds to reduce coupling. Noisy digital grounds can affect sensitive DC subsystems.
- All ground vias should be connected to every ground plane. In addition, every power via should be connected to all power planes at equal potential. This helps reduce circuit inductance.
- Physically locate grounds between a signal path and its return. This minimizes the loop area.

- Avoid fast rise/fall times as much as possible. Signals with fast rise and fall times contain many high frequency harmonics which can radiate EMI.
- The ground plane beneath the filter/transformer module should be split (see Figure 6). The RJ-45 connector side of the transformer module should have chassis ground beneath it. By splitting ground planes beneath transformer, noise coupling between the primary and secondary sides of the transformer and between the adjacent coils in the transformer is minimized. There should not be a power plane under the magnetics module.

5.4 Schematic for EEPROM Footprints and LCI Connection

There are two options for EEPROM footprints. OEMs can choose either a common EEPROM footprint for the 82540EM, 82551QM, 82562EZ(EX), and ICHx or an independent EEPROM footprint for each LAN silicon.

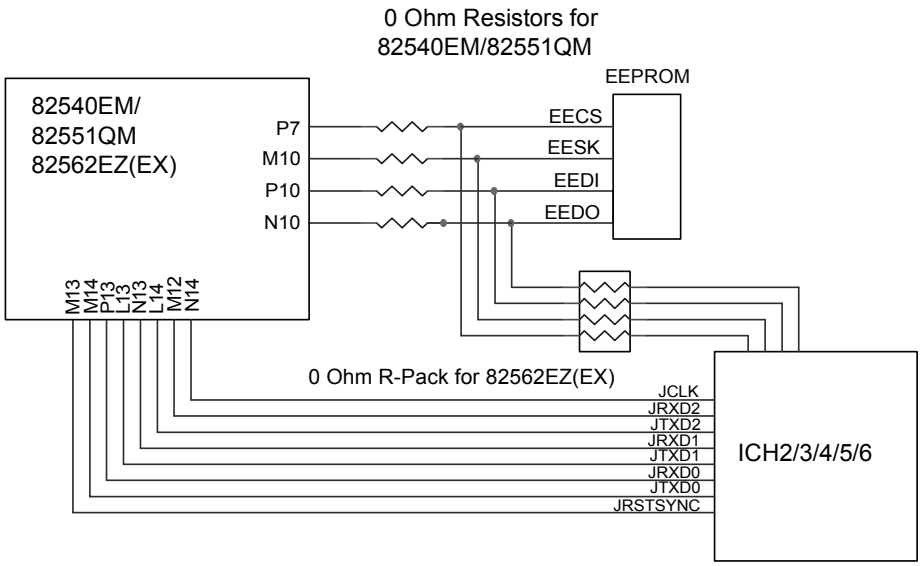


Figure 7. Common EEPROM Footprint for Both 82540EM, 82551QM, and 82562EZ(EX)

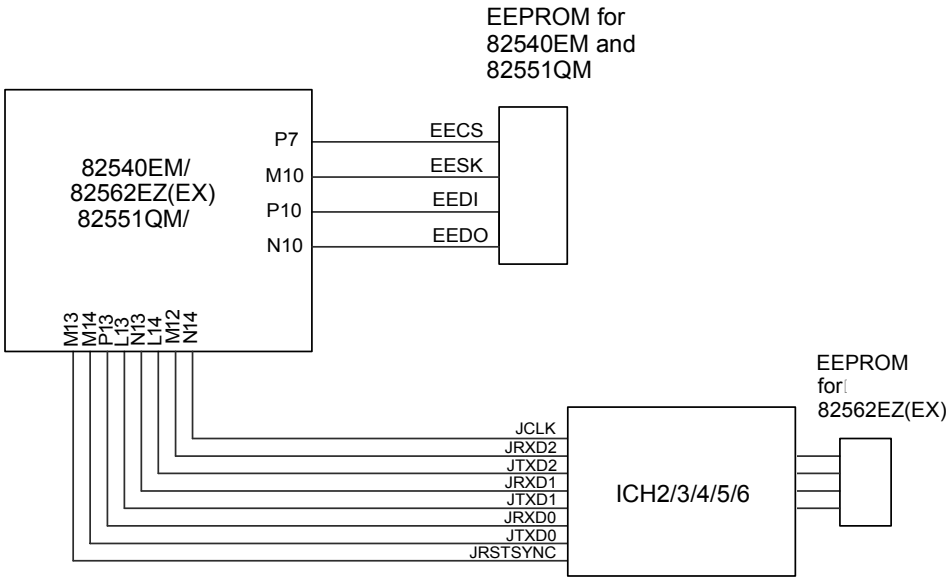


Figure 8. Independent EEPROM Footprints for Individual LAN Silicon

5.5 Termination of Unused Differential Signals on Gb Magnetics for 10/100 LOM Design

Since the number of differential signals are different between a 10/100 LAN silicon and a gigabit LAN silicon, the two major problems confronted in designing the dual footprint LOM design are:

1. Choosing the pin compatible magnetics modules for both 10/100 and gigabit silicon.
2. Terminating unused differential signals for gigabit between the selected magnetics module and RJ-45 connector when a 10/100 LAN design is implemented.

The three sections that follow provide the remedies for this issue.

5.5.1 Option 1: Board Level Stuffing

1. Layout resistor footprints on the pairs three and four of the differential traces for 82540EM LOM design. Refer to Figure 9.
2. Possibly rework the magnetics module for 10/100 to be footprint compatible with the magnetics for gigabit.

3. Replace the magnetics for the 82540EM with the one for the 82551QM, or the 82562EZ(EX) and then populate R1/R2 and R3/R4 for a 82551QM/82562EZ(EX) LOM design. Refer to Figure 10.

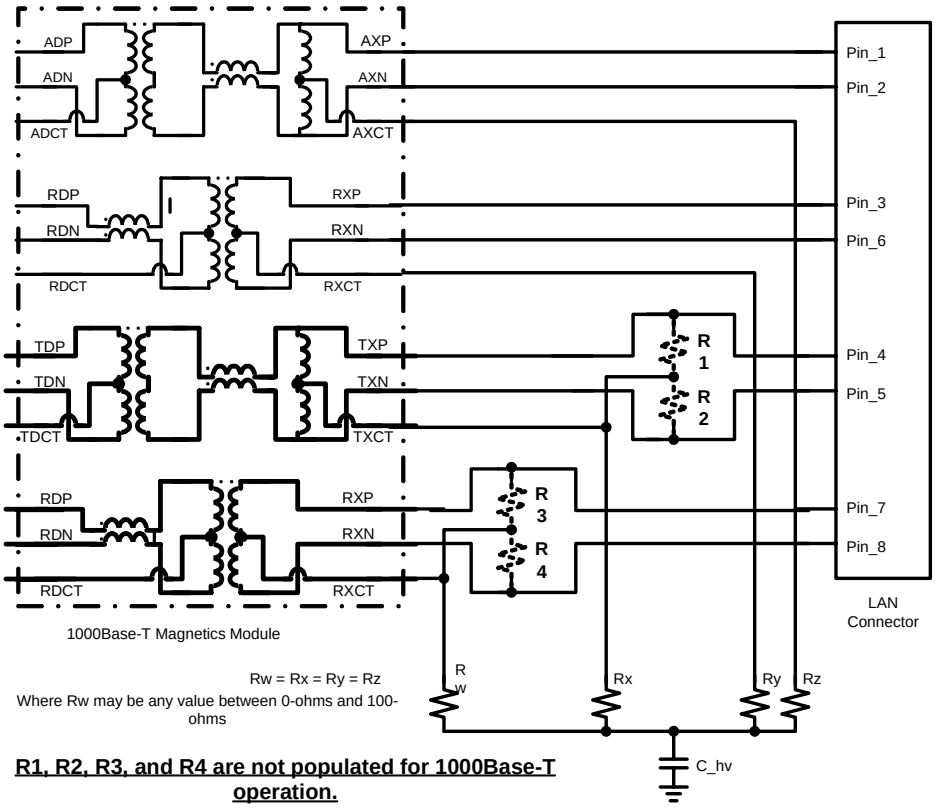


Figure 9. Typical Magnetics for Gb LAN Controller with Optional Resistors Footprint

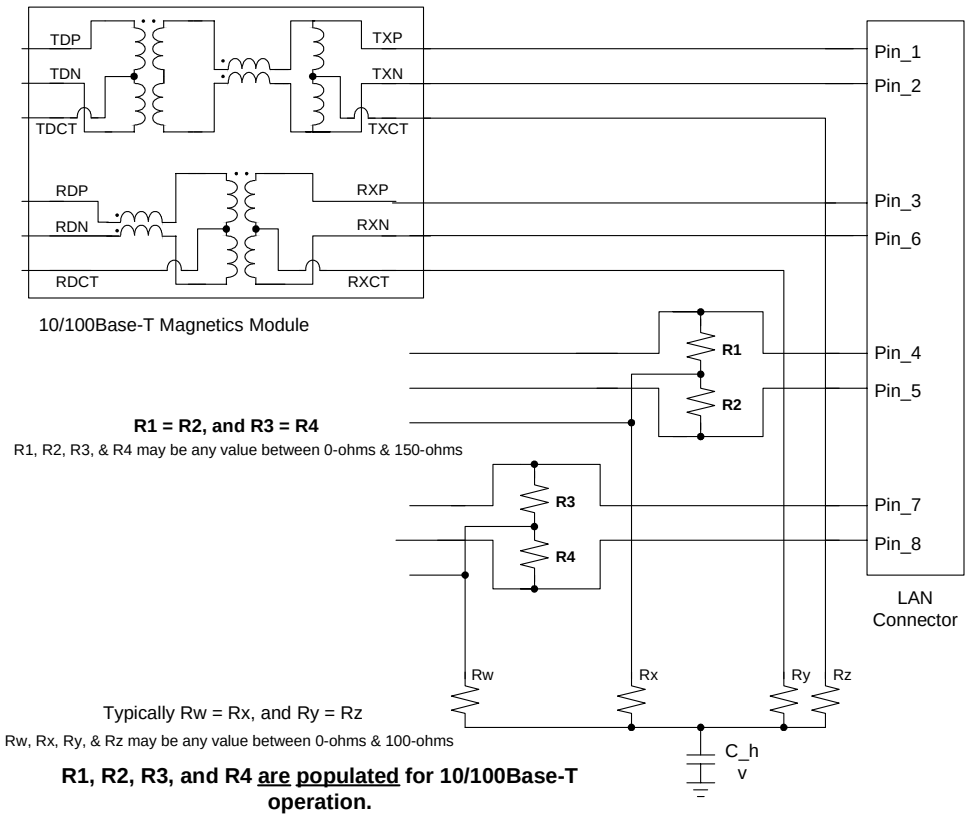


Figure 10. Replacement of Magnetics for 10/100 LAN Controller with Optional Resistors Populated

5.5.2 Option 2: Rework of Gigabit Magnetics[1]

Option two is a rework of a gigabit magnetics component with an internal jumper for 10/100 Mbps design.

In order to make a common footprint on differential pairs between the magnetics and RJ-45 connector for both 10/100 and Gigabit LOM design, one of the approaches is to rework the magnetics module for gigabit controller with internal jumpers to short pair three and four of differential signals. OEMs need to work with their magnetics vendors for this option.

1. Intel is working with some magnetics vendors to standardize the pinout assignments on the integrated magnetics module.

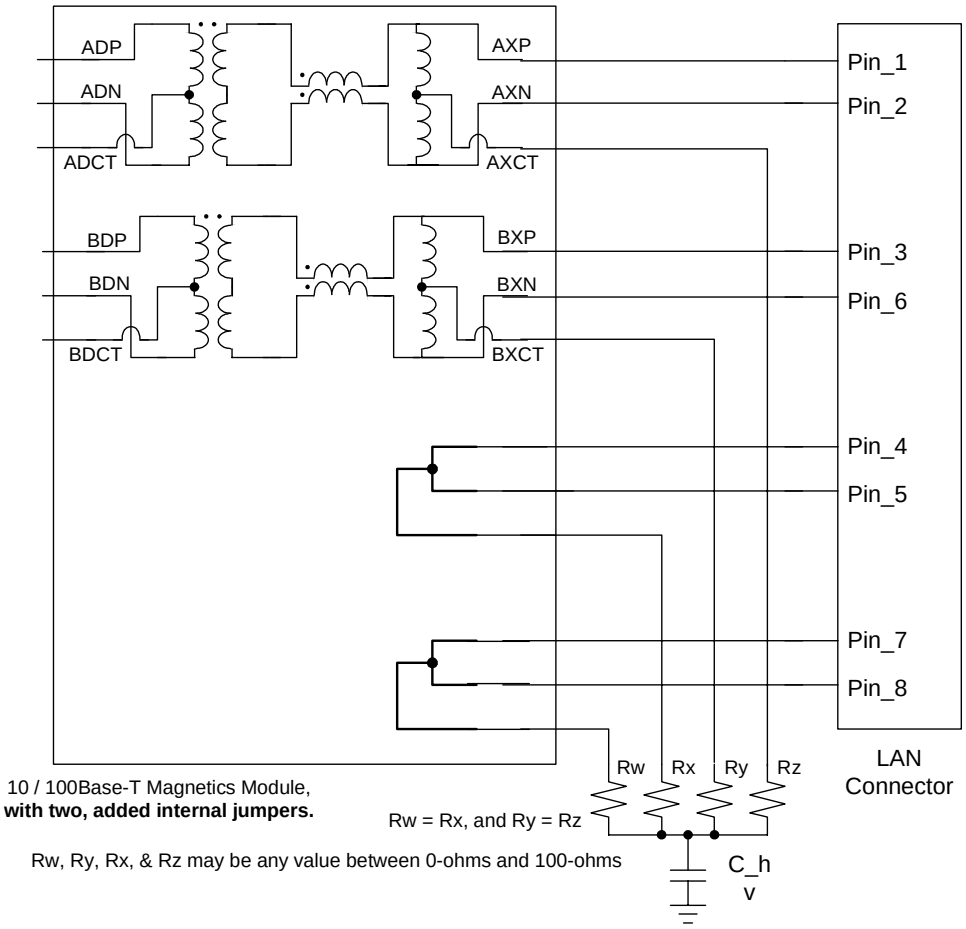


Figure 11. Rework of Gb Magnetics with Shorted Pair Three and Four on Differential Traces for 10/100 LOM Design

5.5.3 Option 3: Integrated Magnetics Module for 10/100 Mbps and Gigabit

Refer to Table 3.

Note: This page intentionally left blank.

6.0 Selecting a Magnetics Module for 10/100/1000 LOM Designs

6.1 Qualifying Magnetics for 10/100/1000 LOM Design

One of the most important component choices in a 10/100 and 1000 Mbps Ethernet LOM design is the magnetics module. The module has a critical effect on overall IEEE and emission compliance. The device selected should meet the required design performance. Occasionally, components that meet basic specifications can cause the system (LOM, NIC, Repeater, etc.) to fail because of unintentional interactions with board effects. Examples of these phenomena could be an unexpected series of parallel capacitance values or expected series inductance values within the magnetics module. This can cause the design to fail certain IEEE specifications.

In order to help OEMs qualify a magnetics module, Intel provides the electrical specifications for magnetics modules used with Intel's LOM or NIC designs as a reference.

Table 3. Magnetics Meeting Intel Specifications (Refer to Table 4 and Table 5)

	10/100	1000
Discrete Magnetics	H1012T / S558-5999-46 H1267 (82551QM MAC/PHY) H1267 (82562EZ/EX) PHY)	H5007 (82540EM MAC/PHY)
Pulse (Discrete MDI-X)	H1338 (82551QM only)	

Table 4. Electrical Specifications at 25°C for 10/100 Magnetics

Insertion Loss (TX / RX)	
0.1 through 0.999 MHz	1.0 dB maximum
1.0 through 15 MHz	0.35 dB maximum
15.1 through 6 0MHz	0.7 dB maximum
60.1 through 100 MHz	1.2 dB maximum
Return Loss (TX / RX)	
1.0 through 30 MHz	18 dB minimum
30.1 through 60 MHZ	19 - [20Log(f/30 MHz)] dB minimum
60.1 through 80 MHz	12 dB minimum
Transmit Common Mode-to-Common Mode Reject	
1.0 through 60 MHz	48 dB minimum
60.1 through 100 MHz	43 dB minimum
100.1 through 150 MHz	42 dB minimum
Effective Common Mode-to-Common Mode Reject	
1.0 through 60 MHz	38 dB minimum
60.1 through 100 MHz	34 dB minimum
100.1 through 150 MHz	32 dB minimum
Transmit Differential to Common Mode Reject	
1.0 through 60 MHz	38 dB minimum
60.1 through 100 MHz	35 dB minimum
100.1 through 150 MHz	32 dB minimum
Receive Differential to Common Reject	
1.0 THRU 60 MHz	30 dB minimum
60.1 through 100 MHz	25 dB minimum
100.1 through 150 MHz	20 dB minimum
Crosstalk Isolation (TX / RX)	
1.0 through 60 MHz	48 dB minimum
60.1 through 100 MHz	43 dB minimum
100.1 through 150 MHz	38 dB minimum
High Voltage Isolation	
IEEE 14.3.1.1	2250 V dc for 60 seconds
OCL with 8mA Bias 100 KHz	400 µH

Table 5. Electrical Specifications at 25° C for 1000 Gb Silicon

Insertion Loss (TX / RX)	
0.1 through 999 kHz	1.0 dB maximum
1.0 through 60.0 MHz	0.6 dB maximum
60.1 through 80.0 MHz	0.8 dB maximum
80.1 through 100.0 MHz	1.0 dB maximum
100 through 125.0 MHz	2.4 dB maximum
Return Loss (TX / RX)	
1.0 through 40.0 MHz	18 dB minimum
40.1 through 100 MHZ	12 - [20Log(f/80 MHz)] dB minimum
Common Mode-to-Common Mode Rejection	
1.0 through 60 MHz	48 dB minimum
60.1 through 100 MHz	42 dB minimum
100.1 through 150 MHz	37 dB minimum
Differential-to-Common Mode Rejection	
1.0 through 60 MHz	35 dB minimum
60.1 through 100 MHz	29 dB minimum
100.1 through 150 MHz	22 dB minimum
Crosstalk Isolation (TX / RX)	
1.0 through 80 MHz	36 dB minimum
80.1 through 150 MHz	27dB minimum
High Voltage Isolation	
1500 Vrms minimum, at 50 to 60 Hz, for 60 sec.	2250 V dc for 60 seconds
OCL with 8 mA Bias	400 uH minimum

Note: This page intentionally left blank.

7.0 EEPROM Information

The 82562EZ(EX), 82551QM, and 82540EM EEPROMs are used for hardware and software configuration and are read be software to determine specific design features.

7.1 Serial EEPROM for 82562EZ(EX) Implementations

Serial EEPROM for LAN implementations based on 82562EZ(EX) devices connects to the ICH5. Depending upon the size of the EEPROM, the 82562EZ(EX) may or may not support legacy manageability. Table 6 and Table 7 list the EEPROM map for the 82562EZ(EX) PLC device. For details on the EEPROM, refer to the appropriate *I/O Control Hub 2, 3, 4, 5, 6, and 7 EEPROM Map and Programming Information*.

Table 6. 82562EZ(EX) Memory Layout (128 Byte EEPROM)

00h **3Fh**	HW/SW Reserved Area

NOTE: No manageability provided.

Table 7. 82562EZ(EX) Memory Layout (512 Byte EEPROM)

00h **3Fh**	HW/SW Reserved Area
40h **FFh**	ASF and Legacy Manageability

NOTE: Legacy manageability only.

7.2 Serial EEPROM for 82540EM Controller Implementations

82540EM Gigabit Ethernet Controllers can use either a Microwire* or an SPI* serial EEPROM. The EEPROM mode is selected on the EEMODE input (pin J4). A no connect denotes an SPI* EEPROM. A pull-down resistor to ground denotes a Microwire EEPROM. Several words of the EEPROM are accessed automatically by the device after reset to provide pre-boot configuration data before it is accessed by host software. The remainder of the EEPROM space is available to software for storing the MAC address, serial numbers, and additional information.

For non-ASF applications, a 64 register by 16-bit Microwire serial EEPROM should be used, and for ASF 1.0 applications, a larger 93C66 Microwire or AT25040 SPI* serial EEPROM. ASF 2.0 requires an 8 KB SPI* serial EEPROM.

Intel has an MS-DOS* software utility called EEUPDATE, which can be used to program EEPROM images in development or production line environments. To obtain a copy of this program, contact your Intel representative.

The EEPROM access algorithm programmed into the 82540EM controller is compatible with most, but not all, commercially available 3.3 V Microwire* interface, serial EEPROM devices, with 64 x 16 (or 256 x 16) organization and a 1 MHz speed rating. The 82540EM EEPROM access algorithm drives extra pulses on the shift clock at the beginnings and ends of read and write cycles. The extra pulses may violate the timing specifications of some EEPROM devices. In selecting a serial EEPROM, choose a device that specifies “don't care” shift clock states between accesses.

Microwire EEPROMs that have been found to work satisfactorily with the 82540EM Gigabit Ethernet Controller are listed in Table 8.

Table 8. Microwire 64 x 16 Serial EEPROMs

Manufacturer	Manufacturer's Part Number
Atmel	AT93C46[1]
Catalyst	CAT93C46[1,2]

1. No manageability provided.
2. Revision H is not supported. Product die revision letter is marked on top of the package as a suffix to the production data code (e.g., AYWW**H**.)

SPI* EEPROMs that have been found to work satisfactorily with the 82540EM device are listed in Table 9. SPI* EEPROMs must be rated for a clock rate of at least 2 MHz.

Table 9. SPI* Serial EEPROMs for 82540EM Controller

Application	Manufacturer	Manufacturer's Part Number
ASF 1.0 or IMPI pass through	ATMEL	AT25040
ASF 2.0 or IMPI advanced pass through	ATMEL	AT25080

7.2.1 EEPROM Map Information

Table 10 lists the EEPROM map for the 82540EM Gigabit Ethernet Controller. For details on the EEPROM, refer to the *82540EM and 82540EP EEPROM Map and Programming Information.*

Table 10. 82540EM EEPROM Memory Layout

00h **3Fh**	HW/SW Reserved Area
40h **FFh**	ASF and Legacy Manageability
100h **19F**	Manageability Packet Filter Data
1A0 **...** **EEPROM END**	Loadable Manageability Firmware Code

7.3 82551QM EEPROM Map Information

Table 11 lists the EEPROM map for the 82551QM Fast Ethernet Controller. For details on the EEPROM, refer to the *82551QM/ER/IT EEPROM Map and Programming Information*.

Table 11. 82551QM EEPROM Memory Layout

00h **3Fh**	HW/SW Reserved Area
40h **FFh**	ASF and Legacy Manageability

Note: This page intentionally left blank.

8.0 Pin Number to Signal Mapping with Population Options

Table 12 lists the pin names for the four controllers and the corresponding shared ball reference value. Note that the 82540EM pin name in the 82551QM Datasheet/Design Guide is slightly different from the signal name on the reference schematic. The Datasheet/Design Guide signal names maintain consistency with the 64-bit gigabit controller naming convention, while the schematic names follow the conventions used by our engineers on their design tools.

Table 12. Ball Number to Signal Mapping (Sheet 1 of 9)

				Population Options			
Ball Ref	**82540EM Pin Name**	**82551QM Pin Name**	**82562EZ(EX) Pin Name**	**82540EM**	**82551QM**	**82562EZ(EX)**	**Comments**
A1	NC	NC	NC				
A2	SERR#	SERR#	NC			No stuff	
A3	VDDO (3.3 V)	VCC	VCC			3.3 V	
A4	IDSEL	IDSEL	NC			No stuff	
A5	AD[25]	AD[25]	NC			No stuff	
A6	PME#	PME#	NC			No stuff	
A7	VDDO (3.3 V)	VCC	VCC			3.3 V	
A8	AD[30]	AD[30]	NC			No stuff	
A9	LAN_PWR_GOOD	ALTRST#	NC	Master Reset	Pull-up or Master Reset	No stuff	Master chip reset for the 82540EM and 82551QM. The 82551QM can be pulled up and use an internal reset.
A10	SMBCLK	SMBCLK	NC				
A11	VDDO (3.3 V)	VCC	VCCT			3.3 V	VCCT = 3.3 V
A12	LED0/LINK_UP#	LILED#	LILED#			LINK_LED	Same signal - different names.
A13	TEST	TEST	TESTEN	Pull-down	Pull-down	Pull-down	May have LAN Disable logic connected to this signal for 82562EZ(EX). Test enable signal for the 82540EM/ 82551QM. Both require an external pull-down resistor.
A14	NC	NC	NC				
B1	AD[22]	AD[22]	NC			No stuff	
B2	AD[23]	AD[23]	NC			No stuff	
B3	GND	VSSPP	VSS				
B4	AD[24]	AD[24]	NC			No stuff	
B5	AD[26]	AD[26]	NC			No stuff	
B6	AD[27]	AD[27]	NC			No stuff	
B7	GND	VSSPP	VSS				

Table 12. Ball Number to Signal Mapping (Sheet 2 of 9)

				Population Options			
Ball Ref	**82540EM Pin Name**	**82551QM Pin Name**	**82562EZ(EX) Pin Name**	**82540EM**	**82551QM**	**82562EZ(EX)**	**Comments**
B8	AD[31]	AD[31]	NC			No stuff	
B9	RST#	ISOLATE#	NC			No stuff	Signals are the same. ISOLATE# is used as RST#.
B10	SMB_ALERT#	SMB_ALERT#/ LAN_PWR_ GOOD	NC				
B11	LED2/LINK100#	SPDLED#	SPDLED#			LED	Same signal - different names.
B12	LED3/LINK1000#	TO	TOUT	LED	NC	No stuff	Testability output for 82562EZ(EX). LINK1000 LED not applicable to the 82551QM.
B13	CTRL25	RBIAS100	RBIAS100	Power Regulator	649 pull-down	649 pull-down	Connect to PNP or populate 82562EZ(EX) and 82551QM with a pull-down and the 82540EM with a transistor.
B14	IEEE_TEST+	RBIAS10	RBIAS10	2.49 K Ω pull-down	619 pull-down	619 pull-down	Change the value of the pull-down resistor for each option.
C1	AD[21]	AD[21]	NC			No stuff	
C2	M66EN	RST#	NC		Pull-up	No stuff	This may require a 0 Ω resistors to a M66EN signal.
C3	REQ#	REQ#	NC			No stuff	
C4	C/BE#[3]	C/BE#[3]	NC			No stuff	
C5	APM_WAKEUP	CSTSCHG	NC				Same signal - different names.
C6	AD[28]	AD[28]	NC			No stuff	
C7	AD[29]	AD[29]	NC			No stuff	
C8	NC	CLK_RUN#	NC	Don't care	Pull-down	No stuff	The pull-down resistor for the 82551QM can be left alone or depopulated for the 82540EM.
C9	SMBDATA	SMBDATA	NC				
C10	GND	VSSPT	VSS				
C11	LED1/ACTIVITY#	ACTLED#	ACTLED#			LED	Same signal - different names.
C12	GND	VREF	VSSA	VSS	VSS	VSS	VSSA and VREF = VSS. The 82551QM connection is usually NC (it has an internal pull-down), but VSS is ok.

Table 12. Ball Number to Signal Mapping (Sheet 3 of 9)

				Population Options			
Ball Ref	**82540EM Pin Name**	**82551QM Pin Name**	**82562EZ(EX) Pin Name**	**82540EM**	**82551QM**	**82562EZ(EX)**	**Comments**
C13	MDI[0]+	TDP	TDP			MDI	Same signal - different names.
C14	MDI[0]-	TDN	TDN			MDI	Same signal - different names.
D1	AD[18]	AD[18]	NC			No stuff	
D2	AD[19]	AD[19]	NC			No stuff	
D3	AD[20]	AD[20]	NC			No stuff	
D4	GND	VSS	VSS	VSS	VSS		
D5	GND	VSS	VSS				
D6	GND	VSS	VSS				
D7	GND	VSS	VSS				
D8	GND	VSS	VSS				
D9	AVDDL (2.5 V)	NC	NC	2.5 V	Don't care		This is used as the 2.5 V power source for the 82540EM. It is not populated for the 82562EZ(EX)/ 82551QM.
D10	NC	NC	ISOL_EXEC			NC	May have LAN Disable logic connected to this signal for 82562EZ(EX).
D11	AVDDL (2.5 V)	NC	NC	2.5 V	Don't care	No stuff	This is used as the 2.5 V power source for the 82540EM. It is not populated for the 82562EZ(EX)/ 82551QM.
D12	NC	TI	ISOL_TI	NC	NC	No stuff	May have LAN Disable logic connected to this signal for 82562EZ(EX). This is a no connect for the 82540EM.
D13	GND	TEXEC	VSSA	VSS	VSS	VSS	VSSA = VSS. The 82551QM connection is usually NC, but VSS is ok and works for tests.
D14	IEEE_TEST-	TCK	ISOL_TCK	NC	NC	NC	May have LAN Disable logic connected to this signal for 82562EZ(EX). The 82551QM uses this as a test point for testability.
E1	VDDO (3.3 V)	VCC	VCC			3.3 V	
E2	GND	VSSPP	VSS				

Table 12. Ball Number to Signal Mapping (Sheet 4 of 9)

				Population Options			
Ball Ref	**82540EM Pin Name**	**82551QM Pin Name**	**82562EZ(EX) Pin Name**	**82540EM**	**82551QM**	**82562EZ(EX)**	**Comments**
E3	AD[17]	AD[17]	NC			No stuff	
E4	GND	VSS	VSS				
E5	GND	VSS	VSS				
E6	GND	VSS	VSS				
E7	GND	VSS	VSS				
E8	GND	VSS	VSS				
E9	GND	VSS	VSS				
E10	GND	VSS	VSS				
E11	DVDD (1.5V)	NC	VCCT	1.5 V	Don't care	3.3 V	The 82540EM connects to a 1.5 V rail. The 82551QM connects to a 3.3 V rail.
E12	DVDD (1.5V)	VCC	VCCT	1.5 V	3.3 V	3.3 V	This is 1.5 V power signal or 0 Ω connected 3.3 V power signal.
E13	MDI[1]+	RDP	RDP			MDI	Same signal - different names.
E14	MDI[1]-	RDN	RDN			MDI	Same signal - different names.
F1	IRDY#	IRDY#	NC			No stuff	
F2	FRAME#	FRAME#	NC			No stuff	
F3	C/BE#[2]	C/BE#[2]	NC			No stuff	
F4	GND	VSS	VSS				
F5	GND	VSS	VSS				
F6	GND	VSS	VSS				
F7	GND	VSS	VSS				
F8	GND	VSS	VSS				
F9	GND	VSS	VSS				
F10	GND	VSS	VSS				
F11	GND	VSS	VSS			VSS	
F12	NC	FLD2	NC	NC	NC	NC	This is a no connect signal for the 82540EM/ 82562EZ(EX).
F13	MDI[2]+	FLD1	NC	Magnetics	NC	Magnetics	10/100 Magnetics will not have a pin connected here.
F14	MDI[2]-	FLD0	NC	Magnetics	NC	Magnetics	10/100 Magnetics will not have a pin connected here.
G1	CLK	CLK	NC			No stuff	
G2	VIO	VIO	NC			VIO	

Table 12. Ball Number to Signal Mapping (Sheet 5 of 9)

				Population Options			
Ball Ref	**82540EM Pin Name**	**82551QM Pin Name**	**82562EZ(EX) Pin Name**	**82540EM**	**82551QM**	**82562EZ(EX)**	**Comments**
G3	TRDY#	TRDY#	NC			No stuff	
G4	ZP_COMP	NC	NC	Pull-up	Don't care	NC	Populate the pull-up resistor for the 82540EM.
G5	DVDD (1.5 V)	VCC	VCCR	1.5 V	3.3 V	3.3 V	This is 1.5 V power signal or 0 Ω connected 3.3 V power signal.
G6	DVDD (1.5 V)	VCC	VCC	1.5 V	3.3 V	3.3 V	
G7	GND	VSS	VSS				
G8	GND	VSS	VSS				
G9	GND	VSS	VSS				
G10	GND	VSS	VSS				
G11	GND	VSS	VSS			VSS	
G12	AVDDL (2.5 V)	FLD3	NC	2.5 V	NC	No stuff	For the 82540EM/ 82551QM, these signals need a 0 Ω population option.
G13	DVDD (1.5 V)	VCC	VCC	1.5 V	3.3	3.3 V	This is 1.5 V power signal or 0 Ω connected 3.3 V power signal.
G14	GND	VSSPL	VSS				VSSPL = VSS.
H1	STOP#	STOP#	NC			No stuff	
H2	INTA#	INTA#	NC			No stuff	
H3	DEVSEL#	DEVSEL#	NC			No stuff	
H4	ZN_COMP	NC	NC	Pull-down	Don't care	No stuff	Populate the pull-down resistor for the 82540EM.
H5	DVDD (1.5 V)	VCC	VCCR	1.5 V	3.3 V	3.3 V	This is 1.5 V power signal or 0 Ω connected 3.3 V power signal.
H6	DVDD (1.5 V)	VCC	VCC	1.5 V	3.3 V	3.3 V	
H7	DVDD (1.5 V)	VCC	VCC	1.5 V	3.3 V	3.3 V	
H8	DVDD (1.5 V)	VCC	VCC	1.5 V	3.3 V	3.3 V	
H9	GND	VSS	VSS				
H10	GND	VSS	VSS				
H11	DVDD (1.5 V)	NC	VCC	1.5 V	Don't care	3.3 V	The 82540EM connects to a 1.5 V rail and the 82551QM to a 3.3 V rail.
H12	NC	FLD6	NC	NC	NC	NC	This is a no connect signal for the 82540EM/ 825562EZ(EX).
H13	MDI[3]+	FLD5	NC	Magnetics	NC	Magnetics	10/100 Magnetics will not have a pin connected here.

Table 12. Ball Number to Signal Mapping (Sheet 6 of 9)

				Population Options			
Ball Ref	**82540EM Pin Name**	**82551QM Pin Name**	**82562EZ(EX) Pin Name**	**82540EM**	**82551QM**	**82562EZ(EX)**	**Comments**
H14	MDI[3]-	FLD4	NC	Magnetics	NC	Magnetics	10/100 Magnetics will not have a pin connected here.
J1	PAR	PAR	NC			No stuff	
J2	PERR#	PERR#	NC			No stuff	
J3	GNT#	GNT#	NC			No stuff	
J4	NC	NC	NC			NC	
J5	DVDD (1.5 V)	VCC	VCCR	1.5 V	3.3 V	3.3 V	This is 1.5 V power signal or 0 Ω connected 3.3 V power signal.
J6	DVDD (1.5 V)	VCC	VCC	1.5 V	3.3 V	3.3 V	
J7	DVDD (1.5 V)	VCC	VCC	1.5 V	3.3 V	3.3 V	
J8	DVDD (1.5 V)	VCC	VCC	1.5 V	3.3 V	3.3 V	
J9	DVDD (1.5 V)	VCC	VCC	1.5 V	3.3 V	3.3 V	
J10	DVDD (1.5 V)	VCCR	VCC	1.5 V	3.3 V	3.3 V	
J11	DVDD (1.5 V)	VCCR	VCC	1.5 V	3.3 V	3.3 V	
J12	AUX_PWR	FLA1/AUX_PWR	NC			No stuff	These are the same. The 82551QM FLA1 signal samples auxiliary power at reset. The 82540EM always samples auxiliary power.
J13	NC	FLA0	NC	NC	NC	No stuff	This can be a no connect for the 82540EM/ 82551QM.
J14	XTAL2	FLD7	X2	XTAL2	NC		For the 82540EM/ 82551QM, these signals need a 0 Ω population option.
K1	AD[16]	AD[16]	NC			No stuff	
K2	GND	VSSPP	VSS				VSSPP = VSS
K3	VDDO (3.3 V)	VCC	VCC			3.3 V	
K4	VDDO (3.3 V)	VCC	VCC			3.3 V	
K5	DVDD (1.5 V)	VCC	VCC	1.5 V	3.3 V	3.3 V	This is 1.5 V power signal or 0 Ω connected 3.3 V power signal.
K6	DVDD (1.5 V)	VCC	VCC	1.5 V	3.3 V	3.3 V	
K7	DVDD (1.5 V)	VCC	VCC	1.5 V	3.3 V	3.3 V	
K8	DVDD (1.5 V)	VCC	VCC	1.5 V	3.3 V	3.3 V	
K9	DVDD (1.5 V)	VCC	VCC	1.5 V	3.3 V	3.3 V	
K10	DVDD (1.5 V)	VCC	VCC	1.5 V	3.3 V	3.3 V	
K11	DVDD (1.5 V)	VCC	VCC	1.5 V	3.3 V	3.3 V	
K12	GND	VSSPL	VSS			VSS	VSSPL =VSS
K13	VDDO (3.3 V)	VCC	VCC			3.3 V	

Table 12. Ball Number to Signal Mapping (Sheet 7 of 9)

				Population Options			
Ball Ref	**82540EM Pin Name**	**82551QM Pin Name**	**82562EZ(EX) Pin Name**	**82540EM**	**82551QM**	**82562EZ(EX)**	**Comments**
K14	XTAL1	FLA2	X1	XTAL1	NC		For the 82540EM/ 82551QM, these signals need a 0 Ω population option.
L1	AD[14]	AD[14]	NC			No stuff	
L2	AD[15]	AD]15]	NC			No stuff	
L3	C/BE#[1]	C/BE#[1]	NC			No stuff	
L4	DVDD (1.5 V)	VCC	VCC	1.5 V	3.3 V	3.3 V	This is 1.5 V power signal or 0 Ω connected 3.3 V power signal.
L5	DVDD (1.5 V)	VCC	VCC	1.5 V	3.3 V	3.3 V	
L6	GND	VSS	VSS				
L7	NC	MDMCS#	ADV10	NC	NC	NC	No connect for the 82540EM.
L8	AVDDL (2.5 V)	NC	NC	2.5 V	Don't care	No stuff	This is the 2.5 V power source for the 82540EM. No connect for the 82551QM/ 82562EZ(EX).
L9	DVDD (1.5 V)	VCC	VCC	1.5 V	3.3 V	3.3 V	This is 1.5 V power signal or 0 Ω connected 3.3 V power signal
L10	DVDD (1.5 V)	VCC	VCC	1.5 V	3.3 V	3.3 V	
L11	GND	VSS	VSS				
L12	JTAG_TMS	FLA5	NC	JTAG	NC	NC	ICH drives this signal low. TRST# needs to be grounded to disable JTAG. JTAG becomes difficult to use.
L13	JTAG_TRST#	FLA4	JTXD[1]	JTAG	NC	LCI	
L14	JTAG_TCK	FLA3	JTXD[2]	JTAG	NC	LCI	
M1	AD[11]	AD[11]	NC			No stuff	
M2	AD[12]	AD[12]	NC			No stuff	
M3	AD[13]	AD[13]	NC			No stuff	
M4	C/BE#[0]	C/BE#[0]	NC			No stuff	
M5	AD[5]	AD[5]	NC			No stuff	
M6	GND	VSSPP	VSS				
M7	AD[1]	AD[1]	NC			No stuff	
M8	CLK_VIEW	FLOE#	NC	NC	NC	NC	No connect for the 82562EZ(EX).
M9	FLSH_CE#	FLWE#	NC	NC	NC	NC	No connect for the 82562EZ(EX).
M10	EESK	FLA15/ EESK	NC			EESK	These are the same signals but have different names.

Table 12. Ball Number to Signal Mapping (Sheet 8 of 9)

				Population Options			
Ball Ref	**82540EM Pin Name**	**82551QM Pin Name**	**82562EZ(EX) Pin Name**	**82540EM**	**82551QM**	**82562EZ(EX)**	**Comments**
M11	FLSH_SI	FLA12	NC	NC	NC	NC	No connect for the 82562EZ(EX).
M12	SDP[7]	FLA11	JRXD[2]	SDP	NC	LCI	De-populate any SDP logic for the 82551QM. ICH expects this signal to be high or undriven.
M13	JTAG_TDI	FLA7	JRSTSYNC	JTAG	NC	LCI	ICH expects this signal to be high or undriven. JTAG becomes difficult to use.
M14	JTAG_TDO	FLA6	JTXD[0]	JTAG	NC	LCI	
N1	GND	VSSPP	VSS				VSSPP = VSS
N2	AD[10]	AD[10]	NC			No stuff	
N3	AD[9]	AD[9]	NC			No stuff	
N4	AD[7]	AD[7]	NC			No stuff	
N5	AD[4]	AD[4]	NC			No stuff	
N6	VDDO (3.3 V)	VCC	VCC			3.3 V	
N7	AD[0]	AD[0]	NC			No stuff	
N8	VDDO (3.3 V)	VCC	VCC			3.3 V	
N9	FLSH_SCK	FLCS#	NC	NC	NC	NC	No connect for the 82562EZ(EX).
N10	EEDO	FLA14/ EEDO	NC			EEDO	If desired, this can be shorted to the ICH EEDI b/c it is an input in ICH in reset.
N11	NC	X1	NC	Don't care	XTAL	NC	For the 82540EM/ 82551QM, these signals require a 0 Ω population option.
N12	GND	VSSPL	VSSP			VSS	VSSP and VSSPL = VSS
N13	SDP[6]	FLA10	JRXD[1]	SDP	NC	LCI	De-populate any SDP logic for the 82551QM. ICH expects this signal to be high or undriven.
N14	SDP[0]	FLA8/IOCHRDY	JCLK	SDP	NC	LCI	
P1	NC	NC	NC				
P2	VDDO (3.3 V)	VCC	VCC			3.3 V	
P3	AD[8]	AD[8]	NC			No stuff	
P4	AD[6]	AD[6]	NC			No stuff	
P5	AD[3]	AD[3]	NC			No stuff	
P6	AD[2]	AD[2]	NC			No stuff	
P7	EECS	EECS	NC			EECS	
P8	GND	VSSPL	VSS			VSS	VSSPL = VSS

Table 12. Ball Number to Signal Mapping (Sheet 9 of 9)

				Population Options			
Ball Ref	**82540EM Pin Name**	**82551QM Pin Name**	**82562EZ(EX) Pin Name**	**82540EM**	**82551QM**	**82562EZ(EX)**	**Comments**
P9	FLSH_SO	FLA16	NC	NC	NC	LAN_EN	Connect to LAN Enable signal.
P10	EEDI	FLA13/ EEDI	NC			EEDI	If desired, this can be shorted to the ICH EEDI because it is an input in ICH in reset.
P11	CTRL15	X2	NC	Power Regulator	XTAL	No stuff	For the 82540EM/ 82551QM, these signals require a 0 Ω population option. Connect to PNP. Don't' stuff PNP on 82562EZ(EX).
P12	VDDO (3.3 V)	VCC	VCC			3.3 V	
P13	SDP[1]	FLA9	JRXD[0]	NC	NC	LCI	De-populate any SDP logic for the 82551QM. ICH expects this signal to be high or undriven.
P14	NC	NC	NC			NC	

Note: This page intentionally left blank.

9.0 Self-Review Checklist for Combined Footprint LOM

A Portable Data Format (PDF) Self-Review Checklist for a Combined Footprint LOM is available to aid designers via:

http://www.intel.com

Note: This page intentionally left blank.

10.0 Reference Schematic

The following pages contain reference schematics for the 82562EZ(EX)/82551QM and 82540EM Combined Footprint LOM Design Guide.

REVISIONS		
REV	DESCRIPTION	DATE

82540EM, 82551QM, 82562EZ/EX REFERENCE DESIGN

15mm x 15mm BGA

1mm pitch

***A** = Install component if using 82540EM MAC/PHY*

***B** = Install component if using 82551QM MAC/PHY*

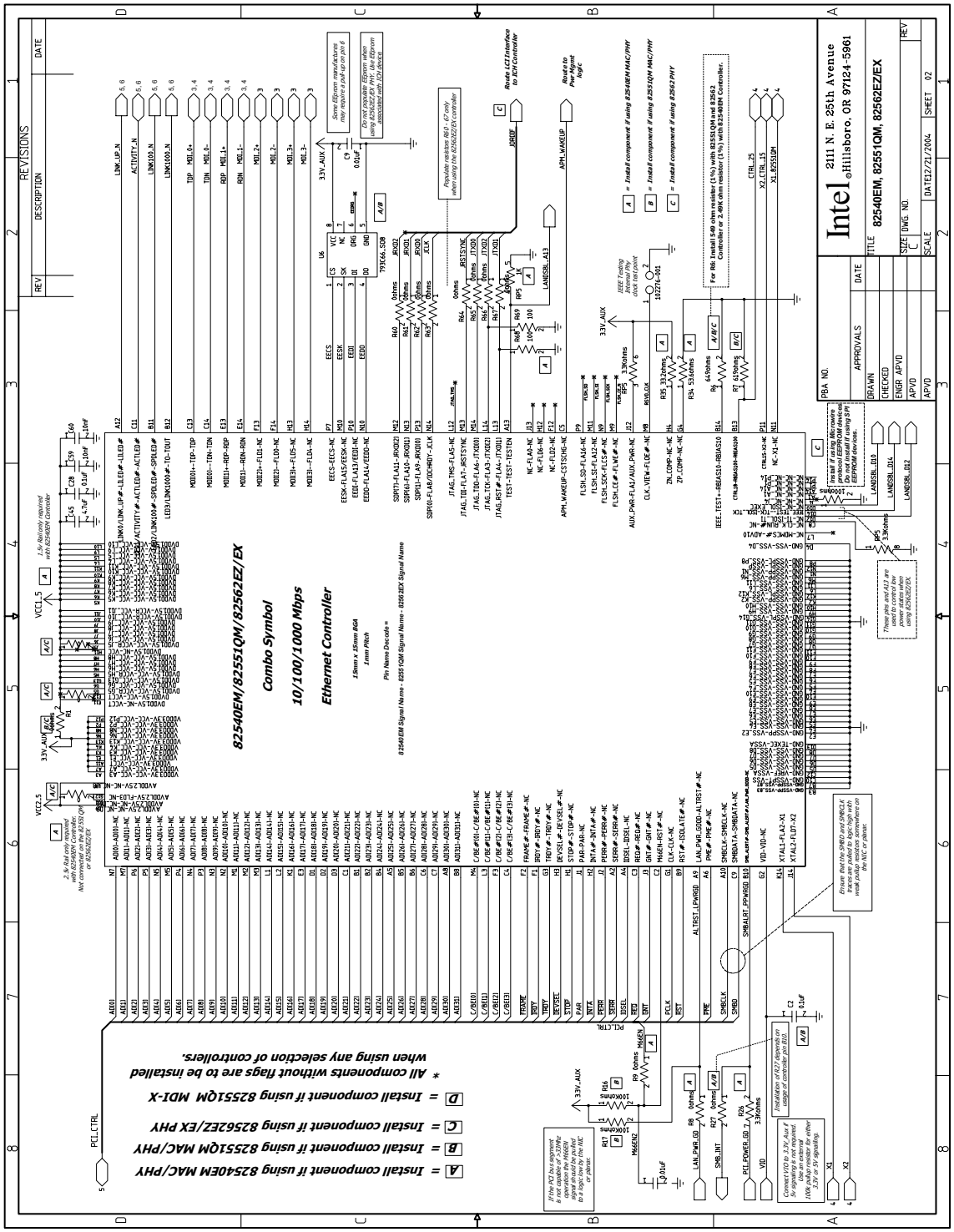
***C** = Install component if using 82562EZ/EX PHY*

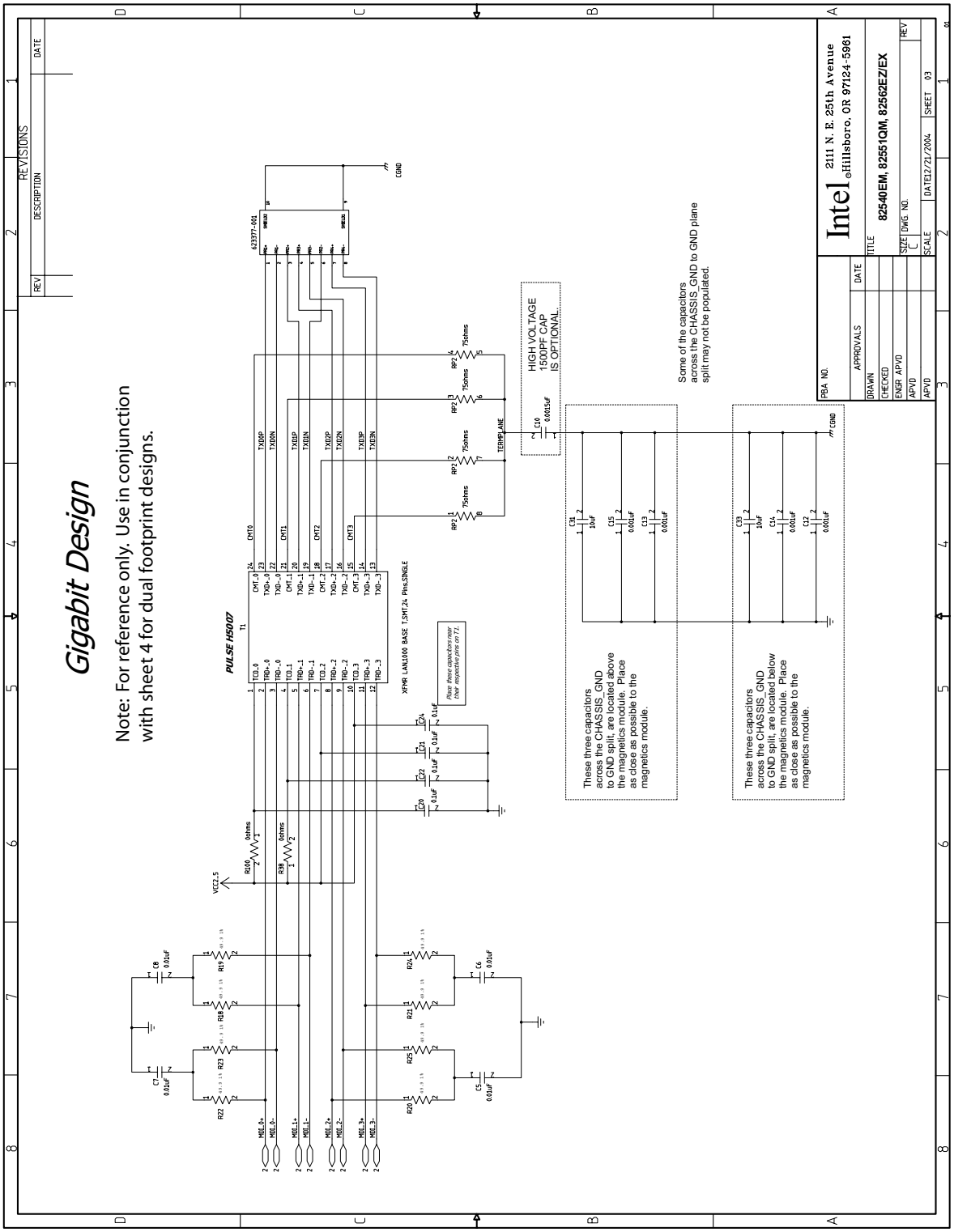
***D** = Install component if using 82551QM MDI-X*

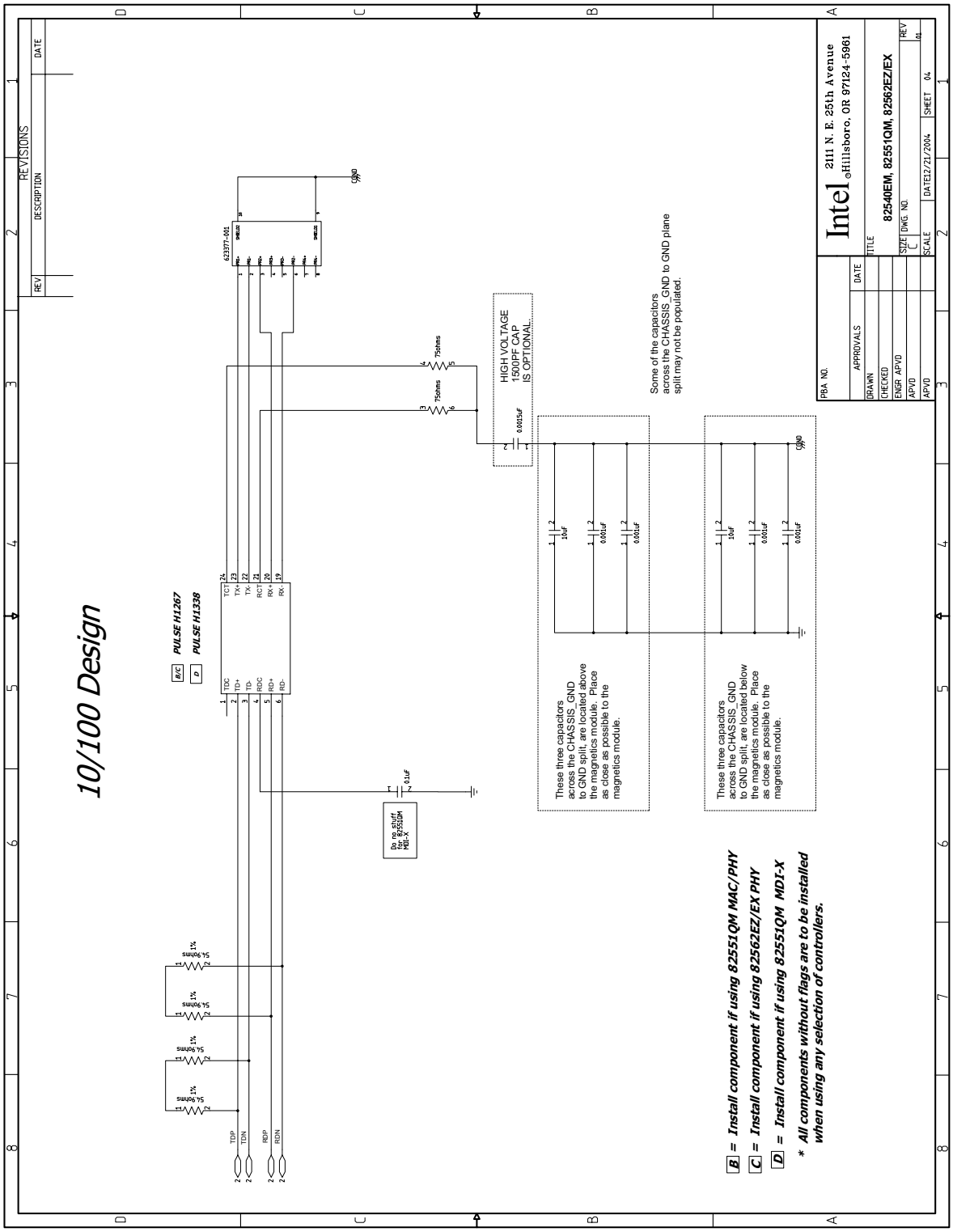
** All components without flags are to be installed when using any selection of controllers.*

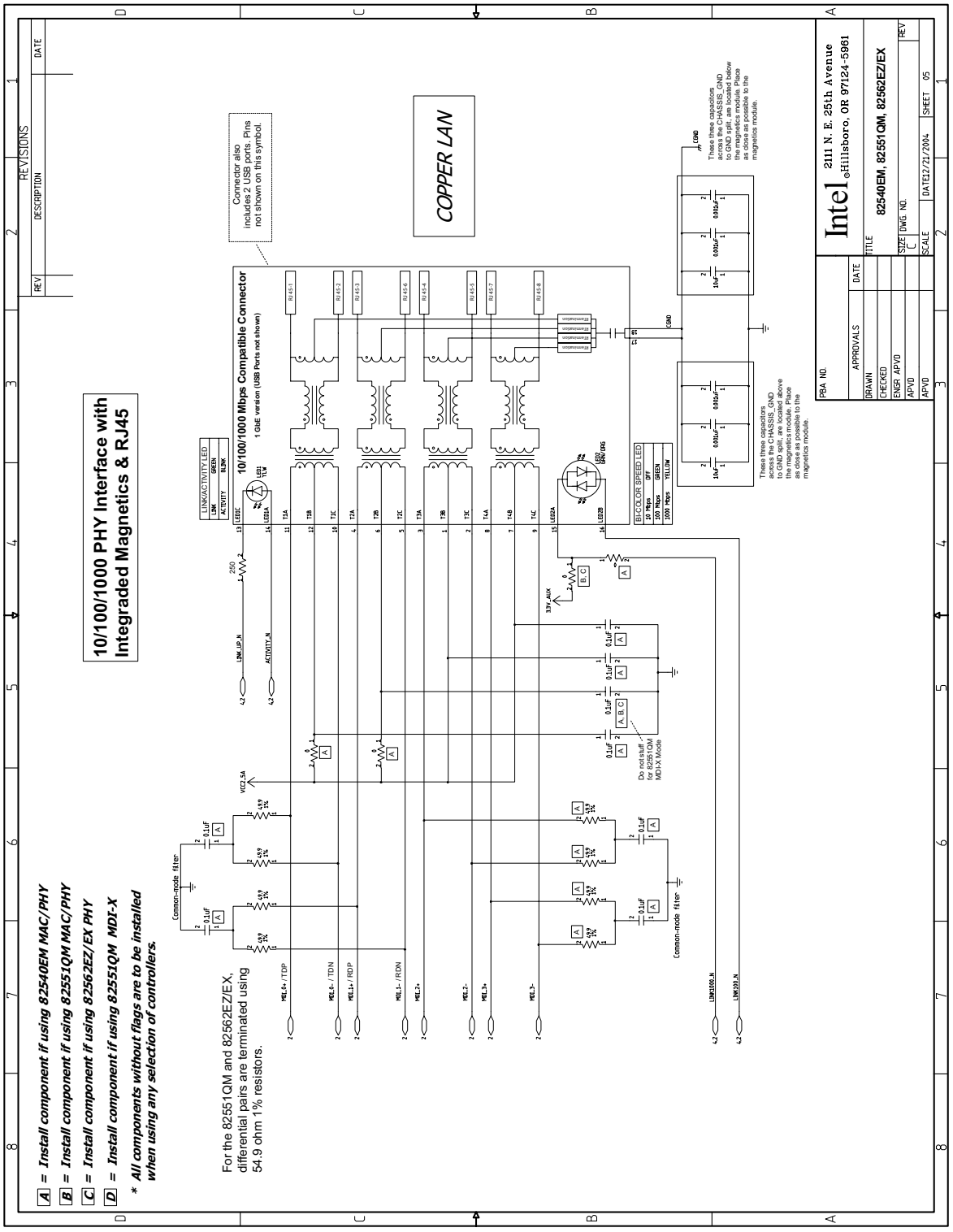
rev 1.5
12/2104

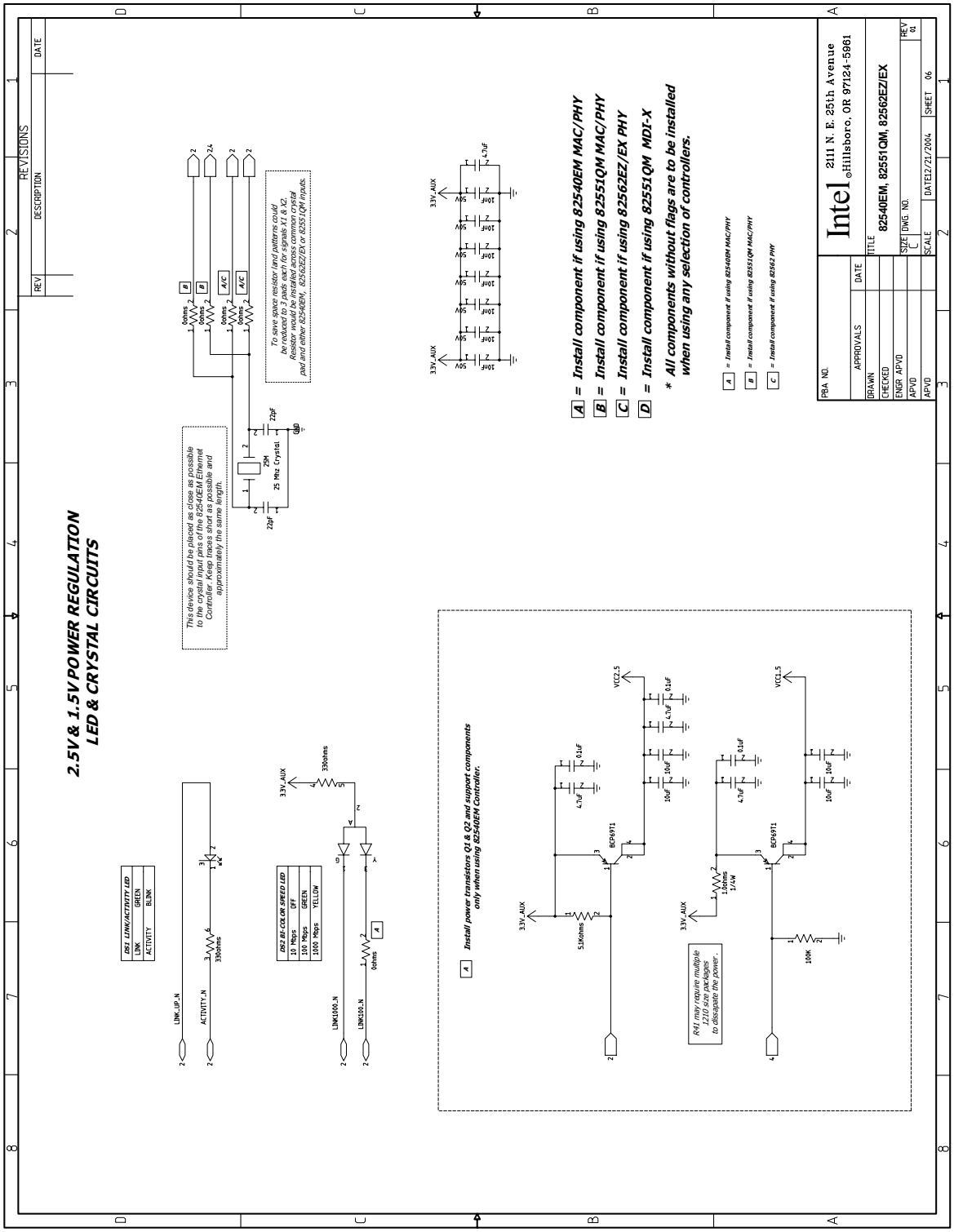
PBA NO.		Intel 2111 N. E. 25th Avenue ©Hillsboro, OR 97124-5961	
APPROVALS	DATE	TITLE	
DRAWN		82540EM, 82551QM, 82562EZ/EX	
CHECKED			
ENGR APVD			
APVD		SIZE C / DWG. NO.	REV 02
APVD		SCALE / DATE 12/21/2004 / SHEET 01	

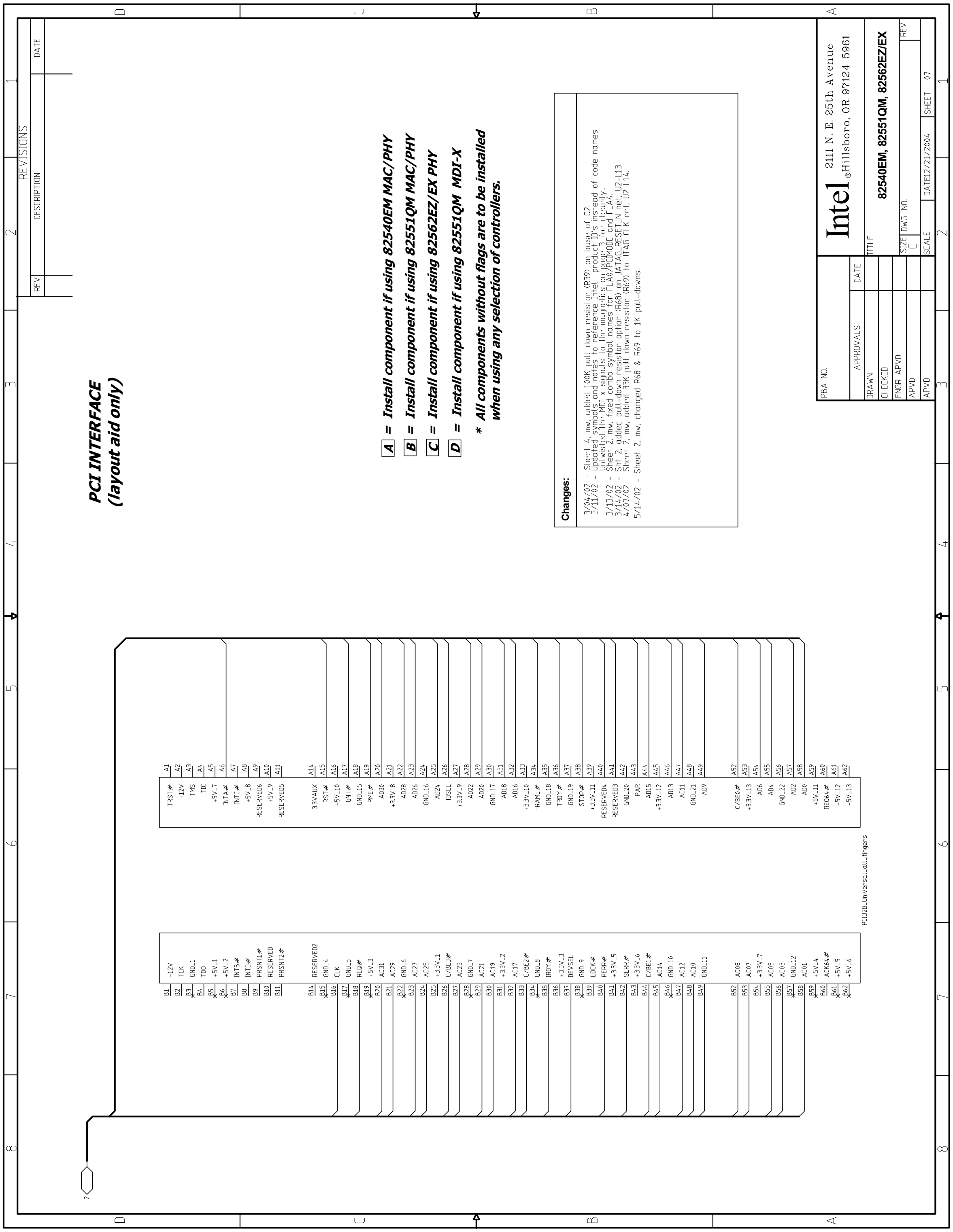

82540EM/82551QM/82562EZ/EX
Combo Symbol
10/100/1000 Mbps
Ethernet Controller
15mm x 15mm BGA
1mm Pitch
Pin Name Decode =
82540EM Signal Name - 82551QM Signal Name - 82562EX Signal Name
A = Install component if using 82540EM MAC/PHY
B = Install component if using 82551QM MAC/PHY
C = Install component if using 82562EZ/EX PHY
D = Install component if using 82551QM MDI-X
* All components without flags are to be installed when using any selection of controllers.
Intel
2111 N. E. 25th Avenue
Hillsboro, OR 97124-5961
82540EM, 82551QM, 82562EZ/EX
REVISIONS
DESCRIPTION
DATE
APPROVALS
DRAWN
CHECKED
ENGR APVD
APVD
SIZE
DWG NO.
REV
SCALE
SHEET 02
DATE12/21/2004

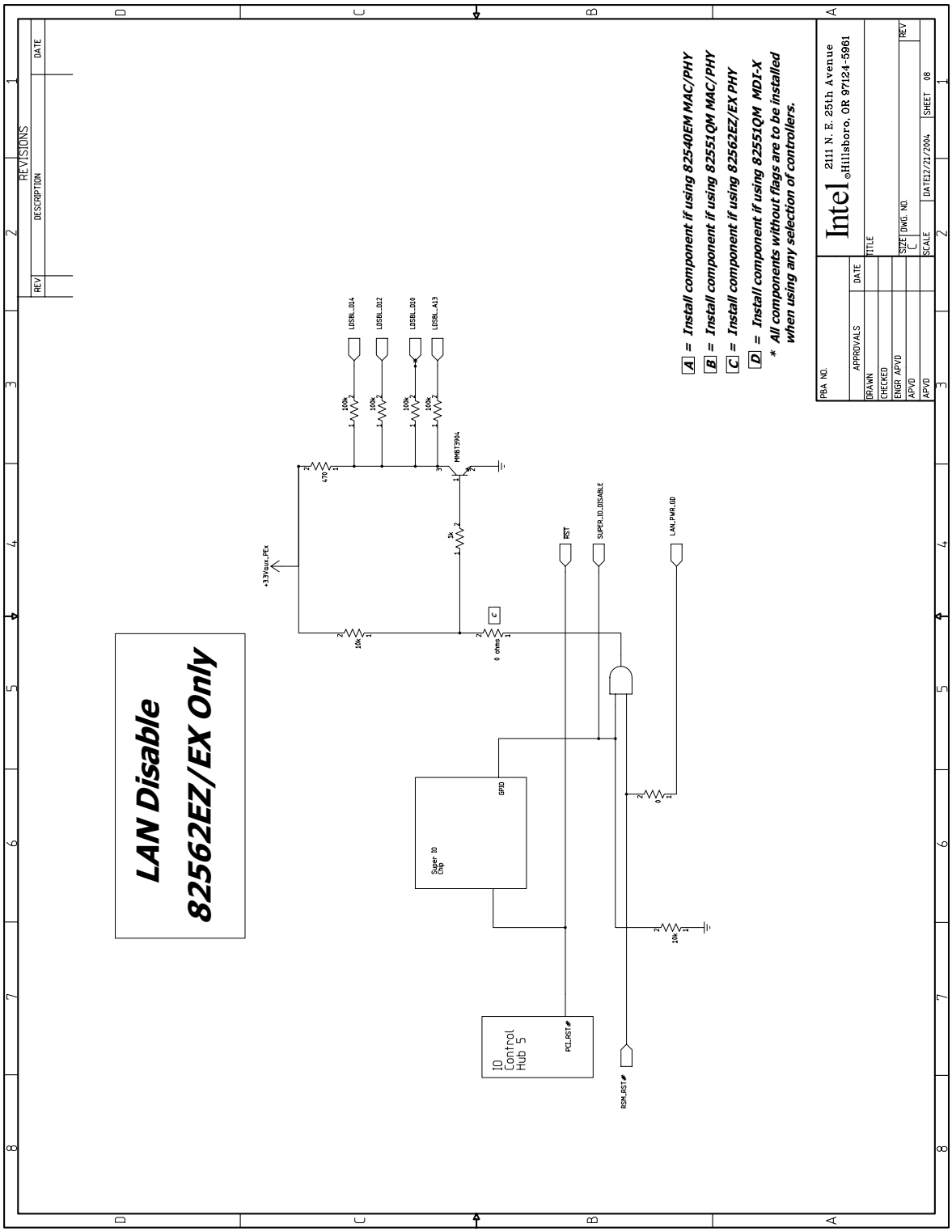

Gigabit Design
Note: For reference only. Use in conjunction with sheet 4 for dual footprint designs.
REVISIONS
REV
DESCRIPTION
DATE
PULSE H5007
T1
XFMR LAN1000 BASE T,SMT,24 Pins,SINGLE
HIGH VOLTAGE 1500PF CAP IS OPTIONAL
These three capacitors across the CHASSIS_GND to GND split, are located above the magnetics module. Place as close as possible to the magnetics module.
These three capacitors across the CHASSIS_GND to GND split, are located below the magnetics module. Place as close as possible to the magnetics module.
Some of the capacitors across the CHASSIS_GND to GND plane split may not be populated.
Intel
2111 N. E. 25th Avenue
Hillsboro, OR 97124-5961
82540EM, 82551QM, 82562EZ/EX


10/100 Design
PULSE H1267
PULSE H1338
HIGH VOLTAGE 1500PF CAP IS OPTIONAL
Some of the capacitors across the CHASSIS_GND to GND plane split may not be populated.
These three capacitors across the CHASSIS_GND to GND split, are located above the magnetics module. Place as close as possible to the magnetics module.
These three capacitors across the CHASSIS_GND to GND split, are located below the magnetics module. Place as close as possible to the magnetics module.
Do no stuff for 82551QM MDI-X
B = Install component if using 82551QM MAC/PHY
C = Install component if using 82562EZ/EX PHY
D = Install component if using 82551QM MDI-X
* All components without flags are to be installed when using any selection or controllers.
82540EM, 82551QM, 82562EZ/EX
Intel
2111 N. E. 25th Avenue
Hillsboro, OR 97124-5961


10/100/1000 PHY Interface with
Integraded Magnetics & RJ45
COPPER LAN
10/100/1000 Mbps Compatible Connector
1 GbE version (USB Ports not shown)
Connector also includes 2 USB ports. Pins not shown on this symbol.
LINK/ACTIVITY LED
ACTIVITY
BLINK
BI-COLOR SPEED LED
10 Mbps
100 Mbps
1000 Mbps
GREEN
YELLOW
Common-mode filter
For the 82551QM and 82562EZ/EX, differential pairs are terminated using 54.9 ohm 1% resistors.
Do not stuff for 82551QM MDI-X Mode
These three capacitors across the CHASSIS_GND to GND split, are located above the magnetics module. Place as close as possible to the magnetics module.
REVISIONS
REV
DESCRIPTION
DATE
Intel ©Hillsboro, OR 97124-5961
2111 N. E. 25th Avenue
APPROVALS
DRAWN
CHECKED
ENGR APVD
APVD
APVD
PBA NO.
TITLE
82540EM, 82551QM, 82562EZ/EX
SIZE
C
DWG NO.
REV
SCALE
DATE12/21/2004
SHEET 05
A = Install component if using 82540EM MAC/PHY
B = Install component if using 82551QM MAC/PHY
C = Install component if using 82562EZ/EX PHY
D = Install component if using 82551QM MDI-X
* All components without flags are to be installed when using any selection of controllers.


2.5V & 1.5V POWER REGULATION
LED & CRYSTAL CIRCUITS
REVISIONS
REV
DESCRIPTION
DATE
DS1 LINK/ACTIVITY LED
LINK GREEN
ACTIVITY BLINK
DS2 BI-COLOR SPEED LED
10 Mbps OFF
100 Mbps GREEN
1000 Mbps YELLOW
LINK_UP_N
ACTIVITY_N
LNK1000_N
LNK100_N
330ohms
0ohms
3.3V_AUX
VCC2.5
VCC1.5
BCP69T1
51Kohms
100K
10ohms 1/4W
4.7uF
0.1uF
10uF
10nF
50V
22pF
25M
25 Mhz Crystal
GND
A/C
This device should be placed as close as possible to the crystal input pins of the 82540EM Ethernet Controller. Keep traces short as possible and approximately the same length.
To save space resistor land patterns could be reduced to 3 pads each for signals X1 & X2. Resistor would be installed across common crystal pad and either 82540EM, 82562EZ/EX or 82551QM inputs.
R41 may require multiple 1210 size packages to dissipate the power.
A = Install component if using 82540EM MAC/PHY
B = Install component if using 82551QM MAC/PHY
C = Install component if using 82562EZ/EX PHY
D = Install component if using 82551QM MDI-X
* All components without flags are to be installed when using any selection of controllers.
Install power transistors Q1 & Q2 and support components only when using 82540EM Controller.
PBA NO.
APPROVALS
DATE
DRAWN
CHECKED
ENGR APVD
APVD
APVD
Intel
2111 N. E. 25th Avenue
Hillsboro, OR 97124-5961
TITLE
82540EM, 82551QM, 82562EZ/EX
SIZE
C
DWG. NO.
REV
01
SCALE
DATE12/21/2004
SHEET
06


PCI INTERFACE
(layout aid only)
A = Install component if using 82540EM MAC/PHY
B = Install component if using 82551QM MAC/PHY
C = Install component if using 82562EZ/EX PHY
D = Install component if using 82551QM MDI-X
* All components without flags are to be installed when using any selection of controllers.
Changes:
3/04/02 - Sheet 4, mw, added 100K pull down resistor (R39) on base of Q2.
3/11/02 - Updated symbols and notes to reference Intel product ID's instead of code names.
Untwisted the MDI_x signals to the magnetics on page 3 for clearity..
3/13/02 - Sheet 2, mw, fixed combo symbol names for FLA0/PCIMODE and FLA4.
3/14/02 - Sht 2, added pull-down resistor option (R68) on JATAG_RESET_N net, U2-L13.
4/07/02 - Sheet 2, mw, added 33K pull down resistor (R69) to JTAG_CLK net, U2-L14.
5/14/02 - Sheet 2, mw, changed R68 & R69 to 1K pull-downs.
PCI32B_Universal_all_fingers
REVISIONS
REV
DESCRIPTION
DATE
PBA NO.
APPROVALS
DATE
DRAWN
CHECKED
ENGR APVD
APVD
APVD
Intel
2111 N. E. 25th Avenue
Hillsboro, OR 97124-5961
TITLE
82540EM, 82551QM, 82562EZ/EX
SIZE C
DWG. NO.
REV
SCALE
DATE 12/21/2004
SHEET 07


LAN Disable
82562EZ/EX Only
A = Install component if using 82540EM MAC/PHY
B = Install component if using 82551QM MAC/PHY
C = Install component if using 82562EZ/EX PHY
D = Install component if using 82551QM MD1-X
* All components without flags are to be installed when using any selection of controllers.
REVISIONS
REV
DESCRIPTION
DATE
Intel
2111 N. E. 25th Avenue
Hillsboro, OR 97124-5961
PBA NO.
APPROVALS
DATE
DRAWN
CHECKED
ENGR APVD
APVD
APVD
TITLE
SIZE
C
DWG. NO.
REV
SCALE
DATE12/21/2004
SHEET 08
LDSBL_D14
LDSBL_D12
LDSBL_D10
LDSBL_A13
100k
470
MMBT3904
1k
+3.3Vaux_PEx
10k
0 ohms
C
RST
SUPER_IO_DISABLE
LAN_PWR_GD
Super IO Chip
GPIO
IO Control Hub 5
PCI_RST#
RSM_RST#

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Appendix A Measuring LAN Reference Frequency Using a Frequency Counter

A.1 Background

To comply with IEEE specifications for 10/100 Mbps and 10/100/1000Base-T Ethernet LAN, the transmitter reference frequency must be correct and accurate within ±50 parts per million (ppm).

Note: Intel recommends a frequency tolerance of ±30 (ppm).

Most Intel LAN devices will operate properly with a 25.000 MHz reference crystal, provided it meets the recommended requirements for frequency stability, equivalent series resistance at resonance (ESR), and load capacitance.

Most circuits for series resonant crystals include two discrete capacitors (typically C1 and C2), with values between 5 pF and 36 pF.

The most accurate way to determine the appropriate value for the discrete capacitors is to install the approximately correct values for C1 and C2. Next, a frequency counter should be used to measure the transmitter reference frequency (or transmitter reference clock).

- If the transmitter reference frequency is more than 20 ppm below the target frequency, then the values for C1 and C2 are too big and should be decreased.
- If the transmitter reference frequency is more than 20 ppm above the target frequency, then the values for C1 and C2 are too small and should be increased.

This Appendix provides instructions and illustrations that explain how to use a frequency counter and probe to determine the Ethernet LAN device transmit center frequency. An example describing how to calculate the frequency accuracy of the measured and averaged center frequency with respect to the target center frequency is also included.

A.2 Required Test Equipment

- Tektronix CMC-251, or similar high resolution, digital counter
- Tektronix P6246, or similar high bandwidth, low capacitance (less than 1 pF) probe
- Tektronix 1103, or similar probe power supply or probe amplifier
- BNC, 50 Ω coaxial cable (less than 6 feet long)
- System with power supply and test software for the LAN circuit to be tested

A.3 Indirect Probing Method

The indirect probing test method is applicable foremost devices that support 100BASE-T. Since probe capacitance can load the reference crystal and affect the measured frequency, the preferred method is to use the indirect probing test method when possible.

Almost all Intel LAN silicon that support 1000BASE-T Ethernet can provide a buffered 125 MHz clock, which can be used for indirect probing of the transmitter reference clock. The buffered 125 MHz clock will be a 5X multiple of the crystal circuit's reference frequency (Figure 12).

Different LAN devices may require different register settings, to enable the buffered 125 MHz reference frequency. Please obtain the settings or instructions that are appropriate for the LAN controller you are using.

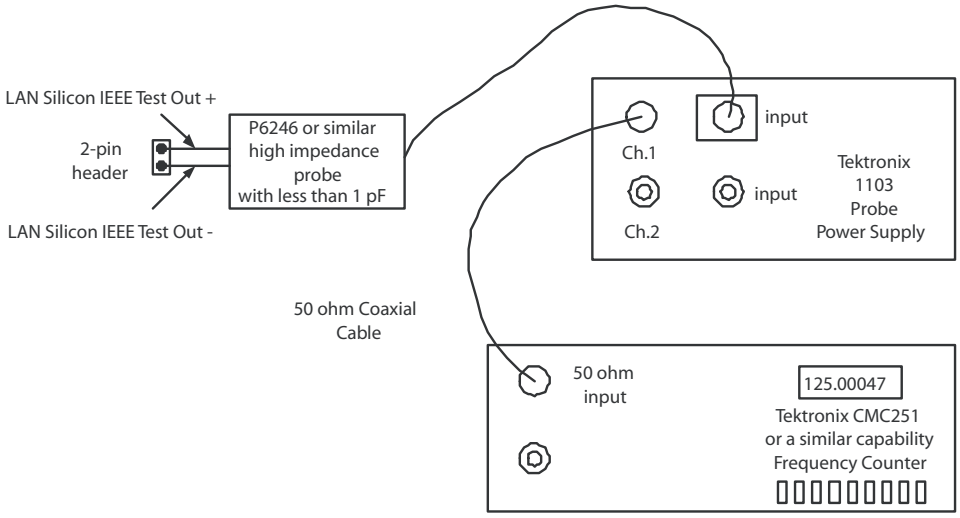

Figure 12. Indirect Probing Setup

A.4 Indirect Frequency Measurement and Frequency Accuracy Calculation Steps

1. Make sure the system BIOS has the LAN controller enabled.
2. Connect the test equipment as shown in Figure 12.
3. Using the appropriate controls for your model of high resolution digital counter, make sure it can display ~125.0000 MHz with at least four decimal places frequency resolution.
4. Enable the 125 MHz buffered reference clock.
5. Determine the center reference frequency as accurately as possible. This can be done by taking 30 to 50 different readings using the frequency counter and then calculating the average results of the readings.
6. Calculate the accuracy of the measured and averaged center frequency with respect to an ideal 125.0000 MHz reference frequency.

$$FrequencyAccuracy(ppm) = \frac{(x-y)}{(y/1000000)}$$

where x = Average measured frequency in Hertz and
y = Ideal reference frequency in Hertz

Example 1.

Given: The measured averaged center frequency is 124.99942 MHz (or 124,999,420 Hertz).

$$FrequencyAccuracy(ppm) = \frac{(124999420 - 125000000)}{(125000000/1000000)} = -4.64ppm$$

Example 2.

Given: The measured averaged center frequency is 125.00087 MHz (or 125,000,870 Hertz).

$$FrequencyAccuracy(ppm) = \frac{(125000870 - 125000000)}{(125000000 / 1000000)} = 6.96ppm$$

Note: The following items should be noted for an ideal reference crystal on a typical printed circuit board.

- If the transmitter reference frequency is more than 8 ppm below the target frequency, then the values for C1 and C2 are too big and they should be decreased. When tests are performed across temperature, it may be acceptable for the center frequency deviation to be a little greater than 8 ppm.
- If the transmitter reference frequency is more than 8 ppm above the target frequency, then the values for C1 and C2 are too small and they should be increased. When tests are performed across temperature, it may be acceptable for the center frequency deviation to be a little greater than 8 ppm.

A.5 Direct Probing Test Method, Applicable for Most 10/100 Devices (Devices that do NOT support 1000Base-T)

Because probe capacitance can load the reference crystal affecting the measured frequency, it is preferable to use a probe with less than 1 pF capacitance.

The probe should be connected between the X2 (or Xout) pin of the LAN device and a nearby ground. Typically, it is possible to connect the probe pins across one of the discrete load capacitors (C2 in Figure 13).

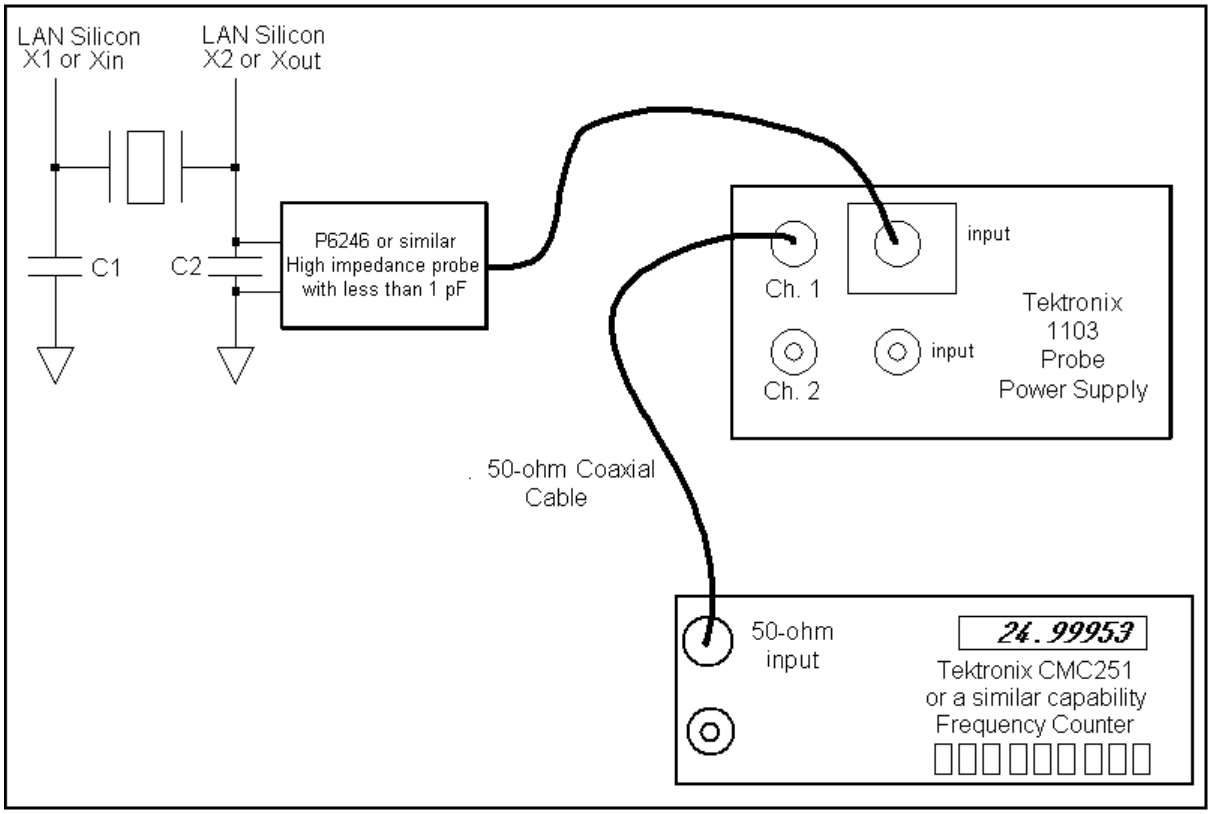

Figure 13. Direct Probing Method

A.6 Direct Frequency Measurement and Frequency Accuracy Calculation Steps

1. Make sure the system BIOS has the LAN controller enabled.
2. Connect the test equipment as shown in Figure 13.
3. Using the appropriate controls for your model of high resolution digital counter, make sure it can display ~25.0000 MHz with at least four decimal places frequency resolution.
4. Ensure the LAN circuits are powered.
5. Determine the center reference frequency as accurately as possible. This can be done by taking 30 to 50 different readings using the frequency counter and then calculating the average results of the readings.
6. Calculate the accuracy of the measured and averaged center frequency with respect to an ideal 25.0000 MHz reference frequency.

$$FrequencyAccuracy(ppm) = \frac{(x - y)}{(y / 1000000)}$$

where x = Average measured frequency in Hertz and
y = Ideal reference frequency in Hertz

Example 3.

Given: The measured averaged center frequency is 24.99963 MHz (or 24,999,630 Hertz).

$$FrequencyAccuracy(ppm) = \frac{(24999630 - 25000000)}{(25000000 / 1000000)} = -14.8ppm$$

Example 4.

Given: The measured averaged center frequency is 25.00027 MHz (or 25,000,270 Hertz).

$$FrequencyAccuracy(ppm) = \frac{(25000270 - 25000000)}{(25000000 / 1000000)} = 10.8ppm$$

Note: The following items should be noted for an ideal reference crystal on a typical printed circuit board.

- If the transmitter reference frequency is more than 8 ppm below the target frequency, then the values for C1 and C2 are too big and they should be decreased. When tests are performed across temperature, it may be acceptable for the center frequency deviation to be a little greater than 8 ppm.
- If the transmitter reference frequency is more than 8 ppm above the target frequency, then the values for C1 and C2 are too small and they should be increased. When tests are performed across temperature, it may be acceptable for the center frequency deviation to be a little greater than 8 ppm.