



Tuning the 8255x Controller's Equalizer for Capacitor-Coupled Applications

Application Note (AP-435)



Revision History

| Revision | Revision Date | Description |
|----------|---------------|--------------------------------|
| 1.1 | Nov 2005 | Initial Release |
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1.0 Introduction

The adaptive equalizer is a key circuit block within the 8255x controller PHY unit. Its job is to restore the distorted MLT-3 signal received at the end of the wire to a waveform that can be used to reliably extract the 125 MHz clock and decode the data.

Equalization is a three-step process based on voltage, phase, and bit error detection. Normally, the equalizer performs adaptation on a received signal that traversed a length of balanced CAT5 cable and passed through two magnetics modules along the way. The equalizer is optimized to amplify this specific signal for a range of cable lengths from zero to 100 meters. Equalizer adaptation occurs every time the PHY attempts to establish link.

When the 8255x controller is used in a point-to-point or backplane application, the differential pairs are typically connected to a link partner through circuit board traces and AC coupling capacitors instead of through magnetics modules and CAT5 cables. With capacitive coupling, “looks” like a high pass filter instead of the low pass filter presented by transformer-based connections. The MLT-3 signal passing through a capacitive coupled circuit will be distorted differently than an MLT-3 signal passing through a transformer. Higher slew rate and higher signal overshoot suggest a very “strong” signal. The signal amplitude may be higher than a signal attenuated by cable, but it could be lower than expected for such steep rise and fall times.

The 8255x controller's adaptive equalizer can become confused by a received signal that is distorted in this way and it can make setting errors. If the equalizer is set for too much gain, the controller may exhibit failure to achieve link, loss of link or symbol errors. This Technical Advisory explains how to read the PHY equalizer settings and how to program the settings manually. If the 8255x controller in your system readily achieves link and receives data without errors, there is no need to adjust the equalizer settings, regardless of capacitive coupling on the analog pairs.

Note: The techniques described here rely on 8255x functions usually reserved for factory tests and validation. Implementation may require considerable testing by the user.

When tuning the adaptive equalizer, keep in mind that irregular trace impedance, transmitter clock jitter, and noise can also make it difficult for the PHY to lock on to the received signal. This document assumes that those potential problems have been ruled out.

2.0 Products Affected

| Product Description | Part Number | Comments |
|---|--|----------|
| 8255x family devices beginning with 82559 | 82559, 82559ER 82550EY, 82550GY 82550GM, 82550PM 82551QM, 82551ER | |

3.0 Reading and Setting the 8255x Controller Equalizer Configuration

The 8255x Equalizer Control and Status Register is MII Register #26 (1Ah) in the PHY. This register is arranged as a command port with many bit options. The high order three bits, Bits [15:13], comprise a write command opcode that denotes the access type (read status, force setting, set configuration) you are trying to perform. For writes, the write data is contained in specific bit fields. For reads, subsequent read operations return the data.

To read the equalizer status, perform the following operations:

| | |
|-----------------------|--|
| Write Reg 'h1A 'h8000 | {Command that requests loading the status values to the output port} |
| Read Reg 'h1A | {First read is dummy to reload output port with new data} |
| Read Reg 'h1A | {Valid status read} |
| Read Reg 'h1A | {Each following read provides new data in real time} |

The register bits have the following meanings for equalizer status:

| | |
|--------------|--|
| Bits [3:0] | Reserved |
| Bits [7:4] | Equalizer Zero Value. A “zero” value represents the equalizer gain setting. Zero = 0 means no gain and Zero = 'hF is maximum gain. For very short cables and short point-to-point board connections, the zero values should be 2 or less. If you observe larger zero values, the equalizer probably made an error. |
| Bit [8] | Signal Detect. This bit is asserted when the incoming signal exceeds the squelch threshold. |
| Bit [9] | Lock mechanism. This bit is asserted when the equalizer is locked on the correct zero. This mechanism is triggered in case of a symbol error. |
| Bit [10] | Equalizer Position. A one in this position indicates it is decrementing. Otherwise the bit will be 0. |
| Bits [15:11] | Reserved |

There are two ways to configure the equalizer and control its zero settings. You can *force* a zero by placing a fixed zero value (gain) into the equalizer. Alternatively, you can *set* a zero by placing a zero value, but still allow the zero value to change according to the adaptation algorithm. For configuration writes, the register bits have the following meanings:

| | |
|--------------|---|
| Bits [12:10] | Reserved |
| Bit [9] | Disable lock mechanism. Required for advanced jitter mode (see below). |
| Bits [8:6] | Reserved |
| Bit [5] | Set Zero Command |
| Bit [4] | Force Zero Command |
| Bit [3:0] | Equalizer Forced or Set Value. There are 16 possible values. For very short cables and short point-to-point board connections, test zero values in the range of 2 or less. The optimum value will depend on the output drive characteristics of the transmitter at the other end as well as the layout and termination of the receive analog pair. You may find more than one value that works satisfactorily. Perform tests on several units under a variety of operating conditions to optimize the zero value. |

To test the equalizer by *forcing* zeros, perform the following series of operations:

| | |
|-----------------------|--|
| Write Reg 'h1A 'h2010 | {Bits [15:13] = '001 denotes configuration write. Force zero value to 0} |
| Write Reg 'h1A 'h2011 | {Force zero value to 1} |
| Write Reg 'h1A 'h2012 | {Force zero value to 2} |
| ... | |
| ... | |
| Write Reg 'h1A 'h201F | {Force zero value to 'hF} |

To test the equalizer by *setting* zeros, perform the following series of operations:

| | |
|-----------------------|--|
| Write Reg 'h1A 'h2020 | {Bits [15:13] = '001 denotes configuration write. Set zero value to 0} |
| Write Reg 'h1A 'h2021 | {Set zero value to 1} |
| Write Reg 'h1A 'h2022 | {Set zero value to 2} |
| ... | |
| ... | |
| Write Reg 'h1A 'h202F | {Set zero value to 'hF} |

4.0 Advanced 8255x Controller Equalizer Tests

The 8255x controller PHY has an option to read the jitter value used in the adaptation algorithm. The read operation uses a 20-bit register. Before reading the jitter, force a zero value. For an application with short cables or point-to-point connections, repeat the process for zero values from 0 to 3. You can use this capability to identify an optimum zero value (lowest observed jitter) without relying on the external indication of acquiring or losing link.

To read the jitter value, perform the following operations:

| | |
|------------------------------|--|
| Write Reg 'h1A 'h2210 | { Disable lock mechanism and force zero value to 0.} |
| Write Reg 'h1A 'hA000 | {Command that requests high level jitter count output to Bits [19:4], OR} |
| Write Reg 'h1A 'hA001 | {Command that requests low level jitter count output to Bits [19:4]} |
| Read Reg 'h1A | {First read is dummy to reload output port with new data.} |
| Read Reg 'h1A | {Valid accumulated jitter read.} |
| Read Reg 'h1A | {Each following read provides new data in real time.} |
| Write Reg 'h1A 'h2211 | {Disable lock mechanism and force zero value to 1. Try several values.} |

The register bits have the following meanings for equalizer jitter:

| | |
|--------------------|--|
| Bits [15:0] | Accumulated Jitter. Output if a low level jitter count is requested. For a low level jitter count, Bits [19:16] are always 0. |
| Bits [19:4] | Accumulated Jitter. Output if a high level jitter count is requested. For a high jitter count, Bits [19:16] are valid. |

The PHY also has an equalizer probe mode that allows the equalizer output to be placed on an external pin for viewing on an oscilloscope. This output has been sampled internally by the recovered clock and it represents the incoming data in the receiver. Attach the scope probe to the Speed LED output pin and use the link partner's transmit clock as a trigger. Probe mode does not disrupt normal PHY operation.

Set up the scope to view an eye pattern, looking for a clean pattern with a large eye opening (>1.5ns). As long as the pattern is good, the system should have no receive errors. If there are errors anyway, check first for jitter in the 8255x controller's clock.

To read the jitter value, write a '1' to Bit 12 in Register 18:

| | |
|------------------------------|------------------------------------|
| Write Reg 'h12 'h1000 | {Sets equalizer probe mode} |
|------------------------------|------------------------------------|

5.0 Utilizing the Equalizer Tuning Capability

In a capacitor-coupled point-to-point or backplane Ethernet system, it is acceptable to force a particular equalizer setting as long as you know the link partner and signal path cannot change. If the system allows different link partners to be plugged into connectors, it is probably impractical to determine optimum PHY equalizer values to accommodate all the possible partners.

There are several circuit changes that can be made instead of relying on equalizer adjustments. If you make circuit changes, you can read the equalizer zero value to see how the equalizer is responding. For transformerless designs with the 8255x controller, consider the following experiments:

- Add shunt capacitance across the differential pair at the receiver to attenuate the signal slightly and round off edges. Suggested values are in the range of 10pF to 27pF.
- If the transmitter's output buffer is current-sourced through the analog pair, bias the buffer through inductors instead of resistors. From the transmitter end, the DC path will "look" more like the primary of the missing transformer. This change may result in a less distorted waveform. A suggested starting value is 150μH.
- Modify the value of the AC coupling capacitors. Suggested values are in the range of 0.1μF to 0.3μF.
- Terminate the receive pair by using two 50Ω resistors with a 0.01mF common mode bypass capacitor to ground, instead of the single 120Ω resistor typically used with 8255x controllers.
- Adjust the amplitude of the transmitted signal at the transmitter. For point-to-point connections, reducing the amplitude may be useful for troubleshooting. However, it is recommended that the final configuration operate with a nominal 1000mV differential signal.