82559 LAN on Motherboard (LOM) Design Guide

Application Note (AP-392)

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Revision History

Revision Date	Revision	Description
June 1998	1.0	First release.
July 1998	1.1	Added Section 8.0, "Signal Descriptions" on page 12, Section 9.0, "Package and Pinout Information" on page 18, and Section 10.0, "Bill of Materials" on page 22.
November 1998	1.2	Incorporated new schematics.
December 1998	1.3	Final B5-Step Schematics Added
January 1999	1.4	Initial Public Release - removed references to AP-393

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1.0 Introduction

The 82559 provides: a higher level of integration, enhanced features set, reduced power consumption, and small footprint (15 mm by 15 mm). The 82559 has been optimized to accelerate the integration of LAN into desktop, server, PC cards, docking stations (port replicators), and mobile platforms.

1.1 Scope

This application note covers the design of the 82559 into a platform based on Intel's PCI to ISA/ IDE Xcelerator 4 (PIIX4). The 82559 will reduce cost, power, and real estate in existing LAN On Motherboard (LOM) designs. Platform designs for other chipsets are available from your Intel representative.

1.2 Reference Documents

This application note assumes that the designer has a working knowledge of high-speed design and layout issues. A knowledge of the Advanced Configuration and Power Interface (ACPI) Specification and power management industry initiatives is valuable prior to beginning the integration of the 82559 into any platform. The following reference list provides sufficient background material.

- PCI Specification, PCI Special Interest Group.
- Network Device Class Reference, Revision 1.0, Intel Corporation, Microsoft Corporation, and Toshiba.
- Advanced Configuration and Power Interface (ACPI) Specification, Intel Corporation, Microsoft Corporation, Toshiba.
- Advanced Power Management (APM) Specification, Intel Corporation and Microsoft Corporation.
- 82559 Fast Ethernet Multifunction PCI/CardBus Controller Datasheet, Intel Corporation.
- LAN On Motherboard (LOM) Design Guide Application Note (AP-391), Intel Corporation.
- WOL Header Recommendations, Intel Corporation.

2.0 PCI Interface

The 82559 provides a direct (glueless) 32-bit interface to the PCI bus. Prior to configuration, the 82559 operates as a simple slave device. After the device has been configured all data transactions with the device are through memory structures in system memory. The PCI interface must be enabled for bus mastering for normal operation. Address, data, and control signals are as defined in the PCI Specification. Additional clarification of the PCIMODE, CLKRUN#, RST#, PME#, WOL, ISOLATE#, ALTRST#, and VIO pins are provided in the following sections.

2.1 PCI Mode

Flash Address[0] (FLA0) doubles as the bus mode select pin during PCI reset. The PCIMODE# input signal (sampled during PCI RST#) determines whether the 82559 operates as a PCI or CardBus device. If this signal is sampled low when the RST# is active, the 82559 will operate as a PCI device; if sampled high, then a CardBus device. In a LOM design the pin is either left open (internal pull-down), pulled low (through a resistor), or connected to a Flash device. It should be pulled high only in a CardBus design.

2.2 Clockrun Operations

The CLKRUN# signal is used by the system to pause or slow down the PCI Clock signal and by the 82559 to enable and disable PCI Clock signal suspension or to request a restart of the PCI clock. If clockrun is not used, this pin should be pulled low through a resistor (the reference design provided in Section 11.0, “Appendix A: 82559/PIIX4 LOM Designs” on page 23 uses a value of 62 KΩ). Pull-down resistor values were selected based on the requirements of Intel’s Nand-tree test equipment. If the Nand-tree test capabilities of the 82559 are not used then any reasonable value will be adequate, i.e. 1- 10 KΩ.

2.3 Reset Considerations

The 82559 can maintain a virtual connection to the network regardless of the power state of the system. Therefore, the state of the PCI bus signals can be undefined when the 82559 is operating from auxiliary power. The 82559 response to a reset event varies based on operational mode. The 82559 provides three signals that enable the device to operate correctly in these environments. Connections to these signals vary based on system implementation.

2.3.1 PCI Reset

The PCI Reset (RST#) signal is used to put PCI registers, sequencers, and signals in a consistent state. When the RST# signal is asserted, all PCI output signals are tri-stated. In LOM designs the 82559’s RST# pin would normally be connected to the PCI Reset pin.

Note: In designs where an signal to drive the ISOLATE# pin on the 82559 is not available, the PCI reset signal may be routed to the ISOLATE# pin. In these designs the RST# pin on the 82559 would be pulled-up to the 82559’s power rail through a 3.3 KΩ resistor.

2.3.2 ALTRST#

ALTRST# is the power-on reset signal to the 82559. This signal is required due to the unique functionality provided by the 82559 when the system is in a low power state. ALTRST# is used to provide a complete reset to the 82559 on power-up. In systems that support V_{AUX}, ALTRST# should be connected to a power-up detection circuit (i.e. 3.3V_standby powergood indication). In systems that do not have an auxiliary power source, the ALTRST# pin should be tied to the 82559's V_{CC} (3.3V) power-rail. The reference design in Section 11.0, "Appendix A: 82559/PIIX4 LOM Designs" on page 23 shows the ALTRST# pin connected to a signal called AUX_GOOD. This signal should be asserted low whenever the auxiliary power is not available. The AUX_GOOD signal can be generated by a power supply supervisory circuit, and the 82559 will be completely reset anytime the signal is asserted low.

2.3.3 ISOLATE#

The ISOLATE# signal is used to isolate the 82559 from the PCI bus. When ISOLATE# is asserted, the 82559 will not drive its PCI output signals (excluding the PME# and CSTSCHG signals) and ignores PCI input signals (including the RST# and CLK signals). If V_{AUX} is not supplied, then the ISOLATE# pin should be left unconnected. In designs which do not shut down the PCI bus (such as the reference design provided in Section 11.0, "Appendix A: 82559/PIIX4 LOM Designs" on page 23), the ISOLATE# pin should be connected to the PCI Reset signal. The ISOLATE# signal must be driven low (active) prior to the assertion of the PCI_Power_Good signal. As the PCI bus is re-activated, the ISOLATE# signal must be driven active until the PCI bus is completely stable. The following diagram depicts timing relationship in a visual form:

Figure 1. Power Good Signal to Isolate Signal Relationship

Note: In designs where an signal to drive the ISOLATE# pin on the 82559 is not available, the PCI reset signal may be routed to the ISOLATE# pin. In these designs the RST# pin on the 82559 would pulled-up to the 82559's power rail through a 3.3 KΩ resistor.

2.4 Setting PCI Signal Levels

Although the 82559 is a 3.3 V part, it is tolerant of 5 V signals on its PCI/CardBus interface. The signaling level of the bus is detected at reset by sensing the voltage on the VIO pin. The VIO pin should be pulled up to a 5 Volt PCI voltage source through a resistor (a 3.3- 10KΩ is adequate). All other pins on the 82559 are not 5 volt tolerant.

3.0 Wake-up Events

The 82559 provides two output signals to alert the system of a wake-up event, PME# and CSTSCHG (WOL). In ACPI compliant designs, the PME# pin alerts the system of any incoming event; and CSTSCHG, in CardBus systems. The WOL pin acts as an active high Wake on LAN (WOL) signal when used in PCI systems. This alleviates the need for external circuitry to create the WOL signal in Advanced Power Management (APM) designs. The WOL header requirements document is available from the wired for management website at http://developer.intel.com/ial/WfM/index.htm.

3.1 ACPI Designs

The Power Management Event signal is an active low, open drain signal that indicates an event in ACPI compliant systems. It is usually connected to the General Purpose Input/Output 1 (GPIO1) signal of the PIIX. In an ACPI compliant system, the Power Management Event signal is common to all PCI devices. Since the signal is driven from open drain sources, a single pull-up resistor to the 3.3 V_{AUX} must be provided. If configured, the 82559 will assert PME# anytime the system needs to be woken up.

The 82559 was designed to be fully ACPI Specification compliant. The ACPI specification requires that PCI devices implement a power management event signal. The 82559 implements this through its PME# pin. For the 82559 to function properly in an ACPI context, the PME# signal should be connected to a pin on the PIIX4 device that resides in the resume well and is capable of generating a System Control Interrupt (SCI). In a PIIX4 design, which is intended to be both APM and ACPI compliant, it is recommended that the PME# signal is connected to the General Purpose Input 1 (GPI1) PIIX4 pin. The GPI1 signal is capable of generating both a SCI and System Management Interrupt (SMI) making it the ideal pin to use.

Note: As per the ACPI specification, the 82559 will not generate a follow-on wake-up indication until the device is re-armed. The re-arming is accomplished by clearing the PME bit

3.2 Advanced Power Management Designs

The Wake on LAN pin provides the active high signal that wakes the system in APM designs. This signal is distributed via a 3-pin header in network interface card (adapter) implementations. The WOL signal is not necessary in LOM designs because it provides the same indication as the PME# signal (albeit active high). However, in adapter designs it can be used to build a card that provides both signal levels. If APM support is desired, then the PME# or WOL pin must be routed to a pin on the chipset capable of generating a SMI while the chipset is powered only from an auxiliary power source.

It is recommended that the incoming signal from the WOL header is routed to a separate input on the PIIX4. The use of separate inputs provides the ability to interrogate the PIIX4 device once the system has powered up and discern the source of the wake event. The LID input of the PIIX4 is recommended since it resides in the resume well and is capable of generating a SMI or SCI.

4.0 Local Memory Ports

The 82559 supports both a serial EEPROM for configuration information and a parallel Flash for user data. In most designs, the Flash interface is used for expansion ROM, such as Preboot Execution Environment (PXE) code.

4.1 Serial EEPROM

The serial EEPROM of the 82559 provides storage for initialization, the heartbeat packet in managed designs, and the Card Information Structure (CIS) in CardBus designs. The EEPROM interface consists of the following signals:

- EEPROM Data Input (EEDO)

  The EEDO pin is multiplexed with the Flash Address[14] pin and acts as the serial input data pin to the EEPROM Data Output signal.

- EEPROM Data Output (EEDI)

  The EEDI pin is multiplexed with the Flash Address[13] pin and acts as the serial output data pin to the EEPROM Data Input signal.

- EEPROM Serial Clock (EESK)

  The EESK pin is a multiplexed with the Flash Address[15] pin and acts as the serial clock output to the EEPROM.

- EEPROM Chip Select (EECS)

  The EECS pin is used to assert chip select to the serial EEPROM.

In unmanaged (TCO controllerless) PCI designs (such as the reference design provided in Section 11.0, “Appendix A: 82559/PIIX4 LOM Designs” on page 23), a 64-word device is required. The EEPROM must be 3.3 V powered in order to operate with the 82559.

4.2 Flash Interface

The 82559 support a glueless interface to an 8-bit wide (128 Kbyte), 3.3 V parallel memory device. This port can be used for a 128 Kbyte Flash or any other parallel 8-bit device which meets the 82559’s AC timing. The reference design provided in Section 11.0, “Appendix A: 82559/PIIX4 LOM Designs” on page 23 depicts a Flash socket, which may not be required if there is no requirement for the system to boot from the LAN or if the PXE code will be stored in main flash.

The 82559 uses a number of the Flash address pins for auxiliary functions based on the configuration or the state of the device reset. The 82559 Datasheet contains additional details regarding these secondary pin functions.

5.0 Test Port

The 82559 uses an internal NAND tree configuration for test purposes. The Test Port is not normally accessed in LOM designs. The Test pin (pin A13) must be pulled low through a 4.7 KΩ resistor to place the device in normal operational mode.

6.0 82559 Board Design Considerations

6.1 Clock Source

The 82559 can operate from either its internal oscillator using a 25 MHz crystal or an external oscillator as a 25 MHz clock source. If a crystal is used, then it should be connected across the X1 and X2 input pins. If an external oscillator is used, then it can be connected directly to the X1 input, with X2 left unconnected. In both cases the clock should be accurate within 50ppm. The 82559 can also provide its internal clock as an output on the CLK25 pin (pin N9, which is multiplexed with FLA[16]). The clock out function is enabled by asserting the CLKEN pin during PCI reset. The CLKEN pin is multiplexed with FLA[7].

A sampling of crystals that meet the specifications outlined is listed below:

Manufacturer	Manufacturer's Part Number
Raltron	TT-SMDC-25.00-20-T
Epson-Seiko	MA-406-25.000M-20PF

6.2 LED Indicators

The 82559 provide three indication LED outputs:

- Link (LILED)
- Activity (ACTLED)
- Speed (SPEEDLED)

The 82559 can sink up to 10 mA of current for each LED.

6.3 Magnetics Selection

One of the most critical component choices in a 100 Mbps Ethernet design is the magnetics module. The module has a critical effect on overall IEEE and emissions compliance. The device selected should meet the performance required for a design. Occasionally, components that meet basic specifications may cause the system (LOM, adapter, repeater, etc.) to fail because of unintentional interactions with board effects. Examples of these phenomena could be an unexpected series or parallel capacitance values or unexpected series inductance values within the magnetics module. This could cause the overall design to fail certain IEEE specifications. Qualifying a new magnetics module can help to alleviate these sorts of issues. The three-step process outlined below is recommended when evaluating suppliers:

1. Verify vendor's specification.

   The component should have more margins than the system specification. For example, "Does the module have a minimum of 400 µH of open circuit inductance (OCL) with 8 mA of DC Bias?".

2. Check module's electrical qualifications.

   The electrical specifications of the module should be verified by performing stand-alone electrical qualification. Several modules should be tested (not in circuit) with two goals in mind:

a. Does the component meet the published specifications?

b. Does the vendor's published data correlate to the measured data?

3. Perform IEEE conformance tests

   System level IEEE PHY conformance and EMC (FCC and EN) testing should be done to verify that the system meets all electrical requirements with the new component.

A sampling of modules that meet the specifications outlined is listed below:

Manufacturer	Manufacturer's Part Number
Pulse Engineering	H1012T
Pulse Engineering	H1088
Pulse Engineering	H1138
Bel Fuse	S558-5999-46
Bel Fuse	S558-5999-K7

6.4 Trace Routing

Generic Trace routing considerations for final layout are described in the LAN On Motherboard (LOM) Design guide Application Note (AP-391). 82559 specific layout information can be found in the 82559 Printed Circuit Board (PCB) Design Application Note (AP-399). Critical layout issues are covered in the following section for completeness. Critical signal traces should be kept as short as possible to decrease the likelihood of being affected by high frequency noise from other signals, including those propagated through power and ground planes. Capacitive loading, which is caused by the signal trace, can also be reduced by keeping the traces as short as possible. Maximum separation between differential pairs should be no more than one tenth of an inch as illustrated in the figure below.

6.5 Signal Terminations

A single 100 Ω (1%) resistor is used to terminate the transmit differential (TDP/TDN) pair. For the receive differential (RDP/RDN) pairs, a 120 Ω (1%) resistor was utilized. The 120 Ω resistor was used in the layout of this design because of the improvements in receive performance, the designer may want to experiment with values from 100 Ω to 120 Ω on the receive side. They should be placed as close to the 82559 as possible.

6.5.1 Termination Plane

Resistors are used to terminate noise from the unused inputs of both the RJ45 connector and the magnetics module to the termination plane. The netname TERMPLANE (for termination plane) is provided as a guide to the termination plane. A termplane is a plane fabricated into the printed circuit board (PCB) substrate. This plane, which has no DC termination, acts like a capacitive path for the coupled noise.

6.5.2 Termination Plane Capacitance

It is recommended that the termination plane capacitance equal a minimum value of 1500 pF. This helps reduce the amount of cross-talk on the differential pairs (TDP/TDN and RDP/RDN) from the unused pairs of the RJ45. Pads may be placed for additional capacitance, which may be required due to failure of electrical fast transient testing. If 1500pf is not achievable, then the series capacitor may need to be populated.

6.6 Critical Dimensions

There are two critical dimensions that must be considered during the layout phase of an 82559 LOM implementation. These dimensions are identified in Figure 2 as A and B:

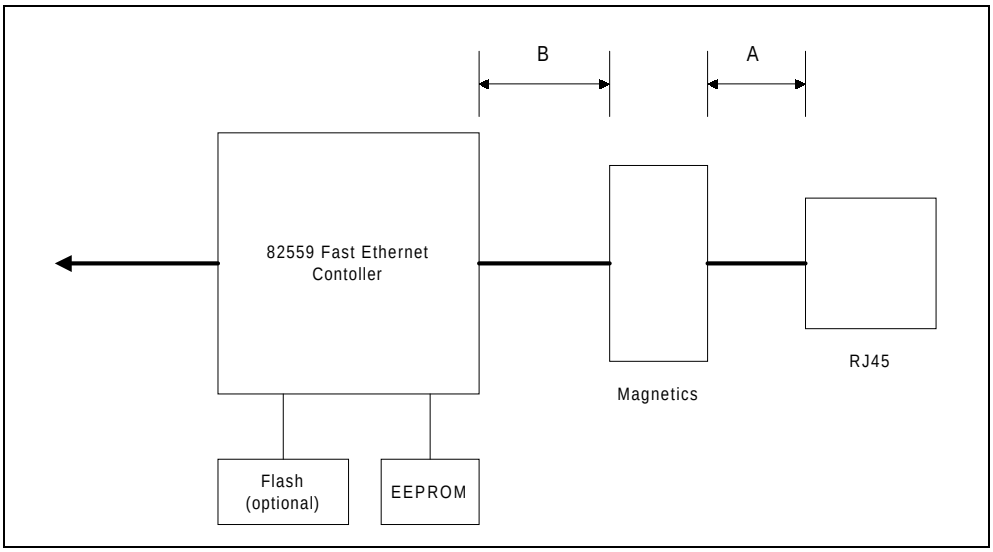

Figure 2. Critical Dimensions for Component Placement

6.6.1 Distance A: Magnetics to RJ45 (Priority 1)

The distance labeled “A” in Figure 2 should be given the highest priority in board layout. The distance between the magnetics module and the RJ45 connector should be kept to less than one inch of separation. The following trace characteristics are important and should be observed:

1. Differential Impedance: The differential impedance should be 100 Ω. The single ended trace impedance will be approximately 50 Ω; however, the differential impedance can also be affected by the spacing between the traces.
2. Trace Symmetry: Differential pairs (such as TDP and TDN) should be routed with consistent separation and with exactly the same lengths and physical dimensions (for example, width).

Caution: Asymmetrical and unequal length traces in the differential pairs contribute to common mode noise. This can degrade the receive circuit’s performance and contribute to radiated emissions from the transmit circuit.

If the 82559 must be placed further than a couple of inches from the RJ45 connector, distance B can be sacrificed. Keeping distance A as short as possible should be a priority.

6.6.2 Distance B: PHY to Magnetics (Priority 2)

Distance B from Figure 2 should also be designed to extend less than one inch between devices. The high speed nature of the signals propagating through these traces requires that the distance between these components are closely observed. In general, any section of traces that is intended for use with high speed signals should observe proper termination practices.

Proper termination of signals can reduce reflections caused by impedance mismatches between devices and traces. The reflections of a signal may have a high frequency component that may contribute more EMI than the original signal itself. For this reason, these traces should be designed to a 100 Ω differential value.

7.0 Power Supply Requirements

WOL designs require a segmented power supply. The auxiliary power supply (+3.3VSB) is used to provide the trickle power necessary to keep key components operational in WOL mode.

7.1 +3.3VSB Power Requirement

In designs that utilize 3.3VSB, the 82559 will operate from this supply in all operational states. Therefore, the +3.3VSB must be capable of supplying 175 mA of current (worst case requirements for the 82559).

7.2 +3.3VSB Power Recommendation

Ideally the power supply will provide an AUX_GOOD signal. The AUX_GOOD signal indicates that the auxiliary power supply is ready to provide stable power and is similar to the PWR_GOOD signal on many of today's common power supplies.

Note: The AUX_GOOD signal from the power supply is the same as the ALTRST# signal of the 82559.

8.0 Signal Descriptions

8.1 Signal Type Definitions

Type	Name	Description
IN	Input	The input pin is a standard input only signal.
OUT	Output	The output pin is a Totem Pole Output pin and is a standard active driver.
T/S	Tri-State	The tri-state pin is a bidirectional, input/output pin.
S/T/S	Sustained Tri-State	The sustained tri-state pin is an active low tri-state signal owned and driven by one agent at a time. The agent asserting the S/T/S pin low must drive it high at least one clock cycle before floating the pin. A new agent can only assert an S/T/S signal low one clock cycle after it has been tri-stated by the previous owner.
O/D	Open Drain	The open drain pin allows multiple devices to share this signal as a wired-OR.
A/I	Analog Input	The analog input pin is used for analog input signals.
A/O	Analog Output	The analog output pin is used for analog output signals.
B	Bias	The bias pin is an input bias.

8.2 PCI Bus and CardBus Interface Signals

8.2.1 Address and Data Signals

Symbol	Type	Name and Function
AD[31:0]	T/S	**Address and Data.** The address and data lines are multiplexed on the same PCI pins. A bus transaction consists of an address phase followed by one or more data phases. During the address phase, the address and data lines contain the 32-bit physical address. For I/O, this is a byte address; for configuration and memory, it is a Dword address. The 82559 uses little-endian byte ordering (in other words, AD[31:24] contain the most significant byte and AD[7:0] contain the least significant byte). During the data phases, the address and data lines contain data.
C/BE[3:0]#	T/S	**Command and Byte Enable.** The bus command and byte enable signals are multiplexed on the same PCI pins. During the address phase, the C/BE# lines define the bus command. During the data phase, the C/BE# lines are used as Byte Enables. The Byte Enables are valid for the entire data phase and determine which byte lanes carry meaningful data.
PAR	T/S	**Parity.** Parity is even across AD[31:0] and C/BE[3:0]# lines. It is stable and valid one clock after the address phase. For data phases, PAR is stable and valid one clock after either IRDY# is asserted on a write transaction or TRDY# is asserted on a read transaction.Once PAR is valid, it remains valid until one clock after the completion of the current data phase. The master drives PAR for address and write data phases; and the target, for read data phases.

8.2.2 Interface Control Signals

Symbol	Type	Name and Function
FRAME#	S/T/S	**Cycle Frame.** The cycle frame signal is driven by the current master to indicate the beginning and duration of a transaction. FRAME# is asserted to indicate the start of a transaction and de-asserted during the final data phase.
IRDY#	S/T/S	**Initiator Ready.** The initiator ready signal indicates the bus master's ability to complete the current data phase and is used in conjunction with the target ready (TRDY#) signal. A data phase is completed on any clock cycle where both IRDY# and TRDY# are sampled asserted (low) simultaneously.
TRDY#	S/T/S	**Target Ready.** The target ready signal indicates the selected device's ability to complete the current data phase and is used in conjunction with the initiator ready (IRDY#) signal. A data phase is completed on any clock cycle where both IRDY# and TRDY# are sampled asserted (low) simultaneously.
STOP#	S/T/S	**Stop.** The stop signal is driven by the target to indicate to the initiator that it wishes to stop the current transaction. As a bus slave, STOP# is driven by the 82559 to inform the bus master to stop the current transaction. As a bus master, STOP# is received by the 82559 to stop the current transaction.
IDSEL	IN	**Initialization Device Select.** The initialization device select signal is used by the 82559 as a chip select during PCI configuration read and write transactions. This signal is provided by the host in PCI systems. In a CardBus system, this pin should not be connected.
DEVSEL#	S/T/S	**Device Select.** The device select signal is asserted by the target once it has detected its address. As a bus master, the DEVSEL# is an input signal to the 82559 indicating whether any device on the bus has been selected. As a bus slave, the 82559 asserts DEVSEL# to indicate that it has decoded its address as the target of the current transaction.
REQ#	T/S	**Request.** The request signal indicates to the bus arbiter that the 82559 desires use of the bus. This is a point-to-point signal and every bus master has its own REQ#.
GNT#	IN	**Grant.** The grant signal is asserted by the bus arbiter and indicates to the 82559 that access to the bus has been granted. This is a point-to-point signal and every master has its own GNT#.
INTA#	O/D	**Interrupt A.** The interrupt A signal is used to request an interrupt by the 82559. This is an active low, level triggered interrupt signal.
SERR#	O/D	**System Error.** The system error signal is used to report address parity errors. When an error is detected, SERR# is driven low for a single PCI clock.
PERR#	S/T/S	**Parity Error.** The parity error signal is used to report data parity errors during all PCI transactions except a Special Cycle. The parity error pin is asserted two clock cycles after the error was detected by the device receiving data. The minimum duration of PERR# is one clock for each data phase where an error is detected. A device cannot report a parity error until it has claimed the access by asserting DEVSEL# and completed a data phase.

8.2.3 System and Power Management Signals

Symbol	Type	Name and Function
CLK	IN	**Clock.** The Clock signal provides the timing for all PCI transactions and is an input signal to every PCI device. The 82559 requires a PCI Clock signal (frequency greater than or equal to 16 MHz) for nominal operation. The 82559 supports Clock signal suspension using the Clockrun protocol.
CLKRUN#	IN/OUT O/D	**Clockrun.** The Clockrun signal is used by the system to pause or slow down the PCI Clock signal. It is used by the 82559 to enable or disable suspension of the PCI Clock signal or restart of the PCI clock. When the Clockrun signal is not used, this pin should be connected to an external pull-down resistor.
RST#	IN	**Reset.** The PCI Reset signal is used to place PCI registers, sequencers, and signals into a consistent state. When RST# is asserted, all PCI output signals will be tri-stated.
PME# (PCI)	O/D	**Power Management Event.** The Power Management Event signal indicates that a power management event has occurred in a PCI bus system.
CSTSCHG (CardBus)/ WOL (PCI)	OUT	**Card Status Change/Wake on LAN.** This pin is multiplexed to provide Card Status Change or Wake on LAN signals. In a CardBus system, it is used as the Card Status Change output signal and is an asynchronous signal to the Clock signal. It indicates that a power management event has occurred in a CardBus system. In a PCI system, it is used as the WOL pin and provides a positive pulse of approximately 52 ms upon detection of an incoming Magic Packet*.
ISOLATE#	IN	**Isolate.** The Isolate signal is used to isolate the 82559 from the PCI bus. When Isolate is active (low), the 82559 does not drive its PCI outputs (except PME# and CSTSCHG) or sample its PCI inputs (including CLK and RST#). If the 82559 is not powered by an auxiliary power source, The ISOLATE# pin should not be connected.
ALTRST#	IN	**Alternate Reset.** The Alternate Reset signal is used to reset the 82559 on power-up. In systems that support an auxiliary power supply, ALTRST# should be connected to a power-up detection circuit. Otherwise, ALTRST# should be tied to V_{cc}.
VIO	B IN	**Voltage Input/Output.** The VIO pin is a voltage bias pin and should be 5 V ± 5% in a PCI bus system and V_{CC} in a CardBus system.

8.3 Local Memory Interface Signals

Symbol	Type	Name and Function
FLD[7:0]	T/S	**Flash/Modem Data Input/Output.** These pins are used for Flash/ Modem data interface.
FLA[16]/ CLK25	OUT	**Flash Address[16]/25 MHz Clock.** This multiplexed pin is controlled by the status of the Flash Address[7] (FLA[7]) pin. If FLA[7] is left floating, this pin is used as FLA[16]; otherwise, if FLA[7] is connected to a pull-up resistor, this pin is used as a 25 MHz clock.
FLA[15]/ EESK	OUT	**Flash Address[15]/EEPROM Data Output.** During Flash accesses, this multiplexed pin acts as the Flash Address [15] output signal. During EEPROM accesses, it acts as the serial shift clock output to the EEPROM.

Symbol	Type	Name and Function
FLA[14]/ EEDO	IN/OUT	**Flash Address[14]/EEPROM Data Output.** During Flash accesses, this multiplexed pin acts as the Flash Address [14] output signal. During EEPROM accesses, it acts as serial input data to the EEPROM Data Output signal.
FLA[13]/ EEDI	OUT	**Flash Address[13]/EEPROM Data Input.** During Flash accesses, this multiplexed pin acts as the Flash Address [13] output signal. During EEPROM accesses, it acts as serial output data to the EEPROM Data Input signal.
FLA[12]/ MCNTSM#	OUT O/D	**Flash Address[12]/Modem Central Site Mode.** This multiplexed pin acts as the Flash Address[12] output signal in a non-modem card. If modem is enabled, it is used as an output signal to the modem. It is either floated by default or driven low by the Modem System Control Registers.
FLA[11]/ MINT	IN/OUT	**Flash Address[11]/Modem Interrupt.** This multiplexed pin acts as the Flash Address[11] output signal in a non-modem card. If modem is enabled, it is used as the Modem Interrupt input signal.
FLA[10]/ MRING#	IN/OUT	**Flash Address[10]/Modem Ring.** This multiplexed pin acts as the Flash Address[10] output signal in a non-modem card. If modem is enabled, it is used as the Modem Ring input signal.
FLA[9]/ MRST	OUT	**Flash Address[9]/Modem Reset.** This multiplexed pin acts as the Flash Address[9] output signal in a non-modem card. If modem is enabled, it acts as the Modem Reset signal with an active high output.
FLA[8]/ IOCHRDY	IN/OUT	**Flash Address[8]/ISA Input/Output Channel Ready.** This multiplexed pin acts as the Flash Address[8] output signal in a non-modem card. If modem is enabled, it is used as the ISA IOCHRDY input signal.
FLA[7]/ CLKEN	T/S	**Flash Address[7]/Clock Enable.** This is a multiplexed pin and acts as the Flash Address[7] output signal during nominal operation. When the PCI RST# signal is active, this pin acts as input control over the FLA[16]/CLK25 output signal. If the FLA[7]/CLKEN pin is connected to a pull-up resistor (3.3 KΩ), a 25 MHz clock signal is provided on the FLA[16]/CLK25 output; otherwise, it is used as FLA[16] output.
FLA[6:2]	OUT	**Flash Address[6:2].** These pins are used as Flash/modem address outputs to support 128 Kbyte Flash addressing.
FLA[1]/ AUXPWR	T/S	**Flash Address[1]/Auxiliary Power.** This multiplexed pin acts as the Flash Address[1] output signal during nominal operation. When RST is active (low), it acts as the power supply indicator. If the 82559 is fed PCI power, this pin should be connected to a pull-down resistor; if fed by auxiliary power, a pull-up resistor.
FLA[0]/ PCIMODE#	T/S	**Flash Address [0]/PCI Mode.** This multiplexed pin acts as the Flash Address[0] output signal during nominal operation. When RST# is active (low), it acts as the input system type. If the 82559 is used in a CardBus system, this pin should be connected to a pull-up resistor (3.3 KΩ); otherwise, the 82559 considers the host as a PCI system.
EECS	OUT	**EEPROM Chip Select.** The EEPROM Chip Select signal is used to assert chip select to the serial EEPROM.
FLCS#/AEN	OUT	**Flash Chip Select/Address Enable.** The Flash Chip Select signal is active during Flash. In modem mode, it acts as an ISA-like Address Enable signal (modem chip select).
FLOE#	OUT	**Flash Output Enable.** This pin provides an active low output enable control to the Flash or modem.
FLWE#	OUT	**Flash Write Enable.** This pin provides an active low write enable control to the Flash or modem.

8.4 System Management Bus (SMB) Interface Signals

Symbol	Type	Name and Function
SMBD	IN O/D	**SMB Data.** This signal is stable when the SMB Clock signal is high.
SMBCLK	IN O/D	**SMB Clock.** This pin is used as the SMB Clock signal. One clock pulse is generated for each data bit transferred.
SMBALRT#	O/D	**SMB Alert.** This pin is used as an interrupt signal for a slave device on the SMB.

Note: Do not connect the SMBus signals to the PIIX4, unless the PIIX4's pins are configured for SMBus support. This is especially critical for the SMB ALert signal.

8.5 Testability Port Signals

Symbol	Type	Name and Function
TEST	IN	**Test.** If this input pin is high, the 82559 will enable the test port. During nominal operation this pin should be connected to a pull-down resistor.
TCK	IN	**Testability Port Clock.** This pin is used for the Testability Port Clock signal.
TI	IN	**Testability Port Data Input.** This pin is used for the Testability Port Data Input signal.
TEXEC	IN	**Testability Port Execute Enable.** This pin is used for the Testability Port Execute Enable signal.
TO	OUT	**Testability Port Data Output.** This pin is used for the Testability Port Data Output signal.

8.6 PHY Signals

Symbol	Type	Name and Function
X1	A/I	**Crystal Input One.** X1 and X2 can be driven by an external 3.3 V 25 MHz crystal. Otherwise, X1 may be driven by an external metal-oxide semiconductor (MOS) level 25 MHz oscillator when X2 is left floating.
X2	A/O	**Crystal Input Two.** X1 and X2 can be driven by an external 3.3 V 25 MHz crystal. Otherwise, X1 may be driven by an external MOS level 25 MHz oscillator when X2 is left floating.
TDP TDN	A/O	**Analog Twisted Pair Ethernet Transmit Differential Pair.** These pins transmit the serial bit stream for transmission on the Unshielded Twisted Pair (UTP) cable. The current-driven differential driver can be two-level (10BASE-T) or three-level (100BASE-TX) signals depending on the mode of operation. These signals interface directly with an isolation transformer.

Symbol	Type	Name and Function
RDP RDN	A/I	**Analog Twisted Pair Ethernet Receive Differential Pair.** These pins receive the serial bit stream from the isolation transformer. The bit stream can be two-level (10BASE-T) or three-level (100BASE-TX) signals depending on the mode of operation.
ACTLED#	OUT	**Activity LED.** The Activity LED pin indicates either transmit or receive activity. When activity is present, the activity LED is on; when no activity is present, the activity LED is off. In Wake on LAN mode, the ACTLED# signal is used to indicate that the received frame passed MAC address filtering.
LILED#	OUT	**Link Integrity LED.** The Link Integrity LED pin indicates link integrity. If the link is valid in either 10 or 100 Mbps, the LED is on; if link is invalid, the LED is off.
SPEEDLED#	OUT	**Speed LED.** The Speed LED pin indicates the speed. The speed LED will be on at 100 Mbps and off at 10 Mbps.
RBIAS100	B	**Reference Bias Resistor (100 Mbps).** This pin should be connected to a 619 Ω (1%) pull-down resistor.
RBIAS10	B	**Reference Bias Resistor (10 Mbps).** This pin should be connected to a 549 Ω (1%) pull-down resistor.
VREF	B	**Voltage Reference.** This pin is connected to a 1.25 V ± 1% external voltage reference generator. To use the internal voltage reference source, this pin should be left floating.

NOTE: 619 Ω and 549 Ω for the RBIAS100 and RBIAS10, respectively, are only a recommended values and should be fine tuned for various designs.

9.0 Package and Pinout Information

9.1 Package Information

The 82559 is a 196-pin Ball Grid Array (BGA) package. Package dimensions are shown in Figure 3. More information on Intel device packaging is available in the Intel Packaging Handbook, which is available from the Intel Literature Center or your local Intel sales office.

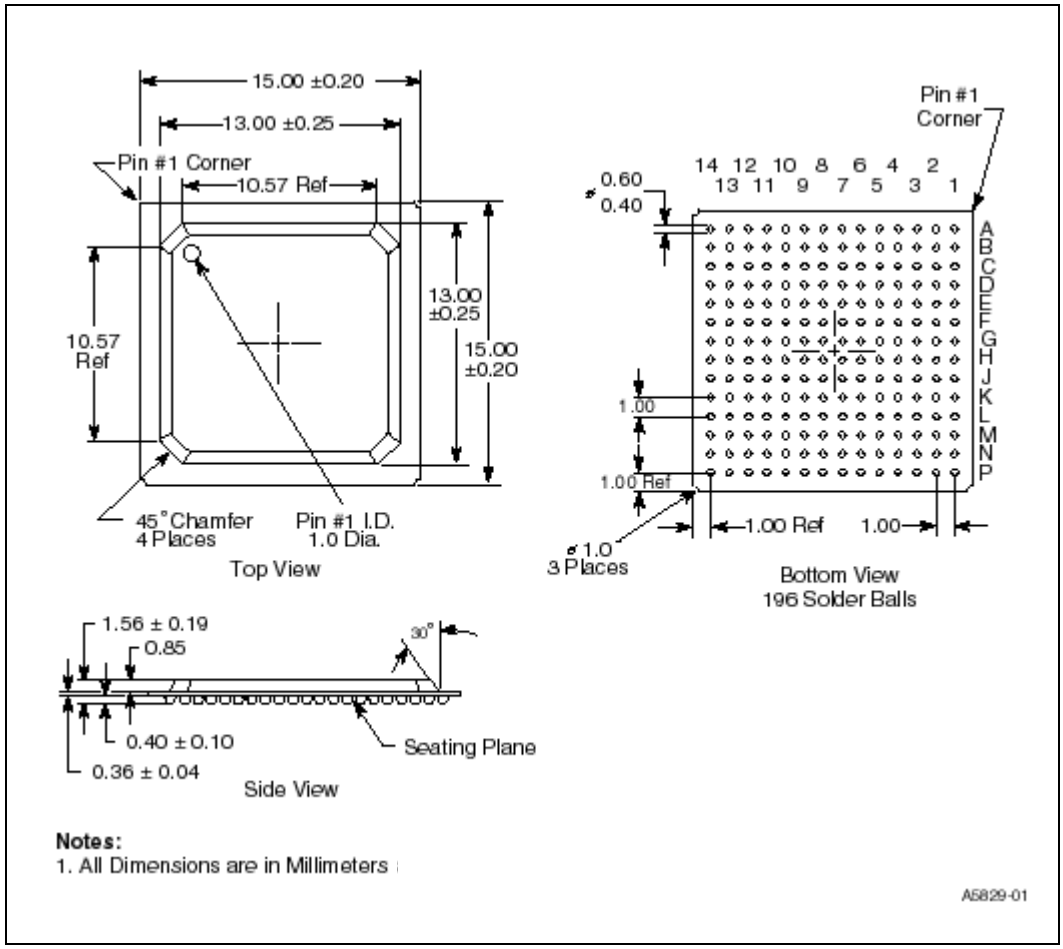

Figure 3. Dimension Diagram for the 82559 196-pin BGA

9.2 Pinout Information

9.2.1 82559 Pin Assignments

Table 1. 82559 Pin Assignments

Pin	Name	Pin	Name	Pin	Name
A1	NC	A2	SERR#	A3	VCCPP
A4	IDSEL	A5	AD25	A6	PME#
A7	VCCPP	A8	AD30	A9	ALTRST#
A10	SMBCLK	A11	VCCPT	A12	LILED
A13	TEST	A14	NC		
B1	AD22	B2	AD23	B3	VSSPP
B4	AD24	B5	AD26	B6	AD27
B7	VSSPP	B8	AD31	B9	ISOLATE#
B10	SMBALRT#	B11	SPEEDLED	B12	TO
B13	RBIAS100	B14	RBIAS10		
C1	AD21	C2	RST#	C3	REQ#
C4	C/BE3#	C5	CSTSCHG	C6	AD28
C7	AD29	C8	CLKRUN#	C9	SMBD
C10	VSSPT	C11	ACTLED	C12	VREF
C13	TDP	C14	TDN		
D1	AD18	D2	AD19	D3	AD20
D4	VSS	D5	VSS	D6	VSS
D7	VSS	D8	VSS	D9	NC
D10	NC	D11	VSS	D12	TI
D13	TEXEC	D14	TCK		
E1	VCCPP	E2	VSSPP	E3	AD17
E4	VSS	E5	VSS	E6	VSS
E7	VSS	E8	VSS	E9	VSS
E10	VSS	E11	VSS	E12	VCC
E13	RDP	E14	RDN		
F1	IRDY#	F2	FRAME#	F3	C/BE2#
F4	VSS	F5	VSS	F6	VSS
F7	VSS	F8	VSS	F9	VSS
F10	VSS	F11	VSS	F12	FLD2
F13	FLD1	F14	FLD0		
G1	CLK	G2	VIO	G3	TRDY#
G4	NC	G5	VCC	G6	VCC
G7	VSS	G8	VSS	G9	VSS
G10	VSS	G11	VSS	G12	FLD3
G13	VCCPL	G14	VSSPL		

Table 1. 82559 Pin Assignments

Pin	Name	Pin	Name	Pin	Name
H1	STOP#	H2	INTA#	H3	DEVSEL#
H4	NC	H5	VCC	H6	VCC
H7	VCC	H8	VCC	H9	VSS
H10	VSS	H11	VSS	H12	FLD6
H13	FLD5	H14	FLD4		
J1	PAR	J2	PERR#	J3	GNT#
J4	NC	J5	VCC	J6	VCC
J7	VCC	J8	VCC	J9	VCC
J10	VCC	J11	VCC	J12	FLA1
J13	FLA0	J14	FLD7		
K1	AD16	K2	VSSPP	K3	VCCPP
K4	VCC	K5	VCC	K6	VCC
K7	VCC	K8	VCC	K9	VCC
K10	VCC	K11	VCC	K12	VSSPL
K13	VCCPL	K14	FLA2		
L1	AD14	L2	AD15	L3	C/BE#1
L4	VCC	L5	VCC	L6	VSS
L7	NC	L8	NC	L9	VCC
L10	VCC	L11	VSS	L12	FLA5
L13	FLA4	L14	FLA3		
M1	AD11	M2	AD12	M3	AD13
M4	C/BE0#	M5	AD5	M6	VSSPP
M7	AD1	M8	FLOE#	M9	FLWE#
M10	FLA15/EESK	M11	FLA12	M12	FLA11
M13	FLA7	M14	FLA6		
N1	VSSPP	N2	AD10	N3	AD9
N4	AD7	N5	AD4	N6	VCCPP
N7	AD0	N8	VCCPL	N9	FLCS#
N10	FLA14/EEDO	N11	X1	N12	VSSPL
N13	FLA10	N14	FLA8/IOCHRDY		
P1	NC	P2	VCCPP	P3	AD8
P4	AD6	P5	AD3	P6	AD2
P7	EECS	P8	VSSPL	P9	FLA16
P10	FLA13/EEDI	P11	X2	P12	VCCPL
P13	FLA9	P14	NC		

9.2.2 82559 Ball Grid Array Diagram

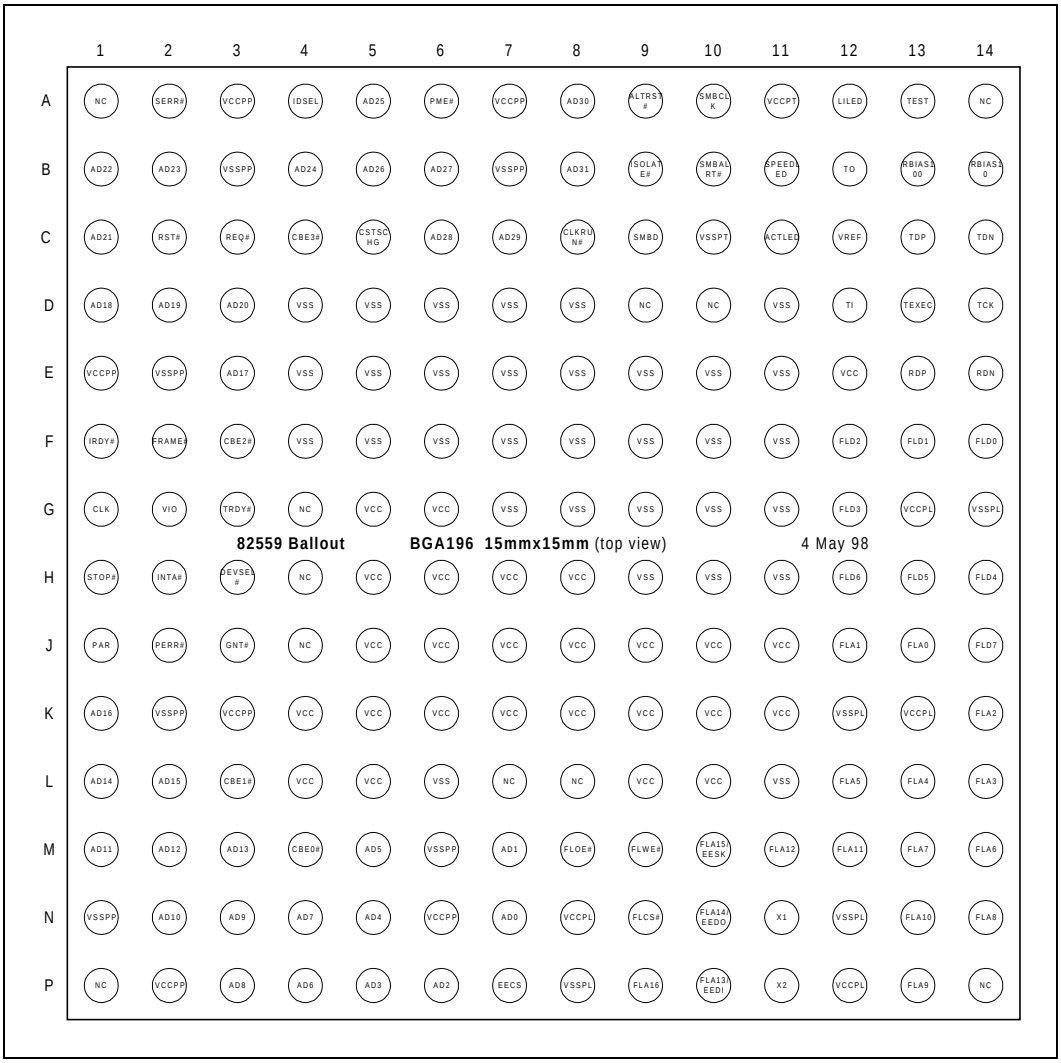

Figure 4. 82559 Ball Grid Array Diagram

10.0 Bill of Materials

Part	Part Number	Quantity	Reference Designator
22 pF Capacitor	C603C220J5GAC-T/R Kemet	2	C1, C2
0.1 uF Capacitor	0603YC104KAT$A AVX	3	C3, C5, C7
8.2 pF Capacitor		1	C4
1500 pF Capacitor		1	C6
LED		2	D1, D2
RJ45 connector	78186-003 Berg	1	J1
62 KΩ Resistor		3	R1, R2, R8
330 Ω Resistor	MCR03EZ$J#331 Rohm	2	R3, R4
549 Ω Resistor	ERJ3EKF5490FT Panasonic	1	R7
619 Ω Resistor	ERJ3EKF6190V Panasonic	1	R8
100 Ω Resistor	ERJ3EKF1000V Panasonic	2	R9, R14
75 Ω Resistor	EXB38V750JV Panasonic	4	R10, R11, R12, R13
1:1 Magnetics	H1012T Pulse Engineering	1	T1
82559	Intel	1	U1
93C46 EEPROM	AT92C46A-10SC2.7 Atmel	1	U2
PLCC Socket	821977-1 AMP	1	U3
25 MHz Crystal	TT-SMDC-25.000-20T Raltron	1	Y1

11.0 Appendix A: 82559/PIIX4 LOM Designs

The Intel 82559 is fully compatible with the Intel PCI to ISA/IDE Xcelerator 4 (PIIX4). The following pages provide a complete reference design for a 82559/PIIX4 solution. Schematic notes are also provided below.

Schematic Notes

- GPI1 of the PIIX4 is used for the PME# input from the 82559. It should also be used for PME# inputs from PCI slots. GPI1 can cause SMI, SCI, and Resume events allowing it to operate in Advanced Configuration and Power Interface (ACPI) and Advanced Power Management (APM) applications.
- The PWR_GOOD signal feeds into the Power Good (PWROK) input pin of the PIIX4 as well as discrete logic for the ISOLATE# signal
- LAN_WAKE is a 50 ms pulse used in APM WOL cases to wake the system. It is connected to the LID input of the PIIX4 which allows for resume events (no SMI and no SCI).

Information on the PIIX4 can be obtained from the Intel 82371AB PCI-to-ISA/IDE Xcelerator (PIIX4) Datasheet.

REVISION 0.5

Revisions		
REV	Description	Date
01	Initial A1 Step Schematic Release	04/29/98
02	Initial B-Step Schematic Release	07/06/98
03	Updated Phy Passive Values and added Connection to pin P2	10/30/98
04	Corrected improper connection on pin P2 and added clarifying notes to VIO pin connections	11/29/98
05	Final B-5 Step Schematic Release	12/18/98

** PLEASE NOTE THESE SCHEMATICS ARE SUBJECT TO CHANGE

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Intel may make changes to specifications and product Descriptions at any time, without notice. The Intel 82559 10/100Mbit LAN may contain design defects or errors known as errata, which may cause the product to deviate from published specifications. Current characterized errata are available on request.

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Hillsboro, OR 97124-5961

Title: 82559 Piix4 LOM Reference Design

Size: B | Document Number: {Doc} | Rev: 05

Date: Tuesday, December 22, 1998 | Sheet 1 of 3

1) The decoupling capacitor should be added to VIO pin.

2) The voltage on VIO determines the slope of the signals on the bus. So although the device will communicate if VIO is connected to 3.3V in 3.3V PCI systems, optimal performance will be acheived if this signal is connected to +5V in PCI bus systems regardless of Bus voltage.

All Vcc Pins are connected together on the board level. The power on the symbol is broken down between Core power (Vcc), Local Bus Power (Vccpl), Transmit Power (Vcct), and PCI power (Vccpp) just for clarity. See enclosed table for Vcc pins.

PCI_5V

R1 62K

C1 0.1uF

VIO

TO PCI BUS

AD[31:0]

AD0 AD1 AD2 AD3 AD4 AD5 AD6 AD7 AD8 AD9 AD10 AD11 AD12 AD13 AD14 AD15 AD16 AD17 AD18 AD19 AD20 AD21 AD22 AD23 AD24 AD25 AD26 AD27 AD28 AD29 AD30 AD31

C/BE[3:0]

C/BE0 C/BE1 C/BE2 C/BE3

FRAME# IRDY# TRDY# DEVSEL# STOP# PAR

INTA PERR# SERR# IDSEL REQ# GNT# RST# CLK ISOLATE# AUX_GOOD PME# CLKRUN#

SMBALRT# SMBCLK SMBD

U1

82559 B-5

196 PIN BGA

The ISOLATE signal should be a signal that is driven LOW just prior to the PCI bus shutting down, and it should be driven HIGH imediately following the PCI reactivating.

R8 62K

The SMBus connection provides access to the TCO features of the 82559. Connect the SMBCLK and SMBD pins to the systems TCO controller, or pull them up to the 3.3 volt rail through 100K resistors if not used. These signals should not be connected in embedded designs.

All Vss Pins are connected together on the board level. The power on the symbol is broken down between Core power (Vss), Local Bus Power (Vsspl), Transmit Power (Vsst), and PCI power (Vsspp) just for clarity. See enclosed table for a listing of Vss pins.

PME# TO PIIX4

LILED ACTLED SPEEDLED

D1 LED R2 330

D2 LED R3 330 3VSB

The 82559 can drive three LEDs with the cathode of each device connected to the 82559 as shown with the SPEEDLED, or a two LED configuration can be employed, as shown. In the two LED configuration the Link and and Activity functions would share a indicator. In this scheme the LINK LED would flash LOW whenever activity was detected.

TDP TDN RDP RDN

FLA16/CLK25 FLA15/EESK FLA14/EEDO FLA13/EEDI FLA12/MCNTSM# FLA11/MINT FLA10/MRING# FLA9/MRST FLA8/IOCHRDY FLA7/CLKEN FLA6 FLA5 FLA4 FLA3 FLA2 FLA1/AUXPWR FLA0/PCIMODE#

FLD7 FLD6 FLD5 FLD4 FLD3 FLD2 FLD1 FLD0

EECS FLCS#/AEN FLOE# FLWE#

TEST TEXEC TCK TI TO VREF RBIAS10 RBIAS100

3VSB R4 3.3K

U2 93C46 EEDI EEDO EESK EECS

VREF: EXTERNAL VREF MAYBE APPLIED HERE IF THE INTERNAL REFERENCE IS NOT USED. THE INTERNAL REFERNCE IS RECOMMENDED, BUT IF AN EXTERNAL REFERENCE IS IMPLEMENTED, THEN THIS WILL CAUSE THE RBIAS VALUES TO CHANGE

R6 549 R7 619

RBIAS10 AND RBIAS100 SHOULD BE "TUNED" FOR YOUR APPLICATION. THE VALUES SHOWN ARE A GOOD STARTING VALUE

X1 X2 Y1 25MHz C2 22pF C3 22pF

R5 62K

Pulldown resistors are utilized on strapped pins to enable the NANDtree test mode to work. The value of 62K was chosen Strictly on the basis of Intel's test fixturing requirements. Other values can be used, but it is recommended that resistors be used other that hard strapping the pins.

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This capicitor is not normally installed, but a placement location can be provided. It may need to be placed based on the results of FCC conformance testing. If it is required, values in the pico farad range would be used. Large capicitance values installed in this location will have a negative effect on long cable performance. so care must be taken in selecting values used.

C4

T1

KEEP TRACE LENGTH FROM MAGNETICS TO RJ-45 CONNECTOR UNDER 1 INCH.

J1
RJ45

TDP

TDN

USE SYMETRICAL 100 OHM DIFFERENTIAL TRACES FOR RDP/RDN AND TDP/TDN

R9
100
1%

14	TDC	TX+	10
16	TD+	TX-	11
15	TD-	RX+	7
1	RD+	CMT	12
2	RD-	RXC	5
3	RDC	RX-	6

1:1 MAGNETICS

C5
0.1uF

R10
75

R11
75

R12
75

R13
75

TERMPLANE

C6
1500pF

C7
0.1uF

CHASSIS GROUND
USE PLANE FOR
THIS SIGNAL

KEEP ALL TERMINATION RESISTORS AS CLOSE TO THE 82559 AS POSSIBLE

R14
120
1%

CREATE TERMINATION PLANE IN PWB. THIS PLANE WILL ACT A PATH FOR LOW-FREQUENCY NOISE THAT MAYBE COUPLED TO UNUSED PINS. THE PLANE SHOULD NOT HAVE ANY DIRECT COMNECTION.

OPTIONAL CAP TO HELP WITH EFT CONFORMANCE

3VSB

C8	4.7uF	C9	4.7uF	C10	0.1uF	C11	0.1uF	C12	0.1uF	C13	0.1uF	C14	0.1uF	C15	0.1uF	C16	0.1uF	C17	0.1uF	C18	0.1uF	C19	0.1uF

Place decoupling capacitiors as close to the 82559 as possible. If component placements are utilized on the bottom side of the board than place decoupling under the 82559.

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Size B	Document Number {Doc}	Rev 05
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