82551QM/82540EM Interchangeable LOM Design Guide

Application Note (AP-432)

December 2003

Revision 1.0

Revision History

Date	Revision	Description
Dec 2003	1.0	Initial public release. (Confidential status was removed.)

Contents

1.0 Introduction

The Intel® 82540EM Gigabit Ethernet Controller and the Intel® 82551QM Fast Ethernet Controller are both manufactured in a footprint compatible 15 mm x 15 mm, 196-Ball Grid Array (BGA) package. Many of the critical signal pin locations on the 82540EM are identical to signals on the 82551QM, allowing designers to create a single design that accommodates both parts. However, the usage of some signals and pins differ between the two devices. Thus, they are not referred to as pin compatible. They are footprint compatible, which means that they share the same package size and the same number and pattern of pins, allowing the signal layout to be flexible and cost effective and to be used as a multipurpose design. This enables a single board design for either device maximizing its value and matching performance needs.

This design is also backwards compatible with the 82559 and 82550 controllers. Engineers with experience implementing these previous generations of Intel Fast Ethernet controllers can easily and confidently update older designs or modify those designs enabling upgrades for the 82540EM Gigabit Ethernet Controller to meet customer requirements while minimizing design variables.

Note: The 82559 and 82550 designs are not forward compatible to this design. Support for features such as IP Security, Alert Standard Format, and Alert on Lan*, is dependant on the feature set of the controller, which is detailed in the device product brief or datasheet. These documents should be referenced to better understand the capabilities of the device selected for a design.

1.1 Document Scope

This application note identifies the design differences between the 82540EM and the 82551QM.

Section 2.0, "Pin Number to Signal Mapping," contains a table summarizing the population options for both devices, and a reference schematic is contained in Section 4.0, "Reference Schematic."

1.2 Reference Documents

It is assumed that the designer is acquainted with high-speed design and board layout techniques. The following documents provide additional information:

- Intel® 82551QM Fast Ethernet Multifunction PCI/CardBus Controller Datasheet, Intel Corporation.
- Intel® 82540EM Gigabit Ethernet Controller Datasheet, Intel Corporation.
- PCI Local Bus Specification, Revision 2.2, PCI Special Interest Group.
- PCI Bus Power Management Interface Specification, Rev. 1.1, PCI Special Interest Group.
- IEEE Standard 802.3, 1996 Edition, Institute of Electrical and Electronics Engineers (IEEE).
- IEEE Standard 802.3u, 1995 Edition, Institute of Electrical and Electronics Engineers (IEEE).
- IEEE Standard 802.3x, 1997 Edition, Institute of Electrical and Electronics Engineers (IEEE).
- IEEE Standard 802.3z, 1998 Edition, Institute of Electrical and Electronics Engineers (IEEE).
- IEEE Standard 802.3ab, 1999 Edition, Institute of Electrical and Electronics Engineers (IEEE).
- Intel® Ethernet Controllers Timing Device Selection Guide, AP-419. Intel Corporation.

1.3 Product Code

The product ordering code for the 82551QM is: GD82551QM.

The product ordering code for the 82540EM is: RC82540EM.

2.0 Pin Number to Signal Mapping

The table below shows the pin names for each controller corresponding to the shared ball reference value.

Note: The 82540EM pin names in this table and reference schematic found at the end of this document may differ slightly from the pin names in the datasheet. The datasheet signal names maintain consistency with the 64-bit gigabit controller naming convention, while the reference schematics follow the convention used by our engineers on their design tools.

Table 1. Pin Number to Signal Mapping with Population Options

82551QM Pin Name	Ball	82540EM Pin Name	Signal Name	Δ	Population Options		Remarks
					8251QM	82540EM	
NC	A1	NO_CONNECT	NC				
PCI_SERR_N	A2	SERR#	PCI_SERR_N				
3.3V	A3	VDDO (3.3V)	3.3V				
PCI_IDSEL	A4	IDSEL	PCI_IDSEL				
PCI_AD[25]	A5	PCI_AD[25]	PCI_AD[25]				
PCI_PME_N	A6	PME#	PCI_PME_N				
3.3V	A7	VDDO (3.3V)	3.3V				
PCI_AD[30]	A8	PCI_AD[30]	PCI_AD[30]				
ALT_RST_N	A9	LAN_PWR_ GOOD	LAN_PWR_ GOOD	X	Pull-up or Master Reset	Master Reset	Master chip reset for both; 82551QM can be pulled up and use an internal reset.
SMB_CLK	A10	SMBCLK	SMB_CLK				
3.3V	A11	VDDO (3.3V)	3.3V				
LINK_LED	A12	LINKA#	LINK_UP_N	X			These are the same. They just use different names.
TEST	A13	TEST	TEST_MAC_DM	X	Pull-down	Pull-down	This is a test enable signal. Both require an external pull-down resistor.
NC	A14	NO_CONNECT	NC				
PCI_AD[22]	B1	PCI_AD[22]	PCI_AD[22]				
PCI_AD[23]	B2	PCI_AD[23]	PCI_AD[23]				
VSS	B3	GND	VSS				
PCI_AD[24]	B4	PCI_AD[24]	PCI_AD[24]				
PCI_AD[26]	B5	PCI_AD[26]	PCI_AD[26]				

Table 1. Pin Number to Signal Mapping with Population Options

82551QM Pin Name	Ball	82540EM Pin Name	Signal Name	Δ	Population Options		Remarks
					8251QM	82540EM	
PCI_AD[27]	B6	PCI_AD[27]	PCI_AD[27]				
VSS	B7	GND	VSS				
PCI_AD[31]	B8	PCI_AD[31]	PCI_AD[31]				
ISOLATE_N	B9	RST#	PCI_RST_N	X			These are the same. ISOLATE_N is used as PCI_RST_N.
SMB_ALERT_N	B10	SMBALRT#	SMB_ALERT_N				
SPEED_LED	B11	LINKA100#	LINK100_N	X			These signals have the exact same functionality but use different names.
TO	B12	LINKA1000#	LINK1000_N	X	NC	LED	LINK1000 LED does not exist in the 82551QM.
RBIAS100	B13	CTRL_25	CTRL_25	X	619 Ω pull-down resistor	Power Regulator	Populate the 82551QM design with a pull-down and the 82540EM with a transistor.
RBIAS10	B14	PHY REF	PHY REF	X	549 Ω pull-down	2.49 KΩ pull-down	Change the value of the pull-down resistor for each option.
PCI_AD[21]	C1	PCI_AD[21]	PCI_AD[21]				
PCI_RST_N	C2	M66EN	M66EN	X	Pull-up	PCI M66EN	This may require zero ohm resistors to a M66EN signal.
PCI_REQ_N	C3	REQ#	PCI_REQ_N				
PCI_CBE_N[3]	C4	CBE3#	PCI_CBE_N[3]				
CSTCHG	C5	APM_WAKEUP	APM_WAKEUP	X			These signals are the same but have different names.
PCI_AD[28]	C6	PCI_AD[28]	PCI_AD[28]				
PCI_AD[29]	C7	PCI_AD[29]	PCI_AD[29]				
CLK_RUN_N	C8	NO_CONNECT	NC	X	Pull-down	Don't care	The pull-down resistor for the 82551QM can be left alone or depopulated for the 82540EM.
SMB_DAT	C9	SMBDAT	SMB_DAT				
VSS	C10	GND	VSS				
ACT_LED	C11	ACT_A#	ACTIVITY_N	X			These signals are the same but have different names.
VREF	C12	GND	VSS	X	VSS	VSS	The 82551QM connection is usually NC (it has an internal pull-down), but VSS is okay.
TX_PLUS	C13	MDIA[2]-	MDI_PLUS[0]	X			These signals are the same but have different names.
TX_MINUS	C14	MDIA[0]-	MDI_MINUS[0]	X			

Table 1. Pin Number to Signal Mapping with Population Options

82551QM Pin Name	Ball	82540EM Pin Name	Signal Name	Δ	Population Options		Remarks
					8251QM	82540EM	
PCI_AD[18]	D1	PCI_AD[18]	PCI_AD[18]				
PCI_AD[19]	D2	PCI_AD[19]	PCI_AD[19]				
PCI_AD[20]	D3	PCI_AD[20]	PCI_AD[20]				
VSS	D4	GND	ALT_CLK125	X	VSS	VSS	ALT_CLK125 needs to be grounded in production mode.
VSS	D5	GND	VSS				
VSS	D6	GND	VSS				
VSS	D7	GND	VSS				
VSS	D8	GND	VSS				
NC	D9	AVDDL (2.5V)	2.5V	X	Don't care	2.5V	This is used for the 2.5V power source of 82540EM. It is not populated for the 82551QM.
NC	D10	NO_CONNECT	NC				
NC	D11	AVDDL (2.5V)	2.5V	X	Don't care	2.5V	This is used for the 2.5V power source of 82540EM. It is not populated for the 82551QM.
TI	D12	NO_CONNECT	NC	X	NC	NC	This is a no connect signal for both devices.
TEXEC	D13	GND	VSS	X	VSS	VSS	82551QM connection is usually NC, but VSS is okay and works for tests.
TCK	D14	NO_CONNECT	NC	X	NC	NC	This is a no connect signal for both devices. The 82551QM uses this as a test point for testability.
3.3V	E1	VDDO (3.3V)	3.3V				
VSS	E2	GND	VSS				
PCI_AD[17]	E3	PCI_AD[17]	PCI_AD[17]				
VSS	E4	GND	VSS				
VSS	E5	GND	VSS				
VSS	E6	GND	VSS				
VSS	E7	GND	VSS				
VSS	E8	GND	VSS				
VSS	E9	GND	VSS				
VSS	E10	GND	VSS				
NC	E11	DVDD (1.5V)	1.5V	X	Don't care	1.5V	The 82540EM connects to a 1.5V rail, and the 82551QM, to a 3.3V rail.
3.3V	E12	DVDD (1.5V)	1.5V	X	3.3V	1.5V	This is 1.5V power signal or zero ohm connected 3.3V power signal.

Table 1. Pin Number to Signal Mapping with Population Options

82551QM Pin Name	Ball	82540EM Pin Name	Signal Name	Δ	Population Options		Remarks
					8251QM	82540EM	
RX_PLUS	E13	MDIA[2]+	MDI_PLUS[1]	X			These are the same signals with different names.
RX_MINUS	E14	MDIA[0]+	MDI_MINUS[1]	X			
PCI_IRDY_N	F1	IRDY#	PCI_IRDY_N				
PCI_FRAME_N	F2	FRAME#	PCI_FRAME_N				
PCI_CBE_N[2]	F3	CBE2#	PCI_CBE_N[2]				
VSS	F4	GND	VSS				
VSS	F5	GND	VSS				
VSS	F6	GND	VSS				
VSS	F7	GND	VSS				
VSS	F8	GND	VSS				
VSS	F9	GND	VSS				
VSS	F10	GND	VSS				
VSS	F11	GND	VSS				
FLSH_DATA[2]	F12	NO_CONNECT	PHY_TSTPT	X	NC	NC	This is a no connect signal for both devices.
FLSH_DATA[1]	F13	MDIA[3]-	MDI_PLUS[2]	X	NC	Magnetics	De-populate the magnetics for the 82551QM.
FLSH_DATA[0]	F14	MDIA[1]-	MDI_MINUS[2]	X	NC	Magnetics	
PCI_CLK	G1	CLK	PCI_CLK				
VIO	G2	VIO	VIO				
PCI_TRDY_N	G3	TRDY	PCI_TRDY_N				
NC	G4	ZP_COMP	PCI_ZP	X	Don't care	Pull-up	Populate the pull-up resistor for the 82540EM.
3.3V	G5	DVDD (1.5V)	1.5V	X	3.3V	1.5V	This is 1.5V power signal or zero ohm connected 3.3V power signal.
3.3V	G6	DVDD (1.5V)	1.5V	X	3.3V	1.5V	
VSS	G7	GND	VSS				
VSS	G8	GND	VSS				
VSS	G9	GND	VSS				
VSS	G10	GND	VSS				
VSS	G11	GND	VSS				
FLSH_DATA[3]	G12	AVDDL (2.5V)	2.5V	X	NC	2.5V	This needs a zero ohm population option.
3.3V	G13	DVDD (1.5V)	1.5V	X	3.3V	1.5V	This is 1.5V power signal or zero ohm connected 3.3V power signal.
VSS	G14	GND	VSS				
PCI_STOP_N	H1	STOP#	PCI_STOP_N				
PCI_INTA_N	H2	INTA#	PCI_INTA_N				
PCI_DEVSEL_N	H3	DEVSEL#	PCI_DEVSEL_N				

Table 1. Pin Number to Signal Mapping with Population Options

82551QM Pin Name	Ball	82540EM Pin Name	Signal Name	Δ	Population Options		Remarks
					8251QM	82540EM	
NC	H4	ZN_COMP	PCI_ZN	X	Don't care	Pull-down	Populate the pull-down resistor for the 82540EM.
3.3V	H5	DVDD (1.5V)	1.5V	X	3.3V	1.5V	This is 1.5V power signal or zero ohm connected 3.3V power signal.
3.3V	H6	DVDD (1.5V)	1.5V	X	3.3V	1.5V	
3.3V	H7	DVDD (1.5V)	1.5V	X	3.3V	1.5V	
3.3V	H8	DVDD (1.5V)	1.5V	X	3.3V	1.5V	
VSS	H9	GND	VSS				
VSS	H10	GND	VSS				
NC	H11	DVDD (1.5V)	1.5V	X	Don't care	1.5V	The 82540EM connects to a 1.5V rail, and the 82551QM, to a 3.3V rail.
FLSH_DATA[6]	H12	NO_CONNECT	HSDACN	X	NC	NC	This is a no connect signal for both devices.
FLSH_DATA[5]	H13	MDIA[3]+	MDI_PLUS[3]	X	NC	Magnetics	De-populate the magnetics for the 82551QM.
FLSH_DATA[4]	H14	MDIA[1]+	MDI_MINUS[3]	X	NC	Magnetics	
PCI_PAR	J1	PAR	PCI_PAR				
PCI_PERR_N	J2	PERR#	PCI_PERR_N				
PCI_GNT_N	J3	GNT#	PCI_GNT_N				
NC	J4	NO_CONNECT	NC				
3.3V	J5	DVDD (1.5V)	1.5V	X	3.3V	1.5V	This is 1.5V power signal or zero ohm connected 3.3V power signal.
3.3V	J6	DVDD (1.5V)	1.5V	X	3.3V	1.5V	
3.3V	J7	DVDD (1.5V)	1.5V	X	3.3V	1.5V	
3.3V	J8	DVDD (1.5V)	1.5V	X	3.3V	1.5V	
3.3V	J9	DVDD (1.5V)	1.5V	X	3.3V	1.5V	
3.3V	J10	DVDD (1.5V)	1.5V	X	3.3V	1.5V	
3.3V	J11	DVDD (1.5V)	1.5V	X	3.3V	1.5V	
FLSH_ADDR[1]	J12	AUX_PWR	AUX_PWR	X			These are the same. 82551QM FLA[1] signal samples auxiliary power at reset. 82540EM always samples auxiliary power.
FLSH_ADDR[0]	J13	NO_CONNECT	HSDACP	X	NC	NC	This can be no connect for both devices.
FLSH_DATA[7]	J14	XTAL2	XTAL2	X	NC	XTAL2	These signals need a zero ohm population option.
PCI_AD[16]	K1	PCI_AD[16]	PCI_AD[16]				
VSS	K2	GND	VSS				
3.3V	K3	VDDO (3.3V)	3.3V				
3.3V	K4	VDDO (3.3V)	3.3V				

Table 1. Pin Number to Signal Mapping with Population Options

82551QM Pin Name	Ball	82540EM Pin Name	Signal Name	Δ	Population Options		Remarks
					8251QM	82540EM	
3.3V	K5	DVDD (1.5V)	1.5V	X	3.3V	1.5V	This is 1.5V power signal or zero ohm connected 3.3V power signal.
3.3V	K6	DVDD (1.5V)	1.5V	X	3.3V	1.5V	
3.3V	K7	DVDD (1.5V)	1.5V	X	3.3V	1.5V	
3.3V	K8	DVDD (1.5V)	1.5V	X	3.3V	1.5V	
3.3V	K9	DVDD (1.5V)	1.5V	X	3.3V	1.5V	
3.3V	K10	DVDD (1.5V)	1.5V	X	3.3V	1.5V	
3.3V	K11	DVDD (1.5V)	1.5V	X	3.3V	1.5V	
VSS	K12	GND	VSS				
3.3V	K13	VDDO (3.3V)	3.3V				
FLSH_ADDR[2]	K14	XTAL1	XTAL1	X	NC	XTAL1	These pins require a zero ohm population option.
PCI_AD[14]	L1	PCI_AD[14]	PCI_AD[14]				
PCI_AD[15]	L2	PCI_AD[15]	PCI_AD[15]				
PCI_CBE_N[1]	L3	CBE1#	PCI_CBE_N[1]				
3.3V	L4	DVDD (1.5V)	1.5V	X	3.3V	1.5V	This is 1.5V power signal or zero ohm connected 3.3V power signal.
3.3V	L5	DVDD (1.5V)	1.5V	X	3.3V	1.5V	
VSS	L6	GND	VSS				
MODEM_CS_N	L7	NO_CONNECT	CLK_BYP_N	X	NC	NC	No connect.
NC	L8	AVDDL (2.5V)	2.5V	X	Don't care	2.5V	This is the 2.5V power source for the 82540EM. It is not populated for the 82551QM.
3.3V	L9	DVDD (1.5V)	1.5V	X	3.3V	1.5V	This is 1.5V power signal or zero ohm connected 3.3V power signal.
3.3V	L10	DVDD (1.5V)	1.5V	X	3.3V	1.5V	
VSS	L11	GND	VSS				
FLSH_ADDR[5]	L12	JTAG_TMS	JTAG_TMS	X	NC	JTAG	De-populate any JTAG passive or active logic in the 82551QM.
FLSH_ADDR[4]	L13	JTAG_TRST#	JTAG_TRST_N	X	NC	JTAG	
FLSH_ADDR[3]	L14	JTAG_TCK	JTAG_TCK	X	NC	JTAG	
PCI_AD[11]	M1	PCI_AD[11]	PCI_AD[11]				
PCI_AD[12]	M2	PCI_AD[12]	PCI_AD[12]				
PCI_AD[13]	M3	PCI_AD[13]	PCI_AD[13]				
PCI_CBE_N[0]	M4	CBE0#	PCI_CBE_N[0]				
PCI_AD[5]	M5	PCI_AD[5]	PCI_AD[5]				
VSS	M6	GND	VSS				
PCI_AD[1]	M7	PCI_AD[1]	PCI_AD[1]				
FLSH_OE_N	M8	CLK_VIEW	CLK_VIEW	X	NC	NC	No connect.
FLSH_WE_N	M9	NO_CONNECT	FLSH_CE_N	X	NC	NC	No connect.

Table 1. Pin Number to Signal Mapping with Population Options

82551QM Pin Name	Ball	82540EM Pin Name	Signal Name	Δ	Population Options		Remarks
					8251QM	82540EM	
FLSH_ADDR[15] /EESK	M10	EE_SK	EESK	X			These are the same signals but have different names.
FLSH_ADDR[12]	M11	NO_CONNECT	FLSH_SI	X	NC	NC	No connect.
FLSH_ADDR[11]	M12	SDP[7]	SDP[7]	X	NC	SDP	De-populate any SDP logic with the 82551QM.
FLSH_ADDR[7]	M13	JTAG_TDI	JTAG_TDI	X	NC	JTAG	De-populate any JTAG passive or active logic in the 82551QM.
FLSH_ADDR[6]	M14	JTAG_TDO	JTAG_TDO	X	NC	JTAG	
VSS	N1	GND	VSS				
PCI_AD[10]	N2	PCI_AD[10]	PCI_AD[10]				
PCI_AD[9]	N3	PCI_AD[9]	PCI_AD[9]				
PCI_AD[7]	N4	PCI_AD[7]	PCI_AD[7]				
PCI_AD[4]	N5	PCI_AD[4]	PCI_AD[4]				
3.3V	N6	VDDO (3.3V)	3.3V				
PCI_AD[0]	N7	PCI_AD[0]	PCI_AD[0]				
3.3V	N8	VDDO (3.3V)	3.3V				
FLSH_CE_N	N9	NO_CONNECT	FLSH_SCK	X	NC	NC	No connect.
FLSH_ADDR[14] /EEDO	N10	EE_DO	EE_DO	X			These are the same signals but have different names.
XTAL1	N11	NO_CONNECT	NC	X	XTAL	Don't care	These require a zero ohm population option.
VSS	N12	GND	VSS				
FLSH_ADDR[10]	N13	SDP[6]	SDP[6]	X	NC	SDP	De-populate any SDP logic with the 82551QM.
FLSH_ADDR[8] /IOCHRDY	N14	SDP[0]	SDP[0]	X	NC	SDP	
NC	P1	NO_CONNECT	NC				
3.3V	P2	VDDO (3.3V)	3.3V				
PCI_AD[8]	P3	PCI_AD[8]	PCI_AD[8]				
PCI_AD[6]	P4	PCI_AD[6]	PCI_AD[6]				
PCI_AD[3]	P5	PCI_AD[3]	PCI_AD[3]				
PCI_AD[2]	P6	PCI_AD[2]	PCI_AD[2]				
EE_CS	P7	EE_CS	EE_CS				
VSS	P8	GND	VSS				
FLSH_ADDR[16]	P9	NO_CONNECT	FLSH_SO	X	NC	NC	No connect.
FLSH_ADDR[13] /EEDI	P10	EE_DI	EE_DI	X			These are the same signals but have different names.
XTAL2	P11	CTRL_15	CTRL_15	X	XTAL	Power Regulator	These require a zero ohm population option.

Table 1. Pin Number to Signal Mapping with Population Options

82551QM Pin Name	Ball	82540EM Pin Name	Signal Name	Δ	Population Options		Remarks
					8251QM	82540EM	
3.3V	P12	VDDO (3.3V)	3.3V				
FLSH_ADDR[9]	P13	SDP[1]	SDP[1]	X	NC	NC	De-populate any SDP logic with 82551QM.
NC	P14	NO_CONNECT	NC				

3.0 Gigabit Ethernet Design

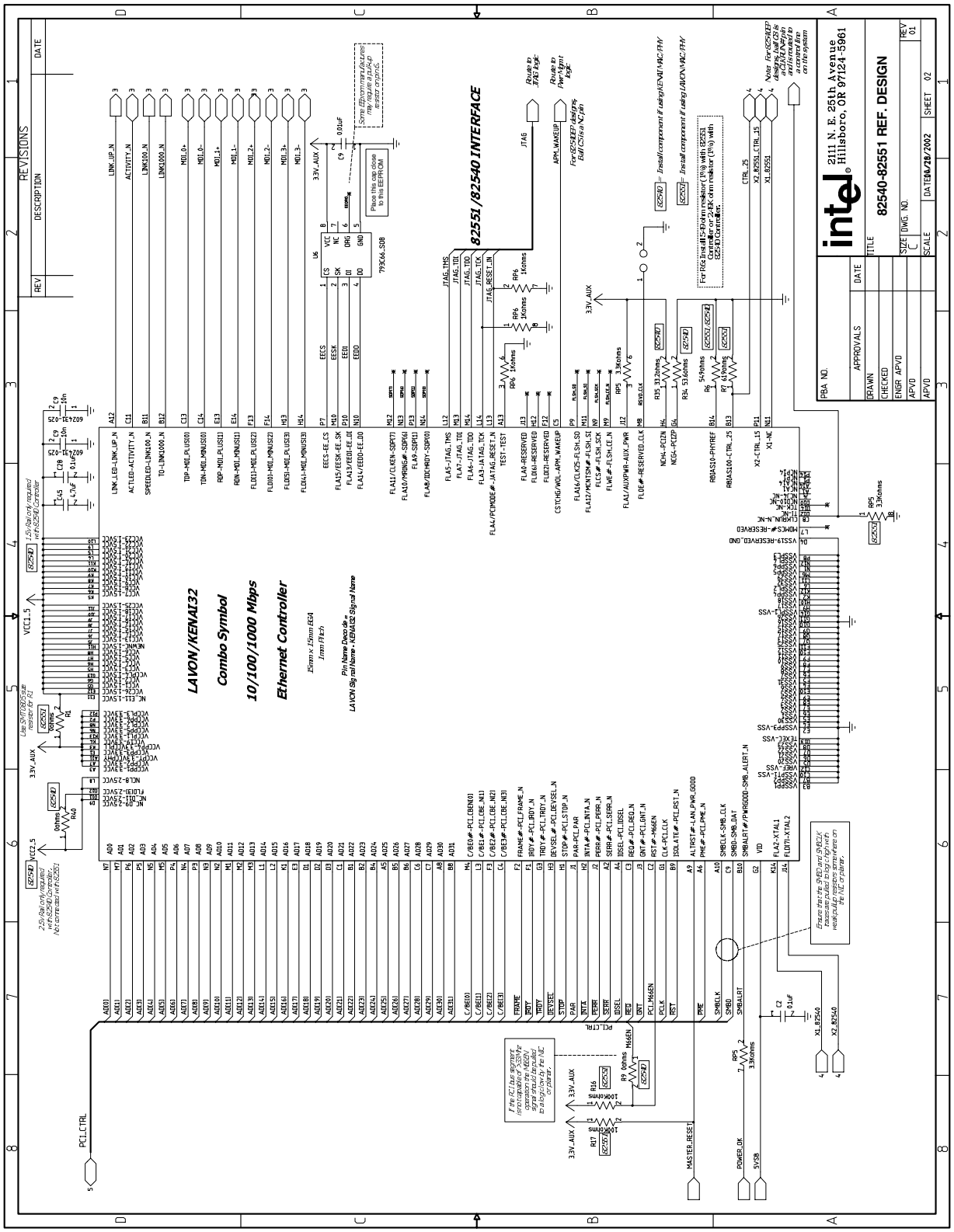
The 82540EM Gigabit Ethernet Controller Datasheet provides information relating to design considerations specific to Gigabit Ethernet. Fast Ethernet and Gigabit Ethernet designs share many of the same requirements. The primary differences between Fast Ethernet and Gigabit Ethernet designs are:

- The increased number of traces from the device PHY unit. Gigabit Ethernet requires 8 traces, and Fast Ethernet, 4 traces.
- Tighter signaling characteristics for Gigabit Ethernet.

4.0 Reference Schematic

The following pages illustrate a dual purpose Fast Ethernet and Gigabit Ethernet design using the 82551QM and 82540EM controllers.

Note: The 82540EM pin names in the reference schematic found at the end of this document may differ slightly from the pin names in the datasheet. The datasheet signal names maintain consistency with the 64-bit gigabit controller naming convention, while the reference schematics follow the convention used by our engineers on their design tools.


LAVON/KENAI32
Combo Symbol
10/100/1000 Mbps
Ethernet Controller
8255L/82540 INTERFACE
REVISIONS
REV
DESCRIPTION
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intel
2111 N. E. 25th Avenue
Hillsboro, OR 97124-5961
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POWER_OK
5VSB
LINK_UP_N
ACTIVITY_N
LINK100_N
LINK1000_N
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MDI_0-
MDI_1+
MDI_1-
MDI_2+
MDI_2-
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APM_WAKEUP
CTRL_25
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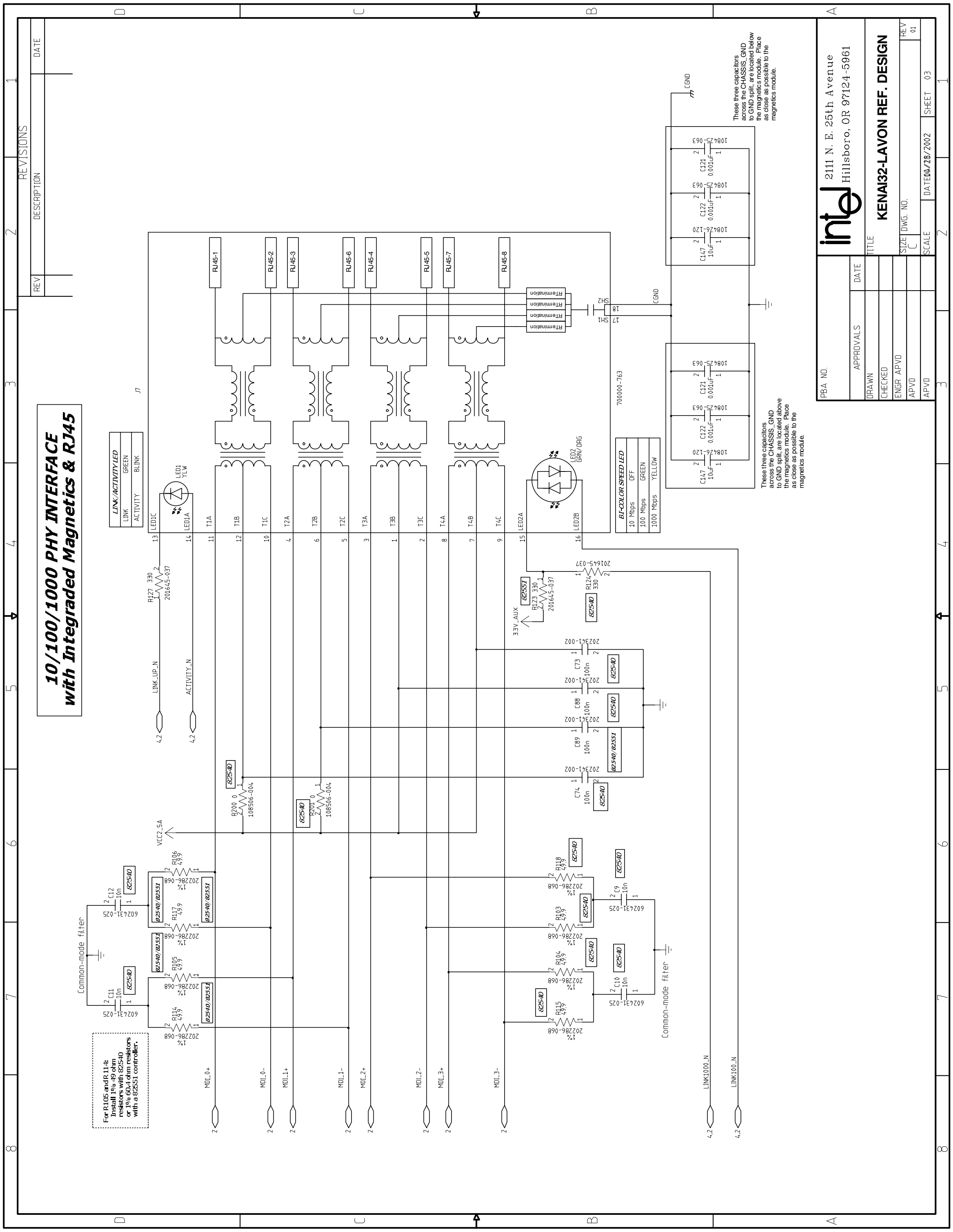
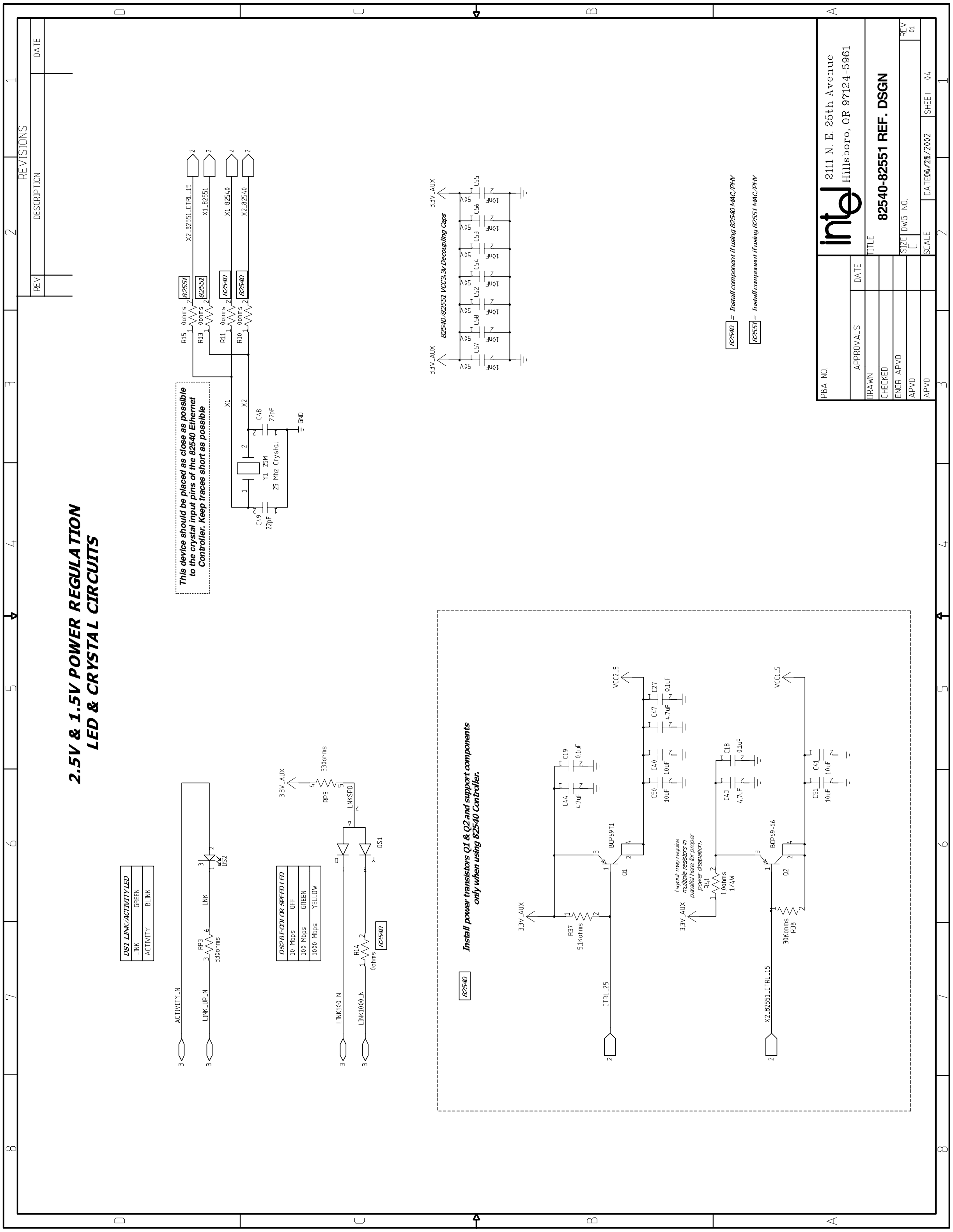
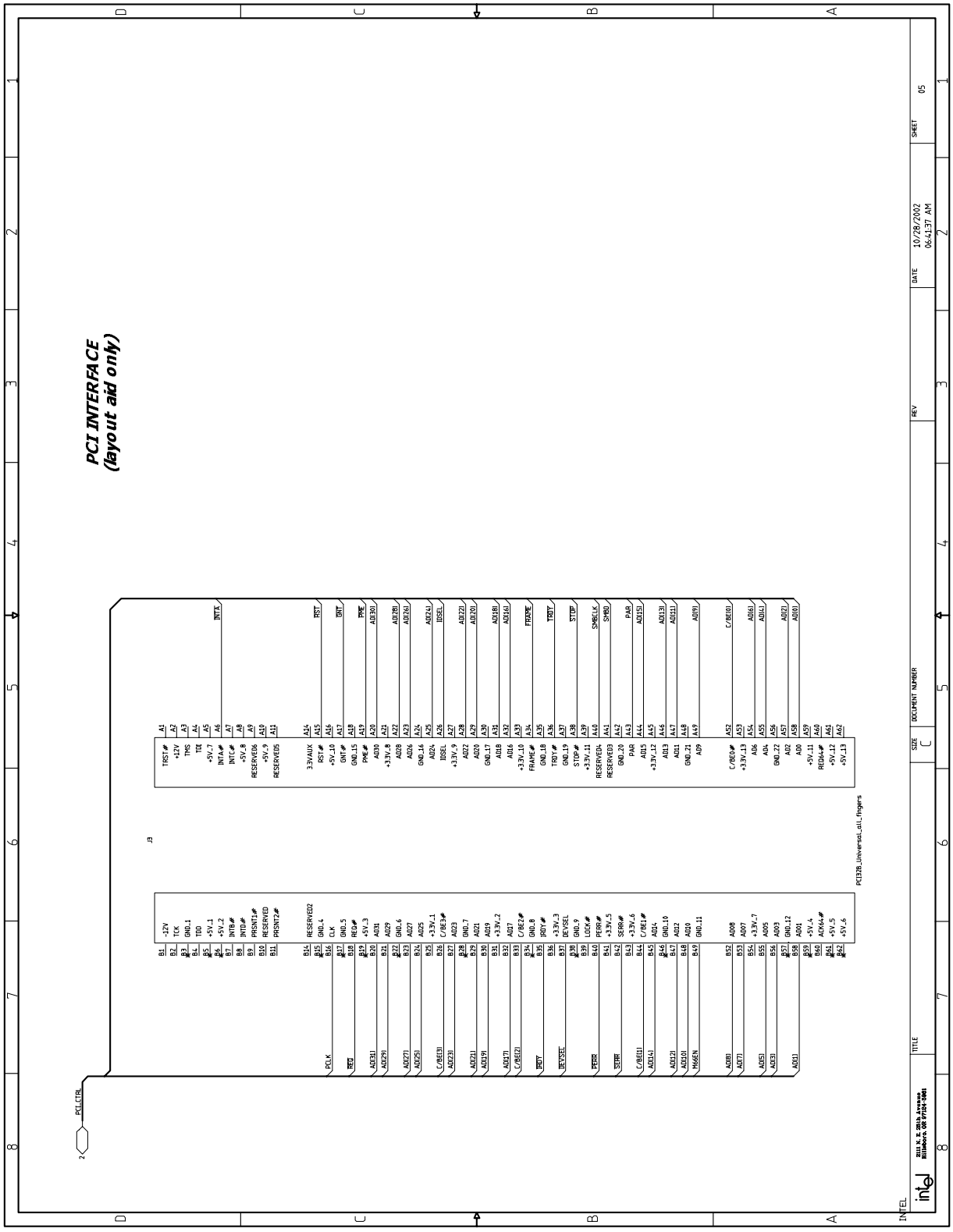
X2_82551_CTRL_25
X1_82540
X2_82540


10/100/1000 PHY INTERFACE
with Integrated Magnetics & RJ45
KENAI32-LAVON REF. DESIGN
2111 N. E. 25th Avenue
Hillsboro, OR 97124-5961
REVISIONS
LINK/ACTIVITY LED
BI-COLOR SPEED LED
Common-mode filter
For R105 and R114: Install 1% 49.9 ohm resistors with 82540 or 1% 60.4 ohm resistors with a 82551 controller.
These three capacitors across the CHASSIS_GND to GND split, are located below the magnetics module. Place as close as possible to the magnetics module.
These three capacitors across the CHASSIS_GND to GND split, are located above the magnetics module. Place as close as possible to the magnetics module.


2.5V & 1.5V POWER REGULATION
LED & CRYSTAL CIRCUITS
This device should be placed as close as possible to the crystal input pins of the 82540 Ethernet Controller. Keep traces short as possible
82540/82551 VCC3.3v Decoupling Caps
82540 = Install component if using 82540 MAC/PHY
82551 = Install component if using 82551 MAC/PHY
Install power transistors Q1 & Q2 and support components only when using 82540 Controller.
Layout may require multiple resistors in parallel here for proper power dissipation.
DS1 LINK/ACTIVITY LED
DS2 BI-COLOR SPEED LED
2111 N. E. 25th Avenue
Hillsboro, OR 97124-5961
82540-82551 REF. DSGN


PCI INTERFACE
(layout aid only)
PCI_CTRL
PCI32B_Universal_all_fingers
INTEL
DOCUMENT NUMBER
SIZE
C
DATE
10/28/2002
06:41:37 AM
SHEET
05
REV