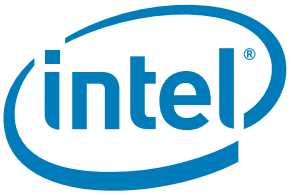

Intel® 82545/82546 Dynamically Changing Link Modes

Application Note

February 2007

316413-001
Revision 1.1

Contents

Figure

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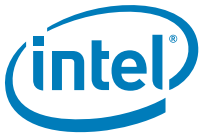
Revision History

Date	Revision	Description
Feb 2007	1.1	Updated the Reset PHY blocks of Figure 1 “Sample Transition Diagram”.
Feb 2004	1.0	Initial release



1.0 Introduction

The 82545EM/82545GM and 82546EB/82546GB Gigabit Ethernet Controllers contain three link modes of operation. The first incorporates the use of an internal fully IEEE-compliant Gigabit Media Independent Interface (GMII) connecting the MAC and internal PHY units. The second mode of operation incorporates the use of an internal Ten-Bit Interface (TBI), which connects the MAC to an internal Serial/De-serializing device (SerDes). In standard applications, the 82545EM/GM and 82546EB/GB are designed in one of the two modes of operation. The third mode of operation exposes the internal TBI interface on external pins, bypassing the internal SerDes.

It might be desirable to create a design application such that the controller can dynamically switch, via software, between internal PHY mode and internal SerDes mode. After research and testing, Intel has identified a mechanism that appears to support such an application. It is important to note that though Intel believes to have identified a mechanism, as this is not a pre-production design-target or feature of the products, all responsibility for validating and supporting any implementation of such an application is considered to be customer responsibility. Additionally, for the purpose of this document, discussions surrounding the internal SerDes mode of operation also applies to external TBI mode of operation. The exception is the Link_Mode indication bits and the pin descriptions discussed later in this application note.

It is the intention of this document to be used as a guide, in conjunction with current 82545EM/GM and 82546EB/GB design documentation, describing how to develop a design capable of switching from internal PHY mode to internal SerDes mode without requiring a system level reset or power cycle. This document refers to signal definitions and circuit connections described in the following documents:

- *Intel 82546EB Dual Port Gigabit Ethernet Controller Networking Silicon Datasheet*
- *Intel 82546GB Dual Port Gigabit Ethernet Controller Networking Silicon Datasheet*
- *AP-439 – 82545EM, 82545GM, 82546EB, and 82546GB Gigabit Ethernet Controllers Design Guide Application Note*
- *Intel 82545EM Dual Port Gigabit Ethernet Controller Networking Silicon Datasheet*
- *Intel 82545GM Dual Port Gigabit Ethernet Controller Networking Silicon Datasheet*
- *Intel PCI/PCI-X Family of Gigabit Ethernet Controllers Software Developer's Manual*

It is intended that future revisions of the design guides and software developer's manuals incorporate changes described within this document.

2.0 Circuit Connections for Dynamic Mode Switching

The following tables list the operation of pins affected in designs using dynamic mode switching. For information on all pins, pin-outs, and design implementations on either internal PHY or internal SerDes based designs, please see the appropriate design guide.

The external interface signals are electrically defined in one of the following fashions:

- **I** - A standard input-only signal
- **O** - A standard output-only signal
- **A** - Analog signal
- **P** - Power signal

3.0 Internal SerDes Pin Descriptions

The internal SerDes interface using the internal TBI bus to connect the Media Access Controller (MAC) function of the device to the internal SerDes device. When the device is not in internal SerDes mode, the device holds the interface in a high impedance state.

Note that SIG_DETECT B, TXB+/-, and RXB+/- signals are applicable only for the 82546EB/GB controllers.

Table 1. Internal SerDes Pin Descriptions

Signal Name	Type	Name & Function
TXA+/- TXB+/-	O	SerDes Transmit Pairs A and B These signals make the differential transmit pair for 1.25 GHz serial interface. If the SerDes interface is not used, these pins should not be connected.
RXA+/- RXB+/-	I	SerDes Receive Pairs A and B These signals make the differential receive pair for the 1.25 GHz serial interface. If the SerDes interface is not used, these pins should not be connected.
SIG_DETECT (A and B)	I	Signal Detects A and B These pins indicate whether the SerDes signals (connected to the 1.25 GHs serial interface) have been detected by the optical transceivers. If the SerDes interface is not used, the SIG_DETECT inputs should be connected to ground using pull-down resistors.

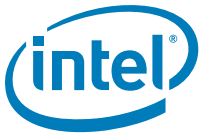
4.0 Internal PHY Interface Signals

When the GMII interface is being used, the internal PHY is powered. The PHY signals used are listed here. When the device is not in GMII mode, it powers down the internal PHY to save on power consumption and heat dissipation.

Note that the Reference B and MDIB[0:4]+/- signals are only applicable for the 82546EB/GB devices.

Table 2. Internal PHY Pin Description

Signal Name	Type	Name & Function
REF_A	P	Reference A This reference signal should be connected to Vss through an external 2.49 K ohm resistor.
MDIA[0]+/-	A	Media Dependent Interface A [0]. 1000BASE-T: In MDI configuration, MDIA[0]+/- corresponds to BI_DA+/- and in MDIX configuration MDIA[0]+/- corresponds to BI_DB+/-. 100BASE-TX: In MDI configuration, MDIA[0]+/- is used for the transmit pair and in MDIX configuration MDIA[0]+/- is used for the receive pair. 10BASE-T: In MDI configuration, MDIA[0]+/- is used for the transmit pair and in MDIX configuration MDIA[0]+/- is used for the receive pair.



Signal Name	Type	Name & Function
MDIA[1]+/-	A	Media Dependent Interface A [1]. 1000BASE-T: In MDI configuration, MDIA[1]+/- corresponds to BI_DB+/- and in MDIX configuration MDIA[1]+/- corresponds to BI_DA+/-. 100BASE-TX: In MDI configuration, MDIA[1]+/- is used for the receive pair and in MDIX configuration MDIA[1]+/- is used for the transmit pair. 10BASE-T: In MDI configuration, MDIA[1]+/- is used for the receive pair and in MDIX configuration MDIA[1]+/- is used for the transmit pair.
MDIA[2]+/-	A	Media Dependent Interface A [2]. 1000BASE-T: In MDI configuration, MDIA[2]+/- corresponds to BI_DC+/- and in MDIX configuration MDIA[2]+/- corresponds to BI_DD+/-. 100BASE-TX: Unused. 10BASE-T: Unused.
MDIA[3]+/-	A	Media Dependent Interface A [3]. 1000BASE-T: In MDI configuration, MDIA[3]+/- corresponds to BI_DD+/- and in MDIX configuration MDIA[3]+/- corresponds to BI_DC+/-. 100BASE-TX: Unused. 10BASE-T: Unused.
REF_B	P	Reference B This reference signal should be connected to Vss through an external 2.49 K ohm resistor.
MDIB[0]+/-	A	Media Dependent Interface B [0]. 1000BASE-T: In MDI configuration, MDIB[0]+/- corresponds to BI_DA+/- and in MDIX configuration MDIB[0]+/- corresponds to BI_DB+/-. 100BASE-TX: In MDI configuration, MDIB[0]+/- is used for the transmit pair and in MDIX configuration MDIB[0]+/- is used for the receive pair. 10BASE-T: In MDI configuration, MDIB[0]+/- is used for the transmit pair and in MDIX configuration MDIB[0]+/- is used for the receive pair.
MDIB[1]+/-	A	Media Dependent Interface B [1]. 1000BASE-T: In MDI configuration, MDIB[1]+/- corresponds to BI_DB+/- and in MDIX configuration MDIB[1]+/- corresponds to BI_DA+/-. 100BASE-TX: In MDI configuration, MDIB[1]+/- is used for the receive pair and in MDIX configuration MDIB[1]+/- is used for the transmit pair. 10BASE-T: In MDI configuration, MDIB[1]+/- is used for the receive pair and in MDIX configuration MDIB[1]+/- is used for the transmit pair.
MDIB[2]+/-	A	Media Dependent Interface B [2]. 1000BASE-T: In MDI configuration, MDIB[2]+/- corresponds to BI_DC+/- and in MDIX configuration MDIB[2]+/- corresponds to BI_DD+/-. 100BASE-TX: Unused. 10BASE-T: Unused.
MDIB[3]+/-	A	Media Dependent Interface B [3]. 1000BASE-T: In MDI configuration, MDIB[3]+/- corresponds to BI_DD+/- and in MDIX configuration MDIB[3]+/- corresponds to BI_DC+/-. 100BASE-TX: Unused. 10BASE-T: Unused.

5.0 External TBI Support

Note that when internal copper PHY or internal SerDes is used, such that the external TBI interface is unused, all inputs on this interface should be grounded, either directly to ground or through (a) resistor(s).

Table 3. External TBI Pin Descriptions

Signal Name	Type	Name & Function
LOS / LINK	I	Loss of Signal (TBI) / Link Indication (Internal PHY) Loss of signal (high for lost signal) from the optical transceiver when LINK_MODE=11; active-high link indication from PHY in Internal PHY mode.
TX_DATA[9] TX_DATA[8] TX_DATA[7] TX_DATA[6] TX_DATA[5] TX_DATA[4] TX_DATA[3] TX_DATA[2] TX_DATA[1] TX_DATA[0]	O	Transmit Data: TBI: TX_DATA[9:0] for transmit data bus.
GTX_CLK	O	Transmit Clock: TBI: 125 MHz transmit clock.
EWRAP	O	Enable Wrap: TBI: EWRAP is low in normal operation. When it is high, the SerDes device is forced to transceiver loopback the serialized transmit data to the receiver. This pin is tri-stated during EEPROM read. In order to avoid a floating input in an external SerDes a weak external pull-down should be connected to this pin.
RX_DATA[9] RX_DATA[8] RX_DATA[7] RX_DATA[6] RX_DATA[5] RX_DATA[4] RX_DATA[3] RX_DATA[2] RX_DATA[1] RX_DATA[0]	I	Receive Data: TBI: RX_DATA[9:0] for receive data bus.
RBC0	I	Receive Clock 0: TBI: RBC0 is receive clock (62.5 Mb/s)
RBC1	I	Receive Clock 1: TBI: RBC1 is receive clock (62.6 Mb/s; 180 degree phase shift of RBC0).

6.0 Software Support for Dynamic Mode Switching

The device's link mode is controlled by the Extended Device Control register -- CTRL_EXT (0x00018) bits 23:22. The definitions of the LINK_MODE bits are as follows:

Table 4. Link Mode Bit Description

Field	Bits	Initial Value	Description
LINK_MODE	23:22	0[1]	Link mode This controls which interface is used to talk to the link. 00b = Direct Copper (1000Base-T) interface (GMII/MII internal PHY mode). 01bb = Reserved. 10 = Direct Fiber interface (using internal SerDes). 11b = external TBI interface.

1. Indicates value is loaded from the EEPROM upon power up.

Note: Though the LINK_MODE configuration may be specified separately for each LAN device within a dual port controller (82546EB/GB), the device only provides pins capable of supporting a single external TBI interface device at any given time. If the pins are used to support an external TBI interface, it is the responsibility of the system designer to ensure that only a single LAN device is configured for use of the external interface at any one time via the EEPROM and software settings.

The default value for the LINK_MODE setting is directly mapped from the EEPROM's Initialization Control Word 3 (bits 1:0). Software can modify the LINK_MODE indication by writing the corresponding value into this register.

In order to enable the device to dynamically change modes, the EEPROM must be programmed so that the device powers up in internal PHY mode. Therefore, it is a requirement that ICW3 bits 1:0 are set to 00b. Once the device is powered up, software can change the link mode in order to switch which interface that is currently active.

Note: Before dynamically cycling a mode, ensure via the software device driver that the current mode of operation is not in the process of transmitting or receiving data. This is achieved by disabling the transmitter and receiver, waiting until the device is in an idle state, and then beginning the process for changing the link mode.

Figure 1 shows an example of the transition process for changing modes between internal PHY and internal SerDes.

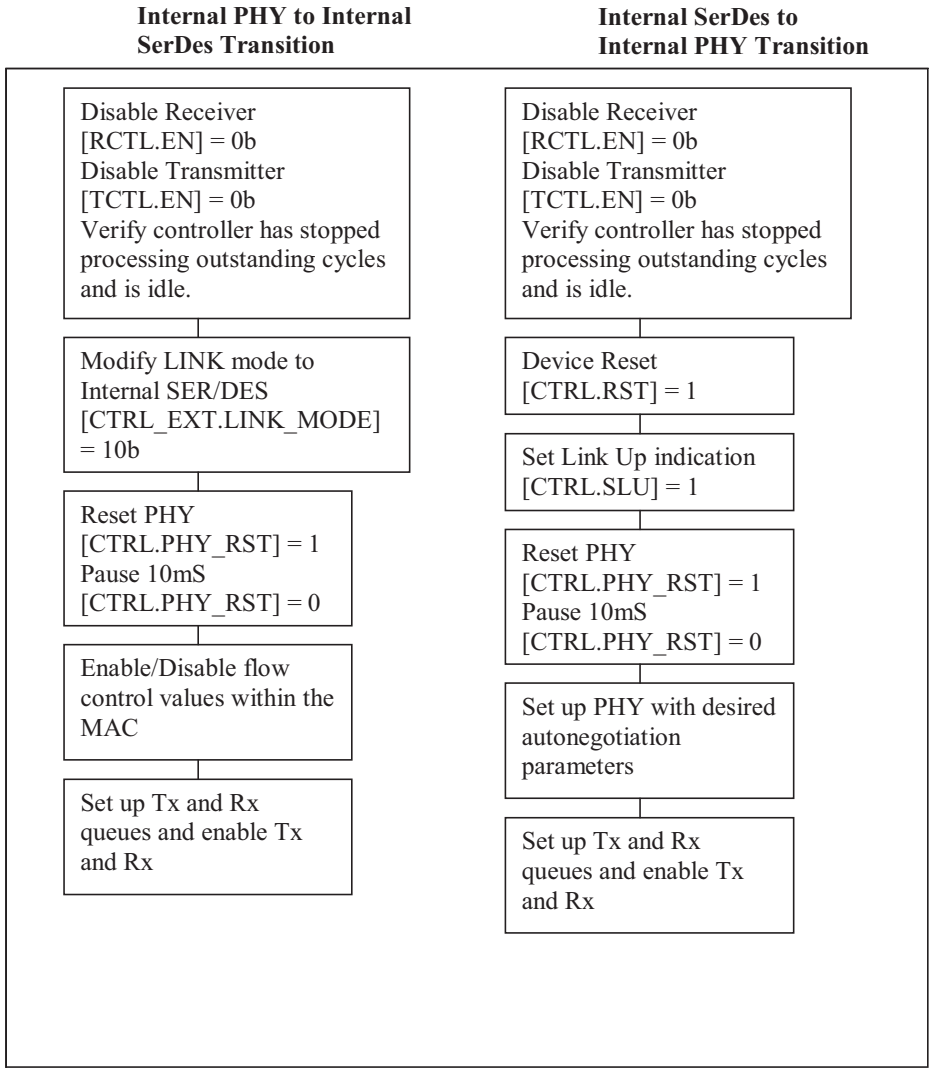


Figure 1. Sample Transition Diagram

Once the device is configured for internal SerDes mode, any device reset forces a re-read of the EEPROM, thus resetting the mode to internal PHY mode. Therefore, if software resets the device for any reason other than switching back to internal PHY mode, it is necessary to reset the link to internal SerDes mode as previously described.

Complete requirements of the software depends upon the platform and the specific application being addressed. A developer needs to configure the auto-negotiation parameters, transmit and receive configuration, and the descriptor structure for each mode as described in the *PCI/PCI-X Family of Gigabit Ethernet Controllers Software Developer's Manual*.