82541PI(ER) and 82562GZ(GX) Dual Footprint LOM Design Guide

Application Note (AP-468)

Revision 2.1
April 2005

Revision History

Revision	Revision Date	Description
0.6	Jun 2004	• Initial release
0.7	Jul 2004	• Distinguished 82562G Family from other products in line.
1.0	Aug 2004	• Added references to MDI/MDI-X feature.
1.1	Oct 2004	• Initial release White Cover Confidential (WCC). • Corrected LED configuration modes. • Replaced MagJack* references with magnetics modules.
1.2	Nov 2004	• Updated reference schematics. • Added Appendix A “Measuring LAN Reference Frequency Using a Frequency Counter.
1.3	Dec 2004	• Removed confidential status. • Added reference schematics.
2.0	Feb 2005	• Added 82541PI(ER) board design and layout information to match reference schematics. • Removed 82562G(GT) Shrink Small Outline Package (SSOP) information. This information now resides in the 82562ET/GT/G LAN on Motherboard Design Guide.
2.1	Apr 2005	• Added internal/external pull-up/pull-down resistor values for hardware configuration signals TESTEN, ISOL_EXEC, ISOL_TI, ISOL_TCK, and ADV10/LAN_DISABLE#. • Added a note on sheet 2 of reference schematics stating CLK_RUN# is not applicable to the 82541ER.

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1.0 Introduction

82541PI(ER) Gigabit Ethernet controllers and 82562GZ(GX) Platform LAN Connect (PLC) devices are all manufactured in a footprint-compatible 15 mm x 15 mm, 196-ball grid array package. Many of the critical signal pin locations on the 82541PI(ER) are identical to signals on the 82562GZ(GX) allowing designers to create a single design that accommodates these two parts. Because the usage of some pins on the 82541PI(ER) differ from the usage on the 82562GZ(GX), the two parts are not referred to as “pin compatible”. The term “footprint compatible” refers to the fact that the parts share the same package size, same number and pattern of pins, and layout of signals that allow for the flexible, cost effective, multipurpose design. Therefore, it is easy to populate a single board design with any of the two parts to maximize value while matching your customers' performance needs.

1.1 Scope

This application note identifies the design differences between the 82541PI(ER) and the 82562GZ(GX). The table in Section 5.0 lists the pinout assignments for each of the two parts.

For other necessary design collateral, please refer to “Reference Documents” (Section 1.3).

1.2 Terms

AFE	Analog Front End.
BER	Bit Error Rate.
DFD	Dual Footprint Design — a design that uses an 82562GZ/GX device with an Intel® 82541PI(ER) Gigabit Ethernet controller.
DUT	Device Under Test.
ICHx	I/O Controller Hub (ICH) that supports the 82562GZ(GX) PLC interface (x = 5, 6, or 7).
LCI	LAN Connect Interface.
BGA	Ball Grid Array.
PLC	Platform LAN Connect.
USB	Universal Serial Bus

1.3 Reference Documents

This application note assumes that you have a working knowledge of high-speed design and layout issues and the Advanced Configuration and Power Interface (ACPI) Specification. An understanding of power management industry initiatives is valuable prior to beginning the integration of an 82541PI(ER) controller or 82562GZ(GX) device into any platform. The following reference list provides sufficient background material.

- 82541ER Gigabit Ethernet Controller Datasheet. Intel Corporation.
- 82541 Family of Gigabit Ethernet Controllers Datasheet. Intel Corporation.
- 82562GZ 10/100 Mbps Platform LAN Connect (PLC) Datasheet. Intel Corporation.
- 82562GX 10/100 Mbps Platform LAN Connect (PLC) Datasheet. Intel Corporation.
- I/O Control Hub 5, 6 and 7 EEPROM Map and Programming Information. Intel Corporation.
- Intel Packaging Databook, 1999. Intel Corporation (http://developer.intel.com/design/packtech/)

Please contact your Intel representative for information related to EEPROM programming maps and ASF 1.0 implementation.

1.4 Product Codes

Table 1 lists the product ordering codes for the 82541PI(ER) and the 82562GZ(GX).

Table 1. Product Ordering Codes

Device	Product Code	Product Code (Lead Free)
82562GZ	GD82562GZ	LU82562GZ
82562GX	GD82562GX	LU82562GX
82541PI	GD82541PI	LU82541PI
82541ER	GD82541ER	LU82541ER

1.5 82541PI(ER) Gigabit Ethernet Controllers

Intel® 82541PI(ER) Gigabit Ethernet controllers are single, compact components with an integrated Gigabit Ethernet Media Access Control (MAC) and physical layer (PHY) functions. For embedded communication and network devices such as web kiosks, and point-of-sale terminal designs with critical space constraints, the 82541PI(ER) allows for a Gigabit Ethernet implementation in a very small area that is footprint compatible with current generation 10/100 Mbps Fast Ethernet designs.

The Intel® 82541PI(ER) integrates a gigabit MAC design with fully integrated, physical layer circuitry to provide a standard IEEE 802.3 Ethernet interface for 1000BASE-T, 100BASE_TX, and 10BASE-T applications (802.3, 802.3u, and 802.3ab). The controller is capable of transmitting and receiving data at rates of 1000 Mbps, 100 Mbps, or 10 Mbps. In addition to managing MAC and PHY layer functions, the controller provides a 32-bit wide direct Peripheral Component Interconnect (PCI) 2.3 compliant interface capable of operating at 33 or 66 MHz.

1.6 82562GZ(GX) Platform LAN Connect (PLC) Devices

Intel® 82562GZ(GX) PLC devices use an I/O Control Hub (ICHx) that supports the PLC interface. In these designs, an 82562GZ(GX) PLC device is used in place of an 82562EZ(EX) PLC device.

The 82562GZ(GX) is a 10/100 Mbps Ethernet device that uses Low Voltage Differential (LVD) signals (3.3 V) to drive 100 meters of Category 5 (CAT5) cable for 100 Mbps operation and Category 3 (CAT3) for 10 Mbps operation. The devices support a single interface to comply with the IEEE 802.3 standard and are available in these packages:

- 82562GZ, a 196-pin Ball Grid Array (BGA), available in lead and lead-free versions, that replaces the 82562EZ.
- 82562GX, a 196-pin BGA, available in lead and lead-free versions, that has manageability support and replaces the 82562EX.

1.6.1 Usage Modes

This section describes the five usage modes for 82562GZ(GX) devices.

1.6.1.1 Mode 0: Drop-in Replacement

Mode 0 is a drop-in replacement for a similar 82562EZ(EX) device without any required software or hardware modifications. 82562EZ(EX) product collateral can be used to design for this usage mode. Table 2 lists the appropriate replacement choices for the 82562EZ(EX) devices:

Table 2. Drop-in Replacement Mode

82562E	82562G	Description
82562EZ	82562GZ	196-pin BGA
82562EX	82562GX	196-pin BGA with Alert on LAN (AoL) and ASF 1.0 support

Note: For this mode, some BOM component values can be changed to improve performance using 82562GZ(GX) devices without changing the layout of a board designed for 82562EZ(EX) devices. For example, transmit and receive termination resistors as well as RBIAS10 and RBIAS100 resistor values.

1.6.1.2 Modes 1, 2, 3, and 4: New Features

82562GZ(GX) products support several new features that offer design flexibility and reduced BOM cost compared to 82562EZ(EX) devices. To implement these new features, the board design must include the proper pull-up and/or pull-down strapping resistor options that are used to change modes of operation (refer to Table 3).

Table 3. New Usage Modes

Mode	Benefit	Design Impact
Mode 0: 82562EZ(EX) compatible.	No BOM changes necessary for equivalent performance to 82562EZ(EX).	Equivalent functionality to the 82562EZ(EX).
Mode 1: LED configuration B and single-pin LAN disable.	Usability and reduced BOM cost.	Strapping resistors, LAN Disable circuit and LED circuit design.
Mode 2: Same as mode 1, except LED configuration C.	Usability and reduced BOM cost.	Strapping resistors, LAN Disable circuit and LED circuit design.
Mode 3: LED configuration B, Single Pin LAN Disable, and enhanced Tx mode[1].	Usability, reduced BOM cost, and stronger Tx drive strength.	Strapping resistors, LAN Disable circuit and LED circuit design.
Mode 4: Same as mode 3, except LED configuration C. See footnote 1.	Usability, reduced BOM cost, and stronger Tx drive strength.	Strapping resistors, LAN Disable circuit and LED circuit design.

1. Only use this mode if advised to do so by an Intel representative.

2.0 Frequency Control Device Design Considerations

This section provides information regarding frequency control devices, including crystals and oscillators, for use with all Intel® Ethernet controllers. Several suitable frequency control devices are available; none of which present any unusual challenges in selection. The concepts documented herein are applicable to other data communication circuits, including Physical Layer devices (PHYs).

The Intel® Ethernet controllers contain amplifiers which, when used with the specific external components, form the basis for feedback oscillators. These oscillator circuits, which are both economical and reliable, are described in more detail in “Crystal Selection Parameters”.

The Intel® Ethernet controllers also have bus clock input functionality, however a discussion of this feature is beyond the scope of this document, and will not be addressed.

The chosen frequency control device vendor should be consulted early in the design cycle. Crystal and oscillator manufacturers familiar with networking equipment clock requirements may provide assistance in selecting an optimum, low-cost solution.

2.1 Frequency Control Component Types

Several types of third-party frequency reference components are currently marketed. A discussion of each follows, listed in preferred order.

2.2 Quartz Crystal

Quartz crystals are generally considered to be the mainstay of frequency control components due to their low cost and ease of implementation. They are available from numerous vendors in many package types and with various specification options (see Table 4).

Table 4. Recommended Crystals

Manufacturer	Part Number
Raltron	AS-25.000-20-F-SMD-T
Citizen America Corp	HCM4925.000MBBKTR
NDK America Inc	41CD25.0S11005020
TXC Corporation - USA	6C25000131

2.3 Fixed Crystal Oscillator

A packaged fixed crystal oscillator is comprised of an inverter, a quartz crystal, and passive components conveniently packaged together. The device renders a strong, consistent square wave output. Oscillators used with microprocessors are supplied in many configurations and tolerances.

Crystal oscillators should be restricted to use in special situations, such as shared clocking among devices or multiple controllers. As clock routing can be difficult to accomplish, it is preferable to provide a separate crystal for each device.

For Intel® Ethernet controllers, it is acceptable to overdrive the internal inverter by connecting a 25 MHz external oscillator to the X1 lead, leaving the X2 lead unconnected. The oscillator should be specified to drive CMOS logic levels, and the clock trace to the controller should be as short as possible. Controller specifications typically call for a 40% (minimum) to 60% (maximum) duty cycle and a ±50 ppm frequency tolerance across the entire operating temperature range as required by IEEE specifications. Intel recommends a ±30 ppm frequency tolerance.

Note: Please contact your Intel Customer Representative to obtain the most current device documentation prior to implementing this solution.

2.4 Programmable Crystal Oscillators

A programmable oscillator can be configured to operate at many frequencies. The device contains a crystal frequency reference and a phase lock loop (PLL) clock generator. The frequency multipliers and divisors are controlled by programmable fuses.

A programmable oscillator's accuracy depends heavily on the Ethernet controller's differential transmit lines. The Physical Layer (PHY) uses the clock input from the device to drive a differential Manchester (for 10 Mbps operation), an MLT-3 (for 100 Mbps operation) or a PAM-5 (for 1000 Mbps operation) encoded analog signal across the twisted pair cable. These signals are referred to as self-clocking, which means the clock must be recovered at the receiving link partner. Clock recovery is performed with another PLL that locks onto the signal at the other end.

PLLs are prone to exhibit frequency jitter. The transmitted signal can also have considerable jitter even with the programmable oscillator working within its specified frequency tolerance. PLLs must be designed carefully to lock onto signals over a reasonable frequency range. If the transmitted signal has high jitter and the receiver's PLL loses its lock, then bit errors or link loss can occur.

PHY devices are deployed for many different communication applications. Some PHYs contain PLLs with marginal lock range and cannot tolerate the jitter inherent in data transmission clocked with a programmable oscillator. The American National Standards Institute (ANSI) X3.263-1995 standard test method for transmit jitter is not stringent enough to predict PLL-to-PLL lock failures, therefore, the use of programmable oscillators is generally not recommended.

2.5 Ceramic Resonator

Similar to a quartz crystal, a ceramic resonator is a piezoelectric device. A ceramic resonator typically carries a frequency tolerance of ±0.5%, – inadequate for use with Intel® Ethernet controllers, and therefore, should not be used.

3.0 Ethernet Component Design Guidelines

This section provides recommendations for selecting components and connecting special pins. The main design elements are the 82562GZ(GX) PLC device or the 82541PI(ER) Gagabit Ethernet controller, external resistor connections (82562GZ(GX) only), a magnetics module with RJ-45 connector, and a crystal clock source.

3.1 General Design Considerations for Ethernet Controllers

These recommendations apply to all designs, 10/100 Mbps or 10/100/1000 Mbps.

Good engineering practices should be followed with respect to unused inputs by terminating them with pull-up or pull-down resistors, unless the datasheet, design guide or reference schematic indicates otherwise. Do not attach pull-up or pull-down resistors to any balls identified as reserved (unless explicitly included in the reference schematic). These devices may have special test modes that could be entered inadvertently.

3.1.1 Crystal Selection Parameters

Quartz crystals are generally considered to be the mainstay of frequency control components due to their low cost and ease of implementation. They are available from numerous vendors in many package types and with various specification options.

All crystals used with Intel® Ethernet controllers are described as “AT-cut”, which refers to the angle at which the unit is sliced with respect to the long axis of the quartz stone.

Table 5 lists the crystal electrical parameters and provides suggested values for typical designs. The parameters listed are described in the following subsections.

Table 5. Crystal Parameters

Parameter	Suggested Value
Vibration Mode	Fundamental
Nominal Frequency	25,000 MHz at 25° C (required)
Frequency Tolerance	• ±30 ppm recommended; ±50 ppm across the entire operating temperature range as required by IEEE specifications • ±30 ppm required for the 82562GZ(GX)
Temperature Stability	• ±50 ppm at 0° C to 70° C • ±30 ppm at 0° C to 70° C required for the 82562GZ(GX)
Calibration Mode	Parallel
Non Operating Temperature Range	-40 to 90° C for the 82562GZ(GX)
Load Capacitance	• 16 pF to 20 pF • 20 pF required for the 82562GZ(GX)
Pullability from Nominal Load Capacitance	15 ppm/pF maximum for the 82562GZ(GX)
Shunt Capacitance	6 pF maximum
Equivalent Series Resistance	50 Ω maximum

Table 5. Crystal Parameters

Drive Level	0.5 mW maximum
Aging	±5 ppm per year maximum
Insulation Resistance	500 MΩ minimum at DC 100 V for the 82562GZ(GX)
Package	HC49 for the 82562GZ(GX)

Note: A sampling of crystals that meet the specifications outlined for the 82562GZ(GX) is listed below:

Epson-Seiko MA-406-25.000M-20PF*

Epson-Seiko MA-406H*

Please consult with your Intel representative before implementing a design that uses another type of clock source. Careful design is required if using a fixed oscillator. Intel discourages the use of programmable oscillators and ceramic resonators. See Appendix A, "Measuring LAN Reference Frequency Using a Frequency Counter" for more information.

3.1.1.1 Vibration Mode

Crystals in the frequency range listed in Table 5 are available in both fundamental and third overtone. Unless there is a special need for third overtone, use fundamental mode crystals.

At any given operating frequency, third overtone crystals are thicker and more rugged than fundamental mode crystals. Third overtone crystals are more suitable for use in military or harsh industrial environments. Third overtone crystals require a trap circuit (extra capacitor and inductor) in the load circuitry to suppress fundamental mode oscillation as the circuit powers up. Selecting values for these components is beyond the scope of this document.

3.1.1.2 Nominal Frequency

Intel® Ethernet controllers use a crystal frequency of 25.000 MHz. The 25 MHz input is used to generate a 125 MHz transmit clock for 100BASE-TX and 1000BASE-TX operation; 10 MHz and 20 MHz transmit clocks, for 10BASE-T operation.

3.1.1.3 Frequency Tolerance

The frequency tolerance for an Ethernet physical layer device is dictated by the IEEE 802.3 specification as ±50 parts per million (ppm). This measurement is referenced to a standard temperature of 25° C.

Note: Intel recommends a frequency tolerance of ±30 ppm.

3.1.1.4 Temperature Stability and Environmental Requirements

Temperature stability is a standard measure of how the oscillation frequency varies over the full operational temperature range (and beyond). Several optional temperature ranges are currently available, including -40° C to +85° C for industrial environments. Some vendors separate operating temperatures from temperature stability. Manufacturers may also list temperature stability as 50 ppm in their data sheets.

Note: Crystals also carry other specifications for storage temperature, shock resistance, and reflow solder conditions. Crystal vendors should be consulted early in the design cycle to discuss the application and its environmental requirements.

3.1.1.5 Calibration Mode

The terms “series-resonant” and “parallel-resonant” are often used to describe crystal circuits. Specifying parallel mode is critical to determining how the crystal frequency is calibrated at the factory.

A crystal specified and tested as series resonant oscillates without problem in a parallel-resonant circuit, but the frequency is higher than nominal by several hundred parts per million. The purpose of adding load capacitors to a crystal circuit is to establish resonance at a frequency higher than the crystal’s inherent series resonant frequency.

Figure 1 illustrates a simplified schematic of the 82562GZ(GX) and the 82541PI(ER) controller’s crystal circuit. The crystal and the capacitors form a feedback element for the internal inverting amplifier. This combination is called parallel-resonant, because it has positive reactance at the selected frequency. In other words, the crystal behaves like an inductor in a parallel LC circuit.

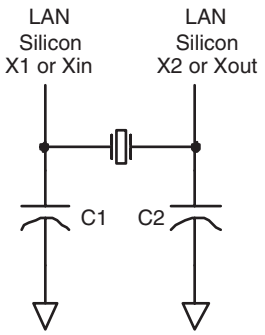


Figure 1. Crystal Circuit

3.1.1.6 Load Capacitance

The formula for crystal load capacitance is as follows:

$$C_L = \frac{(C1 \cdot C2)}{(C1 + C2)} + C_{stray}$$

where C1 = C2 = 22 pF (as suggested in most Intel reference designs)
and C_{stray} = allowance for additional capacitance in pads, traces and the chip carrier within the Ethernet controller package

An allowance of 3 pF to 7 pF accounts for lumped stray capacitance. The calculated load capacitance is 16 pF with an estimated stray capacitance of about 5 pF.

Individual stray capacitance components can be estimated and added. For example, surface mount pads for the load capacitors add approximately 2.5 pF in parallel to each capacitor. This technique is especially useful if Y1, C1 and C2 must be placed farther than approximately one-half (0.5) inch from the controller. It is worth noting that thin circuit boards generally have higher stray capacitance than thick circuit boards.

Standard capacitor loads used by crystal manufacturers include 16 pF, 18 pF and 20 pF. Any of these values will generally operate with the controller. However, a difference of several picofarads between the calibrated load and the actual load will pull the oscillator slightly off frequency.

Note: C1 and C2 can vary by as much as 5% (approximately 1 pF) from their nominal values.

3.1.1.7 Shunt Capacitance

The shunt capacitance parameter is relatively unimportant compared to load capacitance. Shunt capacitance represents the effect of the crystal's mechanical holder and contacts. The shunt capacitance should equal a maximum of 6 pF (7 pF is also acceptable).

3.1.1.8 Equivalent Series Resistance

Equivalent Series Resistance (ESR) is the real component of the crystal's impedance at the calibration frequency, which the inverting amplifier's loop gain must overcome. ESR varies inversely with frequency for a given crystal family. The lower the ESR, the faster the crystal starts up. Use crystals with an ESR value of 50 Ω or better.

3.1.1.9 Drive Level

Drive level refers to power dissipation in use. The allowable drive level for a Surface Mounted Technology (SMT) crystal is less than its through-hole counterpart, because surface mount crystals are typically made from narrow, rectangular AT strips, rather than circular AT quartz blanks.

Some crystal data sheets list crystals with a maximum drive level of 1 mW. However, Intel® Ethernet controllers drive crystals to a level less than the suggested 0.5 mW value. This parameter does not have much value for on-chip oscillator use.

3.1.1.10 Aging

Aging is a permanent change in frequency (and resistance) occurring over time. This parameter is most important in its first year because new crystals age faster than old crystals. Use crystals with a maximum of ±5 ppm per year aging.

3.1.2 Reference Crystal

The normal tolerances of the discrete crystal components can contribute to small frequency offsets with respect to the target center frequency. To minimize the risk of tolerance-caused frequency offsets causing a small percentage of production line units to be outside of the acceptable frequency range, it is important to account for those shifts while empirically determining the proper values for the discrete loading capacitors, C1 and C2.

Even with a perfect support circuit, most crystals will oscillate slightly higher or slightly lower than the exact center of the target frequency. Therefore, frequency measurements (which determine the correct value for C1 and C2) should be performed with an ideal reference crystal. When the capacitive load is exactly equal to the crystal's load rating, an ideal reference crystal will be perfectly centered at the desired target frequency.

3.1.3 Reference Crystal Selection

There are several methods available for choosing the appropriate reference crystal:

- If a Saunders and Associates (S&A) crystal network analyzer is available, then discrete crystal components can be tested until one is found with zero or nearly zero ppm deviation (with the appropriate capacitive load). A crystal with zero or near zero ppm deviation will be a good reference crystal to use in subsequent frequency tests to determine the best values for C1 and C2.
- If a crystal analyzer is not available, then the selection of a reference crystal can be done by measuring a statistically valid sample population of crystals, which has units from multiple lots and approved vendors. The crystal, which has an oscillation frequency closest to the center of the distribution, should be the reference crystal used during testing to determine the best values for C1 and C2.
- It may also be possible to ask the approved crystal vendors or manufacturers to provide a reference crystal with zero or nearly zero deviation from the specified frequency when it has the specified CLoad capacitance.

When choosing a crystal, customers must keep in mind that to comply with IEEE specifications for 10/100 and 10/100/1000Base-T Ethernet LAN, the transmitter reference frequency must be precise within ±50 ppm. Intel® recommends customers to use a transmitter reference frequency that is accurate to within ±30 ppm to account for variations in crystal accuracy due to crystal manufacturing tolerance. For information about measuring transmitter reference frequency, refer to Appendix A, "Measuring LAN Reference Frequency Using a Frequency Counter".

3.1.4 Circuit Board

Since the dielectric layers of the circuit board are allowed some reasonable variation in thickness, the stray capacitance from the printed board (to the crystal circuit) will also vary. If the thickness tolerance for the outer layers of dielectric are controlled within ±17 percent of nominal, then the circuit board should not cause more than ±2 pF variation to the stray capacitance at the crystal. When tuning crystal frequency, it is recommended that at least three circuit boards are tested for frequency. These boards should be from different production lots of bare circuit boards.

Alternatively, a larger sample population of circuit boards can be used. A larger population will increase the probability of obtaining the full range of possible variations in dielectric thickness and the full range of variation in stray capacitance.

Next, the exact same crystal and discrete load capacitors (C1 and C2) must be soldered onto each board, and the LAN reference frequency should be measured on each circuit board.

The circuit board, which has a LAN reference frequency closest to the center of the frequency distribution, should be used while performing the frequency measurements to select the appropriate value for C1 and C2.

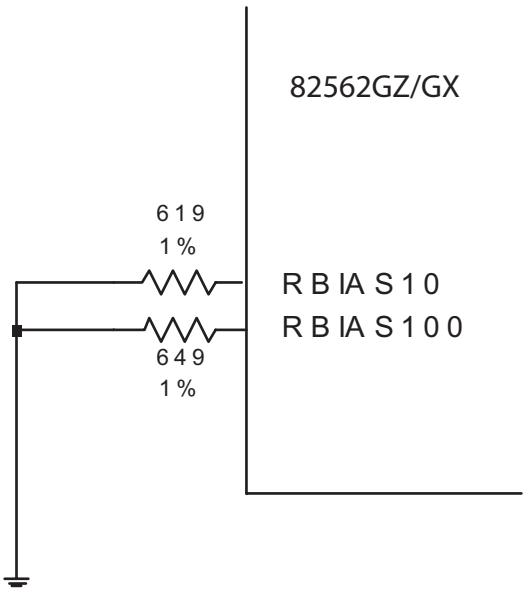
3.1.5 Temperature Changes

Temperature changes can cause the crystal frequency to shift. Therefore, frequency measurements should be done in the final system chassis across the system's rated operating temperature range.

3.2 Analog References for 82562GZ(GX) Designs

There are two inputs, RBIAS10 and RBIAS100, to 82562GZ(GX) devices that require external resistor connections to bias the internal analog section of the device. These inputs are sensitive to the resistor value and experimentation is needed to select the correct values for any given layout. Resistors of 1% tolerance must be used. Figure 2 shows an example of one possible design.

Figure 2. RBIAS10 and RBIAS100 Circuits



3.3 Integrated Magnetics Module

The magnetics module has a critical effect on overall IEEE and emissions conformance. The device should meet the performance required for a design with reasonable margin to allow for manufacturing variation. Occasionally, components that meet basic specifications may cause the system to fail IEEE testing because of interactions with other components or the Printed Circuit Board (PCB) itself. Carefully qualifying new magnetics modules can go a long way toward preventing this type of problem.

The steps involved in magnetics module qualification are similar to those for oscillator qualification:

1. Verify that the vendor's published specifications in the component data sheet meet the required IEEE specifications.
2. Independently measure the component's electrical parameters on a test bench, checking samples from multiple lots. Check that the measured behavior is consistent from sample to sample as well as meeting the published specifications.
3. Perform physical layer conformance testing and EMC (FCC and EN) testing in real systems.

Note: Magnetics modules for 1000Base-T Ethernet are similar to those designed solely for 10/100 Mbps, with the exception of four differential signal pairs instead of two for 10/100 Mpbs.

3.4 Designing with the 82562GZ(GX) Platform LAN Connect Device

This section provides design guidelines specific to the PLC device.

3.4.1 Power Supplies for 82562GZ(GX) PLC Implementations

The 82562GZ(GX) PLC device uses a single 3.3 V power supply. The 3.3 V supply must provide approximately 90 mA of current for full speed operation. Standby power must be furnished in order to wake up from a power down.

3.4.2 82562GZ(GX) Device Test Capability

The 82562GZ(GX) device contains an XOR test tree mechanism for simble board tests. Details of the XOR tree operation are contained in the 82562GZ and 82562GX datasheets.

3.4.3 82562GZ/GX PLC Device LAN Disable Guidelines

For 82562GZ(GX) drop-in mode LAN disable circuit, see the “Drop-in Replacement Schematic” in Section 7.0 and the appropriate 82562EZ(EX) product design guide.

For the new single pin LAN Disable circuit available in modes 1-4, see the related schematics in Section 7.0.

3.4.4 Serial EEPROM for 82562GZ(GX) Implementations

Serial EEPROM for LAN implementations based on 82562GZ(GX) devices connect to the ICH5, ICH6, or ICH7). Depending on the size of the EEPROM, the 82562GZ(GX) can support legacy manageability or not. Table 6 and Table 7 list the EEPROM map for the 82562GZ(GX) PLC device; Table 8 lists the recommended EEPROM manufacturers. For details on the EEPROM, see the *I/O Control Hub 5, 6, and 7 EEPROM Map and Programming Information*.

Note: See your Intel representative for later information on later versions of the I/O Control Hub.

Table 6. 82562GZ(GX) Memory Layout (128B EEPROM)

00h **3Fh**	HW/SW Reserved Area

Note: No manageability provided.

Table 7. 82562GZ(GX) Memory Layout (512B EEPROM)

00h **3Fh**	HW/SW Reserved Area
40h **FFh**	ASF and Legacy Manageability

Note: Legacy manageability only.

Table 8. Recommended EEPROM Manufacturers

Vendor	Part Number	Package	Interface	Size (Kb)
Catalyst[1]	CAT93C46S-TE13	SOIC8	uWire	1
Atmel	AT93C46-10SI-2.7	SOIC8	uWire	1
Catalyst	CAT93C66S-TE13	SOIC8	uWire	4
Atmel	AT93C66-10SI-2.7	SOIC8	uWire	4

1. Revision H is not supported. Product die revision letter is marked on top of the package as a suffix to the production data code (e.g., AYWW**H**.)

3.4.5 Magnetics Modules for 82562GZ(GX) PLC Devices

A 5-core magnetics module should be carefully selected for specific designs. Table 9 lists suggested integrated magnetics modules for use with 82562GZ(GX) PLC devices. These modules also contain integrated USB jacks.

Note: These components are pin-compatible with the magnetics modules listed in Table 13 for the 82541PI(ER) controller.

Table 9. Recommended Magnetics Modules

Manufacturer	Part Number	Type
Pulse	H1138	Discrete
Pulse	JWOA1P01R	Integrated
Stewart Connector Systems	SI-70027	RJ-45/Magnetic
Pulse	H1338 (MDI-X only)	Discrete

3.5 Flash Interface

The ICHx does not support a Flash interface.

Note: The Intel Boot Agent is supported via the System BIOS.

3.6 Designing with 82541PI(ER) Gigabit Controllers

This section provides design guidelines specific to 82541PI(ER) Gigabit Ethernet Controllers.

3.6.1 82541PI(ER) Gigabit Controller LAN Disable Guidelines

The 82541PI(ER) controller has a LAN disable function that is present on FLSH_SO, ball P9. This pin can be connected to a Super IO component to allow the BIOS to disable the Ethernet port (see Figure 3). If the serial Flash interface is populated, the Flash serial output pin must not interfere with this function.

Do not attempt to use the LAN_POWER_GOOD signal for a LAN disable input on the 82541PI(ER) controller. This pin is intended to operate as a power-on reset connected to a power monitor circuit.

The input of the 82541PI(ER) FLSH_SO (pin P9) is the LAN_DISABLE# signal. It is sampled on the rising edge of LAN_PWR_GOOD or RST#. The signal must be held valid for 80 ns after either rising edge.

If it is sampled high, the LAN functions normally. If it is sampled low, then the following occurs:

1. The LAN is disabled.
2. The PHY is powered down.

3. Most MAC clock domains are gated.
4. Most functional blocks are held in reset.
5. PCI inputs and outputs are floated.
6. The device will not respond to PCI cycles (including configuration cycles).
7. The device is put in a low power state, which is equivalent to D3 without wakeup or manageability.

Note: To use this configuration for the 82562GZ(GX) PLC device, be sure the AND gate U1 is populated. Depopulate the 0 Ω resistor R2.

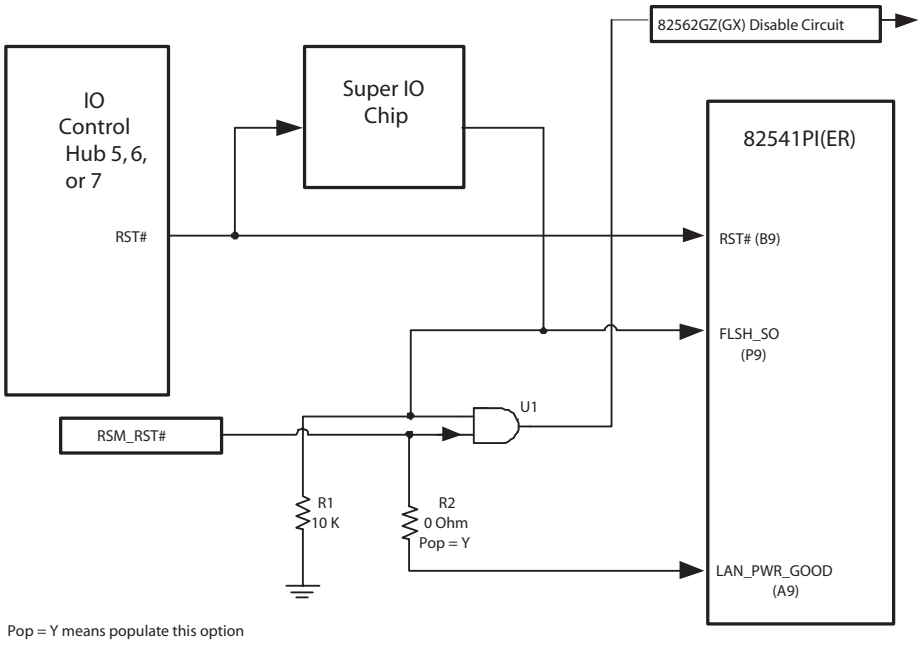


Figure 3. 82541PI(ER) LAN Disable Circuitry

3.6.2 Power Supplies for 82541PI(ER) Gigabit Ethernet Controllers

The 82541PI(ER) controller requires three power supplies: 1.2 V, 1.8 V, and 3.3 V. The 1.2 V supply must provide approximately 500 mA current, and the 1.8 V supply, approximately 230 mA current. The 3.3 V supply must provide only 30 mA current.

A central power supply can provide all the required voltage sources, or the power can be derived and regulated locally near the Ethernet control circuitry. All voltage sources must remain present during power down in order to use the 82541PI(ER) LAN wake up capability. This consideration makes it more likely that at least some of the voltage sources will be local.

Instead of using external regulators to supply 1.2 V and 1.8 V, power transistors can be used in conjunction with on-chip regulation circuitry. (See the reference schematic for an implementation example.)

The 82541PI(ER) controller has a LAN_PWR_GOOD input. Treat this signal as an external device reset which works in conjunction with the internal power-on reset circuitry. In the situation where a central power supply furnishes all the voltage sources, LAN_PWR_GOOD can be tied to the POWER_GOOD output of the power supply. Designs that generate some of the voltages locally can connect LAN_PWR_GOOD to a power monitor chip.

The power sources are all expected to ramp up during a brief power-up interval (approximately 20 ms) with LAN_PWR_GOOD de-asserted. The 82541PI(ER) controller must not be left in a prolonged state where some, but not all, voltages are applied. The 3.3 V source should be powered up prior to the 1.2 V or 1.8 V sources. The 1.2 V and 1.8 V power supplies may power up simultaneously. At any time during power up, the supply voltages must be: 1.2 V < 1.8 V < 3.3 V.

3.6.3 82541PI(ER) Controller Power Supply Filtering

The 82541PI(ER) controller switches relatively high currents at high frequencies, requiring generous use of both bulk capacitance and high speed decoupling capacitance adjacent to the device.

Bypass capacitors for each power rail should be 0.1 µF. If possible, orient the capacitors close to the device and adjacent to power pads. Decoupling capacitors should connect to the power and ground planes with short, thick traces (15 mils or 0.4 mm or more), and 14 mil (3.5 mm) vias per capacitor pad.

Furnish approximately 20 µF of bulk capacitance for each of the main 1.2 V and 1.8 V levels. This can be easily achieved by using two 10 µF capacitors, placing them as close to the device power connections as possible.

3.6.4 82541PI(ER) Controller Power Management and Wake Up

The 82541PI(ER) controller supports low power operation as defined in the PCI Bus Power Management Specification. There are two defined power states, D0 and D3. The D0 state provides full power operation and is divided into two sub-states: D0u (uninitialized) and D0a (active). The D3 state provides low power operation and is also divided into two sub-states: D3hot and D3cold.

To enter the low power state, the software driver must stop data transmission and reception. Either the operating system or the driver must program the Power Management Control/Status Register (PMCSR) and the Wakeup Control Register (WUC). If wakeup is desired, the appropriate wakeup LAN address filters must also be set. The initial power management settings are specified by EEPROM bits.

When the 82541PI(ER) controller transitions to either of the D3 low power states, the 1.2 V, 1.8 V, and 3.3 V sources must continue to be supplied to the device. Otherwise, it will not be possible to use a wakeup mechanism. The AUX_POWER signal is a logic input to the 82541PI(ER) controller that denotes auxiliary power is available. If AUX_POWER is asserted, the 82541PI(ER controller advertises that it supports wake up from a D3cold state.

The 82541PI(ER) device supports both Advanced Power Management (APM) wakeup and Advanced Configuration and Power Interface (ACPI) wakeup. APM wakeup has also been known in the past as “Wake on LAN.”

Wakeup uses the PME# signal to wake the system. PME# is an active low signal connected to a GPIO port on the ICH5, ICH6, or ICH7 that goes active in response to receiving a Magic Packet*, a network wake-up packet, or link status change indication. PME# remains asserted until it is disabled through the Power Management Control/Status Register.

3.6.5 82541PI(ER) Controller Test Capability

The 82541PI(ER) controller contains a test access port conforming to the IEEE 1149.1a-1994 (JTAG) Boundary Scan specification. To use the test access port, these balls need to be connected to pads accessible by the test equipment. The TRST# input also needs to be connected to ground through a pull-down resistor (approximately 100 Ω) so that the test capability cannot be invoked by mistake.

A Boundary Scan Definition Language (BSDL) file describing the 82541PI(ER) controller is available for use in your test environment.

The 82541PI(ER) controller also contains an XOR test tree mechanism for simple board tests. Details of XOR tree operation may be obtained through your Intel representative.

3.6.6 Serial EEPROM for 82541PI(ER) Controller Implementations

82541PI(ER) controllers can use either a Microwire* or an SPI* serial EEPROM. The EEPROM mode is selected on the EEMODE input (pin J4). A no connect denotes an SPI EEPROM and a pull-down resistor to ground denotes a Microwire EEPROM. Several words of the EEPROM are accessed automatically by the device after reset to provide pre-boot configuration data before it is accessed by host software. The remainder of the EEPROM space is available to software for storing the MAC address, serial numbers, and additional information.

For non-ASF applications, a 64 register by 16-bit Microwire serial EEPROM should be used, and for ASF 1.0 applications, a larger 93C66 Microwire or AT25040 SPI* serial EEPROM. ASF 2.0 requires an 8 KB SPI* serial EEPROM.

Intel has an MS-DOS* software utility called EEUPDATE, which can be used to program EEPROM images in development or production line environments. To obtain a copy of this program, contact your Intel representative.

The EEPROM access algorithm programmed into the 82541PI(ER) controller is compatible with most, but not all, commercially available 3.3 V Microwire* interface, serial EEPROM devices, with 64 x 16 (or 256 x 16) organization and a 1 MHz speed rating. The 82541PI(ER) EEPROM access algorithm drives extra pulses on the shift clock at the beginnings and ends of read and write cycles. The extra pulses may violate the timing specifications of some EEPROM devices. In selecting a serial EEPROM, choose a device that specifies “don't care” shift clock states between accesses.

Microwire EEPROMs that have been found to work satisfactorily with the 82541PI(ER) Gigabit Ethernet controller are listed in Table 10:

Table 10. Microwire 64 x 16 Serial EEPROMs

Manufacturer	Manufacturer's Part Number
Atmel	AT93C46[1]
Catalyst	CAT93C46[1,2]

1. No manageability provided.
2. Revision H is not supported. Product die revision letter is marked on top of the package as a suffix to the production data code (e.g., AYWW**H**.)

SPI* EEPROMs that have been found to work satisfactorily with the 82541PI(ER) controller are listed in Table 11. SPI* EEPROMs must be rated for a clock rate of at least 2 MHz.

Table 11. SPI* Serial EEPROMs for 82541PI(ER) Controller

Application	Manufacturer	Manufacturer's Part Number
ASF 1.0 or IPMI pass through	ATMEL	AT25040
ASF 2.0 or IPMI advanced pass through	ATMEL	AT25080

3.6.7 EEPROM Map Information

Table 12 lists the EEPROM map for the 82541PI(ER) Gigabit Ethernet controller.

Table 12. 82541PI(ER) EEPROM Memory Layout

00h **3Fh**	HW/SW Reserved Area
40h **FFh**	ASF and Legacy Manageability
100h **19F**	Manageability Packet Filter Data
1A0 **...** **EEPROM END**	Loadable Manageability Firmware Code

NOTE: Full manageability provided.

3.6.8 Magnetics Modules for 82541PI(ER) Controller Applications

There are several different types of magnetics modules. For example, some magnetics modules have USB connectors or RJ-45 connectors. There are also several discrete modules that can be used for optimal performance. A gigabit magnetics module should be carefully selected for your design.

Table 13 lists suggested integrated magnetics modules for use with the 82541PI(ER) controller. These modules also contain integrated USB jacks. A good quality Gigabit Ethernet magnetics module can also be used with the 82562GZ(GX) PLC device. Table 14 and Table 15 list the electrical specifications for the 10/100/1000 magnetics.

Note: These components are pin-compatible with the magnetics modules shown in Table 9 for the 82562GZ(GX) PLC device.

Table 13. 82541PI(ER) Recommended Magnetics Modules

Manufacturer	Manufacturer's Part Number
Pulse	JW0A2P019D (82541PI)
Discrete	H5007 (82541ER)

Table 14. Electrical Specifications at 25°C for 10/100 Magnetics

Insertion Loss (TX / RX)	
0.1 through 0.999 MHz	1.0 dB maximum
1.0 through 15 MHz	0.35 dB maximum
15.1 through 6 0MHz	0.7 dB maximum
60.1 through 100 MHz	1.2 dB maximum
Return Loss (TX / RX)	
1.0 through 30 MHz	18 dB minimum
30.1 through 60 MHZ	19 - [20Log(f/30 MHz)] dB minimum
60.1 through 80 MHz	12 dB minimum
Transmit Common Mode-to-Common Mode Reject	
1.0 through 60 MHz	48 dB minimum
60.1 through 100 MHz	43 dB minimum
100.1 through 150 MHz	42 dB minimum
Effective Common Mode-to-Common Mode Reject	
1.0 through 60 MHz	38 dB minimum
60.1 through 100 MHz	34 dB minimum
100.1 through 150 MHz	32 dB minimum
Transmit Differential to Common Mode Reject	
1.0 through 60 MHz	38 dB minimum
60.1 through 100 MHz	35 dB minimum
100.1 through 150 MHz	32 dB minimum
Receive Differential to Common Reject	
1.0 THRU 60 MHz	30 dB minimum
60.1 through 100 MHz	25 dB minimum
100.1 through 150 MHz	20 dB minimum
Crosstalk Isolation (TX / RX)	
1.0 through 60 MHz	48 dB minimum
60.1 through 100 MHz	43 dB minimum
100.1 through 150 MHz	38 dB minimum
High Voltage Isolation	
IEEE 14.3.1.1	2250 V dc for 60 seconds
OCL with 8mA Bias 100 KHz	400 µH

Table 15. Electrical Specifications at 25° C for 1000 Gb Silicon

Insertion Loss (TX / RX)	
0.1 through 999 kHz	1.0 dB maximum
1.0 through 60.0 MHz	0.6 dB maximum
60.1 through 80.0 MHz	0.8 dB maximum
80.1 through 100.0 MHz	1.0 dB maximum
100 through 125.0 MHz	2.4 dB maximum
Return Loss (TX / RX)	
1.0 through 40.0 MHz	18 dB minimum
40.1 through 100 MHZ	12 - [20Log(f/80 MHz)] dB minimum
Common Mode-to-Common Mode Rejection	
1.0 through 60 MHz	48 dB minimum
60.1 through 100 MHz	42 dB minimum
100.1 through 150 MHz	37 dB minimum
Differential-to-Common Mode Rejection	
1.0 through 60 MHz	35 dB minimum
60.1 through 100 MHz	29 dB minimum
100.1 through 150 MHz	22 dB minimum
Crosstalk Isolation (TX / RX)	
1.0 through 80 MHz	36 dB minimum
80.1 through 150 MHz	27dB minimum
High Voltage Isolation	
1500 Vrms minimum, at 50 to 60 Hz, for 60 sec.	2250 V dc for 60 seconds
OCL with 8 mA Bias	400 uH minimum

3.6.9 Oscillators for 82541PI Controllers

The 82541PI clock input circuit is optimized for use with an external crystal. However, an oscillator may also be used in place of the crystal with the proper design considerations (see Table 17):

- The clock oscillator has an internal voltage regulator of 1.2 V to isolate it from the external noise of other circuits to minimize jitter. If an external clock is used, this imposes a maximum input clock amplitude of 1.2 V.
- The input capacitance introduced by the 82541PI (approximately 20 pF) is greater than the capacitance specified by a typical oscillator (approximately 15 pF).
- The input clock jitter from the oscillator can impact the 82541PI clock and its performance.

Table 16. 82541PI Clock Oscillator Specifications

Symbol	Parameter	Specifications			Units
		Min	Typical	Max	
f0	Frequency		25		MHz
df0	Frequency Variation	-50		+30	ppm
Dc	Duty Cycle	40		60	%
tr	Rise Time			5	ns
tf	Fall Time			5	ns
σi	Clock Jitter, rms (if specified)			50	ps
C1	Clock Capacitance (pushed by clock)		15	50	pF
VDD	Supply Voltage		3.3 or 1.8		V
Operating temperature				70	° C
CMOS output levels	Voltage Output High (Voh), Voltage Output Low (Vol)	80% VDD		 20% VDD	V V

3.6.10 82541PI(ER) Oscillator Solution

There are two oscillator solutions for the 82541PI(ER): high voltage and low voltage.

3.6.10.1 High Voltage Solution (VDD = 3.3 V)

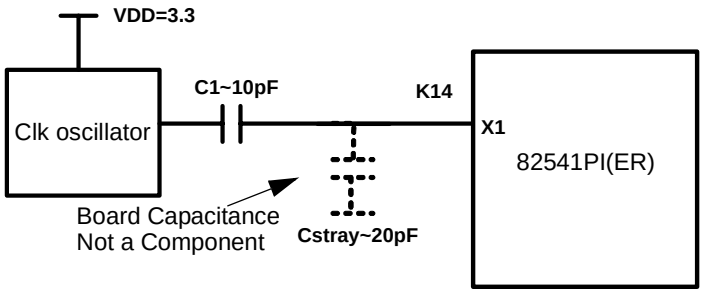
This solution involves capacitor C1, which forms a capacitor divider with C_{stray} of about 20 pF. This attenuates the input clock amplitude and adjusts the clock oscillator load capacitance.

$$V_{in} = VDD * (C1/(C1 + C_{stray}))$$
$$V_{in} = 3.3 * (C1/(C1 + C_{stray}))$$

This enables load clock oscillators of 15 pF to be used. If the value of C_{stray} is unknown, C1 should be adjusted by tuning the input clock amplitude to approximately 1 V_{ptp}. If C_{stray} equals 20 pF, then C1 is 10 pF ±10%.

A low capacitance, high impedance probe (C < 1 pF, R > 500 K Ω) should be used for testing. Probing the parameters can affect the measurement of the clock amplitude and cause errors in the adjustment. A test should also be done after the probe has been removed for circuit operation.

If jitter performance is poor, a lower jitter clock oscillator can be implemented.



3.6.10.2 Low Voltage Solution (VDD = 1.8 V)

The low voltage solution is similar to the high voltage solution. However, the low voltage includes a low consumption and low jitter clock oscillator that uses a 1.8 V external power supply. In this case, C1 will require adjusting according to the stray capacitance from X1.

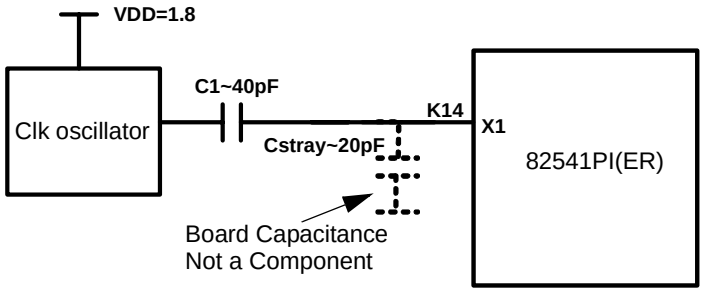


Table 17. 82541PI(ER) Recommended Oscillators

Manufacturer	Part Number
Raltron	CO4305-25.000-TR
Citizen America Corp	CSX750FBB25.000MTR

Note: This page intentionally left blank.

4.0 General Layout Considerations for Ethernet Controllers

Critical signal traces should be kept as short as possible to decrease the likelihood of being affected by high frequency noise from other signals, including noise carried on power and ground planes. Keeping the traces as short as possible can also reduce capacitive loading.

Since the transmission line medium extends onto the PCB, special attention must be paid to layout and routing of the differential signal pairs.

The differential signal pairs should not be routed near each other over long distances. Routing them too close to each other induces crosstalk and can also cause common mode noise that degrades the long cable receive bit error rate performance. To prevent these problems, separate the differential pairs from each other by at least 5 times the height from the GND plane (Figure 4). For example, separate them by 35 mils on a 7 mil thick prepreg.

Designing for Gigabit operation is very similar to designing for 10/100 Mbps. For the 82541PI(ER) controller, system level tests should be performed at all three speeds.

4.1 Guidelines for Component Placement

Component placement can affect signal quality, emissions, and component operating temperature This section provides guidelines for component placement.

Careful component placement can:

- Decrease potential problems directly related to EMI, which could cause failure to meet applicable government test specifications.
- Simplify the task of routing traces. To some extent, component orientation affects the complexity of trace routing. One overall objective is to minimize turns and crossovers between traces.

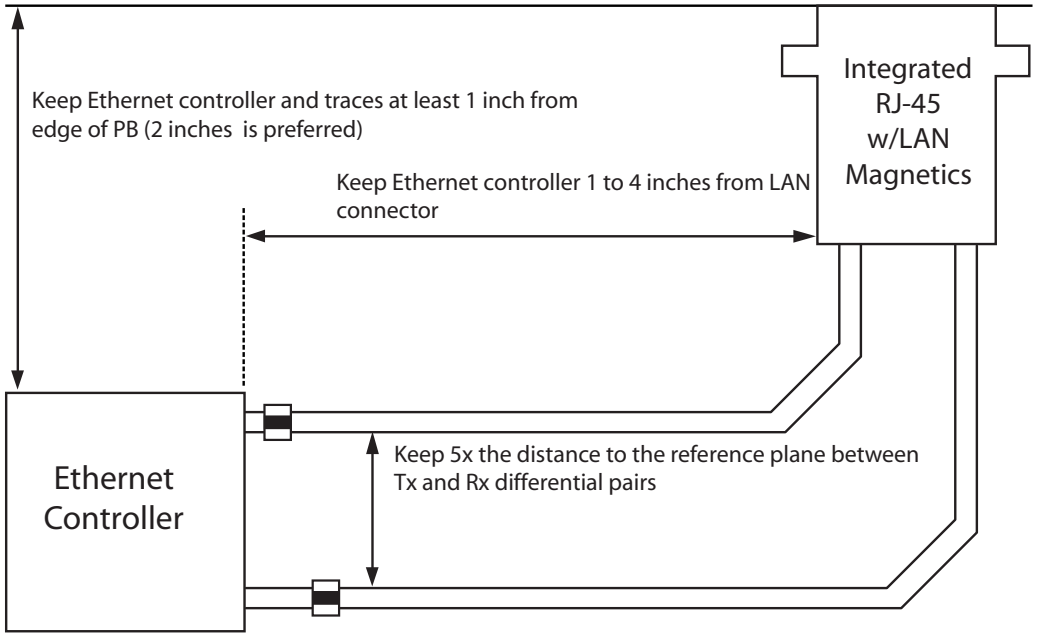
The following recommendations can be used as guidelines in the layout phase of the design implementation:

1. The Ethernet controller should be located at least one inch away from the RJ45 connector (distance D in Figure 5).
2. The Ethernet controller should be placed at least two inches from the PCB edge (distance E in Figure 5).

Minimizing the amount of space needed for the Ethernet LAN interface is important because other interfaces will compete for physical space on a LOM near the connector. The Ethernet LAN circuits need to be as close as possible to the connector.

Figure 4 shows some basic placement distance guidelines. Figure 4 also shows two differential pairs, but can be generalized for a Gigabit system with four differential pairs. The ideal placement for the Ethernet controller would be approximately one inch behind the magnetics module. Also note that the TX and RX termination resistors are located close to the Ethernet controller. This is vital for meeting IEEE physical layer conformance tests.

Figure 4. General Placement Distances



While it is generally a good idea to minimize lengths and distances, this figure also illustrates the need to keep the Ethernet controller away from the edge of the PCB and the magnetics module for best EMI performance.

4.1.1 Crystals

Crystals should not be placed near I/O ports or PCB edges. Radiation from these devices may be coupled onto the I/O ports or out of the system chassis. Crystals should also be kept away from the Ethernet magnetics module to prevent interference. Traces should be referenced to a continuous low impedance ground plane.

Place the crystal and its load capacitors on the PCBs as close to the LAN device as possible (within 0.75-inch). Keep other potentially noisy traces away from the crystal traces.

The restraining straps of the crystal should be grounded to reduce the possibility of radiation from the crystal's case. Crystals should lay flat against the PCB to provide better coupling of electromagnetic fields to the PCB.

4.1.2 Board Stackup Recommendations

PCBs for these designs typically have four, six, eight, or more layers. Following is a description of a typical four-layer board stackup:

- Layer 1 is a signal layer. It can contain the differential analog pairs from the Ethernet device to the magnetics module.
- Layer 2 is a signal ground layer. Chassis ground may also be fabricated in Layer 2 under the connector side of the magnetics module.

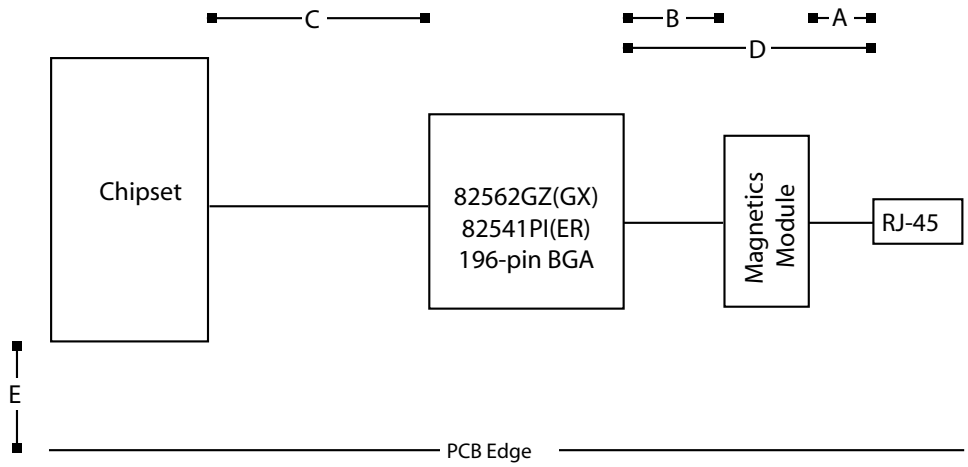
- Layer 3 is used for power planes.
- Layer 4 is a signal layer.

This board stackup configuration can be adjusted to conform to specific design rules.

4.2 Critical Dimensions for Discrete Magnetics Module and RJ-45

There are four critical dimensions that must be considered during the layout phase of an 82541PI(ER) and 82562GZ(GX) LOM implementation. These dimensions are identified in Figure 5 as A, B, C, and D.

Figure 5. Critical Dimensions for Component Placement (Discrete Magnetics Solution)



4.2.1 Distance A: Magnetics to RJ45 (Priority 1)

The distance labeled “A” in Figure 5 should be given the highest priority in board layout. The distance between the magnetics module and the RJ45 connector should be kept to less than one inch of separation. The following trace characteristics are important and should be observed:

- Differential Impedance. The differential impedance should be 100 Ω. The single ended trace impedance will be approximately 50 Ω; however, the differential impedance can also be affected by the spacing between the traces.
- Trace Symmetry. Differential pairs should be routed with consistent separation and with exactly the same lengths and physical dimensions (for example, width).

Caution: Asymmetrical and unequal length traces in the differential pairs contribute to common mode noise, which can degrade the receive circuit’s performance and contribute to radiated emissions from the transmit circuit.

If an Ethernet controller must be placed further than two inches from the RJ45 connector, distance “B” can be sacrificed. Keeping distance “A” as short as possible should be a priority.

4.2.2 Distance B: PHY to Magnetics (Priority 2)

Distance B in Figure 5 should also be designed to extend less than one inch between devices for the 82541PI(ER) and two inches between devices for the 82562GZ(GX). The high speed nature of the signals propagating through these traces requires that the distance between these components are closely observed. In general, any section of traces that is intended for use with high speed signals should observe proper termination practices. Proper termination of signals can reduce reflections caused by impedance mismatches between devices and traces.

The reflections of a signal may have a high frequency component that may contribute more EMI than the original signal itself. For this reason, these traces should be designed to a 100 Ω differential value.

4.2.3 Distance C: LAN Controller to Chipset (Priority 3)

The distance labeled “C” should be addressed separately between the 82541PI(ER) and the 82562GZ(GX).

4.2.3.1 LAN Connect Interface Distance for the 82562GZ(GX)

This section contains guidelines for LOM designs that comply with the LCI. These guidelines should not be treated as a specification; however, it must be ensured that the system meets specified timings. This can be verified through simulations or other techniques. The LCI can be routed to support a 10/100 Mbps LOM solution with 82562GZ(GX) devices.

Distance C, the LCI, should be less than 10 inches.

4.2.3.2 PCI Interface for the 82541PI(ER)

The PCI bus on 82541PI(ER) meets PCI 2.3 specification and operate as PCI slave devices for configuration and register programming. After the controllers have been properly initialized, they can also operate as PCI masters to fetch memory descriptors and to read/write data buffers.

The controllers are capable of operating in either a 5 V or 3.3 V signaling environment. The VIO terminals can be connected to either 3.3 V or 5 V to choose the appropriate PCI bus levels.These connections bias the controller PCI I/O buffers for the correct switching strength. However, all other digital inputs and outputs use 3.3 V signaling unless specified separately.

4.2.4 Distance D: The Overall Length of Differential Traces from LAN to RJ-45 (Priority 4)

The overall length of differential pairs should be less than four inches measured from the LAN controller to RJ-45 through the magnetics module.

The lengths of the differential traces (within each pair) should be equal within 50 mils (1.25 mm) and as symmetrical as possible.

4.2.5 Distance E: Ethernet Controller to PCB Edge

The Ethernet controller should be placed at least one inch from the PCB edge (two inches is preferred).

4.3 Critical Dimensions for an Integrated Magnetics Module

Figure 6 shows the critical dimensions for component placement with an integrated magnetics module.

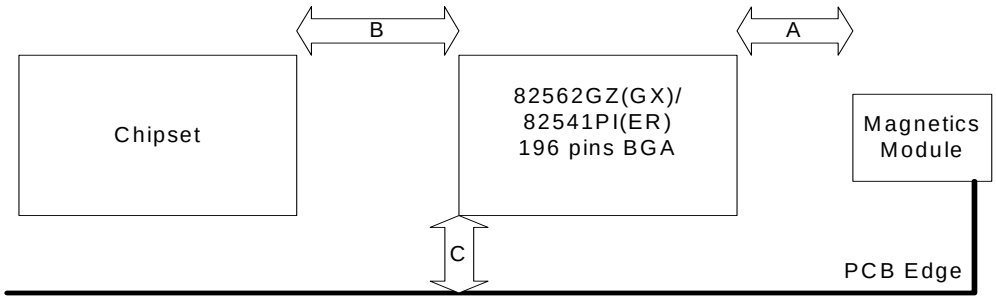


Figure 6. Critical Dimensions for 82562GZ(GX) and 82541PI(ER) Component Placement with Integrated Magnetics Module

4.3.1 Distance A: The Overall Length of Differential Traces

The overall length of differential pairs should be between one and four inches measured from the Ethernet controller to the RJ-45 connector having integrated magnetics (shortest lengths give the best performance.).

4.3.2 Distance B: Ethernet Controller to Chipset

For LCI on 82562GZ(GX) devices, the maximum length should be less than 10 inches on an ICH5, ICH6, or ICH7 platform. For the PCI bus on 82541PI(ER) controllers, the bus routing should meet PCI specifications.

4.3.3 Distance C: LAN Controller to PCB Edge

The Ethernet controller should be placed at least one inch from the PCB edge (two inches is preferred.).

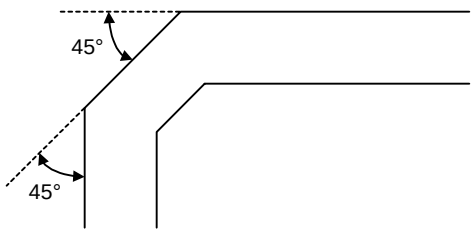
4.4 Differential Pair Trace Routing

Trace routing considerations are important to minimize the effects of crosstalk and propagation delays on sections of the PCB where high-speed signals exist. Signal traces should be kept as short as possible to decrease interference from other signals, including those propagated through power and ground planes.

Observe the following suggestions to help optimize board performance. Note that some suggestions are specific to a 4.3 mil stackup for the 82541ER:

- Maintain constant symmetry and spacing between the traces within a differential pair.
- Keep the signal trace lengths within a differential pair equal to each other.
  - For the 82541PI, do not use serpentines to try to match trace lengths in the differential pair. Serpentines cause impedance variations causing signal reflections, which can be a source of signal distortion. Try to keep the length difference of the differential pair less than 50 mil (~15 pS). Always go straight to the required via or pad.
- Keep the total length of each differential pair under four inches. Designs with differential traces longer than five inches are much more likely to have:
  - Degraded receive Bit Error Rate (BER) performance
  - IEEE PHY conformance failures
  - Excessive EMI radiation
- For the 82562GZ(GX), keep at least 5 times the distance to the reference plane between Tx and Rx differential pairs.
- For the 82541PI(ER), keep at least 5 times the distance to the reference plane between all four Tx and Rx differential pairs.
- For all Ethernet controllers, do not route any other signal traces parallel to the differential pairs closer than 5 times the distance to the reference plane.
- For the 82562GZ(GX) and the 82541ER, keep maximum separation within differential pairs to seven mils.
- For the 82541PI, separate traces within a differential pair as small as possible down to five to eight mils. Close separation of the traces allow them to couple well to each other.
- For high-speed signals, the number of corners and vias should be kept to a minimum. If a 90° bend is required, it is recommended to use two 45° bends instead. See Figure 7.

Figure 7. Corner Trace Routing



- For all Ethernet controllers, traces should be routed away from board edges by a distance greater than the trace height above the ground plane. This allows the field around the trace to couple more easily to the ground plane rather than to adjacent wires or boards.
- Do not route traces and vias under crystals or oscillators. This prevents coupling to or from the clock. And as a general rule, place traces from clocks and drives at a minimum distance from apertures by a distance that is greater than the largest aperture dimension.

- The reference plane for the differential pairs should be continuous and low impedance. It is recommended that the reference plane be ground (or 1.8 V, the voltage used by the 82541PI PHY). This provides an adequate return path for high frequency noise currents.
- Do not route differential pairs over splits in the associated reference plane.
- Differential termination components should be placed as close as possible to the LAN controller.

4.4.1 Signal Trace Geometry

The key factors in controlling trace EMI radiation are the trace length and the ratio of trace-width to trace-height above the ground plane. To minimize trace inductance, high-speed signals and signal layers that are close to a ground or power plane should be as short and wide as practical. Ideally, this trace width to height above the ground plane ratio is between 1:1 and 3:1. To maintain trace impedance, the width of the trace should be modified when changing from one board layer to another if the two layers are not equidistant from the power or ground plane.

Each pair of signals should have a differential impedance of 100 Ω +/- 20%. If a particular tool cannot correctly calculate or predict differential traces, it is permissible to specify 55 to 60 Ω single-ended traces as long as the spacing between the two traces is minimized. As an example, consider a differential trace pair on Layer 1 that is 8 mils (0.2 mm) wide and 2 mils (0.05 mm) thick, with a spacing of eight mils (0.2mm). If the fiberglass layer is 8 mils (0.2 mm) thick with a dielectric constant, E_R, of 4.7, the calculated single-ended impedance would be about 61 Ω and the calculated differential impedance would be approximately 100 Ω.

When performing a board layout, do not allow the CAD tool auto-router to route the differential pairs without intervention. In most cases, the differential pairs will have to be routed manually.

Components should be laid out in the following order of priority:

- Differential traces
- Termination resistors
- Bypass capacitors
- Other components

Note: Measured differential trace impedance for layout designs targeting 100 Ω often indicates lower actual impedance. Designers should verify actual trace impedance and adjust the layout accordingly. If the actual impedance is consistently low, a target of 105 – 110 Ω should compensate for second order effects.

It is necessary to compensate for trace-to-trace edge coupling, which can lower the differential impedance by up to 10 Ω, when the traces within a pair are closer than 30 mils (edge to edge).

Traces between decoupling and I/O filter capacitors should be as short and wide as practical. Long and thin traces are more inductive and would reduce the intended effect of decoupling capacitors. Also for similar reasons, traces to I/O signals and signal termination should be as short as possible. Vias to the decoupling capacitors should be sufficiently large in diameter to decrease series inductance. Additionally, the PLC should not be closer than one inch to the connector/magnetics/ edge of the board.

4.4.2 Impedance Discontinuities

Impedance discontinuities cause unwanted signal reflections. Avoid vias (signal through holes) and other transmission line irregularities. If vias must be used, a reasonable budget is two per differential trace. Unused pads and stub traces should also be avoided.

4.4.3 Reducing Circuit Inductance

Traces should be routed over a continuous ground plane with no interruptions. If there are vacant areas on a ground or power plane, the signal conductors should not cross the vacant area. This increases inductance and associated radiated noise levels. Noisy logic grounds should be separated from analog signal grounds to reduce coupling. Noisy logic grounds can sometimes affect sensitive DC subsystems such as analog to digital conversion, operational amplifiers, etc. All ground vias should be connected to every ground plane layer; similarly, every power via should be connected to all equal potential power plane layers. This helps reduce circuit inductance. Another recommendation is to physically locate grounds to minimize the loop area between a signal path and its return path. Rise and fall times should be as slow as permissible because signals with fast rise and fall times contain many high frequency harmonics, which can radiate significantly. The most sensitive signal returns closest to the chassis ground should be connected together. This results in a smaller loop area and reduce the likelihood of crosstalk. The effect of different configurations on the amount of crosstalk can be studied using electronics modeling software.

4.4.4 Signal Isolation

To maintain best signal integrity, keep digital signals far away from the analog traces. If digital signals on other PCB layers cannot be separated by a ground plane, they should be routed at right angles with respect to the differential pairs. If there is another LAN controller on the PCB, take care to keep the differential pairs from that circuit away.

Some rules to follow for signal isolation:

- Separate and group signals by function on separate layers if possible. Maintain a gap of 5 times the distance to the reference plane between all differential pairs (Ethernet) and other nets, but group associated differential pairs together.
- Isolate I/O signals from high-speed signals to minimize crosstalk, which can increase EMI emission and susceptibility to EMI from other signals.
- Avoid routing high-speed LAN traces near other high-frequency signals associated with a video controller, cache controller, processor, or other similar devices.

4.4.5 Power and Ground Planes

Good grounding requires minimizing inductance levels in the interconnections and keeping ground returns short, signal loop areas small, and power inputs bypassed to signal return, will significantly reduce EMI radiation.

The following guidelines help reduce circuit inductance in motherboards:

- Route traces over a continuous plane with no interruptions. Do not route over a split power or split ground plane. If there are vacant areas on a ground or power plane, avoid routing signals over the vacant area. This increases inductance and EMI radiation levels.
- Separate noisy digital grounds from analog grounds to reduce coupling. Noisy digital grounds can affect sensitive DC subsystems.
- All ground vias should be connected to every ground plane layer; similarly, every power via should be connected to all equal potential power plane layers. This helps reduce circuit inductance.
- Use vias in pairs. Two (or more) small vias have less inductance and are preferable over large vias. The small vias might also require less board space.
- Physically locate grounds between a signal path and its return. This minimizes the loop area.
- Avoid fast rise/fall times as much as possible. Signals with fast rise and fall times contain many high frequency harmonics, which can radiate EMI.
- If the magnetics module is a discrete module, the ground plane beneath the magnetics module should be split. The RJ45 connector side of the transformer module should have chassis ground beneath it (see Section 4.4.7).
- Power planes are not recommended as reference (or AC ground) planes for the differential since most of them are noisy and can contaminate signals.

4.4.6 Traces for Decoupling Capacitors

Traces between decoupling and I/O filter capacitors should be as short and wide as practical. Long and narrow traces are more inductive and would reduce the intended effect of decoupling capacitors. Also for similar reasons, traces to I/O signals and signal terminations should be as short as possible. Vias to the decoupling capacitors should be sufficiently large in diameter to decrease series inductance.

4.4.7 Ground Planes Under a Discrete Magnetics Module

The magnetics module's chassis or output ground (secondary side of transformer) should be separated from the digital or input ground (primary side) by a physical separation of 100 mils minimum. Splitting the ground planes beneath the transformer minimizes noise coupling between the primary and secondary sides of the transformer and between the adjacent coils in the magnetics. This arrangement also improves the common mode choke functionality of magnetics module.

Figure 8 illustrates the split plane layout for a discrete magnetics module. Capacitors are used to interconnect chassis ground and signal ground.

Figure 8. Ground Plane Separation

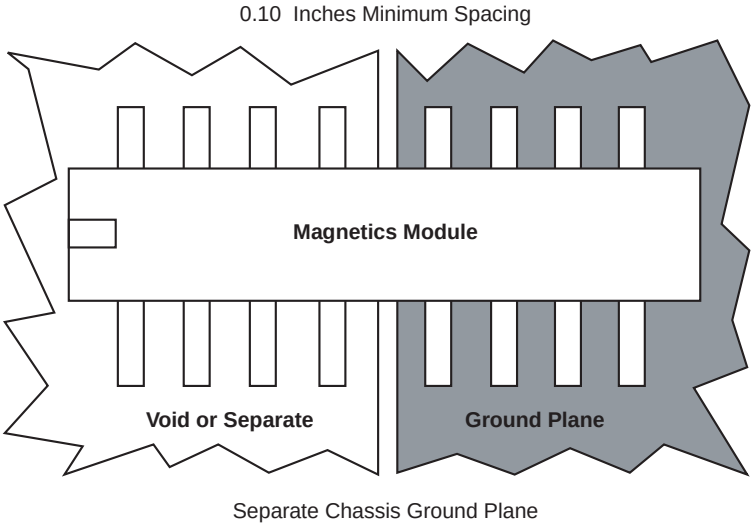
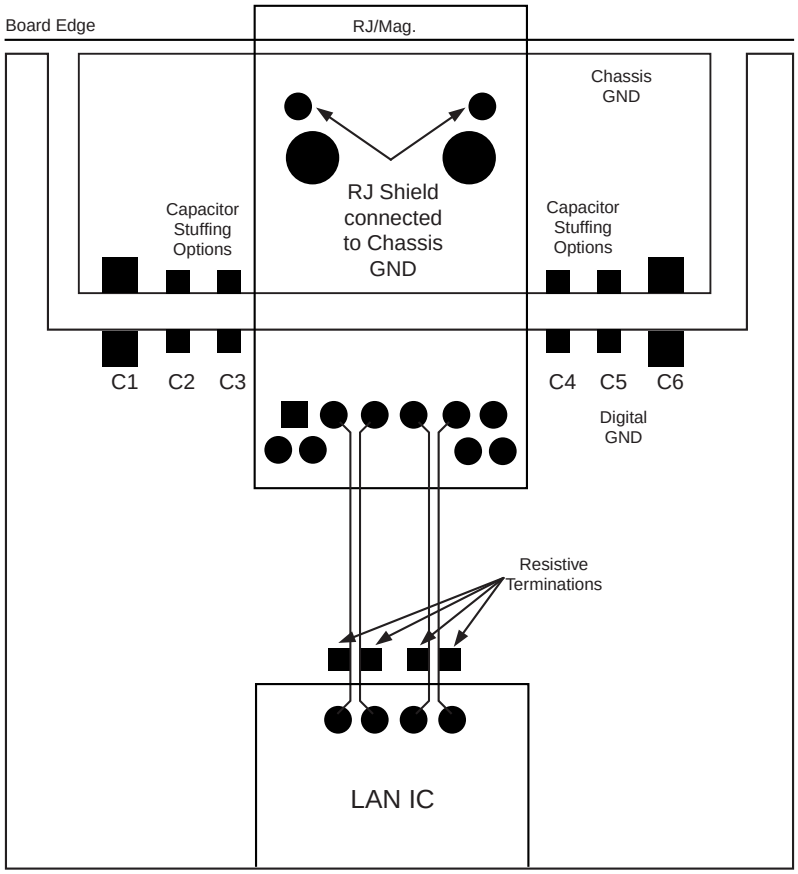


Figure 9 shows the preferred method for implementing a ground split under an integrated magnetics module/RJ-45 connector without USB. The capacitor stuffing options (C1-C6) are used to reduce/filter high frequency emissions. The value(s) of the capacitor stuffing options may be different for each PCB. Experiments need to be performed to determine which value(s) provide best EMI performance. Integrated RJ-45 discrete magnetics with USB usually do not have split planes under them.

Figure 9. Ideal Ground Split Implementation (for Integrated RJ-45 without USB)



The table below gives some starting values for these capacitors.

Capacitors	Value
C1, C6	4.7µF or 10 µF
C2, C3, C4, C5,	470 pF to 0.1 µF

The placement of C1 – C6 may also be different for each PCB design. For example, all capacitors might not need to be populated). Also, the capacitors may not be needed on both sides of the magnetic module.

Systems with integrated USB ports on the magnetics module might have difficulty using a chassis ground configuration due to the need to get DC ground to certain USB pins. One technique is to fabricate an incomplete ground split (partially open on one end). By connecting the ground planes around the RJ magnetics module through a slim, high impedance connection, the path of the high frequency noise can be controlled.

4.4.8 Non-Integrated Magnetics Modules/RJ-45 Connectors

It is possible to employ discrete (non-integrated) magnetics modules and RJ-45 connectors. Similar rules apply to design and layout. The differential pairs should be routed to be as short and symmetrical as possible and the overall lengths of the differential pairs (including the width of the magnetics module) should not exceed approximately four inches.

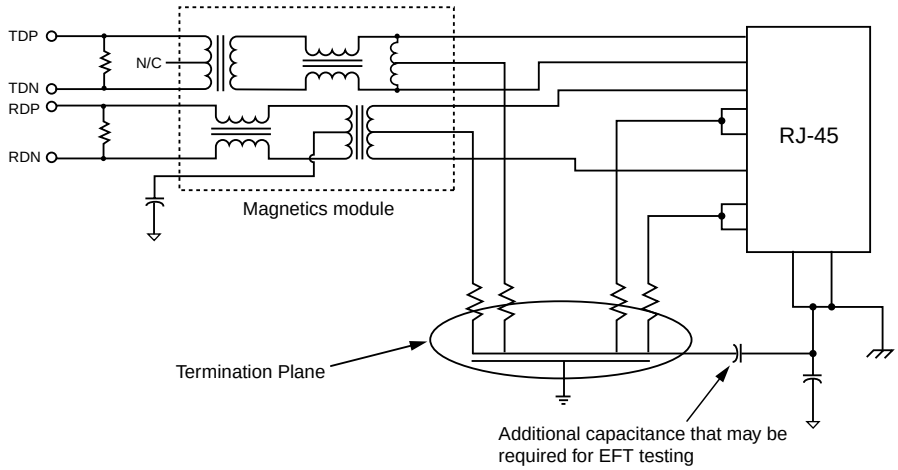
Additional design and layout steps are required to add a dedicated board termination plane parallel to chassis ground, 75 Ω termination resistors, and a 1500 pF capacitor. This “Bob Smith” termination scheme is normally contained inside an integrated magnetics module.

For the 82541PI, the 75 termination resistors are required to terminate the common mode of the twisted pairs that behave as a transmission line. These resistors help ensure that emissiion requirements are met.

In Ethernet designs, it is common practice to terminate unused connections on the RJ-45 connector and the magnetics module to ground. Depending on overall shielding and grounding design, this may be done to the chassis ground, signal ground, or a termination plane. Care must be taken when using various grounding methods to insure that emission requirements are met. In the “Bob Smith” termination method, a floating termination plane is cut out of a power plane layer. This floating plane acts as a plate of a capacitor with an adjacent ground plane. The signals can be routed through 75 Ω resistors to the plane. Stray energy on unused pins is then carried to the plane.

It is recommended that the termination plane capacitance equal a minimum value of 1500 pF. This helps reduce the amount of crosstalk on the differential pairs from the unused pairs of the RJ-45 connector. Pads may be placed for an additional capacitance to chassis ground, which may be required if the termination plane capacitance is not large enough to pass Electrical Fast Transient (EFT) testing. If a discrete capacitor is used, to meet the EFT requirements it should be rated for at least 1000 Vac.

Figure 10. Termination Plane Example for 82562GZ/GX PLC Device and Discrete Magnetics



4.4.9 82562GZ(GX) Layout Guidelines (Routing LAN 3.3 V When Using a Copper Trace)

When 3.3 V for the LAN device is NOT supplied by a solid copper power plane, then it becomes more important to make sure the power source will not carry system noise to the LAN device, and to ensure that the power trace does not restrict current flow to the LAN device.

4.4.9.1 Avoid Restricting Current Flow

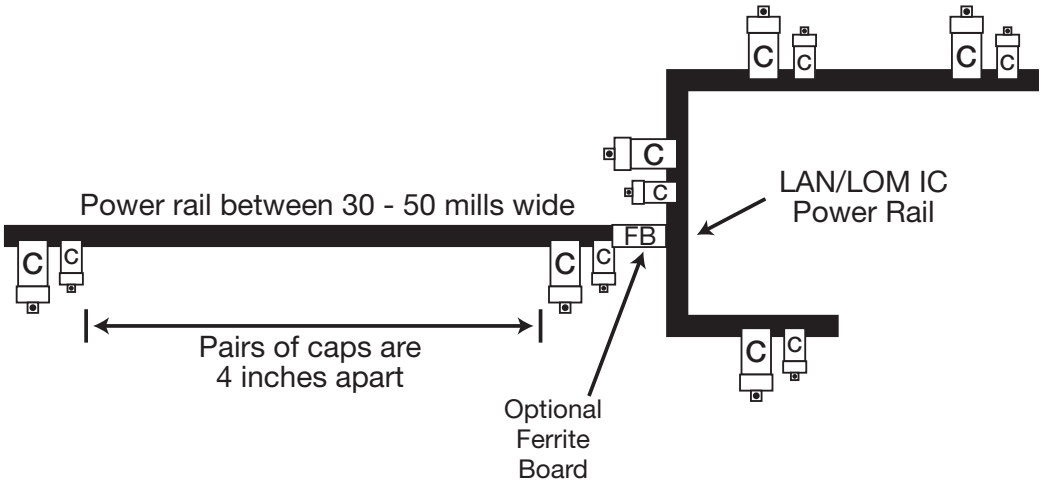
When a 3.3 V power trace is used to supply power to the LAN device, the power trace should be at least 50 mils wide, to avoid restricting current flowing to the LAN device. On designs where there is enough PCB space, a power trace that is 200 mils wide or wider, is better.

4.4.9.2 Power Trace Decoupling

If a power trace is more than an inch long, it should be decoupled at both the source and near the destination.

Extremely long power traces should be decoupled every three to five inches. Placing a decoupling cap on the power trace, once every few inches, greatly reduces the amount of noise that will reach the LAN device. In-turn, this reduces radiated emissions, and improves IEEE PHY conformance.

Figure 11. Decoupled LAN Power Trace (Power Supplied by Trace)

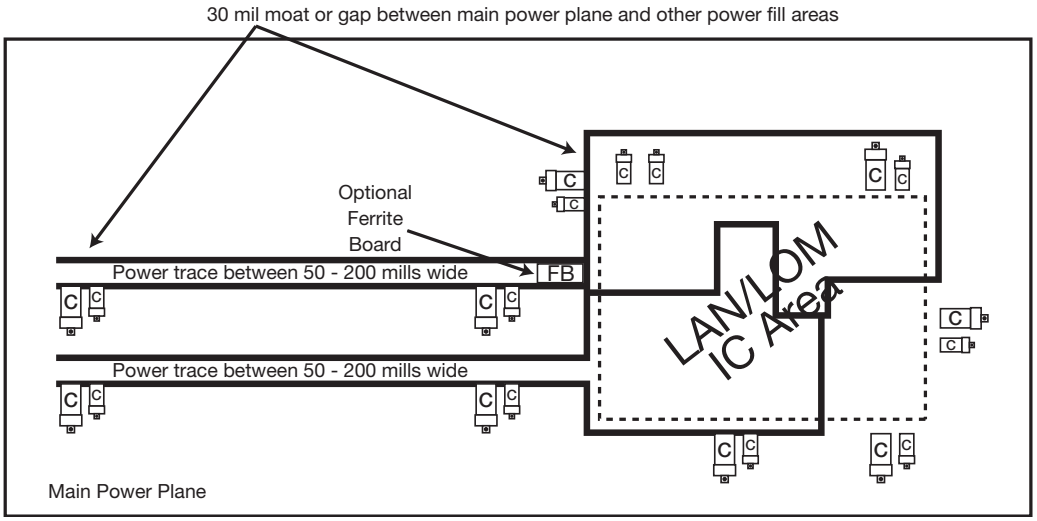


1. Big C >= 4.7 uF. Little c = 0.1 uF (or 0.01 uF).
2. Noise above 500 MHz might require a COG cap between 470 pF and 1000 pF.
3. To reduce noise in the LAN device and on the wire; If a power trace is more than an inch long, it should be decoupled both at source and near destination. Also, a series Ferrite Bead near the destination can help.

4.4.9.3 Moat (a Space) Around LAN Power Trace, to Reduce Noise From Adjacent Signals

To further reduce power supply noise, it is desirable to keep the LAN power trace or LAN power fill separated from other signals and other voltage rails, by 30 mils, if possible. Separating power traces and power-fills with 20 to 30 mil wide moats reduce signal and power noise from coupling onto the LAN power trace or onto the LAN power-fill.

Figure 12. Using a Moat to Reduce Noise From Adjacent Traces and Power Fills



4.5 82562GZ(GX) Signal Terminations

Two differential pairs are terminated using 54.9 Ω (1% tolerance) resistors, placed near the LAN controller. One resistor connects to the MDI+ (MDI positive) signal trace and another resistor connects to the MDI- (MDI negative) signal trace.

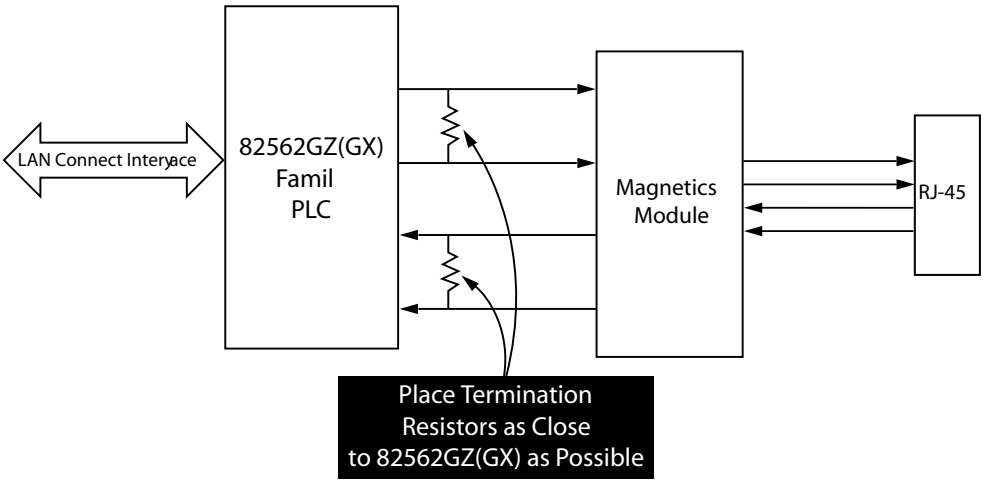
Termination resistor values were recently increased from 49.9 Ω to 54.9 Ω to improve return loss. However, on some designs, this change caused the PCB's output amplitude to be slightly above the peak-to-peak center of the IEEE specification. As a result, RBIAS resistor values were increased (RBIAS10 549 to 619 Ω and RBIAS100 619 to 649 Ω) to reduce the PCB's output amplitude to better meet the IEEE peak-to-peak center specification.

For 100Base-TX designs, the IEEE specification allows a -950 mVpk to -1050 mVpk for the negative peak and +950 mVpk to +1050 mVpk for the positive peak. Ideally, a typical PCB output amplitude should be within -975 mVpk to -1025 mVpk for the negative peak and +975 mVpk to +1025 mVpk for the positive peak.

For 10Base-T designs, the IEEE specification allows a -2.2 mVpk to -2.8 mVpk for the negative peak and +2.2 mVpk to +2.8 mVpk for the positive peak. Ideally, a typical PCB output amplitude should be within -2.35 mVpk to -2.55 mVpk for the negative peak and +2.35 mVpk to +2.55 mVpk for the positive peak.

The RBIAS values previously listed should be considered starting values. Intel recommends that board designers measure each of their PCB's output amplitude and then adjust the RBIAS values as required.

Figure 13. Termination Resistors Placement (Integrated Magnetics Solution)



4.5.1 Termination Plane

Resistors are used to terminate noise from the unused inputs of both the RJ45 connector and the magnetics module to the termination plane. The netname “termplane” is provided as a guide to the termination plane. A termplane is a plane fabricated into the PCB substrate. This plane, which has no DC termination, acts like one-half of a capacitor that provides a path for the coupled noise.

4.5.2 Termination Plane Capacitance

It is recommended that the termination plane capacitance equal a minimum value of 1500 pF. This helps reduce the amount of crosstalk on the differential pairs (TDP and TDN and RDP and RDN) from the unused pairs of the RJ45. Pads may be placed for additional capacitance, which may be required if failure occurs during electrical fast transient testing.

Note: This capacitor must be designed to tolerate 2 KV voltage injections to meet International Special Committee on Radio Interference (CISPR) Electrostatic Discharge (ESD) specifications.

4.6 Light Emitting Diodes for Designs Based on 82562GZ(GX) PLC

The 82562GZ(GX) PLC device has three high-current outputs to directly drive LEDs for link, activity and speed indication. Since LEDs are likely to be integral to a magnetics module, take care to route the LED traces away from potential sources of EMI noise. In some cases, it may be desirable to attach filter capacitors.

4.7 82541PI(ER) Signal Terminations

The four differential pairs are terminated with 49.9 Ω (1% tolerance) resistors, placed near the 82541PI(ER) controller. One resistor connects to the MDI+ (MDI positive) signal trace and another resistor connects to the MDI- (MDI negative) signal trace. The opposite ends of the resistors, using a wide trace, connect together and to ground through a single 0.1 µF capacitor. The capacitor should be placed as close as possible to the 49.9 Ω resistors using a wide trace.

Do not vary the suggested component values. Be sure to lay out symmetrical pads and traces for these components such that the length and symmetry of the differential pairs are not disturbed.

4.8 Light Emitting Diodes for Designs Based on 82541PI(ER)

The 82541PI(ER) controller provides four programmable high-current outputs to directly drive LEDs for link activity and speed indication. Since the LEDs are likely to be integral to a magnetics module, route the LED traces away from potential sources of EMI noise. In some cases, it may be desirable to attach filter capacitors.

4.9 Schematic for EEPROM Footprints and LCI Connection

There are two options for EEPROM footprints. OEMs can choose either a common EEPROM footprint for the 82541PI(ER), 82562GZ(GX), and ICHx or an independent EEPROM footprint for each LAN controller.

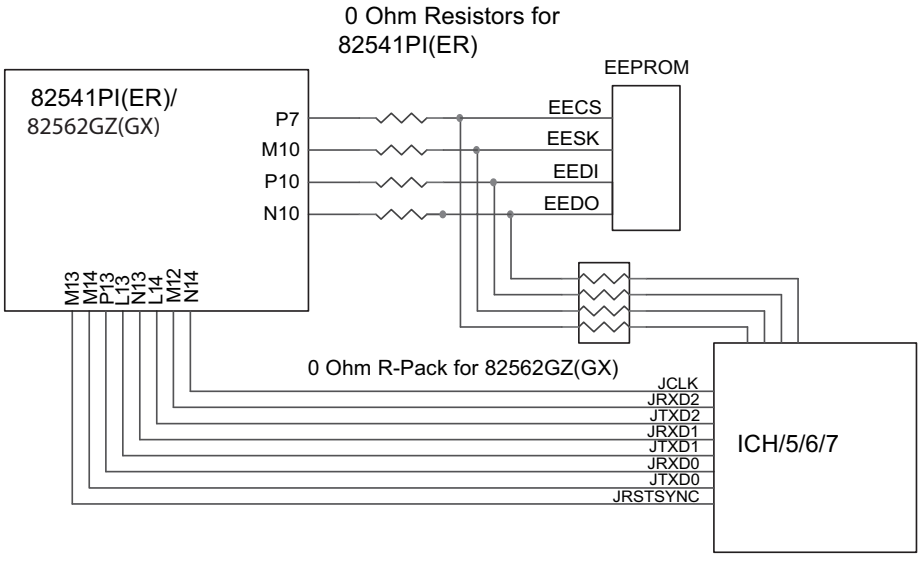


Figure 14. Common EEPROM Footprint for Both 82541PI(ER) and 82562GZ(GX)

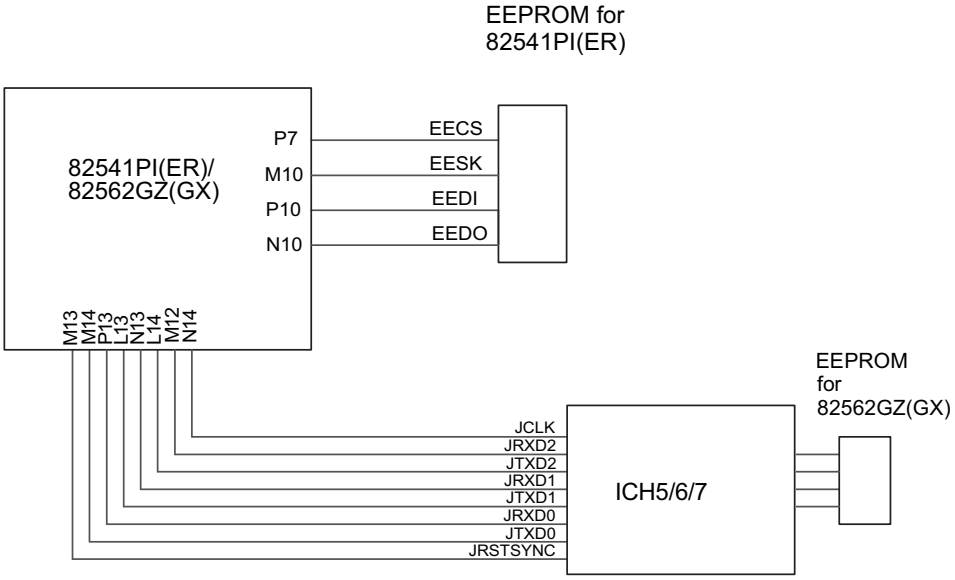


Figure 15. Independent EEPROM Footprints for Individual LAN Controllers

4.10 Termination of Unused Differential Signals on Gigabit Magnetics for 10/100 LOM Design

Since the number of differential signals are different between a 10/100 LAN controller and a gigabit LAN controller, the two major problems confronted in designing the dual footprint LOM design are:

1. Choosing the pin compatible magnetics modules for both 10/100 and gigabit controller.
2. Terminating unused differential signals for gigabit between the selected magnetics module and RJ-45 connector when a 10/100 LAN design is implemented.

The three sections that follow provide the remedies for this issue.

4.10.1 Option 1: Board Level Stuffing

1. Layout resistor footprints on the pairs three and four of the differential traces for 82541PI(ER) LOM design. Refer to Figure 16.
2. Possibly rework the magnetics module for 10/100 to be footprint compatible with the magnetics for gigabit.

3. Replace the magnetics for the 82541PI(ER) with the one for the 82562GZ(GX) and then populate R1/R2 and R3/R4 for an 82562GZ(GX) LOM design. Refer to Figure 17.

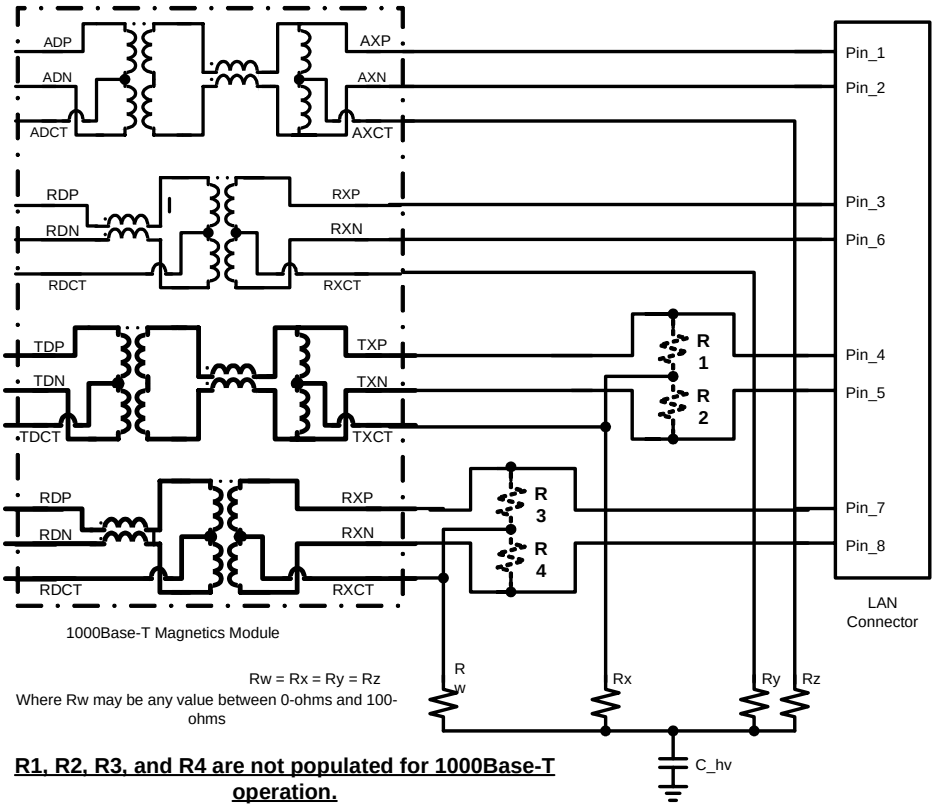


Figure 16. Typical Magnetics for Gigabit LAN Controller with Optional Resistors Footprint

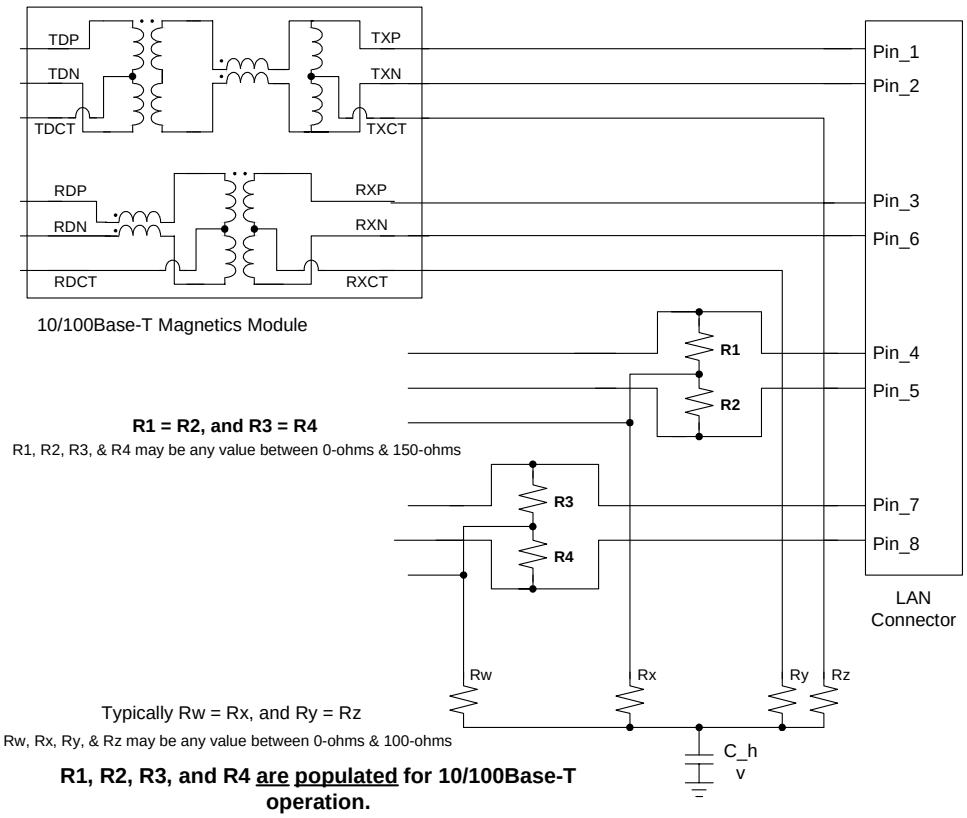


Figure 17. Replacement of Magnetics for 10/100 LAN Controller with Optional Resistors Populated

4.10.2 Option 2: Rework of Gigabit Magnetics[1]

Option two is a rework of a gigabit magnetics component with an internal jumper for 10/100 Mbps design.

In order to make a common footprint on differential pairs between the magnetics and RJ-45 connector for both 10/100 and gigabit LOM design, one of the approaches is to rework the magnetics module for gigabit controller with internal jumpers to short pair three and four of differential signals. OEMs need to work with their magnetics vendors for this option.

1. Intel is working with some magnetics vendors to standardize the pinout assignments on magnetics modules.

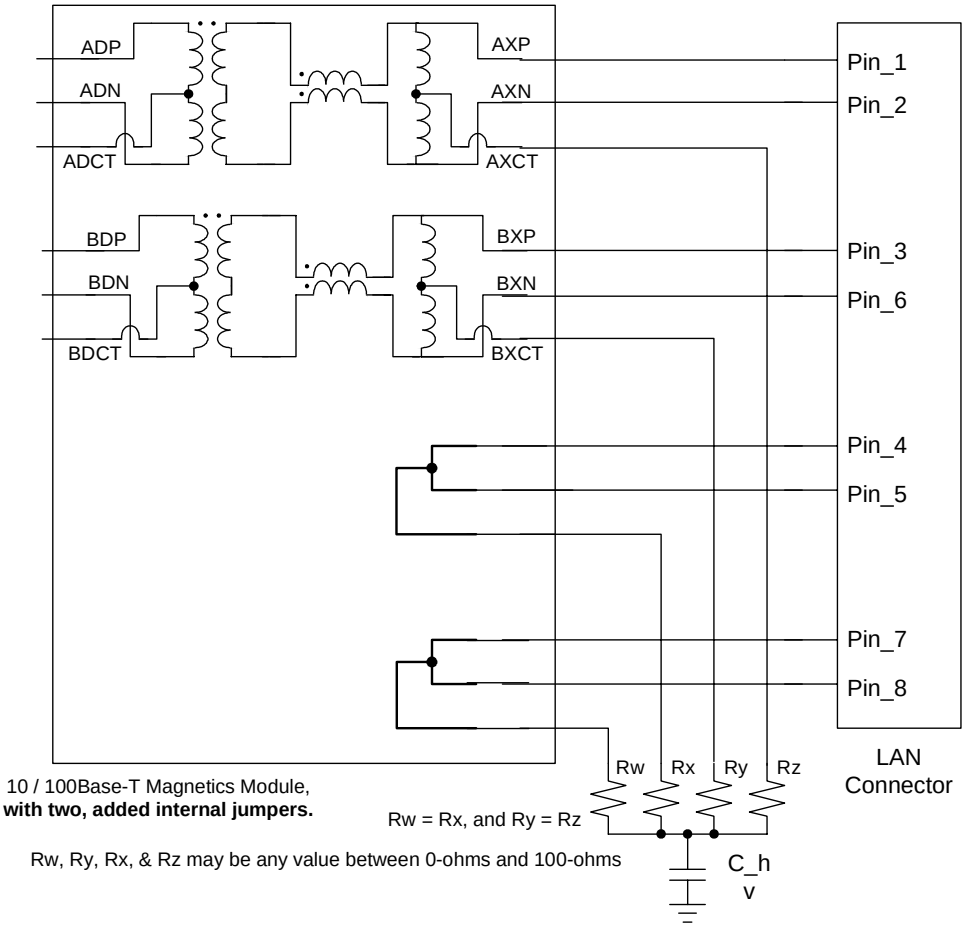


Figure 18. Rework of Gigabit Magnetics with Shorted Pair Three and Four on Differential Traces for 10/100 LOM Design

4.10.3 Option 3: Integrated Magnetics Module for 10/100 Mbps and Gigabit

Refer to Table 13.

4.11 Physical Layer Conformance Testing

Physical layer conformance testing (also known as IEEE testing) is a fundamental capability for all companies with Ethernet LAN products. PHY testing is the final determination that a layout has been performed successfully. If your company does not have the resources and equipment to perform these tests, consider contracting the tests to an outside facility.

Crucial tests are as follows, listed in priority order:

1. Bit Error Rate (BER). This test is a good indicator of real world network performance. It should be done with long and short cables and many link partners. The test limit is 10 to 11 errors (10/100/1000 Mbps).
2. Output Amplitude, Rise and Fall Time (10/100 Mbps), Symmetry and Droop (1000 Mbps). For the 82541PI(ER) controller, use the appropriate PHY test waveform.
3. Return Loss. This test indicates proper impedance matching, measured through the RJ-45 connector back toward the magnetics module.
4. Jitter Test (10/100 Mbps) or Unfiltered Jitter Test (1000 Mbps). This test indicates clock recovery ability (master and slave for Gigabit controller).
5. Harmonic Content for 10 Mbps.
6. Output Symmetry for 100/1000 Mbps.
7. Rise and Fall Time for 100 Mbps.
8. Droop for 1000 Mbps.
9. Duty Cycle Distortion for 100 Mbps.

4.12 Troubleshooting Common Physical Layout Issues

The following is a list of common physical layer design and layout mistakes in LOM designs.

1. Unequal length of the two traces within a differential pair. Inequalities create common-mode noise and will distort the transmit or receive waveforms.
2. Lack of symmetry between the two traces within a differential pair. Asymmetry can create common-mode noise and distort the waveforms. For each component or via that one trace encounters, the other trace should encounter the same component or a via at the same distance from the Ethernet controller.
3. Excessive distance between the LAN controller and the magnetics. Long traces on FR4 fiberglass epoxy substrate will attenuate and distort the analog signals. In addition, any impedance mismatch in the traces will be aggravated if they are longer than the four inch rule.
4. Routing any other trace parallel to and close to one of the differential traces. Crosstalk getting onto the receive channel will cause degraded long cable BER. Crosstalk getting onto the transmit channel can cause excessive EMI emissions and can cause poor transmit BER on long cables. At a minimum, other signals should be kept 0.1 inch from the differential traces.
5. Routing one pair of differential traces too close to another pair of differential traces. After exiting the LAN controller, the trace pairs should be kept 0.1 inch or more away from the other trace pairs. The only possible exceptions are in the vicinities where the traces enter or exit the magnetics, the RJ-45 connector, and the LAN controller.
6. Using a low quality magnetics module.
7. Re-use of an out-of-date physical layer schematic in a LAN controller design. The terminations and decoupling can be different from one PHY to another.
8. Incorrect differential trace impedances. It is important to have approximately 100 Ω impedance between the two traces within a differential pair. This becomes even more important as the differential traces become longer. To calculate differential impedance, many impedance calculators only multiply the single-ended impedance by two. This does not take into account edge to edge capacitive coupling between the two traces or other edge effects. When the two traces within a differential pair are kept close to each other, the edge coupling can lower the effective differential impedance by 5 Ω to 20 Ω. Short traces will have fewer problems if the differential impedance is slightly off target.
9. For 82562GZ(GX) PLC designs, use of capacitor that is too large between the transmit traces or too much capacitance on the magnetics module's transmit center tap to ground. Using capacitors more than a few picoFarads in either of these locations can slow the 100 Mbps rise and fall time. This will also cause return loss to fail at higher frequencies and will degrade the transmit BER performance. If capacitors are used, the total of all capacitors placed on the transmit traces and the center tap should equal less than 22 pF.

5.0 Pin Number to Signal Mapping with Population Options

Table 18 lists the pin names for the three controllers and the corresponding shared ball reference value. Note that the 82541PI(ER) pin name in the 82541PI(ER) Datasheet/Design Guide is slightly different from the signal name on the reference schematics. The Datasheet/Design Guide signal names maintain consistency with the 64-bit gigabit controller naming conventions, while the schematic names follow the conventions used by our engineers on their design tools.

Table 18. Ball Number to Signal Mapping (Sheet 1 of 8)

				Population Options			
Ball Ref	**82541ER Pin Name**	**82541PI Pin Name**	**82562GZ(GX) Pin Name**	**82541ER**	**82541PI**	**82562GZ(GX)**	**Comments**
A1	NC	NC	NC				
A2	SERR#	SERR#	NC	SERR#	SERR#	No stuff	
A3	VCC	3.3 V	VCC	3.3 V		3.3 V	
A4	IDSEL	IDSEL	NC	IDSEL	IDSEL	No stuff	
A5	AD[25]	AD[25]	NC	AD[25]	AD[25]	No stuff	
A6	NC	PME#	NC	No stuff	PME#	No stuff	
A7	VCC	3.3 V	VCC	3.3 V		3.3 V	
A8	AD[30]	AD[30]	NC	AD[30]	AD[30]	No stuff	
A9	LAN_PWR_GOOD	LAN_PWR_ GOOD	NC	Supervisor IC	Supervisor IC	No stuff	
A10	VCC	SMBCLK	NC	3.3 V	SMBCLK		
A11	VCC	3.3 V	VCC	3.3 V	3.3 V	3.3 V	VCCT = 3.3 V
A12	LINK_LED#	LED0/ LINK_UP#	LILED#	LINK_LED#	LINK_LED#	LINK_LED#	Same signal - different names.
A13	TEST	TEST	TESTEN	Pull-down	Pull-down	Pull-down	May have LAN Disable logic connected to this signal for 82562GZ(GX). An external 200 Ω pull-up resistor is also required for the 82562GZ(GX).
A14	NC	NC	NC				
B1	AD[22]	AD[22]	NC	AD[22]	AD[22]	No stuff	
B2	AD[23]	AD[23]	NC	AD[23]	AD[23]	No stuff	
B3	VSS	VSS	VSS				
B4	AD[24]	AD[24]	NC	AD[24]	AD[24]	No stuff	
B5	AD[26]	AD[26]	NC	AD[26]	AD[26]	No stuff	
B6	AD[27]	AD[27]	NC	AD[27]	AD[27]	No stuff	
B7	VSS	VSS	VSS				
B8	AD[31]	AD[31]	NC	AD[31]	AD[31]	No stuff	
B9	RST#	RST#	NC	RST#	RST#	No stuff	

Table 18. Ball Number to Signal Mapping (Sheet 2 of 8)

				Population Options			
Ball Ref	**82541ER Pin Name**	**82541PI Pin Name**	**82562GZ(GX) Pin Name**	**82541ER**	**82541PI**	**82562GZ(GX)**	**Comments**
B10	VCC	SMB_ALERT# LAN_PWR_ GOOD	NC	3.3 V	SMB_ALERT#		
B11	LINK100#	LED2/ LINK100#	SPDLED#	LED	LED	LED	Same signal - different names.
B12	LINK1000#	LED3/ LINK1000#	TOUT	LED	LED	No stuff	Testability output for 82562GZ(GX).
B13	CTRL18	CTRL18	RBIAS100	Pwr Regulator	Pwr Regulator	649 pull-down	Connect to PNP or to pull-down.
B14	IEEE_TEST+	IEEE_TEST+	RBIAS10	NC	NC	619 pull-down	Install resistor or not.
C1	AD[21]	AD[21]	NC	AD[21]	AD[21]	No stuff	
C2	M66EN	M66EN	NC	M66EN	M66EN	No stuff	
C3	REQ#	REQ#	NC	REQ#	REQ#	No stuff	
C4	C/BE#[3]	C/BE#[3]	NC	C/BE#[3]	C/BE#[3]	No stuff	
C5	NC	RSVD_NC	NC		NC		
C6	AD[28]	AD[28]	NC	AD[28]	AD28	No stuff	
C7	AD[29]	AD[29]	NC	AD[29]	AD29	No stuff	
C8	NC	CLK_RUN#	NC	NC	CLK_RUN#	No stuff	
C9	VCC	SMBDATA	NC	3.3 V	SMBDATA		
C10	VSS	VSS	VSS				
C11	ACTIVITY#	LED1/ ACTIVITY#	ACTLED#	LED	LED	LED	Same signal - different names.
C12	AVSS	AVSS	VSS	VSS	VSS	VSS	AVSS = VREF = VSS
C13	MDI[0+]	MDI[0+]	TDP	MDI	MDI	MDI	Same signal - different names.
C14	MDI[0-]	MDI[0-]	TDN	MDI	MDI	MDI	Same signal - different names.
D1	AD[18]	AD[18]	NC	AD[18]	AD[18]	No stuff	
D2	AD[19]	AD[19]	NC	AD[19]	AD[19]	No stuff	
D3	AD[20]	AD[20]	NC	AD[20]	AD[20]	No stuff	
D4	VSS	RSVD_VSS	VSS		VSS		
D5	VSS	VSS	VSS				
D6	VSS	VSS	VSS				
D7	VSS	VSS	VSS				
D8	VSS	VSS	VSS				
D9	NC	NC	NC		1.8 V		

Table 18. Ball Number to Signal Mapping (Sheet 3 of 8)

				Population Options			
Ball Ref	**82541ER Pin Name**	**82541PI Pin Name**	**82562GZ(GX) Pin Name**	**82541ER**	**82541PI**	**82562GZ(GX)**	**Comments**
D10	NC	NC	ISOL_EXEC	NC	NC	NC	May have LAN Disable logic connected to this signal for 82562GZ(GX). Has an internal 10 K Ω pull-down resistor for the 82562GZ(GX).
D11	ANALOG_1.8 V	ANALOG_ 1.8V	NC	1.8 V	1.8 V	No stuff	PHY Power Plane
D12	CLKR_1.8 V	CLKR_1.8 V	ISOL_TI	1.8 V	1.8 V	No stuff	May have LAN Disable logic connected to this signal for 82562GZ(GX). Has an internal 10 K Ω pull-down resistor for the 82562GZ(GX).
D13	AVSS	AVSS	VSS	VSS	VSS	VSS	AVSS = VSS
D14	IEEE_TEST-	IEEE_TEST-	ISOL_TCK	2-pin header	2-pin header	NC	May have LAN Disable logic connected to this signal for 82562GZ(GX). Has an internal 10 K Ω pull-down resistor for the 82562GZ(GX).
E1	VCC	3.3 V	VCC	3.3 V		3.3 V	
E2	VSS	VSS	VSS				
E3	AD[17]	AD[17]	NC	AD[17]	AD[17]	No stuff	
E4	VSS	RSVD_VSS	VSS				
E5	VSS	VSS	VSS				
E6	VSS	VSS	VSS				
E7	VSS	VSS	VSS				
E8	VSS	VSS	VSS				
E9	VSS	VSS	VSS				
E10	VSS	VSS	VSS				
E11	ANALOG_1.2 V	ANALOG_ 1.2 V	VCCT	1.2 V	1.2 V	3.3 V	Core Power Plane
E12	ANALOG_1.2 V	ANALOG_1.2 V	VCCT	1.2 V	1.2 V	3.3 V	Core Power Plane
E13	MDI[1]+	MDI[1]+	RDP	MDI	MDI	MDI	Same signal - different names.
E14	MDI[1]-	MDI[1]-	RDN	MDI	MDI	MDI	Same signal - different names.
F1	IRDY#	IRDY#	NC	IRDY#	IRDY#	No stuff	
F2	FRAME#	FRAME#	NC	FRAME#	FRAME#	No stuff	
F3	C/BE#[2]	C/BE#[2]	NC	C/BE#[2]	C/BE#[2]	No stuff	

Table 18. Ball Number to Signal Mapping (Sheet 4 of 8)

				Population Options			
Ball Ref	**82541ER Pin Name**	**82541PI Pin Name**	**82562GZ(GX) Pin Name**	**82541ER**	**82541PI**	**82562GZ(GX)**	**Comments**
F4	VSS	VSS	VSS		VSS		
F5	VSS	VSS	VSS		VSS		
F6	VSS	VSS	VSS				
F7	VSS	VSS	VSS				
F8	VSS	VSS	VSS				
F9	VSS	VSS	VSS				
F10	VSS	VSS	VSS				
F11	AVSS	AVSS	VSS	VSS	VSS	VSS	AVSS = VSS
F12	NC	NC	NC	NC	NC	NC	
F13	MDI[2]+	MDI[2]+	NC	Magnetics	Magnetics	Magnetics	10/100 Magnetics will not have a pin connected here
F14	MDI[2]-	MDI[2]-	NC	Magnetics	Magnetics	Magnetics	10/100 Magnetics will not have a pin connected here
G1	CLK	CLK	NC	CLK	CLK	No stuff	
G2	VIO	VIO	NC	VIO	VIO	VIO	
G3	TRDY#	TRDY#	NC	TRDY#	TRDY#	No stuff	
G4	PLL_1.2 V	PLL_1.2 V	NC	1.2 V	1.2 V	NC	
G5	1.2 V	1.2 V	VCCR	1.2 V	1.2 V	3.3 V	Core Power Plane
G6	1.2 V	1.2 V	VCC	1.2 V	1.2 V	3.3 V	Core Power Plane
G7	VSS	VSS	VSS				
G8	VSS	VSS	VSS				
G9	VSS	VSS	VSS				
G10	VSS	VSS	VSS				
G11	AVSS	AVSS	VSS	VSS	VSS	VSS	AVSS = VSS
G12	ANALOG_1.8 V	ANALOG_ 1.8 V	NC	1.8 V	1.8 V	No stuff	PHY Power Plane
G13	ANALOG_1.2 V	ANALOG_ 1.2 V	3.3 V	1.2 V	1.2 V	3.3 V	Core Power Plane
G14	AVSS	AVSS	VSS		VSS		AVSS = VSS = VSSPL
H1	STOP#	STOP#	NC	STOP#	STOP#	No stuff	
H2	INTA#	INTA#	NC	INTA#	INTA#	No stuff	
H3	DEVSEL#	DEVSEL#	NC	DEVSEL#	DEVSEL#	No stuff	
H4	PLL_1.2 V	PLL_1.2 V	NC	1.2 V	1.2 V	No stuff	
H5	1.2 V	1.2 V	VCCR	1.2 V	1.2 V	3.3 V	Core Power Plane
H6	1.2 V	1.2 V	3.3 V	1.2 V	1.2 V	3.3 V	Core Power Plane

Table 18. Ball Number to Signal Mapping (Sheet 5 of 8)

				Population Options			
Ball Ref	**82541ER Pin Name**	**82541PI Pin Name**	**82562GZ(GX) Pin Name**	**82541ER**	**82541PI**	**82562GZ(GX)**	**Comments**
H7	1.2 V	1.2 V	3.3 V	1.2 V	1.2 V	3.3 V	Core Power Plane
H8	1.2 V	1.2 V	3.3 V	1.2 V	1.2 V	3.3 V	Core Power Plane
H9	VSS	VSS	VSS				
H10	VSS	VSS	VSS				
H11	ANALOG_1.2 V	ANALOG_ 1.2 V	3.3 V	1.2 V	1.2 V	3.3 V	Core Power Plane
H12	NC	NC	NC	NC	NC	NC	
H13	MDI[3]+	MDI[3]+	NC	Magnetics	Magnetics	Magnetics	10/100 Magnetics will not have a pin connected here
H14	MDI[3]-	MDI[3]-	NC	Magnetics	Magnetics	Magnetics	10/100 Magnetics will not have a pin connected here
J1	PAR	PAR	NC	PAR	PAR	No stuff	
J2	PERR#	PERR#	NC	PERR#	PERR#	No stuff	
J3	GNT#	GNT#	NC	GNT#	GNT#	No stuff	
J4	EEMODE	EEMODE	NC	Pull-down or NC	Pull-down or NC	NC	82541ER: Connect a pull-down for Microwire and a NC for SPI
J5	1.2 V	1.2 V	VCCR	1.2 V	1.2 V	3.3 V	Core Power Plane
J6	1.2 V	1.2 V	3.3 V	1.2 V	1.2 V	3.3 V	Core Power Plane
J7	1.2 V	1.2 V	3.3 V	1.2 V	1.2 V	3.3 V	Core Power Plane
J8	1.2 V	1.2 V	3.3 V	1.2 V	1.2 V	3.3 V	Core Power Plane
J9	1.2 V	1.2 V	3.3 V	1.2 V	1.2 V	3.3 V	Core Power Plane
J10	1.2 V	1.2 V	3.3 V	1.2 V	1.2 V	3.3 V	Core Power Plane
J11	1.2 V	1.2 V	3.3 V	1.2 V	1.2 V	3.3 V	Core Power Plane
J12	AUX_PWR	AUX_PWR	NC	AUX_PWR	AUX_PWR	No stuff	
J13	XTAL_1.8 V	XTAL_1.8 V	NC	1.8 V	1.8 V	No stuff	PHY Power Plane
J14	XTAL2	XTAL2	X2				
K1	AD[16]	AD[16]	NC	AD[16]	AD[16]	No stuff	
K2	VSS	VSS	VSS				VSSPP = VSS
K3	VCC	3.3 V	VCC	3.3 V		3.3 V	
K4	VCC	3.3 V	VCC	3.3 V		3.3 V	
K5	1.2 V	1.2 V	3.3 V	1.2 V	1.2 V	3.3 V	Core Power Plane

Table 18. Ball Number to Signal Mapping (Sheet 6 of 8)

				Population Options			
Ball Ref	**82541ER Pin Name**	**82541PI Pin Name**	**82562GZ(GX) Pin Name**	**82541ER**	**82541PI**	**82562GZ(GX)**	**Comments**
K6	1.2 V	1.2 V	3.3 V	1.2 V	1.2 V	3.3 V	Core Power Plane
K7	1.2 V	1.2 V	3.3 V	1.2 V	1.2 V	3.3 V	Core Power Plane
K8	1.2 V	1.2 V	3.3 V	1.2 V	1.2 V	3.3 V	Core Power Plane
K9	1.2 V	1.2 V	3.3 V	1.2 V	1.2 V	3.3 V	Core Power Plane
K10	1.2 V	1.2 V	3.3 V	1.2 V	1.2 V	3.3 V	Core Power Plane
K11	1.2 V	1.2 V	3.3 V	1.2 V	1.2 V	3.3 V	Core Power Plane
K12	AVSS	AVSS	VSS	VSS	VSS	VSS	AVSS = VSSPL =VSS
K13	VCC	3.3 V	VCC	3.3 V	3.3 V	3.3 V	
K14	XTAL1	XTAL1	X1				
L1	AD[14]	AD[14]	NC	AD[14]	AD[14]	No stuff	
L2	AD[15]	AD[15]	NC	AD[15]	AD[15]	No stuff	
L3	C/BE#[1]	C/BE#[1]	NC	C/BE#[1]	C/BE#[1]	No stuff	
L4	1.2 V	1.2 V	3.3 V	1.2 V	1.2 V	3.3 V	Core Power Plane
L5	1.2 V	1.2 V	3.3 V	1.2 V	1.2 V	3.3 V	Core Power Plane
L6	VSS	VSS	VSS		VSS		
L7	NC	RSVD_NC	ADV10/ LAN_DISABLE#	NC	NC	NC	An internal 10 K Ω pull-down resistor is required for the 82562GZ(GX).
L8	NC	NC	NC	NC	1.8 V	No stuff	PHY Power Plane
L9	1.2 V	1.2 V	3.3 V	1.2 V	1.2 V	3.3 V	Core Power Plane
L10	1.2 V	1.2 V	3.3 V	1.2 V	1.2 V	3.3 V	Core Power Plane
L11	VSS	VSS	VSS		VSS		
L12	JTAG_TMS	JTAG_TMS	NC	NC	NC	NC	
L13	JTAG_TRST#	JTAG_TRST#	JTXD[1]	LCI	LCI	LCI	ICH drives this signal low. TRST needs to be grounded to disable JTAG. JTAG becomes difficult to use.
L14	JTAG_TCK	JTAG_TCK	JTXD[2]	LCI	LCI	LCI	ICH drives this signal low. TCK needs to be biased. JTAG becomes difficult to use.
M1	AD[11]	AD[11]	NC	AD[11]	AD[11]	No stuff	
M2	AD[12]	AD[12]	NC	AD[12]	AD[12]	No stuff	

Table 18. Ball Number to Signal Mapping (Sheet 7 of 8)

				Population Options			
Ball Ref	**82541ER Pin Name**	**82541PI Pin Name**	**82562GZ(GX) Pin Name**	**82541ER**	**82541PI**	**82562GZ(GX)**	**Comments**
M3	AD[13]	AD[13]	NC	AD[13]	AD[13]	No stuff	
M4	C/BE#[0]	C/BE#[0]	NC	C/BE#[0]	C/BE#[0]	No stuff	
M5	AD[5]	AD[5]	NC	AD[5]	AD[5]	No stuff	
M6	VSS	VSS	VSS				
M7	AD[1]	AD[1]	NC	AD[1]	AD[1]	No stuff	
M8	NC	RSVD_NC	NC	NC	NC	NC	
M9	FLSH_CE#	FLSH_CE#	NC	NC	NC	NC	
M10	EESK	EESK	NC	EESK	EESK	EESK	
M11	FLSH_SI	FLSH_SI	NC	NC	NC	NC	
M12	SDP[3]	SDP[3]	JRXD[2]	LCI	LCI	LCI	ICH expects this signal to be high or undriven.
M13	JTAG_TDI	JTAG_TDI	JRSTSYNC	LCI	LCI	LCI	ICH expects this signal to be high or undriven. JTAG becomes difficult to use.
M14	JTAG_TDO	JTAG_TDO	JTXD[0]	LCI	LCI	LCI	ICH expects this signal to be high or undriven. JTAG becomes difficult to use.
N1	VSS	VSS	VSS				VSSPP = VSS
N2	AD[10]	AD[10]	NC	AD[10]	AD[10]	No stuff	
N3	AD[9]	AD[9]	NC	AD[9]	A[D9]	No stuff	
N4	AD[7]	AD[7]	NC	AD[7]	AD[7]	No stuff	
N5	AD[4]	AD[4]	NC	AD[4]	AD[4]	No stuff	
N6	VCC	3.3 V	VCC	3.3 V	3.3 V	3.3 V	
N7	AD[0]	AD[0]	NC	AD[0]	AD[0]	No stuff	
N8	VCC	3.3 V	VCC	3.3 V	3.3 V	3.3 V	
N9	FLSH_SCK	FLSH_SCK	NC	NC	NC	NC	
N10	EEDO	EEDO	NC	EEDO	EEDO	EEDO	If desired, this can be shorted to the ICH EEDI b/c it is an input in ICH in reset.
N11	NC	RSVD_NC	NC	NC	NC	NC	
N12	VSS	VSS	VSSP	VSS	VSS	VSS	VSSP = VSSPL = VSS
N13	SDP[2]	SDP[2]	JRXD[1]	LCI	LCI	LCI	ICH expects this signal to be high or undriven.
N14	SDP[0]	SDP[0]	JCLK	LCI	LCI	LCI	ICH expects this signal to be low or undriven.
P1	NC	NC	NC				
P2	VCC	3.3 V	VCC	3.3 V		3.3 V	
P3	AD[8]	AD[8]	NC	AD[8]	AD[8]	No stuff	

Table 18. Ball Number to Signal Mapping (Sheet 8 of 8)

				Population Options			
Ball Ref	**82541ER Pin Name**	**82541PI Pin Name**	**82562GZ(GX) Pin Name**	**82541ER**	**82541PI**	**82562GZ(GX)**	**Comments**
P4	AD[6]	AD[6]	NC	AD[6]	AD[6]	No stuff	
P5	AD[3]	AD[3]	NC	AD[3]	AD[3]	No stuff	
P6	AD[2]	AD[2]	NC	AD[2]	AD[2]	No stuff	
P7	EECS	EECS	NC	EECS	EECS	EECS	
P8	VSS	VSS	VSS	VSS	VSS	VSS	VSSPL = VSS
P9	FLSH_SO	FLSH_SO/ LAN_ DISABLE#	NC	LAN_EN	LAN_EN	LAN_EN	Connect to LAN Enable signal
P10	EEDI	EEDI	NC	EEDI	EEDI	EEDI	If desired, this can be shorted to the ICH EEDI because it is an input in ICH in reset.
P11	CTRL12	CTRL12	NC	Pwr Regulator	Pwr Regulator	No stuff	Connect to PNP. Don't' stuff PNP on 82562GZ(GX).
P12	VCC	3.3 V	VCC	3.3 V	3.3 V	3.3 V	
P13	SDP[1]	SDP[1]	JRXD[0]	LCI	LCI	LCI	ICH expects this signal to be high or undriven.
P14	NC	NC	NC	NC	NC	NC	

6.0 Self-Review Checklist for Combined Footprint LOM

A Portable Data Format (PDF) Self-Review Checklist for a Combined Footprint LOM is available to aid designers via:

http://developer.intel.com

Note: This page intentionally left blank.

7.0 Reference Schematics

Following are reference schematics for the 82541PI/ER and 82562GX/EX (Mode 0 and 1).

REVISIONS		
REV	DESCRIPTION	DATE

82541PI/ER or 82562GZ(GX) LAN Controller Reference Design

(82562GZ(GX)/EZ(EX Mode 0)

Note: GZ/EZ and GX/EX are interchangable

A = Install component if using 82541PI/ER

B = Install component if using 82562GZ/GX

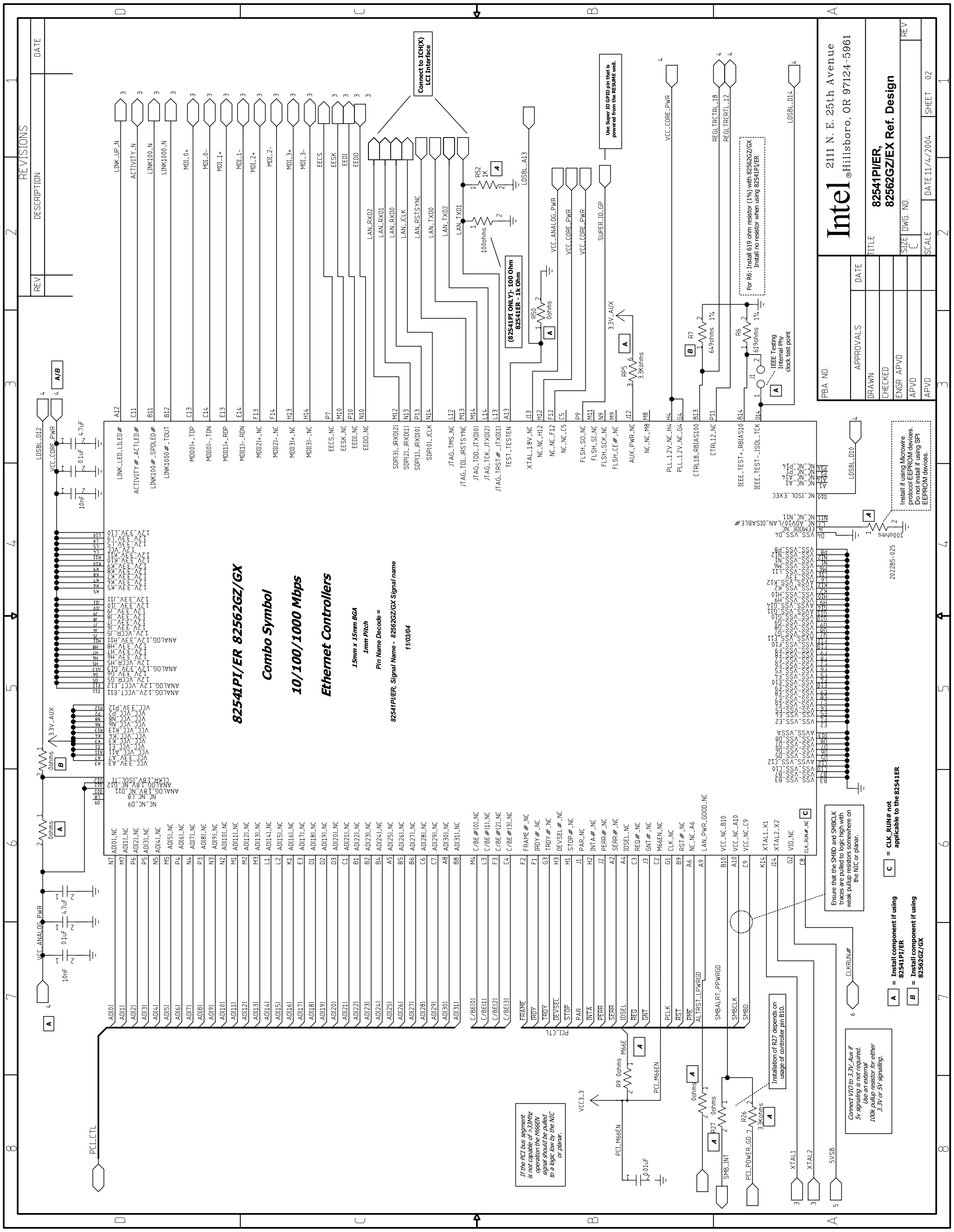
*** All components without flags are to be installed when using any selection of controllers.**

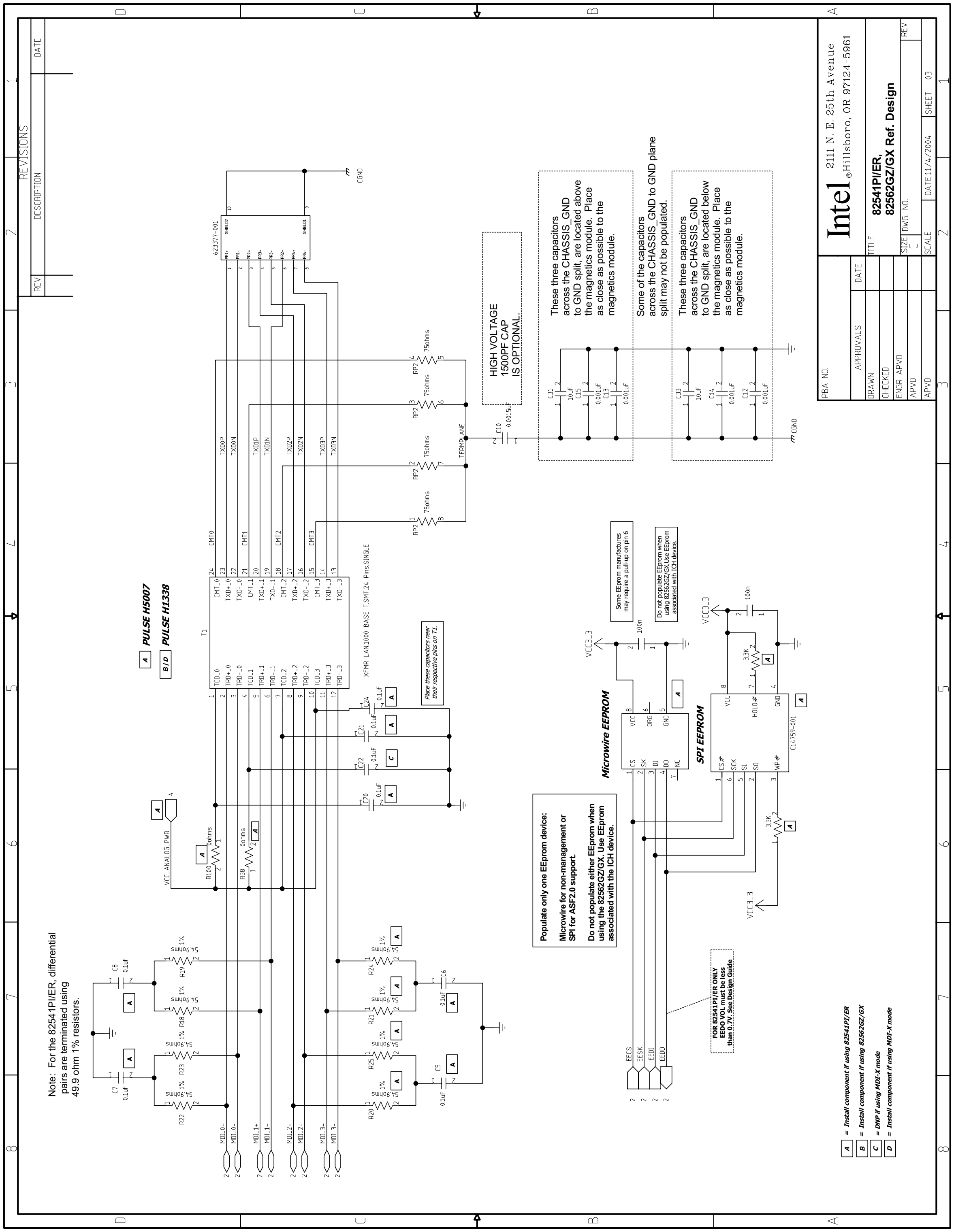
15mm x 15mm BGA

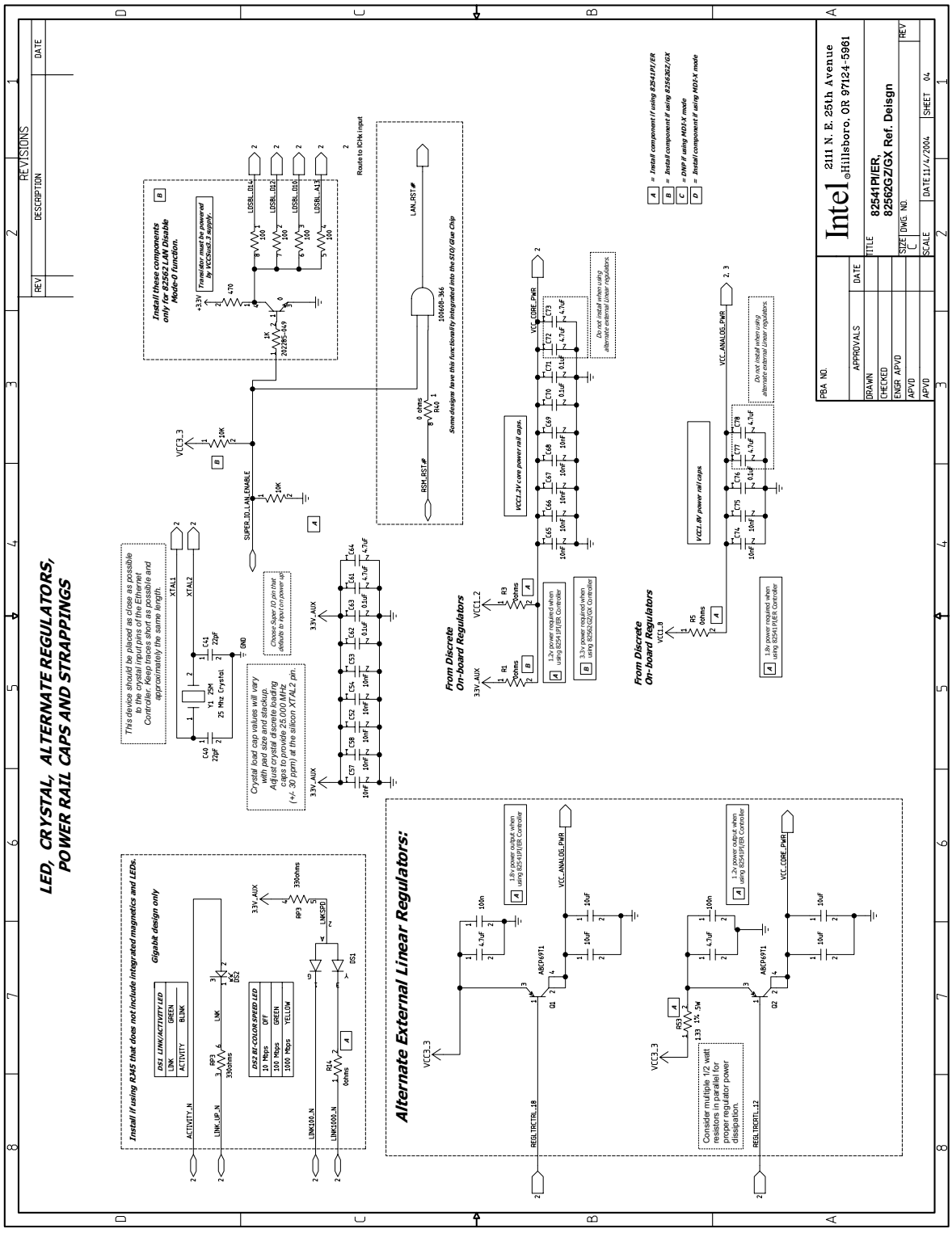
1mm pitch

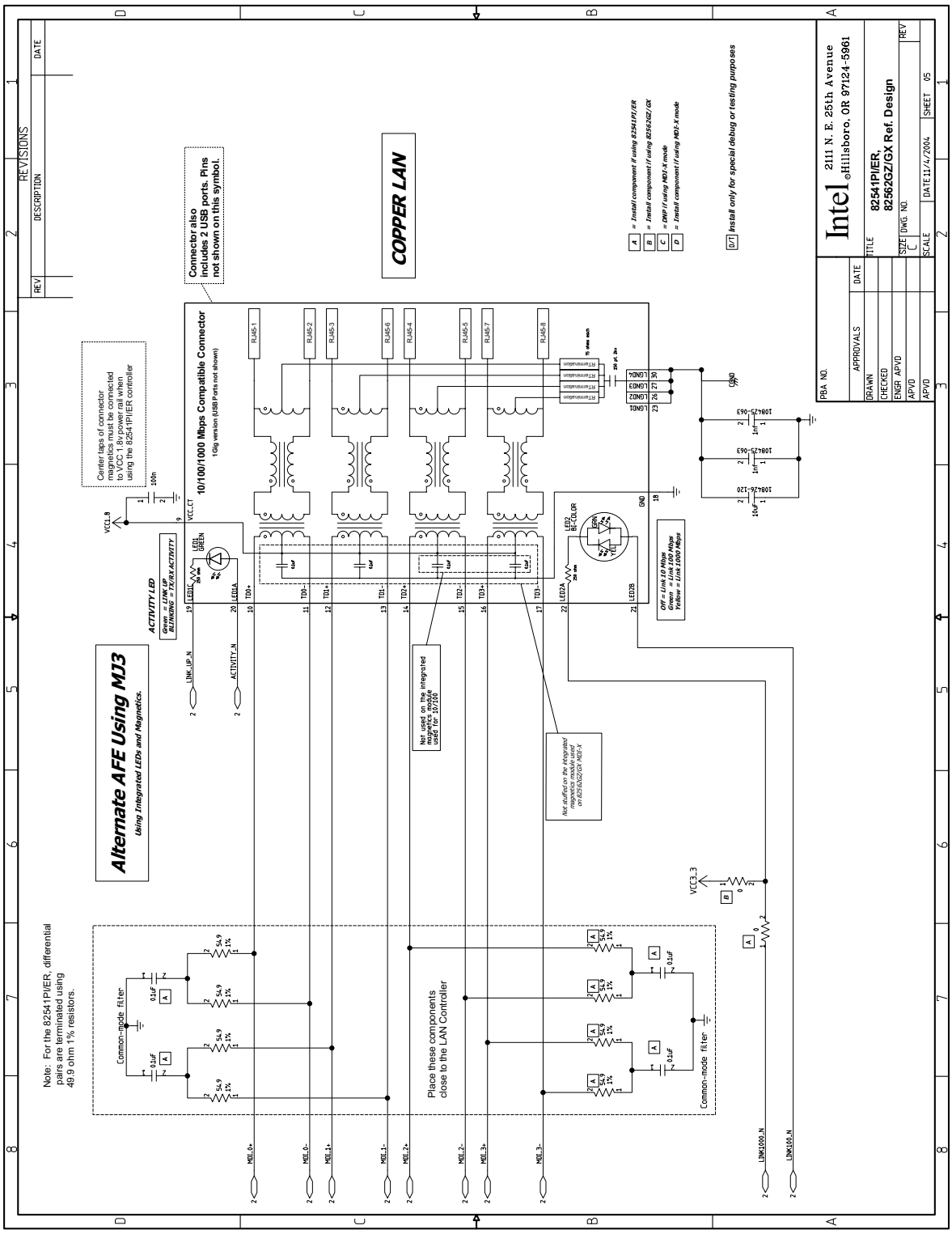
PAGE 2: COMBO 82541PI/ER AND 82562GX EHTERNET CONTROLLER SYMBOL
PAGE 3: 10/100/1000 PHY INTERFACE AND EEPROMS.
PAGE 4: LEDS, CRYSTAL, CAPS AND ALTERNATE REGULATORS.
PAGE 5: ALTERNATE AFE WITH INTEGRATED RJ45 CONN.

PBA NO.		Intel 2111 N. E. 25th Avenue ©Hillsboro, OR 97124-5961		
APPROVALS	DATE	TITLE	82541PI/ER, 82562GZ/GX Ref. Design	
DRAWN		SIZE C	DWG. NO.	REV
CHECKED		SCALE	DATE 11/4/2004	SHEET 01
ENGR APVD				
APVD				
APVD				


82541PI/ER 82562GZ/GX
Combo Symbol
10/100/1000 Mbps
Ethernet Controllers
2111 N. E. 25th Avenue
Hillsboro, OR 97124-5961
82541PI/ER,
82562GZ/EX Ref. Design
REVISIONS


Note: For the 82541PI/ER, differential pairs are terminated using 49.9 ohm 1% resistors.
PULSE H5007
PULSE H1338
XFMR LAN1000 BASE T,SMT,24 Pins,SINGLE
Place these capacitors near their respective pins on T1.
HIGH VOLTAGE 1500PF CAP IS OPTIONAL.
These three capacitors across the CHASSIS_GND to GND split, are located above the magnetics module. Place as close as possible to the magnetics module.
Some of the capacitors across the CHASSIS_GND to GND plane split may not be populated.
These three capacitors across the CHASSIS_GND to GND split, are located below the magnetics module. Place as close as possible to the magnetics module.
Populate only one EEprom device:
Microwire for non-management or SPI for ASF2.0 support.
Do not populate either EEprom when using the 82562GZ/GX. Use EEprom associated with the ICH device.
Microwire EEPROM
SPI EEPROM
Some EEprom manufactures may require a pull-up on pin 6
Do not populate EEprom when using 82562GZ/GX.Use EEprom associated with ICH device.
FOR 82541PI/ER ONLY EEDO VOL must be less than 0.7V. See Design Guide.
A = Install component if using 82541PI/ER
B = Install component if using 82562GZ/GX
C = DNP if using MDI-X mode
D = Install component if using MDI-X mode
2111 N. E. 25th Avenue
Hillsboro, OR 97124-5961
82541PI/ER, 82562GZ/GX Ref. Design
DATE 11/4/2004
SHEET 03


LED, CRYSTAL, ALTERNATE REGULATORS, POWER RAIL CAPS AND STRAPPINGS
Alternate External Linear Regulators:
From Discrete On-board Regulators
Intel 2111 N. E. 25th Avenue Hillsboro, OR 97124-5961
82541PI/ER, 82562GZ/GX Ref. Deisgn


Alternate AFE Using MJ3
Using Integrated LEDs and Magnetics.
COPPER LAN
10/100/1000 Mbps Compatible Connector
1Gig version (USB Ports not shown)
Connector also includes 2 USB ports. Pins not shown on this symbol.
Center taps of connector magnetics must be connected to VCC 1.8v power rail when using the 82541PI/ER controller
ACTIVITY LED
Green = LINK UP
BLINKING = TX/RX ACTIVITY
LED1 GREEN
LED2 BI-COLOR
Off = Link 10 Mbps
Green = Link 100 Mbps
Yellow = Link 1000 Mbps
Not used on the integrated magnetics module used for 10/100
Not stuffed on the integrated magnetics module used on 82562GX/GZ MDI-X
Place these components close to the LAN Controller
Common-mode filter
Note: For the 82541PI/ER, differential pairs are terminated using 49.9 ohm 1% resistors.
A = Install component if using 82541PI/ER
B = Install component if using 82562GZ/GX
C = GND if using MDI-X mode
D = Install component if using MDI-X mode
D/T Install only for special debug or testing purposes
PBA NO.
APPROVALS
DRAWN
CHECKED
ENGR APVD
APVD
APVD
DATE
Intel 2111 N. E. 25th Avenue Hillsboro, OR 97124-5961
TITLE
82541PI/ER, 82562GZ/GX Ref. Design
SIZE C
DWG. NO.
REV
SCALE
DATE 11/4/2004
SHEET 05
REVISIONS
REV
DESCRIPTION
DATE

REVISIONS		
REV	DESCRIPTION	DATE

82541PI/ER or 82562GZ(GX) LAN Controller Reference Design

(82562GZ(GX)/EZ(EX Mode 1)

Note: GZ/EZ and GX/EX are interchangable

A = Install component if using 82541PI/ER

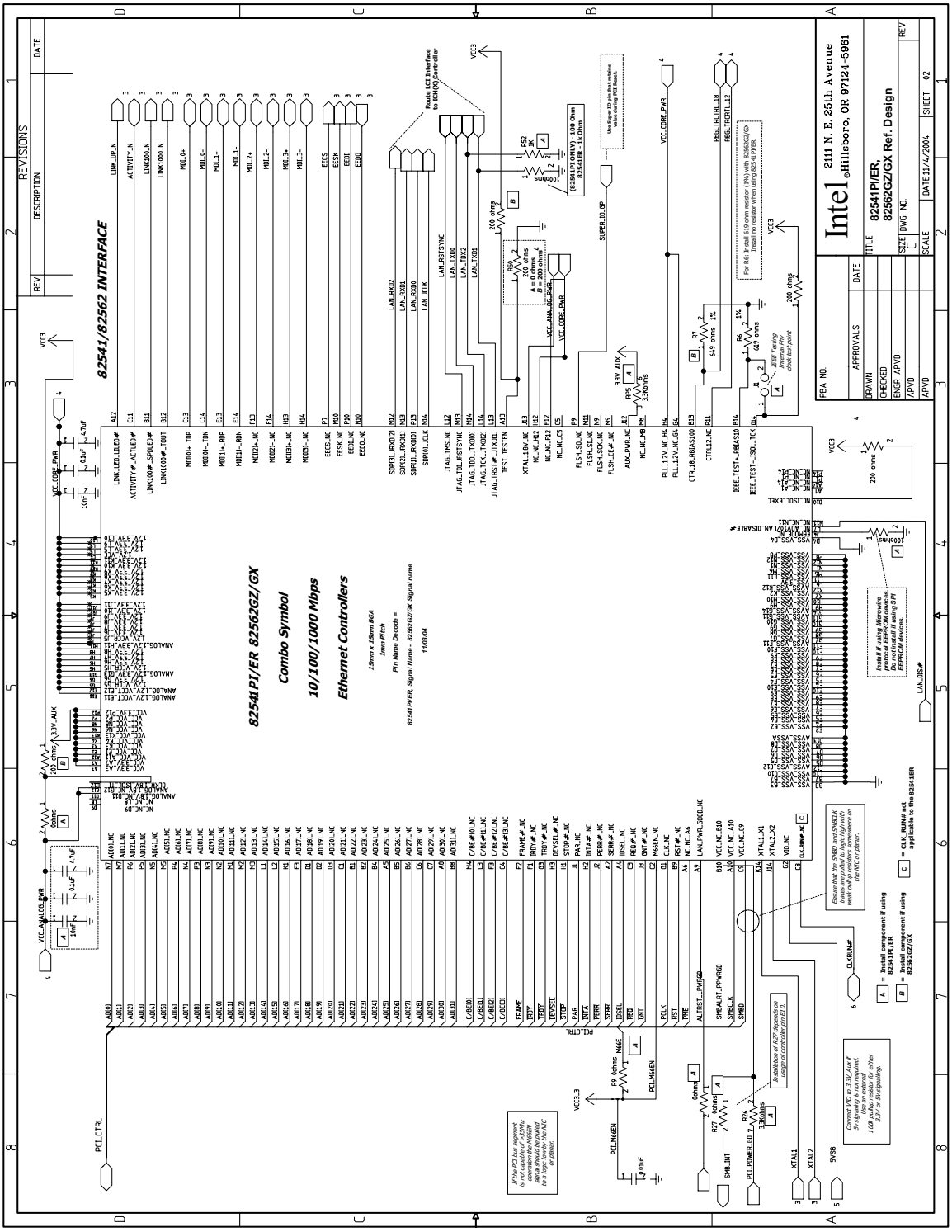
B = Install component if using 82562GZ/GX

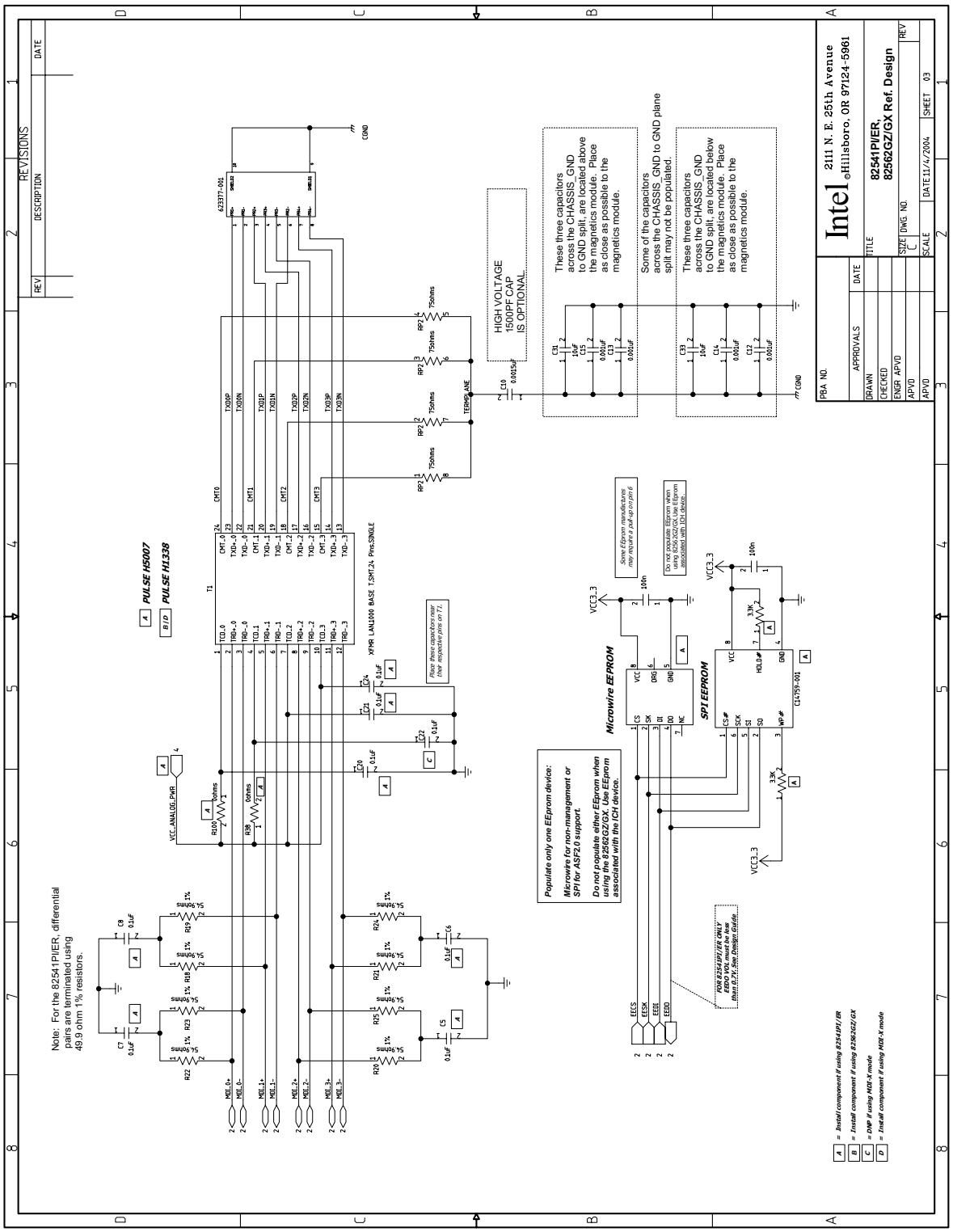
*** All components without flags are to be installed when using any selection of controllers.**

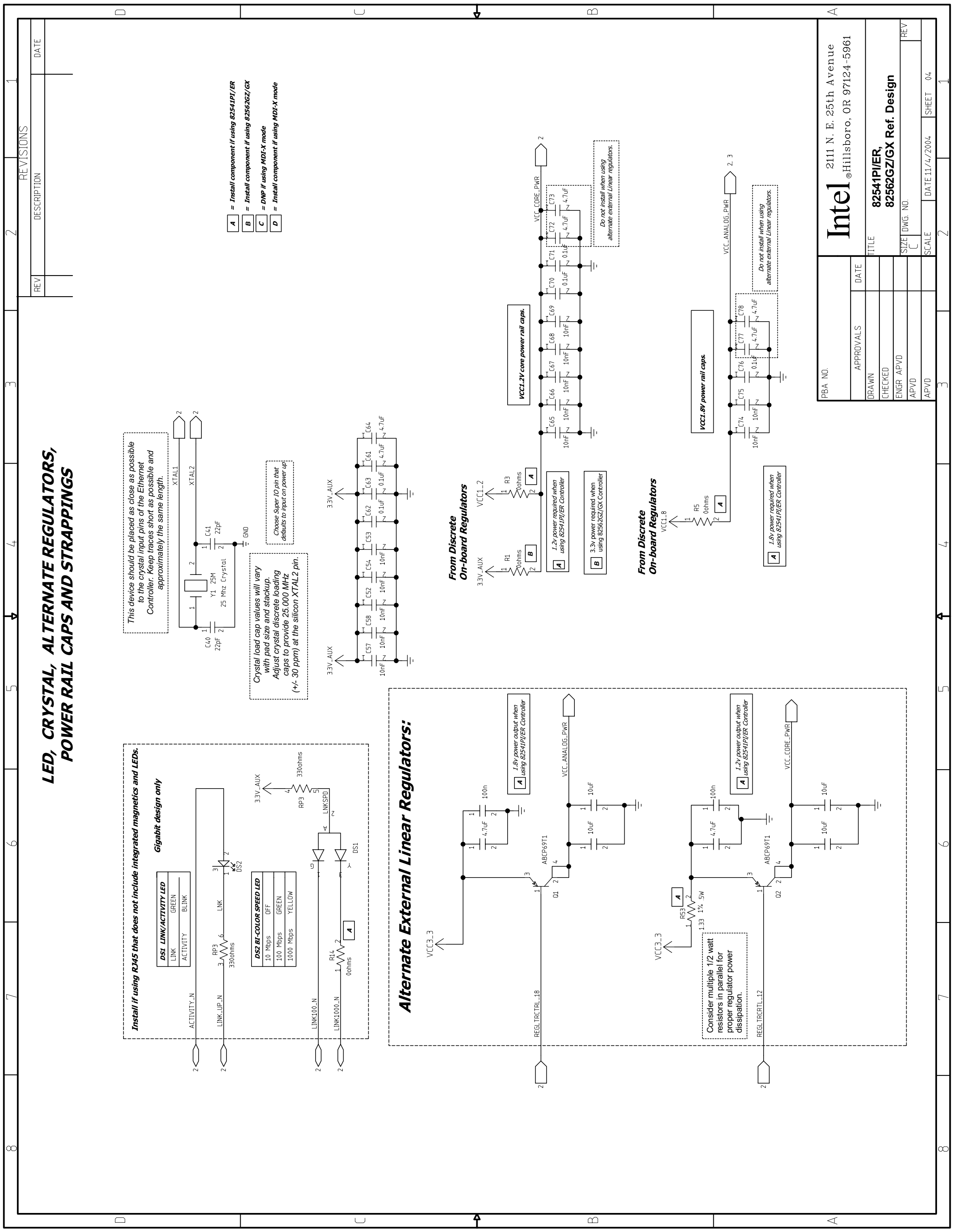
15mm x 15mm BGA

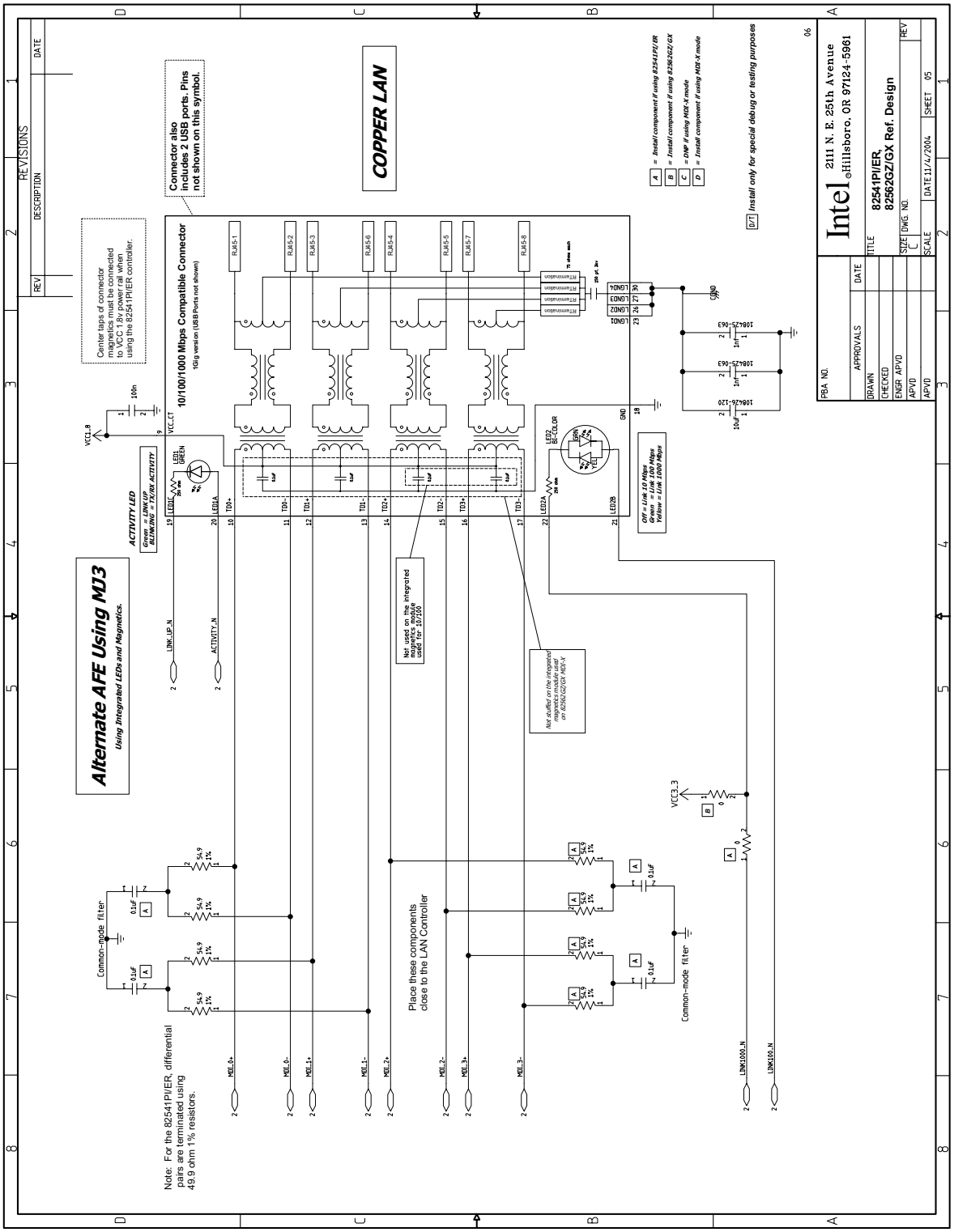
1mm pitch

PBA NO.		Intel 2111 N. E. 25th Avenue Hillsboro, OR 97124-5961		
APPROVALS	DATE	TITLE	82541PI/ER, 82562GZ/GX Ref. Design	
DRAWN		SIZE C	DWG. NO.	REV
CHECKED		SCALE	DATE 11/4/2004	SHEET 01 1 of 6
ENGR APVD				
APVD				
APVD				


82541/82562 INTERFACE
82541PI/ER 82562GZ/GX
Combo Symbol
10/100/1000 Mbps
Ethernet Controllers
19mm x 19mm BGA
1mm Pitch
Pin Name Decode =
82541PI/ER_Signal Name - 82562GZ/GX Signal name
1/103/04
PCI_CTRL
SMB_INT
PCI_POWER_GD
XTAL1
XTAL2
5VSB
CLKRUN#
LANDIS#
Intel
2111 N. E. 25th Avenue
Hillsboro, OR 97124-5961
82541PI/ER,
82562GZ/GX Ref. Design
APPROVALS
DRAWN
CHECKED
ENGR APVD
APVD
APVD
PBA NO.
SIZE
C
DWG. NO.
REV
SCALE
DATE 11/4/2004
SHEET 02


REVISIONS
REV
DESCRIPTION
DATE
PULSE H5007
PULSE H1338
T1
XFMR LAN1000 BASE T-SMT-24 PINS,SINGLE
HIGH VOLTAGE
1500PF CAP
(IS_OPTIONAL
These three capacitors across the CHASSIS_GND to GND split, are located above the magnetics module. Place as close as possible to the magnetics module.
Some of the capacitors across the CHASSIS_GND to GND plane split may not be populated.
These three capacitors across the CHASSIS_GND to GND split, are located below the magnetics module. Place as close as possible to the magnetics module.
Microwire EEPROM
SPI EEPROM
Populate only one EEprom device:
Microwire for non-management or SPI for ASF2.0 support.
Do not populate either EEprom when using the 82562GZ/GX. Use EEprom associated with the ICH device.
Note: For the 82541PI/ER, differential pairs are terminated using 49.9 ohm 1% resistors.
A = Install component if using 82541PI/ER
B = Install component if using 82562GZ/GX
C = DNP if using MDI-X mode
D = Install component if using MDI-X mode
Intel
2111 N. E. 25th Avenue
Hillsboro, OR 97124-5961
82541PI/ER,
82562GZ/GX Ref. Design
APPROVALS
DRAWN
CHECKED
ENGR APVD
APVD
APVD
SIZE
DWG. NO.
REV
SCALE
DATE 11/4/2004
SHEET 03


LED, CRYSTAL, ALTERNATE REGULATORS,
POWER RAIL CAPS AND STRAPPINGS
Alternate External Linear Regulators:
From Discrete On-board Regulators
VCC1.2V core power rail caps.
VCC1.8V power rail caps.
Consider multiple 1/2 watt resistors in parallel for proper regulator power dissipation.
Gigabit design only
Install if using RJ45 that does not include integrated magnetics and LEDs.
This device should be placed as close as possible to the crystal input pins of the Ethernet Controller. Keep traces short as possible and approximately the same length.
Crystal load cap values will vary with pad size and stackup. Adjust crystal discrete loading caps to provide 25.000 MHz (+/- 30 ppm) at the silicon XTAL2 pin.
Intel
2111 N. E. 25th Avenue
Hillsboro, OR 97124-5961
82541PI/ER,
82562GZ/GX Ref. Design


COPPER LAN
Alternate AFE Using MJ3
Using Integrated LEDs and Magnetics.
10/100/1000 Mbps Compatible Connector
Connector also includes 2 USB ports. Pins not shown on this symbol.
Place these components close to the LAN Controller
Common-mode filter
Note: For the 82541PI/ER, differential pairs are terminated using 49.9 ohm 1% resistors.
Intel
2111 N. E. 25th Avenue
Hillsboro, OR 97124-5961
82541PI/ER, 82562GZ/GX Ref. Design

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Appendix A Measuring LAN Reference Frequency Using a Frequency Counter

A.1 Background

To comply with IEEE specifications for 10/100 Mbps and 10/100/1000Base-T Ethernet LAN, the transmitter reference frequency must be correct and accurate within ±30 parts per million (ppm).

Most Intel LAN devices will operate properly with a 25.000 MHz reference crystal, provided it meets the recommended requirements for frequency stability, equivalent series resistance at resonance (ESR), and load capacitance.

Most circuits for series resonant crystals include two discrete capacitors (typically C1 and C2), with values between 5 pF and 36 pF.

The most accurate way to determine the appropriate value for the discrete capacitors is to install the approximately correct values for C1 and C2. Next, a frequency counter should be used to measure the transmitter reference frequency (or transmitter reference clock).

- If the transmitter reference frequency is more than 20 ppm below the target frequency, then the values for C1 and C2 are too big and should be decreased.
- If the transmitter reference frequency is more than 20 ppm above the target frequency, then the values for C1 and C2 are too small and should be increased.

This Appendix provides instructions and illustrations that explain how to use a frequency counter and probe to determine the Ethernet LAN device transmit center frequency. An example describing how to calculate the frequency accuracy of the measured and averaged center frequency with respect to the target center frequency is also included.

A.2 Required Test Equipment

- Tektronix CMC-251, or similar high resolution, digital counter
- Tektronix P6246, or similar high bandwidth, low capacitance (less than 1 pF) probe
- Tektronix 1103, or similar probe power supply or probe amplifier
- BNC, 50 Ω coaxial cable (less than 6 feet long)
- System with power supply and test software for the LAN circuit to be tested

A.3 Indirect Probing Method

The indirect probing test method is applicable foremost devices that support 100BASE-T. Since probe capacitance can load the reference crystal and affect the measured frequency, the preferred method is to use the indirect probing test method when possible.

Almost all Intel Ethernet controllers that support 1000BASE-T Ethernet can provide a buffered 125 MHz clock, which can be used for indirect probing of the transmitter reference clock. The buffered 125 MHz clock will be a 5X multiple of the crystal circuit's reference frequency (Figure 19).

Different LAN devices may require different register settings, to enable the buffered 125 MHz reference frequency. Please obtain the settings or instructions that are appropriate for the LAN controller you are using.

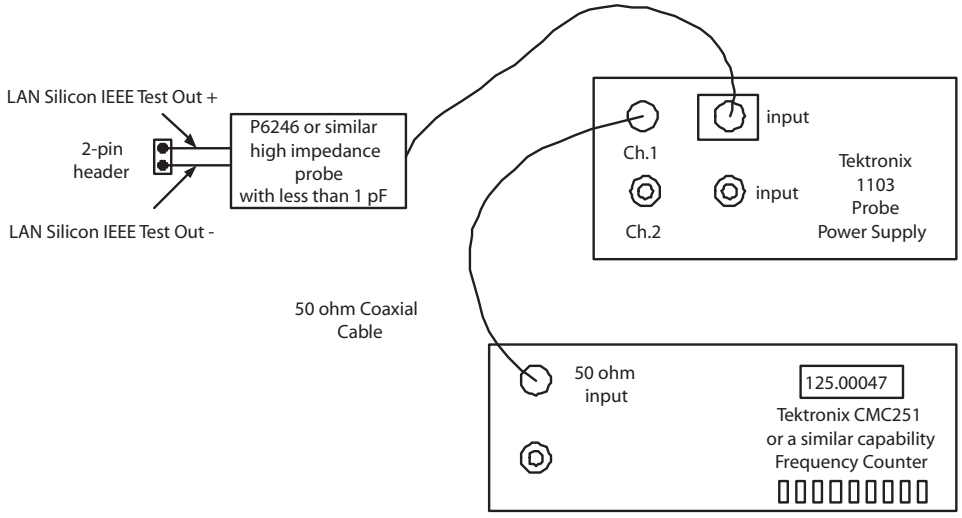

Figure 19. Indirect Probing Setup

A.4 Indirect Frequency Measurement and Frequency Accuracy Calculation Steps

1. Make sure the system BIOS has the LAN controller enabled.
2. Connect the test equipment as shown in Figure 19.
3. Using the appropriate controls for your model of high resolution digital counter, make sure it can display ~125.0000 MHz with at least four decimal places frequency resolution.
4. Enable the 125 MHz buffered reference clock.
5. Determine the center reference frequency as accurately as possible. This can be done by taking 30 to 50 different readings using the frequency counter and then calculating the average results of the readings.
6. Calculate the accuracy of the measured and averaged center frequency with respect to an ideal 125.0000 MHz reference frequency.

$$FrequencyAccuracy(ppm) = \frac{(x-y)}{(y/1000000)}$$

where x = Average measured frequency in Hertz and
y = Ideal reference frequency in Hertz

Example 1.

Given: The measured averaged center frequency is 124.99942 MHz (or 124,999,420 Hertz).

$$FrequencyAccuracy(ppm) = \frac{(124999420 - 125000000)}{(125000000/1000000)} = -4.64ppm$$

Example 2.

Given: The measured averaged center frequency is 125.00087 MHz (or 125,000,870 Hertz).

$$FrequencyAccuracy(ppm) = \frac{(125000870 - 125000000)}{(125000000 / 1000000)} = 6.96ppm$$

Note: The following items should be noted for an ideal reference crystal on a typical printed circuit board.

- If the transmitter reference frequency is more than 8 ppm below the target frequency, then the values for C1 and C2 are too big and they should be decreased. When tests are performed across temperature, it may be acceptable for the center frequency deviation to be a little greater than 8 ppm.
- If the transmitter reference frequency is more than 8 ppm above the target frequency, then the values for C1 and C2 are too small and they should be increased. When tests are performed across temperature, it may be acceptable for the center frequency deviation to be a little greater than 8 ppm.

A.5 Direct Probing Test Method, Applicable for Most 10/100 Devices (Devices that do NOT support 1000Base-T)

Because probe capacitance can load the reference crystal affecting the measured frequency, it is preferable to use a probe with less than 1 pF capacitance.

The probe should be connected between the X2 (or Xout) pin of the LAN device and a nearby ground. Typically, it is possible to connect the probe pins across one of the discrete load capacitors (C2 in Figure 20).

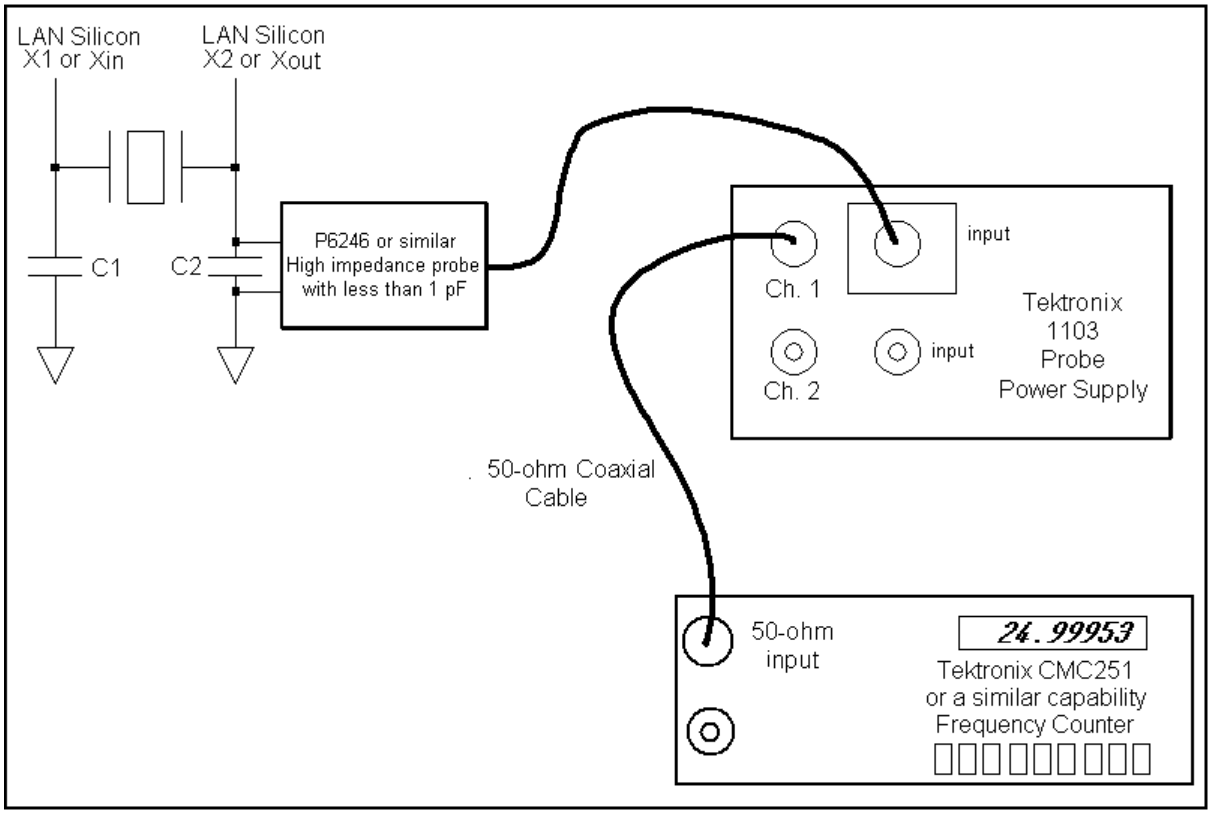

Figure 20. Direct Probing Method

A.6 Direct Frequency Measurement and Frequency Accuracy Calculation Steps

1. Make sure the system BIOS has the LAN controller enabled.
2. Connect the test equipment as shown in Figure 20.
3. Using the appropriate controls for your model of high resolution digital counter, make sure it can display ~25.0000 MHz with at least four decimal places frequency resolution.
4. Ensure the LAN circuits are powered.
5. Determine the center reference frequency as accurately as possible. This can be done by taking 30 to 50 different readings using the frequency counter and then calculating the average results of the readings.
6. Calculate the accuracy of the measured and averaged center frequency with respect to an ideal 25.0000 MHz reference frequency.

$$FrequencyAccuracy(ppm) = \frac{(x - y)}{(y / 1000000)}$$

where x = Average measured frequency in Hertz and
y = Ideal reference frequency in Hertz

Example 3.

Given: The measured averaged center frequency is 24.99963 MHz (or 24,999,630 Hertz).

$$FrequencyAccuracy(ppm) = \frac{(24999630 - 25000000)}{(25000000 / 1000000)} = -14.8ppm$$

Example 4.

Given: The measured averaged center frequency is 25.00027 MHz (or 25,000,270 Hertz).

$$FrequencyAccuracy(ppm) = \frac{(25000270 - 25000000)}{(25000000 / 1000000)} = 10.8ppm$$

Note: The following items should be noted for an ideal reference crystal on a typical printed circuit board.

- If the transmitter reference frequency is more than 8 ppm below the target frequency, then the values for C1 and C2 are too big and they should be decreased. When tests are performed across temperature, it may be acceptable for the center frequency deviation to be a little greater than 8 ppm.
- If the transmitter reference frequency is more than 8 ppm above the target frequency, then the values for C1 and C2 are too small and they should be increased. When tests are performed across temperature, it may be acceptable for the center frequency deviation to be a little greater than 8 ppm.