631xESB/632xESB I/O Controller Hub EEPROM Information Guide

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Revision History

Revision	Revision Date	Description
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0.25	Dec 2004	Initial release (Intel Secret).

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1.0 Introduction

A series of Intel® 631xESB/632xESB I/O Controller Hub EEPROMs are developed and validated as part of the 631xESB/632xESB validation effort. These dev_starter images represent a cross section of configurations that are available. Intel strongly recommends that designers use the dev_starter image that corresponds most closely with the desired configuration options. Dev_starter images have been fully validated with the reference design and can be used to ensure that the base functionality of a specific design is working as expected.

Dev_starter images are developed using generic modules (modules that expose a particular feature in a given EEPROM). Because some features are mutually exclusive, these modules are developed to preclude any generation of an EEPROM that has conflicting features. If a dev_starter image does not contain all the appropriate features that a specific design requires, please contact your Intel representative instead of modifying individual word or bit assignments to avoid conflicts.

The 631xESB/632xESB uses an EEPROM device for storing product configuration information. The EEPROM is divided into three general regions:

- **Hardware Accessed —** Loaded by the 631xESB/632xESB after power up, PCI reset de-assertion, a D3 to D0 transition, or a software commanded EEPROM read (CTRL_EXT.EE_RST).
- **Software Accessed —** Used by software only. These registers are listed in this document for convenience and are only for software and are ignored by the 631xESB/632xESB.
- **Firmware Accessed —** Used by BMC, PT, SPT, or ASF firmware. For more information about manageability, contact your Intel field representative.
  - Firmware Reset (all modes) - occurs after any of the following:

    LAN power up (LAN_PWR_GOOD assertion)

    Software-initiated firmware reset through a host command

    Software-initiated firmware reset through MAC CSRs (writing 40h and then 80h to HICR)

    Certain unrecoverable errors during manageability operation (RAM parity error, hardware watchdog timer expiration, etc.)
  - Software-Initiated EEPROM Reload (ASF mode only) - occurs after any of the following:

    Software-initiated assertion of the SWSM.WMNG bit while the manageability clock is off

    Software-initiated EEPROM reload through an ASF register (asserting FR_RST.FRC_EELD or FRC_FLUSH)

    Software-initiated ERPROM reload through a host command

    System state transition S0 to S5 while ASF register bit CTL_PWRLS is cleared

1.1 Reference Documents

- *82571/82572/631xESB/632xESB System Manageability* Application Note, Intel Corporation.
- *PCIe* Family of Gigabit Ethernet Controllers Software Developer's Manual*, Intel Corporation.

Note: Contact your Intel field representative for access to these documents.

1.2 EEPROM Device

The EEPROM interface supports Serial Peripheral Interface (SPI) mode 0 and expects the EEPROM to be capable of 2 MHz operation.

The 631xESB/632xESB is compatible with many sizes of 4-wire serial EEPROM devices. If flexibility mode functionality is desired (ASF, PT, SPT, or full BMC), up to a 256 Kb serial SPI can be used. All EEPROMs are accessed in 16-bit words (for compatibility with older designs) even though the EEPROM is designed to also accept 8-bit data accesses.

Note: Minimum EEPROM sizes: 32 Kb (no manageability image); 128 Kb (manageability image).

The 631xESB/632xESB automatically determines the address size to be used with the SPI EEPROM it is connected to and sets the *EEPROM Size* field of the EEPROM/Flash Control (EEC) and Data Register (EEC.EE_ADDR_SIZE; bit 10). Software uses this size to determine the EEPROM access method. The exact size of the EEPROM is stored within one of the EEPROM words.

Note: The different EEPROM sizes have two different numbers of address bits (8 bits or 16 bits). As a result, they must be accessed with a slightly different serial protocol. Software must be aware of this if it accesses the EEPROM using direct access.

Table 1. List of Recommended Manufacturers and Part Numbers

Density	Atmel PN	STM PN	Catalyst PN
8 Kb	AT25080AN-10SI-2.7	M95080WMN6T	CAT25C080S-TE13
16 Kb	AT25160AN-10SI-2.7	M95160WMN6T	CAT25C16S-TE13
32 Kb	AT25320AN-10SI-2.7	M95320WMN6T	CAT25C32S-TE13
64 Kb	AT25640AN-10SI-2.7	M95640WMN6T	CAT25C64S-TE13
128 Kb	AT25128AN-10SI-2.7	M95128WMN6T	CAT25CS128-TE13
256 Kb	AT25256AN-10SI-2.7	M95256WMN6T	

Note: Please visit the respective manufacturer’s website for any updated information regarding their EEPROM device.

1.3 Software Accesses

The 631xESB/632xESB provides two different methods for software access to the EEPROM. It can either use the built-in controller to read the EEPROM or access the EEPROM directly using the EEPROM's 4-wire interface.

Software can use the EEPROM Read register (EERD) to cause the 631xESB/632xESB to read a word from the EEPROM that the software can then use. To do this, software writes the address to read into the *Read Address* field (EERD.ADDR; bits 15:2) and simultaneously writes a 1b to the *Start Read* bit (EERD.START; bit 0). The 631xESB/632xESB then reads the word from the EEPROM, sets the *Read Done* bit (EERD.DONE; bit 1), and puts the data in the *Read Data* field (EERD.DATA; bits 31:16). Software can poll the EEPROM Read register until it sees the *Read Done* bit set, then use the data from the *Read Data* field. Any words read this way are not written to the 631xESB/632xESB's internal registers.

Software can also directly access the EEPROM's 4-wire interface through the EEPROM/Flash Control register (EEC). It can use this for reads, writes, or other EEPROM operations.

To directly access the EEPROM, software should follow these steps:

1. Write a 1b to the *EEPROM Request* bit (EEC.EE_REQ; bit 6).
2. Read the *EEPROM Grant* bit (EEC.EE_GNT; bit 7) until it becomes 1b. It remains 0b as long as the hardware is accessing the EEPROM.
3. Write or read the EEPROM using the direct access to the 4-wire interface as defined in the EEPROM/Flash Control & Data register (EEC). The exact protocol used depends on the EEPROM placed on the board and can be found in the appropriate datasheet.
4. Write a 0b to the *EEPROM Request* bit (EEC.EE_REQ; bit 6).

Finally, software can cause the 631xESB/632xESB to re-read part of the hardware accessed fields of the EEPROM (setting the 631xESB/632xESB's internal registers appropriately) by writing a 1b to the *EEPROM Reset* bit of the Extended Device Control register (CTRL_EXT.EE_RST; bit 13).

1.4 Signature and CRC Fields

The only way the 631xESB/632xESB can discover whether an EEPROM is present is by attempting to read the EEPROM. The 631xESB/632xESB first reads the EEPROM *Sizing & Protected* field Word at address 12h. The 631xESB/632xESB checks the signature value for bits 15 and 14. If bit 15 is 0b and bit 14 is 1b, it considers the EEPROM to be present and valid and reads additional EEPROM words and programs its internal registers based on the values read. Otherwise, it ignores the values it read from that location and does not read any other words.

Note: When the signature is not correct (the EEPROM is blank), it cannot be accessed by parallel access if its size is 512 bytes or smaller. As a result, the EEPROM should be accessed using the bit-bang mechanism.

1.5 Protected EEPROM Space

The 631xESB/632xESB provides a mechanism to enable different levels of protection for different areas in the EEPROM. All the protection mechanisms only affect host accesses. There are no restrictions on firmware accesses to the EEPROM. The EEPROM can be divided into three areas from a host point of view:

1. Read only area: This area usually contains the basic setup of the hardware and firmware.

Note: The PXE area (30h:3Fh) can be written by software even if it's part of the read only area.

2. Read/Write area: This area usually contains the host related structures.
3. Hidden area: This area usually contains secret data such as encryption keys or authentication signatures.

The protected areas cannot be accessed via the EEPROM registers in the CSR space. It can be accessed only by the management subsystem. For more information on the management subsystem, contact your Intel field representative.

The protection mechanisms are activated using the following fields in the EEPROM:

- Word 12h[3:0] defines the size of the hidden area. This area is located at the high addresses of the EEPROM. The size is fixed according to Table 2.
- Word 12h[4] enables all the protection mechanisms. As long as this bit is zero, all the areas are accessible to the host to read and write. It is highly recommended to set this bit *only* after the EEPROM image is stable and tested. Once this bit is set, word 12h becomes read-only to the software.
- Word 12h[15:14] indicates the presence of a programmed EEPROM. If these bits are not equal to 01b, it is assumed the EEPROM is not present or empty. All protection mechanisms are disabled in this case.
- Word 2Ch[14:0] – indicates the end of the read-only area. The read-only area starts at address 00h. This word points to the address of the last word in the read only area. If this word is 0h, then this protection mechanism is disabled.

Table 2. Size of EEPROM Hidden Block

Word 12h[3:0]	Hidden block size
0000b	No hidden block
0001b	2 bytes
0010b	4 bytes
0011b	8 bytes
0100b	16 bytes
0101b	32 bytes
0110b	64 bytes
0111b	128 bytes
1000b	256 bytes
1001b	512 bytes
1010b	1 KB
1011b	2 KB
1100b	4 KB
1101b	8 KB
1110b	16 KB
1111b	32 KB

Note: When software issues a burst to the EEPROM using the bit-bang mechanism and a burst starts at a non-protected area and ends inside the protected area, the entire burst is not performed even if protection was disabled. To remedy:

- Either no protection areas are defined in the EEPROM
- Software uses the parallel access mechanism
- The burst can be split into two bursts where the first burst ends at the boundary of the non-protected area

1.5.1 Initial EEPROM Programming

In most applications, initial EEPROM programming is done directly on the EEPROM pins. Nevertheless, it is desirable to enable existing software utilities (accessing the EEPROM via the host interface) to initially program the whole EEPROM without breaking the protection mechanism. Following a power-up sequence, the 631xESB/632xESB reads the hardware initialization words in the EEPROM. If the signature in word 12h does not equal 01b the EEPROM is assumed as non-programmed. There are two effects for non-valid signature:

- The 631xESB/632xESB stops reading EEPROM data and sets the relevant registers to default values.
- The 631xESB/632xESB enables access to any location in the EEPROM via the EEPROM CSR registers. Note that bit 4 in word 12h must not be set.

1.5.2 Activating the Protection Mechanism

Following ESB2 LAn initialization, it reads the EEPROM. It then turns on the protection mechanism if word 12h [15:14] contains a valid signature (equals 01b) and a hidden area with a non-zero size is defined (bit 4 in word 12h must be set). Once the protection mechanism is turned on, word 12h becomes write-protected and the area that is defined by word 12h becomes hidden (read/write protected). Note that the area defined by word 2Ch also becomes read only.

1.5.3 Non Permitted Accessing to Protected areas in the EEPROM

This section refers to EEPROM accesses via the EEC (bit banging) or EERD (parallel read access) registers. Following a write access to the write protected areas in the EEPROM, the hardware responds properly on the PCIe* bus, but does not initiate any access to the EEPROM. Following a read access to the hidden area in the EEPROM (as defined by word 12h), the hardware does not access the EEPROM and returns meaningless data to the host.

Note: Using bit banging, the SPI EEPROM can be accessed in a burst mode. For example, providing an opcode address and then reading or writing data for multiple bytes. The hardware inhibits an attempt to access the protected EEPROM locations even in burst accesses.

Software should not access the EEPROM in a Burst Write mode starting in a non protected area and continue to a protected one. In such a case, it is not guaranteed that the write access to any area ever takes place.

1.6 EEPROM Map

Table 3 lists the EEPROM map used in the 631xESB/632xESB.

Table 3. 631xESB/632xESB EEPROM Map (Sheet 1 of 3)

Word	Used By	15 8	7 0	Image Value	Function
00h 01h 02h	HW HW HW	Ethernet Address Byte 2 Ethernet Address Byte 4 Ethernet Address Byte 6	Ethernet Address Byte 1 Ethernet Address Byte 3 Ethernet Address Byte 5	IA(2,1) IA(4,3) IA(6,5)	LAN 0/1 (both)
03h 04h	SW	Compatibility High	Compatibility Low	0000h 0000h	both
05h	SW	EEPROM Major Version	EEPROM Minor Version	0000h	
06h 07h	SW	OEM Configuration		0000h 0000h	
08h 09h	SW	PBA, Byte 1 PBA, Byte 3	PBA, Byte 2 PBA, Byte 4		
0Ah	HW	Init Control 1			both
0Bh	HW	Subsystem ID			both
0Ch	HW	Subsystem Vendor ID			both
0Dh	HW	Device ID		1096h	LAN 0
0Eh	HW	Vendor ID			both

Table 3. 631xESB/632xESB EEPROM Map (Sheet 2 of 3)

Word	Used By	15 8	7 0	Image Value	Function
0Fh	HW	Init Control 2			both
10h	HW	Software Defined Pins Control		xxxxh	LAN 1
11h	HW	Device ID		1096h	LAN 1
12h	HW	EEPROM Sizing and Protected Fields			both
13h	HW	Management Enable Bits	Management Capabilities		both
14h	HW	Init Control 3		xxxxx	LAN 1
15h 16h	HW	Reserved			
17h	FW	Reserved			both
18h	HW	PCIe* Init Configuration 1			both
19h	HW	PCIe* Init Configuration 2			both
1Ah	HW	PCIe* Init Configuration 3			both
1Bh	HW	PCIe* Control			both
1Ch	HW	LEDCTL 1 3 Default			both
1Dh	HW	Reserved			both
1Eh	FW	Device REV ID			both
1Fh	FW	LEDCTL 0 2 Default			both
20h	HW	Software Defined Pins Control		xxxxh	LAN 0
21h	HW	Functions Control			MNG
22h	HW	LAN Power Consumption		280Ch	both
23h	HW	Management Hardware Config Control		xxxxh	both
24h	HW	Init Control 3		xxxxx	LAN 0
25h 26h	HW	Reserved			
27h	HW	CRID3 **Note:** CRID = Chipset Revision ID)	CRID2		both
28h	HW	CRID1			both
29h	HW	Hardware Setup		D080h	both
2Ah	HW	Reserved			
2Bh	HW	Parallel Flash Info		0004h	MNG
2Ch	HW	End of RO Area			both
2Dh	HW	LAN Boot Control			MNG
2Eh	HW	Function Control 2			MNG
2Fh		Vital Product Data (VPD) Pointer **Note:** OEM configurable, see Section 1.8 for detailed description.			
30h:35h	PXE	PXE Block			
. . .		. . .			

Table 3. 631xESB/632xESB EEPROM Map (Sheet 3 of 3)

Word	Used By	15 8	7 0	Image Value	Function
3Dh	SW	ISCSI Configuration Start Address			
3Eh		PXE Word			
3Fh		Software Checksum, Words 00h Through 3Fh			
40h:FFh		ASF/Pass Through/BMC Configuration Area			
100h/40h	HW	MNG D0 Power Consumption			MNG
101h/41h	HW	MNG D3 Power Consumption			MNG
102h/42h	HW	IDE Device ID		1084h	MNG
103h/43h	HW	Serial Port Device ID		1085h	MNG
104h/44h	HW	IPMI/KCS Device ID		1086h	MNG
105h/45h	HW	IDE Subsystem ID			MNG
106h/46h	HW	Serial Port Subsystem ID			MNG
107h/47h	HW	IPMI/KCS Subsystem ID			MNG
108h/48h		IDE Boot Control			IDE
109h/49h . . . 10Dh/ 4Dh		Reserved			
10Eh/4Eh		IPMI Device Class Code Low			MNG
10Fh/4Fh		IPMI Device Class Code High			MNG
110h/50h	HW	UHCI Device ID		1087h	PCIe*
111h/51h	HW	Reserved		1088h	PCIe*
112h/52h	HW	BT Device ID		1089h	PCIe*
113h/53h	HW	UHCI Subsystem ID		0000h	PCIe*
114h/54h	HW	Reserved		0000h	PCIe*
115h/55h	HW	BT Subsystem ID		0000h	PCIe*
116h/56h	HW	Reserved		0000h	PCIe*
117h/57h	HW	BT function Class Code Low		0702h	PCIe*
118h/58h	HW	BT function Class Code High		0Ch	PCIe*
119h/59h	HW	Mng D0 Power Consumption 2			PCIe*
11Ah/5Ah	HW	Mng D3 Power Consumption 2			PCIe*
11Bh/5Bh …	FW	Firmware and Software Area Structures Located According to Internal Firmware Pointers			both
		Secured …			

Note: If any of the MNG function (IDE, KT, KCS, UHCI, or BT) is enabled in the PCIe* config space, then the EEPROM size should be at least 256 bytes if the *PCICL* bit (word 13h, bit 15) is set, or 512 bytes if the *PCICL* bit is cleared.

1.7 Hardware Accessed Words

This section describes the EEPROM words that are loaded by the 631xESB/632xESB hardware. Most of these bits are located into a configuration registers. The words are only read and used if the signature field in the EEPROM Sizing and Protected Fields (word 12h) is valid.

Note: When changing the default value of a reserved bit, the 631xESB/632xESB behavior is undefined.

1.7.1 Ethernet Address (Words 02h:00h)

The Ethernet Individual Address (IA) is a 6-byte field that must be unique for each Ethernet port and each copy of the EEPROM image. The first three bytes are vendor specific. The value from this field is loaded into the Receive Address Register 0 (RAL0/RAH0) after resets and after being in D3.

The Ethernet address is loaded for LAN0 and bit 41, the LSB of the last Ethernet address byte, is inverted (bit 8 of Word 2) for LAN1.

Note: Note: A default value of FFFFh means the word is not used for any purpose.

For the purpose of this programming information guide, the IA byte numbering convention is listed in Table 4.

Table 4. IA Byte Ordering Convention

IA Byte / Value						
Vendor	**1**	**2**	**3**	**4**	**5**	**6**
Example 1 (Intel Original)	00	AA	00	Variable	Variable	Variable
Example 2 (Intel New)	00	A0	C9	Variable	Variable	Variable

1.7.2 Initialization Control Word 1 (Word 0Ah)

The first word read by the 631xESB/632xESB contains initialization values that:

- Set defaults for some internal registers
- Enable/disable specific features
- Determine which PCI configuration space values are loaded from the EEPROM

Table 5. Initialization Control Word 1 (Word 0Ah)

Bit	Name	Default	Description
15:12	Reserved	0011b	Reserved, must be set to 0011b
11	FRCSPD	0b	Default setting for the *Force Speed* bit in the Device Control register (CTRL[11]). The hardware default value is 0b.
10	FD	1b	Default setting for duplex setting. Mapped to Device Control register bit 0 (CTRL[0]) and Transmit Configuration Word register bit 5 (TXCW[5]). The hardware default value is 1b.

Table 5. Initialization Control Word 1 (Word 0Ah)

Bit	Name	Default	Description
9	LRST	0b	Default setting for link reset (CTRL[3]). Should be set to 0b for hardware to initiate Auto-Negotiation upon power up or assertion of PCIe* reset without driver intervention. The hardware default is value 0b.
8	Reserved	0b	Reserved. Should be set to 0b.
7:4	Reserved	0000b	Reserved. Should be set to 0000b.
3	Reserved	1b	Reserved. Should be set to 1b.
2	Reserved	0b	Reserved. Should be set to 0b.
1	Load Subsystem IDs	1b	This bit, when set to 1b, indicates that the 631xESB/632xESB is to load its PCIe* Subsystem ID and Subsystem Vendor IDs from the EEPROM (words 0Bh, 0Ch).
0	Load Vendor/ Device IDs	1b	This bit, when set to 1b, indicates that the 631xESB/632xESB is to load its PCIe* Vendor and Device IDs from the EEPROM (words 0Dh, 0Eh).

1.7.3 Subsystem ID (Word 0Bh)

If the Load Subsystem IDs in word 0Ah is set, this word is read in to initialize the Subsystem ID. The default value is 0h.

1.7.4 Subsystem Vendor ID (Word 0Ch)

If the Load Subsystem IDs in word 0Ah is set, this word is read in to initialize the Subsystem Vendor ID. the default value is 8086h.

1.7.5 Device ID (Word 0Dh, 11h)

If the *Load Vendor/Device IDs* bit in the Initialization Control Word 1 (0Ah) is set, this word is used to initialize the Device ID of LAN0 and LAN1 functions, respectively. Default values are listed in Table 6.

Table 6. Device ID (Word 0Dh, 11h)

Device ID	Product Code	Device Description
1096h	631xESB/ 632xESB	Copper: Dual Port 10/100/1000 Mb/s Ethernet controller integrated into the 631xESB/632xESB, copper interface with Intel I/O Acceleration Technology.
1097h	631xESB/ 632xESB	Fiber: Dual Port 1000 Mb/s Ethernet controller integrated into the 631xESB/ 632xESB; using fiber media from SerDes port with Intel I/O Acceleration Technology.
1098h	631xESB/ 632xESB	SerDes: Dual Port 1000 Mb/s Ethernet controller, 1000BASE-X backplane with Intel I/O Acceleration Technology.
10BB	631xESB/ 632xESB	Super Pass Through (SPT) SerDes: Single Port 10/100/1000 Mb/s Ethernet controller integrated into the 631xESB/632xESB, copper interface with Intel I/O Acceleration Technology.

1.7.6 Vendor ID (Word 0Eh)

If the Load Vendor/Device IDs in word 0Ah is set, this word is read in to initialize the Vendor ID. The default value is 8086h.

1.7.7 Initialization Control Word 2 (Word 0Fh)

This is the second word read by the 631xESB/632xESB and contains additional initialization values that:

- Set defaults for some internal registers
- Enable/disable specific features

Table 7. Initialization Control Word 2 (Word 0Fh)

Bit	Name	Default	Description
15	APM PME# Enable	0b	Initial value of the *Assert PME On APM Wakeup* bit in the Wake Up Control register (WUC.APMPME).
14	Reserved	0b	Reserved. Should be set to 0b.
13:12	Pause Capability	11b	Desired PAUSE capability for advertised configuration base page. Mapped to TXCW[8:7].
11	ANE	0b	Auto-Negotiation Enable. Mapped to TXCW[31].
10:8	Serial FLASH Size Indication	001b	Indicates Serial FLASH size. 000b = 64 KB 001b = 128 KB 010b = 256 KB 011b = 512 KB 100b = 1 MB 101b = 2 MB 110b = 4 MB 111b = 8 MB
7	Reserved	0b	Always set to 0b.
6	PHY Power Down Enable	1b	When set, enable the PHY to enter a low-power state. 0b = Disable. 1b = Enable.
5:4	Reserved	10b	Reserved. Should be set to 10b.
3	DMA Dynamic Clock Gating	0b	Always set to 0b.
2:1	Reserved	00b	Reserved. Should be set to 00b.
0	Reserved	0b	Reserved. Must be set to 0b.

1.7.8 Software Defined Pins Control (Word 10h, 20h)

These words are used to configure the initial settings of the Software Definable Pins.

Note: Word 10h is for LAN1 and Word 20h is for LAN0.

Table 8. Software Defined Pins Control (Word 10h, 20h)

Bit	Name	Default	Description
15	Reserved	0b	Reserved. Should be reset to 0b.
14	SDPDIR[2]	0b	SDP2 Pin - Initial Direction. This bit configures the initial hardware value of the *SDP2_IODIR* bit in the Extended Device Control Register (CTRL_EXT) following power up. This relates to the SDP0/SDP1 ports, respectively, for LAN 0 / LAN 1. 0b = Input. 1b = Output.
13:12	Reserved	00b	Reserved. Should be set to 00b.
11	LAN_DIS	0b	LAN Disable. When set to 1b, the appropriate LAN is disabled. 0b = Enable. 1b = Disable.
10	LAN _PCI_DIS	0b	LAN PCI Disable. When set to 1b the appropriate LAN PCI function is disabled. For example, the LAN is functional for MNG operation but is not connected to the host through PCIe*. 0b = Enable. 1b = Disable.
9	SDPDIR[1]	0b	SDP1 Pin - Initial Direction. This bit configures the initial hardware value of the *SDP1_IODIR* bit in the Device Control Register (CTRL) following power up. This relates to SDP0/SDP1 ports, respectively, for LAN 0/LAN 1. 0b = Input. 1b = Output.
8	SDPDIR0]	0b	SDP0 Pin - Initial Direction. This bit configures the initial hardware value of the *SDP0_IODIR* bit in the Device Control Register (CTRL) following power up. This relates to SDP0/SDP1 ports, respectively, for LAN 0/LAN 1. 0b = Input. 1b = Output.
7	Reserved	0b	Reserved. Should be reset to 0b.
6	SDPVAL[2]	0b	SDP2 Pin - Initial Output Value. This bit configures the initial power on value output on SDP2 (when configured as an output) by configuring the initial hardware value of the *SDP2_DATA* bit in the Extended Device Control Register (CTRL_EXT) after power up. This relates to SDP0/SDP1 ports, respectively, for LAN 0 / LAN 1.
5:3	Reserved	000b	Reserved. Bit 5 should be set to 0b. Bits 4:3 must be set to 0b.

Table 8. Software Defined Pins Control (Word 10h, 20h)

Bit	Name	Default	Description
2	D3COLD_ WAKEUP_ ADV_EN	1b	Configures the initial hardware default value of the *ADVD3WUC* bit in the Device Control Register (CTRL) following power up. 0b = Advertised. 1b = Not advertised.
1	SDPVAL[1]	0b	SDP1 Pin - Initial Output Value. This bit configures the initial power on value output on SDP1 (when configured as an output) by configuring the initial hardware value of the *SDP1_DATA* bit in the Device Control Register (CTRL) after power up. This relates to SDP0/SDP1 ports, respectively, for LAN 0/LAN1.
0	SDPVAL[0]	0b	SDP0 Pin - Initial Output Value. This bit configures the initial power on value output on SDP0 (when configured as an output) by configuring the initial hardware value of the *SDP0_DATA* bit in the Device Control Register (CTRL) after power up. This relates to SDP0/SDP1 ports, respectively, for LAN 0/LAN 1.

1.7.9 EEPROM Sizing and Protected Fields (Word 12h)

Note: The software driver can only read this word. It has no write access to this word through the EEC and EERD registers. Write access is possible only through an authenticated firmware interface.

Table 9. EEPROM Sizing and Protected Fields (Word 12h)

Bit	Name	Default	Description
15:14	Signature	01b	The Signature field indicates to the device that there is a valid EEPROM present. If the Signature field is not 01b, the other bits in this word are ignored, no further EEPROM read is performed and default values are used for the configuration space IDs.
13:10	EEPROM Size	1000b	These bits indicate the EEPROM actual size: 0000b = 128 B 0001b = 256 B 0010b = 512 B 0011b = 1 KB 0100b = 2 KB 0101b = 4 KB 0110b = 8 KB 0111b = 16 KB 1000b = 32 KB 1001b = 64 KB 1010b - 1011b = Reserved

Table 9. EEPROM Sizing and Protected Fields (Word 12h)

Bit	Name	Default	Description
9:5	Reserved	00000b	Reserved. Should be set to 000000b.
4	Enable EEPROM Protection	0b	If set, all EEPROM protection schemes are enabled. 0b = Disable. 1b = Enable.
3:0	HEPSize	0000b	Hidden EEPROM Block Size. 0000b = No hidden block. 0001b = 2 B. 0010b = 4 B. 0011b = 8 B. 0100b = 16 B. 0101b = 32 B. 0110b = 64 B. 0111b = 128 B. 1000b = 256 B. 1001b = 512 B. 1010b = 1 KB. 1011b = 2 KB. 1100b = 4 KB. 1101b = 8 KB. 1110b = 16 KB. 1111b = 32 KB.

1.7.10 Management Enable Byte (Word 13h, High Byte)

This byte contains information for firmware regarding enabled manageability functions. After this byte is updated, the software device driver should notify firmware of the change. If the manageability subsystem is in a mode where its host interface is active, then it should be done by the manageability host command. If the host interface is inactive, the software device driver should wake the manageability subsystem by asserting the *Wake Management Clock (WMNG)* bit in the Software Semaphore (SWSM) register.

Note: The Management Enable Byte word 13h must be set to 000b (no manageability) when using the ASF EEPROM image. It is the ASF agent's responsibility to set this field to 001b for ASF mode.

1.7.11 Management Enable Byte (Word 13h, Low Byte)

This byte is reserved for use by firmware.

1.7.12 Initialization Control 3 (Word 14h, 24h Lower Byte)

Table 10. Initialization Control 3 (Word 14h, 24h Lower Byte)

Bit	Name	Default	Description
7:1	Reserved	0h	Reserved. Should be set to 0h.
0	No PHY Reset for IDE	0b	No PHY reset when IDE or SOL is enabled. When asserted, this bit can prevent the PHY reset signal according to the CTRL BLK_PHY_RST value. This bit should be set to the same value at both words (14h, 24h) to reflect the same option to both LANs. 0b = PHY reset always asserted by a PCIe* reset. 1b = PHY reset blocked by firmware.

1.7.13 Initialization Control 3 (Word 14h, 24h Upper Byte)

This word controls general initialization values.

Note: Word 14h is used for LAN 1. Word 24 is used for LAN 0.

Table 11. Initialization Control 3 (Word 14h, 24h Upper Byte)

Bit	Name	Default	Description
15	Reserved	0b	Reserved. Should be set to 0b.
14	Reserved	1b	Reserved. Should be set to 1b.
13	LAN Flash Disable	1b	When set to 1b, disables the Flash logic. Flash access BAR in the PCI configuration space is disabled (parallel and serial flash). The Flash accessed by the LAN is defined in word 2Bh. 0b = Enable. 1b = Disable.
12	Interrupt Pin	LAN 0 (0b) LAN 1 (1b)	Controls the value advertised in the *Interrupt Pin* field of the PCI configuration header for a given port. A value of 0b, reflected in the *Interrupt Pin* field, indicates that the 631xESB/632xESB uses INTA#; a value of 1b indicates that the 631xESB/632xESB uses INTB#. 0b = INT# A. 1b = INT# B. **Note:** If a single port of the 631xESB/632xESB is enabled, this value is ignored and the *Interrupt Pin* field of the enabled port reports INTA# usage.
11	LAN Boot Enable	1b	A value of 1b disables the Expansion ROM BAR in the PCI configuration space. 0b = Enable. 1b = Disable.
10	APM Enable	1b	Initial value of *Advanced Power Management Wake Up Enable* in the Wake Up Control register (WUC.APME). 0b = APM wakeup disabled. 1b = APM wakeup enabled.
9:8	Link Mode	00b	Initial value of the *Link Mode* bits in the Extended Device Control register (CTRL_EXT.LINK_MODE), specifying which link interface and protocol is used by the 631xESB/632xESB. 00b = MAC operates in Kumeran mode. 01b = Reserved. 10b = Reserved. 11b = MAC operates in SerDes mode.

Table 12 lists the different combinations for bits 13 and 11 of word 14h, 24h.

Table 12. Bits 5 and 3 Combinations of Word 14h, 24h

Bit 13 (Flash Disable)	Bit 11 (Boot Disable)	Functionality (Active Window)
0b	0b	Flash and Expansion ROM BARs are active.
0b	1b	Flash BAR enabled Expansion ROM BAR disabled.
1b	0b	Flash BAR disabled Expansion ROM BAR enabled.
1b	1b	Flash and Expansion ROM BARs are disabled.

1.7.14 PCIe* Init Configuration Word 1 (Word 18h)

This word is used to set the defaults for some internal registers as well as enable/disable specific features.

Table 13. PCIe* Init Configuration Word 1 (Word 18h)

Bit	Name	Default	Description
15	Reserved	0b	Reserved. Should be set to 0b.
14:12	Reserved	110b (32 µs-64 µs)	Reserved. Should be set to 110b.
11:9	Reserved	110b (32 µs-64 µs)	Reserved. Should be set to 110b.
8:6	Reserved	011b (512 ns)	Reserved. Should be set to 011b.
5:3	Reserved	001b	Reserved. Should be set to 001b.
2:0	Reserved	001b	Reserved. Should be set to 001b.

1.7.15 PCIe* Init Configuration Word 2 (Word 19h)

This word is used to set defaults for some internal registers.

Table 14. PCIe* Init Configuration Word 2 (Word 19h)

Bit	Name	Default	Description
15:14	Reserved	00b	Reserved. Should be set to 00b.
13	DEVTYPE	1b	This bit defines the type of device as reported in the PCIe* Capability register of the IDE function. 1b = Legacy End Point. 0b = Native End Point. All other functions are defined as Native devices.
12	Reserved	1b	Reserved. Should be set to 1b.
11:8	Reserved	0011b	Reserved. Must be set to 0011b.
7:0	Reserved	FFh	Reserved. Should be set to FFh.

1.7.16 PCIe* Init Configuration Word 3 (Word 1Ah)

This word is used to set defaults for some internal registers.

Table 15. PCIe* Init Configuration Word 3 (Word 1Ah)

Bit	Name	Default	Description
15:13	Reserved	000b	Reserved. Should be set to 000b.
12	Cache Line Size	0b	This bit represents the cache line size. 0b = 64 bytes. 1b = 128 bytes. **Note:** The value loaded must be equal to the actual cache line size used by the platform as configured by system software.
11:10	Reserved	01b	Reserved. Always set to 01b.
9	IO Support	1b	I/O Support (I/O BAR Request). 0b = Not supported. 1b = Supported.
8	Max Packet Size	1b	This bit identifies the status of the default packet size. 0b = 128 bytes. 1b = 256 bytes.
7:6	Reserved	10b	Reserved. Must be set to 10b.
5:2	Reserved	0000b	Reserved. Should be set to 0000b.
1	Reserved	1b	Reserved. Should be set to 1b.
0	Reserved	0b	Reserved. Should be set to 0b.

1.7.17 PCIe* Control (Word 1Bh)

This word is used to configure the initial settings for the PCIe* default functionality.

Table 16. PCIe* Control

Bit	Name	Default	Description
15:14	Reserved	0b	Reserved. Must be set to 0b.
13	Reserved	1b	Reserved. Must be set to 1b.
12	Reserved	1b	Reserved. Should be set to 1b.
11	Reserved	0b	Reserved. Always set to 0b
10	Reserved	1b	Reserved. Always set to 1b.
9:7	Reserved	000b	Reserved. Always set to 000b.
6	Reserved	0b	Reserved. Should be set to 0b
5	Reserved	0b	Reserved. Should always be reset to 0b.
4:2	Reserved	000b	Reserved. Should be set to 000b.
1:0	Reserved	11b	Reserved. Should be set to 11b.

1.7.18 LED 1-3 Configuration Defaults (Word 1Ch)

This EEPROM word specifies the hardware defaults for the LEDCTL register fields controlling the LED1 (ACTIVITY indication) and LED3 (LINK_1000 indication) output behaviors.

Table 17. LED 1-3 Configuration Defaults (Word 1Ch)

Bit	Name	Default	Description
15	LED3 Blink	0b	Initial value of.LED3_BLINK field. 0b = Non-blinking. 1b = Blinking.
14	LED3 Invert[a]	0b	Initial value of LED3_IVRT field. 0b = None inverted (active-low output). 1b = Inverted (active-high output).
13	LED3 Blink Mode	0b[b]	LED3 Blink Mode. 0b = Blink at 200 ms on and 200 ms off. 1b = Blink at 83 ms on with no defined off time.
12	Reserved	0b	Reserved. Set to 0b.
11:8	LED3 Mode	0111b	Initial value of the LED3_MODE field specifying what event/state/pattern is displayed on the LED3 (LINK_1000) output. A value of 0111b (7h) indicates 1000 MB/s operation. See Table 18 for all available LED modes.
7	LED1 Blink	0b	Initial value of LED1_BLINK field. 0b = Non-blinking. 1b = Blinking.
6	LED1 Invert[a]	0b	Initial value of LED1_IVRT field. 0b = Not inverted (active-low output). 1b = Inverted (active-high output).
5	LED1 Blink Mode	0b[b]	LED1 Blink Mode. 0b = Blink at 200 ms on and 200 ms off. 1b = Blink at 83 ms on with no defined off time.
4	Reserved	0b	Reserved. Set to 0b.
3:0	LED1 Mode	0011b	Initial value of the LED1_MODE field specifying what event/state/pattern is displayed on the LED1 (ACTIVITY) output. A value of 0011b (3h) indicates the ACTIVITY state. See Table 18 for all available LED modes.

a. When LED Blink mode is enabled, the appropriate LED Invert bit should be set to 0b.
b. These bits are read from the EEPROM.

Note: Asserted = active low.

Table 18. LED Modes

Mode	Selected Mode	Source Indication
0000b	LINK_10/1000	Asserted when either 10 or 1000 Mb/s link is established and maintained.
0001b	LINK_100/1000	Asserted when either 100 or 1000 Mb/s link is established and maintained.
0010b	LINK_UP	Asserted when any speed link is established and maintained.
0011b	FILTER_ACTIVITY	Asserted when link is established and packets are being transmitted or received that passed MAC filtering.
0100b	LINK/ACTIVITY	Asserted when link is established AND when there is NO transmit or receive activity.
0101b	LINK_10	Asserted when a 10 Mb/s link is established and maintained.
0110b	LINK_100	Asserted when a 100 Mb/s link is established and maintained.
0111b	LINK_1000	Asserted when a 1000 Mb/s link is established and maintained.
1000b	SDP_MODE	LED activation is a reflection of the SDP signal. SDP0, SDP1, SDP2, SDP3 are reflected to LED0, LED1, LED2, LED3, respectively.
1001b	FULL_DUPLEX	Asserted when the link is configured for full duplex operation.
1010b	COLLISION	Asserted when a collision is observed.
1011b	ACTIVITY	Asserted when link is established and packets are being transmitted or received.
1100b	BUS_SIZE	Asserted when the device detects a 1 Lane PCIe* connection.
1101b	PAUSED	Asserted when the device's transmitter is flow controlled.
1110b	LED_ON	Always asserted.
1111b	LED_OFF	Always de-asserted.

NOTES:
1. The dynamic LED modes (Link/Activity and Activity) should be used with LED Blink mode enabled.
2. When LED Blink mode is enabled and CCM PLL is stopped, the blinking frequencies will be one-fifth of the stated rates.

1.7.19 Device Rev ID (Word 1Eh)

Table 19. Device Rev ID (Word 1Eh)

Bit	Name	Default	Description
15	Reserved	0b	Reserved. Should always be set to 0b.
14	Reserved	1b	Reserved. Must be set to 1b.
13:11	Reserved	000b	Reserved. Should be set to 000b.
10:8	Reserved	100b	Reserved. Always set to 100b.
7:0	DEVREVID	FFh	Device Rev ID. The actual device revision ID is the EEPROM value. Should be set to FFh.

1.7.20 LED 0-2 Configuration Defaults (Word 1Fh)

This EEPROM word specifies the hardware defaults for the LEDCTL register fields controlling the LED0 (LINK_UP) and LED2 (LINK_100) output behaviors.

Table 20. LED 0-2 Configuration Defaults (Word 1Fh)

Bit	Name	Default	Description
15	LED2 Blink	0b	Initial value of LED2_BLINK field. 0b = Non-blinking
14	LED2 Invert[a]	0b	Initial value of LED2_IVRT field. 0b = Not inverted (active-low output). 1b = Inverted (active-high output).
13	LED2 Blink Mode	0b[b]	LED2 Blink Mode. 0b = Blink at 200 ms on and 200 ms off. 1b = Blink at 83 ms on with no defined off time.
12	Reserved	0b	Reserved. Set to 0b.
11:8	LED2 Mode	0110b	Initial value of the LED2_MODE field specifying what event/state/pattern is displayed on the LED2 (LINK_100) output. A value of 0110b (6h) indicates 100 MB/s operation. See Table 18 for all available LED modes.
7	LED0 Blink	0b	Initial value of LED0_BLINK field. 0b = Non-blinking
6	LED0 Invert[a]	0b	Initial value of LED0_IVRT field. 0b = Not inverted (active-low output). 1b = Inverted (active-high output).
5	LED0 Blink Mode	0b[b]	Global Blink Mode. 0b = Blink at 200 ms on and 200 ms off. 1b = Blink at 83 ms on with no defined off time.
4	Reserved	0b	Reserved. Set to 0b.
3:0	LED0 Mode	0010b	Initial value of the LED0_MODE field specifying what event/state/pattern is displayed on the LED0 (LINK_UP) output. A value of 0010b (2h) indicates the LINK_UP state. See Table 18 for all available LED modes.

a. When LED Blink mode is enabled, the appropriate LED Invert bit should be set to 0b.
b. These bits are read from the EEPROM.

1.7.21 Functions Control (Word 21h)

Table 21. Functions Control (Word 21h)

Bit	Name	Default	Description
15	IDE Enable	0b	Enables the IDE Function in the PCI Configuration Space. When this bit is cleared, the IDE configuration space is not visible to the system. This bit is reflected in the FACTPS register. 0b = Disable. 1b = Enable.
14	Serial Enable[a]	0b	Enables the Serial Port Function in the PCI Configuration Space. When this bit is cleared, the Serial Port configuration space is not visible to the system. This bit is reflected in the FACTPS register. 0b = Disable. 1b = Enable.
13	IPMI/KCS Enable	0b	Enables the IPMI/KCS Function in the PCI Configuration Space. When this bit is cleared, the IPMI/KCS configuration space is not visible to the system. This bit is reflected in the FACTPS register. 0b = Disable. 1b = Enable.
12	LAN Function Select	0b	When both LAN ports are enabled and the LAN Function Sel equals 0b, LAN 0 is routed to PCI Function 0 and LAN 1 is routed to PCI Function 1. If the LAN Function Sel equals 1b, LAN 0 is routed to PCI Function 1 and LAN 1 is routed to PCI Function 0. This bit is reflected in the FACTPS[30] register.
11:10	IDE INT Select	11b	Default setup of the IDE Interrupt Pin. The value is loaded to the Interrupt Pin register in the PCI configuration space. Default value in INT D. 00b = INT A. 01b = INT B. 10b = INT C. 11b = INT D.
9:8	Serial INT Select	10b	Default setup of the Serial INT Interrupt Pin. The value is loaded to the Interrupt Pin register in the PCI configuration space. Default value in INT C. 00b = INT A. 01b = INT B. 10b = INT C. 11b = INT D.
7:6	IPMI/KCS INT Select	11b	Default setup of the IPMI/KCS Interrupt Pin. The value is loaded to the Interrupt Pin register in the PCI configuration space. Default value in INT D. 00b = INT A. 01b = INT B. 10b = INT C. 11b = INT D.
5:0	Reserved	0h	Reserved. Should be set to 0h.

a. SOL Enable Over PCI (bit 14) and over LPC are **mutually exclusive**. As a result, only one should be enabled in the EEPROM.

1.7.22 LAN Power Consumption (Word 22h)

This word is meaningful only if the EEPROM signature in word 0Ah is valid and Power Management is enabled.

Table 22. LAN Power Consumption (Word 22h)

Bit	Name	Default	Description
15:8	LAN D0a Power	0h	The value in this field is reflected in the PCI Power Management Data Register of the LAN functions for D0a power consumption and dissipation (*Data_Select* = 0 or 4). Power is defined in 100 mW units. The power includes also the external logic required for the LAN function.
7:5	Function 0 Common Power	0h	The value in this field is reflected in the PCI Power Management Data Register of function 0 when the *Data_Select* field is set to 8 (common function). The most significant bits in the Data Register that reflects the power values are padded with zeros.
4:0	LAN D3 Power	0h	The value in this field is reflected in the PCI Power Management Data Register of the LAN functions for D3 power consumption and dissipation (*Data_Select* = 3 or 7). Power is defined in 100 mW units. The power includes also the external logic required for the LAN function. The most significant bits in the Data Register that reflects the power values are padded with zeros.

1.7.23 Management Hardware Configuration Control (Word 23h)

This word contains the bits that direct special firmware behavior when configuring the PHY/ PCIe*/SerDes.

1.7.24 CRID3 (Word 27h, High)[1]

Table 23. CRID3 (Word 27h, High)

Bit	Name	Default	Description
15:8	CRID3	00h	CRID value read in case the key written in Rev ID is 3Dh.

1.7.25 CRID2 (Word 27h, Low)

Table 24. CRID2 (Word 27h, Low)

Bit	Name	Default	Description
7:0	CRID2	00h	CRID value read in case the key written in Rev ID is 2Dh.

1. CRID = Chipset Revision ID

1.7.26 CRID1 (Word 28h, High)

Table 25. CRID1 (Word 28h)

Bit	Name	Default	Description
15:8	CRID1	00h	CRID value read in case the key written in Rev ID is 1Dh.

1.7.27 631xESB/632xESB Specific Hardware Setup (Word 29h)

These bits are used for the 631xESB/632xESB specific hardware setups (read by autoload).

Table 26. 631xESB/632xESB Specific Hardware Setup (Word 29h)

Bit	Name	Default	Description
15	MSI En	1b	Enable MSI in all functions. Influence only the capability declaration in PCIe* config space. 0b = Disable. 1b = Enable.
14	Reserved	0b	Reserved. Should be set to 0b.
13	NMI Enable	1b	If enabled, allows sending IOCHK interrupts through SERIRQ. 0b = Disable. 1b = Enable.
12	SDP Pull Up Enable	1b	If set, all SDP pads wake up with pull up, until released by firmware. If cleared, SDP pads are without pull up. 0b = Disable. 1b = Enable.
11:10	Reserved	00b	Reserved. Should be set to 00b.
9	LAN 1 iSCSI Enable	0b	When set, LAN 1 class code is set to 010000h (SCSI). When reset, LAN 1 class code is set to 020000h (LAN).
8	LAN 0 iSCSI Enable	0b	When set, LAN 0 class code is set to 010000h (SCSI). When reset, LAN 0 class code is set to 020000h (LAN).
7:4	Reserved	8h	Reserved. Should be set to 8h.
3	Reserved	0b	Reserved. Should be set 0b.
2	Reserved	1b	Reserved. Should be set 1b.
1	Reserved	0b	Reserved. Should be set 0b.
0	Reserved	1b	Reserved. Should be set 1b.

1.7.28 Flash Info (Word 2Bh)

This word is read by the autoloader.

Table 27. Flash Info (Word 2Bh)

Bit	Name	Default	Description
15:12	Reserved	0000b	Reserved. Should be set to 0000b.
11:8	Expansion ROM BAR size	0000b	Expansion ROM BAR Size (LAN and IDE) 0000b = 64 KB. 0001b = 128 KB. 0010b = 256 KB. 0011b = 512 KB. 0100b = 1 MB. 0101b = 2 MB. 0110b = 4 MB. 0111b = 8 MB. 1000b = 16 MB. Others = 64 KB.
7	Reserved	0b	Reserved.
6:3	Pflash_size	0000b	Parallel Flash Size 0000b = 64 KB. 0001b = 128 KB. 0010b = 256 KB. 0011b = 512 KB. 0100b = 1 MB. 0101b = 2 MB. 0110b = 4 MB. 0111b = 8 MB. 1000b = 16 MB. Others = 64 KB
2	SW Flash Access Enable	1b	This bit sets the default of bit 7 in the FLA register. 0b = Disabled 1b = Enabled.
1	Mapped Flash in Host	0b	0b = Serial. 1b = Parallel.
0	Reserved	0b	Reserved. Should be set to 0b.

1.7.29 End of Read Only (RO) Area (Word 2Ch)

Defines the end of area in the EEPROM that is RO.

Table 28. End of RO Area (Word 2Ch)

Bit	Name	Default	Description
15	Reserved	0b	Reserved.
14:0	EORO_ area	0h	Defines the end of area in the EEPROM that is RO. The resolution is one word. Can be up to byte address FFFFh (7FFFh words). A value of 0h, indicates no RO area.

1.7.30 LAN Boot Control (Word 2Dh)

This word sets the defaults for some internal registers (read by autoload).

Table 29. LAN Boot Control (Word 2Dh)

Bit	Name	Default	Description
15	Reserved	0b	Reserved.
14:0	Flash Address	0h	Defines the base address of the LAN Boot expansion ROM in the physical FLASH device. Base address in bytes equals 256 times the field value.

1.7.31 Functions Control 2 (Word 2Eh)

Enables an override of the default BT function subsystem ID. This word is read by autoload and reflected in the FACTPS2 register.

Table 30. Functions Control 2 (Word 2Eh)

Bit	Name	Default	Description
15	UHCI Enable	0b	Enables the UHCI Function in the PCI Configuration Space. When this bit is cleared, the UHCI configuration space is not visible to the system. This bit is reflected in the FACTPS2 register. 0b = Disable. 1b = Enable.
14	Reserved	0b	Reserved. Must be set to 0b.
13	BT Enable	0b	Enables the BT Function in the PCI Configuration Space. When this bit is cleared, the BT configuration space is not visible to the system. This bit is reflected in the FACTPS2 register. 0b = Disable. 1b = Enable.
12:11	UHCI INT Select	10b	Default setup of the UHCI Interrupt Pin. The value is loaded to the Interrupt Pin register in the PCI configuration space. Default value in INT C. 00b = INT A. 01b = INT B. 10b = INT C. 11b = INT D.
10:9	Reserved	10b	Reserved. Should be set to 10b.

Table 30. Functions Control 2 (Word 2Eh)

Bit	Name	Default	Description
8:7	BT INT Select	11b	Default setup of the BT Interrupt Pin. The value is loaded to the Interrupt Pin register in the PCI configuration space. Default value in INT D. 00b = INT A. 01b = INT B. 10b = INT C. 11b = INT D.
6	UHCI Device Type	0b	0b = Declare UHCI function as type 0000b (native) PCIe* device. 1b = Declare UHCI as a type 0001b (legacy) PCIe* device.
5	UHCI Memory BAR Enable	1b	1b = Memory BAR enabled in function 5. 0b = Disabled.
4:0	Reserved	1Fh	Reserved.

1.7.32 iSCSI Boot Configuration Start Address (Word 3Dh)

Table 31. iSCSI Boot Configuration Start Address (Word 3Dh)

Bit	Name	Default	Description
15:0	Address	0h	Defines the word address in the EEPROM space of the iSCSI Boot Configuration where the module structure starts.

The iSCSI module structure is listed in Table 32.

Table 32. iSCSI Module Structure

Configuration Item	Max Size in Bytes	Comments
iSCSI Boot Signature	2	‘i’, ‘S’
Total Size	2	The structure size is stored in this field and will be set depending on the amount of free EEPROM space available. The total size of this structure, including variable length fields, must fit within this space.
Structure Version	1	Version of this structure. Should be set to 1.
Checksum	1	Holds 8 bit checksum of this structure.
Flags	2	01h → Enable iSCSI Boot 02h → Valid Configuration This should be set to 1b if the configuration information in this structure is valid and 0b otherwise. 03h → Enable DHCP 04h:05h → Configuration Prompt 0 = 0 Seconds 1 = 2 Seconds 2 = 3 Seconds 3 = 5 Seconds 06h:0Ah → # of Connection Retries

Table 32. iSCSI Module Structure

Configuration Item	Max Size in Bytes	Comments
Initiator IP	4	DHCP flag not set → This field should contain the configured IP address. DHCP flag set → This field should be set to 0b or save the last configured IP address.
Initiator Subnet Mask	4	DHCP flag not set → This field should contain the configured subnet mask. DHCP flag set → This field should be set to 0b or save the last configured subnet mask.
Target IP	4	IP address of iSCSI target.
Target Port	2	IP port of iSCSI target. Default is 3260.
CHAP Password	32	
CHAP User Name	255 + 1	Variable length field.
Initiator Name	255 + 1	Variable length field.
Target Name	255 + 1	Variable length field.

The maximum amount of boot configuration information that is stored is 834 bytes (417 words); however, the iSCSI boot implementation can limit this value in order to work with a smaller EEPROM.

Variable length fields are used to limit the total amount of EEPROM that is used for iSCSI boot information. Each field is preceded by a single byte that indicates how much space is available for that field. For example; if the Initiator Name field is being limited to 128 bytes, then it is preceded with a single byte with the value 128. The following field begins 128 bytes after the beginning of the Initiator Name field regardless of the actual size of the field. The variable length fields must be NULL terminated UNLESS they reach the maximum size specified in the length byte.

1.7.33 Manageability D0 Power Consumption (Word 100h/40h)

This word sets the defaults for some internal registers.

Table 33. Manageability D0 Power Consumption (Word 100h/40h)

Bit	Name	Default	Description
15	Reserved	1b	Reserved. Should be set to 0b.
14:10	IDED0PWR	00000b	Power Consumption value that is reflected in the Data Register of the IDE function in the Power Management registers at D0 power state. The same value is reflected in the Power consumption and Power dissipation.
9:5	SerialD0PWR	00000b	Power Consumption value that is reflected in the Data Register of the Serial Port function in the Power Management registers at D0 power state. The same value is reflected in the Power consumption and Power dissipation.
4:0	KCSD0PWR	00000b	Power Consumption value that is reflected in the Data Register of the IPMI/KCS function in the Power Management registers at D0 power state. The same value is reflected in the Power consumption and Power dissipation.

1.7.34 Manageability D3 Power Consumption (Word 101h/41hh)

This word is used to set the defaults for some internal registers.

Table 34. Manageability D3 Power Consumption (Word 101h/41h)

Bit	Name	Default	Description
15	Reserved	1b	Reserved. Should be set to 0b.
14:10	IDED3PWR	00000b	Power Consumption value that is reflected in the Data Register of the IDE function in the Power Management registers at D3 power state. The same value is reflected in the Power consumption and Power dissipation.
9:5	SerialD3PWR	00000b	Power Consumption value that is reflected in the Data Register of the Serial Port function in the Power Management registers at D3 power state. The same value is reflected in the Power consumption and Power dissipation.
4:0	KCSD3PWR	00000b	Power Consumption value that is reflected in the Data Register of the IPMI/KCS function in the Power Management registers at D3 power state. The same value is reflected in the Power consumption and Power dissipation.

1.7.35 IDE Device ID (Word 102h/42h)

Table 35. IDE Device ID (Word 102h/42h)

Bit	Name	Default	Description
15:0	IDEDID	1084h	IDE Device ID. If the Load Vendor/Device IDs bit in word 0Ah is set, this word is read in to initialize the Device ID of the IDE function.

1.7.36 Serial Port Device ID (Word 103h/43h)

Table 36. Serial Port Device ID (Word 103h/43h)

Bit	Name	Default	Description
15:0	SerialDID	1085h	Serial Port Device ID. If the Load Vendor/Device ID bit in word 0Ah is set, this word is read in to initialize the Device ID of the Serial Port function.

1.7.37 IPMI/KCS Device ID (Word 104h/44h)

This word is used to set the defaults for some internal registers.

Table 37. IPMI/KCS Device ID (Word 104h/44h)

Bit	Name	Default	Description
15:0	IPMIDID	1086h	IPMI/KCS Device ID. If the Load Vendor/Device IDs bit in word 0Ah is set, this word is read in to initialize the Device ID of the IPMI/KCS function.

1.7.38 IDE Subsystem ID (Word 105h/45h)

Table 38. IDE Subsystem ID (Word 105h/45h)

Bit	Name	Default	Description
15:0	IDESubID	0h	IDE Subvendor ID. If the Load Subsystem IDs bit in word 0Ah is set, this word is read in to initialize the IDE Subsystem ID.

1.7.39 Serial Port Subsystem ID (Word 106h/46h)

Table 39. Serial Port Subsystem ID (Word 106h/46h)

Bit	Name	Default	Description
15:0	SerialSubID	0h	Serial Port Subvendor ID. If the Load Subsystem IDs bit in word 0Ah is set, this word is read in to initialize the Serial Port Subsystem ID.

1.7.40 IPMI/KCS Subsystem ID (Word 107h/47h)

Table 40. IPMI/KCS Subsystem ID (Word 107h/47h)

Bit	Name	Default	Description
15:0	KCSSubID	0h	IPMI/KCS Subvendor ID. If the Load Subsystem IDs bit in word 0Ah is set, this word is read in to initialize the IPMI/KCS Subsystem ID.

1.7.41 IDE Boot Control (Word 108h/48h)

This word is used to set the defaults for some internal registers.

Table 41. IDE Boot Control (Word108h/48h)

Bit	Name	Default	Description
15	IDE Boot Disable	0b	Disable the IDE Boot expansion register in the PCI configuration space. When set, the IDE expansion ROM is an RO register with a zero value. By default, the IDE expansion ROM register is enabled. 0b = Enable. 1b = Disable.
14:0	Flash Address	0h	Defines the base address of the IDE Boot expansion ROM in the physical FLASH device. Base address in bytes equals 256 times the field value.

1.7.42 KCS Device Class Code Low (Word 10Eh/4Eh)

This word specifies the device class code of the KCS function. It can be either IPMI/KCS or ASF/KCS.

Table 42. KCS Device Class Code Low (Word 10Eh/4Eh)

Bit	Name	Default	Description
15:8	Class Code Middle Word.	07h	Middle byte of the IPMI class code. In IPMI/KCS mode, these bits are the Sub Class that equals 07h.
7:0	Class Code LSB	01h	LSB byte of the IPMI class code. In IPMI/KCS mode, these bits are the Interface code 01h for KCS.

1.7.43 KCS Device Class Code High (Word 10Fh/4Fh)

This word specifies the device class code of the KCS function. It can be either IPMI/KCS or ASF/KCS.

Table 43. KCS Device Class Code High (Word 10Fh/4Fh)

Bit	Name	Default	Description
15:8	Reserved	0b	Reserved.
7:0	Class Code MSB	0Ch	MSB byte of the IPMI class code. In IPMI/KCS mode, these bits are the Base Class code that equals 0Ch.

1.7.44 UHCI Device ID (Word 110h/50h)

This word allows for an override of the default UHCI function device ID, is read by autoload, and is reflected in the function 5 config space device ID field.

Table 44. UHCI Device ID (Word 110h/50h)

Bit	Name	Default	Description
15:0	UHCI ID	1087h	UHCI function device ID.

1.7.45 BT Device ID (Word 112h/52h)

This word allows for an override of the default BT function device ID, is read by autoload, and is reflected in function 7 config space device ID field.

Table 45. BT Device ID (Word 112h/52h)

Bit	Name	Default	Description
15:0	BT ID	1089h	BT function device ID.

1.7.46 UHCI Subsystem ID (Word 113h/53h)

This word allows for an override of the default UHCI function subsystem ID, is read by autoload, and is reflected in function 5 config space subsystem ID field.

Table 46. UHCI Subsystem ID (Word 113h/53h)

Bit	Name	Default	Description
15:0	UHCI ID	0000h	UHCI function subsystem ID.

1.7.47 BT Subsystem ID (Word 115h/55h)

This word allows for an override of the default BT function subsystem ID, is read by autoload, and is reflected in function 7 config space subsystem ID field

Table 47. BT Subsystem ID (Word 115h/55h)

Bit	Name	Default	Description
15:0	BT ID	0000h	BT function subsystem ID.

1.7.48 BT Device Class Code Low (Word 117h/57H)

This word specifies the device class code of the BT function.

Table 48. BT Device Class Code Low (Word 117h/57h)

Bit	Name	Default	Description
15:8	Class Code Middle Word	07h	Middle byte of the IPMI/BT class code.
7:0	Class Code LSB	02h	LSB byte of the IPMI class code.

1.7.49 BT Device Class Code High (Word 118h/58h)

This word specifies the device class code of the BT function.

Table 49. BT Device Class Code High (Word 118h/58h)

Bit	Name	Default	Description
15:9	Reserved	0b	Reserved.
7:0	Class Code MSB	0Ch	MSB byte of the IPMI class code. In IPMI/BT mode, these bits are the Base Class code that equals 0Ch.

1.7.50 MNG D0 Pwr Consumption 2 (Word 119h/59h)

This word is used to set the defaults for some internal registers.

Table 50. MNG D0 Pwr Consumption 2 (Word 119h/59h)

Bit	Name	Default	Description
15	Reserved	1b	Reserved.
14:10	UHCID0PWR	00000b	Power Consumption value that is reflected in the Data Register of the UHCI function in the Power Management registers at D0 power state. The same value is reflected in the Power consumption and Power dissipation.
9:5	Reserved	00000b	Reserved. Should be set to 00000b
4:0	BTD0PWR	00000b	Power Consumption value that is reflected in the Data Register of the IPMI/BT function in the Power Management registers at D0 power state. The same value is reflected in the Power consumption and Power dissipation.

1.7.51 MNG D3 Pwr Consumption 2 (Word 11Ah/5Ah)

This word is used to set the defaults for some internal registers (read by autoload).

Table 51. MNG D3 Pwr Consumption 2 (Word 11Ah/5Ah)

Bit	Name	Default	Description
15	Reserved	1b	Reserved.
14:10	UHCID3PWR	00000b	Power Consumption value that is reflected in the Data Register of the UHCI function in the Power Management registers at D3 power state. The same value is reflected in the Power consumption and Power dissipation.
9:5	Reserved	00000b	Reserved. Should be set to 00000b.
4:0	BTD3PWR	00000b	Power Consumption value that is reflected in the Data Register of the IPMI/BT function in the Power Management registers at D3 power state. The same value is reflected in the Power consumption and Power dissipation.

1.8 Vital Product Data Pointer (Word 2Fh)

This word can be used to point to a customer writable, 64-word Vital Product Data (VPD) block; a value of 0000h or FFFFh indicates that this field is not used.

1.9 Checksum Word Calculation (Word 3Fh)

The Checksum word (3Fh) should be calculated such that after adding all the words (00h-3Fh), including the Checksum word itself, the sum should be BABAh. The initial value in the 16-bit summing register should be 0000h and the carry bit should be ignored after each addition. This checksum is not accessed by the Ethernet controller. If CRC checking is required, it must be performed by software.

Note: Hardware does not calculate checksum word 3Fh during EEPROM write; it must be calculated by software independently and included in the EEPROM write data. Hardware does not compute a checksum over words 00h-0Fh during EEPROM reads in order to determine the validity of the EEPROM image; this field is provided strictly for software verification of EEPROM validity. All hardware configuration based on word 00h-0Fh content is based on the validity of the Signature field of EEPROM Initialization Control Word 1. Signature must be 01b.

1.10 ASF Controller Words

When the 631xESB/632xESB is in ASF mode, its ASF function reads the ASF section from the EEPROM. Word 44h contains a pointer to the base address and the ASF section is in relative offset B6h:00h. These words are read after power up (LAN_PWR_GOOD assertion), ASF Soft Reset (ASF FRC_RST), or software commanded ASF EEPROM read (ASF FRC_EELD).

Note: These words should be programmed by ASF configuration software. The value of the words from the factory should be all FFh.

1.10.1 ASF Words - Content

The interpretation of these words depends on the ASF Mode functionality.

1.10.2 ASF Words - EEPROM Checksum (CRC)

While the ASF EEPROM words are read, the 631xESB/632xESB also computes the ASF CRC word. Words in relative offset B7h:00h are included in the CRC calculation and compared against the CRC value present in relative word B7h. If the CRC values do not match, the 631xESB/632xESB does not overwrite the ASF configuration registers with the EEPROM values. Therefore, if the ASF CRC is invalid, hardware default values are initially present in ASF registers and any subsequent re-read of EEPROM leaves the ASF registers unchanged (from values current at the time of the EEPROM read).

The details of this CRC can be found at:

http://cell-relay.indiana.edu/cell-relay/publications/software/CRC/32bitCRC.tutorial.html.

1.11 Software Owned EEPROM Words Description

This section describes the software owned EEPROM words (words 09h:03h). Table 52 lists the software owned area and the sections that follow detail the specific words.

1.11.1 EEPROM Map for Words 09h:03h

Table 52. EEPROM Map for Words 09h:03h

Word	Used By	15 8	7 0	Image Value	LAN 0/1
03h	SW	Compatibility 1 High	Compatibility 1 Low	Server: 0410h Client: 0210h	LAN 0/1 (both)
04h	SW	OEM LED 2,3 Configuration	OEM LED 0,1 Configuration	FFFFh	
05h	SW	EEPROM Major Version	EEPROM Minor Version		
06h	SW	Reserved	Bit 3:0 for SerDes Amplitude Adjustment. Bit 7:4 Reserved		
07h	SW	Bit 15 for PHY Class A Enable, Bit 14:8 Reserved	Bit 7:0 Reserved		
08h 09h	SW	PBA, Byte 1 PBA, Byte 3	PBA, Byte 2 PBA, Byte 4		

1.11.2 Software Compatibility Word 1 (Word 03h)

Table 53. Software Compatibility Word 1 (Word 03h)

Bit	Name	Default	Description
15:12	Reserved	0b	Reserved. Should be set to 0b.
11	LOM	1b	1b = LOM. 0b = NIC.
10	Server	1b	1b = Server. 0b = Client.
9	Client	0b	1b = Client. 0b = Server.
8	OEM/Retail	0b	1b = OEM. 0b = Retail.
7:5	Reserved	000b	Reserved. Should be set to 000b.
4	SMBus Connected	1b	1b = SMBus connected. 0b = SMBus not connected.
3	Reserved	0b	Reserved. Should be set to 0b.
2	PCI Bridge	0b	1b = PCI bridge present. 0b = PCI bridge not present.
1:0	Reserved	00b	Reserved. Should be set to 00b.

1.11.3 OEM LED Configuration Word (Word 04h)

Table 54. OEM LED Configuration Word (Word 04h)

Bit	Name	Default	Description		
15:12	LED 3 Config	Fh	Value 1h 2h 3h 4h 5h 6h 7h 8h 9h	Mode 1 Default Default Default On On On Off Off Off	Mode 2 Default On Off Default On Off Default On Off
11:8	LED 2 Config	Fh	Same as LED 3 Config		
7:4	LED 1 Config	Fh	Same as LED 3 Config		
3:0	LED 0 Config	Fh	Same as LED 3 Config		

1.11.4 EEPROM Version Word (Word 05h)

Table 55. EEPROM Version Word (Word 05h)

Bit	Name	Default	Description
15:8	EEPROM Major Version		EEPROM major version number.
7:0	EEPROM Minor Version		EEPROM minor version number.

1.11.5 SerDes Adjustment (Word 06h)

This word is for platform / LOM specific usage. Word 06h is used to store the value for the SerDes amplitude adjustment.

Note: A default value of FFFFh means the word is not used for any purpose.

Table 56. SERDES Adjustment (Word 06h)

Bit	Name	Default	Description
15:8	Reserved		Default to 00h if word 06h is used (word value is not FFFFh).
7:4	Reserved		Default to 0h if word 06h is used (word value is not FFFFh).
3:0	SerDes amplitude		Value of the SERDES amplitude that is written into the PHY register if word 06h is used (i.e. word value is not FFFFh).

1.11.6 Software Configuration (Word 07h)

This word is for platform / LOM specific usage. This word is used to enable the PHY class A.

Note: A default value of FFFFh means this word is not used for any purpose.

Table 57. Software Configuration (Word 07h)

Bit	Name	Default	Description
15	PHY Class A Enable		If word value is not FFFFh: Bit 15 = 1b. Enable PHY class A. Bit 15 = 0b. Class AB mode (i.e. default PHY class mode).
14:1	Reserved		Reserved for future software configurations. Default to 0b if this word is used for any software configuration (i.e. the word value is not FFFFh).
0	Reserved		Default to 0b if this word is being used for any software configuration (i.e. the word value is not FFFFh).

1.11.7 PBA Number (Words 08h, 09h)

The nine-digit Printed Board Assembly (PBA) number used for Intel manufactured adapter cards are stored in a four-byte field. The dash itself is not stored, neither is the first digit of the 3-digit suffix, as it will always be 0b for the affected products. Note that through the course of hardware ECOs, the suffix field (byte 4) is incremented. The purpose of this information is to allow Customer Support (or any user) to identify the exact revision level of a product. Network driver software should not rely on this field to identify the product or its capabilities.

Table 58. PBA Number (Words 08h, 09h)

Product	PWA Number	Byte 1	Byte 2	Byte 3	Byte 4
Example	123456-003	12	34	56	03

Note: A default value of FFFFh means this word is not used for any purpose.

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